2N7002L 6V N-channel MOSFET

1 Features

- Low On-Resistantance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Operating Junction and Storage Temperature:
  - –65°C to +150°C
- 2kV Gate-Source ESD Rating

2 Applications

- Personal Electronics
- Building Automation
- Industrial Automation

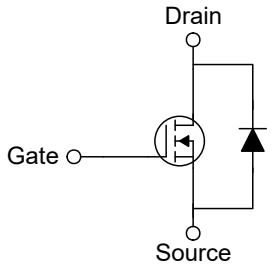
3 Description

This device is a N-channel Field-Effect Transistor in a plastic package. It has been designed to minimize the on-state resistance while maintaining fast switching performance.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
2N7002L	DBZ (SOT-23)	2.92mm × 2.37mm
	DCK (SOT-SC70)	2.10mm x 2.00mm
	DBV (SOT-23)	2.90mm x 2.80mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

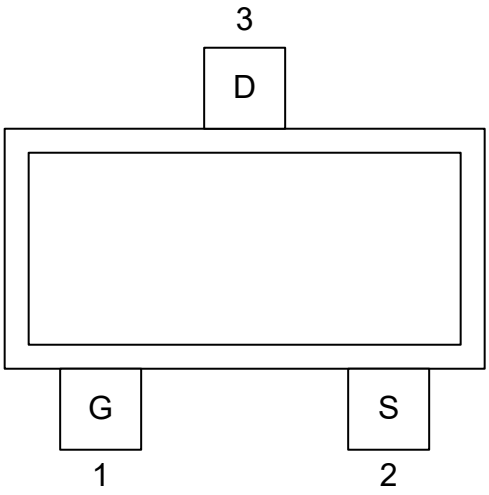


Figure 4-1. DBZ, DBV Package (3-Pin SOT-23) & DCK Package (3-pin SOT-SC70) Top View

Pin Functions

PIN		DESCRIPTION
NAME	DBZ, DBV, DCK	
G	1	Gate
S	2	Source
D	3	Drain

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DS}	Drain-to-Source Voltage		6	V
V_{GS}	Gate-to-Source Voltage		7	V
I_D	Drain Current T_A = 25°C		1.4	A
I_D	Drain Current T_A = 85°C		437	mA
I_{DM}	Pulsed Drain Current (t_p = 1s)		1.43	A
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-65	150	°C
I_S	Source Current		1.4	A
T_L	Lead Temp for Soldering Purpose		260	°C
ESD	Gate-Source / Gate-Drain ESD Rating		2000	V

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*

5.2 Thermal Information

THERMAL METRIC(1)		2N7002L DCK 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265.4	°C/W
$R_{\theta JC(top}$	Junction-to-case (top) thermal resistance	142.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	38.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	81.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.3 Electrical Characteristics

over operating free-air temperature (unless otherwise noted) (1)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS	$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0V, I_D = 1µA	9.7	11.7	13.7	V
	$V_{(BR)DSS}$ / T_J	Drain−to−Source Breakdown Voltage Temperature Coefficient			4		mV/℃
	I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 6V, T_J = 25℃			2.5	nA
	I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 6V, T_J = 125℃			0.26	µA
	I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = +7.0V			384	nA
ON CHARACTERISTICS	V_{GS}	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	0.4	0.7	0.95	V
	$V_{GS/(TH)}$	Negative Threshold Temperature Coefficient			-1.4		mV/℃
	R_{DSON}	Drain-to-Source On Resistance	V_{GS} = 5V, I_D = 64mA	1.2		3	Ω
	R_{DSON}	Drain-to-Source On Resistance	V_{GS} = 3.3V, I_D = 64mA	1.6		4.5	Ω
	G_{FS}	Forward	V_{DS} = 5V, I_D = 64mA	57		181	mS
CHARGES AND CAPACITANCE	C_{ISS}	Input Capacitance	V_{GS} = 0V, f = 1MHz, V_{DS} = 6V		4.8	5	pF
	C_{OSS}	Output Capacitance			7.4	8.5	
	C_{RSS}	Reverse Transfer Capacitance			5	5.5	
	$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 0 to 5V , V_{DS} = 6V (see figure)		0.034		nC
	$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 5V , V_{DS} = 6V (see figure)		0.007		
	Q_{GS}	Gate-to-Source Charge	V_{GS} = 0 to 5V , V_{DS} = 6V (see figure)		0.019		
	Q_{GD}	Gate-to-Drain Charge	V_{GS} = 0 to 5V , V_{DS} = 6V (see figure)		170		fC
SWITCHING CHARACTERISTIC	$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 5V, V_{DD} = 6V, R_G = 25Ω, R_D = 2.49kΩ			1.4	nS
	t_r	Rise Time				1.1	
	$t_{d(OFF)}$	Turn-Off Delay Time				7.0	
	t_f	Fall Time				55	
DRAIN-SOURCE DIODE CHARACTERISTICS	V_{SD}	Forward Diode Voltage	V_{GS} = 0V, I_S = 20mA, T_J = 25℃			0.97	V
			V_{GS} = 0V, I_S = 20mA, T_J = 85℃			0.93	

(1) All typical values are at T_A = 25°C.

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5.4 Typical Characteristics

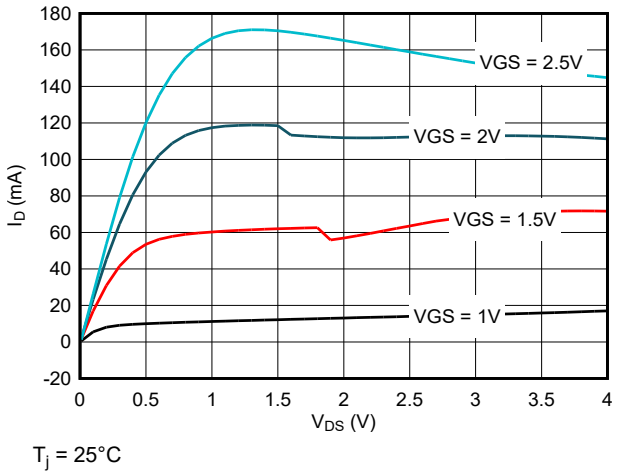


Figure 5-1. Output characteristics: drain current as a function of drain-source voltage

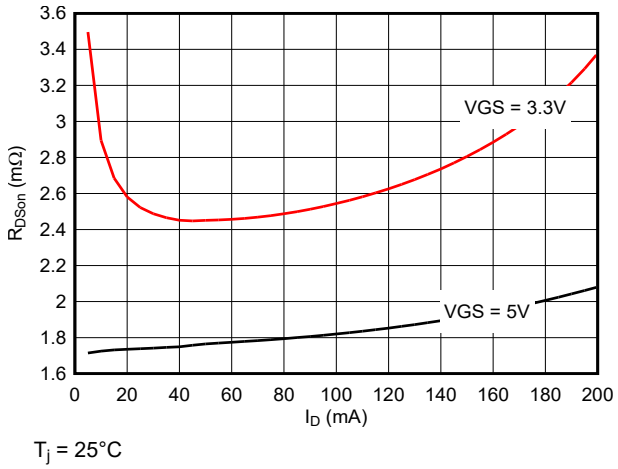


Figure 5-2. Drain-source on-state resistance as a function of drain current

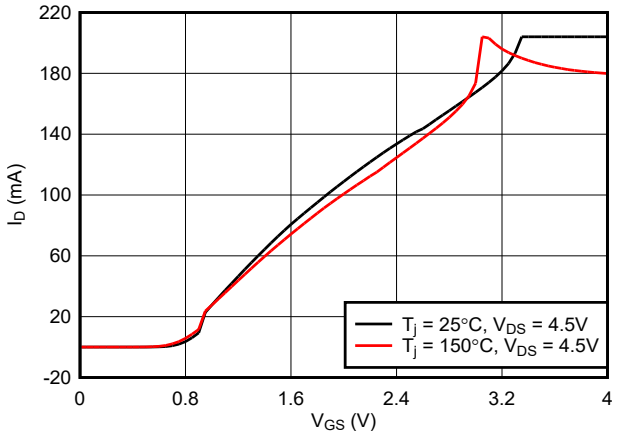


Figure 5-3. Transfer characteristics: drain current as a function of gate-source voltage

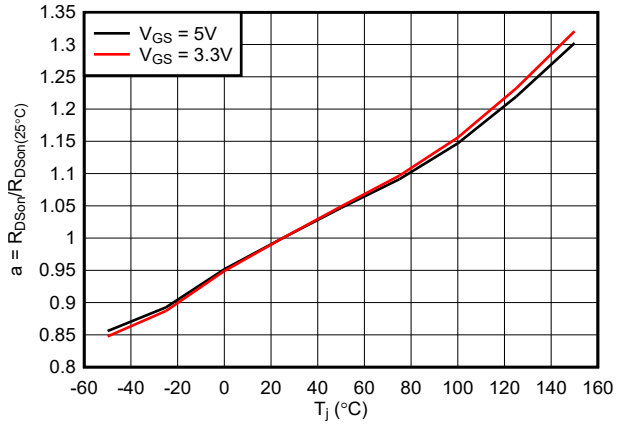


Figure 5-4. Normalized drain-source on-state resistance factor as a function of junction temperature

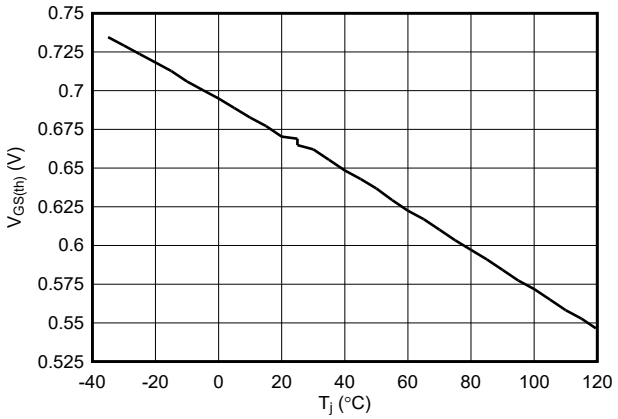


Figure 5-5. Gate-source threshold voltage as a function of junction temperature

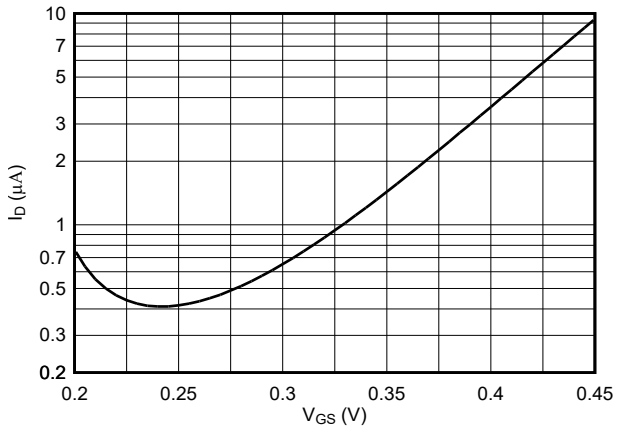
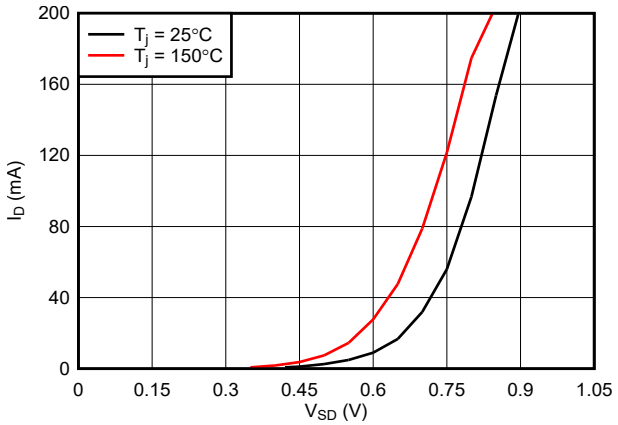


Figure 5-6. Sub-threshold drain current as a function of gate-source voltage

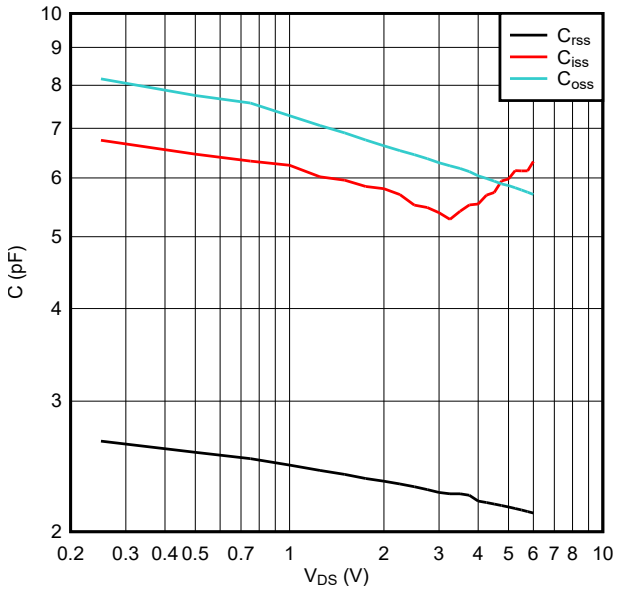
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5.4 Typical Characteristics (continued)



V_{GS} = 0V

Figure 5-7. Source current as a function of source-drain voltage



V_{GS} = 0V, f = 1MHz

Figure 5-8. Capacitances as a function of drain-source voltage

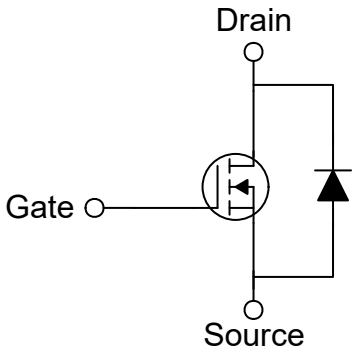
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6 Detailed Description

6.1 Overview

The 2N7002L is an N-channel enhancement-mode MOSFET designed for general purpose switching in low-voltage , low-current applications. In a typical low-side configuration, the source is tied to ground and the gate is driven by a logic-level signal. When the gate voltage exceeds the threshold voltage, the MOSFET turns on and provides a low on-resistance path between drain and source.

6.2 Functional Block Diagram



6.3 Feature Description

The 2N7002L is a voltage-controlled N-channel MOSFET in which drain-to-source conduction is controlled by the applied gate-to-source voltage. When the gate-to-source voltage exceeds the gate threshold voltage, a conduction channel is formed between the drain and source terminals. The channel resistance decreases as the gate-to-source voltage increases.

When the gate-to-source voltage is below the threshold voltage, the drain-to-source path presents a high impedance and limits current flow to leakage levels. The gate draws very little steady-state current, allowing the device to be controlled directly by logic-level signals. The relatively small gate charge and parasitic capacitances support switching operation.

When the device is turned on, how much current flows and which direction it flows depend on the voltages at the drain and source pins and on the other components connected in the circuit, such as pull-up or pull-down elements. When the device is turned off, an internal diode may still allow current to flow in one direction, depending on the voltage across the device, and this behavior should be considered when designing the circuit.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the device.

Table 6-1. Function Table

MODE	DESCRIPTION
OFF	V_{GS} < threshold; device does not conduct
ON	V_{GS} > threshold; device conducts

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The 2N7002L device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages. In the below example, the System Controller drives the gate of the 2N7002L. When the controller outputs a high logic level, the MOSFET turns on and pulls the EN pin of the system device low. When the controller output is low, the MOSTFET turns off and the pull-up resistor brings the EN pin high to 5V. This creates a open-drain style interface for level shifting or for driving enable signals at a higher voltage than the controller's logic domain.

7.2 Typical Applications

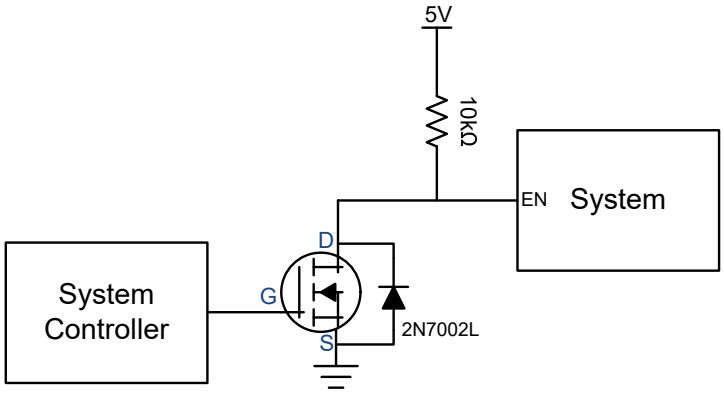


Figure 7-1. Typical Application using 2N7002L

7.2.1 Design Requirements

For proper operation of the 2N7002L, the design must remain within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables.

7.2.2 Detailed Design Procedure

Designing with the 2N7002L requires selecting appropriate operating conditions for gate drive, load current, and switching behavior while ensuring all parameters remain within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables.

1. Select the operating V_{DS}: ensure the supply voltage applied to the drain does not exceed the abs max ratings.
2. Choose a valid V_{GS}: use a logic-level gate voltage that falls within the recommended V_{GS} limits.
3. Confirm load current capability: make sure the drain current is within the device's continuous current and thermal capabilities.
4. Check switching capabilities: verify that the gate-drive strength and switching frequency are compatible with the device's gate charge and capacitances.

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8 Power Supply Recommendations

Operate the 2N7002L within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables. Use a 5V drain supply, and ensure that V_{DS} never exceeds 6V, including during transient events. Drive the gate from logic rails (1.8V, 3.3V, or 5V) and ensure the V_{GS} never exceeds 7V under any condition. Place decoupling capacitors near the device or load to reduce switching-related voltage spikes.

9 Layout

9.1 Layout Guidelines

Minimize trace lengths on the drain, source, and gate connections to reduce parasitic inductance and switching noise.

- Route the gate-drive signal away from noisy switching nodes to prevent coupling.
- Provide adequate copper area on the source or drain pads for thermal dissipation.
- If switching small inductive loads, place any flyback or clamp components close to the device to minimize transient stress.

9.2 Layout Example

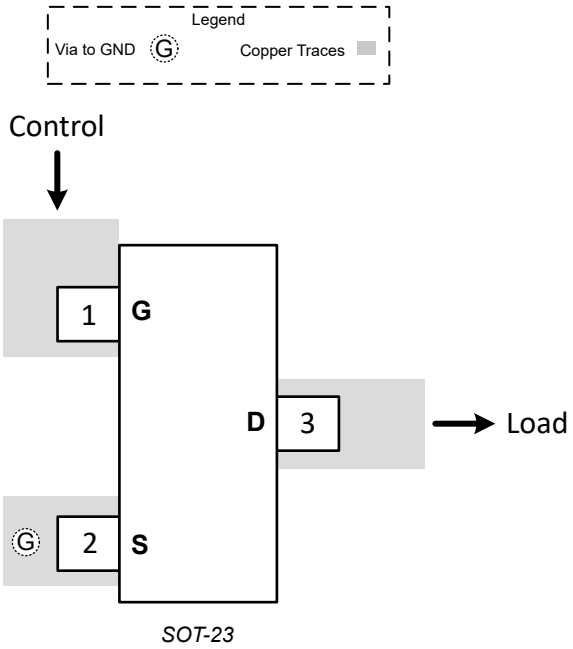


Figure 9-1. Example Layout for the SOT-23 or SOT-SC70 Package

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Designing and Manufacturing with TI's X2SON Packages*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2025) to Revision A (January 2026) — **Page**

- Updated data sheet status from *Advanced Information* to *Production Data* 1
- Added Thermal Information..... 4

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
2N7002LDBVR	Active	Production	SOT-23 (DBV) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	
2N7002LDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N7L
2N7002LDCKR	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2N7
P2N7002LDBZR	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF 2N7002L :

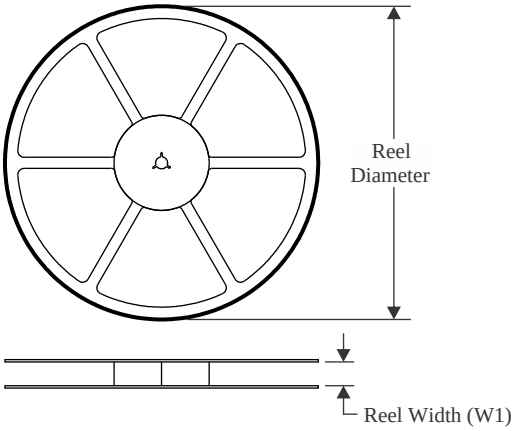
- Automotive : 2N7002L-Q1

NOTE: Qualified Version Definitions:

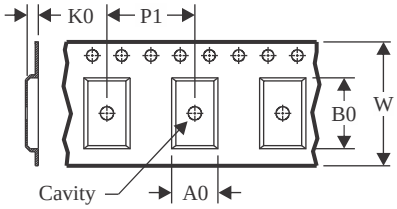
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

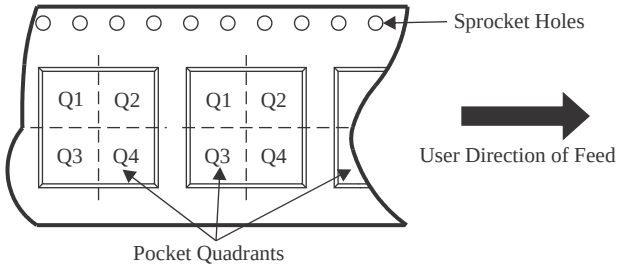


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

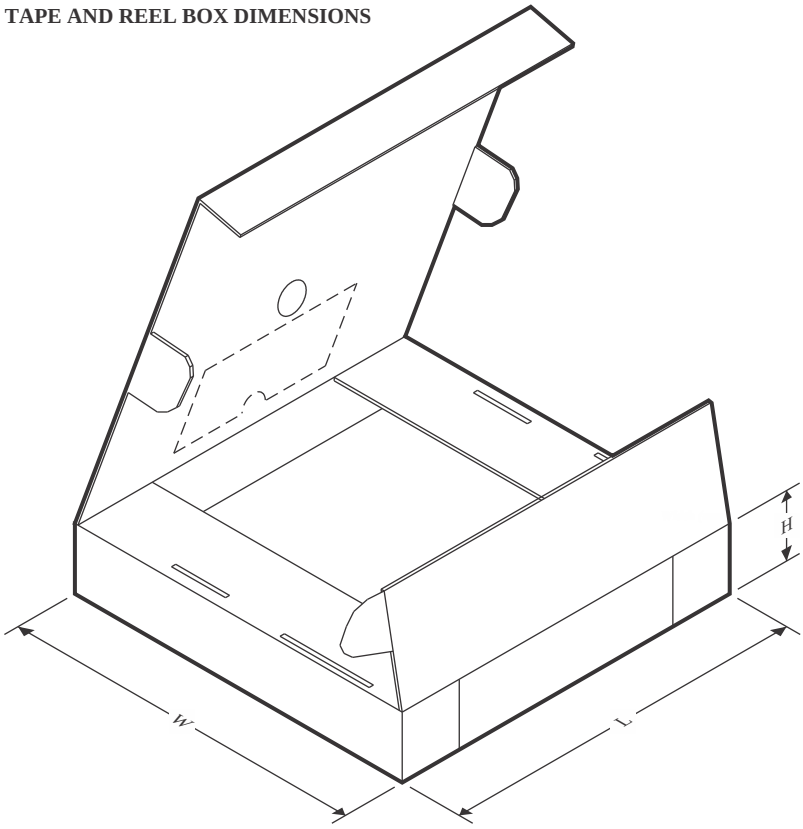
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2N7002LDBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
2N7002LDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
2N7002LDCKR	SC70	DCK	3	3000	180.0	8.4	2.3	2.75	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

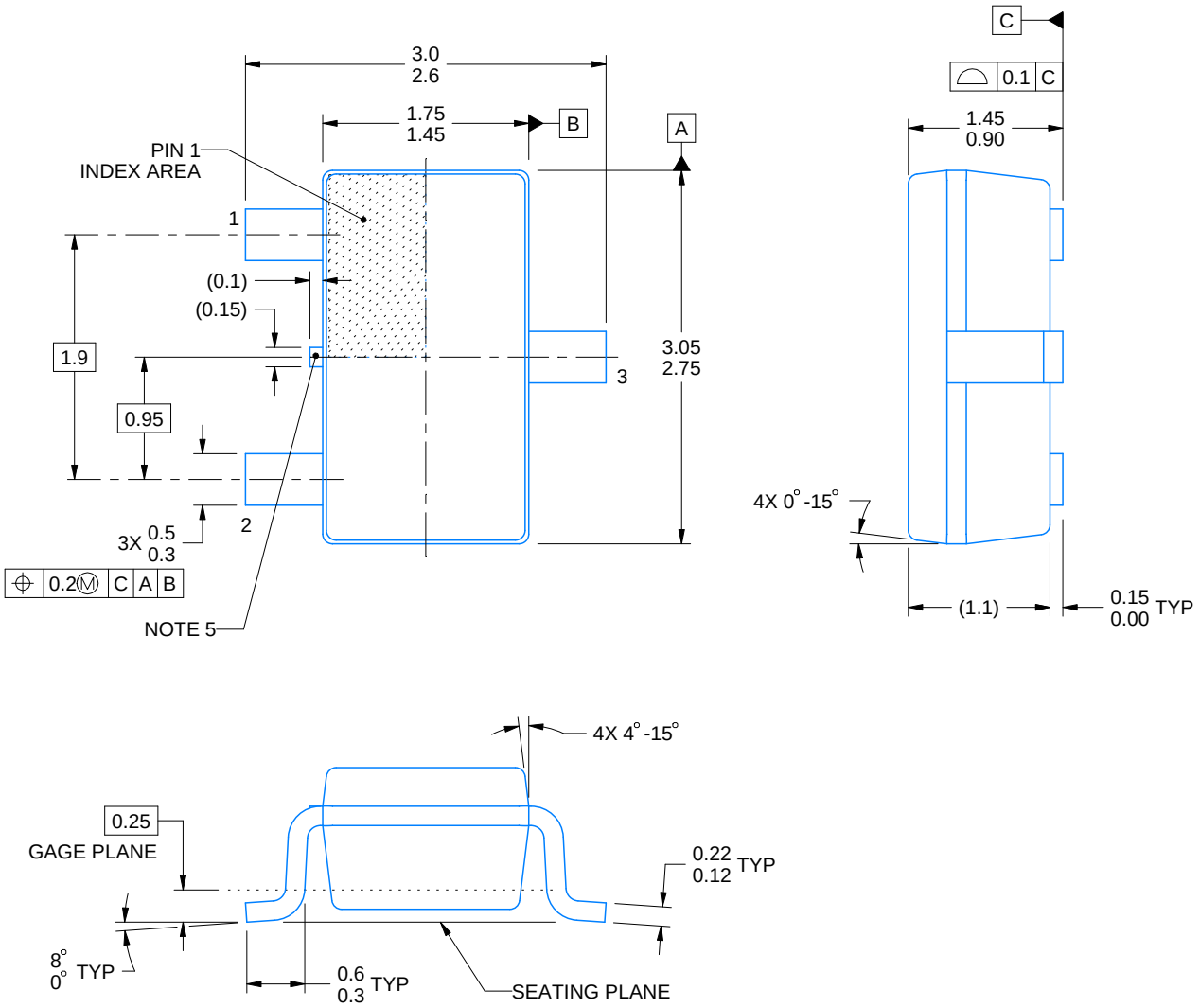
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2N7002LDBVR	SOT-23	DBV	3	3000	190.0	190.0	30.0
2N7002LDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
2N7002LDCKR	SC70	DCK	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0003A

SOT-23 - 1.45 mm max height

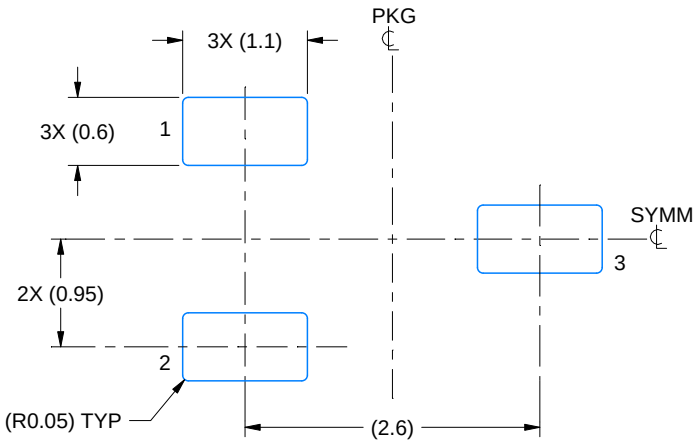
SMALL OUTLINE TRANSISTOR



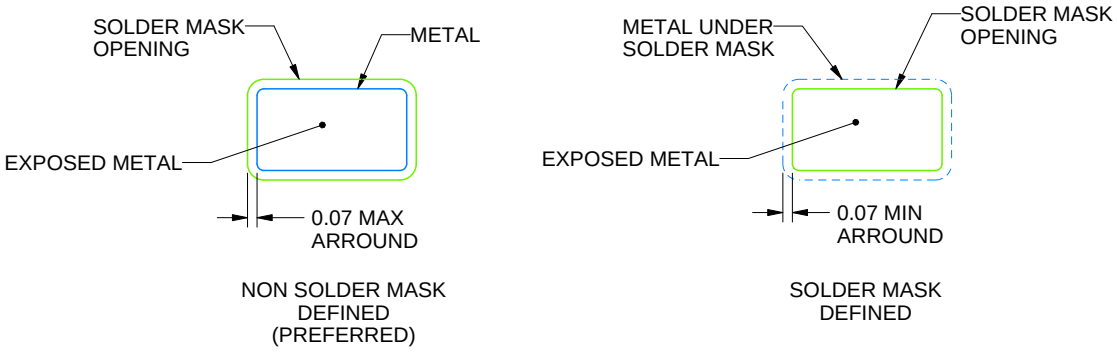
4220743/D 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

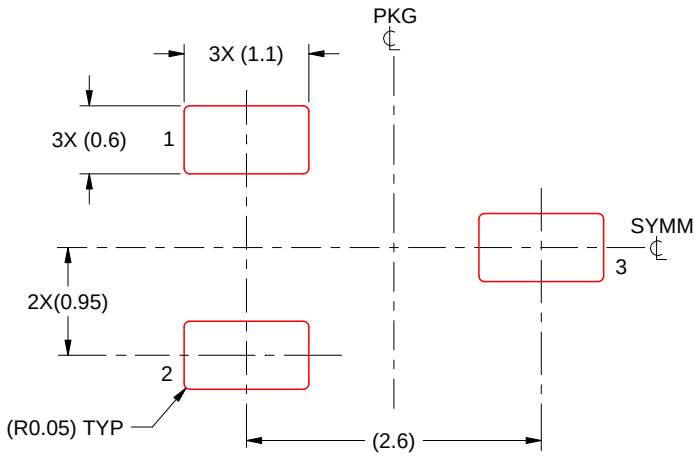


SOLDER MASK DETAILS

4220743/D 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220743/D 08/2024

NOTES: (continued)

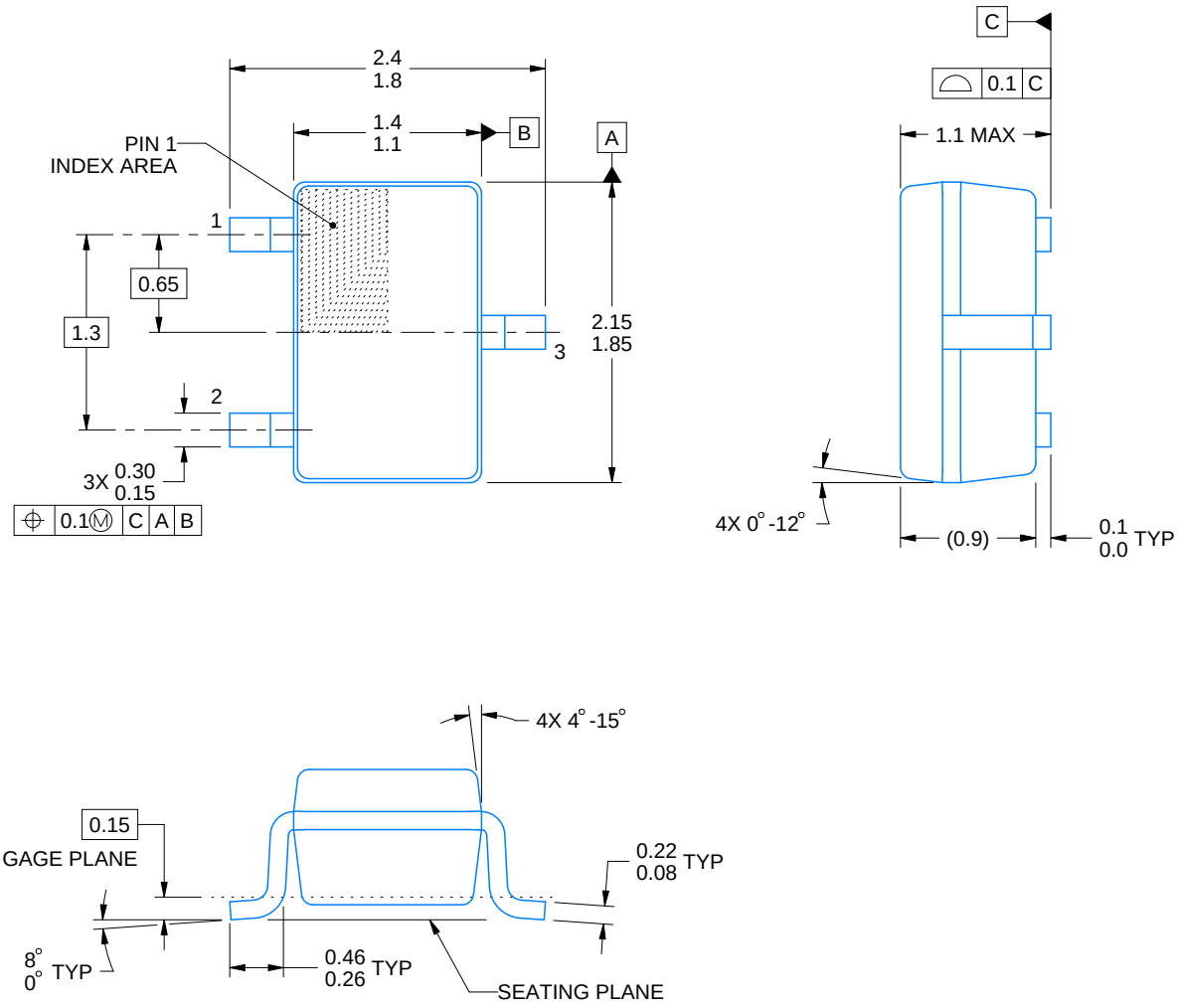
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

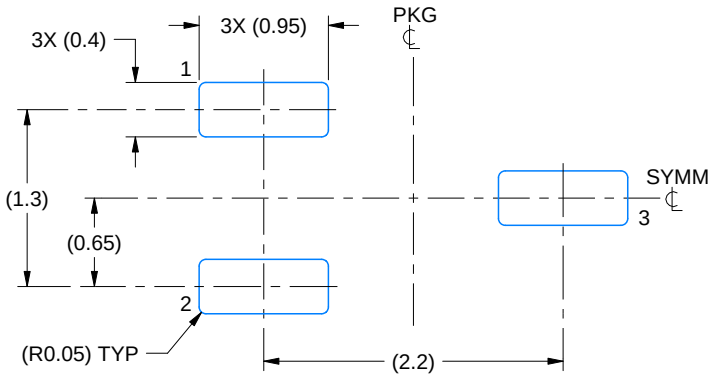
SMALL OUTLINE TRANSISTOR SC70



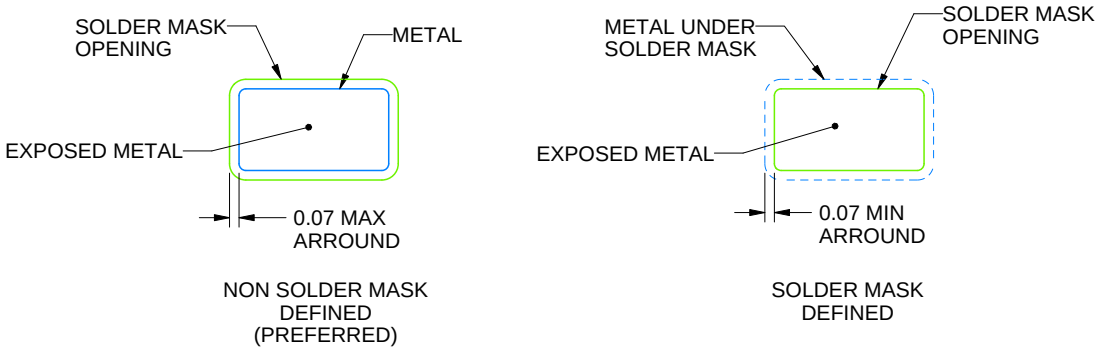
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

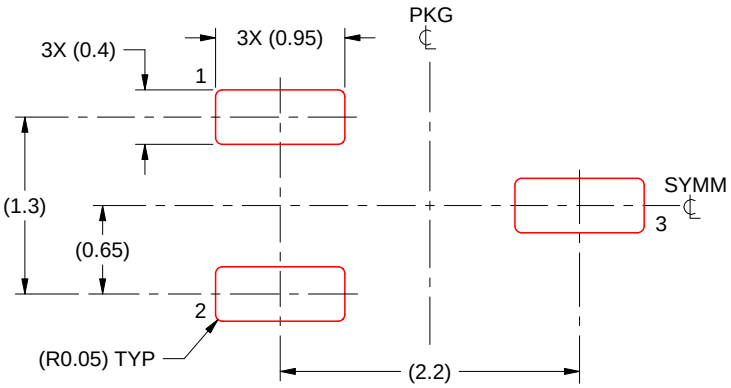


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

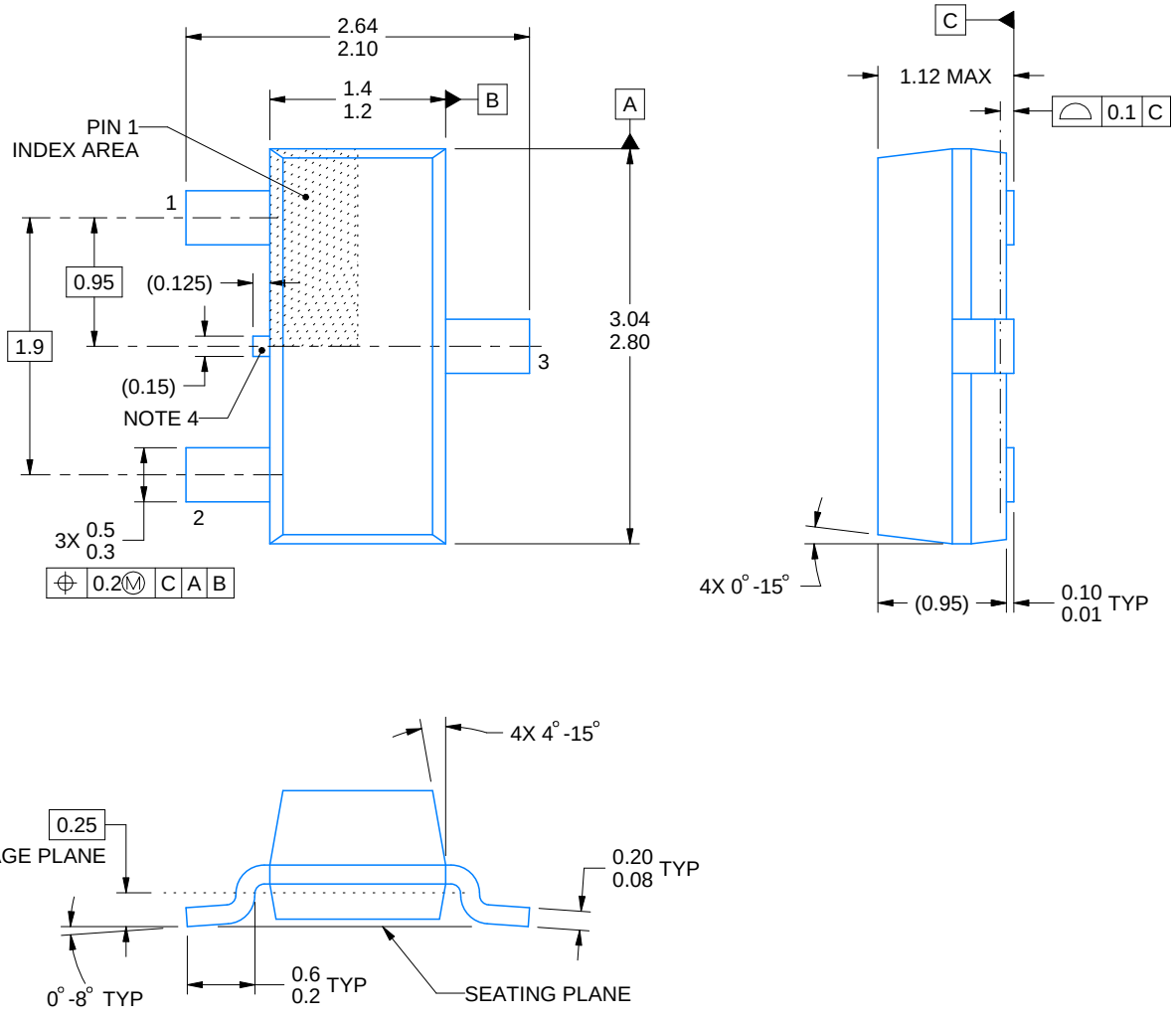
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

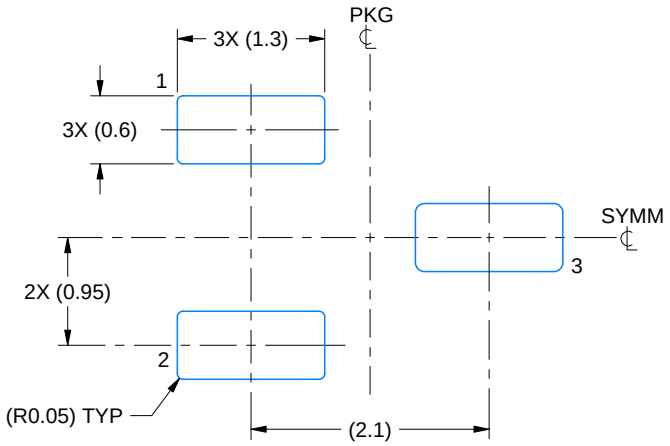
SMALL OUTLINE TRANSISTOR



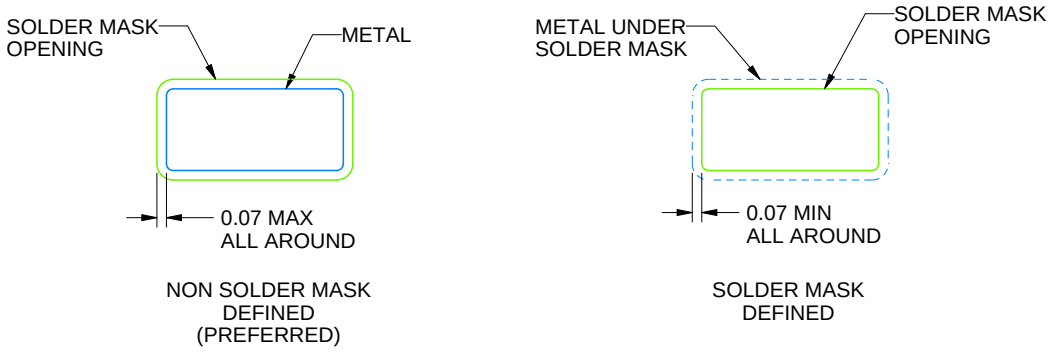
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

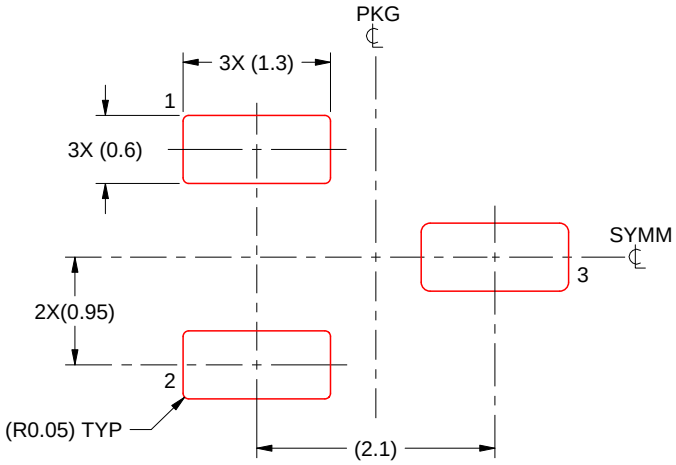


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025