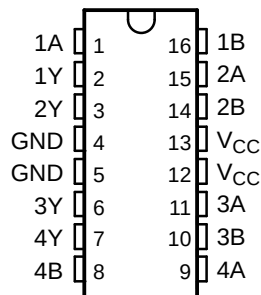


FEATURES

- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typ Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)

**D OR N PACKAGE
(TOP VIEW)**



DESCRIPTION

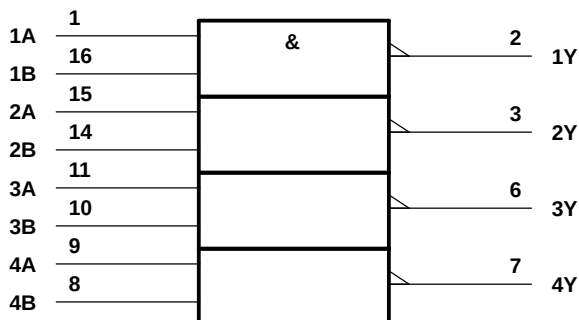
This device contains four independent 2-input NAND gates. It performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 74AC11000 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE
(EACH GATE)**

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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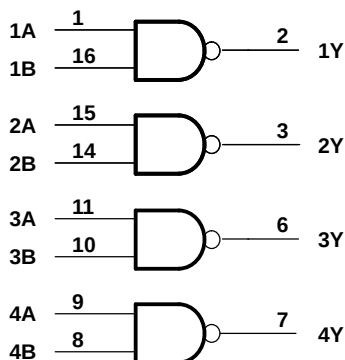
EPIC is a trademark of Texas Instruments.

74AC11000

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS054B–APRIL 1987–REVISED JUNE 2005

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
V _I	Input voltage range ⁽²⁾		−0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0 or V _I > V _{CC}	±20		mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±50		mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±50		mA
Continuous current through V _{CC} or GND			±100		mA
Maximum power dissipation at T _A = 55°C (in still air) ⁽³⁾		D package	1.3		W
		N package	1.1		
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 5.5\text{ V}$		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3\text{ V}$		–4	mA
		$V_{CC} = 4.5\text{ V}$		–24	
		$V_{CC} = 5.5\text{ V}$		–24	
I_{OL}	Low-level output current	$V_{CC} = 3\text{ V}$		12	mA
		$V_{CC} = 4.5\text{ V}$		24	
		$V_{CC} = 5.5\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	3 V		0.1			0.1	V
		4.5 V		0.1			0.1	
		5.5 V		0.1			0.1	
	$I_{OL} = 12\text{ mA}$	3 V		0.36			0.44	
		4.5 V		0.36			0.44	
		5.5 V		0.36			0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
		5.5 V			4		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

74AC11000

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS054B–APRIL 1987–REVISED JUNE 2005

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	7.2	9.8	1.5	11.1	ns
t_{PHL}			1.5	5.8	8.6	1.5	9.6	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

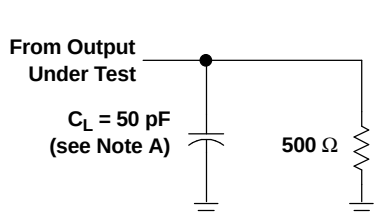
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5	6.5	1.5	7.4	ns
t_{PHL}			1.5	4.4	6.1	1.5	6.8	

Operating Characteristics

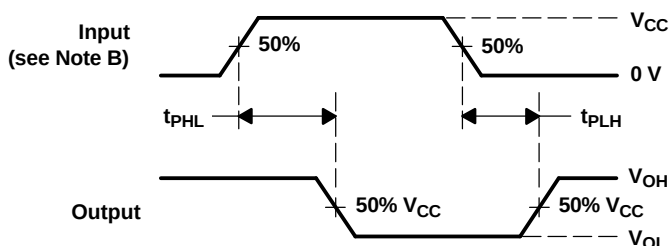
$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	33	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AC11000D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	AC11000
74AC11000DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11000
74AC11000DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11000
74AC11000N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11000N
74AC11000N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11000N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

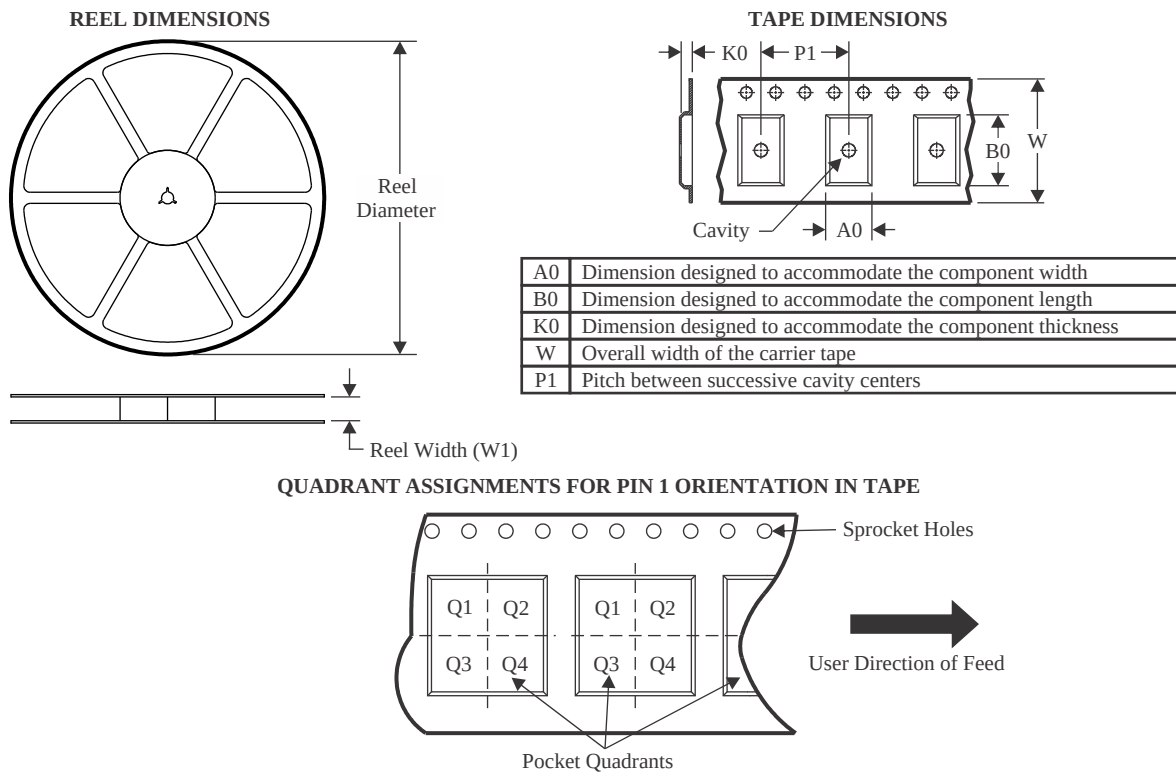
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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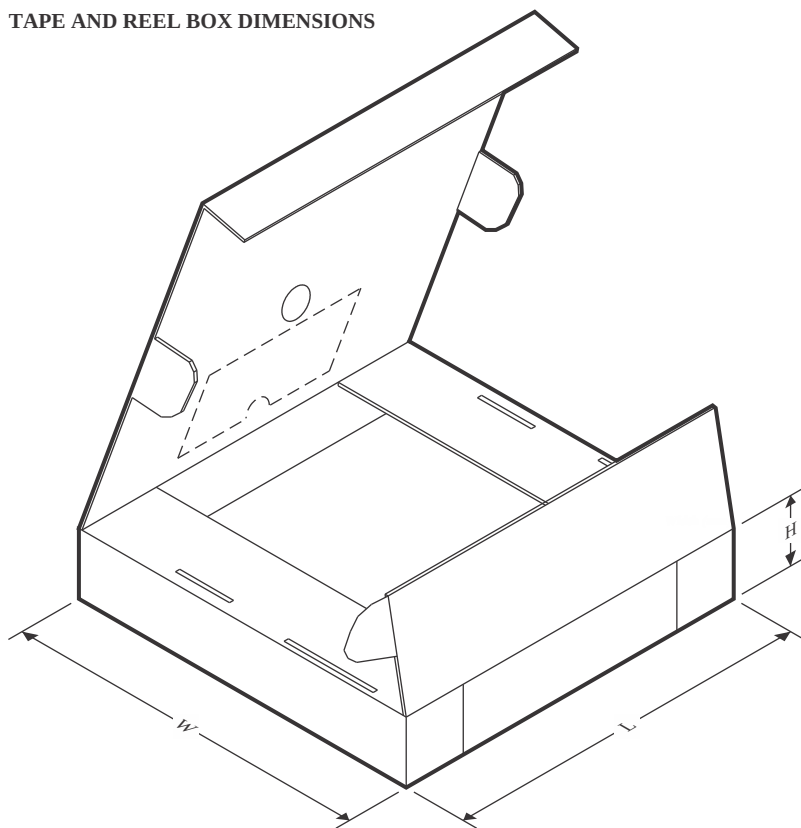
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11000DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

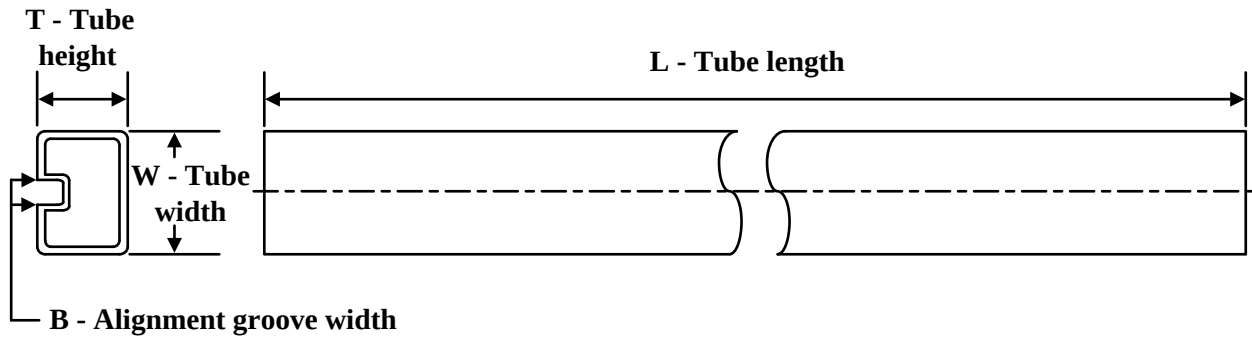
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11000DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE

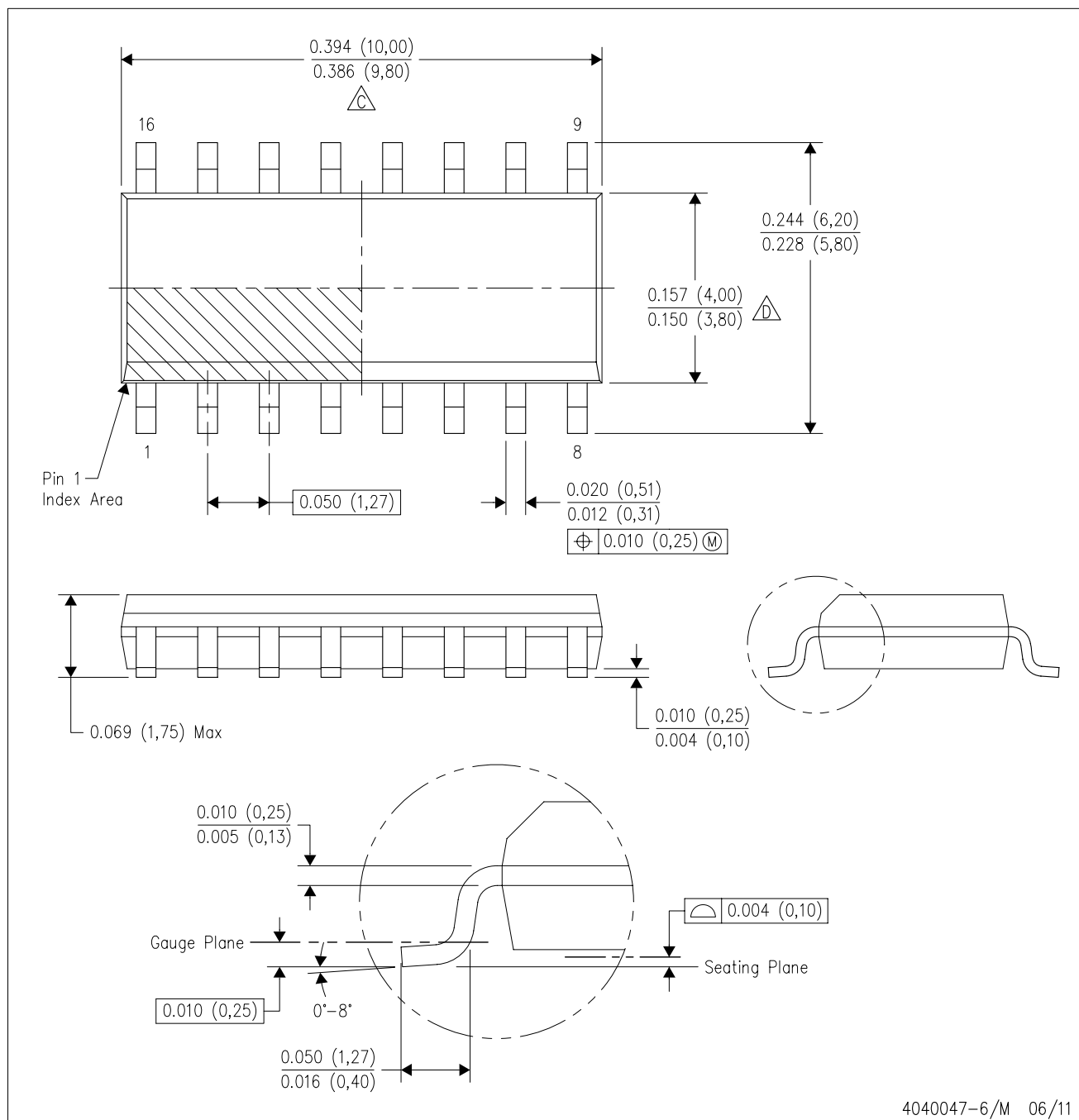


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74AC11000N	N	PDIP	16	25	506	13.97	11230	4.32
74AC11000N	N	PDIP	16	25	506	13.97	11230	4.32
74AC11000N.A	N	PDIP	16	25	506	13.97	11230	4.32
74AC11000N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

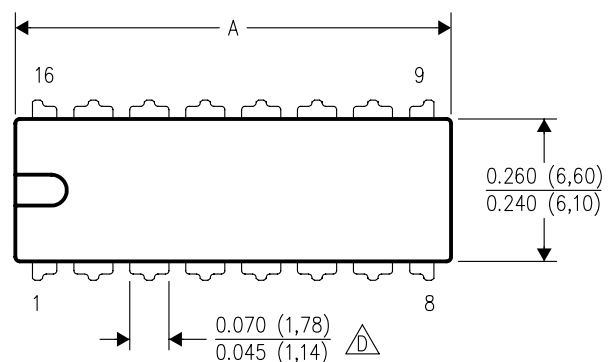


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

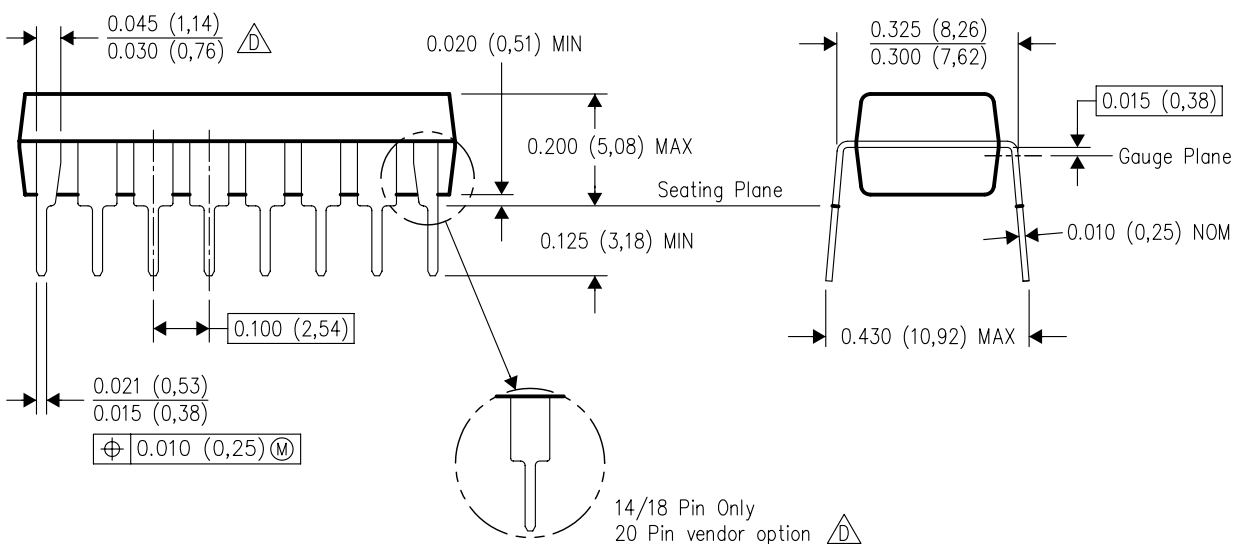
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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