

SN54ACT16651, 74ACT16651 16-BIT TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCAS449A – FEBRUARY 1993 – REVISED APRIL 1996

- Members of the Texas Instruments **Widebus™** Family
- Inputs Are TTL-Voltage Compatible
- Inverting Data Paths
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

description

The SN54ACT16651 and 74ACT16651 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN54ACT16651 and 74ACT16651.

SN54ACT16651 . . . WD PACKAGE
74ACT16651 . . . DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA



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**TEXAS
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description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74ACT16651 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16651 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT16651 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{\text{B}}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{\text{B}}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{\text{A}}$ data to B bus
H	H	L	X	H	X	Input	Output	Stored $\overline{\text{A}}$ data to B bus
H	L	L	L	H	H	Output	Output	Stored $\overline{\text{A}}$ data to B bus and stored $\overline{\text{B}}$ data to A bus

[†] The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.

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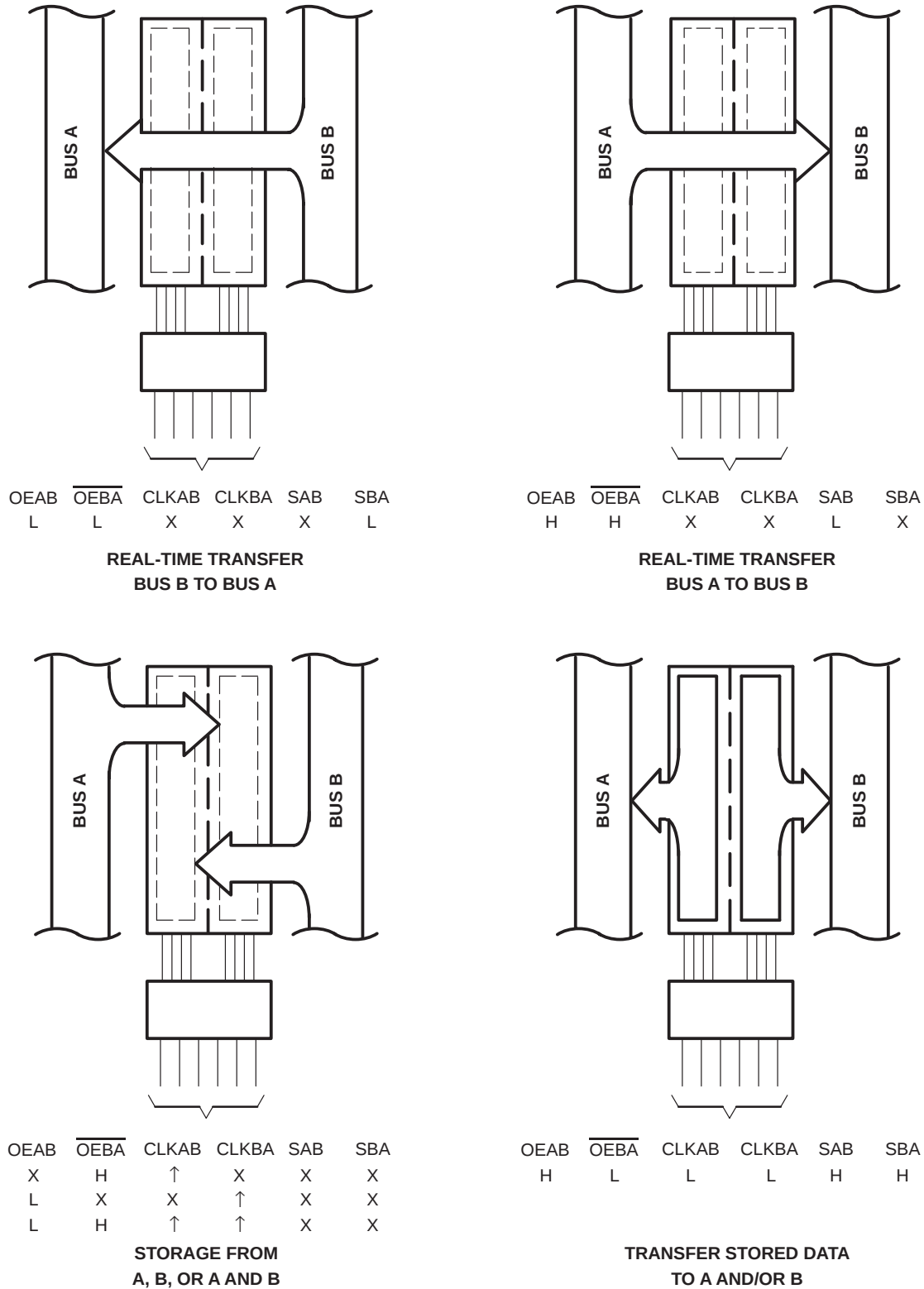


Figure 1. Bus-Management Functions

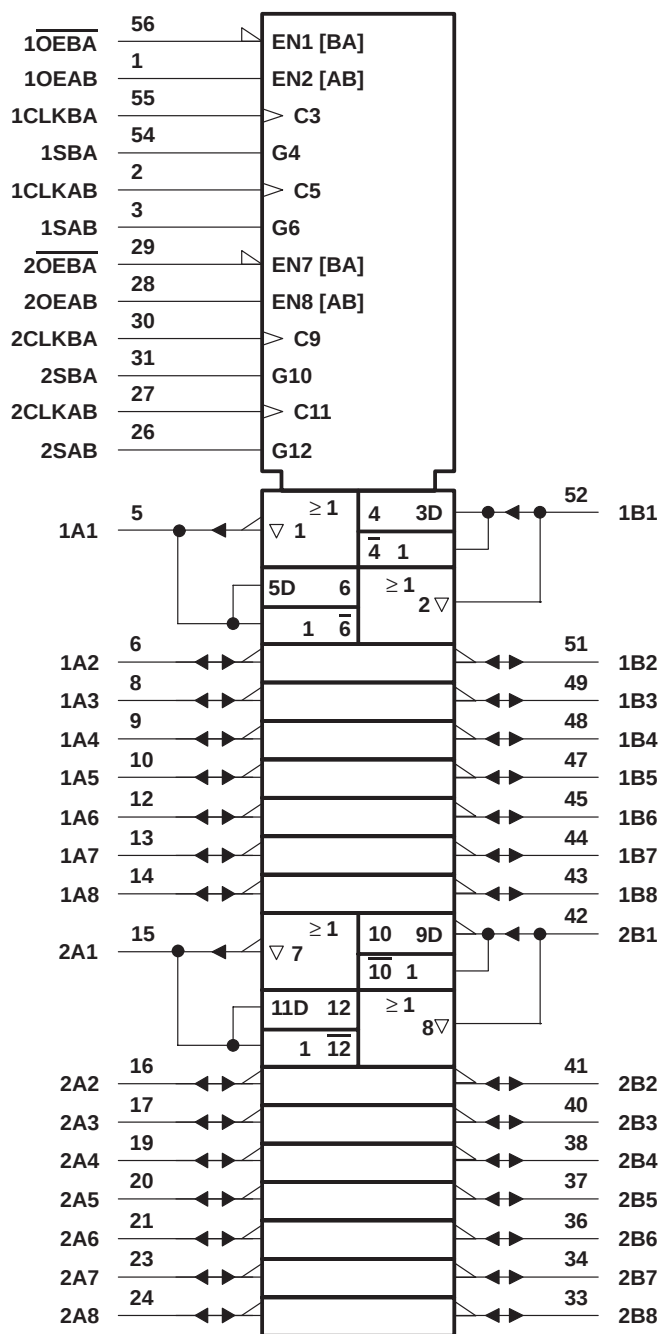
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logic symbol†

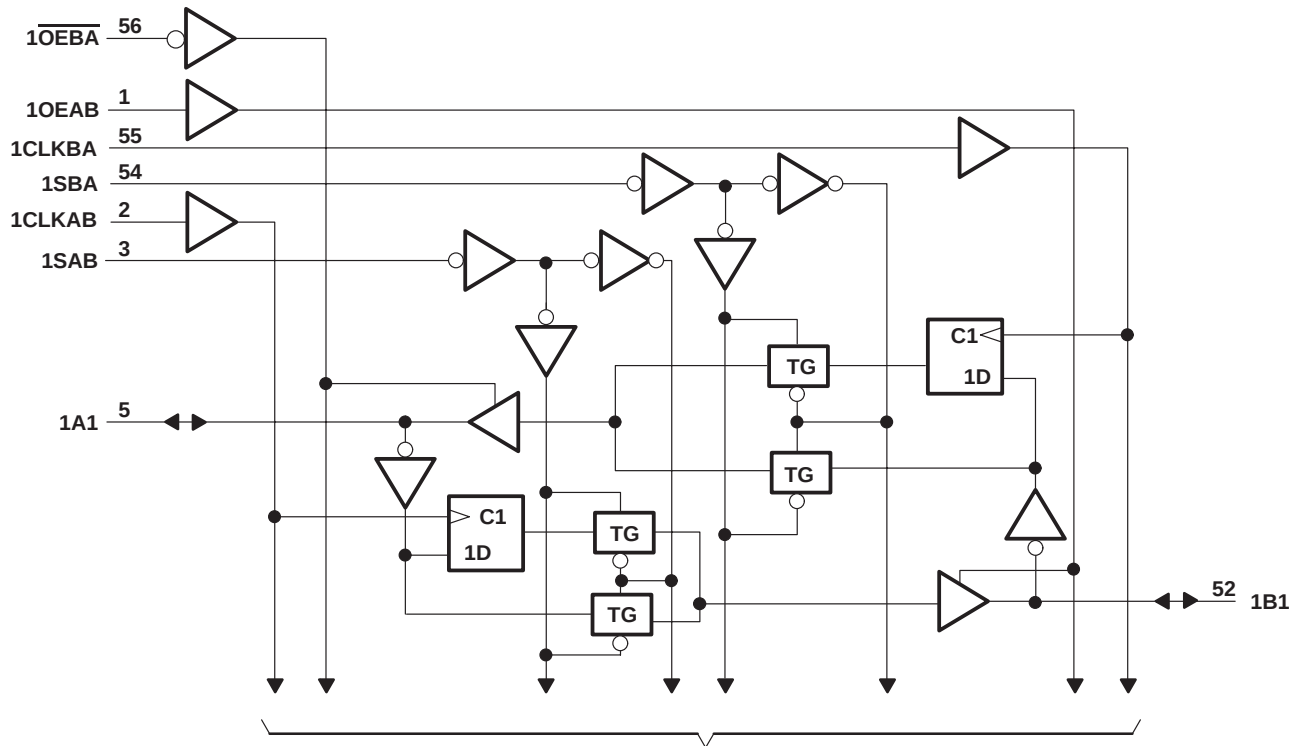


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

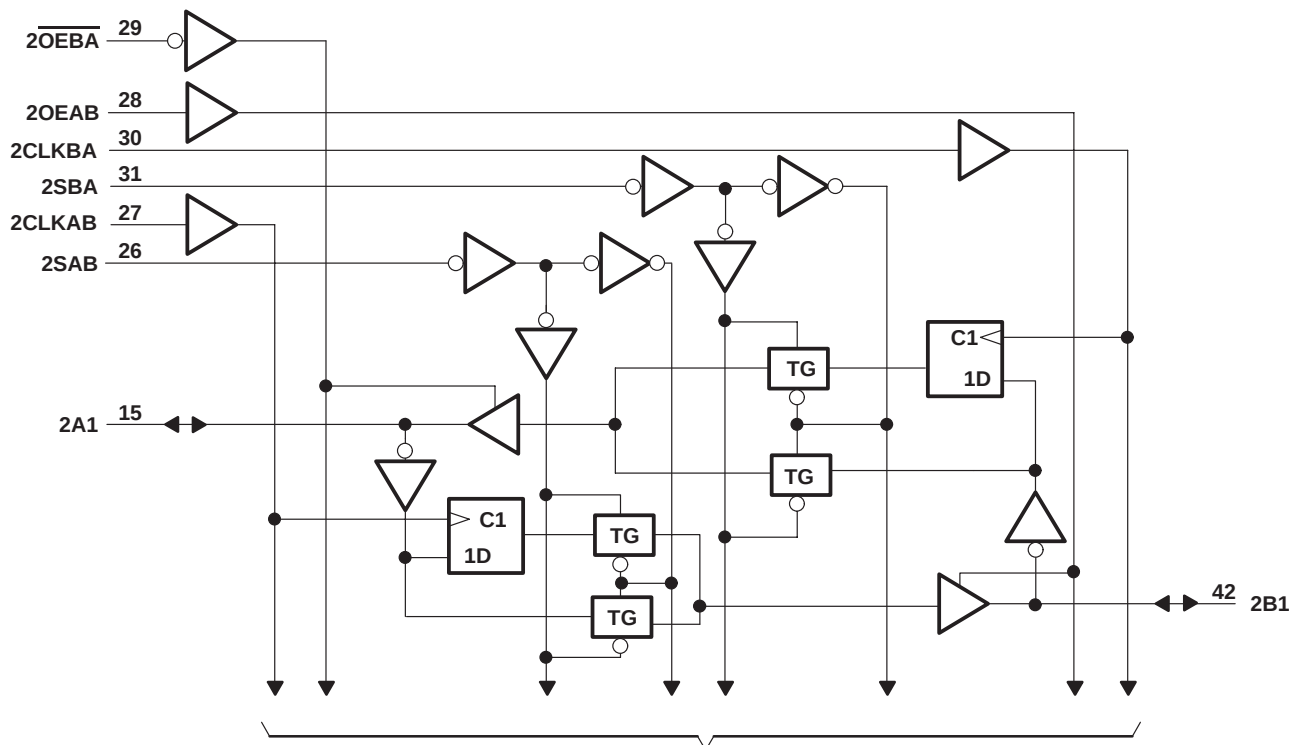
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logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	SN54ACT16651			74ACT16651			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH} High-level output current			–24			–24	mA
I_{OL} Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT16651		74ACT16651		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		I _{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I _{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I _{OH} = –50 mA [†]	5.5 V				3.85				
		I _{OH} = –75 mA [†]	5.5 V						3.85		
V _{OL}		I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I _{OL} = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{OZ} [‡]	A or B ports	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	µA
ΔI _{CC} [§]		One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1		1	mA
C _i	Control inputs	V _I = V _{CC} or GND	5 V			4					pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V			12					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)**

		T _A = 25°C		SN54ACT16651		74ACT16651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	90	0	90	0	90	MHz
t _w	Pulse duration, CLKAB or CLKBA high or low	5.5		5.5		5.5		ns
t _{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	5.3		5.3		5.3		ns
t _h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT16651		74ACT16651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	3	6.6	10	3	12.2	3	11.3	ns
t_{PHL}			4.6	8	10.6	4.6	12.7	4.6	11.9	
t_{PLH}	CLKBA or CLKAB	A or B	5.4	9.1	12	5.4	14.8	5.4	13.7	ns
t_{PHL}			5.4	9.1	12	5.4	14.6	5.4	13.6	
t_{PLH}	SBA or SAB (with A or B high)	A or B	4.6	7.9	10.5	4.6	13.1	4.6	12.1	ns
t_{PHL}			5.4	10.9	15.5	5.4	19.6	5.4	17.8	
t_{PLH}	SBA or SAB (with A or B low)	A or B	5	10.4	14.9	5	19.2	5	17.3	ns
t_{PHL}			4.9	8.6	11.9	4.9	13.7	4.9	12.7	
t_{PZH}	$\overline{\text{OEBA}}$	A	3.2	7.2	10.8	3.2	13.6	3.2	12.3	ns
t_{PZL}			3.8	8	12.2	3.8	15.3	3.8	13.9	
t_{PHZ}	$\overline{\text{OEBA}}$	A	5.1	7.8	9.8	5.1	11.3	5.1	10.6	ns
t_{PLZ}			4.9	7.7	9.9	4.9	11.4	4.9	10.8	
t_{PZH}	OEAB	B	4.9	8	10.5	4.9	12.9	4.9	11.9	ns
t_{PZL}			5.4	8.8	11.8	5.4	14.7	5.4	13.5	
t_{PHZ}	OEAB	B	4.3	7.5	10.7	4.3	12	4.3	11.4	ns
t_{PLZ}			4.5	7.6	10.8	4.5	12.3	4.5	11.6	

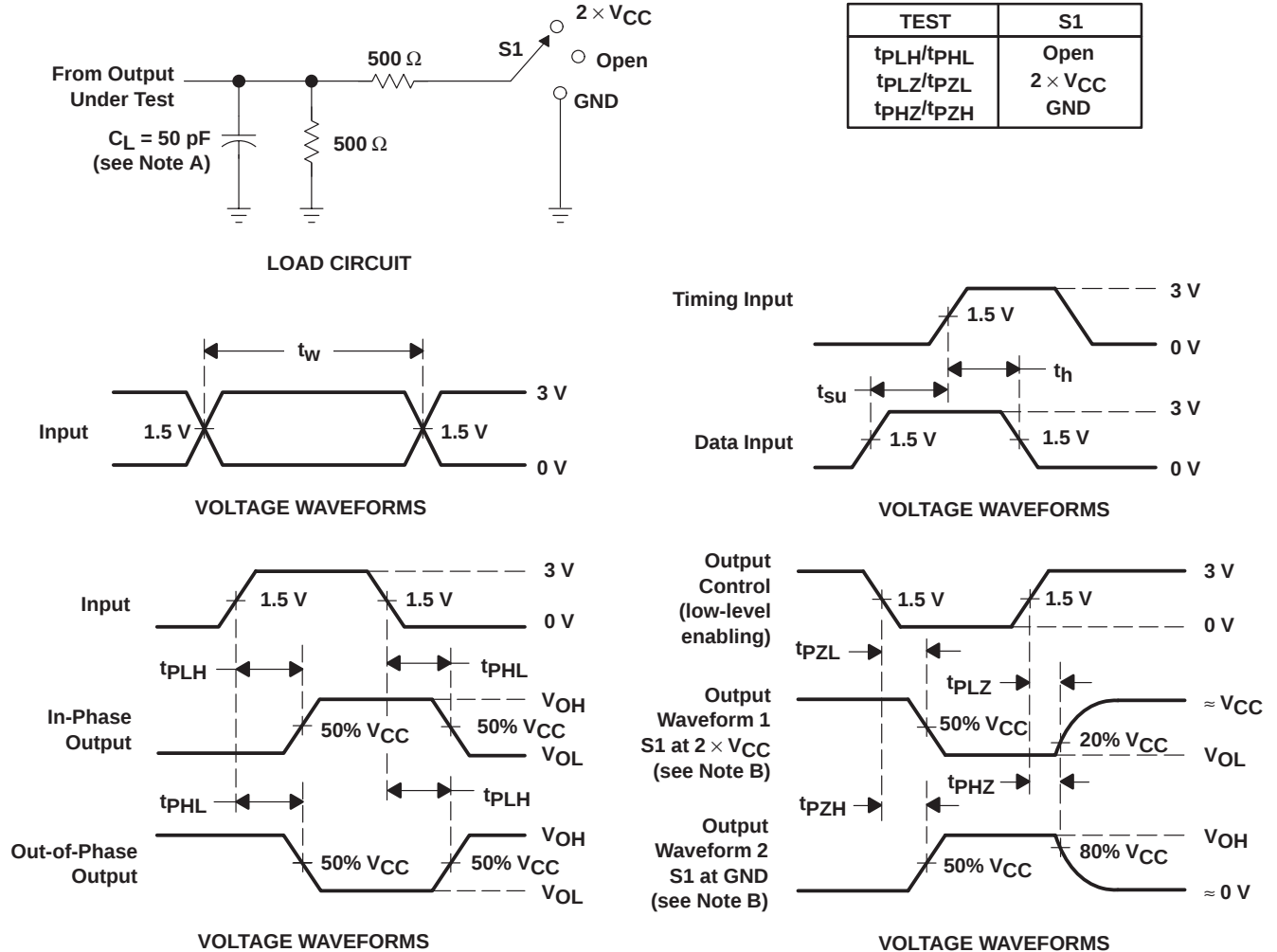
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		62	pF
		Outputs disabled			14	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ACT16651DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16651
74ACT16651DL.A	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16651

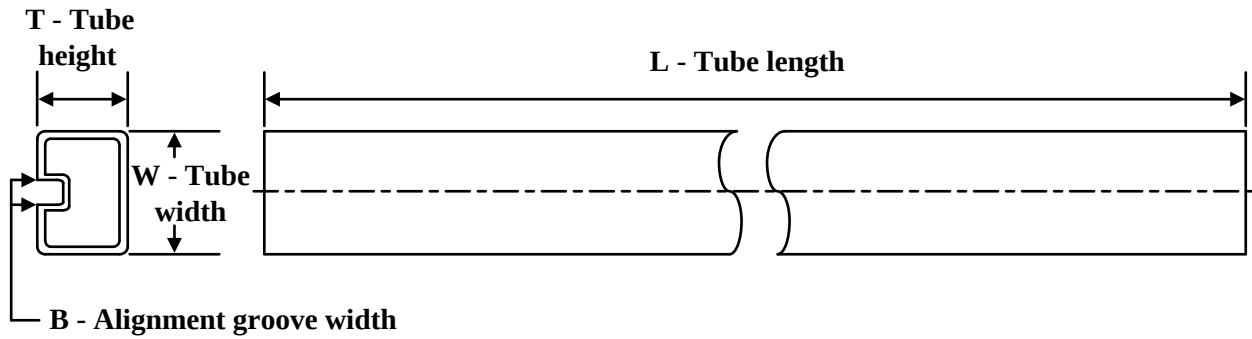
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74ACT16651DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
74ACT16651DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

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