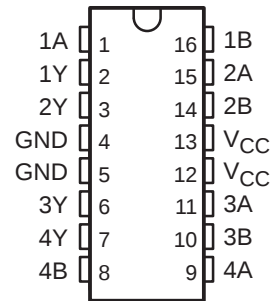


74AC11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS081A – NOVEMBER 1989 – REVISED APRIL 1996

- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)

D OR N PACKAGE
(TOP VIEW)



description

This device contains four independent 2-input exclusive-OR gates. It performs the Boolean function $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

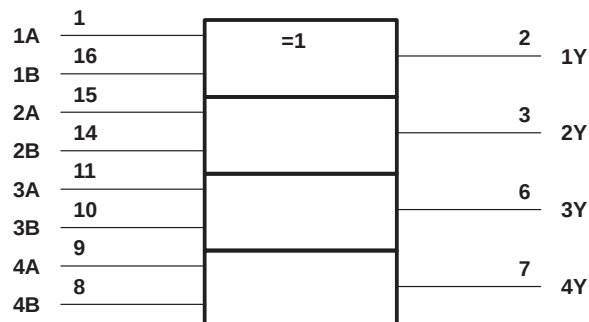
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The 74AC11086 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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**TEXAS
INSTRUMENTS**

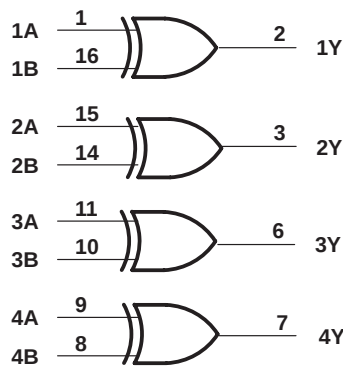
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74AC11086
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logic diagram (positive logic)



exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR



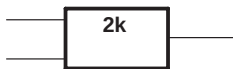
These are five equivalent exclusive-OR symbols valid for a 74AC11086 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



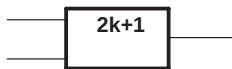
The output is active (high) if all inputs stand at the same logic level (i.e., $A=B$).

EVEN-PARITY ELEMENT



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active (high).

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active (high).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.3 W
N package	1.1 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 5.5\text{ V}$	3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$			0.9	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 5.5\text{ V}$			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3\text{ V}$			-4	mA
		$V_{CC} = 4.5\text{ V}$			-24	
		$V_{CC} = 5.5\text{ V}$			-24	
I_{OL}	Low-level output current	$V_{CC} = 3\text{ V}$			12	mA
		$V_{CC} = 4.5\text{ V}$			24	
		$V_{CC} = 5.5\text{ V}$			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
		5.5 V				3.85		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
	$I_{OL} = 24\text{ mA}$	5.5 V			0.36		0.44	
		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	Y	1.5	5.6	9.4	1.5	10.6	ns
t _{PHL}			1.5	5.1	7.4	1.5	8.2	

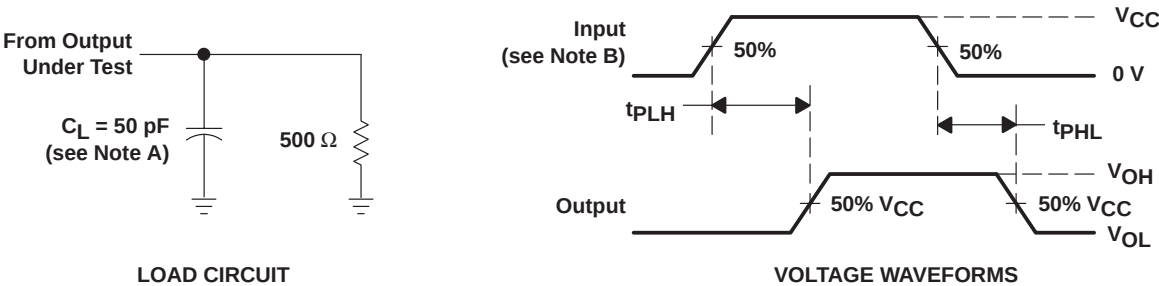
switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	Y	1.5	3.8	6.8	1.5	7.6	ns
t _{PHL}			1.5	3.8	6.2	1.5	6.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.
 - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AC11086D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11086
74AC11086D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11086
74AC11086N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11086N
74AC11086N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11086N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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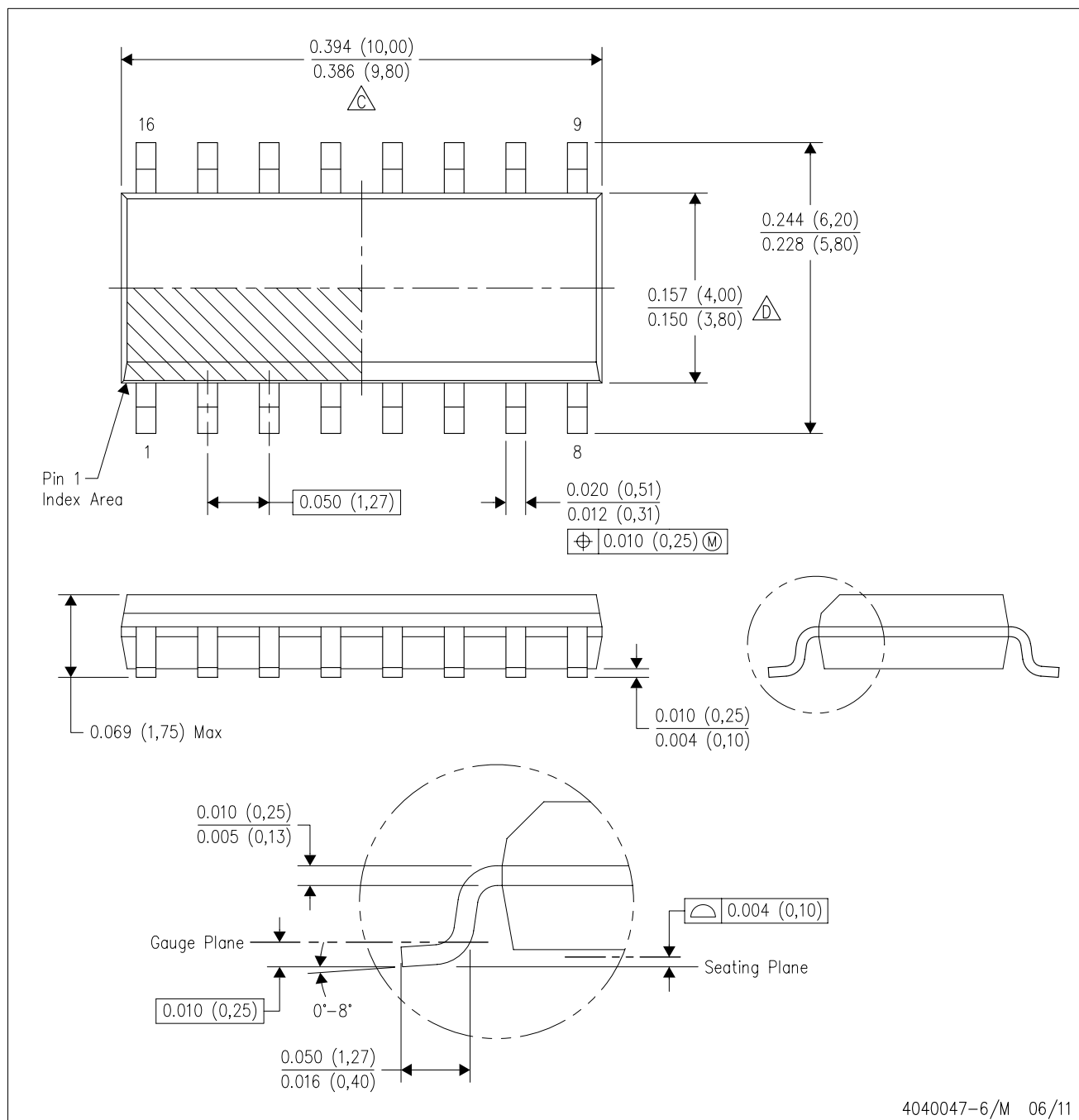
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74AC11086D	D	SOIC	16	40	507	8	3940	4.32
74AC11086D.A	D	SOIC	16	40	507	8	3940	4.32
74AC11086N	N	PDIP	16	25	506	13.97	11230	4.32
74AC11086N	N	PDIP	16	25	506	13.97	11230	4.32
74AC11086N.A	N	PDIP	16	25	506	13.97	11230	4.32
74AC11086N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

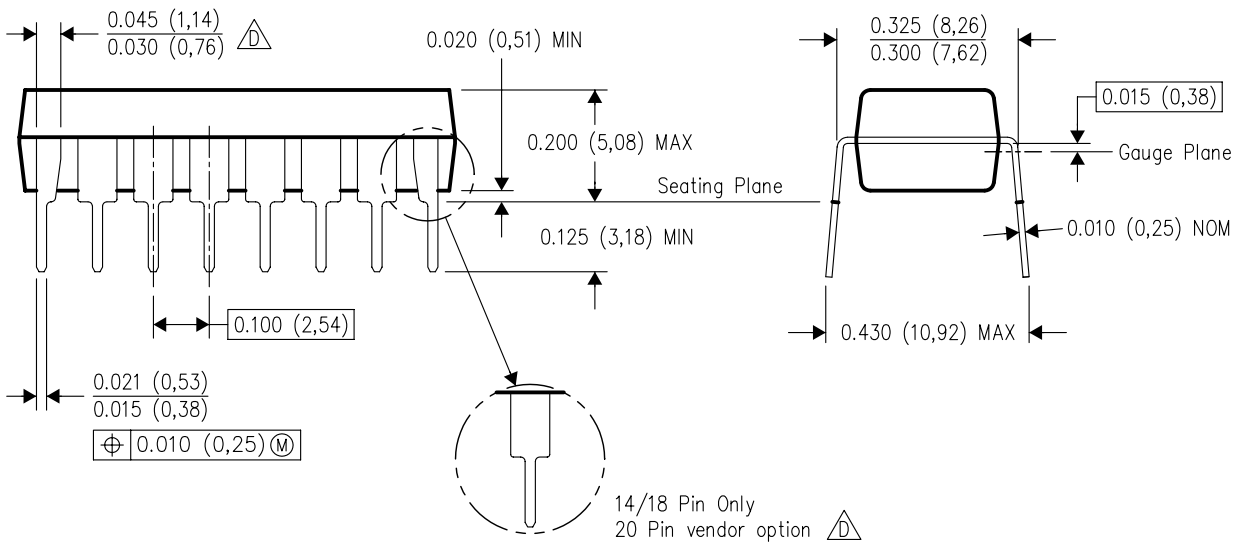
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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