

# 54ACT16543, 74ACT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS126B – MARCH 1990 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

## description

The 'ACT16543 are 16-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. The 'ACT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ( $\overline{\text{LEAB}}$  or  $\overline{\text{LEBA}}$ ) and output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{\text{CEAB}}$ ) and  $\overline{\text{OEAB}}$  inputs must be low to enter data from A or to output data to B. Having  $\overline{\text{CEAB}}$  low and  $\overline{\text{LEAB}}$  low makes the A-to-B latches transparent; a subsequent low-to-high transition at  $\overline{\text{LEAB}}$  puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$  inputs.

The 74ACT16543 is packaged in TI's shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16543 is characterized for operation from –40°C to 85°C.

54ACT16543 . . . WD PACKAGE  
74ACT16543 . . . DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{\text{1OEAB}}$	1	56	$\overline{\text{1OEBA}}$
$\overline{\text{1LEAB}}$	2	55	$\overline{\text{1LEBA}}$
$\overline{\text{1CEAB}}$	3	54	$\overline{\text{1CEBA}}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{\text{2CEAB}}$	26	31	$\overline{\text{2CEBA}}$
$\overline{\text{2LEAB}}$	27	30	$\overline{\text{2LEBA}}$
$\overline{\text{2OEAB}}$	28	29	$\overline{\text{2OEBA}}$



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**TEXAS  
INSTRUMENTS**

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# 54ACT16543, 74ACT16543

## 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**FUNCTION TABLE**  
(each octal register)

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1–B8
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$		
H	X	X	Storing	Z
X	H	X	Storing	
X	X	H		Z
L	L	L	Transparent	Current A data
L	H	L	Storing	Previous A data‡

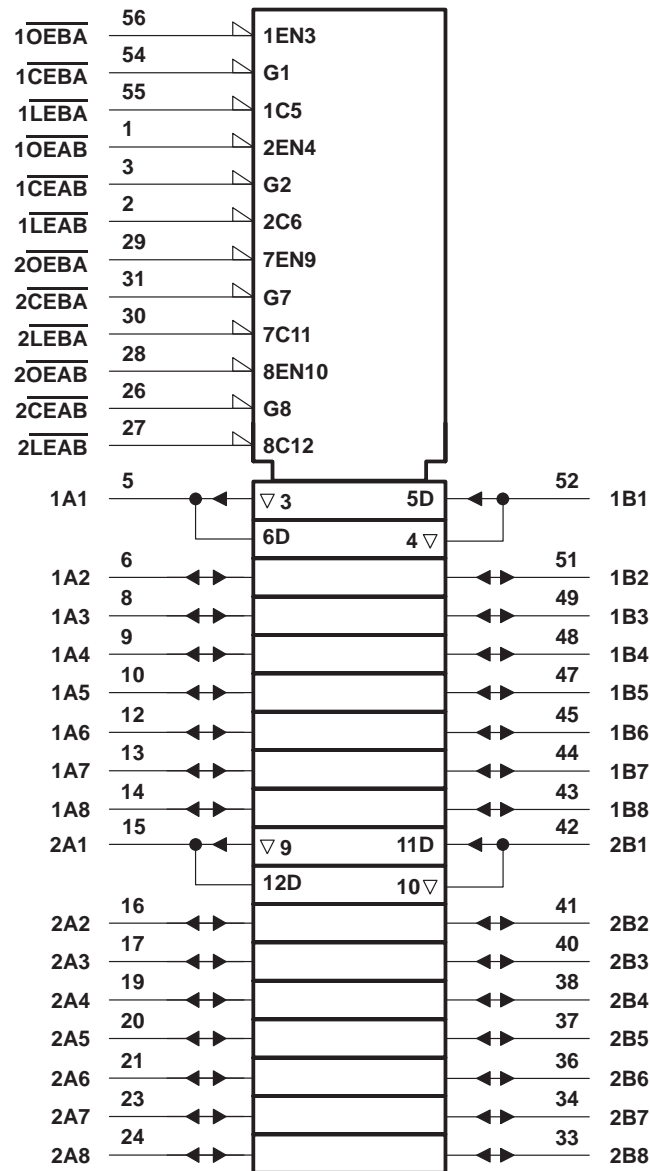
† A-to-B data flow is shown: B-to-A flow control is the same except that it uses  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$ .

‡ Data present before low-to-high transition of  $\overline{\text{LEAB}}$  occurring while  $\overline{\text{CEAB}}$  is low

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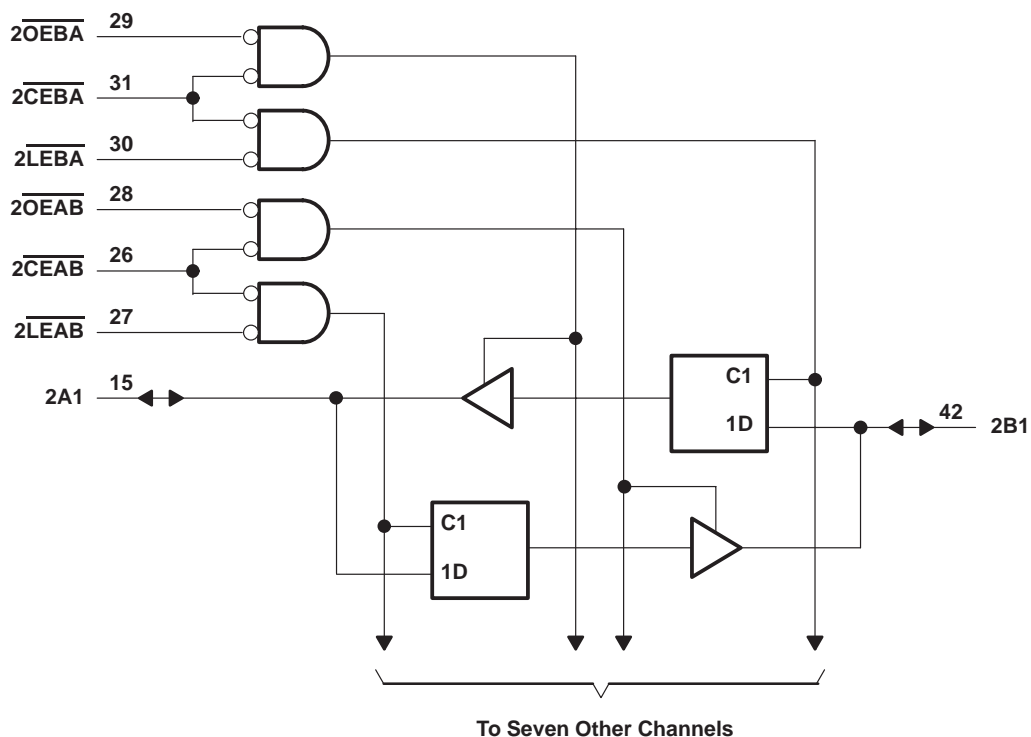
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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The diagram illustrates the internal logic of a 16-channel multiplexer. It features four 3-to-1 multiplexers (labeled C1 1D) and four 2-to-1 multiplexers (labeled C1 1D). The inputs are labeled 1OEAB, 1CEAB, 1LEAB, 1A1, 56, 54, 55, 1, 3, 2, 5, and 52. The outputs are labeled 1B1 and 52. The diagram is a detailed logic circuit showing the internal structure of the multiplexer.



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC}+0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC}+0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**recommended operating conditions (see Note 3)**

	54ACT16543			74ACT16543			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_I$ Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$ High-level output current			–24			–24	mA
$I_{OL}$ Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$ Operating free-air temperature	–55		125	–40		85	°C

- NOTES: 3. Unused pins (inputs and I/O) must be held high or low to prevent them from floating.  
4. All  $V_{CC}$  and GND pins must be connected to the proper voltage power supply.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT16543		74ACT16543		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = -50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85		3.85		
V <sub>OL</sub>		I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V					1.65		1.65	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
I <sub>OZ</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5		±5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80		80	µA
ΔI <sub>CC</sub> <sup>§</sup>		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			0.9		1		1	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5						pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		12						

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54ACT16543		74ACT16543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	7.5		7.5		7.5		ns
t <sub>su</sub>	Setup time, data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}^{\uparrow}$	2.5		2.5		2.5		ns
t <sub>h</sub>	Hold time, data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}^{\uparrow}$	4		4		4		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT16543		74ACT16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	3.5	6.9	9.5	3.5	10.5	3.5	10.5	ns
$t_{PHL}$			3.1	7.3	10.7	3.1	11.6	3.1	11.6	
$t_{PLH}$	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	8.6	12.3	3.9	13.8	3.9	13.8	ns
$t_{PHL}$			3.9	8.7	12.2	3.9	13.5	3.9	13.5	
$t_{PZH}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.6	7.1	10.3	2.6	11.4	2.6	11.4	ns
$t_{PZL}$			3.5	8.3	11.9	3.5	13.2	3.5	13.2	
$t_{PHZ}$	OEBA or OEAB	A or B	4.1	8.2	10.5	4.1	11.1	4.1	11.1	ns
$t_{PLZ}$			5	7.3	9.3	5	9.6	5	9.6	
$t_{PZH}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.1	7.3	10.7	3.1	11.7	3.1	11.7	ns
$t_{PZL}$			3.9	8.5	12.2	3.9	13.5	3.9	13.5	
$t_{PHZ}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.6	8.5	11	4.6	11.6	4.6	11.6	ns
$t_{PLZ}$			5.2	7.4	9.7	5.2	10.5	5.2	10.5	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	45	pF
		Outputs disabled		12	

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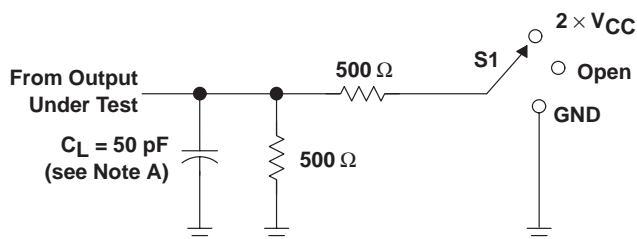


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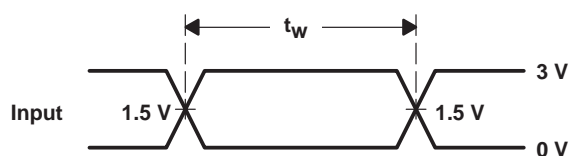
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## PARAMETER MEASUREMENT INFORMATION

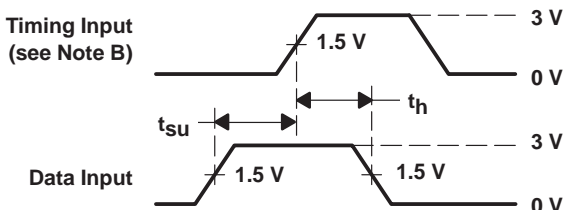


LOAD CIRCUIT

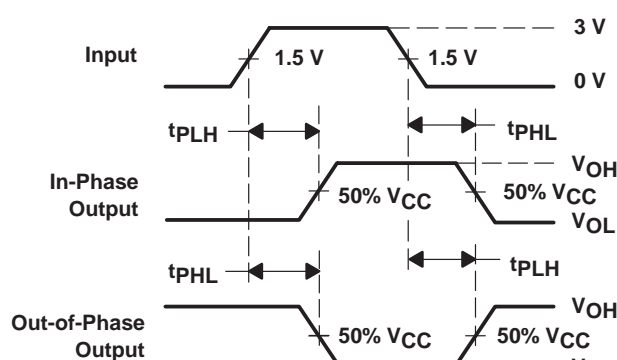
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



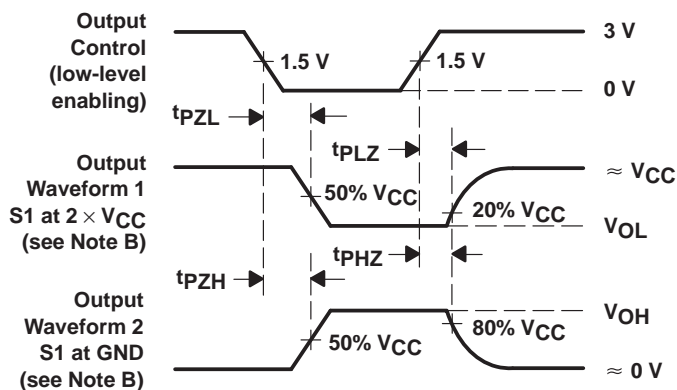
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">74ACT16543DGGR</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16543
74ACT16543DGGR.A	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16543
<a href="#">74ACT16543DL</a>	Obsolete	Production	SSOP (DL)   56	-	-	Call TI	Call TI	-40 to 85	ACT16543
<a href="#">74ACT16543DLR</a>	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16543
74ACT16543DLR.A	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16543

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
74ACT16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16543DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
74ACT16543DLR	SSOP	DL	56	1000	356.0	356.0	53.0

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