ADC128S052, ADC128S052-Q1 8-Channel, 200 kSPS to 500 kSPS, 12-Bit A/D Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
- Eight Input Channels
- Variable Power Management
- Independent Analog and Digital Supplies
- Compatible With SPI™, QSPI™, MICROWIRE, and DSP
- Packaged in 16-Pin TSSOP
- Conversion Rate 200 kSPS to 500 kSPS
- DNL (V_A = V_D = 5 V) + 1.3 or −0.9 LSB (Maximum)
- INL (V_A = V_D = 5 V) ±1 LSB (Maximum)
- Power Consumption
  - 3-V Supply 1.6 mW (Typical)
  - 5-V Supply 8.7 mW (Typical)

2 Applications

- Automotive Navigation
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

3 Description

The ADC128S052x device is a low-power, eight-channel CMOS 12-bit analog-to-digital converter specified for conversion throughput rates of 200 kSPS to 500 kSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to eight input signals at inputs IN0 through IN7.

The output serial data is straight binary and is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.

The ADC128S052x may be operated with independent analog and digital supplies. The analog supply (V_A) can range from 2.7 V to 5.25 V, and the digital supply (V_D) can range from 2.7 V to V_A. Normal power consumption using a 3-V or 5-V supply is 1.6 mW and 8.7 mW, respectively. The power-down feature reduces the power consumption to 0.06 µW using a 3-V supply and 0.25 µW using a 5-V supply.

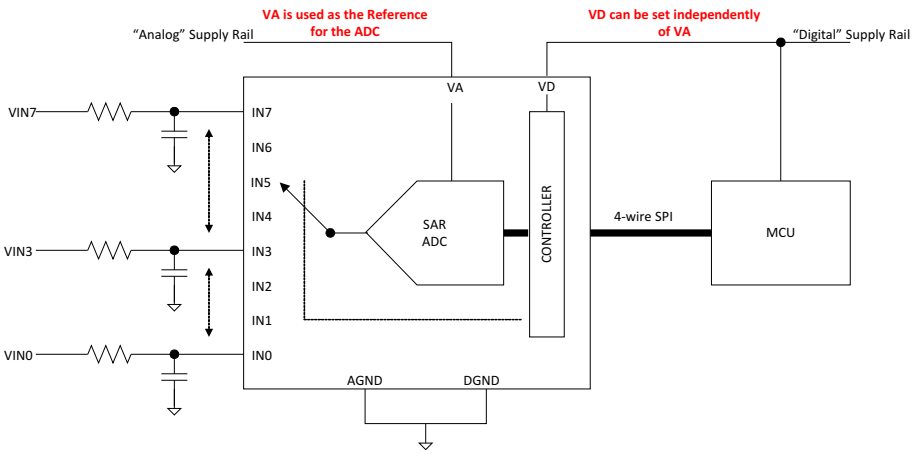
The ADC128S052x is packaged in a 16-pin TSSOP package. The ADC128S052 is ensured over the extended industrial temperature range of −40°C to +105°C while the ADC128S052-Q1 is ensured to an AECQ100 Grade-1 automotive temperature range of −40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC128S052, ADC128S052-Q1	TSSOP (16)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

- Added *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format 23

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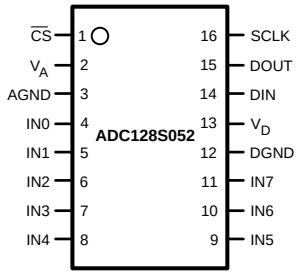
5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	Digital I/O	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
2	V_A	Power Supply	Positive analog supply pin. This voltage is also used as the reference voltage. This pin must be connected to a quiet 2.7-V to 5.25-V source and bypassed to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
3	AGND	Power Supply	The ground return for the analog supply and signals.
4	IN0 to IN7	Analog I/O	Analog inputs. These signals can range from 0 V to V_{REF}.
5			
6			
7			
8			
9			
10			
11			
12	DGND	Power Supply	The ground return for the digital supply and signals.
13	V_D	Power Supply	Positive digital supply pin. This pin must be connected to a 2.7-V to V_A supply, and bypassed to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.
14	DIN	Digital I/O	Digital data input. The control register of the ADC128S052 is loaded through this pin on rising edges of the SCLK pin.
15	DOUT	Digital I/O	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
16	SCLK	Digital I/O	Digital clock input. The ensured performance range of frequencies for this input is 3.2 MHz to 8 MHz. This clock directly controls the conversion and readout processes.

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)(3)

	MIN	MAX	UNIT
Analog Supply Voltage V_A	–0.3	6.5	V
Digital Supply Voltage V_D	–0.3	V_A + 0.3, max 6.5	V
Voltage on Any Pin to GND	–0.3	V_A + 0.3	V
Input Current at Any Pin(4)		±10	mA
Package Input Current(4)		±20	mA
Power Dissipation at T_A = 25°C	See (5)		
Junction Temperature		+150	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) For soldering specifications: see product folder at www.ti.com and SNOA549.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin must be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The absolute maximum junction temperature (T_{JMAX}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{JMAX}, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{JMAX} - T_A)/R_{\theta JA}$. In the 16-pin TSSOP, $R_{\theta JA}$ is 110°C/W, so P_{DMAX} = 1,200 mW at 25°C and 625 mW at the maximum operating ambient temperature of 105°C. Note that the power consumption of this device under normal operation is a maximum of 12 mW. The values for maximum power dissipation listed above is reached only when the ADC128S052 is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

6.2 ESD Ratings – Commercial

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2500	V
		Machine model (MM)(3)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor.
(3) Machine model is a 220-pF discharged through ZERO Ω.

6.3 ESD Ratings – Automotive

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.4 Recommended Operating Conditions

See (1)

		MIN	NOM	MAX	UNIT
Operating Temperature	ADC128S052	−40	T_A	105	°C
	ADC128S052-Q1	−40	T_A	125	°C
V_A Supply Voltage		2.7		5.25	V
V_D Supply Voltage		2.7		V_A	V
Digital Input Voltage		0		V_A	V
Analog Input Voltage		0		V_A	V
Clock Frequency		50		1600	kHz

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

6.5 Thermal Information

THERMAL METRIC(1)		ADC128S052, ADC128S052-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

The following specifications apply for AGND = DGND = 0 V, f_{SCLK} = 3.2 MHz to 8 MHz, f_{SAMPLE} = 200 kSPS to 500 kSPS, C_L = 50 pF, unless otherwise noted. Maximum and minimum limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(2)	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				12	Bits
INL	Integral Non-Linearity (End Point Method)	$V_A = V_D$ = 3 V		±0.3	±1	LSB
		$V_A = V_D$ = 5 V		±0.4	±1	LSB
DNL	Differential Non-Linearity	$V_A = V_D$ = 3 V		0.3	0.9	LSB
			−0.7	−0.2		LSB
		$V_A = V_D$ = 5 V		0.6	1.3	LSB
			−0.9	−0.4		LSB
V_{OFF}	Offset Error	$V_A = V_D$ = 3 V		0.8	±2.3	LSB
		$V_A = V_D$ = 5 V		1.2	±2.3	LSB
OEM	Offset Error Match	$V_A = V_D$ = 3 V		±0.05	±1.5	LSB
		$V_A = V_D$ = 5 V		±0.2	±1.5	LSB
FSE	Full Scale Error	$V_A = V_D$ = 3 V		0.6	±2.0	LSB
		$V_A = V_D$ = 5 V		0.3	±2.0	LSB
FSEM	Full Scale Error Match	$V_A = V_D$ = 3 V		±0.05	±1.5	LSB
		$V_A = V_D$ = 5 V		±0.2	±1.5	LSB

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).

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Electrical Characteristics (continued)

The following specifications apply for AGND = DGND = 0 V, f_{SCLK} = 3.2 MHz to 8 MHz, f_{SAMPLE} = 200 kSPS to 500 kSPS, C_L = 50 pF, unless otherwise noted. Maximum and minimum limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(2)	UNIT
DYNAMIC CONVERTER CHARACTERISTICS						
FPBW	Full Power Bandwidth (−3 dB)	$V_A = V_D$ = 3 V		8		MHz
		$V_A = V_D$ = 5 V		11		MHz
SINAD	Signal-to-Noise Plus Distortion Ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	70	73		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	70	73		dB
SNR	Signal-to-Noise Ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	70.8	73		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	70.8	73		dB
THD	Total Harmonic Distortion	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS		−90	−74	dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS		−89	−74	dB
SFDR	Spurious-Free Dynamic Range	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	75	92		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	75	91		dB
ENOB	Effective Number of Bits	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz	11.3	11.8		Bits
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	11.3	11.8		Bits
ISO	Channel-to-Channel Isolation	$V_A = V_D$ = 3 V, f_{IN} = 20 kHz		81		dB
		$V_A = V_D$ = 5 V, f_{IN} = 20 kHz, −0.02 dBFS		81		dB
IMD	Intermodulation Distortion, Second Order Terms	$V_A = V_D$ = 3 V, f_a = 19.5 kHz, f_b = 20.5 kHz		−98		dB
		$V_A = V_D$ = 5 V, f_a = 19.5 kHz, f_b = 20.5 kHz		−91		dB
	Intermodulation Distortion, Third Order Terms	$V_A = V_D$ = 3 V, f_a = 19.5 kHz, f_b = 20.5 kHz		−89		dB
		$V_A = V_D$ = 5 V, f_a = 19.5 kHz, f_b = 20.5 kHz		−88		dB
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input Range		0		V_A	V
I_{DCL}	DC Leakage Current				±1	µA
C_{INA}	Input Capacitance	Track Mode		33		pF
		Hold Mode		3		pF
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage	$V_A = V_D$ = 2.7 V to 3.6 V	2.1			V
		$V_A = V_D$ = 4.75 V to 5.25 V	2.4			V
V_{IL}	Input Low Voltage	$V_A = V_D$ = 2.7 V to 5.25 V			0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_D		±0.01	±1	µA
C_{IND}	Digital Input Capacitance			2	4	pF

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Electrical Characteristics (continued)

The following specifications apply for AGND = DGND = 0 V, f_{SCLK} = 3.2 MHz to 8 MHz, f_{SAMPLE} = 200 kSPS to 500 kSPS, C_L = 50 pF, unless otherwise noted. Maximum and minimum limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(2)	UNIT
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, $V_A = V_D$ = 2.7 V to 5.25 V	V_D − 0.5			V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA to 1.0 mA, $V_A = V_D$ = 2.7 V to 5.25 V			0.4	V
I_{OZH}, I_{OZL}	Hi-Impedance Output Leakage Current	$V_A = V_D$ = 2.7 V to 5.25 V			±1	µA
C_{OUT}	Hi-Impedance Output Capacitance(1)			2	4	pF
	Output Coding			Straight (Natural) Binary		
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)						
V_A, V_D	Analog and Digital Supply Voltages	$V_A \geq V_D$	2.7		5.25	V
$I_A + I_D$	Total Supply Current Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = 2.7 V to 3.6 V, f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz		0.54	1.2	mA
		$V_A = V_D$ = 4.75 V to 5.25 V, f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz		1.74	2.6	mA
	Total Supply Current Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = 2.7 V to 3.6 V, f_{SCLK} = 0 kSPS		20		nA
		$V_A = V_D$ = 4.75 V to 5.25 V, f_{SCLK} = 0 kSPS		50		nA
P_C	Power Consumption Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = 3 V f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz		1.6	3.6	mW
		$V_A = V_D$ = 5.0 V f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz		8.7	13.0	mW
	Power Consumption Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = 3 V f_{SCLK} = 0 kSPS		0.06		µW
		$V_A = V_D$ = 5 V f_{SCLK} = 0 kSPS		0.25		µW
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}MIN	Minimum Clock Frequency	$V_A = V_D$ = 2.7 V to 5.25 V	3.2	0.8		MHz
f_{SCLK}	Maximum Clock Frequency	$V_A = V_D$ = 2.7 V to 5.25 V		16	8	MHz
f_S	Sample Rate Continuous Mode	$V_A = V_D$ = 2.7 V to 5.25 V	200	50		kSPS
				1000	500	kSPS
$t_{CONVERT}$	Conversion (Hold) Time	$V_A = V_D$ = 2.7 V to 5.25 V			13	SCLK cycles
DC	SCLK Duty Cycle	$V_A = V_D$ = 2.7 V to 5.25 V	40%	30%		
				70%	60%	
t_{ACQ}	Acquisition (Track) Time	$V_A = V_D$ = 2.7 V to 5.25 V			3	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time $V_A = V_D$ = 2.7 V to 5.25 V			16	SCLK cycles
t_{AD}	Aperture Delay	$V_A = V_D$ = 2.7 V to 5.25 V		4		ns

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6.7 Timing Specifications

The following specifications apply for $V_A = V_D = 2.7$ V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 3.2 MHz to 8 MHz, f_{SAMPLE} = 200 kSPS to 500 kSPS, and C_L = 50 pF. Maximum and minimum limits apply for $T_A = T_{MIN}$ to T_{MAX}; all other limits T_A = 25°C. See Figure 1, Figure 2, and Figure 3.

			MIN	NOM	MAX(1)	UNIT
t_{CSH}	$\overline{CS}$ Hold Time after SCLK Rising Edge		10	0		ns
t_{CSS}	$\overline{CS}$ Set-up Time prior to SCLK Rising Edge		10	4.5		ns
t_{EN}	$\overline{CS}$ Falling Edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT Access Time after SCLK Falling Edge			17	27	ns
t_{DHLD}	DOUT Hold Time after SCLK Falling Edge			4		ns
t_{DS}	DIN Set-up Time prior to SCLK Rising Edge		10	3		ns
t_{DH}	DIN Hold Time after SCLK Rising Edge		10	3		ns
t_{CH}	SCLK High Time		0.4 × t_{SCLK}			ns
t_{CL}	SCLK Low Time		0.4 × t_{SCLK}			ns
t_{DIS}	$\overline{CS}$ Rising Edge to DOUT High-Impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns

(1) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).

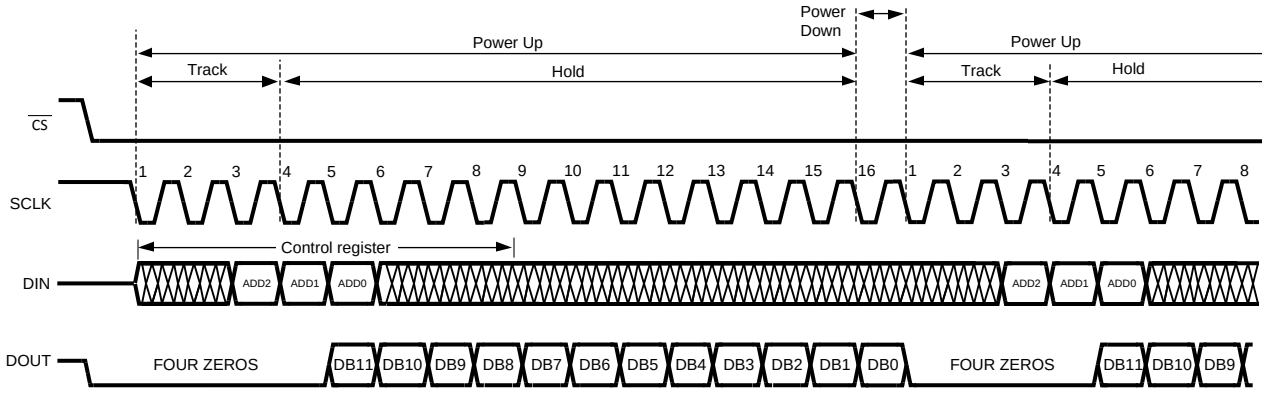

Figure 1. ADC128S052 Operational Timing Diagram

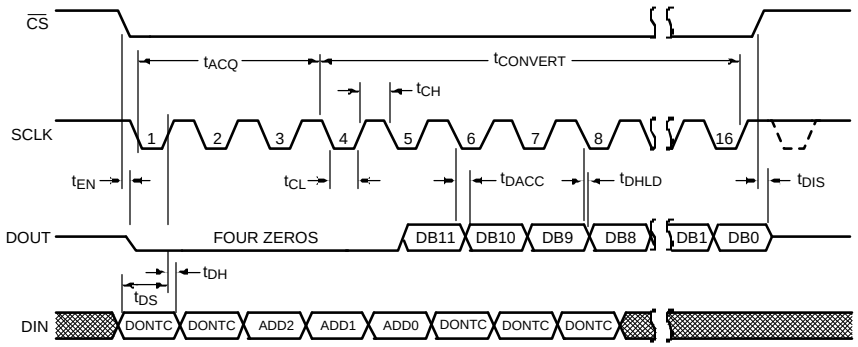

Figure 2. ADC128S052 Serial Timing Diagram

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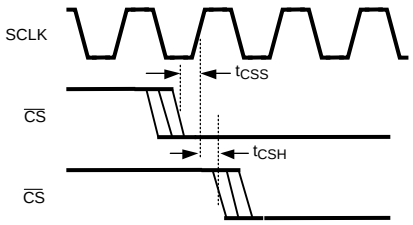

Figure 3. SCLK and $\overline{CS}$ Timing Parameters

6.8 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated

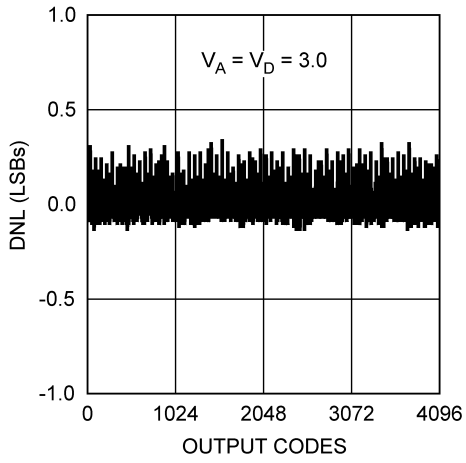

Figure 4. DNL

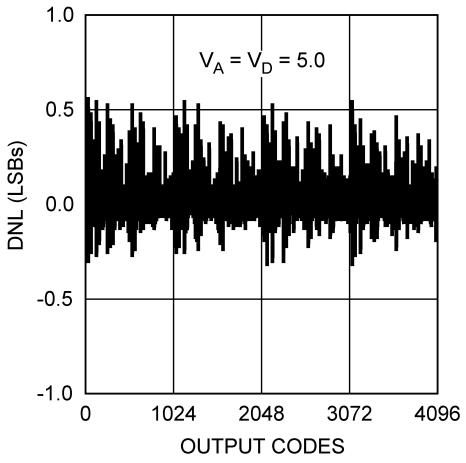

Figure 5. DNL

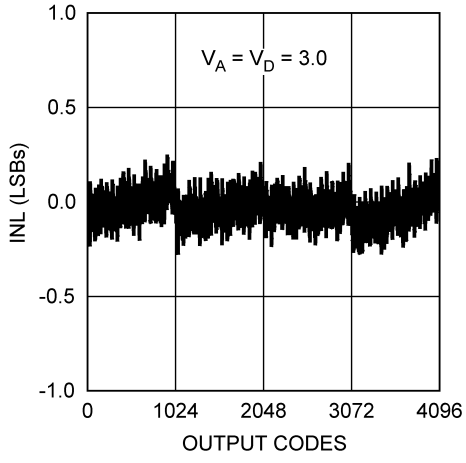

Figure 6. INL

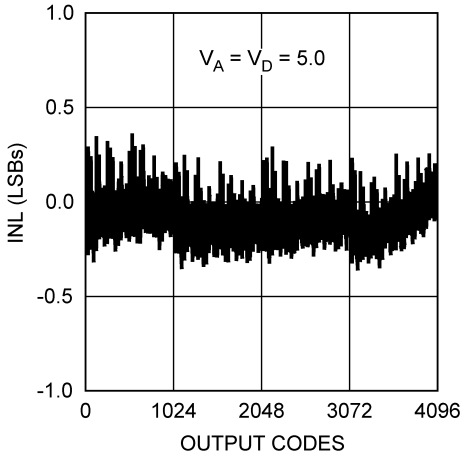

Figure 7. INL

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated

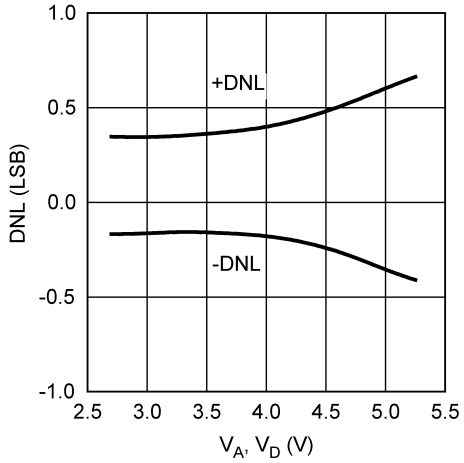


Figure 8. DNL vs Supply

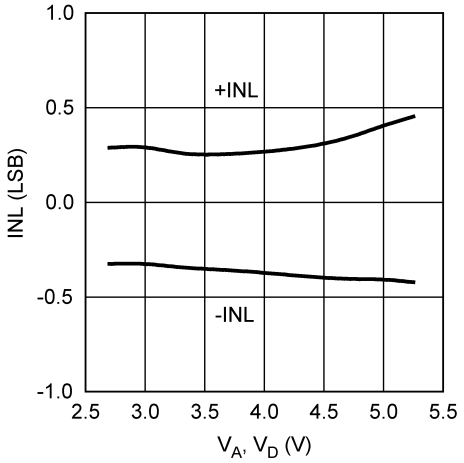


Figure 9. INL vs Supply

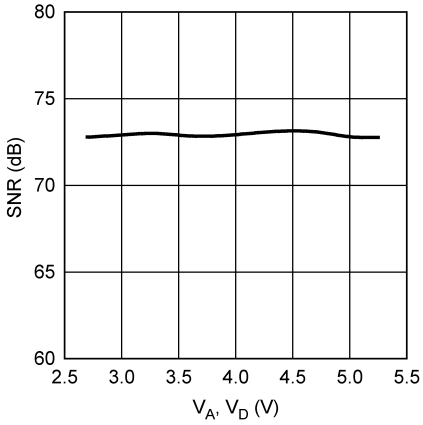


Figure 10. SNR vs Supply

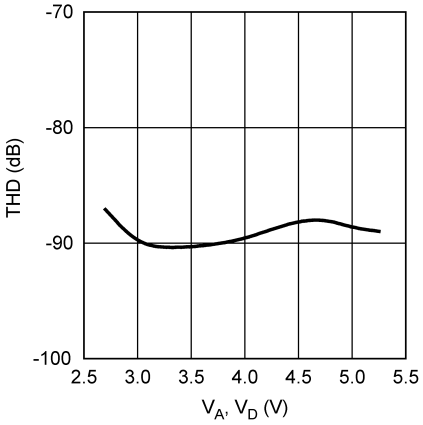


Figure 11. THD vs Supply

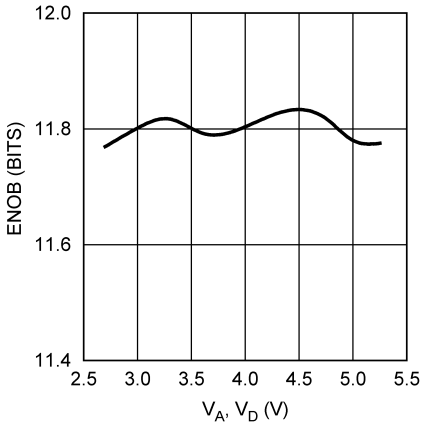
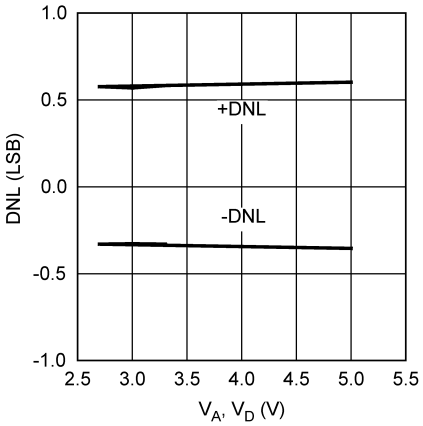


Figure 12. ENOB vs Supply



V_A = 5 V

Figure 13. DNL vs V_D

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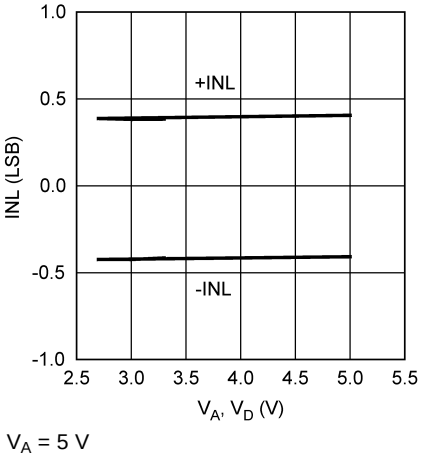
Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated



V_A = 5 V

Figure 14. INL vs V_D

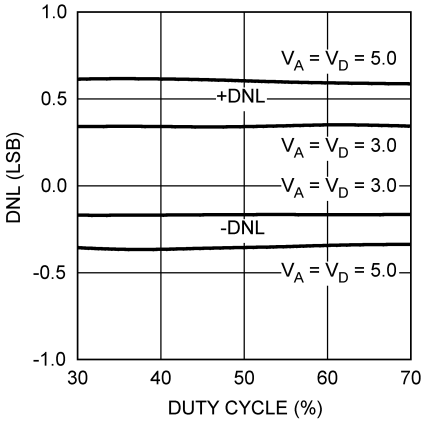


Figure 15. DNL vs SCLK Duty Cycle

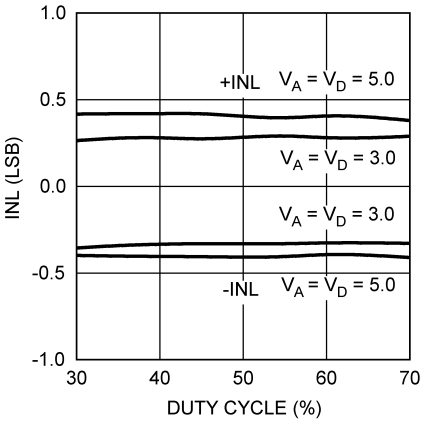


Figure 16. INL vs SCLK Duty Cycle

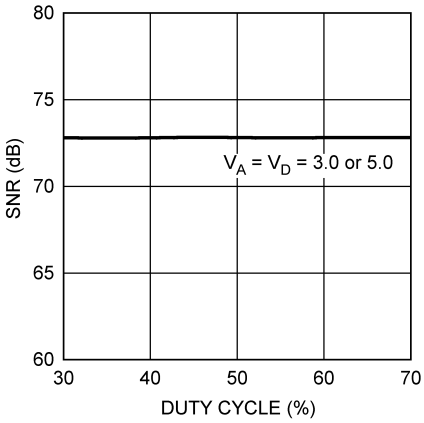


Figure 17. SNR vs SCLK Duty Cycle

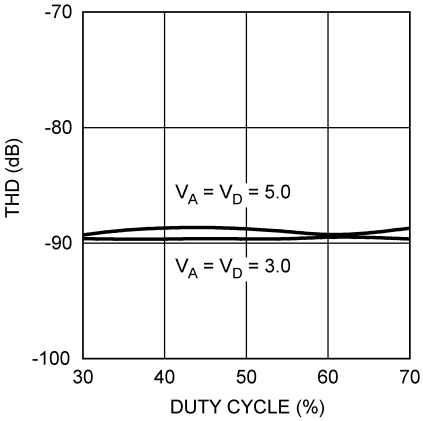


Figure 18. THD vs SCLK Duty Cycle

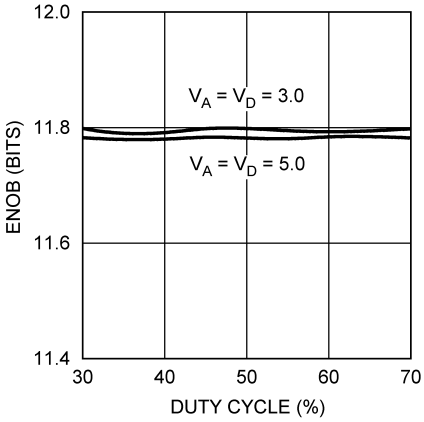


Figure 19. ENOB vs SCLK Duty Cycle

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated

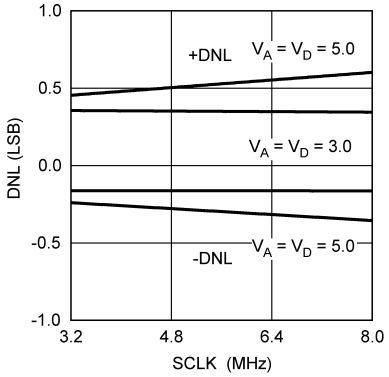

Figure 20. DNL vs SCLK

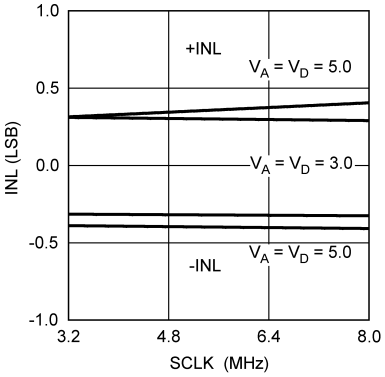

Figure 21. INL vs SCLK

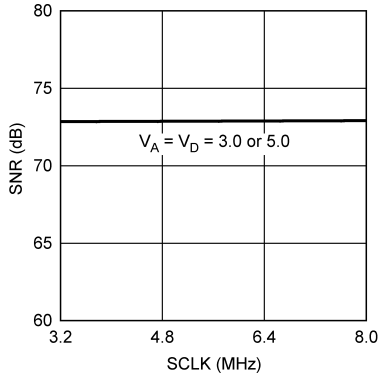

Figure 22. SNR vs SCLK

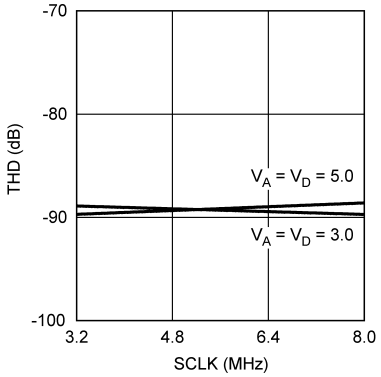

Figure 23. THD vs SCLK

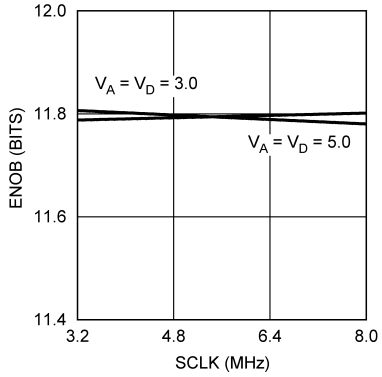

Figure 24. ENOB vs SCLK

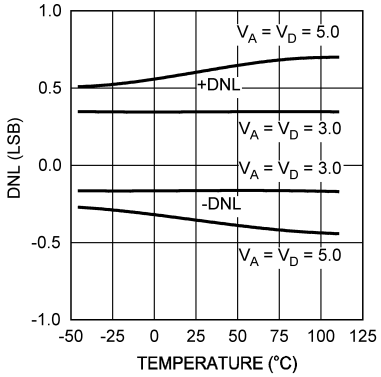

Figure 25. DNL vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated

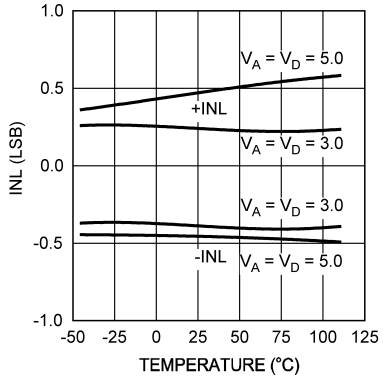

Figure 26. INL vs Temperature

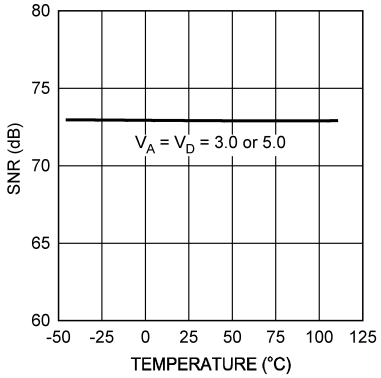

Figure 27. SNR vs Temperature

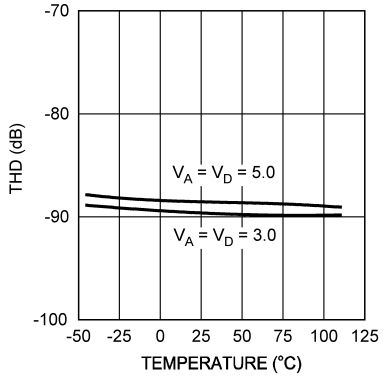

Figure 28. THD vs Temperature

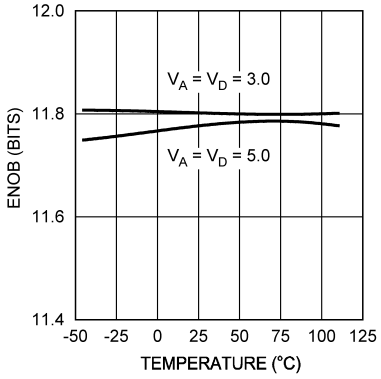

Figure 29. ENOB vs Temperature

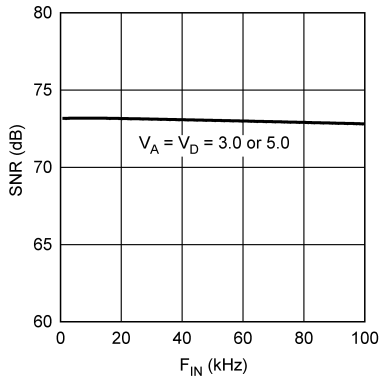

Figure 30. SNR vs Input Frequency

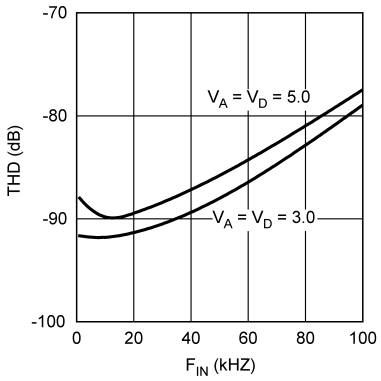

Figure 31. THD vs Input Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated

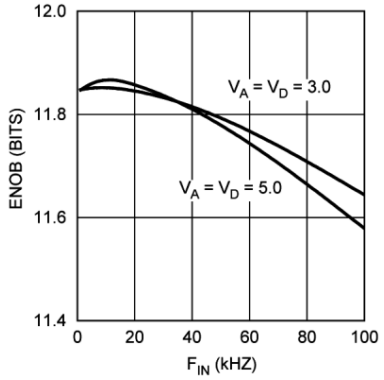

Figure 32. ENOB vs Input Frequency

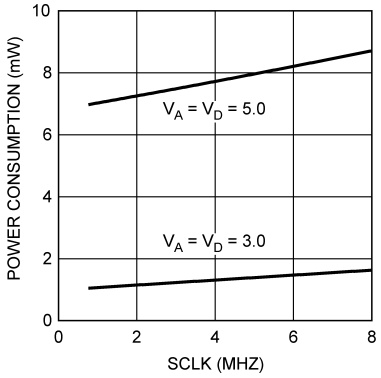

Figure 33. Power Consumption vs SCLK

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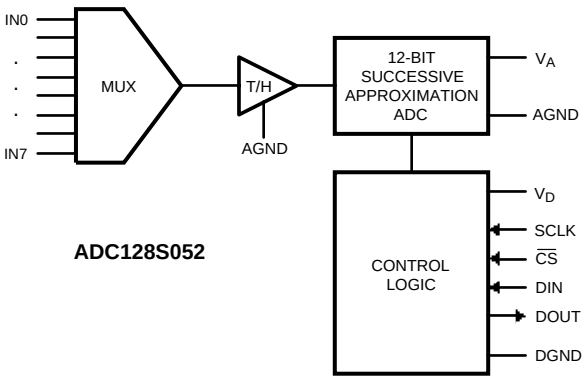
7 Detailed Description

7.1 Overview

The ADC128S052x is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. For the remainder of this document, ADC128S052x is abbreviated to ADC128S052.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

Simplified schematics of the ADC128S052 in both track and hold operation are shown in Figure 34 and Figure 35, respectively. In Figure 34, the ADC128S052 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S052 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 35 shows the ADC128S052 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S052 is in this state for the last thirteen SCLK cycles after $\overline{CS}$ is brought low.

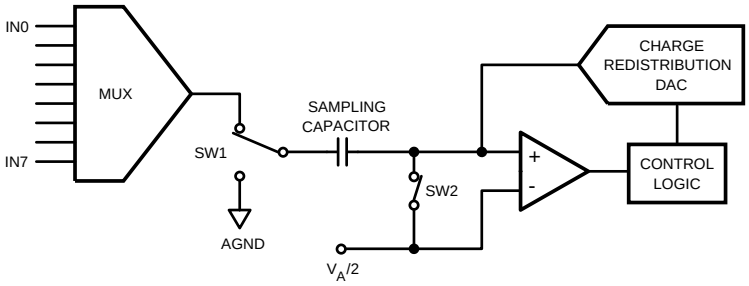


Figure 34. ADC128S052 in Track Mode

Feature Description (continued)

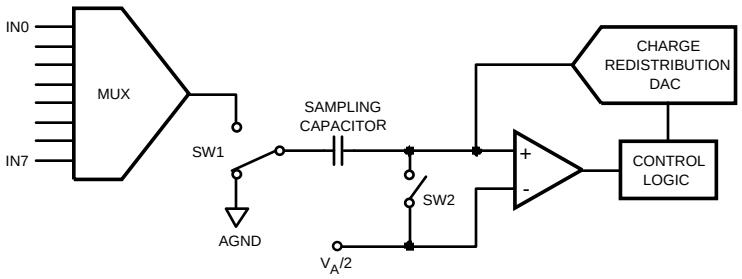


Figure 35. ADC128S052 in Hold Mode

7.3.2 Transfer Function

The output format of the ADC128S052 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S052 is V_A / 4096. The ideal transfer characteristic is shown in Figure 36. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 8192. Other code transitions occur at steps of one LSB.

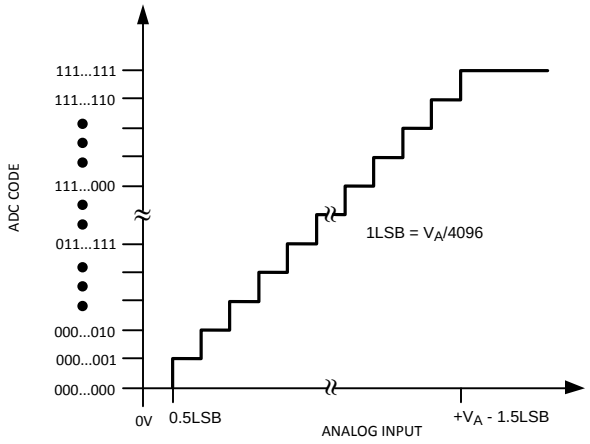


Figure 36. Ideal Transfer Characteristic

7.4 Device Functional Modes

The ADC128S052 is fully powered up whenever $\overline{CS}$ is low and fully powered down whenever $\overline{CS}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S052 automatically enters power-down mode between the SCLK 16th falling edge of a conversion and the SCLK 1st falling edge of the subsequent conversion (see Figure 1).

In continuous conversion mode, the ADC128S052 can perform multiple conversions back-to-back. Each conversion requires 16 SCLK cycles, and the ADC128S052 performs conversions continuously as long as $\overline{CS}$ is held low. Continuous mode offers maximum throughput.

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Device Functional Modes (continued)

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. Figure 33 in the *Typical Characteristics* section shows the typical power consumption of the ADC128S052. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in Equation 1.

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S \quad (1)$$

7.5 Programming

7.5.1 Serial Interface

Figure 1 shows a operational timing diagram, and Figure 2 shows a serial interface timing diagram for the ADC128S052. $\overline{CS}$ (chip select) initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the control register of the device is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Similarly, SCLK is internally gated off when $\overline{CS}$ is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished, and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC re-enters the track mode on the falling edge of SCLK after the N × 16th rising edge of SCLK and re-enter the hold/convert mode on the N × 16 + 4th falling edge of SCLK. *N* is an integer value.

The ADC128S052 enters track mode under three different conditions. In Figure 1, $\overline{CS}$ goes low with SCLK high, and the ADC enters track mode on the first falling edge of SCLK. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously, and the ADC enters track mode. While there is no timing restriction with respect to the rising edges of $\overline{CS}$ and SCLK, see Figure 3 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

While a conversion is in progress, the address of the next input for conversion is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. See Table 1, Table 2, Table 3.

There is no need to incorporate a power-up delay or dummy conversion as the ADC128S052 is able to acquire the input signal to full resolution in the first conversion immediately following power up. The first conversion result after power-up is that of IN0.

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7.6 Register Maps

Table 1. Control Register Bits

7	6	5	4	3	2	1	0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

Table 2. Control Register Bit Descriptions

BIT NO.	SYMBOL	DESCRIPTION
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel is sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 3.
4	ADD1	
3	ADD0	

Table 3. Input Channel Selection

ADD2	ADD1	ADD0	INPUT CHANNEL
0	0	0	IN0 (Default)
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Analog Inputs

An equivalent circuit for one of the input channels of the ADC128S052 is shown in Figure 37. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range causes the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 37 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track or hold switch and is typically 500 Ω. Capacitor C2 is the ADC128S052 sampling capacitor and is typically 30 pF. The ADC128S052 delivers best performance when driven by a low-impedance source (less than 100 Ω). This is especially important when using the ADC128S052 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

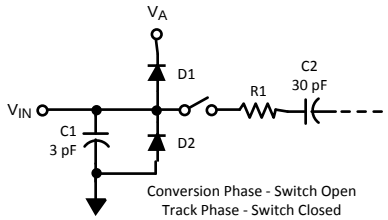

Figure 37. Equivalent Input Circuit

8.1.2 Digital Inputs and Outputs

The digital inputs (SCLK, $\overline{CS}$, and DIN) of the ADC128S052 have an operating range of 0 V to V_A. They are not prone to latch-up and may be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D – 0.5 V (minimum) while the output low voltage is 0.4 V (maximum).

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8.2 Typical Application

A typical application is shown in Figure 38. The analog supply is bypassed with a capacitor network located close to the ADC128S052. The ADC128S052 uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC128S052, it is also possible to use a precision reference as a power supply.

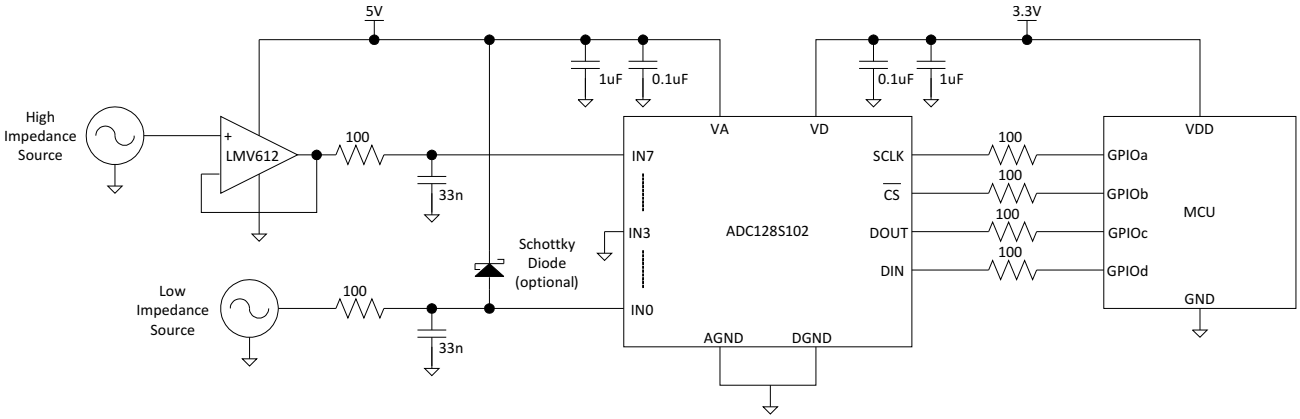

Figure 38. Typical Application Circuit

8.2.1 Design Requirements

A positive supply-only data acquisition system capable of digitizing signals ranging 0 to 5 V, BW = 10 kHz, and a throughput of 125 kSPS.

The ADC128S052 has to interface to a microcontroller with the supply is set at 3.3 V.

8.2.2 Detailed Design Procedure

The signal range requirement forces the design to use 5-V analog supply at V_A, analog supply. This follows from the fact that V_A is also a reference potential for the ADC.

The requirement of interfacing to the microcontroller which is powered by a 3.3-V supply, forces the choice of 3.3 V as a V_D supply.

Sampling is in fact a modulation process which may result in aliasing of the input signal, if the input signal is not adequately band limited. The maximum sampling rate of the ADC128S052 when all channels are enabled is, Fs is calculated by Equation 2:

$$F_s = \frac{F_{SCLK}}{16 \times 8} \tag{2}$$

Note that faster sampling rates can be achieved when fewer channels are sampled. Single channel can be sampled at the maximum rate of:

$$F_{s_single} = \frac{F_{SCLK}}{16} \tag{3}$$

In order to avoid the aliasing the Nyquist criterion has to be met:

$$BW_{signal} < \frac{F_s}{2} \tag{4}$$

Therefore it is necessary to place anti-aliasing filters at all inputs of the ADC. These filters may be single-pole low-pass filters. The pole locations need to satisfy, assuming all channels sampled in sequence, Equation 5 and Equation 6:

$$\frac{1}{\pi \times R \times C} < \frac{F_{SCLK}}{16 \times 8} \tag{5}$$

$$R \times C > \frac{128}{\pi \times F_{SCLK}} \tag{6}$$

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Typical Application (continued)

With F_{SCLK} = 16 MHz, a good choice for the single pole filter is:

- R = 100
- C = 33 nF

This reduces the input BW_{signal} = 48 kHz. The capacitor at the INx input of the device provides not only the filtering of the input signal, but it also absorbs the charge kick-back from the ADC. The kick-back is the result of the internal switches opening at the end of the acquisition period.

The V_A and V_D sources are already separated in this example, due to the design requirements. This also benefits the overall performance of the ADC, as the potentially noisy V_D supply does not contaminate the V_A. In the same vain, further consideration could be given to the SPI interface, especially when the master microcontroller is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path may help in reducing the ground bounce, and thus improve the overall noise performance of the system.

Take care when the signal source is capable of producing voltages beyond V_A. In such instances the internal ESD diodes may start conducting. The ESD diodes are not intended as input signal clamps. To provide the desired clamping action use Schottky diodes as shown in Figure 38.

8.2.3 Application Curve

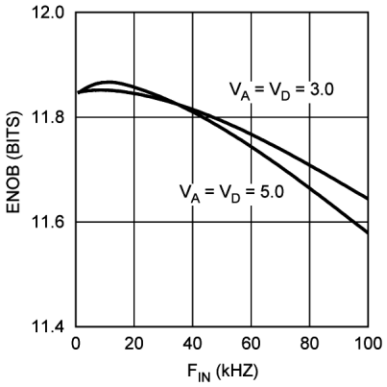

Figure 39. Typical Performance

9 Power Supply Recommendations

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

9.1 Power Supply Sequence

The ADC128S052 is a dual-supply device. The two supply pins share ESD resources, so exercise care to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV, not even on a transient basis. Therefore, V_A must ramp up before or concurrently with V_D.

9.2 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance causes voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply is coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, which is resistive. Load discharge currents causes *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution for keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improves noise performance. Because the series resistor and the load capacitor form a low frequency pole, verify signal integrity once the series resistor has been added.

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10 Layout

10.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC128S052 due to supply noise, do not use the same supply for the ADC128S052 that is used for digital logic.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line must also be treated as a transmission line and be properly terminated.

The analog input must be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (for example, a filter capacitor) connected between the input pins and ground of the converter or to the reference input pin and ground must be connected to a very clean point in the ground plane.

TI recommends the use of a single, uniform ground plane and the use of split power planes. The power planes must be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so forth) must be placed over the analog power plane. All digital circuitry and I/O lines must be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground must be connected together with short traces and enter the analog ground plane at a single, quiet point.

10.2 Layout Example

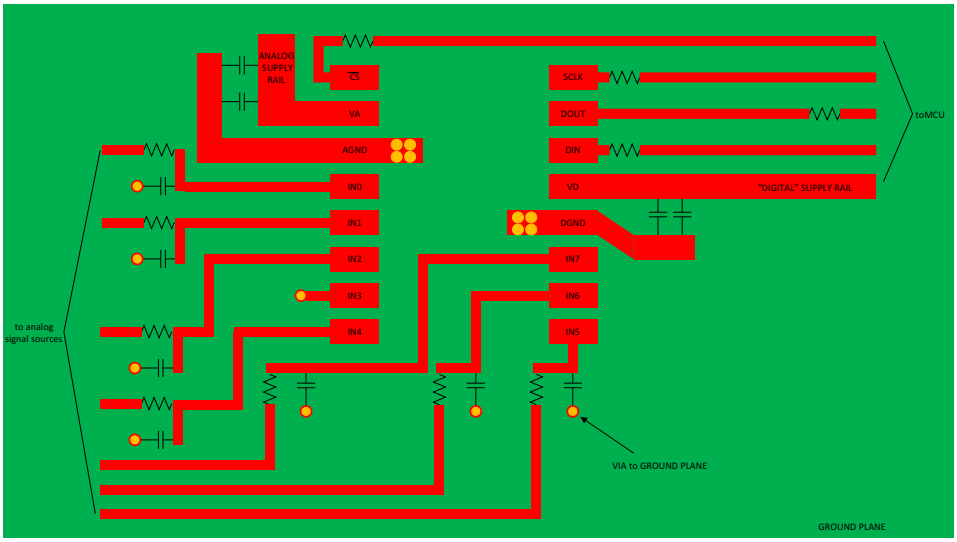

Figure 40. Layout Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CHANNEL-TO-CHANNEL ISOLATION is resistance to coupling of energy from one channel into another channel.

CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal 1½ LSB below V_{REF^+} and is defined as:

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+} \quad (7)$$

- where V_{max} is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in both the second or the third order intermodulation products to the power in one of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are ($2f_a \pm f_b$) and ($f_a \pm 2f_b$). IMD is usually expressed in dB.

MISSING CODES are those output codes that never appear sat the ADC outputs. These codes cannot be reached with any input value. The ADC128S052 is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (that is, GND + 0.5 LSB).

SIGNAL-TO-NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or the harmonics included in THD.

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Device Support (continued)

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f10}^2}{A_{f1}^2}} \quad (8)$$

- where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion and read out times. In the case of the ADC128S052, this is 16 SCLK periods.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC128S052	Click here	Click here	Click here	Click here	Click here
ADC128S052-Q1	Click here	Click here	Click here	Click here	Click here

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11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC128S052CIMT/NO.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 CIMT
ADC128S052CIMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 CIMT
ADC128S052CIMTX/NO.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 CIMT
ADC128S052CIMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 CIMT
ADC128S052QCMT/NO.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 QCMT
ADC128S052QCMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 QCMT
ADC128S052QCMTX/NO.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 QCMT
ADC128S052QCMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S052 QCMT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADC128S052, ADC128S052-Q1 :

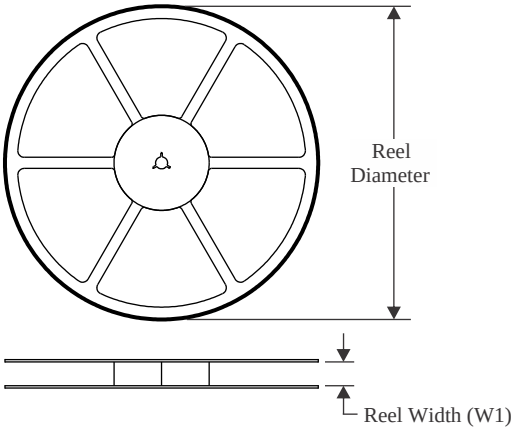
- Catalog : ADC128S052
- Automotive : ADC128S052-Q1

NOTE: Qualified Version Definitions:

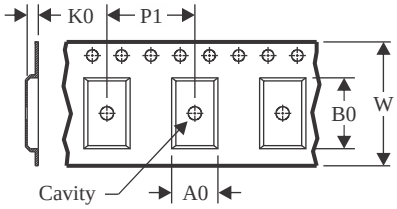
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

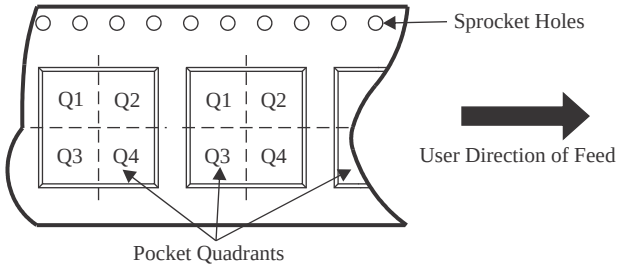


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

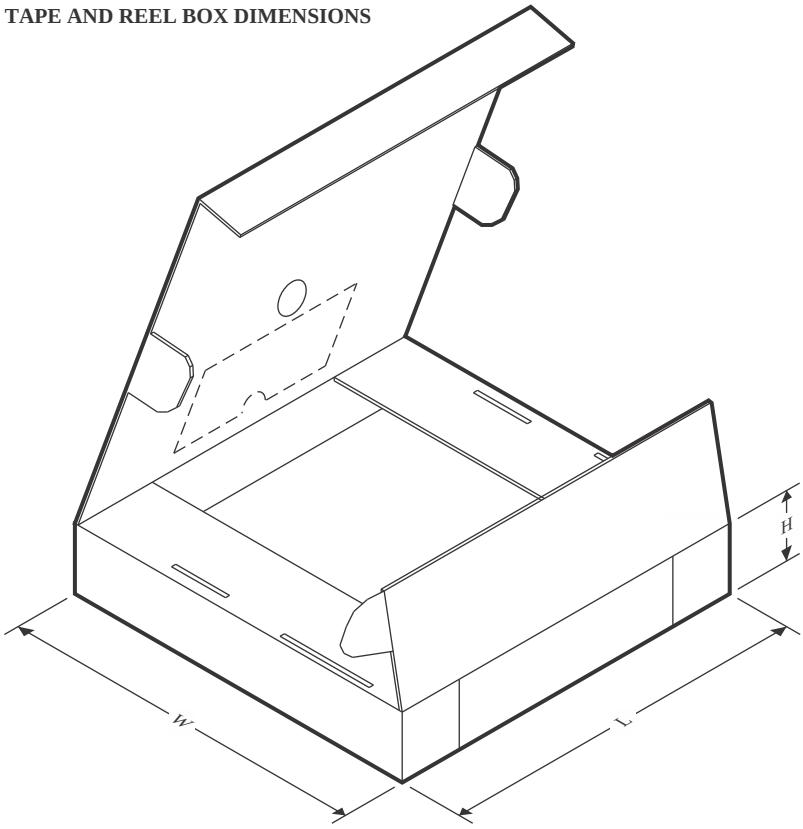
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC128S052CIMTX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
ADC128S052QCMTX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

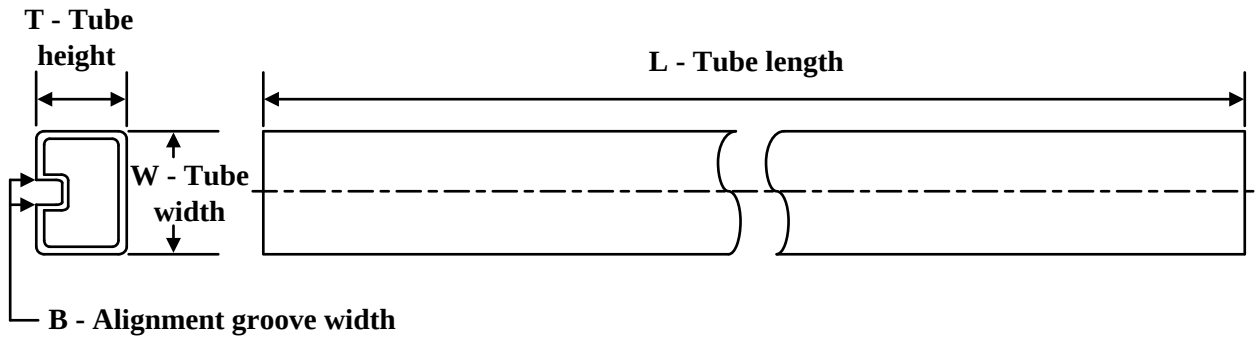
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC128S052CIMTX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
ADC128S052QCMTX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

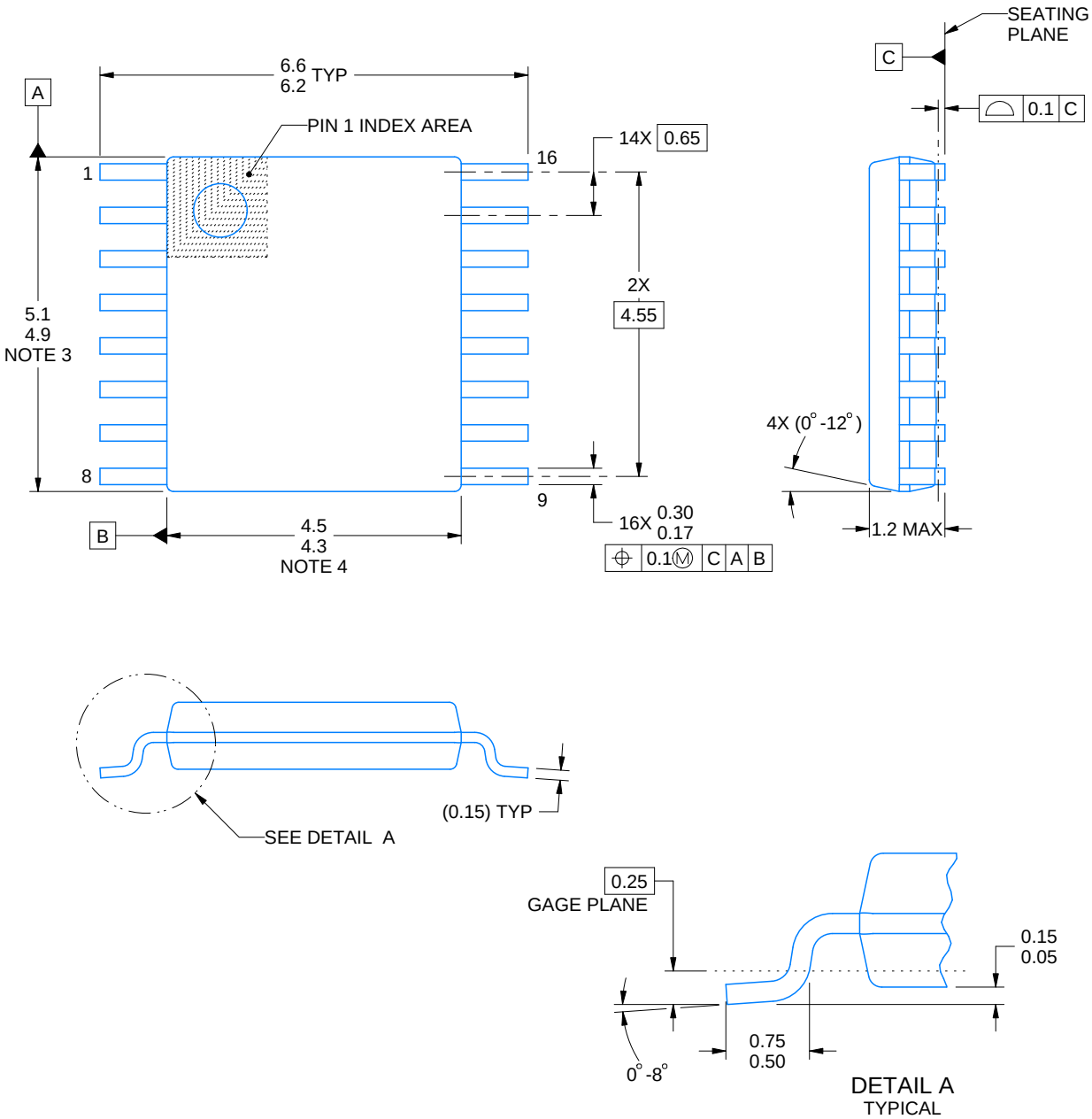
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADC128S052CIMT/NO.A	PW	TSSOP	16	92	495	8	2514.6	4.06
ADC128S052CIMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
ADC128S052QCMT/NO.A	PW	TSSOP	16	92	495	8	2514.6	4.06
ADC128S052QCMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

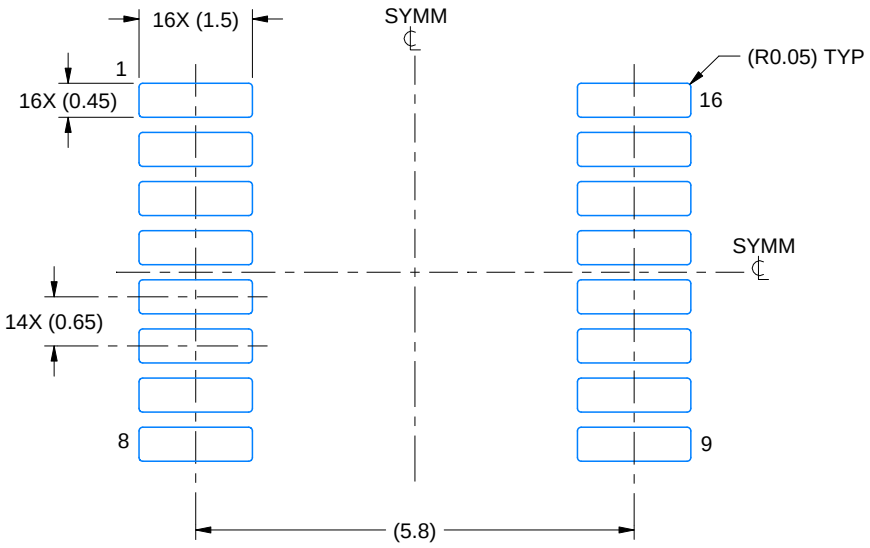
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

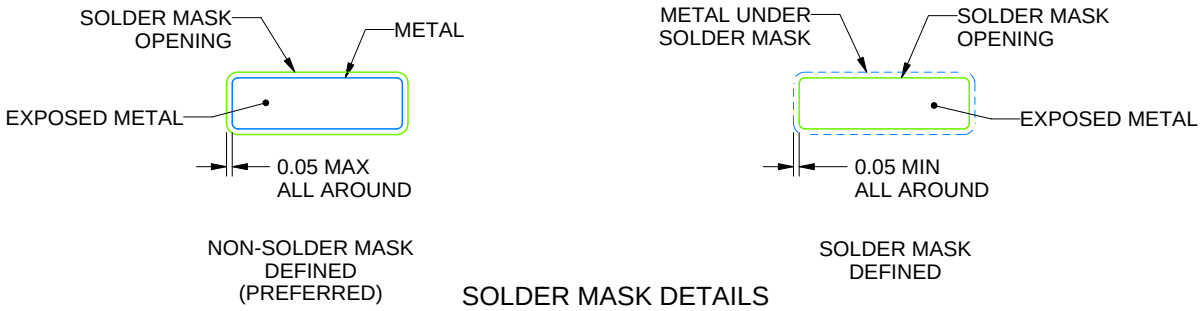


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

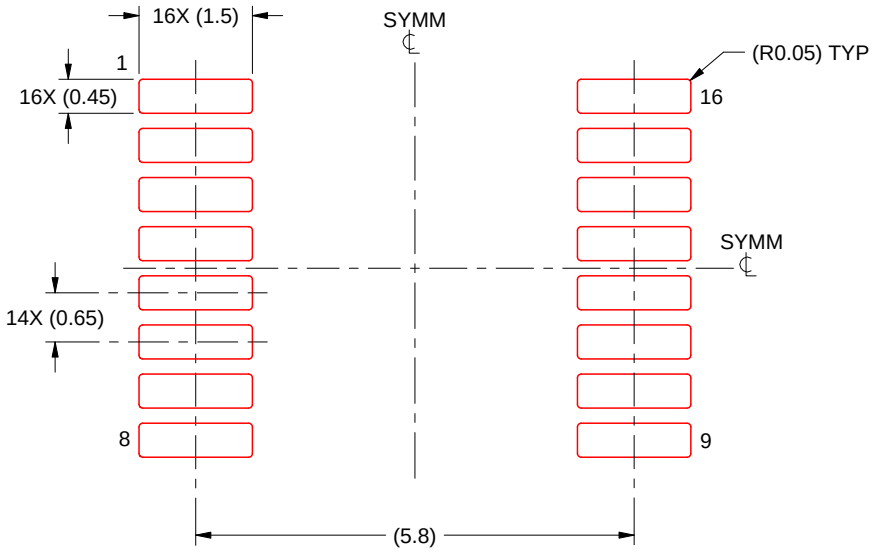


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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