

ADC810-Q1 Automotive 12-bit, 8 channel 3.3-kSPS SAR ADC and 10 channel I/O Expander with I²C interface

1 Features

- Combined Serial ADC + IO Expander
 - Customizable ADC or Digital I/O pin functionality
- Wide supply range: 1.62V to 3.6V
- I²C to Parallel port expander
- ADC resolution: 12 bits
- Programmable data rate: 128SPS to 3.3kSPS
- Configurable Internal voltage reference
- Internal oscillator
- I²C interface: Two pin-selectable addresses
 - 5-V Tolerant
- Up to 10 digital I/Os
- 400kHz Fast I2C Bus
- Internal power-on reset
- ESD Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 and Charged device model (CDM), per JEDEC specification JESD22-C101
- Operating temperature range: -40°C to +125°C

2 Applications

- [Camera modules without processing](#)
- [Automotive center information displays](#)
- [Automotive cluster displays](#)
- [General-purpose voltage and current monitoring](#)

3 Description

The ADC810-Q1 is an I/O expander device that includes a 12-bit, I²C-compatible, analog-to-digital converter (ADC) and provides 8-bits of general-purpose parallel input/output offered in a SOT-16 package. The ADC810-Q1 incorporates an internal voltage reference and an oscillator. The ADC810-Q1 also incorporates a programmable internal voltage reference and a digital comparator. These features, along with a wide operating supply range, are useful for power- and space-constrained, sensor measurement applications.

The device performs conversions at data rates up to 3300 samples per second (SPS). The VREF offers values of 1.4V, 2.5V, and VDD. The ADC810-Q1 features an input multiplexer (MUX) that allows eight single-ended input measurements. The digital comparator in the AC810 can be used for under- and overvoltage detection.

The ADC810-Q1 operates in either continuous-conversion mode or single-shot mode. Data are transferred through an I²C-compatible serial interface.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ADC810-Q1	DYY (SOT, 16)	4.2mm × 3.26mm

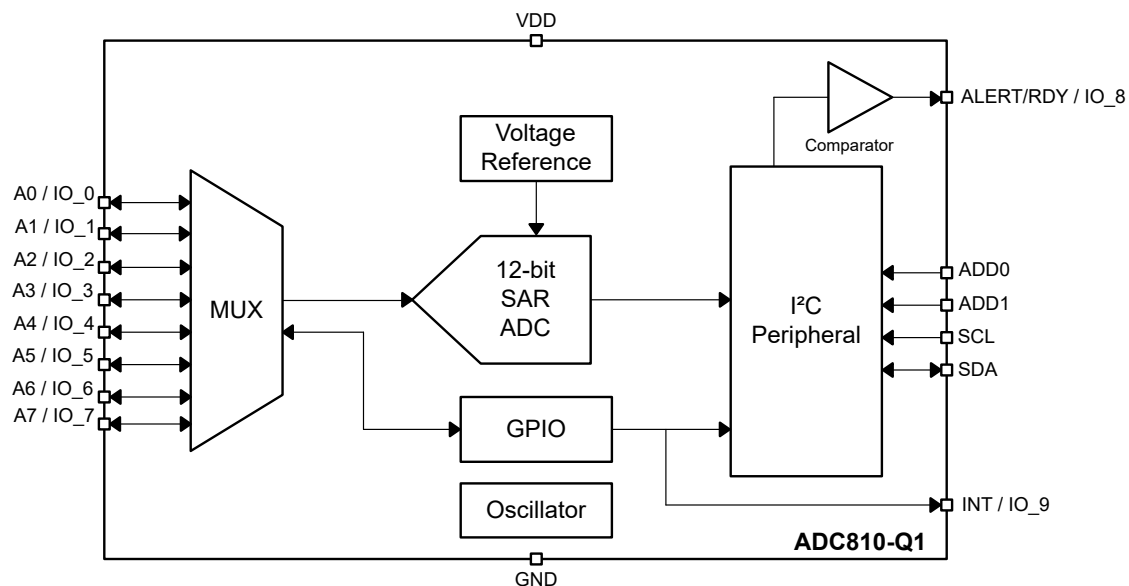
(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	INPUT CHANNELS / IO Numbers	FEATURES
ADC810QDYYRQ1	8 A / 10 IO	VREF, comparator, IO Control





Simplified Block Diagram

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4 Pin Configuration and Functions

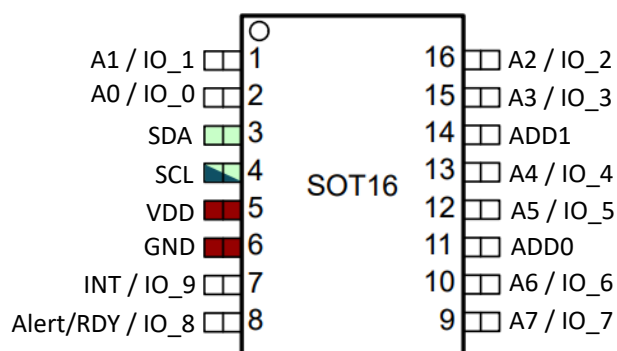


**Figure 4-1. SOT Package,
16-Pin(Top View)**

Table 4-1. Pin Function: SOT package

PIN		TYPE	DESCRIPTION
NAME	ADC810-Q1		
A1 / IO_1	1	Analog input / Digital I/O	Analog input 1 / Digital I/O 1
A0 / IO_0	2	Analog input / Digital I/O	Analog input 0 / Digital I/O 0
SDA	3	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.
SCL	4	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
VDD	5	Analog	Power supply. Connect a 10µF power capacitor, and a 0.1µF, power-supply decoupling capacitor to GND.
GND	6	Analog	Ground
INT / IO_9	7	Digital Output / Digital I/O	Interrupt output / Digital I/O 9 Open-drain output. Connect to VDD using a pullup resistor.
ALERT/RDY / IO_8	8	Digital Output / Digital I/O	Comparator output or conversion ready / Digital I/O 8 Open-drain output. Connect to VDD using a pullup resistor.
A7 / IO_7	9	Analog input / Digital I/O	Analog input 7 / Digital I/O 7

Table 4-1. Pin Function: SOT package (continued)

PIN		TYPE	DESCRIPTION
NAME	ADC810-Q1		
A6 / IO_6	10	Analog input / Digital I/O	Analog input 6 / Digital I/O 6
ADD0	11	Digital input	I ² C target address select 0
A5 / IO_5	12	Analog input / Digital I/O	Analog input 5 / Digital I/O 5
A4 / IO_4	13	Analog input / Digital I/O	Analog input 4 / Digital I/O 4
ADD1	14	Digital input	I ² C target address select 1
A3 / IO_3	15	Analog input / Digital I/O	Analog input 3 / Digital I/O 3
A2 / IO_2	16	Analog input / Digital I/O	Analog input 2 / Digital I/O 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	−0.3	4.1	V
V _I	Input voltage	Applied to 5-V tolerant I2C open-drain pins	−0.3	5.5	V
V _I	Input voltage	Applied to any common tolerance pins	−0.3	V _{DD} + 0.3 (4.1 MAX)	V
I _{VDD}	Current of VDD pin	Current into VDD pin (source), −40 °C ≤ T _a ≤ 85 °C		80	mA
I _{VSS}	Current of VSS pin	Current out of VSS pin (sink), −40 °C ≤ T _a ≤ 85 °C		80	mA
I _{VDD}	Current of VDD pin	Current into VDD pin (source), −40 °C ≤ T _a ≤ 125 °C		48	mA
I _{VSS}	Current of VSS pin	Current out of VSS pin (sink), −40 °C ≤ T _a ≤ 125 °C		48	mA
I _{IO}	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	mA
I _{IO}	Current for I2CIO pins	Current sunk by I2CIO Pins		20	mA
I _D	Supported diode current	Diode current at any device pin except A3/IO_3		±2 ⁽²⁾	mA
T _{stg}		Storage temperature	−40	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, which may affect its reliability, functionality, and performance, and shorten its lifetime.
- (2) Open drain IOs I2C_SDA and I2C_SCL do not have the high side clamps, and A3/IO_3 has an internal connection for the testing purpose, there is no injection current allowed on these pins.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins ⁽¹⁾	±2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per pAEC Q100-011, all pins	±500	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per AEC-Q100-011, Corner pins	±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
IDD	Operating current - 25 °C		1.2		mA
	Operating current - 125 °C		1.6	4	
C _{VDD}	Capacitor placed between VDD and VSS ⁽¹⁾		10		uF
T _A	Ambient temperature	−40		125	°C
T _J	Max junction temperature			130	°C

- (1) Connect C_{VDD} between VDD/VSS, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PACKAGE	VALUE	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	SOT-16 (DYY)	117.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		54.5	°C/W
R _{θJB}	Junction-to-board thermal resistance		54.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter		3.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter		54.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 POR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling			0.01	
V _{POR}	Power-on reset voltage level	Cold start, rising ⁽¹⁾	1.48	1.54	1.615	V
V _{HYS,POR}	POR reset hysteresis			34	41	mV

(1) |dVDD/dt| ≤ 3V/s

5.6 Timing Characteristics

VDD=3.3V, T_a=25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup Timing						
t _{START, RESET}	Device cold start-up time from reset/power-up ⁽¹⁾			780		us

(1) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

5.7 Analog/Digital IO

5.7.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IH}	High level input voltage	I ₂ CIO ⁽¹⁾	VDD ≥ 1.62V	0.7*VDD		5.5	V
		I ₂ CIO ⁽¹⁾	VDD ≥ 2.7V	2		5.5	V
		All I/O except I ₂ CIO	VDD ≥ 1.62V	0.7*VDD		VDD+0.3	V
V _{IL}	Low level input voltage	I ₂ CIO	VDD ≥ 1.62V	-0.3		0.3*VDD	V
		I ₂ CIO	VDD ≥ 2.7V	-0.3		0.8	V
		All I/O except I ₂ CIO	VDD ≥ 1.62V	-0.3		0.3*VDD	V
V _{HYS}	Hysteresis	I ₂ CIO		0.05*VDD			V
		All I/O except I ₂ CIO		0.1*VDD			V
I _{lkg}	High-Z leakage current	SDIO ⁽²⁾⁽³⁾	VDD = 3V			50	nA
C _I	Input capacitance		VDD = 3.3V		5		pF
V _{OH}	High level output voltage	SDIO	VDD ≥ 2.7V, I _{IO} _{max} = 6mA		VDD-0.5		V

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High level output voltage SDIO	VDD ≥ 1.71V, I _{OL} _{max} = 2mA		VDD-0.4	V
V _{OL}	Low level output voltage SDIO	VDD ≥ 2.7V, I _{OL} _{max} = 6mA VDD ≥ 1.71V, I _{OL} _{max} = 2mA		0.4	V
V _{OL}	Low level output voltage I2CIO	VDD ≥ 2.7V, I _{OL} _{max} = 8mA VDD ≥ 1.71V, I _{OL} _{max} = 4mA		0.5	V

- (1) I/O Types: I2CIO= I2C 5V Tolerant Open-Drain, SDIO = Standard-Drive (Includes ADD pins)
- (2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
- (3) The leakage of the Analog/Digital pins is measured individually. The port pin is selected for input, and the pullup/pulldown resistor is disabled.

5.7.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Port output frequency I2CIO	VDD ≥ 1.71V, FM, CL= 20pF - 100pF		400	kHz
t _r , t _f	Output rise/fall time All output ports except I2CIO	VDD ≥ 1.71V		1/ (0.3*24M Hz)	s
t _f	Output fall time I2CIO	VDD ≥ 1.71V, FM, CL= 20pF-100pF	20*VDD/5.5	120	ns

5.8 ADC

5.8.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN(ADC)}	Analog input voltage range ⁽¹⁾ Applies to all ADC analog input pins	0		VDD	V
V _{R+}	Positive ADC reference voltage V _{R+} sourced from VDD		VDD		V
	V _{R+} sourced from internal reference (VREF)		VREF		V
V _{R-}	Negative ADC reference voltage		0		V
F _s	ADC sampling frequency VDD Reference	.128		3.3	ksps
	Internal Reference (1.4V and 2.5V)	.128		3.3	ksps
C _{S/H}	ADC sample-and-hold capacitance		0.22		pF
R _{in}	ADC switch resistance		25		kΩ
ENOB	Effective number of bits VDD reference ⁽²⁾	9.3	10.4		bit
	Internal reference, V _{R+} = VREF = 2.5V	9.4	9.8		bit
SNR	Signal-to-noise ratio VDD reference ⁽²⁾		64		dB
	Internal reference, V _{R+} = VREF = 2.5V		61		dB
PSRR _{DC}	Power supply rejection ratio, DC VDD = VDD _(min) to VDD _(max) Internal reference, V _{R+} = VREF = 2.5V		61		dB

- (1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (2) VDD reference specifications are measured with V_{R+} = VDD = 3.3V and V_{R-} = VSS = 0V

5.8.2 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
E _I	Integral linearity error (INL) VDD reference, 12-bit ⁽²⁾	-4.0		+4.0	LSB
	Internal reference, 12-bit, V _{R+} = VREF = 2.5V	-4.0		+4.0	LSB
E _D	Differential linearity error (DNL) VDD reference, 12-bit ⁽²⁾	-1.0		+4.0	LSB
	Internal reference, 12-bit, V _{R+} = VREF = 2.5V	-1.0		+4.0	LSB

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E _O	Offset error	VDD reference, 12-bit ⁽²⁾	-3		3	mV
		Internal reference, 12-bit, V _{R+} = VREF = 2.5V	-5		5	mV
E _G	Gain error	VDD reference, 12-bit ⁽²⁾	-25		25	LSB
		Internal reference, 12-bit, V _{R+} = VREF = 2.5V	-75		75	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I, E_O, and E_G using the following formula: $TUE = \sqrt{E_I^2 + |E_O|^2 + E_G^2}$

Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate

(2) VDD reference specifications are measured with V_{R+} = VDD and V_{R-} = VSS = 0V.

5.8.3 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{Sample_period}	Sampling time for input			125		μs

5.9 VREF

5.9.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TC _{VREF}	Temperature coefficient of VREF	1.4V or 2.5V	1.4V or 2.5V			75	ppm/°C
TC _{drift}	Long term VREF drift	Time = 1000 hours, 1.4V or 2.5V, T = 25°C	Time = 1000 hours, 1.4V or 2.5V, T = 25°C			300	ppm

5.9.2 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD _{min}	Minimum supply voltage needed for VREF operation	Vref = 1.4V	1.62			V
		Vref = 2.5V	2.7			
VREF	Voltage reference output voltage	Vref = 1.4V	1.378	1.4	1.421	V
		Vref = 2.5V	2.462	2.5	2.541	

5.10 I2C

5.10.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Fast mode		UNIT
			MIN	MAX	
f _{SCL}	SCL clock frequency			400	kHz
t _{HD,STA}	Hold time (repeated) START		0.6		us
t _{LOW}	LOW period of the SCL clock		1.3		us
t _{HIGH}	High period of the SCL clock		0.6		us
t _{SU,STA}	Setup time for a repeated START		0.6		us
t _{HD,DAT}	Data hold time		0		ns
t _{SU,DAT}	Data setup time		100		ns
t _{SU,STO}	Setup time for STOP		0.6		us

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Fast mode		UNIT
			MIN	MAX	
t _{BUF}	bus free time between a STOP and START condition		1.3		us
t _{VD,DAT}	data valid time			0.9	us
t _{VD,ACK}	data valid acknowledge time			0.9	us

6 Detailed Description

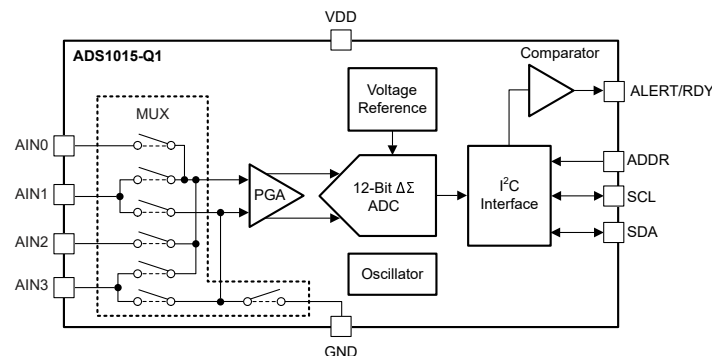
6.1 Overview

The ADC810-Q1 is a 12-bit, SAR analog-to-digital converter (ADC) and 10-bit I/O expander. It consists of a SAR ADC core with an internal voltage reference, a clock oscillator, a programmable digital comparator, I/O expander capabilities, and an I²C interface. Figure 6-1 shows the functional block diagrams of the ADC810-Q1. At power on, the I/O pins (except for I/O 8 and I/O 9) will default to analog, and the ADC results will be formatted in two's complement.

The ADC810-Q1 offers two available ADC conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the conversion value to an internal conversion register. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflects the most recent completed conversion.

The ADC810-Q1 I/O expander module can be controlled through the I/O registers. The capabilities range from output control to inversion input control. The open-drain interrupt (INT) output is activated when any input state differs from its corresponding Input Port Register state and is used to indicate to the system controller that an input state has changed. INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus.

6.2 Functional Block Diagrams



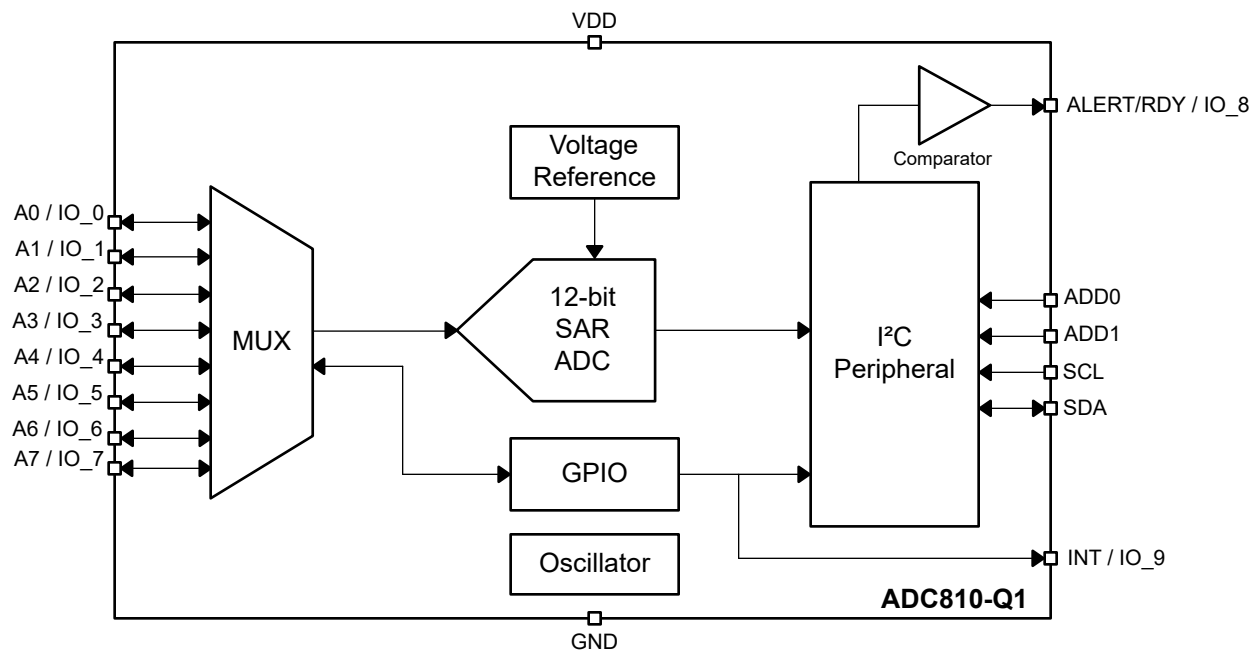


Figure 6-1. ADC810-Q1 Block Diagram

6.3 Feature Description

6.3.1 Multiplexer

The ADC810-Q1 contains an input multiplexer that can track whether a pin is set as an analog pin or a digital pin. The Pin Function register configures the multiplexer register. If a pin is to be an analog pin, the pin will connect to the ADC and can be used to analyze analog signals. The selected channel can be configured by bits MUX[2:0] in the ADC Configuration register.

If set to a digital pin, the pin will be connected to the GPIO module. When an I/O is configured as an input, the pin is left at a high-impedance input. Electrostatic discharge (ESD) diodes connected to VDD and GND protect

the ADC810-Q1 inputs. For IO8 and IO9, the analog mode is not available. Instead, the pins are set to their respective Alert functionality (ALERT/RDY and INT, respectively). The pins can be set as digital pins, however.

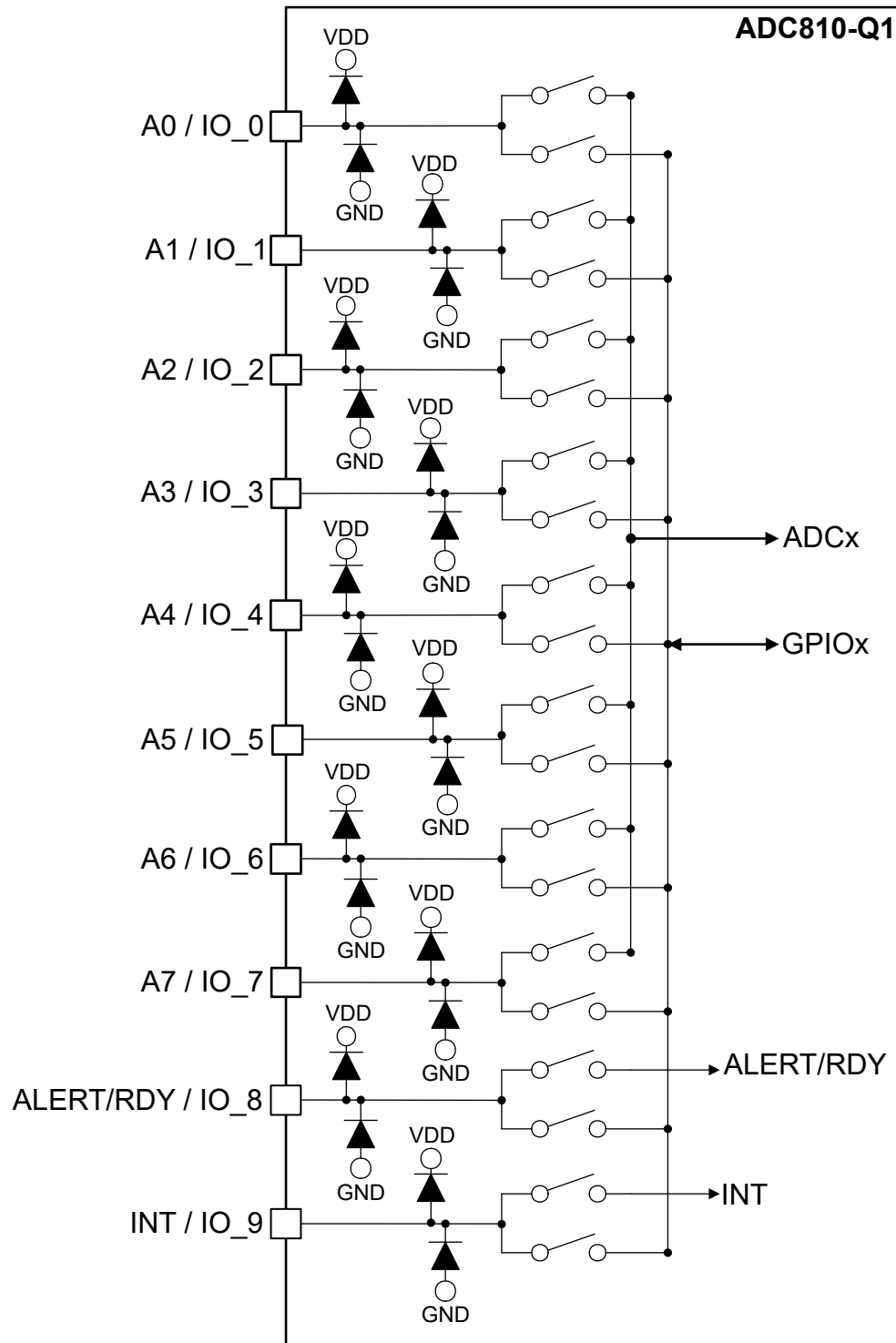


Figure 6-2. Input Multiplexer

6.3.2 Voltage Reference

The ADC810-Q1 has an integrated voltage reference. An external reference cannot be used with these devices. The ADC810-Q1 internal voltage reference can be configured through the VREF bits inside the ADC Configuration register.

6.3.3 Oscillator

The ADC810-Q1 has an integrated oscillator running at 24MHz. No external clock can be applied to operate these devices. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

6.3.4 Output Data Rate and Conversion Time

The ADC810-Q1 offers programmable output data rates. Use the DR[2:0] bits in the [ADC Configuration register](#) to select output data rates of 128SPS, 250SPS, 490SPS, 920SPS, 1600SPS, 2400SPS, or 3300SPS.

Conversions in the ADC810-Q1 settle within a single cycle; thus, the conversion time is equal to $1 / DR$.

6.3.5 Digital Comparator

The ADC810-Q1 features a programmable digital comparator that can issue an alert on the ALERT/RDY pin. The COMP_MODE bit in the [ADC Configuration register](#) configures the comparator as either a traditional comparator or a window comparator. In traditional comparator mode, the ALERT/RDY pin asserts (active low by default) when conversion data exceeds the limit set in the high-threshold register (High_thresh). The comparator then deasserts only when the conversion data falls below the limit set in the low-threshold register (Low_thresh). In window comparator mode, the ALERT/RDY pin asserts when the conversion data exceed the High_thresh register or fall below the Low_thresh register value.

In either window or traditional comparator mode, the comparator can be configured to latch after being asserted by the COMP_LAT bit in the ADC Configuration register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can only be cleared by reading the [ADC Conversion register](#). The ALERT/RDY pin can be configured as active high or active low by the COMP_POL bit in the ADC Configuration register. Operational diagrams for both the comparator modes are shown in [Figure 6-3](#).

The comparator can also be configured to activate the ALERT/RDY pin only after a set number of successive readings exceed the threshold values set in the threshold registers (High_thresh and Low_thresh). The COMP_QUE[1:0] bits in the ADC Configuration register configures the comparator to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin. The COMP_QUE[1:0] bits can also disable the comparator function, and put the ALERT/RDY pin into high-impedance.

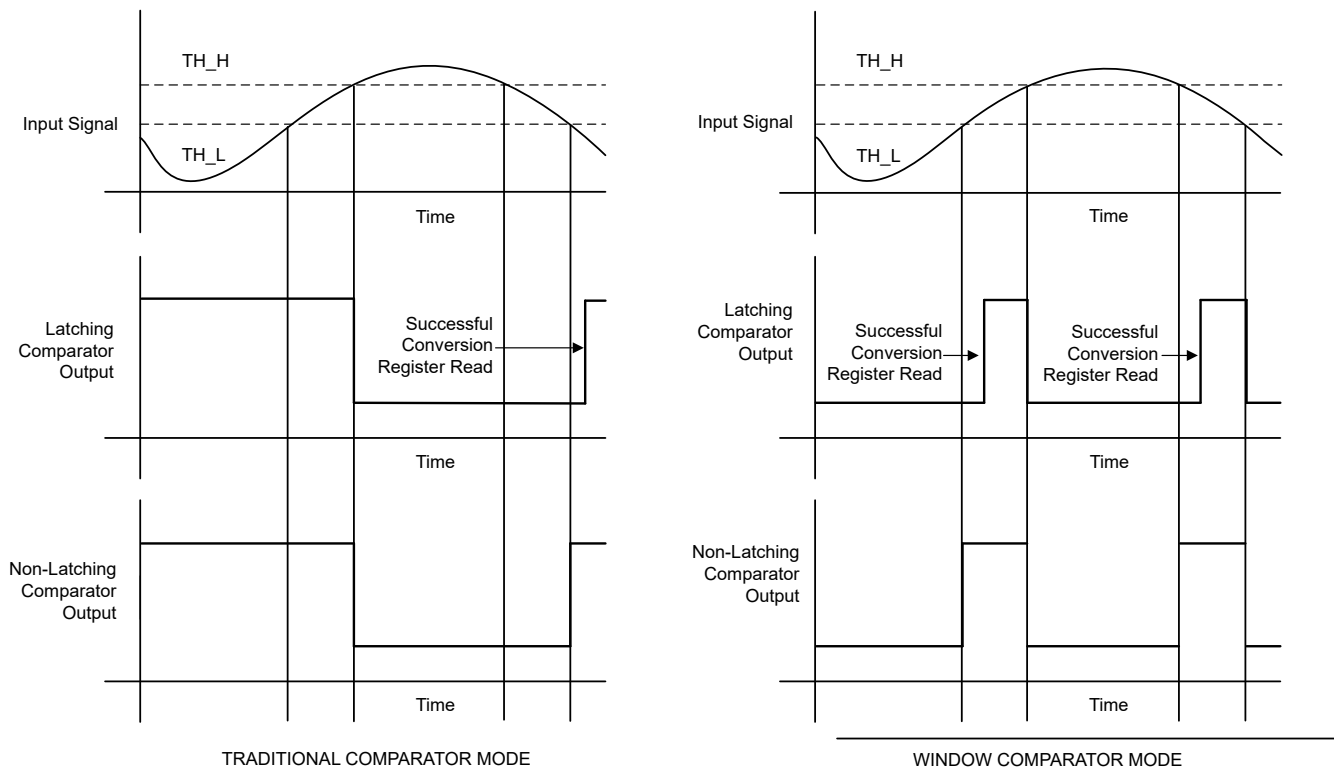


Figure 6-3. ALERT Pin Timing Diagram

6.3.6 Conversion Ready Pin

The ALERT/RDY pin can also be configured as a conversion ready pin. Set the most-significant bit of the High_thresh register to 1b and the most-significant bit of Low_thresh register to 0b to enable the pin as a conversion-ready pin. The COMP_POL bit continues to function as expected. Set the COMP_QUE[1:0] bits to any 2-bit value other than 11b to keep the ALERT/RDY pin enabled, and allow the conversion-ready signal to appear at the ALERT/RDY pin output. The COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion-ready pin, ALERT/RDY continues to require a pullup resistor. The ADC810-Q1 provide an approximately 8 μ s, conversion-ready pulse on the ALERT/RDY pin at the end of each conversion in continuous-conversion mode, as shown in Figure 6-4. In single-shot mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to 0b.

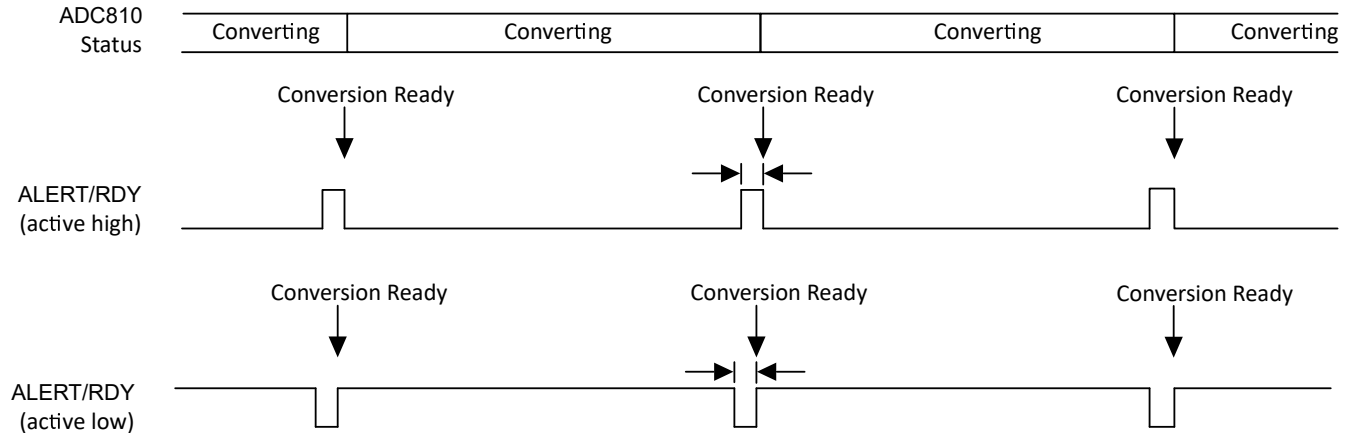


Figure 6-4. Conversion Ready Pulse in Continuous-Conversion Mode

6.3.7 Interrupt Output (INT)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. Resetting the interrupt output is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os (if they are set up as digital) after resetting is detected and is transmitted as INT. Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as a digital output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. The INT output has an open-drain structure and requires pull-up resistor to VCC, depending on the application. INT should be connected to the voltage source of the device that requires the interrupt information.

6.4 Device Functional Modes

6.4.1 Reset and Power-Up

The ADC810-Q1 resets on power-up and sets all the bits in all registers to the respective default values. The ADC810-Q1 has an internal watchdog timer that will fire if the device gets halted for more than 500ms. The watchdog reset will be reflected in the Device Status register (0xEF) and it resets the registers to the respective default values.

The ADC810-Q1 responds to the I²C general-call reset command. When the ADC810-Q1 receives a general-call reset command (06h), an internal reset is performed as if the device is powered-up.

6.4.2 Operating Modes

The ADC810-Q1 ADC operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the ADC Configuration register selects the respective operating mode.

6.4.2.1 Single-Shot Mode

When the MODE bit in the ADC Configuration register is set to 1b, the ADC810-Q1 operates in single-shot mode. The ADC810-Q1 will wait until a 1b is written to the operational status (OS) bit in the ADC Configuration register. When the OS bit is asserted, the OS bit resets to 0b, and starts a single conversion. Writing a 1b to the OS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0b to the MODE bit in the ADC Configuration register.

6.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0b), the ADC810-Q1 performs conversions continuously. When a conversion is complete, the ADC810-Q1 places the result in the [ADC Conversion register](#) and immediately begins another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configuration settings start. To switch to single-shot conversion mode, write a 1b to the MODE bit in the configuration register or reset the device.

6.5 Programming

6.5.1 I²C Interface

The ADC810-Q1 communicate through an I²C interface. I²C is a two-wire open-drain interface that supports multiple devices and controllers on a single bus. Devices on the I²C bus only drive the bus lines low by connecting them to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are always high when no device is driving them low. As a result of this configuration, two devices cannot conflict. If two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the controller and the other as the target. Both the controller and target can read and write, but the target can only do so under the direction of the controller. Some I²C devices can act as a controller or target, but the ADC810-Q1 can only act as a target device.

An I²C bus consists of two lines: SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I²C bus in groups of eight bits. To send a bit on the I²C bus, drive the SDA line to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). After the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I²C bus is held idle for more than 30ms, the bus times out.

The I²C bus is bidirectional; that is, the SDA line is used for both transmitting and receiving data. When the controller reads from a target, the target drives the data line; when the controller writes to a target, the controller drives the data line. The controller always drives the clock line. The ADC810-Q1 cannot act as a controller, and therefore can never drive SCL.

Most of the time, the bus is idle; no communication occurs, and both lines are high. When communication takes place, the bus is active. Only a controller device can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, this change is either a START condition or a STOP condition. A START condition occurs when the clock line is high, and the data line goes from high to low. A STOP condition occurs when the clock line is high, and the data line goes from low to high.

After the controller issues a START condition, the controller sends a byte that indicates with which target device to communicate. This byte is referred to as the *address byte*. Each device on an I²C bus has a unique 7-bit address that the device responds to. The controller sends an address in the address byte, together with a bit that indicates whether the controller wishes to read from or write to the target device.

Every byte (address and data) transmitted on the I²C bus is acknowledged with an *acknowledge* bit. When the controller finishes sending a byte (eight data bits) to a target, the controller stops driving SDA and waits for the target to acknowledge the byte. The target acknowledges the byte by pulling SDA low. The controller then sends a clock pulse to clock the acknowledge bit. Similarly, when the controller completes reading a byte, the controller pulls SDA low to acknowledge this completion to the target. The controller then sends a clock pulse to clock the bit. The controller always drives the clock line.

If a device is not present on the bus and the controller attempts to address the device, the controller receives a *no-acknowledge* because no device is present at that address to pull the line low. A not-acknowledge is performed by simply leaving SDA high during an acknowledge cycle.

When the controller has finished communicating with a target, the controller can issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The controller can also issue another START condition. When a START condition is issued while the bus is active, this condition is referred to as a repeated start condition.

The *Timing Requirements* section provides a timing diagram for the ADC810-Q1 I²C communication.

6.5.1.1 I²C Address Selection

The ADC810-Q1 has two address pins (ADDR0 & ADDR1) that configure the I2C address of the device. The ADDR pins can connect to GND or VDD [Table 6-1](#), which allows four different addresses to be selected with one pin.

Table 6-1. ADDR Pin Connection and Corresponding Target Address

ADDR0 PIN CONNECTION	ADDR1 PIN CONNECTION	TARGET ADDRESS
GND	GND	0b1001001 0x49
GND	VDD	0b1001011 0x4B
VDD	GND	0b1110110 0x76
VDD	VDD	0b1110111 0x77

6.5.1.2 I²C General Call

The ADC810-Q1 responds to the I2C general call address (0000000b) if the eighth bit is 0b. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110b (06h), the ADC810-Q1 resets the internal registers.

6.5.1.3 I²C Speed Modes

The I2C bus operates at one of two speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz. The ADC810-Q1 is fully compatible with both modes. No special action is required to use the ADC810-Q1 in standard or fast mode.

6.5.2 Target Mode Operations

The ADC810-Q1 acts as target receivers or target transmitters. The ADC810-Q1 cannot drive the SCL line as target devices.

6.5.2.1 Receive Mode

In target receive mode, the first byte transmitted from the controller to the target consists of the 7-bit device address followed by a low R/ $\overline{W}$ bit. The next byte transmitted by the controller is the [Address Pointer register](#). The ADC810-Q1 then acknowledges receipt of the Address Pointer register byte. The next two bytes are written to the address given by the register address pointer bits, P[1:0]. The ADC810-Q1 acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

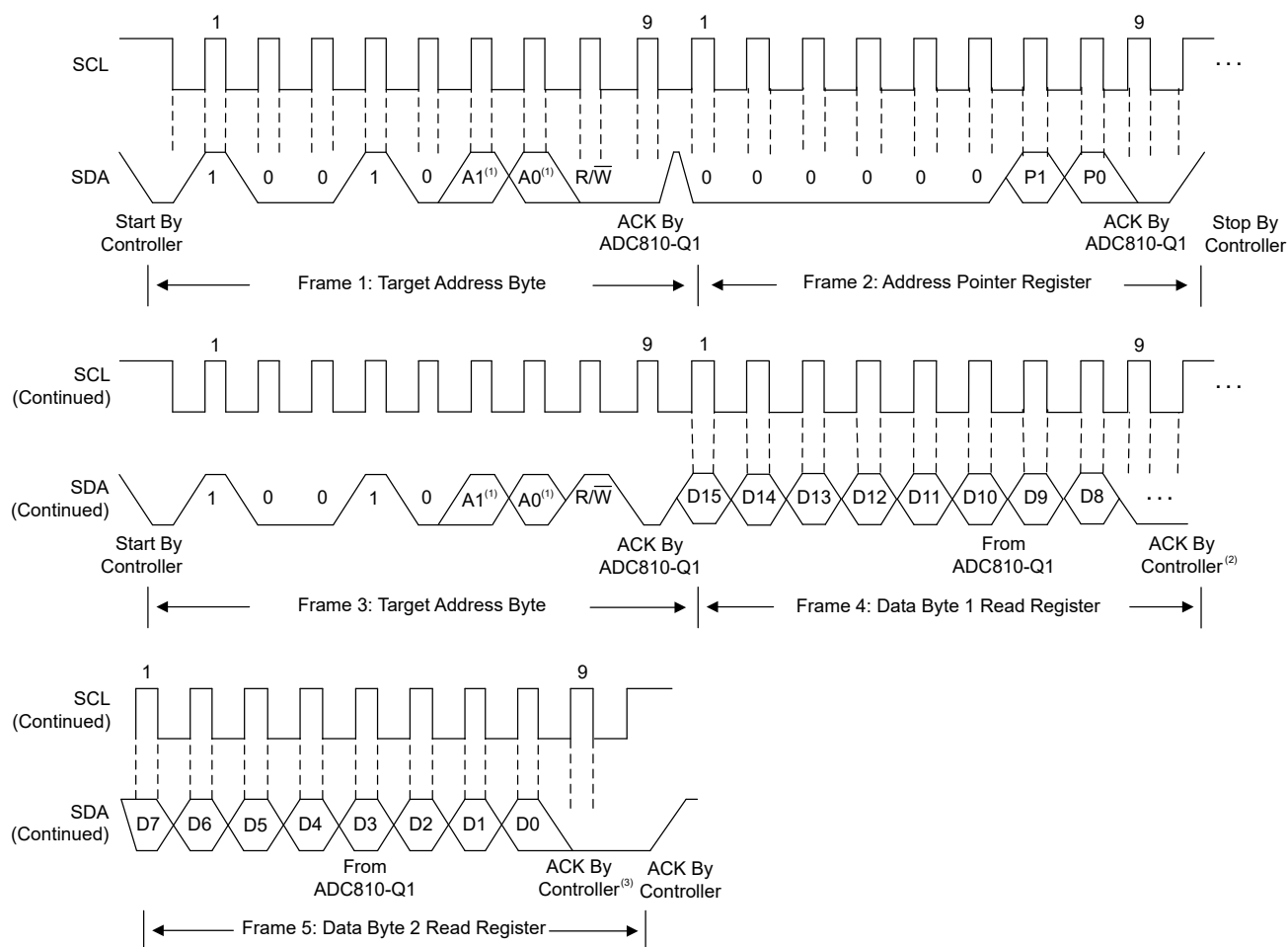
6.5.2.2 Transmit Mode

In target transmit mode, the first byte transmitted by the controller is the 7-bit target address, followed by the high R/W bit. This byte places the target into transmit mode and indicates that the ADC810-Q1 is being read from. The next byte transmitted by the target is the most significant byte of the register that is indicated by the register address pointer bits, P[1:0]. This byte is followed by an acknowledgment from the controller. The remaining least significant byte is then sent by the target and is followed by an acknowledgment from the controller. The controller can terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

6.5.3 Writing To and Reading From the Registers

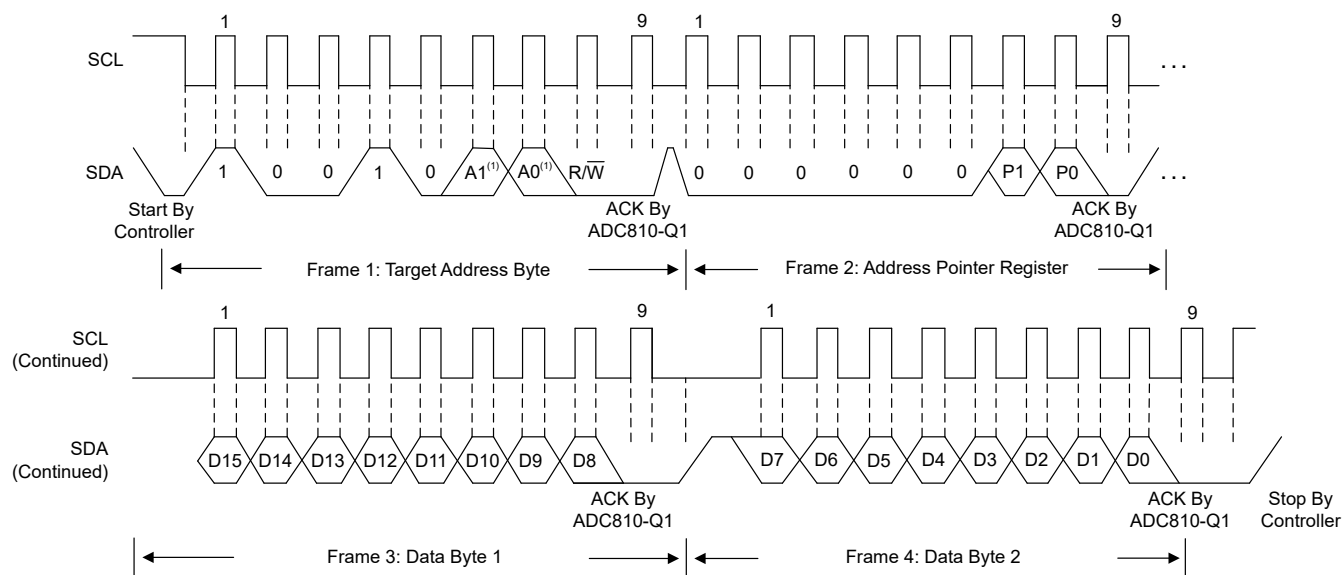
To access a specific register from the ADC810-Q1, the controller must first write an appropriate value to register address pointer bits P[1:0] in the [Address Pointer register](#). The Address Pointer register is written to directly after the target address byte, the low R/W bit, and a successful target acknowledgment. After the Address Pointer register is written, the target acknowledges, and the controller issues a STOP or a repeated START condition.

When reading from the ADC810-Q1, the previous value written to bits P[1:0] determines the register that is read. To change which register is read, a new value must be written to P[1:0]. To write a new value to P[1:0], the controller issues a target address byte with the R/W bit low, followed by the Address Pointer register byte. No additional data has to be transmitted, and the controller can issue a STOP condition. The controller can now issue a START condition and send the target address byte with the R/W bit high to begin the read. If repeated reads from the same register are desired, there is no need to continually send the Address Pointer register, because the ADC810-Q1 stores the value of P[1:0] until modified by a write operation. However, for every write operation, the Address Pointer register must be written with the appropriate values.



- A. The values of A0 and A1 are determined by the ADDR pin
- B. The controller can leave SDA high to terminate a single-byte read operation
- C. The controller can leave SDA high to terminate a two-byte read operation

Figure 6-5. Timing Diagram for Reading From ADC810-Q1



A. The values of A0 and A1 are determined by the ADDR pin

Figure 6-6. Timing Diagram for Writing to ADC810-Q1

6.5.4 Data Format

The ADC810-Q1 provides 12 bits of data in binary two's-complement and an unsigned format that is left-justified within the 16-bit [ADC Conversion register](#). The ADC810-Q1 offers a positive full-scale input that produces an output code of up to 7FFh if selected in two's complement. The output clips at these codes for signals that exceed full-scale. The Input Signal Versus Output Code tables summarize a good choice of output codes for different input signals. [Figure 6-7](#) shows each format code transitions versus input voltage.

Table 6-2. Input Signal Versus Output Code (two's-complement)

INPUT SIGNAL $V_{IN} = (V_{AINP} - V_{AINN})$	OUTPUT CODE
$\geq +FS (2^{11} - 1) / 2^{11}$	7FFh
$+FS / 2^{11}$	001h
0	000h

Table 6-3. Input Signal Versus Output Code (unsigned)

INPUT SIGNAL $V_{IN} = (V_{AINP} - V_{AINN})$	OUTPUT CODE
$\geq +FS (2^{12} - 1) / 2^{12}$	FFFFh
$+FS / 2^{12}$	0001h
0	0000h

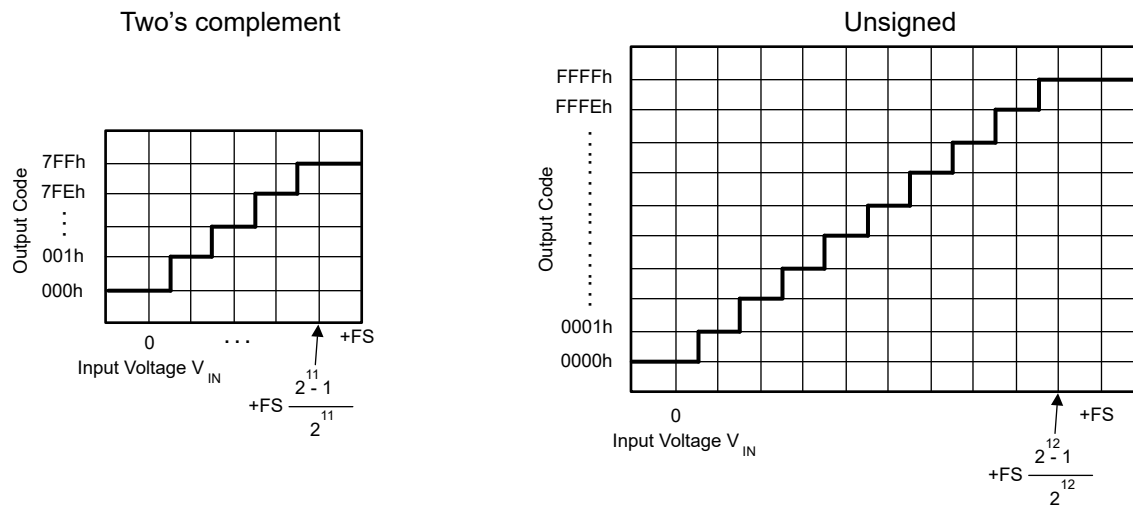


Figure 6-7. Code Transition Diagrams

7 Register Map

The ADC810-Q1 has ten registers that are accessible through the I²C interface using the [Address Pointer register](#). The [ADC Conversion register](#) contains the result of the last conversion. The [ADC Configuration register](#) is used to change the ADC810-Q1 operating modes and query the ADC status. The ADC Comp [Low_Thresh Register](#) and [High_Thresh Register](#) set the threshold values used for the comparator function. The I/O Input Port register reflects the incoming logic levels of the pins. The [I/O Output Port Register](#) displays the outgoing logic levels of the pins defined as outputs by the [I/O Direction Register](#), provided the pin has enabled digital functionality. The [I/O Polarity Inversion Register](#) enables the inversion of polarity for pins designated as digital inputs by the [I/O Direction Register](#). The I/O Direction register configures the direction of the I/O pins and determines whether a pin enables digital or analog functionality. The [Pin Function Register](#) selects the functionality of the I/Os, determining whether the pins are analog or digital, and controls the Alert pins to be either an I/O or an alert. Finally, the [Device Status Register](#) contains the state in which the device is currently operating.

[Table 7-1](#) lists the access codes for the ADC810-Q1 registers.

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read only
R/W	R/W	Read or write
W	W	Write only
Reset or Default Value		
-n		Value after reset or the default value

Address Pointer Register (address = N/A) [reset = N/A]

All nine registers are accessed by writing to the Address Pointer register.

Figure 7-1. Address Pointer Register

7	6	5	4	3	2	1	0
RESERVED				P[3:0]			
W-0h				W-0h			

Table 7-2. Address Pointer Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	W	0h	Always write 0h
3:0	P[3:0]	W	0h	Register address pointer 0000b : ADC Conversion register 0001b : ADC Configuration register 0010b : ADC Comp Low_thresh register 0011b : ADC Comp High_thresh register 0100b : I/O Input Port register 0101b : I/O Output Port register 0110b : Polarity Inversion register 0111b : I/O Direction register 1000b : Pin Function register 1001b : Device Status register

ADC Conversion Register (P[1:0] = 00b) [reset = 0000h]

The 16-bit ADC Conversion register contains the result of the last conversion in binary two's-complement format (can be changed to unsigned format through the DATA_FORMAT bit in the Pin Configuration register). Following power-up, the ADC Conversion register is cleared to 0000h and remains 0000h until the first conversion completes.

Figure 7-2. ADC Conversion Register

15	14	13	12	11	10	9	8
D[11:4]							
R-00h							
7	6	5	4	3	2	1	0
D[3:0]				RESERVED			
R-0h				R-0h			

Table 7-3. ADC Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	Reserved	R	0h	Always reads back 0h

ADC Configuration Register (P[1:0] = 01b) [reset = C183h]

The 16-bit ADC Configuration register is used to control the operating mode, channel selection, data rate, voltage reference configuration, and comparator modes. Note: Only one ADC Channel can be used at a time

Figure 7-3. ADC Configuration Register

15	14	13	12	11	10	9	8
OS	MUX[2:0]				VREF[2:0]		MODE
R/W-1b	R/W-100b				R/W-000b		R/W-1b
7	6	5	4	3	2	1	0
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUEUE[1:0]	
R/W-100b			R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Table 7-4. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OS	R/W	1b	Operational status or single-shot conversion start This bit determines the operational status of the device. OS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0b : No effect 1b : Start a single conversion (when in power-down state) When reading: 0b : Device is currently performing a conversion 1b : Device is not currently performing a conversion
14:12	MUX[2:0]	R/W	100b	Input multiplexer configuration These bits configure the ADC channel to use to capture data. 000b : A4 001b : A5 010b : A6 011b : A7 100b : A0 (default) 101b : A1 110b : A2 111b : A3
11:9	VREF[2:0]	R/W	000b	Programmable VREF configuration These bits set the ADC Vref Voltage. 000b : VDD (default) 001b : VDD 010b : 2.5V 011b : 2.5V 100b : 1.4V 101b : 1.4V 110b : 1.4V 111b : 1.4V

Table 7-4. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MODE	R/W	1b	Device operating mode This bit controls the operating mode. 0b : Continuous-conversion mode 1b : Single-shot mode or power-down state (default)
7:5	DR[2:0]	R/W	100b	Data rate These bits control the data rate setting. 000b : 128SPS 001b : 250SPS 010b : 490SPS 011b : 920SPS 100b : 1600SPS (default) 101b : 2400SPS 110b : 3300SPS 111b : 3300SPS
4	COMP_MODE	R/W	0b	Comparator mode This bit configures the comparator operating mode. 0b : Traditional comparator (default) 1b : Window comparator
3	COMP_POL	R/W	0b	Comparator polarity This bit controls the polarity of the ALERT/RDY pin. 0b : Active low (default) 1b : Active high
2	COMP_LAT	R/W	0b	Latching comparator This bit controls whether the ALERT/RDY pin latches after being asserted or clears after conversions are within the margin of the upper and lower threshold values. 0b : Nonlatching comparator . The ALERT/RDY pin does not latch when asserted (default) 1b : Latching comparator. The asserted ALERT/RDY pin remains latched until conversion data are read by the controller. The device responds with an address, and is the lowest address currently asserting the ALERT/RDY bus line.
1:0	COMP_QUE[1:0]	R/W	11b	Comparator queue and disable These bits perform two functions. When set to 11, the comparator is disabled and the ALERT/RDY pin is set to a high-impedance state. When set to any other value, the ALERT/RDY pin and the comparator function are enabled, and the set value determines the number of successive conversions exceeding the upper or lower threshold required before asserting the ALERT/RDY pin. 00b : Assert after one conversion 01b : Assert after two conversions 10b : Assert after four conversions 11b : Disable comparator and set ALERT/RDY pin to high-impedance (default)

ADC Low_thresh (P[1:0] = 10b) [reset = 8000h] and ADC High_thresh (P[1:0] = 11b) [reset = 7FFFh] Registers

The ADC Comparator high and low threshold values used by the comparator are stored in two 16-bit registers in two's-complement format(can be changed in the Pin Configuration register. The user must write the right values depending on the format the ADC results are currently in.) The comparator is implemented as a digital comparator.

The conversion-ready function of the ALERT/RDY pin is enabled by setting the High_thresh register MSB to 1b and the Low_thresh register MSB to 0b. To use the comparator function of the ALERT/RDY pin, the High_thresh register value must always be greater than the Low_thresh register value. The threshold register formats are shown in [ADC Low_thresh register](#). When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode, and provides a continuous-conversion ready pulse when in continuous-conversion mode.

Figure 7-4. Low_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh[11:4]							
R/W-80h							
7	6	5	4	3	2	1	0
Lo_thresh[3:0]				RESERVED			
R/W-0h				R-0h			

Figure 7-5. High_thresh Register

15	14	13	12	11	10	9	8
Hi_thresh[11:4]							
R/W-7Fh							
7	6	5	4	3	2	1	0
Hi_thresh[3:0]				RESERVED			
R/W-Fh				R-Fh			

Table 7-5. Low_thresh and High_thresh Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	Lo_thresh[11:0]	R/W	800h	Low threshold value
15:4	Hi_thresh[11:0]	R/W	7FFh	High threshold value

I/O Input Port (P[3:0] = 0100b) [reset = 0000h] Register

The I/O Input Port Register reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an analog or digital pin by the Pin Function Register, or as a digital input or a digital output by the I/O Direction Register. They act only on read operation. Writes to this register have no effect. The default value is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I2C device that the Input Port Register will be accessed next. The MSB bit from IN_READ controls I/O_9, and then it goes below until the LSB bit, which control I/O_0.

Figure 7-6. I/O Input Port Register

15	14	13	12	11	10	9	8
RESERVED						IN_READ[9:8]	
R-000000b						R-00b	
7	6	5	4	3	2	1	0
IN_READ[7:0]							
R-00h							

Table 7-6. I/O Input Port Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R	000000b	Always 000000b
9:0	IN_READ[9:0]	R	0000000000b	10-bit I/O input results. Reads all I/O input values regardless of functionality.

I/O Output Port (P[3:0] = 0101b) [reset = 03FFh] Register

The I/O Output Setting Register shows the outgoing logic levels of the pins defined as outputs by the I/O Direction Register. If a bit is set (1) in any of the OUT_LEVEL bits, the output value for that I/O assigned to the bit will be high; if a bit is clear (0), the output value will be low. Bit values in this register have no effect on pins

defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. If the I/O is not enabled as a digital input, the placeholder value for that I/O that is currently not a digital IO input will be the previous IO value it registered before the direction change from input to output, and the IO value will not be affected by this register.

Figure 7-7. I/O Output Port Register

15	14	13	12	11	10	9	8
RESERVED						IN_READ[9:8]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
OUT_LEVEL[7:0]							
R/W-00h							

Table 7-7. I/O Output Port Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000b	Always 000000b
9:0	OUT_LEVEL[9:0]	R/W	111111111b	10-bit I/O output level control 0 : IO output of the designated I/O will be low. 1 : IO output of the designated I/O will be high. (default)

I/O Polarity Inversion (P[3:0] = 0110b) [reset = 0000h] Register

The Polarity Inversion Register allows polarity inversion of pins defined as inputs by the I/O Direction Register. If the I/O bit in the register is not set to be an input, this register won't affect that I/O bit. If a bit in this register is set (written with 1), the polarity of the corresponding port pin is inverted. If a bit in this register is cleared (written with a 0), the original polarity of the corresponding port pin is retained.

Figure 7-8. I/O Polarity Inversion Register

15	14	13	12	11	10	9	8
RESERVED						POL_SEL[9:8]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
POL_SEL[7:0]							
R/W-00h							

Table 7-8. I/O Polarity Inversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000b	Always 000000b
9:0	POL_SEL[9:0]	R/W	000000000b	10-bit I/O polarity control 0 : IO input pin is not inverted. (default) 1 : IO input pin is inverted. Note: Only works if the pin is set as a digital input.

I/O Direction (P[3:0] = 0111b) [reset = 00FFh] Register

The I/O Direction Register configures the direction of the I/O pins. If any CONFIG_IO bits in this register are set to 1, the corresponding port pin is enabled as an input I/O. If any CONFIG_IO bits in this register are cleared to 0, the corresponding port pin is enabled as a output I/O. If the Alert pins are not set to I/O_8 and I/O_9 i.e., the Alert pins are not configured as digital I/Os, then this register doesn't affect these pins.

Figure 7-9. I/O Direction Register

15	14	13	12	11	10	9	8
RESERVED						CONFIG_IO[9:8]	
R/W-000000b						R/W-00b	
7	6	5	4	3	2	1	0
CONFIG_IO[7:0]							
R/W-FFh							

Table 7-9. I/O Direction Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000b	Always 000000b
9:0	IN_READ[9:0]	R/W	0011111111b	10-bit I/O Direction Select 0 : IO pin is set to output. (default for IO8 and IO9) 1 : IO pin is set to input. (default except IO8 and IO9)

Pin Function(P[3:0] = 1000b) [reset = 07FFh] Register

The Pin Function register selects the functionality of the I/Os in the device from I/O_0 to I/O_9. The lower byte controls whether any of the pins in I/O_7 to I/O_0 are selected as digital or analog pins. If a bit in the lower byte is set to 1, the pin will be an Analog pin; if it is set to 0, then the pin will be a Digital pin. Additionally, if any of the AL_CONFIG pins are set to 0, then the pin is configured as a digital input; otherwise, it is set to its respective Alert pin. If a pin is configured as an Analog pin, the INT Alert pin won't recognize any "change" in the input going to that pin. Finally, the Data_Format bit decides whether the data collected from the ADC is set to be two's complement (if the bit is set to 1) or unsigned (if the bit is set to 0)

Figure 7-10. Pin Function Register

15	14	13	12	11	10	9	8
RESERVED						DATA_FORMAT	ADC_AL_CON F
R-00000b						R/W-1b	R/W-1b
7	6	5	4	3	2	1	0
CONFIG_AD_PIN[7:0]							
R/W-FFh							

Table 7-10. Pin Function Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	Reserved	R/W	00000b	Always 00000b
10	DATA_FORMAT	R/W	1b	ADC Conversion Data Format 0 : Unsigned data format. 1 : 2's Complement data format. (default)
9	ADC_AL_CONF	R/W	1b	ADC Alert Configuration 0 : ADC ALERT/RDY pin is set to IO8, i.e., configured as a digital pin. 1 : ADC ALERT/RDY pin set to ALERT/RDY functionality, i.e., logic. (default)
8	INT_AL_CONF	R/W	1b	INT Alert Configuration 0 : INT pin is set to IO9, i.e., configured as a digital pin. 1 : INT pin set to INT functionality, i.e., logic. (default)
7:0	CONFIG_AD_PIN[7:0]	R/W	FFh	I/O Analog or Digital Configuration bytes 0 : Designated pin is set as a digital pin, i.e., IOX. 1 : Designated pin is set as an analog pin, i.e., AX. (default)

Device Status (P[3:0] = 1001b) [reset = 0011h] Register

The 16-bit Device Status register contains the most recent status of the device at the time of reading. The status register is cleared to its default value once the user reads from it.

Figure 7-11. Device Status Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RESERVED				D_STATUS[3:0]			
R-0h				R-0h			

Table 7-11. Device Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R	000h	Always 000h
3:0	D_STATUS[3:0]	R	0h	Device Status 11h : Device working as normal. (default) EFh : A watchdog reset occurred. 77h : ADC Capture encountered an error. 88h : Register Update error detected. 99h : Register Read error detected. AAh : I2C error detected. BBh : ADC Conversion error detected. CCh : ADC Continuous Mode error detected. DDh : Internal clock error detected. EEh : I2C Timeout error detected. 66h : Unknown error detected.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application

8.1.1 Schematic

TI recommends connecting a combination of a 10 μ F and a 0.1 μ F low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used, but they can affect the supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins (within a few millimeters).

Pull-up resistors are required on both the SDA and SCL lines because I2C bus drivers are open-drain. Additionally, pull-up resistors are required on both INT and ALERT/RDY pins because both pins are open-drain.

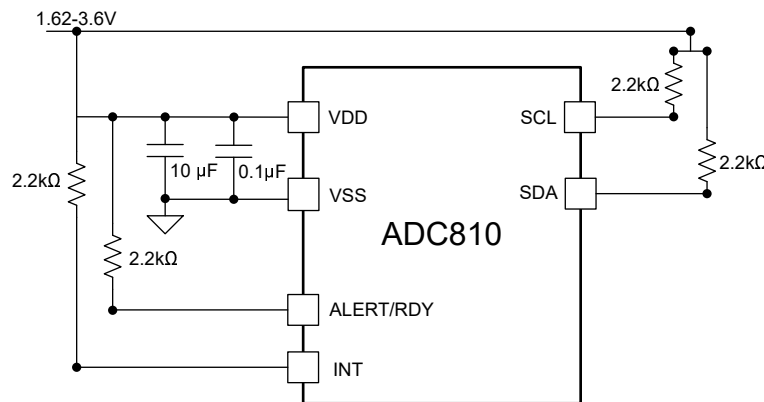


Figure 8-1. Typical Application Schematic

8.1.2 ADC Configuration Examples

The ADC810 can be configured to behave as an ADC in the different modes that are mentioned inside the ADC registers.

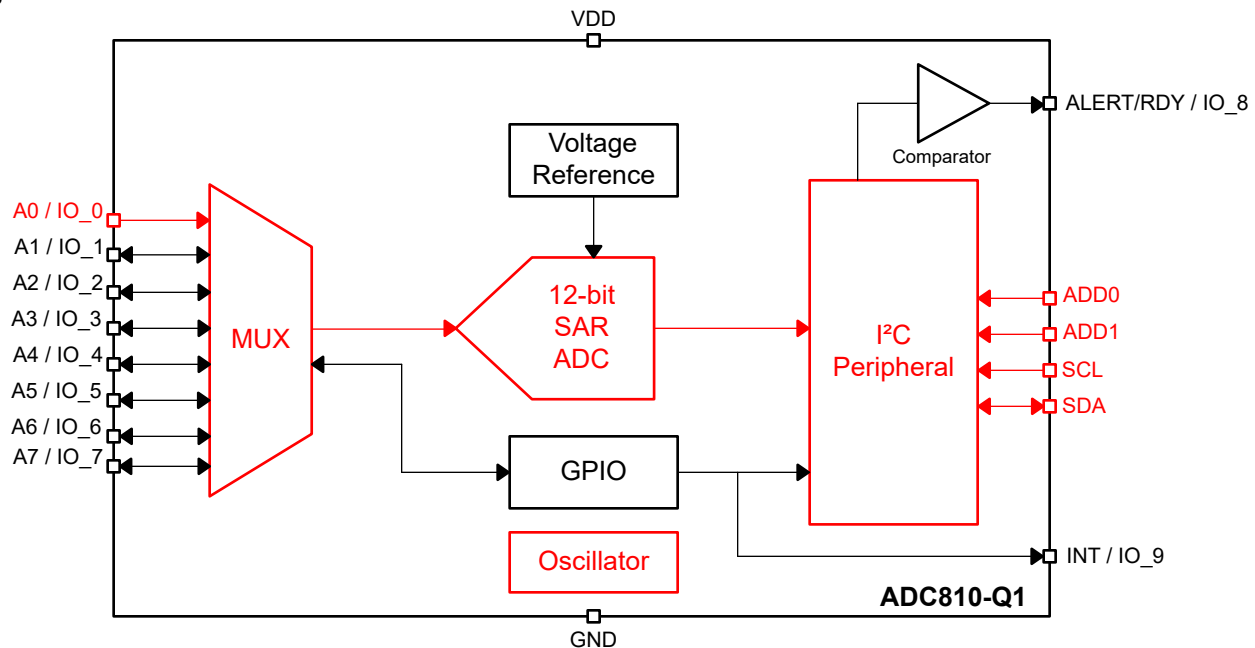


Figure 8-2. ADC Single Capture & Continuous Configuration Highlight

ADC Single Shot Mode

The device is configured to start a single conversion, set the input channel to A0, set VREF to VDD, set the ADC to Single-shot mode, set the SPS to 128, and disable the comparator.

The I2C controller sends a write to the ADC Configuration register targeting the right I2C Address of the ADC810. The following messages can be sent:

1. I2C Controller Message = {0x01, 0xC1, 0x83}

The Conversion Ready Pin functionality can be set up along with the single-shot mode with the following configuration:

1. I2C Controller Data Message #1 = {0x02, 0x00, 0x00}
2. I2C Controller Data Message #2 = {0x03, 0x80, 0x00}
3. I2C Controller Data Message #3 = {0x01, 0xC1, 0x83}

The previous configuration sets the ADC threshold register to its corresponding values, enabling the ADC Alert RDY functionality (Refer to the Conversion Ready Pin section). The ADC configuration remains the same as before.

ADC Continuous Mode

The device is configured so the ADC starts a single conversion, sets the input channel as A0, sets VREF to VDD, sets the ADC to Continuous mode, sets the SPS to 1600, and disables the comparator.

The I2C controller sends a write to the ADC Configuration register targeting the right I2C Address of the ADC810. The following messages can be sent:

1. I2C Controller Message = {0x01, 0xC0, 0x83}

The Conversion Ready Pin functionality can be set up along the continuous mode with the following configuration:

1. I2C Controller Data Message #1 = {0x02,0x00, 0x00}
2. I2C Controller Data Message #2 = {0x03,0x80, 0x00}
3. I2C Controller Data Message #3 = {0x01,0xC0, 0x83}

The previous configuration sets the ADC threshold register to its corresponding values, enabling the ADC Alert RDY functionality (Refer to the Conversion Ready Pin section). The ADC configuration remains the same as before.

ADC Continuous Comparator Mode

The device is configured so the ADC starts a single conversion; sets the input channel as A0; sets VREF to VDD; sets the ADC to Continuous mode; sets the SPS to 1600; sets the comparator to traditional mode; sets the ALERT/RDY pin polarity to active low; disables latching on the ALERT/RDY pin; and makes the ALERT/RDY pin assert after one conversion. Before we set the ADC configuration, we need to set the Low and High Threshold registers to the desired values. In this case, we'll set the low threshold to 900 (0x384) and the high threshold to 1800 (0x3E8).

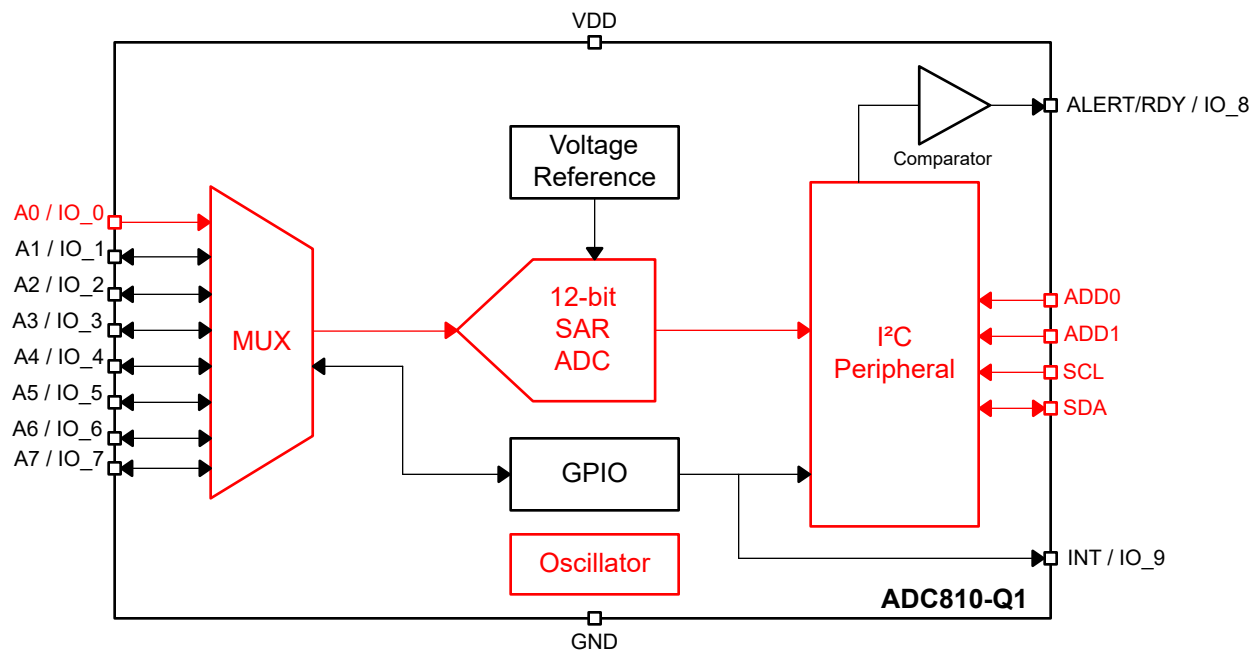


Figure 8-3. ADC Comparator Configuration Highlight

The I2C controller sends a write to the ADC Configuration register targeting the right I2C Address of the ADC810. The following messages can be sent:

1. I2C Controller Data Message #1 = {0x02,0x38,0x40}
2. I2C Controller Data Message #2 = {0x03,0x3E,0x80}
3. I2C Controller Data Message #3 = {0x01,0xC1, 0x80}

The comparator mode can also be set to Window comparator mode. To do so, the following configuration must be written to the ADC Configuration register:

1. I2C Controller Data Message #3 = {0x01,0xC1, 0xE0}

Furthermore, if the user needs the ALERT/RDY pin to latch, the following configuration can be used:

1. I2C Controller Data Message #3 = {0x01,0xC1, 0xE4}

8.1.3 GPIO Configuration Example

The ADC810 can be configured to behave as an IO Expander in the different modes specified in the IO registers.

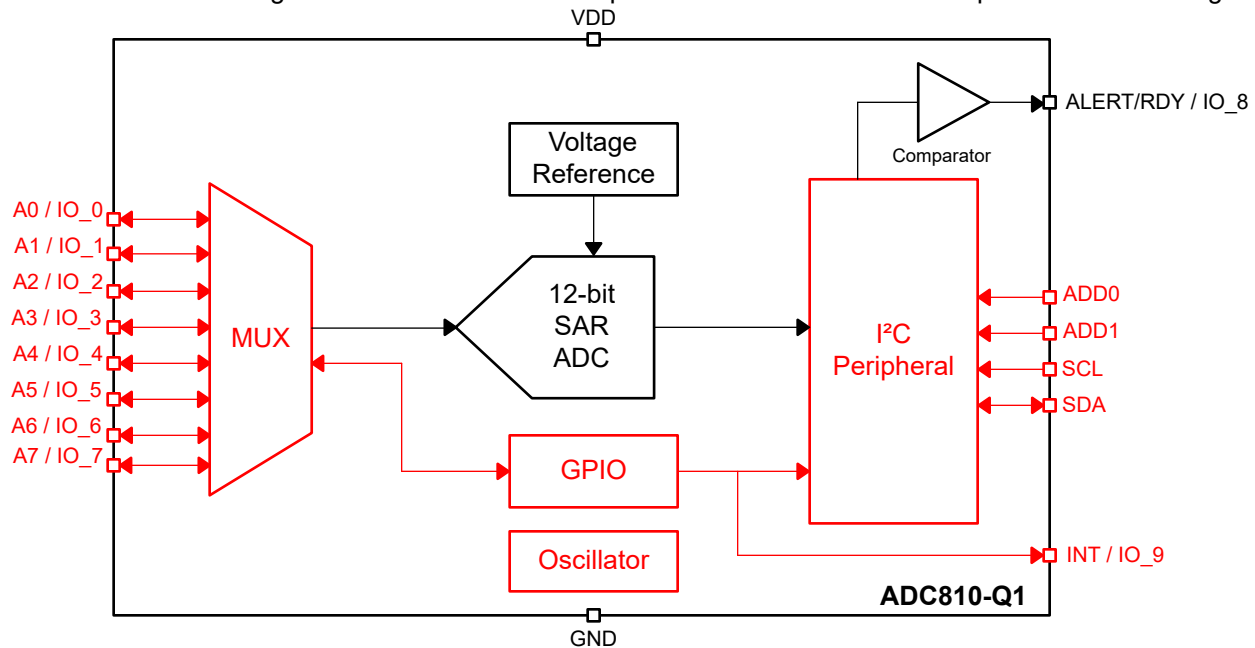


Figure 8-4. GPIO Input and Output Configuration Highlight

GPIO All Pins (except INT pin) Configured to Inputs

The device is configured so that all pins except the INT pin are inputs.

To do so, we'll write to the Pin Function register to set the pins to GPIO functionality, then write to the I/O Direction register to set the pins to inputs:

1. I2C Controller Data Message #1 = {0x08,0x05,0x00}
2. I2C Controller Data Message #2 = {0x07,0x02,0xFF}

When a GPIO changes from its original state to a new reading, the INT pin will indicate a change. To reset/update the IO input states (reset the INT pin), the user needs to read from the Input register.

If the user wants to change the input polarity of the input pins, the additional message can be written into the I/O Polarity Inversion register:

1. I2C Controller Data Message #3 = {0x06,0x02,0xFF}

GPIO All Pins Configured to Outputs

The device is configured so that all pins are outputting a high signal.

To do so, we'll write to the Pin Function register to set the pins to GPIO mode, then write to the I/O Direction register to set the pins to output mode. Finally, we'll set the I/O Output Port register to a desired value, which in this case will be high:

1. I2C Controller Data Message #1 = {0x08,0x04,0x00}
2. I2C Controller Data Message #2 = {0x07,0x00,0x00}
3. I2C Controller Data Message #2 = {0x05,0x03,0xFF}

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all ADC810 devices and support tools. Each ADC810 commercial family member has one prefix: ADC. The prefix represent a fully qualified production device (ADC).

ADC – Fully qualified production device

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the number of ADC channels and the number of I/Os the ADC device has. [Table 9-1](#) provides a legend for reading the complete device name.

Figure 9-1. Device Nomenclature

Table 9-1. Device Nomenclature

Device Family	ADC = Analog to Digital Converter + I/O Expander
Number of ADC Channels	8 = ADC Channels
Number of I/O available	10 = I/Os
Temperature Range	
Package Type	See www.ti.com/packaging
Distribution Format	R = Large reel

For orderable part numbers in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

9.2 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

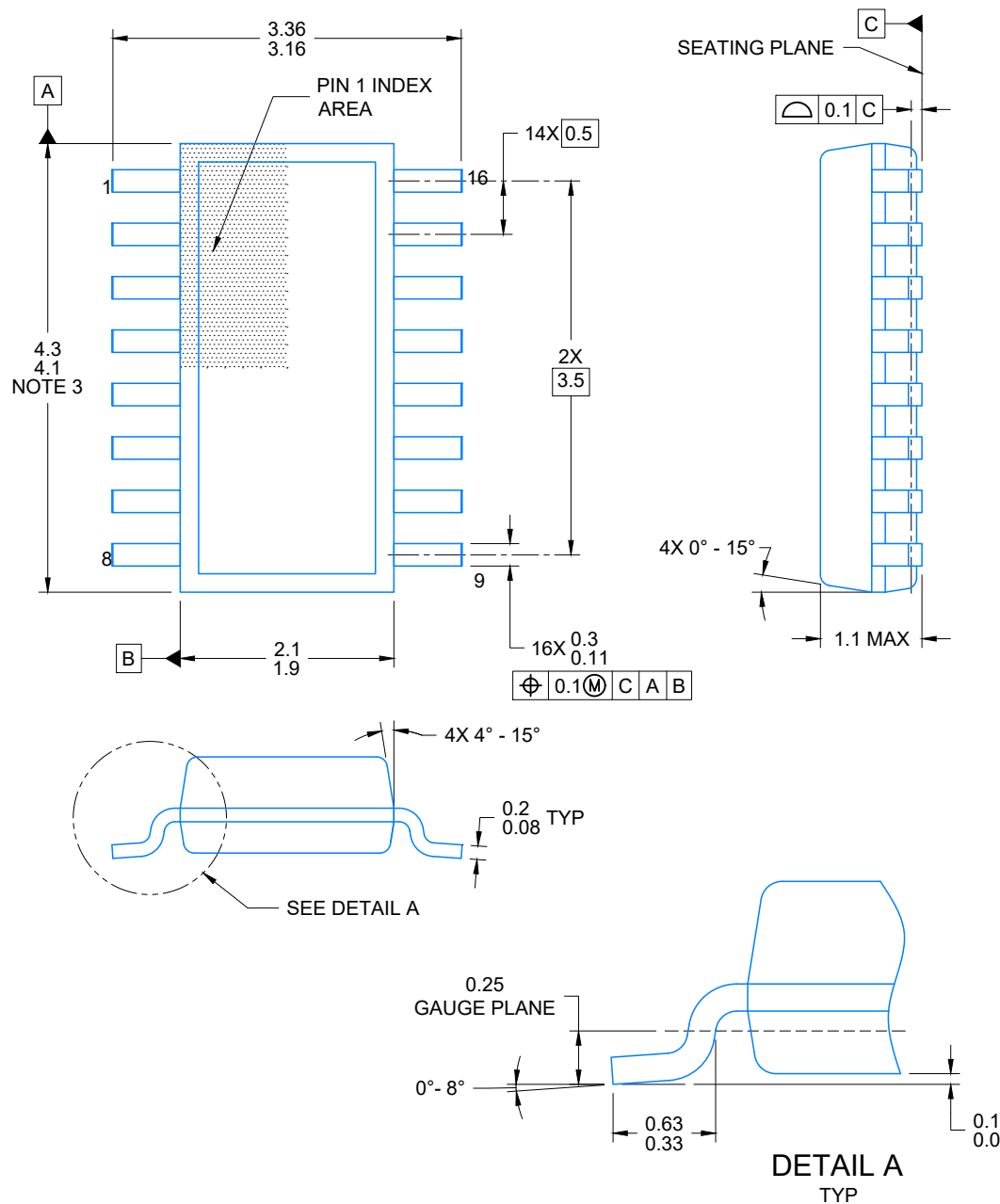
Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC810QDYRQ1	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ADC810Q

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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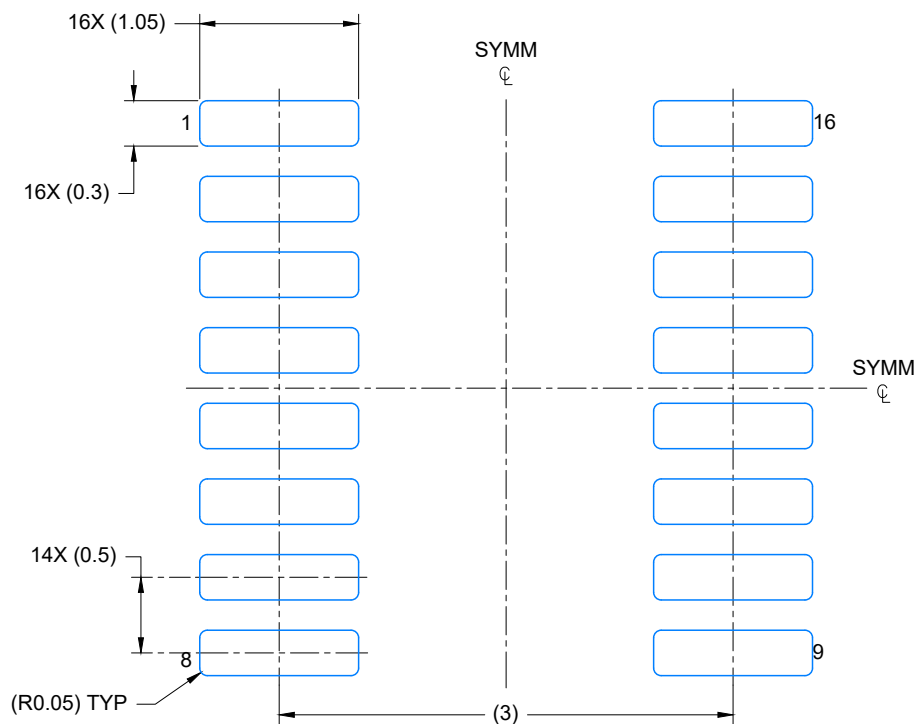
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



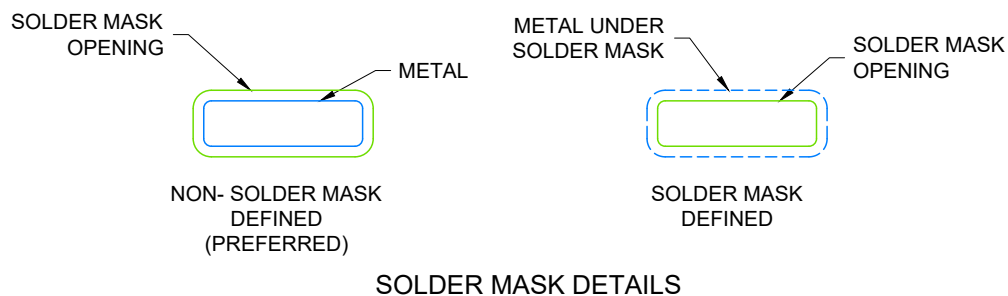
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



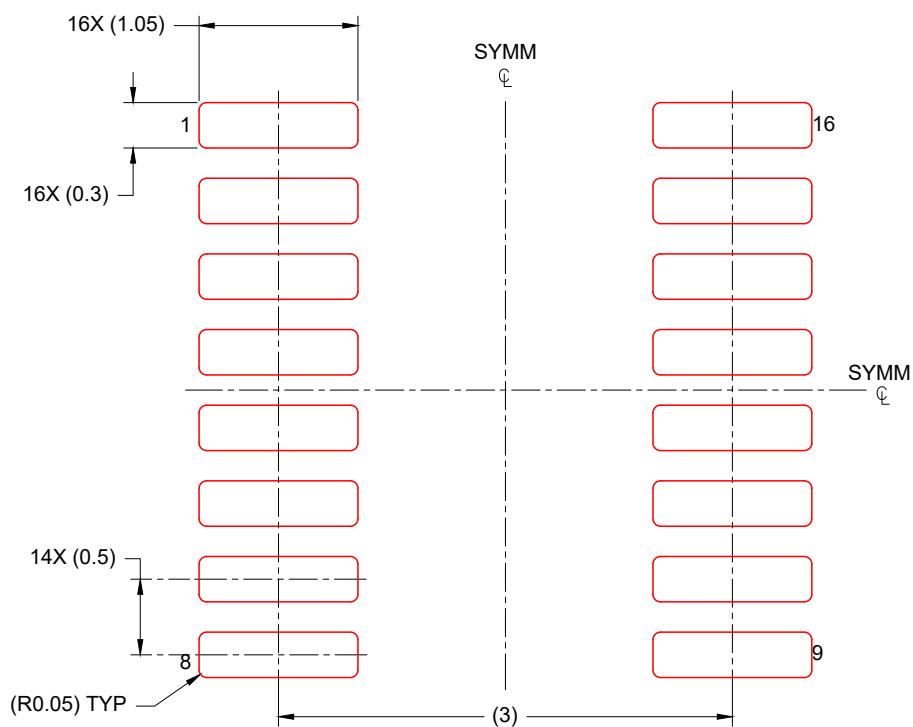
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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