ADCV08832

ADCV08832 Low Voltage, 8-Bit Serial I/O CMOS A/D Converter with Sample/Hold Function

Literature Number: SNAS124A

May 2001

National Semiconductor

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Low Voltage, 8-Bit Serial I/O CMOS A/D Converter with Sample/Hold Function

General Description

The ADCV08832 is a low voltage, 8-Bit successive approximation analog-to-digital converter with a 3-wire serial interface. The serial I/O will interface to microcontrollers, PLD's, microprocessors, DSPs or shift registers. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard.

To minimize total power consumption, the ADCV08832 can be set to go into low power mode whenever it is not performing conversions.

A sample/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion. The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes.

Features

- 3-wire serial digital data link requires few I/O pins
- Single supply 2.7V to 5V
- Analog input track/hold function
- Analog input voltage range from GND to V_{CC}
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- Superior pin compatible replacement for TLV0832 and ADC0832

Applications

- Digitizing sensors and waveforms
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Embedded systems
- Low power circuits

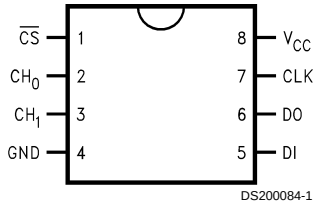
Key Specifications

(For 3.3V supply, typical, unless otherwise noted)

- Resolution 8 bits
- Conversion time (f_{CLK} = 500 kHz) 16 µs (max)
- Power dissipation 1.7 mW
- Power down mode <0.1 µW
- Total Unadjusted Error ±0.8 LSB
- No missing codes over temperature (−40˚C to +125˚C)

Connection Diagram

ADCV08832
SOIC-8 Package



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Ordering Information

Temperature Range Industrial (−40˚C ≤ T_J ≤ +125˚C)	Package	Package Marking	Transport Media
ADCV08832CIM	M08A	ADC08832I	95 Units in Rail
ADCV08832CIMX	M08A	ADC08832I	2500 Units in Tape and Reel

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
ESD Susceptibility (Note 6)	
Human Body Model	2500V
Machine Model	250V
Junction Temperature (Note 5)	150˚C
Storage Temperature Range	−65˚C to +150˚C
Mounting Temperature Infrared	235˚C

Operating Ratings (Notes 2, 3)

Temperature Range	$-40^{\circ}C < T_J < +125^{\circ}C$
Supply Voltage	2.7V to 5.5V
Thermal Resistance (θ_{jA})	
SO Package,	
8-pin Surface Mount	190˚C/W
Clock Frequency	10 kHz ≤ f_{CLK} ≤ 1000 kHz

Electrical Characteristics

The following specifications apply for V_{CC} = 3.3V_{DC} and f_{CLK} = 500 kHz, 50% Duty Cycle, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units
CONVERTER AND MULTIPLEXED CHARACTERISTICS					
TUE	Total Unadjusted Error	(Note 9)	±0.1	**±0.8**	LSB (max)
V_{OFF}	Offset Error		0.03	**±0.5**	LSB
DNL	Differential Nonlinearity		0.1	**±0.5**	LSB
INL	Integral Nonlinearity		0.1	**±0.5**	LSB
FS	Full Scale Error		0.06	**±0.8**	LSB
V_{IN}	Analog Input Voltage	(Note 10)		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	DC Common Mode Error		±0.02		LSB (max)
	Analog Input Leakage Current (Note 11)	On Channel	±11.0		nA
		Off Channel	±3.0		nA
DC CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage		1.0	**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage		1.1	**0.8**	V (max)
I_{IN}	Digital Input Current		±2		µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	V_{CC} = 2.7V I_{OUT} = −360 µA	3.3	**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_{CC} = 2.7V I_{OUT} = 1.6 mA	0.2	**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V V_{OUT} = 3.3V	−2.0 2.0		µA µA
I_{SOURCE}	Digital Output Short Circuit Current	V_{OUT} = 0V	−13		mA
I_{SINK}	Digital Output Sink Circuit	V_{OUT} = V_{CC}	9.6		mA
I_{CC}	Supply Current (Note 15)	$\overline{CS}$ = V_{CC}	0.1		nA
		$\overline{CS}$ = Low, CLK = V_{CC}	330	**500**	µA (max)

Electrical Characteristics

The following specifications apply for V_{CC} = 3.3V, 50% Duty Cycle, and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter	Conditions	Typical	Limits	Units
f_{CLK}	Max Clock Frequency	V_{CC} = 5	1000		kHz
		V_{CC} = 3.3	700	**500**	kHz
		V_{CC} = 2.7	400		kHz

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 3.3V, 50% Duty Cycle, and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter	Conditions	Typical	Limits	Units
	Clock Duty Cycle (Note 12)			**40** **60**	% (min) % (max)
t_{CONV}	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 500 kHz		**8** **16**	$1/f_{CLK}$ µs
t_{ca}	Acquisition Time			**½**	$1/f_{CLK}$ (max)
t_{SET-UP}	Set Up Time Required from Falling $\overline{CS}$ to Rising Clock Edge			**15**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 13)	C_L = 100 pF: Data MSB First Data LSB First		 **150** **100**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of CS to Data Output and SARS Hi-Z	C_L = 100 pF, R_L = 10 kΩ (see TRI-STATE Test Circuit)	35		ns
C_{IN}	Input Capacitance of CH_0, CH_1 (Note 14)		13		pF
C_{IN}	Input Capacitance of CLK, D1		5		pF
C_{OUT}	Output Capacitance of Logic Outputs D0 (in TRI-STATE)		5		pF

Dynamic Characteristics

The following specifications apply for V_{CC} = 3.3V, f_{CLK} = 500 kHz, T_A= 25˚C, R_{SOURCE} = 25Ω, f_{IN} = 9.6 kHz, V_{IN} = $3.3V_{P-P}$, non-coherent 2048 samples.

Symbol	Parameter	Conditions	Typical	Limits	Units
f_S	Sampling Rate		f_{CLK}/13		ksps
SNR	Signal-to-Noise Ratio (Note 16)		49.5		dB
THD	Total Harmonic Distortion (Note 17)		−66		dB
SINAD	Signal-to-Noise and Distortion		49.4		dB
ENOB	Effective Number Of Bits (Note 15)		7.9		Bits
SFDR	Spurious Free Dynamic Range		−67.6		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND = 0 V_{DC}, unless otherwise specified.

Note 4: When the input voltage V_{IN} at any pin exceeds the power supplies (V_{IN} < (GND) or V_{IN} > V_{CC},) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed V_{CC} with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor. The machine mode is a 200 pF capacitor discharged directly into each pin.

Note 7: Typical are at T_J = 25˚C and represent the most likely parametric norm.

Note 8: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 10: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output will be 0000 0000. Two on-chip diodes are tied to each analog input (see Functional Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC}. During testing at low V_{CC} levels (e.g., 2.7V), high level analog inputs (e.g., 3.3V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding the range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 3.30 V_{DC} input voltage range will therefore require a minimum supply voltage of 3.25 V_{DC} over temperature variations, initial tolerance and loading.

Note 11: Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high ($3.3V_{DC}$) and the remaining off channel tied low (0 V_{DC}), total current flow through the off channel is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channel is again measured. The two cases considered for determining the on channel leakage current are the same except total current flow through the selected channel is measured.

Note 12: A 40% to 60% duty cycle range insures proper operation at all clock frequencies.

Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in to allow for comparator response time.

Dynamic Characteristics (Continued)

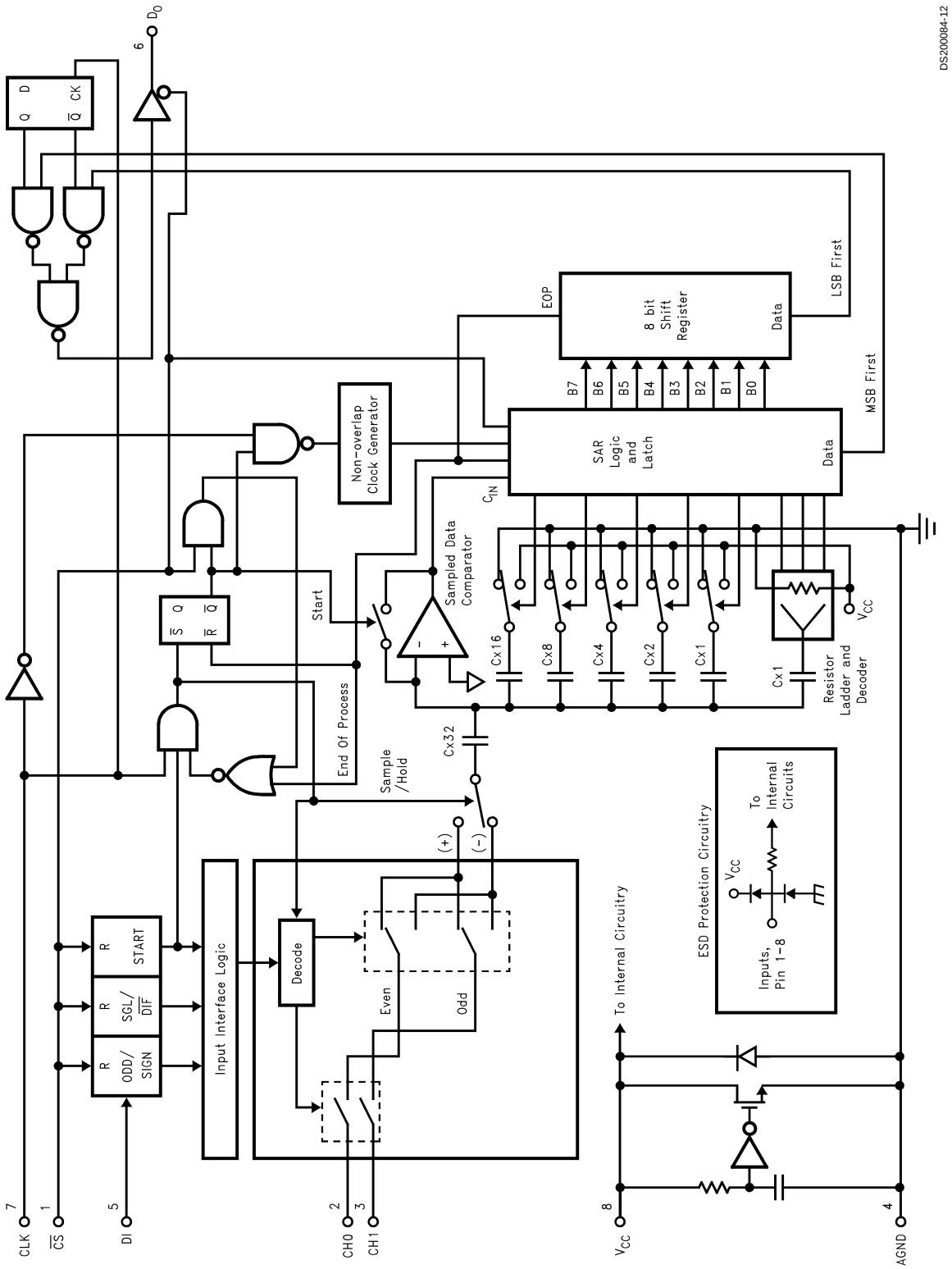
Note 14: Analog inputs are typically 300Ω input resistance in series with a 13 pF sample and hold.

Note 15: Effective Number Of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation ENOB = (SINAD −1.76)/6.02.

Note 16: The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

Note 17: The contributions of the first 6 harmonics are to calculate THD.

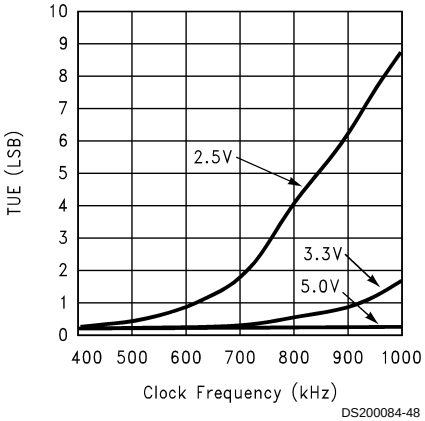
ADCV08832 Functional Block Diagram



Typical Performance Characteristics

The following specifications apply for T_A = 25˚C, V_{CC} = 3.3V, unless otherwise specified.

TUE vs Clock Frequency



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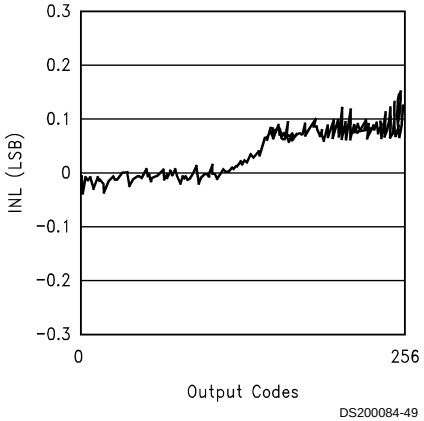
INL vs Output Codes



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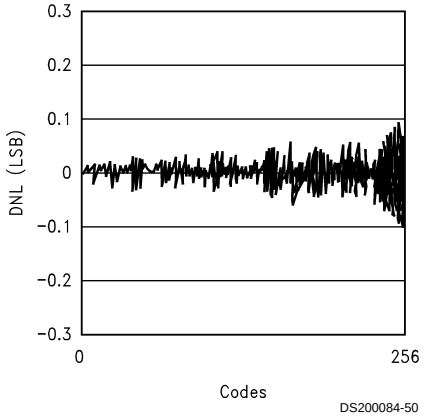
DNL vs Output Codes



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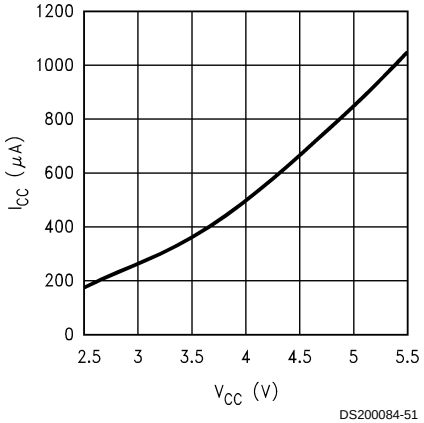
I_{CC} (operating) vs V_{CC}



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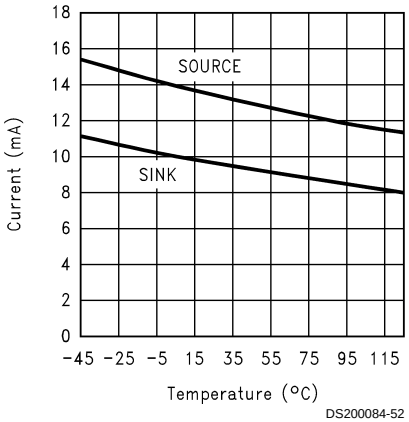
Typical Digital Output Current vs Temperature



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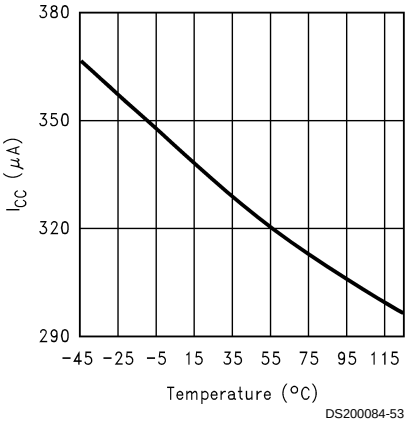
I_{CC} (operating) vs Temperature



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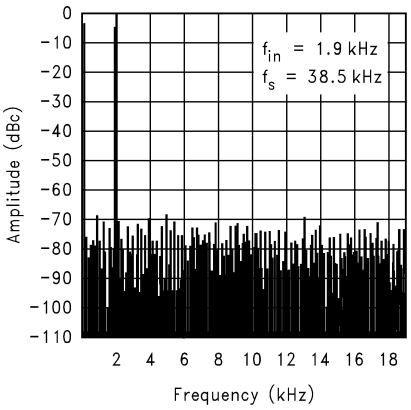
Typical Performance Characteristics

The following specifications apply for T_A = 25˚C, V_{CC} = 3.3V, unless otherwise specified. (Continued)

Spectral Response with 1.9 kHz Sine Wave Input, f_{CLK} = 500 kHz



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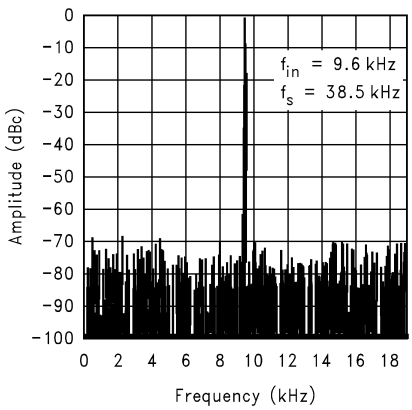
Spectral Response with 9.6 kHz Sine Wave Input, f_{CLK} = 500 kHz



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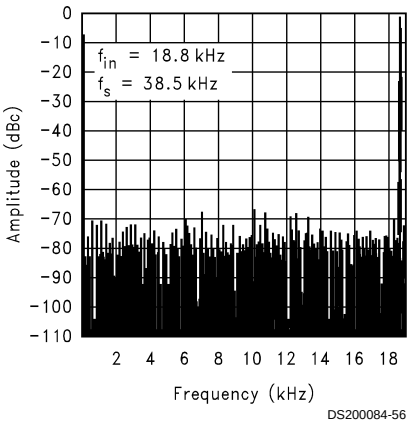
Spectral Response with 18.8 kHz Sine Wave Input, f_{CLK} = 500 kHz



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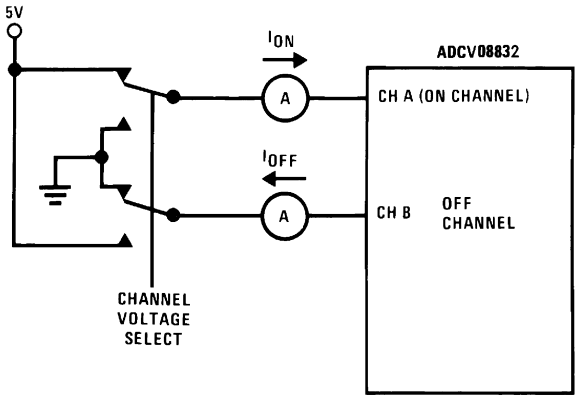
Leakage Current Test Circuit



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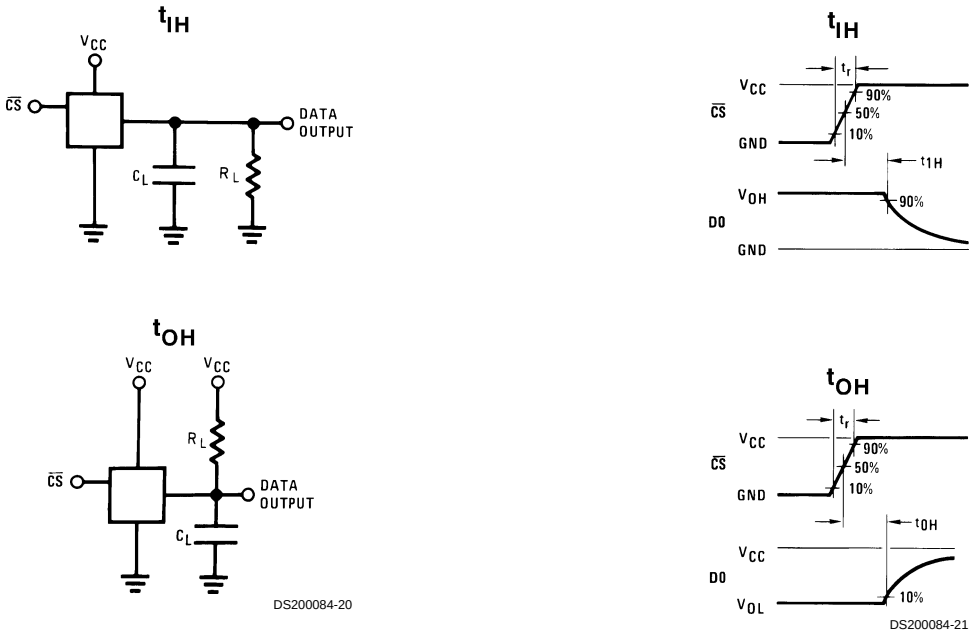
TRI-STATE Test Circuits and Waveforms



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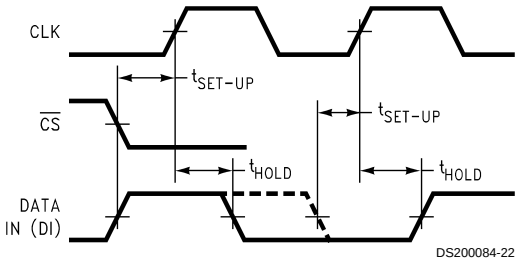
Timing Diagrams

Data Input Timing



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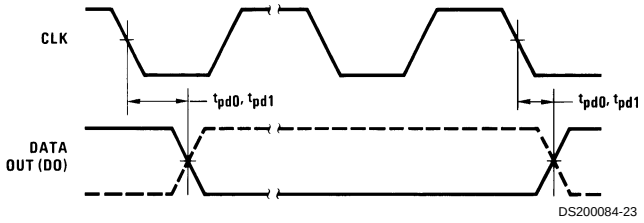
Data Output Timing



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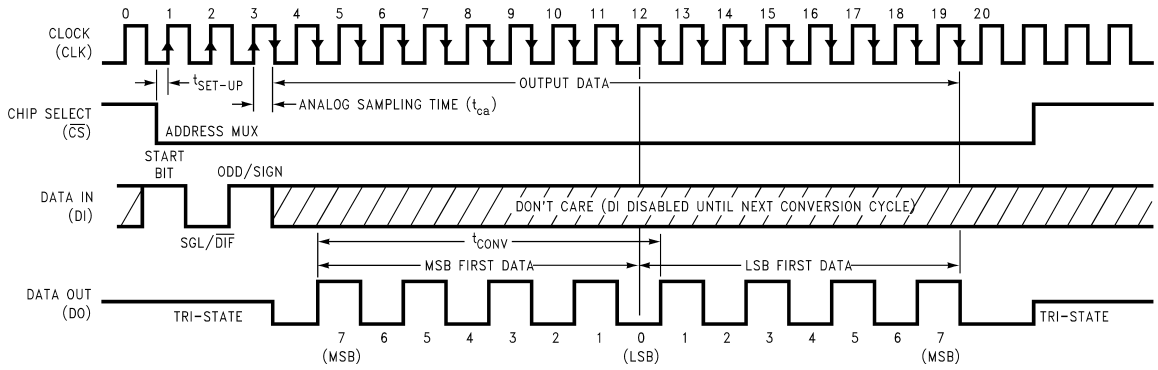
Timing Diagrams (Continued)

ADCV08832 Timing



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Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive approximation routine.

In differential mode the voltage converted is always the difference between the assigned "+" input terminal and the "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

The multiplexor at the analog inputs of the converter provides for the software-configurable single-ended or differential operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. A single ADCV08832 can handle ground referenced inputs, differential inputs, as well as signals with some arbitrary reference voltage.

The input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs will be enabled, and whether this input is single-ended or differential. In addition to selecting the differential mode, the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated in the MUX addressing tables.

MUX Addressing: ADCV08832

Single-Ended MUX Mode				
MUX Address			Channel #	
Start Bit	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	1	0	+	
1	1	1		+

Differential MUX Mode				
MUX Address			Channel #	
Start Bit	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	0	+	−
1	0	1	−	+

Since the input configuration is under software control, it can be modified as required before each conversion. A channel could be treated as a single-ended, ground referenced input for one conversion; then, it could be reconfigured as part of a differential channel for another conversion.

The analog input voltages for each channel can range from 50mV below ground to 50mV above Vcc without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

An important characteristic of this converter is the serial communication interface with the controlling processor. The serial interface facilitates versatile operation in a small package. The small converter can be placed close to the analog source, converting a low level signal into a noise immune bit stream.

To understand the operation of these converters, it is best to refer to the Timing Diagrams and Functional Block Diagram and follow a complete conversion sequence.

1. A conversion is initiated by pulling the $\overline{\text{CS}}$ (chip select) line low. This line must be held low for the entire conversion (13 Clock Cycles). The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the data on the DI line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 bits to be the MUX address.
3. A conversion begins ½ clock after the odd/sign bit is latched. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle to a final analog input value. The DI line is ignored for the remainder of the conversion.
4. On the falling edge of the 3rd clock. DO exits TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

Functional Description (Continued)

5. During the conversion, the output of the SAR comparator indicates whether the successive analog input is greater than (high) or less than (low) a series of voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison, the output of the comparator is clocked to DO on the falling edge of CLK.
6. After 8 clock periods the successive approximation routine is completed.
7. Next, the stored data in the successive approximation register is loaded into an internal shift register and shifted out LSB first. The DO line then goes low until CS is returned high.
8. The DI and DO lines may be tied together and controlled through a bi-directional processor I/O bit with one wire. This is possible because the DI input is valid only during the MUX addressing interval, while the DO line is still in a high impedance state.

3.0 Reducing Power Consumption

At 3.3V supply, the ADCV08832 consumes about 330 µA when $\overline{CS}$ is logic low. When $\overline{CS}$ is pulled high the device will enter a low power mode to minimize total power consumption.

In low power mode some analog circuitry and digital logic are put in a static, low power condition. Also, DO, the output driver is taken into a TRI-STATE mode.

To optimize static power consumption, special attention must be given to the digital input logic signals: CLK, CS, DI. Each digital input has a large CMOS buffer between V_{CC} and GND. A traditional TTL level high (2.4V) will be sufficient for each input to read a logical "1". However, there could be a large V_{IH} to V_{CC} voltage difference at each input. Such a voltage difference would cause excessive static power dissipation, even when CS is high and the part is low power mode.

Therefore, to minimize the static power dissipation, it is recommended that all digital logic levels should equal the converter's supply. Various CMOS logic is particularly well suited for this application.

4.0 THE ANALOG INPUTS

The most important feature of the ADCV08832 is that it can be located right at the analog signal source and through just a few wires can communicate with a controlling processor. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, the following must be considered for situations in which the analog input sources are noisy or riding on a large common-mode voltage.

In a true differential input stage, any signal that is common to both "+" and "-" inputs is cancelled. For the ADCV08832 the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_{ca}). The negative input needs to be stable during the complete conversion sequence because it is sampled before every decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely cancelled and will cause some conversion errors. The linear worse case approximation of a common mode sinusoidal signal error is:

$V_{error}(MAX) = V_{PEAK}\ (2\pi f_{CM})(t_{conv})$

Where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_{conv} is the A/D's conversion time ($t_{conv} = 13/f_{CLK}$).

For a 60 Hz common-mode signal to generate a ¼ LSB error (5 mV) with the converter running at 500 kHz, its peak value would have to be 0.328V.

4.1 Sample and Hold

The ADCV08832 provides a built-in sample-and-hold to acquire the input signal. The sample and hold can sample input signals in either single-ended or pseudo differential mode.

4.2 Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time. To achieve the full sampling rate, the analog input should be driven with a low impedance source (100Ω) or a high-speed op amp such as the LM6142. Higher impedance sources or slower op amps can easily be accommodated by allowing more time for the analog input to settle.

4.3 Source Resistance

The analog inputs of the ADCV08832 appears as a 13 pF capacitor (C_{IN}) in series with a 300Ω resistor (R_{ON}). C_{IN} gets switched between the selected "+" and "-" inputs during each conversion cycle. Large external source resistors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog input to completely settle.

4.4 Board Layout Considerations, Grounding and Bypassing

The ADCV08832 should be used with an analog ground plane and single-point grounding techniques. The GND pin should be tied directly to the ground plane.

The supply pin should be bypassed to the ground plane with a ceramic capacitor with leads as short as possible in single ended mode. All analog inputs should be referenced directly to the single-point ground.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The offset of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. In differential mode the converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 6.4 mV).

6.0 DYNAMIC PERFORMANCE

Dynamic performance specifications are often useful in applications requiring waveform sampling and digitization. Typically, a memory buffer is used to capture a stream of consecutive digital outputs for post processing. Capturing a number of samples that is a power of 2 (ie, 1024, 2048, 4096) allows the Fast Fourier Transform (FFT) to be used to

Functional Description (Continued)

digitally analyze the frequency components of the signal. Depending on the application, further digital processing can be applied.

6.1 Sampling Rate

The Sampling Rate, sometimes referred to as the Throughput Rate, is the time between repetitive samples by an Analog-to-Digital Converter. The sampling rate includes the conversion time, as well as other factors such a MUX setup time, acquisition time, and interfacing time delays. Typically, the sampling rate is specified in the number of samples taken per second, at the maximum analog-to-digital converter clock frequency.

Signals with frequencies exceeding the Nyquist frequency (1/2 the sampling rate), will be aliased into frequencies below the Nyquist frequency. To prevent signal degradation, sample at twice (or more) than the highest frequency component of the input signal and/or use of a low pass (anti-aliasing) filter on the front-end. Sampling at a much higher rate than the input signal will reduce the requirements of the anti-aliasing filter.

6.2 Signal-to-Noise Ratio

Signal-to-Noise Ratio (SNR) is the ratio of RMS magnitude of the fundamental to the RMS sum of all the non-fundamental signal, excluding the harmonics, up to 1/2 of the sampling frequency (Nyquist).

6.3 Total Harmonic Distortion

Total Harmonic distortion is the ratio of the RMS sum of the amplitude of the harmonics to the fundamental input frequency.

$$THD = 20 \log [(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)^{1/2}/V_1]$$

Where V_1 is the RMS amplitude of the fundamental and V_2,V_3, V_4, V_5, V_6 are the RMS amplitudes of the individual harmonics. In theory, all harmonics are included in THD calculations, but in practice only about the first 6 make significant contributions and require measurement.

6.4 Signal-to-Noise and Distortion

Signal-to-Noise And Distortion ratio (SINAD) is the ratio of RMS magnitude of the fundamental to the RMS sum of all the non-fundamental signals, including the noise and harmonics, up to 1/2 of the sampling frequency (Nyquist), excluding DC.

SINAD is also dependent on the number of quantization levels in the A/D Converter used in the waveform sampling process. The more quantization levels, the smaller the quantization noise and theoretical noise performance. The theoretical SINAD for a n-Bit Analog-to-Digital Converter is given by:

$$SINAD = (6.02\ n + 1.76)\ dB$$

Thus, for an 8-bit converter, the ideal SINAD = 49.92 dB

6.5 Effective Number of Bits

Effective Number Of Bits (ENOB) is another specification to quantify dynamic performance. The equation for ENOB is given by:

$$ENOB = [(SINAD - 1.76) / 6.02]$$

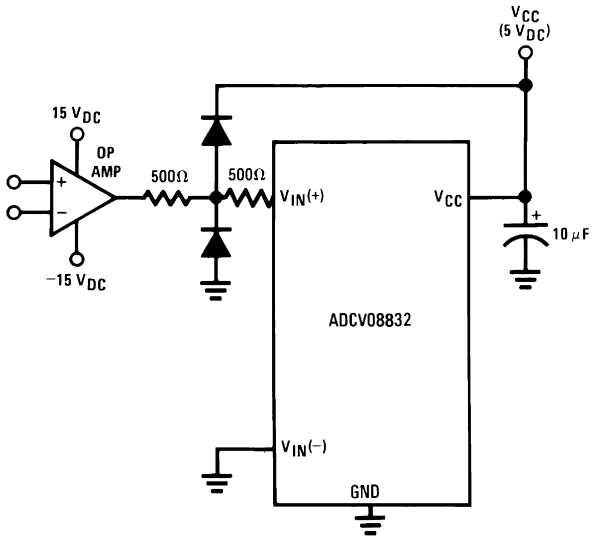
Like SINAD, the Effective Number Of Bits combines the cumulative effect of several errors, including quantization, ADC non-linearities, noise, and distortion.

6.6 Spurious Free Dynamic Range

Spurious Free Dynamic Range (SFDR) is the ratio of the signal amplitude to the amplitude of the highest harmonic or spurious noise component. If the amplitude is at full scale, the specification is simply the reciprocal of the peak harmonic or spurious noise.

Applications

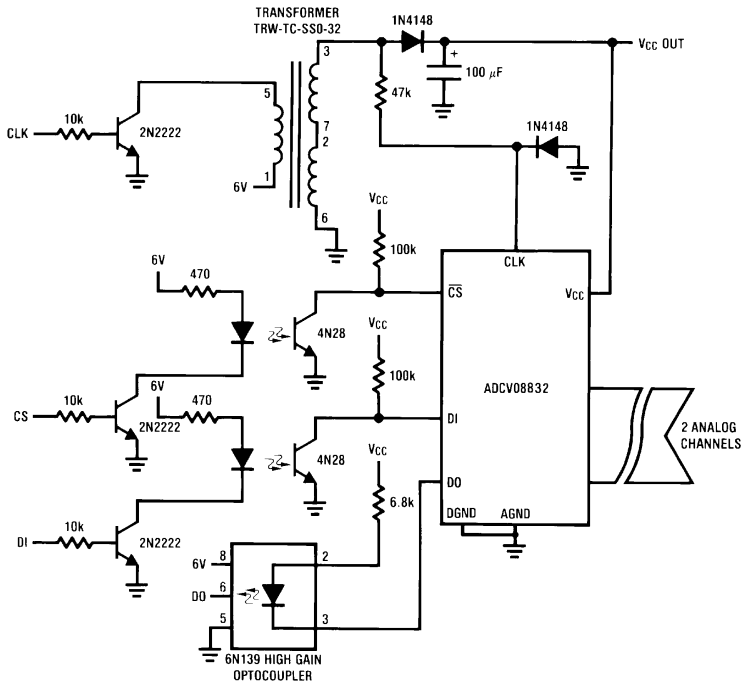
Protecting the Input



DS200084-9

Applications (Continued)

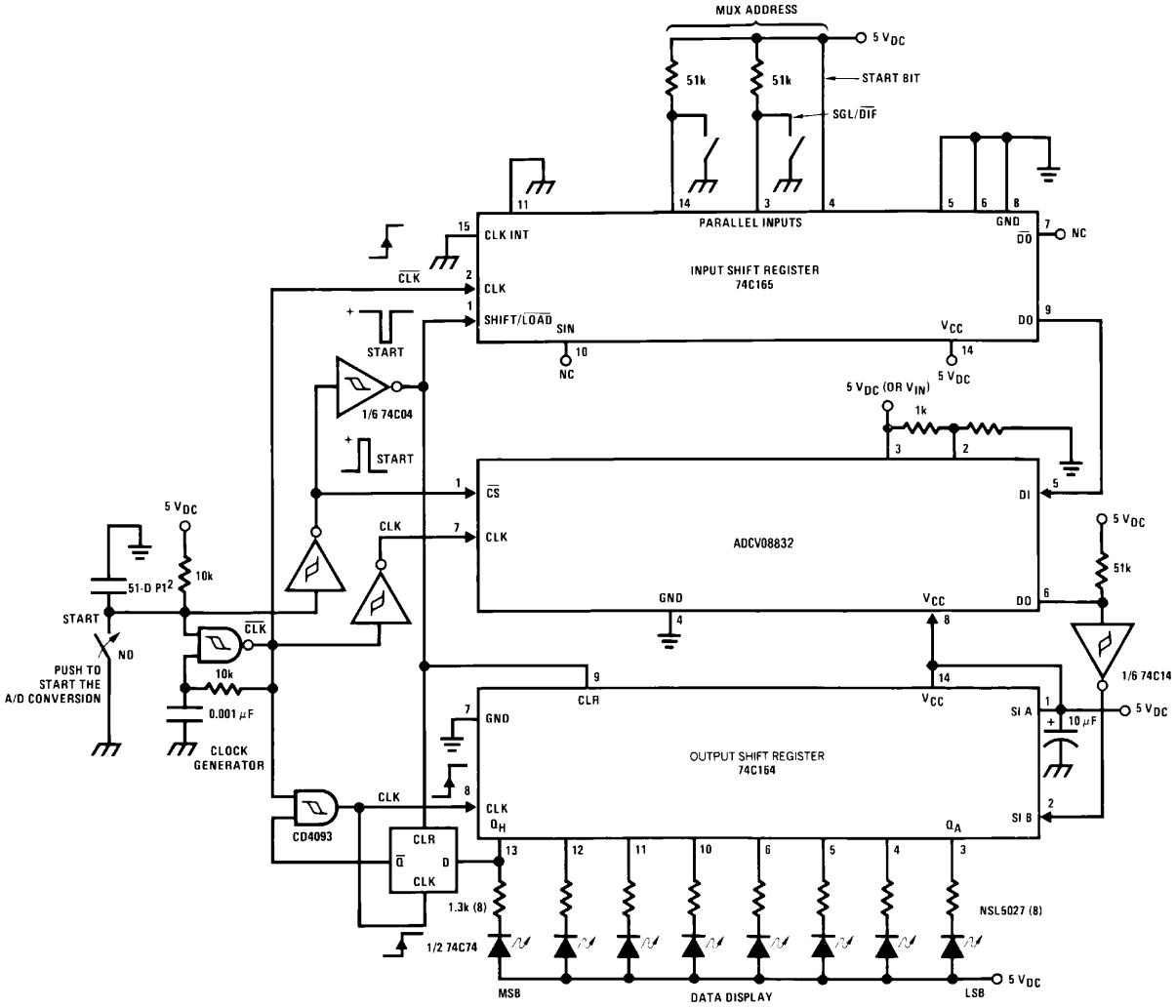
Isolated Data Converter



DS200084-40

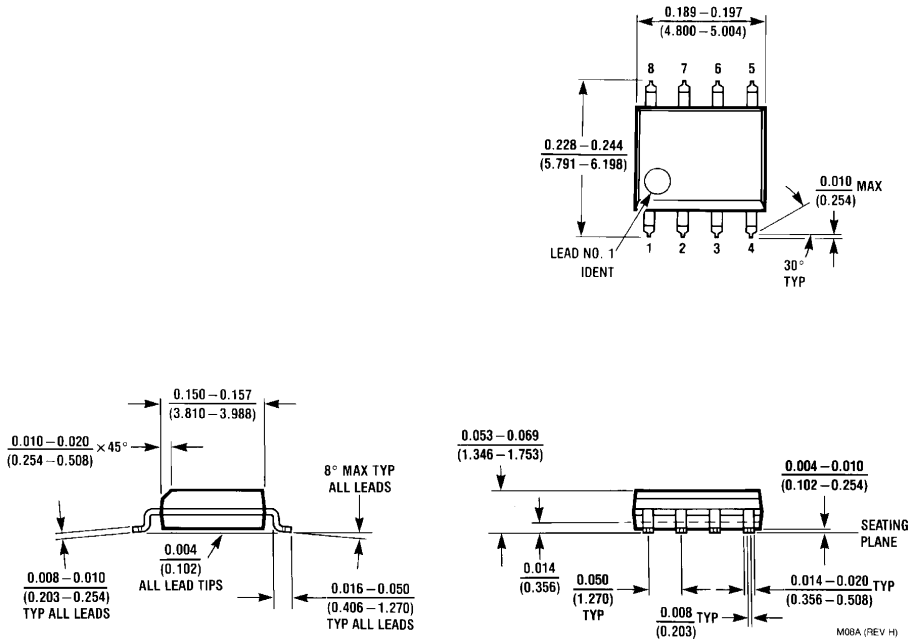
Applications (Continued)

A "Stand-Alone" Hook-Up for ADCV08832 Evaluation



DS200084-39

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number ADCV08832CIM
NS Package Number M08A

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
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National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
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National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADCV08832CIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ADCV0 8832I
ADCV08832CIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ADCV0 8832I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

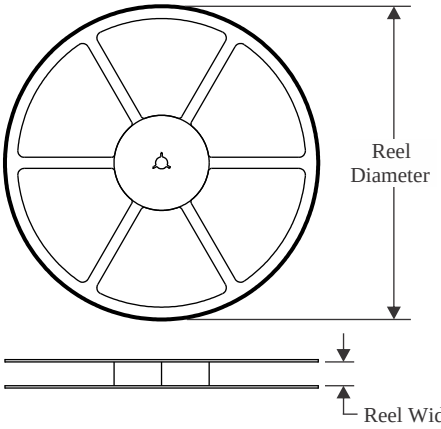
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

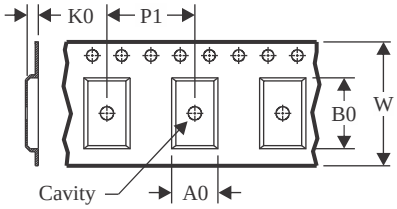
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

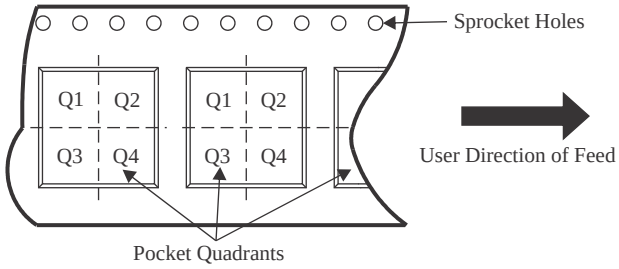


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

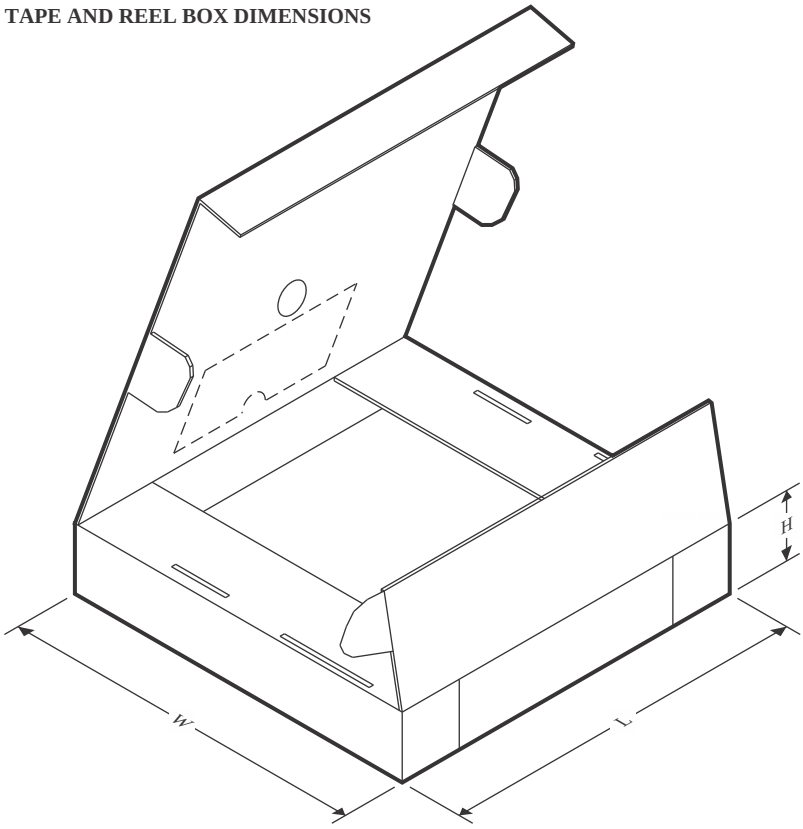
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADCV08832CIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADCV08832CIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

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Last updated 10/2025