ADS1x1S02 Ultra-Small, Low-Power, 12- and 16-Bit, 6 and 4kSPS ADCs With PGA, and Temperature Sensor

1 Features

- Wide supply range: 1.74V to 5.5V
- Low current consumption:
  - 140µA in continuous-converison mode
- 12-bit data rate: 100SPS to 6kSPS
- 16-bit data rate: 10SPS to 4kSPS
- Single-cycle settling
- Internal temperature sensor
- Internal low-drift 1.024V reference
- Internal oscillator
- Operating temperature range: –40°C to +125°C

2 Applications

- Consumer electronics
- Portable instrumentation
- Leak detection in data centers
- Temperature measurement systems
- Factory automation and process control
- General purpose voltage and current monitoring

3 Description

The ADS101S02 and ADS111S02 (ADS1x1S02) are precision, low-power, SPI-compatible, 12- and 16-bit analog-to-digital converters (ADCs). The ADS1x1S02 integrate a low-drift voltage reference, oscillator, a programmable gain amplifier (PGA), and high-accuracy temperature sensor. These features, along with the device wide power supply range from 1.74V to 5.5V, are useful for power- and space-constrained, sensor measurement applications.

The ADS101S02 and ADS111S02 perform conversions at data rates up to 6 and 4kSPS, respectively. The PGA offers gain settings from 1/6 to 16, allowing precise large- and small-signal measurements using the internal 1.024V reference. The ADS1x1S02 feature an input multiplexer (MUX) that allows four single-ended measurements, three differential measurements using AIN3 as a common reference, or two independent differential input pairs.

Package Information

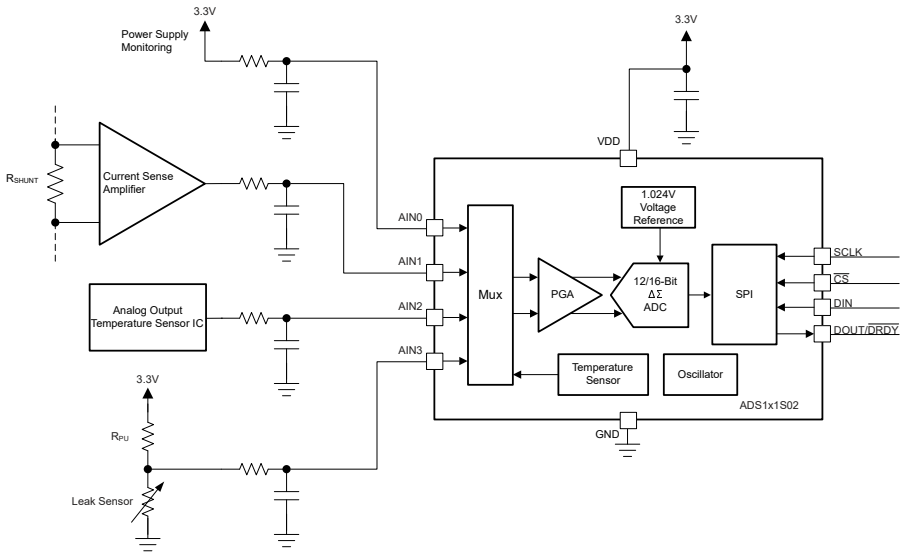
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS1x1S02	RUG (X2QFN, 10)	1.50mm × 2.00mm
	DYN (TSOT, 10)	2.90mm × 2.80mm
	YCJ (DSBGA, 12)	1.38mm × 1.03mm

(1) For all available packages, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	RESOLUTION(1)	DATA RATE (max)
ADS101S02	12-bit	6kSPS
ADS111S02	16-bit	4kSPS

(1) See the *Device Comparison Table* for details.



Server Card System Monitoring

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Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison Table....3
5 Pin Configuration and Functions....3
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Recommended Operating Conditions....6
6.4 Thermal Information....6
6.5 Electrical Characteristics....7
6.6 Timing Requirements....8
6.7 Switching Characteristics....8
6.8 Timing Diagram....8
7 Parameter Measurement Information....9
7.1 Noise Performance....9
8 Detailed Description....10
8.1 Overview....10
8.2 Functional Block Diagrams....10
8.3 Feature Description....11
8.3.1 Multiplexer....11
8.3.2 Voltage Reference....11
8.3.3 Oscillator....11
8.3.4 Output Data Rate and Conversion Time....11
8.3.5 Low-Noise PGA....12
8.3.6 Temperature Sensor....13
8.4 Device Functional Modes....15
8.4.1 Power-Up and Reset....15
8.4.2 Operating Modes....15
8.5 Programming....16
8.5.1 Serial Interface (SPI)....16
8.5.2 Chip Select ($\overline{CS}$)....16
8.5.3 Serial Clock (SCLK)....16
8.5.4 Data Input (DIN)....16
8.5.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)....17
8.5.6 Data Retrieval and Device Configuration....17
8.6 Conversion Data Format....19
9 Register Maps....20
10 Application and Implementation....23
10.1 Application Information....23
10.1.1 Serial Interface Connections....23
10.1.2 Connecting Multiple Devices....24
10.1.3 Single-Ended Inputs....25
10.1.4 Unused Inputs and Outputs....25
10.1.5 Input Protection....25
10.1.6 Analog Input Filtering....26
10.1.7 Duty Cycling For Low Power....27
10.1.8 Pseudo Code Example....28
10.2 Typical Applications....29
10.2.1 K-Type Thermocouple with Thermistor Cold-Junction Compensation....29
10.2.2 Server Card System Monitoring Application....31
10.3 Power Supply Recommendations....32
10.3.1 Power-Supply Sequencing....32
10.3.2 Power-Supply Decoupling....32
10.4 Layout....33
10.4.1 Layout Guidelines....33
10.4.2 Layout Example....34
11 Device and Documentation Support....35
11.1 Documentation Support....35
11.1.1 Related Documentation....35
11.2 Receiving Notification of Documentation Updates....35
11.3 Support Resources....35
11.4 Trademarks....35
11.5 Electrostatic Discharge Caution....35
11.6 Glossary....35
12 Revision History....35
13 Mechanical, Packaging, and Orderable Information....35

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4 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	INTERFACE	DIGITAL I/O LEVELS
ADS101C01	12	6000	1 (1)	I^2C	Ratiometric to VDD
ADS101C02	12	6000	2 (4)	I^2C	Ratiometric to VDD
ADS111C01	16	4000	1 (1)	I^2C	Ratiometric to VDD
ADS111C02	16	4000	2 (4)	I^2C	Ratiometric to VDD
ADS101C01L	12	6000	1 (1)	I^2C	Independent of VDD
ADS101C02L	12	6000	2 (4)	I^2C	Independent of VDD
ADS111C01L	16	4000	1 (1)	I^2C	Independent of VDD
ADS111C02L	16	4000	2 (4)	I^2C	Independent of VDD
ADS101S02	12	6000	2 (4)	SPI	Ratiometric to VDD
ADS111S02	16	4000	2 (4)	SPI	Ratiometric to VDD

5 Pin Configuration and Functions

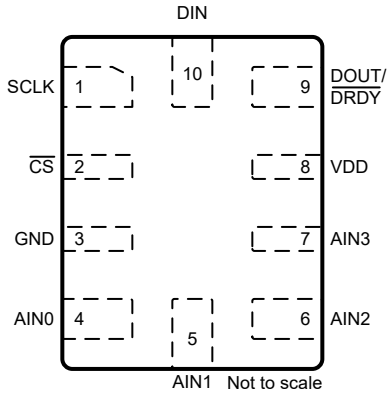


Figure 5-1. RUG Package, (Top View)

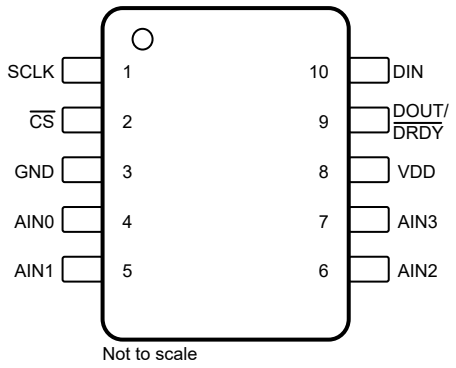


Figure 5-2. DYN Package, (Top View)

Table 5-1. Pin Functions:

PIN		TYPE	DESCRIPTION(1)
NO.	NAME		
4	AIN0	Analog input	Analog input 0
5	AIN1	Analog input	Analog input 1
6	AIN2	Analog input	Analog input 2
7	AIN3	Analog input	Analog input 3
2	$\overline{CS}$	Digital input	Chip select input. Active low. (3)
10	DIN	Digital input	Serial data input
9	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready. Active low.(2)
3	GND	Supply	Ground
1	SCLK	Digital input	Serial data clock input
8	VDD	Supply	Power supply. Connect a 0.1µF, power supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.
(2) Push-pull output.
(3) The ADS1x1S02 can be operated with $\overline{CS}$ tied low permanently if the device is the only peripheral on the SPI bus.

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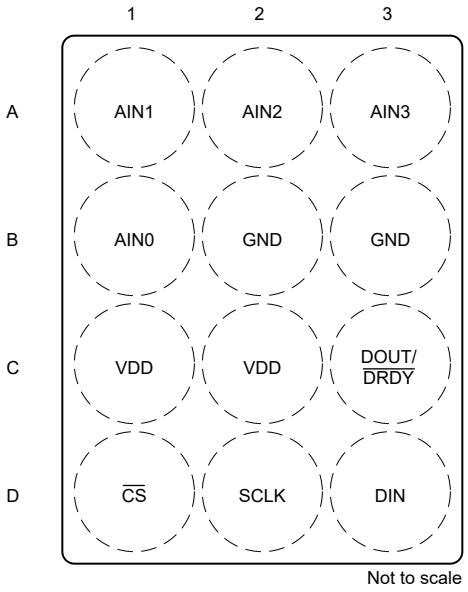


**Figure 5-3. YCJ Package,
12-Pin DSBGA(Top View)**

Table 5-2. Pin Functions: YCJ Package

PIN		TYPE	DESCRIPTION[1]
ADS1x1S02	NAME		
B1	AIN0	Analog input	Analog input 0
A1	AIN1	Analog input	Analog input 1
A2	AIN2	Analog input	Analog input 2
A3	AIN3	Analog input	Analog input 3
D1	$\overline{CS}$	Digital input	Chip select input. Active low. [3]
D3	DIN	Digital input	Serial data input
C3	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready. Active low.[2]
B2, B3	GND	Ground	Ground
D2	SCLK	Digital input	Serial data clock input
C1, C2	VDD	Supply	Power supply. Connect a 0.1µF, power-supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.
(2) Push-pull output.
(3) The ADS1x1S02 can be operated with $\overline{CS}$ tied low permanently if the device is the only peripheral on the SPI bus.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, SDI, SDO/$\overline{DRDY}$	GND – 0.3	VDD + 0.3	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Power supply	VDD to GND	1.74		5.5	V
ANALOG INPUTS(1)						
V_{AINx}	Absolute input voltage		GND		VDD	V
V_{IN}	Differential input voltage(2)(3)	Unipolar straight binary coding	0		V_{REF} / Gain	V
		Binary two's complement coding	$-V_{REF}$ / Gain		V_{REF} / Gain	
DIGITAL INPUTS						
	Input voltage		GND		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the selected positive and negative inputs of the ADC.
(2) V_{REF} = 1.024V (typical)
(3) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V or 5.5V (whichever is smaller) must be applied to this device. See Table 8-1 and Table 8-2 for more information.

6.4 Thermal Information

THERMAL METRIC(1)		DYN (TSOT)	RUG (X2QFN)	YCJ (DSBGA)	UNIT
		10 PINS	10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	245.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	69.3	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	172	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	8.2	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	170.8	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 1.74V to 5.5V, all data rates, all gain settings (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	GND ≤ V_{AINx} ≤ VDD, V_{IN} = 0V		±15		nA
	Differential input current	V_{CM} = VDD/2, –V_{REF}/Gain ≤ V_{IN} ≤ V_{REF}/Gain		±25		nA
	Common-mode input impedance	TBD		100		MΩ
	Differential input impedance	TBD		100		MΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)	ADS101S02	12			Bits
		ADS111S02	16			
DR	Data rate	ADS101S02		100, 500, 2000, 6000		SPS
		ADS111S02		10, 100, 1000, 4000		
	Noise (input-referred)			See *Noise Performance* section		
INL	Integral nonlinearity (best fit)			TBD		ppm_{FSR}
	Gain settings			1/6, 1/4, 1/2, 1, 2, 4 ,8, 16		
	Offset error (input referred)	Differential inputs		±5		µV
		Single-ended inputs		±25		
	Offset drift	Differential inputs		40		nV/°C
		Single-ended inputs		150		
	Gain error	T_A = 25°C, including error of internal voltage reference	–0.5	±0.1	0.5	%
	Gain drift	Including drift of internal voltage reference		2.5	25	ppm/°C
V_{REF}	Reference voltage			1.024		V
CMRR	Common-mode rejection ratio	At dc		120		dB
		f_{CM} = 50Hz or 60Hz, DR = TBD		105		
PSRR	Power-supply rejection ratio	At dc		100		dB
OSCILLATOR						
f_{OSC}	Frequency			1000		kHz
	Accuracy	All data rates	–5		5	%
TEMPERATURE SENSOR						
	Temperature resolution	ADS101S02		0.125		°C/LSB
		ADS111S02		0.03125		
	Accuracy	T_A = –40°C to +125°C, ADS101S02	–1	±0.25	1	°C
		T_A = –40°C to +125°C, ADS111S02	–1	±0.25	1	
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		GND		0.3 VDD	V
V_{IH}	Logic input level, high		0.7 VDD		VDD	V
V_{OL}	Logic output level, low	I_{OL} = 1mA	GND		0.2 VDD	V
V_{OH}	Logic output level, high	I_{OH} = 1mA	0.8 VDD		VDD	V
	Input current	GND ≤ $V_{Digital\ Input}$ ≤ VDD	–10		10	µA
SUPPLY CURRENT AND POWER DISSIPATION						
I_{VDD}	Supply current	Power-down		2.5	10	µA
		Operating		140	220	
P_D	Power dissipation	VDD = 5.5V		0.9		mW
		VDD = 3.3V		0.5		
		VDD = 1.74V		0.2		

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6.6 Timing Requirements

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$t_{c(SC)}$	SCLK period	60		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	30		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	30		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	8		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8		ns
$t_{W(SCIR)}$	Pulse duration, SCLK low to force interface resynchronization	28		ms

6.7 Switching Characteristics

over operating ambient temperature range, C_{LOAD} = 20pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT/$\overline{DRDY}$ driven				25	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT/$\overline{DRDY}$ high impedance state				25	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{DRDY}$				28	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		8			µs

6.8 Timing Diagram

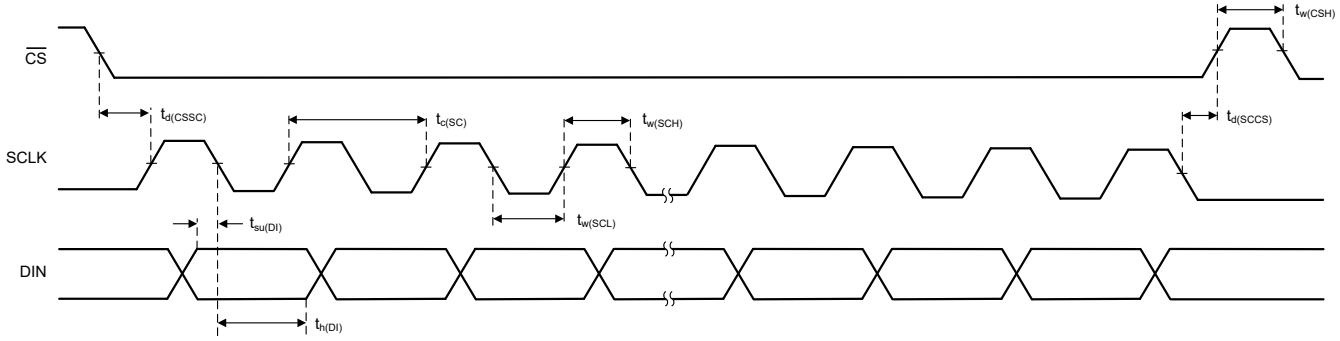


Figure 6-1. Serial Interface Timing Requirements

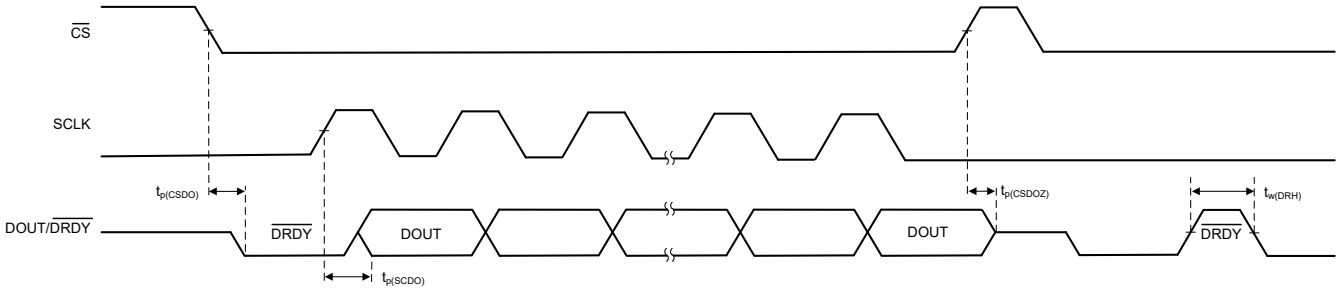


Figure 6-2. Serial Interface Switching Characteristics

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7 Parameter Measurement Information

7.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 7-1 and Table 7-2 show the input-referred noise in units of μV_{RMS} for the conditions shown. The effective resolution values are shown in parenthesis. The effective resolution is calculated from μV_{RMS} values using the following equation. Data are representative of typical noise performance at T_A = 25°C with the inputs shorted together externally using two's compliment data coding.

$$\text{Effective Resolution} = \ln\left[2 \times \frac{V_{REF}}{\text{Gain} \times V_{RMS\ Noise}}\right] \div \ln[2] \quad (1)$$

Table 7-1. Noise in μV_{RMS} (Effective Resolution) for 12-Bit Device at VDD = 3.3V

DATA RATE (SPS)	GAIN							
	1/6	1/4	1/2	1	2	4	8	16
100	45.4 (12)	32.8 (12)	15.9 (12)	8.1 (12)	4.6 (12)	4.6 (12)	4.6 (12)	4.6 (12)
500	90.6 (12)	60.9 (12)	29.3 (12)	15.0 (12)	7.7 (12)	7.6 (12)	7.4 (12)	7.3 (12)
2000	172 (12)	114 (12)	56.9 (12)	28.6 (12)	14.4 (12)	14.3 (12)	14.3 (12)	14.3 (12)
6000	412 (12)	274 (12)	136 (12)	68.3 (12)	35.8 (12)	35.8 (12)	35.4 (12)	34.7 (11.8)

Table 7-2. Noise in μV_{RMS} (Effective Resolution) for 16-Bit Device at VDD = 3.3V

DATA RATE (SPS)	GAIN							
	1/6	1/4	1/2	1	2	4	8	16
10	9.8 (16)	6.9 (16)	3.4 (16)	1.6 (16)	0.83 (16)	0.83 (16)	0.83 (16)	0.83 (16)
100	32.6 (16)	22.2 (16)	11.0 (16)	5.4 (16)	2.7 (16)	2.7 (16)	2.7 (16)	2.7 (16)
1000	112 (16)	74.5 (16)	37.2 (16)	18.6 (16)	9.2 (16)	9.2 (15.7)	9.2 (14.7)	9.2 (13.7)
4000	307 (15.3)	204 (15.3)	102 (15.3)	51.3 (15.3)	25.6 (15.3)	25.6 (14.3)	25.6 (13.3)	25.6 (12.3)

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8 Detailed Description

8.1 Overview

The ADS1x1S02 are a very small, low-power, 12- and 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS1x1S02 consist of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and a SPI interface. These devices integrate a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. Figure 8-1 shows the ADS1x1S02 functional block diagram.

The ADS1x1S02 ADC core measures a differential signal, V_{IN}, that is the difference of V_{AINP} and V_{AINN}. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation of any common-mode signals. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1x1S02 have two available conversion modes: single-shot and continuous-conversion. In single-shot conversion mode, the ADC performs one conversion of the input signal upon request, stores the conversion value to an internal 16-bit Device Conversion Register and then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion completes. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

8.2 Functional Block Diagrams

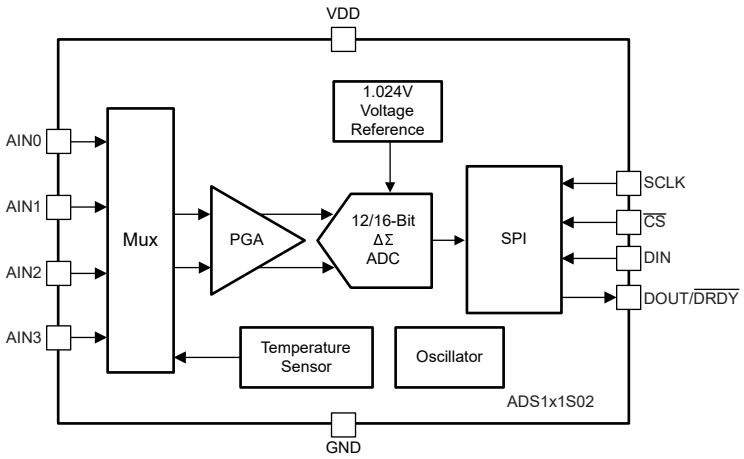


Figure 8-1. ADS1x1S02 Block Diagram

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8.3 Feature Description

8.3.1 Multiplexer

Figure 8-2 shows the input multiplexer (MUX) for the ADS1x1S02. The input multiplexer supports four single-ended measurements referenced to ground, three differential measurements using AIN3 as a common reference input, or two independent differential input pairs. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer. The multiplexer is configured by the MUX[2:0] bits.

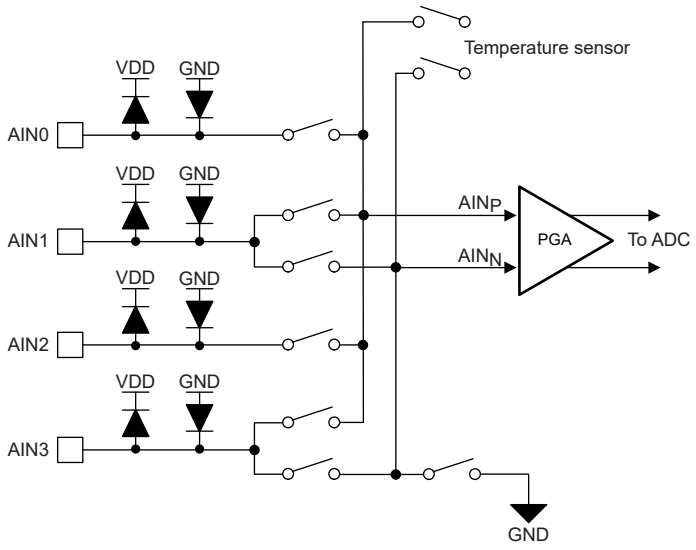


Figure 8-2. Input Multiplexer

Electrostatic discharge (ESD) diodes connected to VDD and GND protect the ADS1x1S02 analog inputs. Keep the absolute voltage of any input within the range shown in Equation 2 to prevent the ESD diodes from turning on.

$$\mathrm{GND} - 0.3\mathrm{V} < \mathrm{V_{AINx}} < \mathrm{VDD} + 0.3\mathrm{V} \quad (2)$$

External Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the *Absolute Maximum Ratings*). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

8.3.2 Voltage Reference

The ADS1x1S02 have an integrated 1.024V voltage reference. An external reference cannot be used with these devices. Errors associated with the internal voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics* table.

8.3.3 Oscillator

The ADS1x1S02 have an integrated 1MHz oscillator. No external clock can be applied to operate these devices. The frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency (f_{MOD}). The 1MHz oscillator frequency is internally divided by a factor of 4 to generate the modulator frequency, f_{MOD} = 250kHz. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

8.3.4 Output Data Rate and Conversion Time

The ADS1x1S02 offer programmable output data rates. Use the DR[1:0] bits to select output data rates of 100SPS, 500SPS, 2kSPS, or 6kSPS for ADS101S02 and 10SPS, 100SPS, 1kSPS, or 4kSPS for ADS111S02. Conversions in the ADS1x1S02 settle within a single cycle. The conversion time is equal to 1 / DR.

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8.3.5 Low-Noise PGA

The ADS1x1S02 integrate a low-noise, low-drift, high input impedance programmable gain amplifier (PGA). Use the PGA[2:0] bits to configure the PGA for gains of 1/6, 1/4, 1/2, 1, 2, 4, 8, or 16. Equation 3 and Equation 4 show how to calculate the full-scale range (FSR), based on the ADC conversion coding using the internal 1.024V reference.

$$FSR_{\text{Binary two's complement coding}} = \pm VREF / Gain \quad (3)$$

$$FSR_{\text{Unipolar straight binary coding}} = 0V \text{ to } +VREF / Gain \quad (4)$$

Use Equation 5 to calculate the LSB size from the FSR and device resolution, n. Table 8-1 summarizes the full-scale range and LSB size when using binary two's compliment coding for all the gain settings, and Table 8-2 shows the full-scale range and LSB size when using unipolar straight binary coding.

$$LSB = FSR / 2^n \quad (5)$$

Table 8-1. Full-Scale Range and LSB Size for Binary Two's Complement Coding

GAIN	FSR	LSB SIZE	
	Binary Two's Compliment	12 Bit	16 Bit
1/6	±6.144V(1)	3mV	187.5µV
1/4	±4.096V(1)	2mV	125µV
1/2	±2.048V	1mV	62.5µV
1	±1.024V	0.5mV	31.25µV
2	±0.512V	0.25mV	15.625µV
4	±0.256V	0.125mV	7.813µV
8	±0.128V	62.5µV	3.906µV
16	±0.064V	31.25µV	1.953µV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

Table 8-2. Full-Scale Range and LSB Size for Unipolar Straight Binary Coding

GAIN	FSR	LSB SIZE	
	Unipolar Straight Binary	12 Bit	16 Bit
1/6	6.144V(1)	1.5mV	93.75µV
1/4	4.096V(1)	1mV	62.5µV
1/2	2.048V	0.5mV	31.25µV
1	1.024V	0.25mV	15.625µV
2	0.512V	0.125mV	7.813µV
4	0.256V	62.5µV	3.906µV
8	0.128V	31.25µV	1.953µV
16	0.064V	15.625µV	0.9766µV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

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8.3.6 Temperature Sensor

The ADS1x1S02 provide an integrated precision temperature sensor to measure the die temperature. To enable the temperature sensor, set bit TS_EN = 1b. When the temperature sensor is enabled, the MUX[2:0] bit settings have no effect. Temperature readings follow the same process as the analog inputs for starting conversions and reading conversion results.

Temperature data formats differ between devices: the ADS101S02 uses 12-bit representation while the ADS111S02 uses 14-bit representation. The temperature data are left-justified within the 16-bit conversion register in both cases.

8.3.6.1 12-Bit Temperature Data Format (ADS101S02)

The ADS101S02 temperature data are represented as a 12-bit result that is left-justified within the 16-bit conversion register. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary two's complement format, as shown in Table 8-3

Table 8-3. 12-Bit Temperature Data Format (ADS101S02)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0100 0000 0000	400h
75	0010 0101 1000	258h
50	0001 1001 0000	190h
25	0000 1100 1000	0C8h
0.25	0000 0000 0010	002h
0	0000 0000 0000	000h
–0.25	1111 1111 1110	FFEh
–25	1111 0011 1000	F38h
–40	1110 1100 0000	EC0h

8.3.6.2 Converting from Digital Codes to Temperature, 12-Bit Temperature Sensor Data

To convert from digital codes to temperature, first read the data bytes from the device and extract the 12-bit temperature value by right-shifting the result. Figure 8-3 shows the 12-bit temperature sensor data alignment within the 16-bit conversion register. The MSB of the 12-bit value determines the sign: 0b indicates a positive temperature and 1b indicates a negative temperature. For positive temperatures convert the 12-bit binary value to decimal and multiply the result by the temperature sensor LSB size, 0.125°C. For negative temperatures, the value is in two's compliment format. Invert all 12 bits and add 1b, convert to decimal, and multiply the result by the negative temperature sensor LSB size, –0.125°C.

1. Positive temperature example: The device reads back 258h. 258h × 0.125°C = 600 × 0.125°C = 75°C

2. Negative temperature example: The device reads back F38h. Subtract 1b and complement the result: F38h → 0C8h, 0C8h × (–0.125°C) = 200 × (–0.125°C) = –25°C

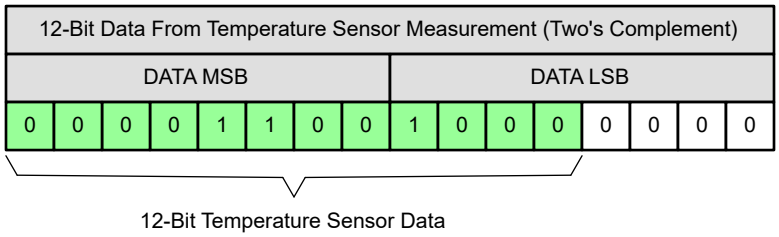


Figure 8-3. 12-Bit Temperature Sensor Data Alignment Within 16-Bit Conversion Register

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8.3.6.3 14-Bit Temperature Data Format (ADS101S02)

The ADS111S02 temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary two's complement format, as shown in Table 8-4

Table 8-4. 14-Bit Temperature Data Format (ADS111S02)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000h
50	00 0110 0100 0000	0640h
25	00 0011 0010 0000	0320h
0.25	00 0000 0000 1000	0008h
0.03125	00 0000 0000 0001	0001h
0	00 0000 0000 0000	0000h
–0.25	11 1111 1111 1000	3FFFh
–25	11 1100 1110 0000	3CE0h
–40	11 1011 0000 0000	3B00h

8.3.6.4 Converting from Digital Codes to Temperature, 14-Bit Temperature Sensor Data

To convert from digital codes to temperature, first read the data bytes from the device and extract the 14-bit temperature value by right-shifting the result. Figure 8-4 shows the 14-bit temperature sensor data alignment within the 16-bit conversion result. The MSB of the 14-bit value determines the sign: 0b indicates a positive temperature and 1b indicates a negative temperature. For positive temperatures convert the 14-bit binary value to decimal and multiply the result by the temperature sensor LSB size, 0.03125°C. For negative temperatures, the value is in two's compliment format. Invert all 14 bits and add 1b, convert to decimal, and multiply the result by the negative temperature sensor LSB size, –0.03125°C.

1. Positive temperature example: The device reads back 0960h. 0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

2. Negative temperature example: The device reads back 3CE0h. Subtract 1b and complement the result. 3CE0h → 0320h, 0320h × (–0.03125°C) = 800 × (–0.03125°C) = –25°C

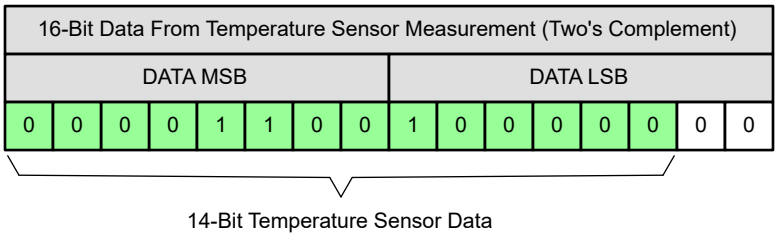


Figure 8-4. 14-Bit Temperature Sensor Data Alignment Within 16-Bit Conversion Result

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8.4 Device Functional Modes

8.4.1 Power-Up and Reset

The ADS1x1S02 reset on power-up and set all bits in the Configuration register to the respective default settings. The ADS1x1S02 enter a power-down state after the reset process completes. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1x1S02 relieves systems with tight power-supply requirements from encountering a surge during power-up.

8.4.2 Operating Modes

The ADS1x1S02 operate in one of two modes: single-shot conversion or continuous-conversion. The MODE bit selects the respective operating mode. Figure 8-5 shows the operation of the device in both single-shot conversion mode and continuous-converison mode.

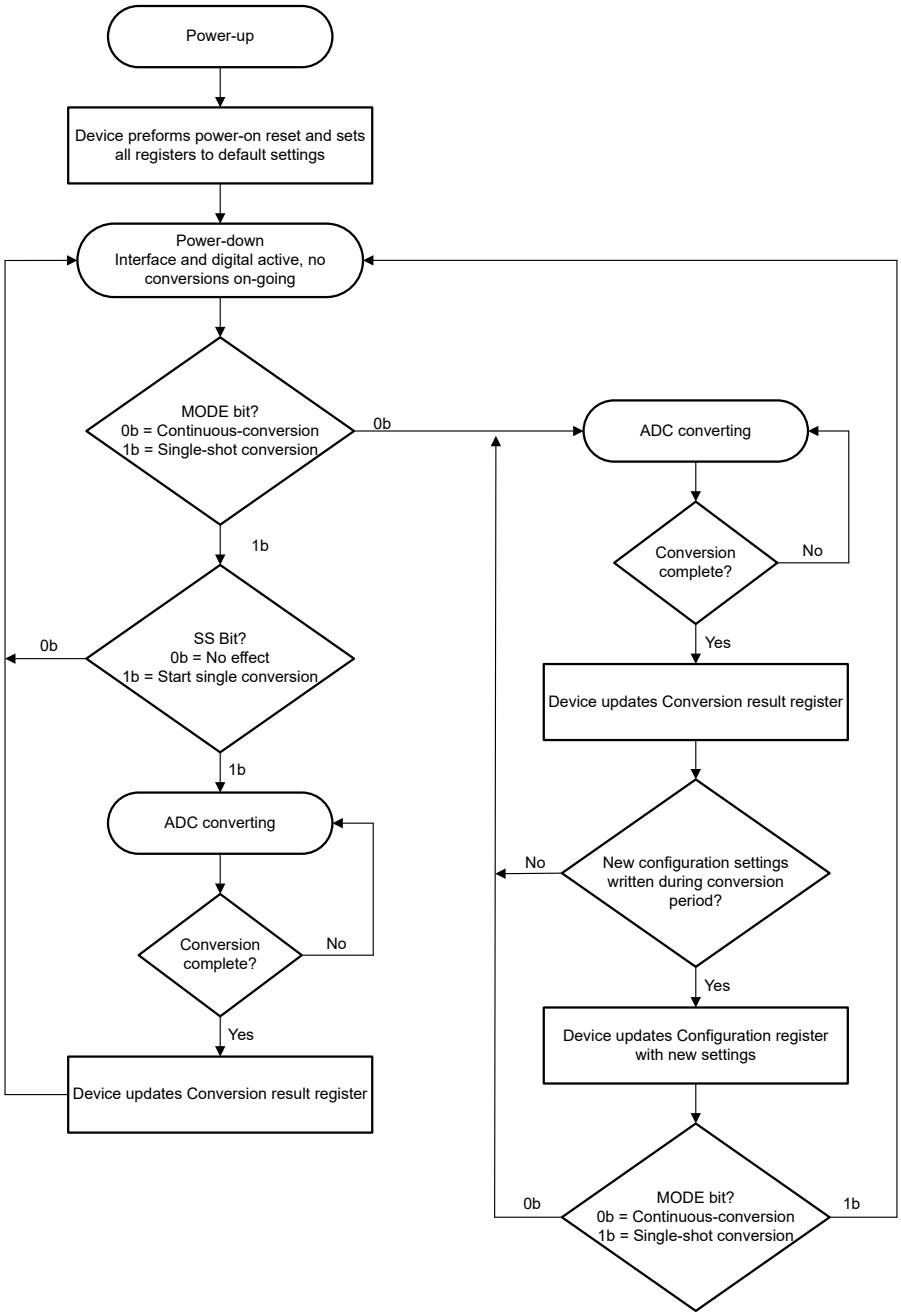


Figure 8-5. Operating Mode State Diagram

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8.4.2.1 Single-Shot Conversion Mode

When the MODE bit is set to 1b, the ADS1x1S02 enter a power-down state, and operate in single-shot conversion mode. This power-down state is the default state for the ADS1x1S02 when power is first applied. The ADS1x1S02 remain in this power-down state until a 1b is written to the single-shot (SS) bit. When the SS bit is asserted, the device power up in approximately 25µs, resets the SS bit to 0b, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. The device still respond to commands, when in power down mode. Writing a 1b to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0b to the MODE bit.

8.4.2.2 Continuous-Conversion Mode

When the MODE bit is set to 0b, the ADS1x1S02 operate in continuous-conversion mode and perform conversions continuously. When a conversion completes, the ADS1x1S02 place the result in the Conversion register and immediately begin another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configurations settings start.

To switch to single-shot conversion mode, write a 1b to the MODE bit. The ongoing conversion stops immediately and the device transitions into the power-down state. To start a single-shot conversion write 1b to the SS bit. Resetting the ADS1x1S02 transitions the device to single-shot conversion mode.

8.5 Programming

8.5.1 Serial Interface (SPI)

The serial interface is used to read conversion data, configure device registers, and control ADC conversions.

The serial interface consists of four lines $\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode. The host always drives SCLK and the device acts as a peripheral. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low, and data update on SCLK rising edges and are latched on SCLK falling edges. The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously.

8.5.2 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the interface for communication. A communication frame starts by taking $\overline{CS}$ low and ends by taking $\overline{CS}$ high. When $\overline{CS}$ is high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state. In this state DOUT/$\overline{DRDY}$ cannot provide data-ready indication. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode.

8.5.3 Serial Clock (SCLK)

SCLK is the serial clock input used to shift data into and out of the ADC. Data on DOUT update on the rising edge of SCLK and data on DIN are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. To reset the serial interface in 3-wire SPI mode hold SCLK low for $t_{W(SCIR)}$. Use this time-out feature to recover communication when a serial interface transmission is interrupted. The next SCLK pulse starts a new communication cycle. When the serial interface is idle, hold SCLK low.

8.5.4 Data Input (DIN)

DIN is the serial interface data input. DIN is used to input data to the device. Input data are latched on the falling edge of SCLK. The ADS1x1S02 never drives the DIN pin.

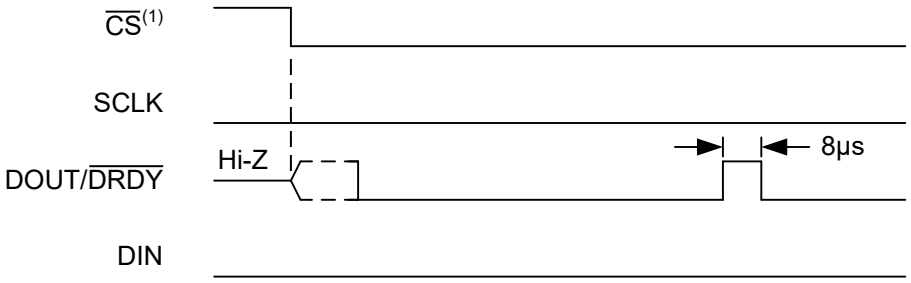
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8.5.5 Data Output and Data Ready (DOUT/$\overline{\text{DRDY}}$)

DOUT/$\overline{\text{DRDY}}$ is a dual-function output pin. During SPI communication, conversion and register data are shifted out on the rising edge of SCLK. This pin also functions as a data-ready indicator, that transitions low when a conversion completes and new data are available. In multi-device systems where conversion completion must be monitored across multiple devices on the SPI bus, periodically lower the $\overline{\text{CS}}$ to poll the DOUT/$\overline{\text{DRDY}}$ status of the device. This method allows the system to identify which device has completed a conversion without requiring dedicated interrupt lines for each device.

When operating in continuous-conversion mode, $\overline{\text{CS}}$ can be periodically pulled low to use DOUT/$\overline{\text{DRDY}}$ as a data ready signal. If no data transfer occurs, DOUT/$\overline{\text{DRDY}}$ transitions high 8µs before the next conversion completes. DOUT/$\overline{\text{DRDY}}$ can trigger a microcontroller to start reading data. This transition is shown in Figure 8-6. Complete the data transfer before DOUT/$\overline{\text{DRDY}}$ returns high, to avoid missing subsequent conversion results.



(1) In continuous-conversion mode $\overline{\text{CS}}$ can be held low. If $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{DRDY}}$ asserts low indicating new data are available.

Figure 8-6. DOUT/$\overline{\text{DRDY}}$ Behavior Without Data Retrieval in Continuous-Conversion Mode With $\overline{\text{CS}}$ Held Low

When $\overline{\text{CS}}$ is high, DOUT/$\overline{\text{DRDY}}$ is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/$\overline{\text{DRDY}}$ floating near midsupply and causing leakage current in the controller. To disable this pullup resistor and configure the pin as a true high-impedance output, set PULL_UP_EN = 0b.

8.5.6 Data Retrieval and Device Configuration

Data is written to and read from the ADS1x1S02 in the same manner for both single-shot and continuous-conversion modes, without having to issue any commands.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Data can be read at any time without concern of data corruption. When DOUT/$\overline{\text{DRDY}}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{\text{DRDY}}$. The MSB of the data on DOUT/$\overline{\text{DRDY}}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out on DOUT/$\overline{\text{DRDY}}$, new Configuration register data are latched on DIN on the SCLK falling edge.

The WRITE_EN[1:0] bits control write access to the Configuration register. The Configuration register is updated only when WRITE_EN[1:0] is set to 01b. All other bit combinations (00b, 10b, 11b) result in a no operation command and prevents the Configuration register from being updated. When a no operation command occurs, DIN data are ignored during SCLK pulses and the Configuration register remains unchanged.

The ADS1x1S02 offers direct readback of the Configuration register settings in the conversion data transmission cycle. The Configuration register data readback transmission cycle consists of 32 bits for and is required for 3-wire SPI mode when $\overline{\text{CS}}$ is tied to ground. When in 4-wire SPI mode the $\overline{\text{CS}}$ is controlled and is not permanently tied low data transmission cycle can consist of 16 bits by taking $\overline{\text{CS}}$ line high after the 16th SCLK cycle, or 32 bits when the Configuration register data readback is used.

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8.5.6.1 32-Bit Data Transmission Cycle

The data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result data, and an additional two bytes of the Configuration register read back data.

To update the Configuration register write the same register settings twice during one transmission cycle as shown in Figure 8-7. Alternatively, write the Configuration register setting once during the first half of the transmission cycle, and then hold the DIN pin either low, as shown in Figure 8-8, or high during the second half of the cycle. If no update to the Configuration register is required, hold the DIN pin either low or high during the entire transmission cycle. The Configuration register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.

A continuous SCLK can be used for the entire 32-bit data transfer as long as the SCLK frequency is less than 1MHz. If an SCLK frequency greater than 1MHz is used, add a delay between the transmission of the first 16 bits and the second 16 bits to allow for complete decoding of the Configuration register write prior to the readback of the Configuration register. Choose the delay such that the time between the SCLK rising edge of the 1st bit of the data and the SCLK rising edge of the 17th bit of data is greater than 16µs.

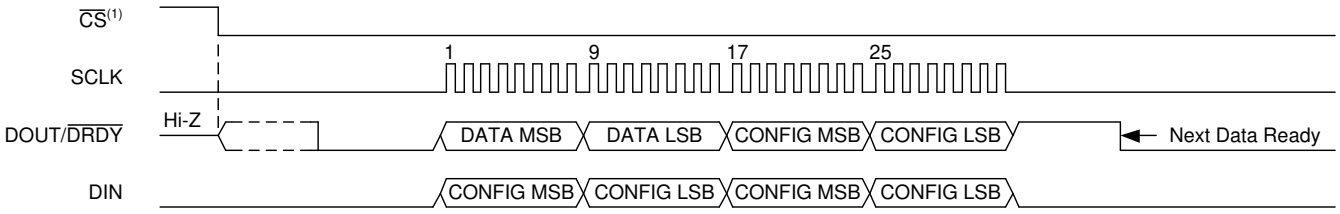


Figure 8-7. 32-Bit Data Transmission Cycle With Config Register Readback

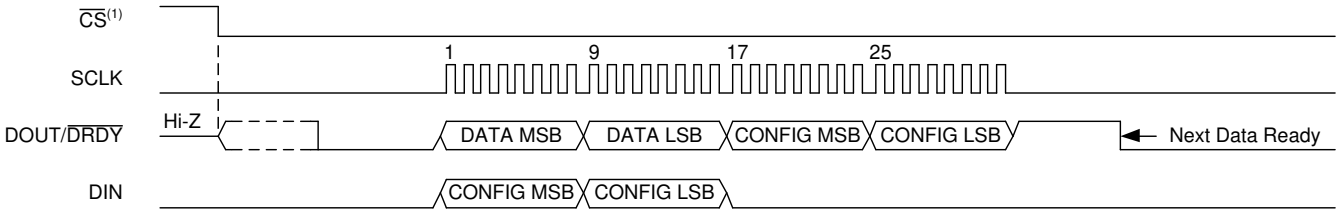


Figure 8-8. 32-Bit Data Transmission Cycle: DIN Held Low

8.5.6.2 16-Bit Data Transmission Cycle

If Configuration register data are not required to be readback conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in Figure 8-9. Take the $\overline{CS}$ line high after the 16th SCLK cycle to reset the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read. The 16-bit data transmission cycle can be used when the $\overline{CS}$ line can be controlled and is not permanently pulled to ground.

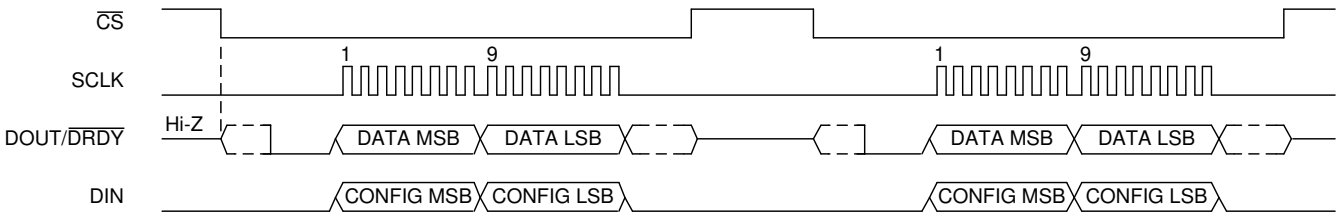


Figure 8-9. 16-Bit Data Transmission Cycle

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8.6 Conversion Data Format

Conversion data are coded depending on the MUX[2:0] configuration. Configurations that use AIN_N = GND use unipolar straight binary data format, all other configurations use binary two's complement data format, MSB first (sign bit). Table 8-5 shows the conversion data format based on the MUX[2:0] settings.

Table 8-5. Conversion Data Format

MUX[2:0]	AIN_P	AIN_N	CONVERSION DATA FORMAT
000b	AIN0	AIN1	Binary Two's Compliment
001b	AIN0	AIN3	Binary Two's Compliment
010b	AIN1	AIN3	Binary Two's Compliment
011b	AIN2	AIN3	Binary Two's Compliment
100b	AIN0	GND	Unipolar Straight Binary
101b	AIN1	GND	Unipolar Straight Binary
110b	AIN2	GND	Unipolar Straight Binary
111b	AIN3	GND	Unipolar Straight Binary

Table 8-6 and Table 8-7 show the output coding for the 12- and 16-bit devices, respectively. In binary two's-complement format, the conversion data clips to positive and negative full-scale code values when the input signal exceeds the respective positive and negative full-scale values. In unipolar straight binary format, conversion data clips to full-scale or zero code values when the input signal exceeds full-scale or is below zero, respectively.

Table 8-6. Ideal Output Code Versus Input Signal (12-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT	UNIPOLAR STRAIGHT BINARY FORMAT
≥ FSR × (2^{12} – 1) / 2^{12}	7FFh	FFFh
≥ FSR × (2^{11} – 1) / 2^{11}		FFEh
FSR / 2^{11}	001h	002h
0	000h	000h
–FSR / 2^{11}	FFFh	
–FSR × (2^{11} – 1) / 2^{11}	801h	
≤ –FSR	800h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

Table 8-7. Ideal Output Code Versus Input Signal (16-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT	UNIPOLAR STRAIGHT BINARY FORMAT
≥ FSR × (2^{16} – 1) / 2^{16}	7FFFh	FFFFh
≥ FSR × (2^{15} – 1) / 2^{15}		FFFEh
FSR / 2^{15}	0001h	0002h
0	0000h	0000h
–FSR / 2^{15}	FFFFh	
–FSR × (2^{15} – 1) / 2^{15}	8001h	
≤ –FSR	8000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

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9 Register Maps

The ADS1x1S02 has two registers that are accessible through the SPI. The Conversion Register contains the result of the last conversion. Use the Configuration Register to change the ADS1x1S02 operating modes and query the status of the devices.

Table 9-1 lists the register access codes.

Table 9-1. Register Access Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
-*n*		Value after reset or the default value

Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary two's-complement format for differential-measurement configurations or unipolar straight binary format in single-ended measurement configurations. Following power up, the Conversion register is cleared to 0000h, and remains 0000h until the first conversion completes. The register format is shown in Figure 9-1.

Table 9-2. 12-bit Device Conversion Register

15	14	13	12	11	10	9	8
D[11:4]							
R-00h							
7	6	5	4	3	2	1	0
D[3:0]				RESERVED#none#			
R-0h				R-0h			

1. ADS101S02 D[3:0] will always read back 0h

Table 9-3. 12-bit Device Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	RESERVED	R	0h	Always reads back 0h

Figure 9-1. 16-bit Device Conversion Register

15	14	13	12	11	10	9	8
D[15:8]							
R-00h							
7	6	5	4	3	2	1	0
D[7:0]							
R-00h							

Table 9-4. 16-bit Device Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

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Configuration Register [reset = 052Bh]

The 16-bit Configuration register controls the operating mode, input selection, data rate, gain, internal temperature sensor, and write enable. The register format is shown in Figure 9-2.

Figure 9-2. Configuration Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0b	R/W-000b			R/W-010b			R/W-1b
7	6	5	4	3	2	1	0
DR[1:0]		RESOLUTION	TS_EN	PULL_UP_EN	WRITE_EN[1:0]		RESERVED
R/W-00b		R-xb	R/W-0b	R/W-1b	R/W-01b		R-1b

Table 9-5. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SS	R/W	0b	**Single-shot conversion start** This bit is used to start a single conversion when the device is configured for single-shot conversion mode (MODE = 1b). SS can only be written when in power-down state and has no effect when a conversion is ongoing. Always reads back 0b. When writing: 0b = No effect 1b = Start a single conversion (when in power-down state)
14:12	MUX[2:0]	R/W	000b	**Input multiplexer configuration** These bits configure the input multiplexer. Configurations that use AIN_N = GND use unipolar straight binary data format, all other configurations use binary two's complement data format, MSB first (sign bit). 000b : AIN_P = AIN0 and AIN_N = AIN1 001b : AIN_P = AIN0 and AIN_N = AIN3 010b : AIN_P = AIN1 and AIN_N = AIN3 011b : AIN_P = AIN2 and AIN_N = AIN3 100b : AIN_P = AIN0 and AIN_N = GND 101b : AIN_P = AIN1 and AIN_N = GND 110b : AIN_P = AIN2 and AIN_N = GND 111b : AIN_P = AIN3 and AIN_N = GND
11:9	PGA[2:0]	R/W	010b	**Programmable gain amplifier configuration** These bits set the gain of the programmable gain amplifier. 000b : Gain = 1/6(1) 001b : Gain = 1/4(1) 010b : Gain = 1/2 011b : Gain = 1 100b : Gain = 2 101b : Gain = 4 110b : Gain = 8 111b : Gain = 16
8	MODE	R/W	1b	**Device operating mode** This bit controls the operating mode. 0b : Continuous-conversion mode 1b : Single-shot conversion mode or power-down state
7:6	DR[1:0]	R/W	00b	**Data rate** These bits control the data rate setting. **ADS101S02**: 00b : 100SPS; 01b : 500SPS; 10b : 2kSPS; 11b : 6kSPS **ADS111S02**: 00b : 10SPS; 01b : 100SPS; 10b : 1kSPS; 11b : 4kSPS
5	RESOLUTION	R	xb	**Resolution identifier** This bit indicates the device resolution. 0b : 12 Bit 1b : 16 Bit

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Table 9-5. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TS_EN	R/W	0b	**Temperature sensor enable** This bit enables the internal temperature sensor for measurement. 0b : Disabled, ADC measures external input configured by MUX[2:0] 1b : Enabled, ADC measures internal temperature sensor
3	PULL_UP_EN	R/W	1b	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{\text{DRDY}}$ pin when $\overline{\text{CS}}$ is high. When enabled, an internal 400kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats. 0b : Pullup resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin 1b : Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin
2:1	WRITE_EN[1:0]	R/W	01b	**Write Enabled** The WRITE_EN[1:0] bits control whether data are written to the Configuration register or not. For data to be written to the Configuration register, the WRITE_EN[1:0] bits must be 01b. Any other value results in no update to the Configuration register. DIN can be held high or low during SCLK pulses without data being written to the Configuration register. 00b : Invalid data, do not update the contents of the Configuration register 01b : Valid data, update the Configuration register 10b : Invalid data, do not update the contents of the Configuration register 11b : Invalid data, do not update the contents of the Configuration register
0	RESERVED	R	1b	**Reserved** Writing either 0b or 1b to this bit has no effect. Always reads back 1b.

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V must be applied to this device.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The ADS1x1S02 are precision, 12- and 16-bit ΔΣ ADCs that offer many integrated features to ease the measurement of the most common sensor types including various types of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1x1S02 in various situations.

10.1.1 Serial Interface Connections

Figure 10-1 shows the principle serial interface connections for the ADS1x1S02.

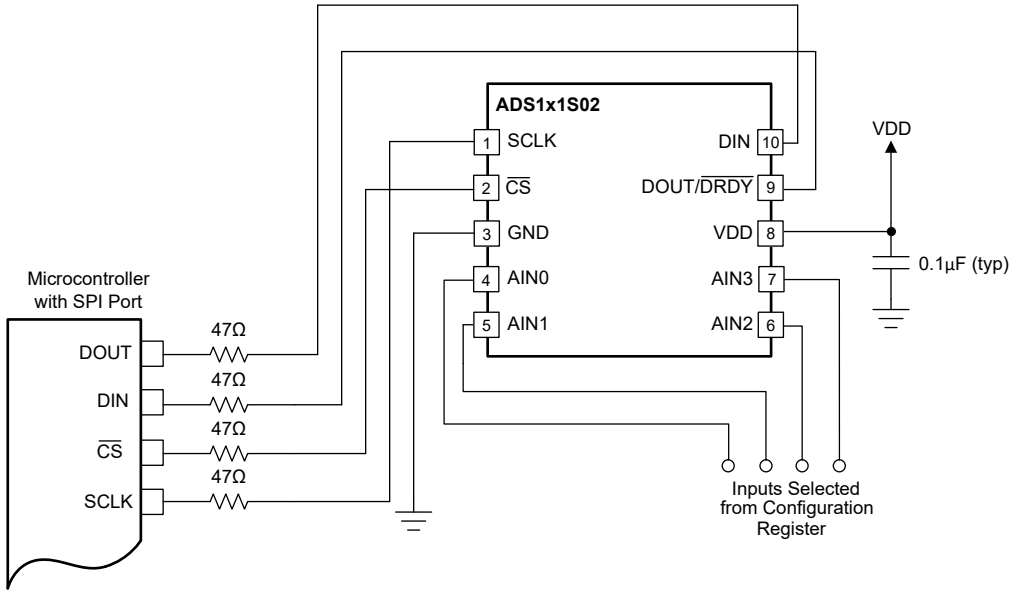


Figure 10-1. Serial Interface Connections

Most microcontroller SPI peripherals can operate with the device. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read on SCLK falling edges.

The $\overline{CS}$ pin can be tied to GND permanently to operate the device in 3-wire SPI mode.

Details of the SPI communication protocol used by the ADS1x1S02 can be found in the *Timing Requirements* section.

Optionally, place resistors in series with all digital input and output pins. Typical series resistor values range from 10Ω to 50Ω. This resistance smooths sharp signal transitions, suppresses overshoot, and offers some overvoltage protection. Take care to meet all SPI timing requirements because these additional series resistors interact with the bus capacitance present on the digital signal lines.

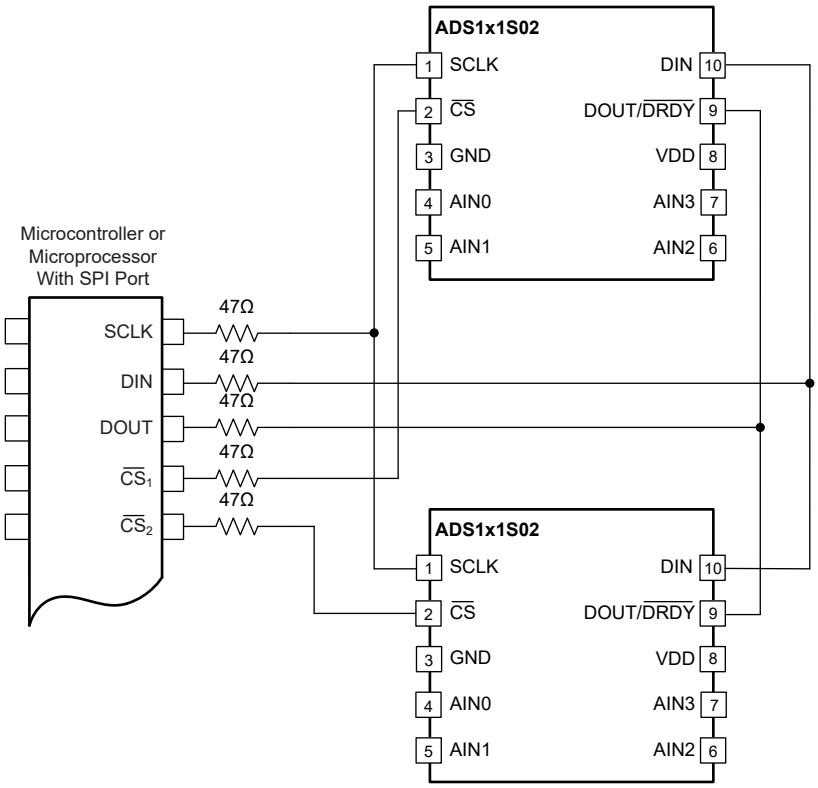
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10.1.2 Connecting Multiple Devices

When connecting multiple ADS1x1S02 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be shared while using a dedicated $\overline{\text{CS}}$ for each SPI enabled device. By default DOUT/$\overline{\text{DRDY}}$ is pulled up to VDD by an internal weak pullup resistor when $\overline{\text{CS}}$ goes high. This feature prevents DOUT/$\overline{\text{DRDY}}$ from floating near midrail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit is set to 0b, the DOUT/$\overline{\text{DRDY}}$ pin enters a High-Z mode when $\overline{\text{CS}}$ transitions high. DOUT/$\overline{\text{DRDY}}$ cannot issue a data ready pulse when $\overline{\text{CS}}$ is high.

To evaluate when a new conversion is ready when using multiple devices, the controller can periodically drop the $\overline{\text{CS}}$ line to the ADS1x1S02. If the DOUT/$\overline{\text{DRDY}}$ line drives low, new data are currently available for clocking out at any time. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available and the ADS1x1S02 returns the last read conversion result. Valid data can be retrieved from the ADS1x1S02 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 10-2. Connecting Multiple ADS1x1S02s

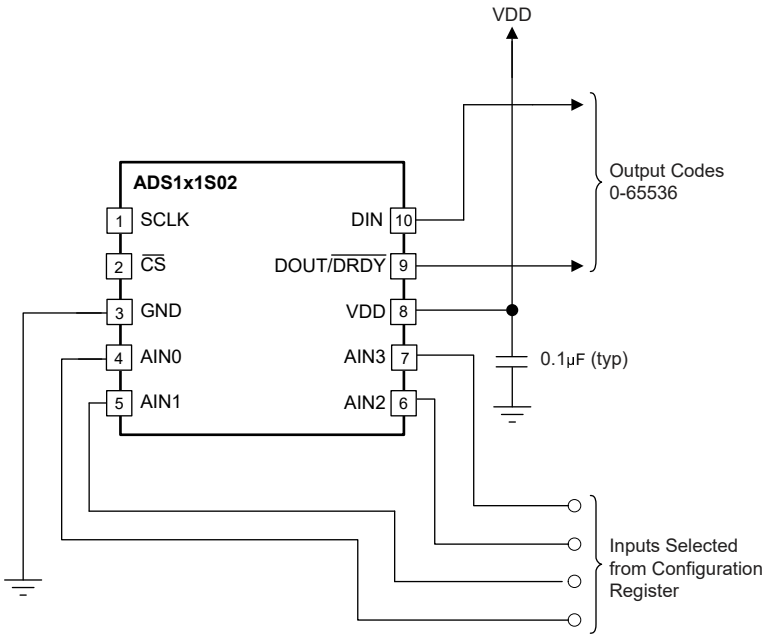
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10.1.3 Single-Ended Inputs

The ADS1x1S02 can measure up to four, single-ended input signals. The ADS1x1S02 measures single-ended signals by appropriate configuration of the MUX[2:0] bits.

Figure 10-3 shows a single-ended connection scheme for the ADS1x1S02. The single-ended signal ranges from 0V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the ADS1x1S02 can only accept positive voltages with respect to ground. The ADS1x1S02 do not lose linearity within the input range.

Single-ended configurations output data in unipolar straight binary format. See the *Conversion Data Format* section for data coding information. Differential configurations provide better common-mode noise rejection than single-ended configurations.



Digital pin connections omitted for clarity.

Figure 10-3. Measuring Single-Ended Inputs

The ADS1x1S02 also allows AIN3 to serve as a common point for measurements by appropriate setting of the MUX[2:0] bits. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1x1S02 operates with inputs, where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < V_{AIN3} < VDD. However, common-mode noise attenuation is not offered.

10.1.4 Unused Inputs and Outputs

Follow the guidelines below for the connection of unused device pins:

- Either float unused analog inputs, or tie unused analog inputs to GND.

10.1.5 Input Protection

The ADS1x1S02 are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1x1S02 can be permanently damaged by analog input voltages that exceed approximately 300mV beyond the rails for extended periods. Place current-limiting resistors in series with the analog inputs to protect against overvoltage events.

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10.1.6 Analog Input Filtering

Analog input filtering serves two purposes: limit the effect of aliasing during the sampling process and reduce external noise from being a part of the measurement.

Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC, also known as the *Nyquist frequency*. These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter, as shown in Figure 10-4, repeats at multiples of the sampling frequency, also known as the modulator frequency (f_{MOD}). Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency, or multiples thereof, are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

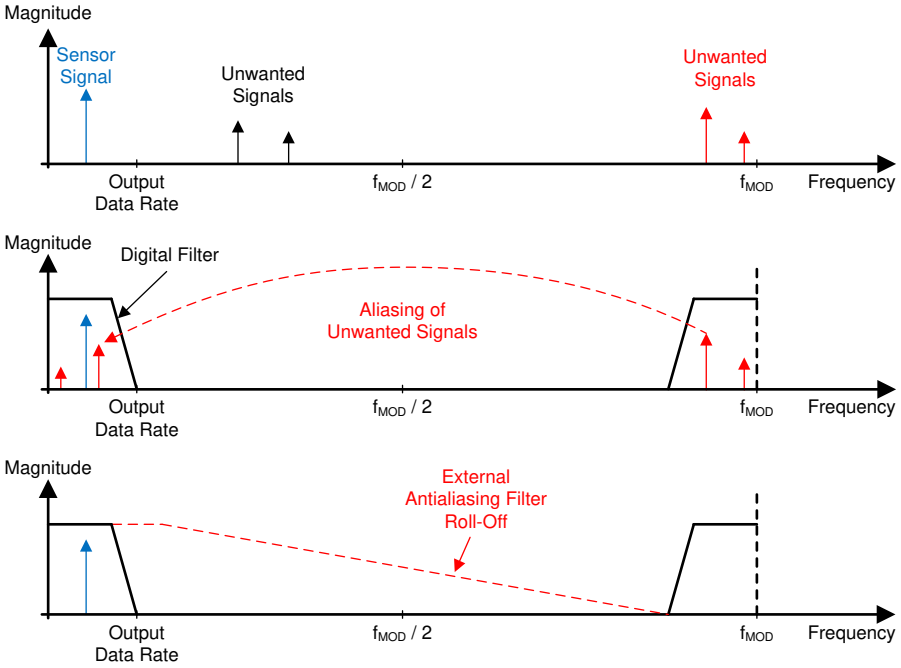


Figure 10-4. Effect of Aliasing

Many sensor signals are inherently band-limited (for example, the output of a thermocouple has a limited rate of change). In this case, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is, in most cases, sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Generally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1x1S02 attenuate signals to a certain degree. In addition, noise components are typically smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

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10.1.7 Duty Cycling For Low Power

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates is not always required. For these applications, the ADS1x1S02 support duty cycling that yields significant power savings by periodically requesting high data rate readings at an effectively lower data rate.

The ADS111S02 operating in power-down mode can achieve an effective 10SPS data rate by executing single-shot conversions every 100ms under microcontroller control, with a 4kSPS data rate configured. A conversion at 4kSPS only requires approximately 0.25ms, so the device enters power-down state for the remaining 99.75ms. In this configuration, the device consumes approximately 1/400th the power consumed in continuous-conversion mode.

The duty cycling rate is completely arbitrary and is defined by the controller. The ADS1x1S02 offer lower data rates that do not implement duty cycling and improved noise performance if required.

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10.1.8 Pseudo Code Example

The flow chart in Figure 10-5 shows a pseudo code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1x1S02. As an example, the default Configuration Register settings are changed to set up the device for Gain = 2, continuous-conversion mode and 100SPS data rate.

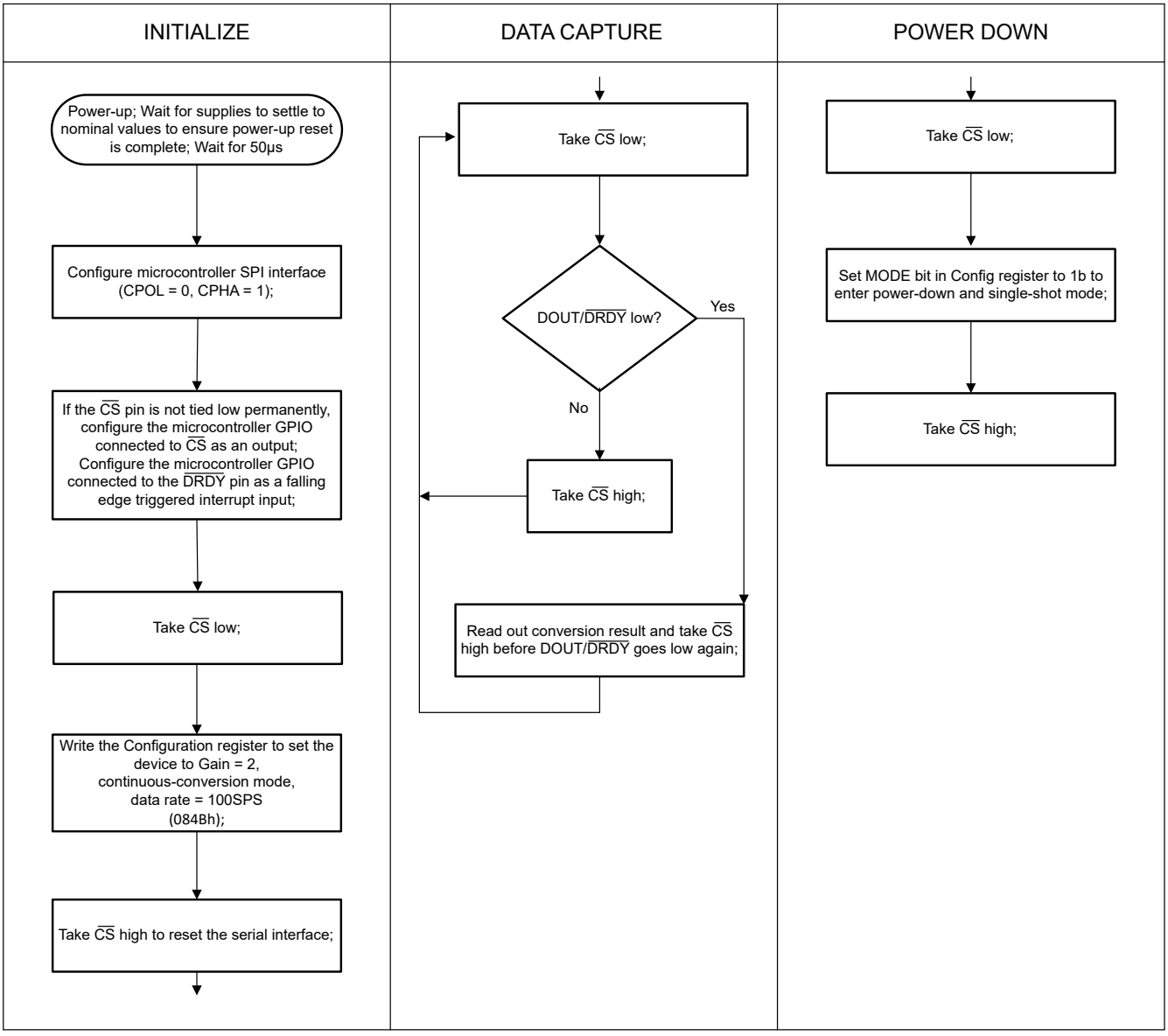


Figure 10-5. Pseudo Code Example Flow Chart

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10.2 Typical Applications

10.2.1 K-Type Thermocouple with Thermistor Cold-Junction Compensation

The application example in Figure 10-6 shows how to use the ADS1x1S02 to monitor a K-Type thermocouple using a linear PTC thermistor for cold-junction compensation.

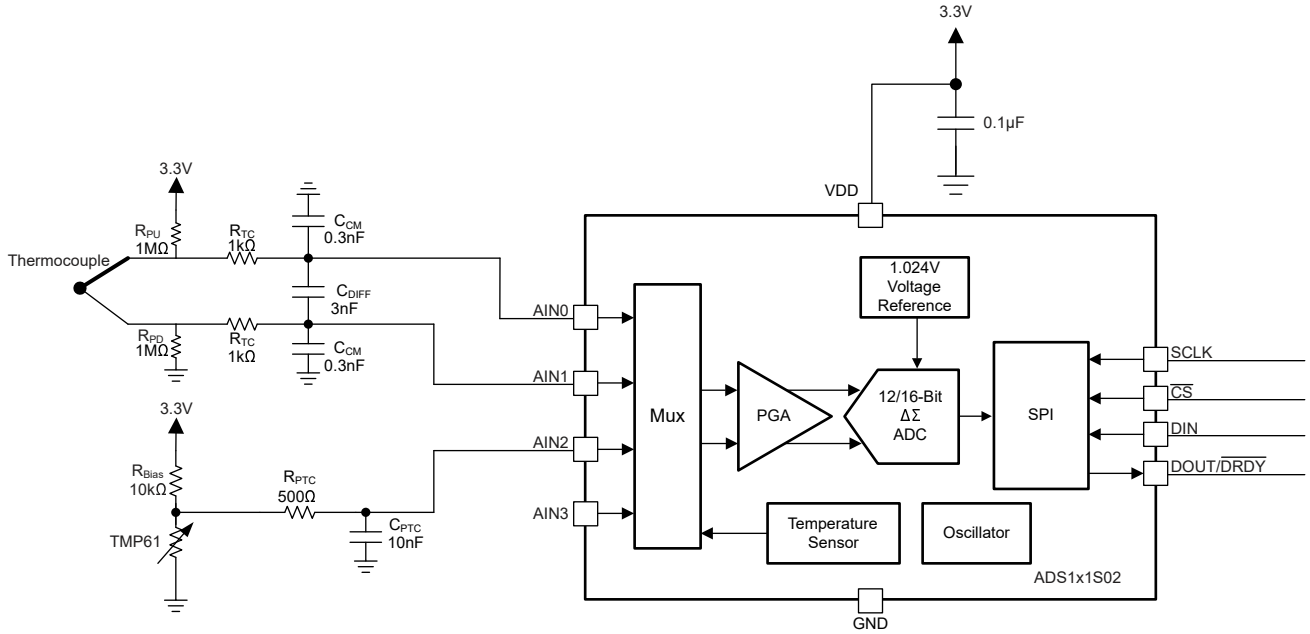


Figure 10-6. K-Type Thermocouple Measurement Using a Thermistor for Cold-Junction Compensation

10.2.1.1 Design Requirements

Table 10-1 lists the design requirements for this application.

Table 10-1. Design Requirements

DESIGN PARAMETER	VALUE
Supply Voltage	3.3V
Thermocouple Type	K
Thermocouple Temperature Measurement Range	–200°C to +1250°C
Thermistor Type	PTC
Thermistor Temperature Measurement Range	–40°C to +125°C
Measurement accuracy at T_A = 25°C(1)	±0.75

(1) Not accounting for error of the thermocouple and cold-junction temperature measurement; offset calibration at $T_{TC} = T_{CJ}$ = 25°C; no gain calibration.

10.2.1.2 Detailed Design Procedure

In this thermocouple measurement example, biasing resistors R_{PU} and R_{PD} set the common-mode voltage of the thermocouple to approximately mid-supply (VDD / 2) to keep the input voltages within the absolute input voltage range of the PGA. These biasing resistors are also useful in detecting an open thermocouple. An open thermocouple lead condition causes R_{PU} and R_{PD} to pull analog inputs AIN0 and AIN1 to VDD and GND respectively. Consequently, the ADC reads a full-scale value outside the normal measurement range, indicating a fault condition. Recommended values for R_{PU} and R_{PD} range from 1MΩ to 50MΩ to minimize self-heating and measurement errors.

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Although the device digital filter attenuates high-frequency noise, further improvement can be achieved by including a first-order passive RC filter at the input. The cutoff frequency of the differential filter (f_C) created by resistors R_{TC} and capacitor C_{DIFF} is calculated using Equation 6.

$$f_C = 1 / [2\pi \times (R_{TC} + R_{TC}) \times C_{DIFF}] \quad (6)$$

Additionally, common-mode capacitors (C_{CM}) provide attenuation of high-frequency common-mode noise. Select values for common-mode capacitors at least 10 times smaller than the differential capacitor to prevent common-mode noise conversion to differential noise.

The filter resistors R_{TC} also serve as current-limiting resistors. These resistors limit the current into analog inputs, AIN0 and AIN1, of the device to safe levels if an overvoltage on the inputs occurs. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs.

The highest resolution is obtained when the largest expected thermocouple voltage is slightly below the full-scale range of the ADC. For example, the maximum thermocouple voltage of a K-type thermocouple at T_{TC} = 1250°C with a cold-junction temperature T_{CJ} = 0°C is approximately 50.644mV, as defined in the tables published by the National Institute of Standards and Technology (NIST). If the cold junction drops below 0°C (minimum specified at –40°C), the output voltage increases. At T_{CJ} = –40°C, the output voltage becomes:

$$V_{TC} = 50.644\text{mV} - (-1.527\text{mV}) = 52.171\text{mV} \quad (7)$$

The maximum gain that can be applied with the 1.024V reference is then calculated as (1.024V / 52.171mV) = 19.6. The next smaller PGA gain setting the device offers is 16.

The device incorporates an internal high-precision temperature sensor to measure the cold junction temperature. Enable the internal temperature sensor by setting bit TS_EN = 1b. Optimal accuracy requires careful board layout to provide efficient thermal coupling between the cold junction and the device package.

The device does not perform automatic cold junction compensation (CJC). Perform CJC within the host controller using the following procedure:

1. Measure the thermocouple voltage, V_{TC}, between AIN0 and AIN1.
2. Measure the cold junction temperature, T_{CJ}, using the internal temperature sensor.
3. Convert T_{CJ} to an equivalent thermocouple voltage (V_{CJ}) using the NIST conversion tables.
4. Compute the total compensated voltage ($V_T = V_{TC} + V_{CJ}$)
5. Convert the compensated voltage (V_T) back to temperature using the NIST tables.

If the internal temperature sensor accuracy is insufficient or the device cannot be placed close enough to the cold junction for good thermal measurement. Use the additional ADC input channels to measure the cold-junction temperature externally using a thermistor or dedicated temperature sensor.

Figure 10-6 shows device uses AIN2 to measure a single-ended thermistor for cold junction compensation. The Texas Instruments TMP61 linear thermistor is selected for the linearity and consistent sensitivity of the device, enabling simple and accurate temperature-to-voltage conversion. A 10kΩ bias resistor is used with the TMP61 to form a voltage divider matched to the TMP61 nominal resistance (10kΩ at 25°C). In this application the thermistor is used for a more precise cold junction temperature measurement compared to the internal temperature sensor of the ADS1x1S02.

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10.2.2 Server Card System Monitoring Application

Figure 10-7 shows an example for a server card monitoring system using the ADS1x1S02. This example shows four single-ended measurements to monitor:

- the power supply,
- a current shunt using an external current shunt amplifier (INA185),
- temperature using an analog output temperature sensor (LMT70A),
- for liquid leaks with a resistive-based leak sensor.

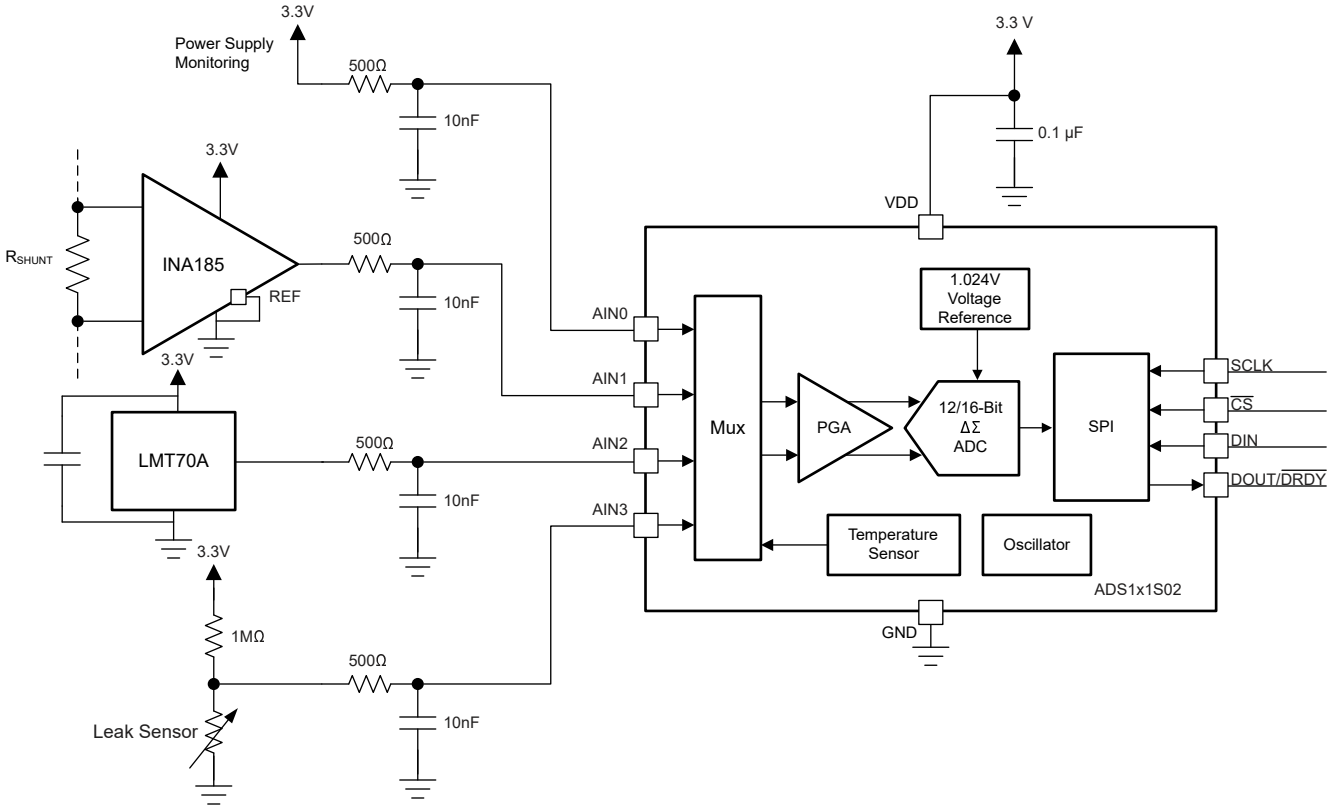


Figure 10-7. Server Card System Monitoring Application

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10.3 Power Supply Recommendations

The device requires a single unipolar supply, VDD, to power both the analog and digital circuitry of the device.

10.3.1 Power-Supply Sequencing

Wait approximately 150µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

10.3.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in Figure 10-8, VDD must be decoupled with at least a 0.1µF capacitor. The 0.1µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the device is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, do not use vias to connect capacitors to the device pins for better noise immunity. Using multiple vias in parallel lowers the overall inductance, and is beneficial for connections to ground planes.

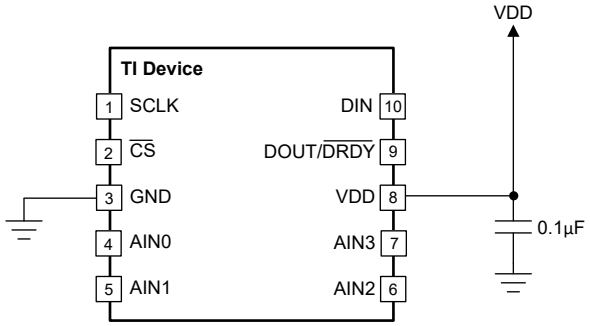


Figure 10-8. ADS1x1S02 Power-Supply Decoupling

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10.4 Layout

10.4.1 Layout Guidelines

The following basic recommendations for the ADS1x1S02 layout help achieve the best possible performance of the ADC.

- For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer.
- Use a ceramic capacitor (for example, X7R grade) for the power-supply decoupling capacitor. High-K capacitors (Y5V) are not recommended. Place the required capacitor as close as possible to the device pin using short, direct traces. Placing the bypass capacitor on the same layer as close to the device yields the best results.
- Use C0G or NP0 capacitors for the RC filters on the analog inputs.
- Route digital traces away from all analog inputs and associated components to minimize interference.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Fill void areas on signal layers with ground fill.

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10.4.2 Layout Example

Figure 10-9 shows a basic layout example for the ADS1x1S02:

- C3 is the power supply decoupling capacitor. Place C3 as close as possible to the supply pin.
- Connect the GND pin to the ground plane.
- Differential antialiasing RC-filters are shown for the differential input pairs AIN0-AIN1 and AIN2-AIN3, respectively.
- Optional series resistors (R5 to R8) are shown for the SPI lines. The series resistors help to reduce overshoot and ringing on the digital lines by smoothing the signal edges.

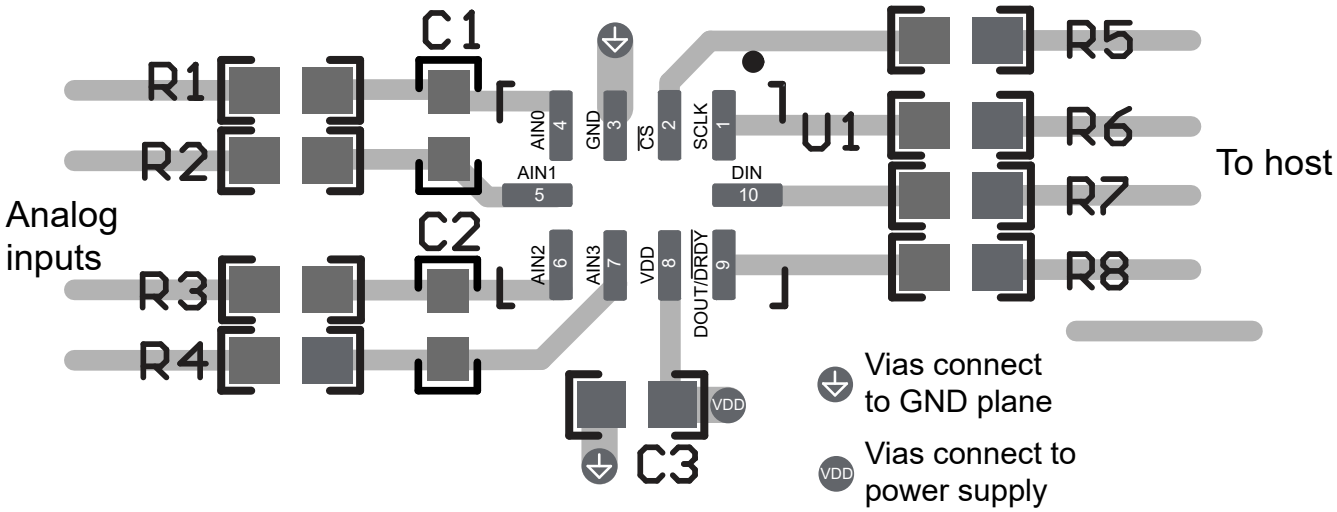


Figure 10-9. ADS1x1S02 X2QFN Package

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP61 ±1% 10kΩ Linear Thermistor With 0402 and 0603 Package Options* datasheet
- Texas Instruments, *LMT70A ±0.05°C Precision Analog Temperature Sensor, RTD and Precision NTC Thermistor IC* datasheet
- Texas Instruments, *INA185 26V, 350kHz, Bidirectional, High-Precision Current Sense Amplifier in UltraSmall (SOT-563) Package* datasheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PADS111S02IRUGR	Active	Preproduction	X2QFN (RUG) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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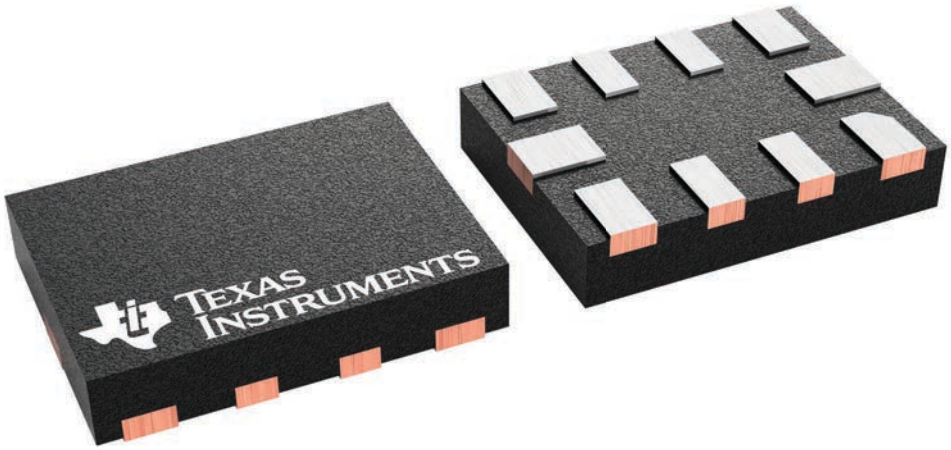
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
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