ADS1x4S1x 16- and 24-Bit, 8- and 18-Channel, 128kSPS, Delta-Sigma ADC With PGA, Voltage Reference, Sequencer, Digital Comparator and SPI

1 Features

- Low power consumption (as low as 64µA)
- Wide supply voltage range:
  - Analog: 1.74V to 3.6V
  - Digital: 1.65V to 5.25V
- Programmable gain: 0.5 to 256
- Programmable data rate (up to 128kSPS) and speed mode to trade power consumption and noise performance
- Simultaneous 50Hz and 60Hz rejection at 20 or 25SPS with single-cycle settling digital filter
- Analog multiplexer with 8 (ADS1x4S14) or 18 (ADS1x4S18) independently selectable inputs
- Dual-matched programmable current sources
- Internal programmable voltage reference: 1.25V or 2.5V with 35ppm/°C (max) drift
- Internal 1% (max) accurate oscillator
- Internal temperature sensor
- Eight general-purpose I/Os (configurable as either push-pull or open-drain outputs)
- Sequencer with 24 individually programmable configurations and digital comparators
- SPI-compatible interface with optional CRC and daisy-chain capability

2 Applications

- Field transmitters: Temperature, pressure, strain, flow
- PLC and DCS analog input modules
- Temperature controllers
- Patient monitoring systems

3 Description

The ADS1x4S1x are precision, low-power, 16- and 24-bit, analog-to-digital converters (ADCs) that offer many integrated features to reduce system cost and component count in the most common sensor measurement applications. The devices feature up to 18 analog inputs through a flexible input multiplexer (MUX), a low-noise, programmable gain amplifier (PGA), a programmable low-drift voltage reference, two programmable excitation current sources, an oscillator, and a temperature sensor.

Four speed modes, with programmable output data rates from 3.9SPS up to 128kSPS, allow to optimize power consumption and noise performance for each application.

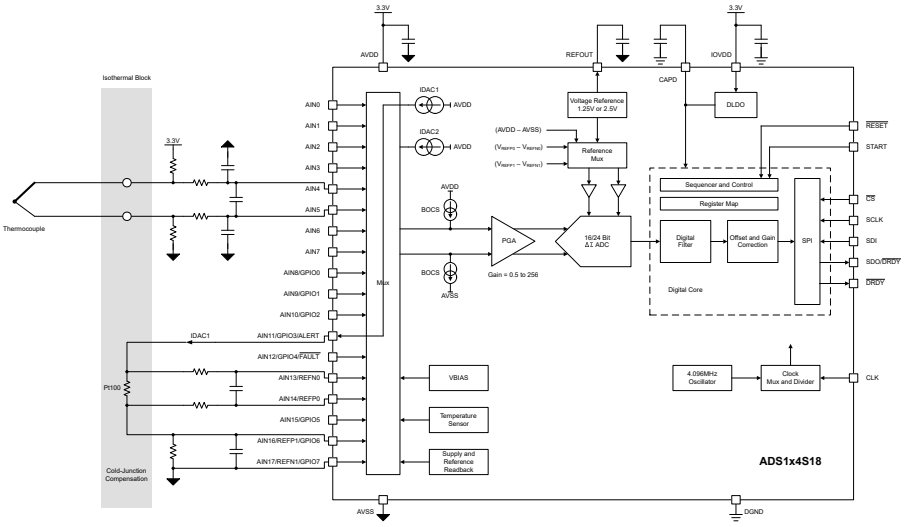
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS1x4S1x	PBS (TQFP, 32)	7.00mm × 7.00mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table 3-1. Device Information

PART NUMBER	RESOLUTION	ANALOG INPUTS
ADS114S14	16 Bit	8
ADS114S18	16 Bit	18
ADS124S14	24 Bit	8
ADS124S18	24 Bit	18



K-Type Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire Pt100 RTD

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4 Pin Configuration and Functions

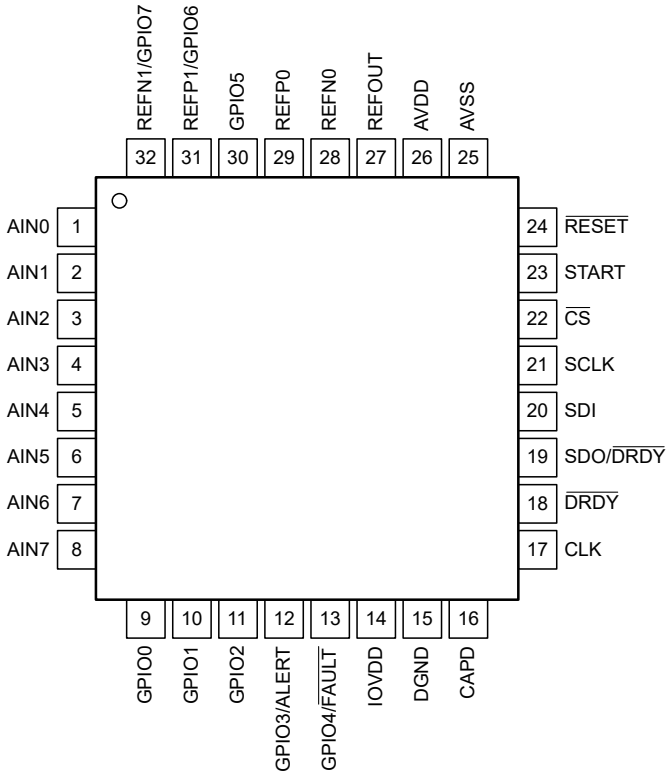


Figure 4-1. ADS1x4S14, PBS Package, 32-pin TQFP, Top View

Table 4-1. ADS1x4S14 Pin Functions

PIN		TYPE	DESCRIPTION[1]
NAME	NO.		
AIN0	1	Analog Input	Analog input 0
AIN1	2	Analog Input	Analog input 1
AIN2	3	Analog Input	Analog input 2
AIN3	4	Analog Input	Analog input 3
AIN4	5	Analog Input	Analog input 4
AIN5	6	Analog Input	Analog input 5
AIN6	7	Analog Input	Analog input 6
AIN7	8	Analog Input	Analog input 7
AVDD	26	Analog Supply	Positive analog supply. Connect a 100nF capacitor to AVSS.
AVSS	25	Analog Supply	Negative analog supply.
CAPD	16	Digital Supply	Internal DLDO output. Connect a 100nF capacitor to DGND.
CLK	17	Digital Input	External clock input[5]
$\overline{CS}$	22	Digital Input	Chip select input. Active low.[5]
DGND	15	Ground	Digital ground
$\overline{DRDY}$	18	Digital Output	Data ready output[3] [5]
GPIO0	9	Digital IO	General purpose digital input/output 0[2] [4]
GPIO1	10	Digital IO	General purpose digital input/output 1[2] [4]
GPIO2	11	Digital IO	General purpose digital input/output 2[2] [4]

Table 4-1. ADS1x4S14 Pin Functions (continued)

PIN		TYPE	DESCRIPTION[1]
NAME	NO.		
GPIO3/ALERT	12	Digital IO	General purpose digital input/output 3.[2] [4] Pin can be configured as dedicated digital comparator ALERT output.
GPIO4/$\overline{\text{FAULT}}$	13	Digital IO	General purpose digital input/output 4.[2] [4] Pin can be configured as dedicated $\overline{\text{FAULT}}$ output.
GPIO5	30	Digital IO	General purpose digital input/output 5[2] [4]
IOVDD	14	Digital Supply	Digital supply. Connect a 100nF capacitor to DGND.
REFN0	28	Analog Input	Negative external reference input 0
REFN1/ GPIO7	32	Analog Input/ Digital IO	Negative external reference input 1. General purpose digital input/output 7.[2] [4]
REFOUT	27	Analog Output	Internal voltage reference output. Connect a 100nF capacitor to AVSS.
REFP0	29	Analog Input	Positive external reference input 0
REFP1/ GPIO6	31	Analog Input/ Digital IO	Positive external reference input 1. General purpose digital input/output 6.[2] [4]
$\overline{\text{RESET}}$	24	Digital Input	Reset input. Active low. Internal 20kΩ pullup resistor to IOVDD.[5]
SCLK	21	Digital Input	Serial data clock input[5]
SDI	20	Digital Input	Serial data input[5]
SDO/$\overline{\text{DRDY}}$	19	Digital Output	Serial data output and data ready indication[3] [5]
START	23	Digital Input	Conversion start control input[5]

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.
(2) Configurable as push-pull or open-drain output.
(3) Push-pull output.
(4) Logic levels referenced to AVDD.
(5) Logic levels referenced to IOVDD.

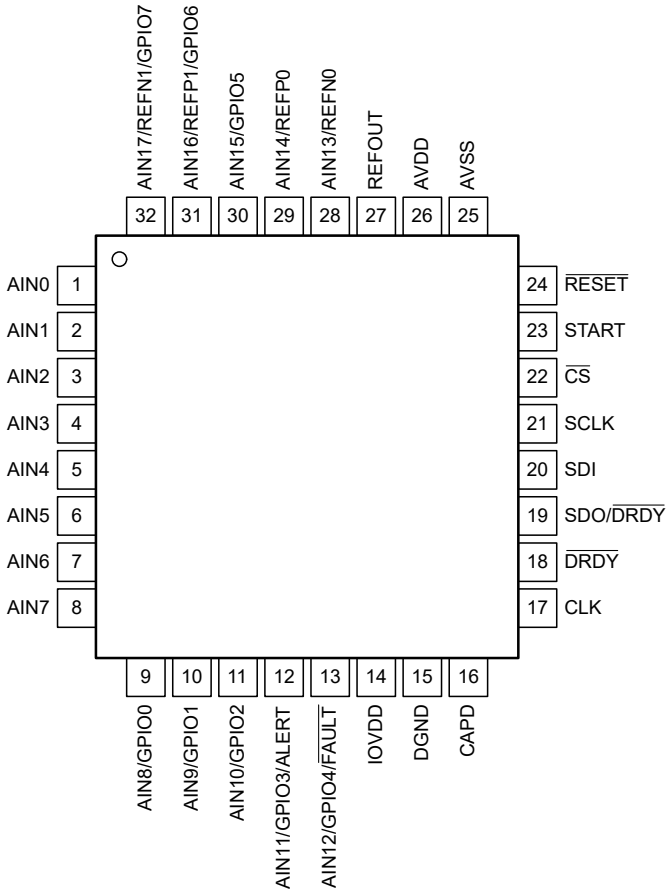


Figure 4-2. ADS1x4S18, PBS Package, 32-pin TQFP, Top View

Table 4-2. ADS1x4S18 Pin Functions

PIN		TYPE	DESCRIPTION[1]
NAME	NO.		
AIN0	1	Analog Input	Analog input 0
AIN1	2	Analog Input	Analog input 1
AIN2	3	Analog Input	Analog input 2
AIN3	4	Analog Input	Analog input 3
AIN4	5	Analog Input	Analog input 4
AIN5	6	Analog Input	Analog input 5
AIN6	7	Analog Input	Analog input 6
AIN7	8	Analog Input	Analog input 7
AIN8/ GPIO0	9	Analog Input/ Digital IO	Analog input 8. General purpose digital input/output 0.[2] [4]
AIN9/ GPIO1	10	Analog Input/ Digital IO	Analog input 9. General purpose digital input/output 1.[2] [4]
AIN10/ GPIO2	11	Analog Input/ Digital IO	Analog input 10. General purpose digital input/output 2.[2] [4]
AIN11/ GPIO3/ALERT	12	Analog Input/ Digital IO	Analog input 11. General purpose digital input/output 3.[2] [4] Pin can be configured as dedicated digital comparator ALERT output.

Table 4-2. ADS1x4S18 Pin Functions (continued)

PIN		TYPE	DESCRIPTION[1]
NAME	NO.		
AIN12/ GPIO4/$\overline{\text{FAULT}}$	13	Analog Input/ Digital IO	Analog input 12. General purpose digital input/output 4.[2] [4] Pin can be configured as dedicated $\overline{\text{FAULT}}$ output.
AIN13/REFN0	28	Analog Input	Analog input 13. Negative external reference input 0.
AIN14/REFP0	29	Analog Input	Analog input 14. Positive external reference input 0.
AIN15/ GPIO5	30	Analog Input/ Digital IO	Analog input 15. General purpose digital input/output 5.[2] [4]
AIN16/REFP1/ GPIO6	31	Analog Input/ Digital IO	Analog input 16. Positive external reference input 1. General purpose digital input/output 6.[2] [4]
AIN17/REFN1/ GPIO7	32	Analog Input/ Digital IO	Analog input 17. Negative external reference input 1. General purpose digital input/output 7.[2] [4]
AVDD	26	Analog Supply	Positive analog supply. Connect a 100nF capacitor to AVSS.
AVSS	25	Analog Supply	Negative analog supply.
CAPD	16	Digital Supply	Internal DLDO output. Connect a 100nF capacitor to DGND.
CLK	17	Digital Input	External clock input[5]
$\overline{\text{CS}}$	22	Digital Input	Chip select input. Active low.[5]
DGND	15	Ground	Digital ground
$\overline{\text{DRDY}}$	18	Digital Output	Data ready output[3] [5]
IOVDD	14	Digital Supply	Digital supply. Connect a 100nF capacitor to DGND.
REFOUT	27	Analog Output	Internal voltage reference output. Connect a 100nF capacitor to AVSS.
$\overline{\text{RESET}}$	24	Digital Input	Reset input. Active low. Internal 20kΩ pullup resistor to IOVDD.[5]
SCLK	21	Digital Input	Serial data clock input[5]
SDI	20	Digital Input	Serial data input[5]
SDO/$\overline{\text{DRDY}}$	19	Digital Output	Serial data output and data ready indication[3] [5]
START	23	Digital Input	Conversion start control input[5]

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.
(2) Configurable as push-pull or open-drain output.
(3) Push-pull output.
(4) Logic levels referenced to AVDD.
(5) Logic levels referenced to IOVDD.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	AVDD to AVSS	–0.3	5	V
	AVSS to DGND	–2.5	0.3	V
	IOVDD to DGND	–0.3	5.5	V
	IOVDD to AVSS		8	V
Analog input voltage	AINx, REFPx, REFNx	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	GPIOx	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, SDI, SDO/$\overline{DRDY}$, $\overline{DRDY}$, $\overline{RESET}$, CLK, START	DGND – 0.3	IOVDD + 0.3	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		140	°C
	Storage, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply (unipolar, AVSS = DGND)	AVDD to AVSS, I_{IDAC} ≤ 500µA	1.74		3.6	V
		AVDD to AVSS, I_{IDAC} > 500µA, or internal V_{REF} = 2.5V	2.7		3.6	
	Analog power supply (bipolar)	AVDD to AVSS, I_{IDAC} ≤ 500µA	1.74		3.6	V
		AVDD to AVSS, I_{IDAC} > 500µA, or internal V_{REF} = 2.5V	2.7		3.6	
		AVDD to DGND	0.85			
		AVSS to DGND	–1.2 × AVDD		0	
	Digital power supply	IOVDD to DGND	1.65		5.25	V
ANALOG INPUTS(1)						
V_{AINx}	Absolute input voltage	Gain = 0.5 to 10	AVSS		AVDD – 0.35	V
		Gain = 16 to 256	AVSS + 0.35		AVDD – 0.4	
V_{IN}	Differential input voltage(2)	Unipolar straight binary coding	0		V_{REF} / Gain	V
		Binary two's complement coding	–V_{REF} / Gain		V_{REF} / Gain	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference input voltage	V_{REF} = (V_{REFPx} – V_{REFNx})	0.5		AVDD	V
V_{REFNx}	Absolute negative reference voltage	Negative reference buffer disabled	AVSS – 0.05			V
		Negative reference buffer enabled	AVSS + 0.1			V
V_{REFPx}	Absolute positive reference voltage	Positive reference buffer disabled			AVDD + 0.05	V
		Positive reference buffer enabled			AVDD – 0.1	V
EXTERNAL CLOCK SOURCE(3)						
f_{CLK}	External clock frequency		3	4.096	4.15	MHz
	Duty Cycle		40	50	60	%
GENERAL-PURPOSE INPUTS (GPIOs)						
	Input voltage		AVSS		AVDD	V
DIGITAL INPUTS (other than GPIOs)						
	Input voltage		DGND		IOVDD	V
TEMPERATURE RANGE						
	Specified ambient temperature		–40		125	°C
T_A	Operating ambient temperature		–50		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. Any of the available analog inputs (AINx) can be selected as either AIN_P or AIN_N by the input multiplexer.
(2) V_{IN} = (V_{AINP} – V_{AINN}). Excluding the effects of offset and gain error.
(3) An external clock is not required when the internal oscillator is used.

5.4 Thermal Information

THERMAL METRIC(1)		TQFP (PBS) 32 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	21.2	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	34.4	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.6	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	34.1	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, $V_{AINx(MIN)} \le V_{AINx} \le V_{AINx(MAX)}$, V_{IN} = 0V	–2	±0.3	2	nA
	Absolute input current drift[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, $V_{AINx(MIN)} \le V_{AINx} \le V_{AINx(MAX)}$, V_{IN} = 0V		2		pA/°C
	Differential input current[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, V_{CM} = (AVDD + AVSS)/2, $–V_{REF}/Gain \le V_{IN} \le V_{REF}/Gain$	–1	±0.1	1	nA
	Differential input current drift[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, V_{CM} = (AVDD + AVSS)/2, $–V_{REF}/Gain \le V_{IN} \le V_{REF}/Gain$		2		pA/°C
PGA						
	Gain settings			0.5, 1, 2, 4, 5, 8, 10, 16, 20, 32, 50, 64, 100, 128, 200, 256		
SYSTEM PERFORMANCE						
	Resolution (no missing codes)	ADS114S1x	16			Bits
		ADS124S1x	24			
f_{DATA}	Output data rate	Speed mode 0 (f_{MOD} = 32kHz)	3.9		4k	SPS
		Speed mode 1 (f_{MOD} = 256kHz)	10		32k	
		Speed mode 2 (f_{MOD} = 512kHz)	10		64k	
		Speed mode 3 (f_{MOD} = 1024kHz)	10		128k	
INL	Integral nonlinearity	V_{CM} = (AVDD + AVSS)/2, best fit		5	15	ppm_{FSR}
V_{IO}	Input offset voltage	T_A = 25°C, gains ≤ 1, global chop disabled	–350	±50	350	µV
		T_A = 25°C, gains = 2 to 10, global chop disabled	–200	±20	200	
		T_A = 25°C, gains ≥ 16, global chop disabled	–50	±10	50	
		T_A = 25°C, gains ≤ 1, global chop enabled	–6	±0.5	6	
		T_A = 25°C, gains ≥ 2, global chop enabled	–2.5	±0.2	2.5	
	Offset drift	Gains ≤ 10, global chop disabled		50	300	nV/°C
		Gains ≥ 16, global chop disabled		20	125	
		Gains ≤ 1, global chop enabled		10	50	
		Gains ≥ 2, global chop enabled		2	20	
	Gain error	T_A = 25°C, all gains, external reference	–0.08	±0.01	0.08	%
	Gain drift	All gains, external reference		0.5	2.5	ppm/°C
	Noise (input-referred)		See the *Noise Performance* section			
CMRR	Common-mode rejection ratio	At dc		120		dB
		f_{CM} = 50Hz or 60Hz (±1Hz), f_{DATA} = 10SPS, 20SPS or 25SPS		130		
		f_{CM} = 50Hz (±1Hz), f_{DATA} = 10SPS, 16.7SPS or 50SPS		130		
		f_{CM} = 60Hz (±1Hz), f_{DATA} = 10SPS or 60SPS		130		
		f_{CM} = 50Hz or 60Hz (±1Hz), f_{DATA} > 60SPS		120		
PSRR	Power-supply rejection ratio	AVDD at dc		115		dB
		IOVDD at dc		120		

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NMRR	Normal-mode rejection ratio	f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 10SPS, sinc3	92	102		dB
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 10SPS, sinc3, external f_{CLK} = 4.096MHz	102			
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 10SPS, sinc4	122	136		
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 10SPS, sinc4, external f_{CLK} = 4.096MHz	136			
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 16.7SPS, sinc3	91	102		
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 16.7SPS, sinc3, external f_{CLK} = 4.096MHz	102			
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 16.7SPS, sinc4	121	135		
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 16.7SPS, sinc4, external f_{CLK} = 4.096MHz	135			
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 20SPS	83	95		
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 20SPS, external f_{CLK} = 4.096MHz	95			
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 25SPS	58	63		
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 25SPS, external f_{CLK} = 4.096MHz	63			
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc3	91	101		
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc3, external f_{CLK} = 4.096MHz	101			
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc4	121	135		
		f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc4, external f_{CLK} = 4.096MHz	135			
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc3	91	103		
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc3, external f_{CLK} = 4.096MHz	103			
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc4	122	137		
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc4, external f_{CLK} = 4.096MHz	137			
VOLTAGE REFERENCE INPUTS						
	Absolute input current	Reference buffer disabled, speed mode 0[2]	–2	±1	2	µA/V
		Reference buffer disabled, speed mode 1[2]	–7	±6	7	
		Reference buffer disabled, speed mode 2[2]	–8	±7	8	
		Reference buffer disabled, speed mode 3[2]	–9	±8	9	
		Reference buffer enabled, speed mode 0	–2	±0.2	2	nA
		Reference buffer enabled, speed mode 1		4	9	
		Reference buffer enabled, speed mode 2		9	17	
		Reference buffer enabled, speed mode 3		17	33	
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Output voltage	(AVDD – AVSS) < 2.7V		1.25		V
		(AVDD – AVSS) ≥ 2.7V		1.25, 2.5		
	Accuracy	T_A = 25°C	–0.1	±0.01	0.1	%
	Temperature drift			14	35	ppm/°C
	Output current	V_{REF} = 1.25V, sink or source	–5		5	mA
		V_{REF} = 2.5V, (AVDD – AVSS) ≥ 2.75V, sink or source	–10		5	
I_{REF_SC}	Short-circuit current limit	Sink or source		±30		mA
PSRR	Power-supply rejection ratio	AVDD at dc		90		dB
	Load regulation	Load current = –5mA to 0mA (source)		75		µV/mA
	Capacitive load stability		50	100	1300	nF
	Reference noise	f = 0.1Hz to 10Hz, 100nF capacitor on REFOUT		4		ppm_{PP}

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start-up time	From power-down mode, 100nF capacitor on REFOUT, 0.01% settling			10	ms
INTERNAL OSCILLATOR						
f_{OSC}	Frequency			4.096		MHz
	Accuracy		–1		1	%
TEMPERATURE SENSOR						
TS_{Offset}	Output voltage	T_A = 25°C		120		mV
TS_{TC}	Temperature coefficient			400		µV/°C
VBIAS						
	Output voltage			(AVDD + AVSS)/2		V
	Capacitive load drive capability	Sum of all capacitors connected to analog inputs where VBIAS is enabled.			10	µF
	Output impedance			200	300	Ω
BURNOUT CURRENT SOURCES (BOCS)						
	Current settings			0.2, 1, 10		µA
	Accuracy	Sink and source		±2		%
EXCITATION CURRENT SOURCES (IDACS)						
	Current settings	IDAC unit current = 1µA		1 to 100		µA
		IDAC unit current = 10µA, (AVDD – AVSS) < 2.7V		10 to 500		
		IDAC unit current = 10µA, (AVDD – AVSS) ≥ 2.7V		10 to 1000		
	Compliance voltage	I_{IDAC} < 100µA, current changes by less than 1% from (AVDD – 1V)	AVSS		AVDD – 0.3	V
		I_{IDAC} ≥ 100µA, current changes by less than 1% from (AVDD – 1V)	AVSS		AVDD – 0.4	
	Accuracy	T_A = 25°C	–3	±0.4	3	%
	Current mismatch between IDACs	I_{IDAC} ≤ 10µA, IDAC1 and IDAC2 set to same value, T_A = 25°C		0.5	1.5	%
		I_{IDAC} ≥ 20µA, IDAC1 and IDAC2 set to same value, T_A = 25°C		0.05	0.3	
	Temperature drift			25	150	ppm/°C
	Temperature drift matching	I_{IDAC} ≤ 10µA, IDAC1 and IDAC2 set to same value		10	50	ppm/°C
		I_{IDAC} ≥ 20µA, IDAC1 and IDAC2 set to same value		1	10	
MONITORS						
TH_{IOVDD_POR}	IOVDD POR release threshold			1.55		V
TH_{AVDD_UV}	AVDD undervoltage threshold(3)		1.2		1.5	V
TH_{REF_UV}	Reference undervoltage threshold(3)	REF_UV_SEL = 0b	0.45		0.65	V
		REF_UV_SEL = 1b	0.9		1.1	
	System monitor voltage readback accuracy	(AVDD – AVSS) / 8		±0.5		%
		(IOVDD – DGND) / 8		±0.5		
		V_{DLDO} / 4		±0.5		
		(V_{REFPx} – V_{REFNx}) / 8		±0.5		

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)						
V_{IL}	Logic input level, low		AVSS		AVSS + 0.3 (AVDD – AVSS)	V
V_{IH}	Logic input level, high		AVSS + 0.7 (AVDD – AVSS)		AVDD	V
V_{OL}	Logic output level, low	I_{OL} = 100µA, open-drain or push-pull output	AVSS		AVSS + 0.2 (AVDD – AVSS)	V
V_{OH}	Logic output level, high	I_{OH} = –100µA, push-pull output	AVSS + 0.8 (AVDD – AVSS)		AVDD	V
	Input hysteresis			10		mV
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.3 IOVDD	V
V_{IH}	Logic input level, high		0.7 IOVDD		IOVDD	V
V_{OL}	Logic output level, low	I_{OL} = 1mA	DGND		0.2 IOVDD	V
V_{OH}	Logic output level, high	I_{OH} = –1mA	0.8 IOVDD		IOVDD	V
	Input hysteresis			180		mV
	Input current	DGND ≤ $V_{Digital\ Input}$ ≤ IOVDD	–1		1	µA

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENTS (AVDD = 3.3V, AVSS = DGND, External Reference, Reference Buffers Disabled, IDACs Disabled, V_{IN} = 0V)						
I_{AVDD}	Analog supply current	Power-down mode		0.7	4	µA
		Standby mode		15	25	
		Conversion mode, speed mode 0, gain = 0.5 to 2		60	68	
		Conversion mode, speed mode 0, gain = 4 and 5		61	71	
		Conversion mode, speed mode 0, gain = 8 to 50		68	78	
		Conversion mode, speed mode 0, gain = 64 to 256		63	73	
		Conversion mode, speed mode 1, gain = 0.5 to 2		155	175	
		Conversion mode, speed mode 1, gain = 4 and 5		180	200	
		Conversion mode, speed mode 1, gain = 8 to 50		225	255	
		Conversion mode, speed mode 1, gain = 64 to 256		280	310	
		Conversion mode, speed mode 2, gain = 0.5 to 2		345	380	
		Conversion mode, speed mode 2, gain = 4 and 5		390	430	
		Conversion mode, speed mode 2, gain = 8 to 50		485	540	
		Conversion mode, speed mode 2, gain = 64 to 256		705	790	
		Conversion mode, speed mode 3, gain = 0.5 to 2		600	655	
		Conversion mode, speed mode 3, gain = 4 and 5		705	780	
		Conversion mode, speed mode 3, gain = 8 to 50		935	1050	
		Conversion mode, speed mode 3, gain = 64 to 256		1155	1300	
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 3.3V, V_{REF} = 2.5V)						
I_{AVDD}	Analog supply current	Internal voltage reference, speed mode 0		4.5	6	µA
		Internal voltage reference, speed mode 1		25	28	
		Internal voltage reference, speed mode 2		35	40	
		Internal voltage reference, speed mode 3		65	75	
		Either REFP or REFN buffer enabled, speed mode 0		4.5	6	
		Either REFP or REFN buffer enabled, speed mode 1		25	28	
		Either REFP or REFN buffer enabled, speed mode 2		35	40	
		Either REFP or REFN buffer enabled, speed mode 3		65	75	
		Both REFP and REFN buffers enabled, speed mode 0		6.5	9	
		Both REFP and REFN buffers enabled, speed mode 1		32	40	
		Both REFP and REFN buffers enabled, speed mode 2		50	60	
		Both REFP and REFN buffers enabled, speed mode 3		102	120	
		IDAC overhead, IDAC unit current = 1µA		4	6	
		IDAC overhead, IDAC unit current = 10µA		14	20	
		VBIAS (no load)		11	18	

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENTS (AVDD = 1.8V, AVSS = DGND, External Reference, Reference Buffers Disabled, IDACs Disabled, V_{IN} = 0V)						
I_{AVDD}	Analog supply current	Power-down mode		0.5	4	µA
		Standby mode		12	22	
		Conversion mode, speed mode 0, gain = 0.5 to 2		55	63	
		Conversion mode, speed mode 0, gain = 4 and 5		57	66	
		Conversion mode, speed mode 0, gain = 8 to 50		63	73	
		Conversion mode, speed mode 0, gain = 64 to 256		59	68	
		Conversion mode, speed mode 1, gain = 0.5 to 2		140	170	
		Conversion mode, speed mode 1, gain = 4 and 5		160	190	
		Conversion mode, speed mode 1, gain = 8 to 50		205	235	
		Conversion mode, speed mode 1, gain = 64 to 256		255	290	
		Conversion mode, speed mode 2, gain = 0.5 to 2		310	345	
		Conversion mode, speed mode 2, gain = 4 and 5		355	395	
		Conversion mode, speed mode 2, gain = 8 to 50		450	505	
		Conversion mode, speed mode 2, gain = 64 to 256		660	750	
		Conversion mode, speed mode 3, gain = 0.5 to 2		540	595	
		Conversion mode, speed mode 3, gain = 4 and 5		640	720	
		Conversion mode, speed mode 3, gain = 8 to 50		870	985	
		Conversion mode, speed mode 3, gain = 64 to 256		1080	1220	
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 1.8V, V_{REF} = 1.25V)						
I_{AVDD}	Analog supply current	Internal voltage reference, speed mode 0		3.5	5	µA
		Internal voltage reference, speed mode 1		16	20	
		Internal voltage reference, speed mode 2		26	32	
		Internal voltage reference, speed mode 3		55	70	
		Either REFP or REFN buffer enabled, speed mode 0		3.5	5	
		Either REFP or REFN buffer enabled, speed mode 1		16	20	
		Either REFP or REFN buffer enabled, speed mode 2		26	32	
		Either REFP or REFN buffer enabled, speed mode 3		55	70	
		Both REFP and REFN buffers enabled, speed mode 0		5.5	8	
		Both REFP and REFN buffers enabled, speed mode 1		25	30	
		Both REFP and REFN buffers enabled, speed mode 2		42	52	
		Both REFP and REFN buffers enabled, speed mode 3		100	120	
		IDAC overhead, IDAC unit current = 1µA		4	6	
		IDAC overhead, IDAC unit current = 10µA		14	20	
		VBIAS (no load)		11	18	

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, IOVDD = 1.65V to 5.25V, AVSS = DGND, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL SUPPLY CURRENTS (IOVDD = 3.3V, All Data Rates, SPI Not Active)						
I_{IOVDD}	Digital supply current	Power-down mode		2.2	20	µA
		Standby mode, speed mode 0		8	26	
		Standby mode, speed mode 1		22	40	
		Standby mode, speed mode 2		32	50	
		Standby mode, speed mode 3		50	70	
		Conversion mode, speed mode 0 (OSR = 8)		11	30	
		Conversion mode, speed mode 1 (OSR = 8)		42	64	
		Conversion mode, speed mode 2 (OSR = 8)		72	100	
		Conversion mode, speed mode 3 (OSR = 8)		129	163	
		Conversion mode, speed mode 0 (OSR ≥ 64)		10	27	
		Conversion mode, speed mode 1 (OSR ≥ 64)		34	53	
		Conversion mode, speed mode 2 (OSR ≥ 64)		54	75	
		Conversion mode, speed mode 3 (OSR ≥ 64)		97	120	
DIGITAL SUPPLY CURRENTS (IOVDD = 1.8V, All Data Rates, SPI Not Active)						
I_{IOVDD}	Digital supply current	Power-down mode		2	19	µA
		Standby mode, speed mode 0		8	25	
		Standby mode, speed mode 1		22	40	
		Standby mode, speed mode 2		30	50	
		Standby mode, speed mode 3		48	66	
		Conversion mode, speed mode 0 (OSR = 8)		11	28	
		Conversion mode, speed mode 1 (OSR = 8)		41	63	
		Conversion mode, speed mode 2 (OSR = 8)		70	95	
		Conversion mode, speed mode 3 (OSR = 8)		127	160	
		Conversion mode, speed mode 0 (OSR ≥ 64)		9	27	
		Conversion mode, speed mode 1 (OSR ≥ 64)		33	52	
		Conversion mode, speed mode 2 (OSR ≥ 64)		53	74	
		Conversion mode, speed mode 3 (OSR ≥ 64)		94	120	

(1) Input currents scale with speed mode, data rate, gain, and global-chop mode settings.
(2) Current is flowing into REFPx and out of REFNx.
(3) Undervoltage monitor always trips below the specified MIN value and never trips above the specified MAX value.

5.6 Timing Requirements

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$t_{c(SC)}$	SCLK period	60	1/(4 f_{DATA})	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	30		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	30		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	8		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	8		ns
$t_{d(fr2fr)}$	Delay time, between frames in 3-wire SPI mode	0		ns
$t_{h(DIIR)}$	Hold time, SDI high to force interface resynchronization (3-wire SPI mode only). Interface resynchronization happens on first SCLK falling edge where SDI is low again.	63		t_{SCLK}
$t_{d(POR)}$	Delay time, first SCLK rising edge after IOVDD exceeds minimum IOVDD voltage	5		ms
$t_{d(RST)}$	Delay time, SPI communication start after $\overline{RESET}$ rising edge or after software reset using SPI reset pattern or RESET[7:0] bit field	500		µs
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low to generate device reset	200		ns
$t_{w(STH)}$	Pulse duration, START high to start conversions	8		t_{MOD}

5.7 Switching Characteristics

over operating ambient temperature range, C_{LOAD} = 20pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven				25	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				25	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				28	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{MOD}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge of conversion result MSB readout to $\overline{DRDY}$ return high				5	t_{MOD}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b			50	ns
$t_{p(GPIO)}$	Propagation delay time, $\overline{CS}$ rising edge of register write command to GPIOx output valid				100	ns

5.8 Timing Diagrams

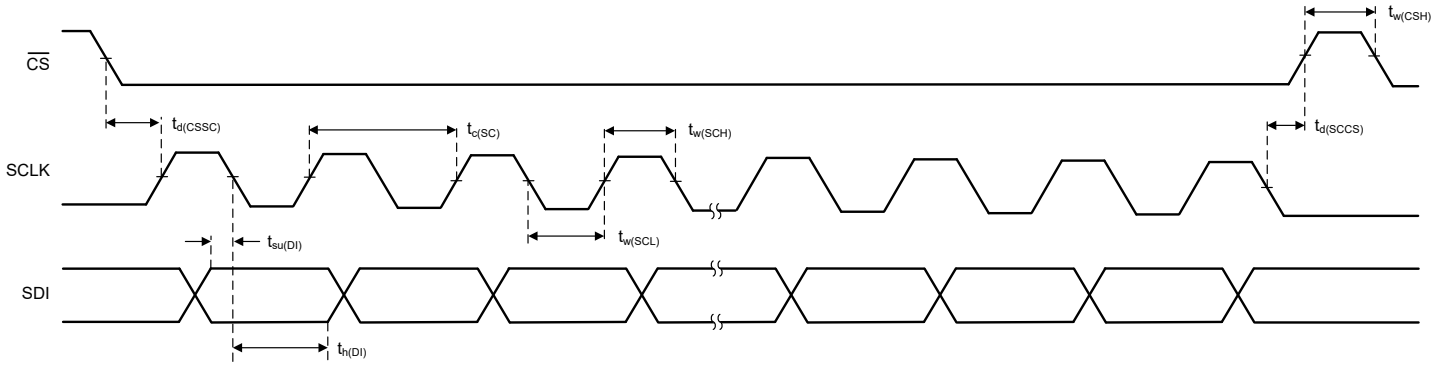


Figure 5-1. Serial Interface Timing Requirements

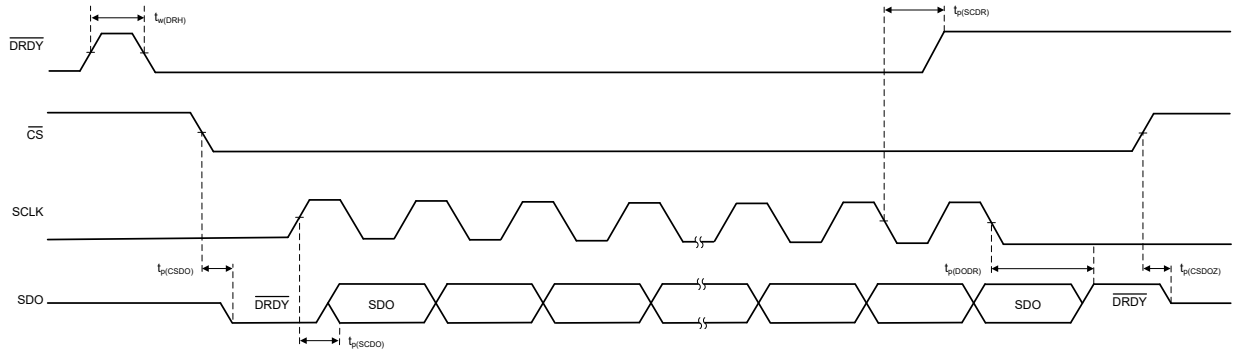


Figure 5-2. Serial Interface Switching Characteristics

5.9 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

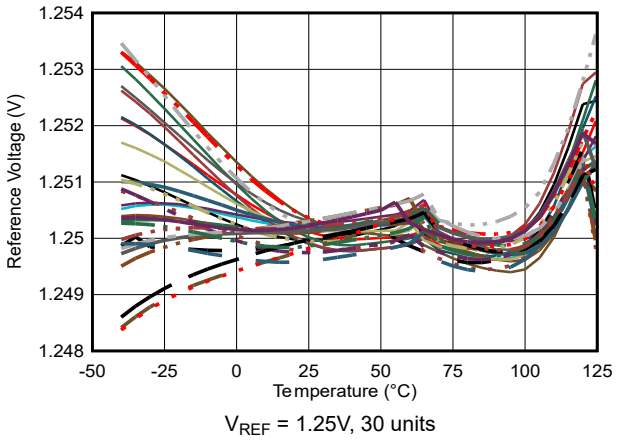


Figure 5-3. Internal Reference Voltage vs Temperature

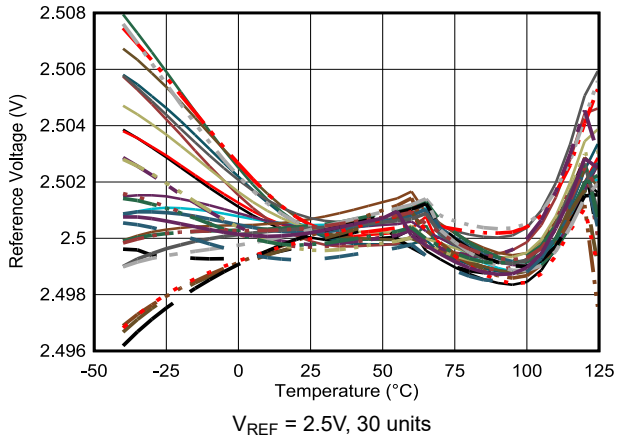


Figure 5-4. Internal Reference Voltage vs Temperature

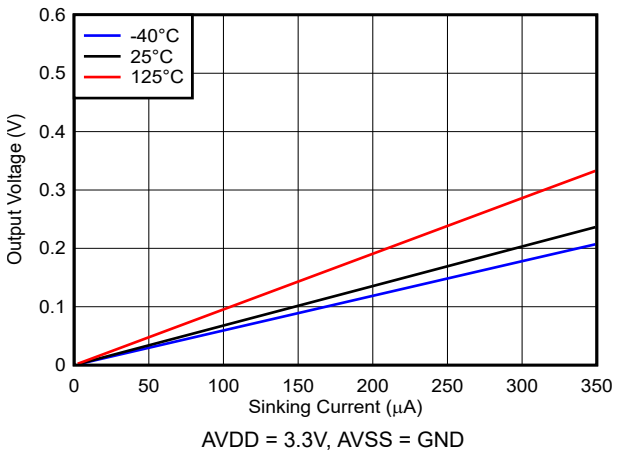


Figure 5-5. GPIO Pin Output Voltage vs Sinking Current

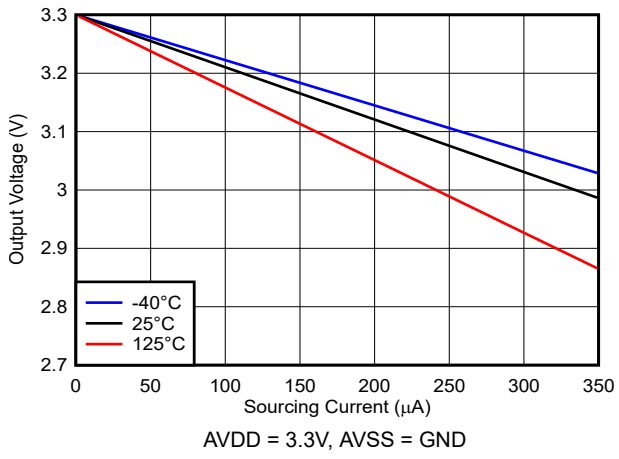


Figure 5-6. GPIO Pin Output Voltage vs Sourcing Current

6 Parameter Measurement Information

6.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called the oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 6-1 to Table 6-8 summarize the typical device noise performance at T_A = 25°C using f_{CLK} = 4.096MHz. The data shown are typical input-referred noise results (e_n) in units of μV_{RMS} with the analog inputs shorted together. A minimum of 1,000 consecutive conversions or 10 seconds of consecutive conversions (whichever occurs first) are used to measure RMS noise. Because of the statistical nature of noise, repeated noise measurements can yield higher or lower noise results.

Use Equation 1 or Equation 2 to calculate effective resolution from the provided μV_{RMS} numbers, depending on the selected coding scheme.

$$\text{Binary two's complement coding: Effective Resolution} = \ln[(2 \times V_{REF} / \text{Gain}) / e_{n(RMS)}] / \ln(2) \quad (1)$$

$$\text{Unipolar straight binary coding: Effective Resolution} = \ln[(V_{REF} / \text{Gain}) / e_{n(RMS)}] / \ln(2) \quad (2)$$

Input-referred noise (e_n) in units of μV_{PP} can be estimated as $e_{n(PP)} = 6.6 \times e_{n(RMS)}$. Use Equation 3 or Equation 4 to calculate noise-free resolution from the estimated μV_{PP} numbers, depending on the selected coding scheme.

$$\text{Binary two's complement coding: Noise-free Resolution} = \ln[(2 \times V_{REF} / \text{Gain}) / e_{n(PP)}] / \ln(2) \quad (3)$$

$$\text{Unipolar straight binary coding: Noise-free Resolution} = \ln[(V_{REF} / \text{Gain}) / e_{n(PP)}] / \ln(2) \quad (4)$$

Input-referred noise performance using shorted inputs does only change insignificantly with the reference voltage. That is, Table 6-1 to Table 6-8 also apply to other reference voltage values.

In global-chop mode, the device averages two measurement of the ADC with the inputs swapped. Global-chop mode significantly reduces the input offset of the device, and reduces noise by a factor of $\sqrt{2}$.

Noise data is measured using the 24-bit version of the device. For the 16-bit device, clip the noise data at the LSB size.

Table 6-1. Input-referred Noise in μV_{RMS}, Speed Mode 0 (f_{MOD} = 32kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	4000	333.94	168.20	85.70	42.75	43.27	22.06	22.15	11.12
16	2000	51.64	25.75	14.02	8.32	8.36	5.81	5.82	3.29
24	1333	36.41	18.51	10.27	6.43	6.45	4.64	4.64	2.67
32	1000	31.69	15.40	8.88	5.61	5.61	4.14	4.12	2.37
64	500	22.05	11.26	6.25	3.91	3.92	2.84	2.86	1.65
128	250	15.47	7.91	4.38	2.85	2.79	2.00	2.05	1.13
256	125	11.00	5.50	3.02	1.95	2.02	1.47	1.44	0.84
512	62.5	8.05	3.95	2.23	1.32	1.39	0.99	0.99	0.59
640	50	6.85	3.42	2.11	1.24	1.24	0.89	0.93	0.51
1024	31.25	5.61	2.81	1.56	1.01	0.98	0.69	0.68	0.43
2048	15.63	3.84	1.91	1.14	0.64	0.69	0.48	0.55	0.29
4096	7.81	2.95	1.28	0.78	0.60	0.46	0.37	0.29	0.23
8192	3.91	4.18	1.06	0.57	0.29	2.48	3.90	0.25	0.13
532	60	7.65	3.80	2.21	1.40	1.37	1.02	1.06	0.58
640	50	7.04	3.58	2.01	1.19	1.24	0.88	0.92	0.52
1920	16.7	4.22	2.22	1.07	0.69	0.69	0.51	0.51	0.29
3200	10	3.43	1.61	0.81	0.48	0.64	0.44	0.44	0.24
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	4000	497.79	249.35	125.99	63.17	63.89	32.16	32.38	16.41
16	2000	78.04	39.07	20.21	11.14	11.37	7.21	7.13	3.96
24	1333	42.42	21.42	11.76	7.17	7.32	5.18	5.15	2.90
32	1000	34.09	17.61	9.71	6.03	6.06	4.35	4.47	2.55
64	500	23.85	11.73	6.74	4.18	4.19	3.14	3.10	1.77
128	250	17.00	8.56	4.69	2.99	3.03	2.15	2.21	1.24
256	125	11.81	6.20	3.27	2.17	2.09	1.59	1.57	0.86
512	62.5	7.85	3.98	2.29	1.53	1.48	1.10	1.17	0.63
640	50	7.63	3.81	2.11	1.34	1.35	0.96	0.96	0.56
1024	31.25	6.11	2.92	1.55	1.07	1.06	0.77	0.83	0.48
2048	15.63	4.25	2.27	1.19	0.75	0.74	0.45	0.50	0.33
4096	7.81	2.96	1.48	0.70	0.54	0.45	0.39	0.43	0.26
8192	3.91	4.60	3.63	3.59	0.37	0.35	0.29	0.27	0.18
532	60	7.96	4.02	2.42	1.44	1.41	1.10	1.04	0.61
640	50	7.13	3.79	2.02	1.31	1.26	1.01	1.04	0.53
1920	16.7	4.18	2.18	1.29	0.82	0.78	0.64	0.54	0.33
3200	10	3.42	1.60	0.89	0.61	0.66	0.43	0.46	0.27

Table 6-1. Input-referred Noise in μV_{RMS}, Speed Mode 0 (f_{MOD} = 32kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	500	27.08	13.51	7.64	4.79	4.79	3.62	3.49	2.03
128	250	20.09	10.39	5.81	3.75	3.73	2.76	2.76	1.57
256	125	15.30	7.43	4.16	2.78	2.73	2.09	2.08	1.14
512	62.5	11.19	5.38	3.08	2.01	1.98	1.43	1.40	0.83
640	50	9.83	5.09	3.02	1.70	1.73	1.31	1.33	0.70
1024	31.25	8.48	4.07	2.47	1.51	1.47	1.06	1.04	0.60
2048	15.63	6.13	2.94	1.55	0.90	1.10	0.81	0.69	0.41
4096	7.81	4.19	2.26	1.11	0.58	0.62	0.52	0.55	0.34
8192	3.91	3.31	1.42	0.65	0.57	0.44	0.29	0.32	0.19
532	60	10.74	5.67	3.12	1.93	1.91	1.35	1.46	0.84
640	50	9.62	5.14	2.80	1.83	1.87	1.32	1.26	0.72
1920	16.7	5.28	3.22	1.70	1.05	1.00	0.79	0.80	0.42
3200	10	4.34	2.05	1.18	0.73	0.77	0.60	0.61	0.30
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
1280	25	8.45	4.06	2.46	1.31	1.44	1.09	1.09	0.64
1600	20	8.39	3.87	2.10	1.31	1.27	0.98	0.98	0.52

(1) Using f_{CLK} = 4.096MHz

Table 6-2. Input-referred Noise in μV_{RMS}, Speed Mode 0 (f_{MOD} = 32kHz), at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	4000	11.32	6.11	6.11	3.68	3.61	2.56	2.57	2.17
16	2000	3.30	2.39	2.35	1.84	1.87	1.62	1.60	1.54
24	1333	2.64	1.93	1.91	1.53	1.56	1.36	1.37	1.28
32	1000	2.33	1.71	1.71	1.37	1.37	1.21	1.22	1.14
64	500	1.65	1.19	1.21	0.97	0.96	0.87	0.86	0.84
128	250	1.21	0.84	0.85	0.68	0.67	0.60	0.60	0.57
256	125	0.83	0.61	0.59	0.49	0.50	0.42	0.43	0.40
512	62.5	0.58	0.43	0.42	0.34	0.35	0.30	0.31	0.27
640	50	0.52	0.36	0.38	0.29	0.31	0.26	0.27	0.28
1024	31.25	0.42	0.28	0.29	0.24	0.22	0.22	0.21	0.20
2048	15.63	0.29	0.21	0.21	0.15	0.16	0.14	0.16	0.14
4096	7.81	0.20	0.15	0.11	0.13	0.12	0.11	0.11	0.10
8192	3.91	0.16	0.09	0.10	0.60	0.60	0.51	0.50	0.06
532	60	0.59	0.41	0.43	0.33	0.34	0.31	0.30	0.28
640	50	0.51	0.37	0.38	0.28	0.32	0.26	0.27	0.25
1920	16.7	0.28	0.21	0.21	0.17	0.19	0.16	0.17	0.15
3200	10	0.24	0.15	0.18	0.13	0.14	0.12	0.12	0.12
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	4000	16.15	8.57	8.61	4.78	4.79	3.09	3.12	2.46
16	2000	3.93	2.62	2.66	2.06	2.01	1.72	1.74	1.65
24	1333	2.88	2.10	2.08	1.69	1.67	1.45	1.45	1.38
32	1000	2.54	1.83	1.83	1.48	1.48	1.29	1.32	1.24
64	500	1.74	1.30	1.28	1.04	1.04	0.92	0.92	0.86
128	250	1.24	0.90	0.90	0.73	0.69	0.66	0.67	0.61
256	125	0.88	0.64	0.63	0.52	0.53	0.48	0.46	0.43
512	62.5	0.63	0.44	0.45	0.35	0.36	0.31	0.32	0.30
640	50	0.55	0.39	0.41	0.33	0.33	0.29	0.28	0.28
1024	31.25	0.45	0.36	0.34	0.26	0.23	0.22	0.23	0.23
2048	15.63	0.29	0.23	0.23	0.17	0.16	0.17	0.16	0.15
4096	7.81	0.22	0.17	0.14	0.14	0.14	0.12	0.13	0.08
8192	3.91	0.14	0.74	0.12	0.61	0.11	0.09	0.09	0.09
532	60	0.62	0.42	0.46	0.35	0.36	0.32	0.32	0.30
640	50	0.56	0.41	0.39	0.33	0.36	0.28	0.30	0.26
1920	16.7	0.31	0.23	0.23	0.19	0.19	0.18	0.17	0.15
3200	10	0.25	0.15	0.17	0.16	0.14	0.12	0.12	0.13

Table 6-2. Input-referred Noise in μV_{RMS}, Speed Mode 0 (f_{MOD} = 32kHz), at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	500	2.03	1.47	1.44	1.17	1.18	1.05	1.04	1.01
128	250	1.59	1.12	1.13	0.92	0.89	0.81	0.81	0.80
256	125	1.18	0.83	0.82	0.70	0.69	0.57	0.60	0.55
512	62.5	0.83	0.62	0.59	0.47	0.48	0.42	0.45	0.41
640	50	0.76	0.53	0.53	0.44	0.44	0.38	0.38	0.36
1024	31.25	0.58	0.41	0.43	0.34	0.37	0.31	0.32	0.27
2048	15.63	0.43	0.30	0.31	0.26	0.24	0.21	0.23	0.20
4096	7.81	0.31	0.21	0.22	0.16	0.19	0.16	0.16	0.14
8192	3.91	0.17	0.17	0.16	0.14	0.12	0.10	0.10	0.13
532	60	0.82	0.57	0.56	0.47	0.46	0.41	0.41	0.40
640	50	0.70	0.54	0.55	0.43	0.41	0.40	0.40	0.38
1920	16.7	0.42	0.31	0.34	0.24	0.26	0.22	0.24	0.22
3200	10	0.35	0.22	0.26	0.17	0.19	0.19	0.16	0.18
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
1280	25	0.65	0.43	0.47	0.37	0.37	0.36	0.33	0.31
1600	20	0.53	0.41	0.44	0.36	0.36	0.32	0.30	0.26

(1) Using f_{CLK} = 4.096MHz

Table 6-3. Input-referred Noise in μV_{RMS}, Speed Mode 1 (f_{MOD} = 256kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	32000	333.78	168.00	82.88	43.99	43.67	24.14	24.07	12.74
16	16000	50.84	26.10	14.89	10.02	9.97	8.36	8.38	5.09
24	10667	35.72	18.45	10.84	7.68	7.78	6.80	6.67	4.03
32	8000	29.85	15.90	9.36	6.75	6.78	5.85	5.84	3.56
64	4000	21.52	11.14	6.51	4.78	4.71	4.13	4.09	2.57
128	2000	15.22	7.83	4.63	3.35	3.33	2.92	2.92	1.79
256	1000	10.57	5.53	3.31	2.38	2.36	2.09	2.06	1.26
512	500	7.35	3.96	2.32	1.65	1.68	1.44	1.47	0.91
640	400	6.83	3.47	2.08	1.47	1.48	1.28	1.31	0.81
1024	250	5.42	2.78	1.59	1.15	1.18	1.02	1.04	0.63
2048	125	3.82	1.97	1.16	0.84	0.83	0.76	0.74	0.45
4096	62.5	2.86	1.38	0.87	0.59	0.61	0.56	0.53	0.33
8192	31.25	2.11	0.94	0.58	0.37	0.44	0.36	0.37	0.21
4256	60	2.44	1.41	0.80	0.58	0.60	0.51	0.51	0.30
5120	50	2.28	1.23	0.76	0.51	0.55	0.48	0.50	0.29
15360	16.7	1.38	0.70	0.44	0.32	0.30	0.26	0.25	0.16
25600	10	1.04	0.54	0.31	0.24	0.24	0.19	0.23	0.13
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	32000	498.66	248.93	125.39	63.67	63.33	33.37	33.24	17.04
16	16000	78.11	39.13	20.97	12.81	12.65	9.62	9.61	5.75
24	10667	41.84	21.61	12.42	8.46	8.46	7.35	7.34	4.46
32	8000	33.79	17.18	10.11	7.08	7.15	6.26	6.19	3.87
64	4000	22.81	11.79	7.22	5.12	5.08	4.43	4.53	2.73
128	2000	16.25	8.27	5.03	3.54	3.58	3.11	3.12	1.94
256	1000	11.33	5.90	3.54	2.52	2.51	2.22	2.22	1.37
512	500	7.95	4.24	2.49	1.77	1.80	1.54	1.56	0.98
640	400	7.28	3.76	2.25	1.62	1.58	1.43	1.41	0.87
1024	250	5.79	2.92	1.73	1.26	1.23	1.13	1.13	0.68
2048	125	4.15	2.08	1.26	0.90	0.93	0.77	0.76	0.49
4096	62.5	2.91	1.46	0.86	0.62	0.64	0.56	0.54	0.32
8192	31.25	1.92	0.93	0.64	0.46	0.41	0.37	0.42	0.24
4256	60	2.86	1.58	0.84	0.61	0.61	0.53	0.52	0.34
5120	50	2.56	1.35	0.77	0.56	0.59	0.51	0.52	0.32
15360	16.7	1.44	0.76	0.46	0.33	0.30	0.30	0.28	0.17
25600	10	0.92	0.56	0.38	0.27	0.31	0.26	0.23	0.13

Table 6-3. Input-referred Noise in μV_{RMS}, Speed Mode 1 (f_{MOD} = 256kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	4000	25.90	13.66	8.14	5.75	5.72	5.04	5.02	3.12
128	2000	20.21	10.37	6.33	4.49	4.45	3.91	3.90	2.41
256	1000	14.89	7.72	4.55	3.30	3.29	2.89	2.88	1.79
512	500	10.69	5.54	3.36	2.31	2.34	2.08	2.08	1.28
640	400	9.69	4.90	2.98	2.13	2.11	1.87	1.87	1.16
1024	250	7.84	3.92	2.39	1.70	1.72	1.48	1.45	0.92
2048	125	5.52	2.86	1.68	1.18	1.20	1.05	1.06	0.64
4096	62.5	3.73	2.07	1.19	0.83	0.90	0.77	0.75	0.44
8192	31.25	2.82	1.41	0.83	0.55	0.60	0.55	0.56	0.34
4256	60	3.92	2.03	1.26	0.78	0.83	0.77	0.76	0.45
5120	50	3.47	1.61	1.06	0.80	0.81	0.66	0.64	0.42
15360	16.7	2.10	0.99	0.66	0.45	0.41	0.36	0.36	0.24
25600	10	1.53	0.87	0.51	0.29	0.37	0.30	0.29	0.19
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
10240	25	2.71	1.54	0.82	0.66	0.63	0.56	0.54	0.31
12800	20	2.56	1.33	0.80	0.54	0.54	0.52	0.48	0.30

(1) Using f_{CLK} = 4.096MHz

Table 6-4. Input-referred Noise in μV_{RMS}, Speed Mode 1 (f_{MOD} = 256kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	32000	12.65	8.18	8.11	4.10	4.04	3.03	3.05	2.65
16	16000	5.14	4.48	4.43	2.21	2.22	2.01	2.00	1.87
24	10667	4.11	3.67	3.65	1.84	1.85	1.64	1.63	1.56
32	8000	3.61	3.18	3.16	1.61	1.62	1.44	1.46	1.35
64	4000	2.55	2.27	2.28	1.16	1.17	1.04	1.05	1.00
128	2000	1.80	1.61	1.61	0.83	0.81	0.75	0.74	0.70
256	1000	1.27	1.14	1.13	0.58	0.58	0.53	0.54	0.49
512	500	0.89	0.80	0.79	0.41	0.41	0.37	0.37	0.35
640	400	0.80	0.72	0.73	0.37	0.36	0.34	0.33	0.31
1024	250	0.64	0.57	0.57	0.28	0.29	0.27	0.27	0.26
2048	125	0.46	0.39	0.39	0.21	0.20	0.19	0.18	0.17
4096	62.5	0.33	0.26	0.27	0.15	0.15	0.14	0.13	0.12
8192	31.25	0.24	0.18	0.18	0.10	0.10	0.09	0.09	0.10
4256	60	0.33	0.28	0.28	0.14	0.14	0.12	0.13	0.12
5120	50	0.27	0.27	0.24	0.13	0.13	0.12	0.12	0.11
15360	16.7	0.17	0.15	0.15	0.08	0.08	0.07	0.07	0.07
25600	10	0.13	0.10	0.11	0.06	0.06	0.06	0.05	0.05
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	32000	17.24	10.27	10.10	5.14	5.14	3.52	3.56	2.89
16	16000	5.73	4.90	4.85	2.45	2.39	2.12	2.16	2.00
24	10667	4.49	3.94	3.98	1.97	1.97	1.75	1.78	1.65
32	8000	3.82	3.41	3.38	1.70	1.72	1.55	1.55	1.45
64	4000	2.78	2.44	2.45	1.25	1.26	1.14	1.16	1.08
128	2000	1.94	1.71	1.72	0.89	0.88	0.80	0.79	0.75
256	1000	1.36	1.22	1.22	0.64	0.62	0.57	0.56	0.54
512	500	0.95	0.87	0.88	0.43	0.44	0.40	0.40	0.38
640	400	0.88	0.75	0.77	0.39	0.40	0.37	0.36	0.34
1024	250	0.69	0.59	0.60	0.31	0.31	0.29	0.28	0.27
2048	125	0.47	0.43	0.43	0.23	0.22	0.20	0.20	0.19
4096	62.5	0.35	0.31	0.30	0.15	0.15	0.15	0.14	0.14
8192	31.25	0.26	0.21	0.21	0.11	0.11	0.11	0.10	0.09
4256	60	0.33	0.29	0.30	0.15	0.16	0.14	0.13	0.12
5120	50	0.30	0.28	0.27	0.14	0.15	0.13	0.13	0.12
15360	16.7	0.17	0.16	0.16	0.07	0.07	0.08	0.08	0.07
25600	10	0.13	0.10	0.11	0.06	0.06	0.06	0.05	0.05

Table 6-4. Input-referred Noise in μV_{RMS}, Speed Mode 1 (f_{MOD} = 256kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	4000	3.13	2.75	2.77	1.43	1.42	1.29	1.30	1.23
128	2000	2.42	2.14	2.15	1.09	1.10	1.00	1.00	0.94
256	1000	1.77	1.59	1.58	0.80	0.81	0.73	0.73	0.69
512	500	1.27	1.12	1.11	0.58	0.57	0.53	0.52	0.51
640	400	1.15	1.02	1.03	0.52	0.52	0.48	0.48	0.45
1024	250	0.92	0.81	0.80	0.41	0.42	0.38	0.38	0.36
2048	125	0.64	0.55	0.59	0.30	0.29	0.27	0.28	0.25
4096	62.5	0.46	0.42	0.42	0.21	0.21	0.19	0.20	0.18
8192	31.25	0.31	0.29	0.26	0.13	0.14	0.13	0.13	0.13
4256	60	0.46	0.41	0.41	0.20	0.20	0.19	0.17	0.17
5120	50	0.40	0.37	0.37	0.18	0.19	0.16	0.17	0.15
15360	16.7	0.22	0.23	0.21	0.10	0.09	0.11	0.10	0.09
25600	10	0.19	0.15	0.16	0.07	0.08	0.08	0.07	0.07
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
10240	25	0.32	0.30	0.29	0.16	0.15	0.14	0.14	0.13
12800	20	0.31	0.26	0.25	0.15	0.14	0.13	0.13	0.12

(1) Using f_{CLK} = 4.096MHz

Table 6-5. Input-referred Noise in μV_{RMS}, Speed Mode 2 (f_{MOD} = 512kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	64000	331.89	168.39	85.04	43.16	42.80	22.34	22.83	11.94
16	32000	50.16	25.61	13.71	8.45	8.25	6.40	6.48	4.36
24	21333	35.15	18.04	9.80	6.33	6.37	5.04	5.21	3.52
32	16000	29.85	14.94	8.40	5.48	5.42	4.45	4.33	3.01
64	8000	20.97	10.63	6.05	3.84	3.84	3.20	3.19	2.18
128	4000	14.78	7.42	4.24	2.77	2.73	2.24	2.24	1.55
256	2000	10.41	5.35	3.03	1.93	1.91	1.57	1.56	1.10
512	1000	7.25	3.77	2.12	1.36	1.35	1.12	1.11	0.77
640	800	6.70	3.35	1.89	1.20	1.22	1.00	0.99	0.70
1024	500	5.22	2.60	1.48	0.96	0.96	0.79	0.79	0.54
2048	250	3.63	1.81	1.07	0.69	0.68	0.56	0.55	0.38
4096	125	2.47	1.33	0.78	0.50	0.47	0.39	0.38	0.28
8192	62.5	1.84	0.91	0.53	0.35	0.32	0.30	0.30	0.20
8512	60	1.68	0.94	0.50	0.34	0.33	0.28	0.27	0.18
10240	50	1.73	0.83	0.49	0.31	0.32	0.26	0.25	0.15
30720	16.7	1.04	0.53	0.29	0.16	0.19	0.15	0.14	0.10
51200	10	0.91	0.38	0.20	0.13	0.13	0.11	0.13	0.07
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	64000	493.10	249.35	125.06	62.77	61.69	31.82	32.39	16.85
16	32000	76.71	38.45	19.94	11.30	11.26	7.74	7.72	4.93
24	21333	40.69	20.62	11.58	7.22	7.26	5.58	5.59	3.80
32	16000	33.05	16.36	9.26	5.91	5.91	4.73	4.76	3.24
64	8000	22.27	11.34	6.56	4.15	4.12	3.37	3.37	2.33
128	4000	15.69	7.90	4.47	2.92	2.91	2.40	2.41	1.66
256	2000	11.18	5.52	3.17	2.06	2.03	1.68	1.70	1.16
512	1000	7.83	3.98	2.20	1.44	1.43	1.20	1.20	0.82
640	800	7.04	3.59	2.01	1.30	1.33	1.07	1.09	0.73
1024	500	5.59	2.78	1.61	1.04	1.04	0.84	0.84	0.57
2048	250	3.86	1.97	1.13	0.71	0.74	0.61	0.60	0.40
4096	125	2.77	1.44	0.83	0.52	0.53	0.42	0.43	0.29
8192	62.5	1.94	1.02	0.61	0.38	0.34	0.29	0.27	0.22
8512	60	1.91	0.98	0.56	0.38	0.35	0.27	0.30	0.19
10240	50	1.85	0.96	0.51	0.33	0.34	0.26	0.27	0.18
30720	16.7	1.09	0.56	0.28	0.19	0.18	0.16	0.16	0.10
51200	10	0.83	0.40	0.22	0.17	0.13	0.12	0.13	0.09

Table 6-5. Input-referred Noise in μV_{RMS}, Speed Mode 2 (f_{MOD} = 512kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	8000	25.43	12.93	7.26	4.75	4.72	4.72	4.72	4.72
128	4000	19.81	10.13	5.62	3.64	3.65	3.65	3.65	3.65
256	2000	14.62	7.30	4.12	2.68	2.72	2.72	2.72	2.72
512	1000	10.40	5.34	3.00	1.93	1.94	1.94	1.94	1.94
640	800	9.25	4.76	2.67	1.74	1.72	1.72	1.72	1.72
1024	500	7.48	3.88	2.13	1.37	1.38	1.38	1.38	1.38
2048	250	5.27	2.72	1.53	0.98	0.97	0.97	0.97	0.97
4096	125	3.79	1.93	1.04	0.68	0.67	0.67	0.67	0.67
8192	62.5	2.81	1.32	0.74	0.48	0.49	0.49	0.49	0.49
8512	60	2.64	1.35	0.78	0.49	0.48	0.48	0.48	0.48
10240	50	2.31	1.27	0.68	0.43	0.45	0.45	0.45	0.45
30720	16.7	1.41	0.64	0.42	0.25	0.26	0.26	0.26	0.26
51200	10	1.13	0.48	0.31	0.21	0.22	0.22	0.22	0.22
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
20480	25	1.96	1.01	0.57	0.35	0.33	0.30	0.29	0.18
25600	20	1.77	0.90	0.49	0.33	0.31	0.27	0.26	0.17

(1) Using f_{CLK} = 4.096MHz

Table 6-6. Input-referred Noise in μV_{RMS}, Speed Mode 2 (f_{MOD} = 512kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	64000	12.25	7.13	7.19	4.03	3.98	2.73	2.71	2.12
16	32000	4.37	3.58	3.54	2.13	2.15	1.71	1.72	1.44
24	21333	3.48	2.90	2.90	1.73	1.76	1.40	1.41	1.19
32	16000	3.04	2.49	2.52	1.51	1.52	1.23	1.21	1.05
64	8000	2.16	1.83	1.81	1.09	1.10	0.90	0.89	0.76
128	4000	1.54	1.27	1.27	0.77	0.78	0.63	0.63	0.54
256	2000	1.07	0.90	0.89	0.54	0.55	0.44	0.44	0.38
512	1000	0.76	0.64	0.64	0.38	0.39	0.32	0.32	0.27
640	800	0.68	0.57	0.58	0.35	0.34	0.28	0.28	0.24
1024	500	0.55	0.45	0.44	0.28	0.27	0.22	0.22	0.19
2048	250	0.38	0.30	0.31	0.20	0.20	0.16	0.16	0.13
4096	125	0.27	0.22	0.23	0.13	0.14	0.11	0.11	0.10
8192	62.5	0.18	0.16	0.15	0.10	0.10	0.08	0.08	0.07
8512	60	0.19	0.15	0.16	0.10	0.09	0.08	0.08	0.06
10240	50	0.17	0.14	0.14	0.09	0.09	0.07	0.07	0.06
30720	16.7	0.10	0.09	0.08	0.05	0.05	0.04	0.04	0.04
51200	10	0.08	0.06	0.07	0.04	0.04	0.03	0.03	0.03
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	64000	16.74	9.54	9.32	5.01	5.05	3.22	3.21	2.35
16	32000	5.01	3.91	3.88	2.34	2.37	1.85	1.83	1.52
24	21333	3.85	3.15	3.08	1.90	1.89	1.51	1.52	1.28
32	16000	3.25	2.69	2.65	1.64	1.61	1.31	1.31	1.12
64	8000	2.33	1.94	1.90	1.16	1.16	0.95	0.95	0.82
128	4000	1.64	1.35	1.37	0.82	0.83	0.68	0.67	0.57
256	2000	1.14	0.96	0.97	0.59	0.59	0.48	0.47	0.42
512	1000	0.83	0.67	0.67	0.41	0.41	0.33	0.34	0.29
640	800	0.74	0.61	0.60	0.37	0.37	0.30	0.30	0.26
1024	500	0.58	0.48	0.48	0.29	0.29	0.24	0.24	0.21
2048	250	0.41	0.34	0.34	0.21	0.21	0.17	0.17	0.14
4096	125	0.30	0.25	0.24	0.14	0.14	0.12	0.12	0.11
8192	62.5	0.21	0.17	0.17	0.11	0.10	0.09	0.08	0.07
8512	60	0.19	0.16	0.17	0.10	0.10	0.08	0.08	0.07
10240	50	0.20	0.15	0.16	0.09	0.10	0.08	0.08	0.07
30720	16.7	0.12	0.09	0.07	0.05	0.06	0.05	0.04	0.04
51200	10	0.08	0.08	0.07	0.04	0.04	0.04	0.03	0.03

Table 6-6. Input-referred Noise in μV_{RMS}, Speed Mode 2 (f_{MOD} = 512kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	8000	2.62	2.19	2.21	1.33	1.33	1.08	1.09	0.94
128	4000	2.03	1.71	1.68	1.04	1.04	0.85	0.84	0.71
256	2000	1.49	1.24	1.25	0.76	0.76	0.62	0.62	0.53
512	1000	1.07	0.89	0.90	0.54	0.55	0.44	0.44	0.39
640	800	0.97	0.80	0.82	0.49	0.49	0.40	0.40	0.34
1024	500	0.77	0.66	0.64	0.40	0.40	0.31	0.32	0.28
2048	250	0.54	0.45	0.45	0.29	0.27	0.23	0.22	0.20
4096	125	0.40	0.32	0.32	0.19	0.19	0.17	0.16	0.14
8192	62.5	0.27	0.23	0.23	0.13	0.14	0.11	0.11	0.10
8512	60	0.29	0.23	0.22	0.14	0.14	0.11	0.11	0.09
10240	50	0.25	0.20	0.21	0.12	0.12	0.10	0.10	0.09
30720	16.7	0.14	0.12	0.13	0.07	0.07	0.06	0.05	0.05
51200	10	0.11	0.08	0.08	0.06	0.05	0.05	0.05	0.04
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
20480	25	0.19	0.17	0.17	0.10	0.10	0.08	0.08	0.07
25600	20	0.18	0.15	0.14	0.09	0.09	0.08	0.07	0.06

(1) Using f_{CLK} = 4.096MHz

Table 6-7. Input-referred Noise in μV_{RMS}, Speed Mode 3 (f_{MOD} = 1024kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	128000	341.43	169.44	84.79	43.36	43.99	24.02	24.33	13.26
16	64000	50.75	26.14	14.60	9.62	9.50	8.46	8.61	5.90
24	42667	35.50	18.32	10.35	7.44	7.39	6.85	6.81	4.81
32	32000	30.36	15.58	8.89	6.37	6.33	5.98	5.94	4.14
64	16000	21.38	10.84	6.34	4.49	4.46	4.17	4.18	2.95
128	8000	15.17	7.72	4.47	3.14	3.17	2.94	2.96	2.07
256	4000	10.54	5.45	3.21	2.26	2.24	2.10	2.09	1.48
512	2000	7.42	3.88	2.25	1.59	1.61	1.50	1.49	1.05
640	1600	6.77	3.52	2.02	1.42	1.42	1.33	1.31	0.92
1024	1000	5.36	2.75	1.58	1.14	1.12	1.03	1.05	0.73
2048	500	3.80	1.94	1.12	0.79	0.78	0.75	0.74	0.52
4096	250	2.68	1.33	0.80	0.57	0.56	0.52	0.53	0.38
8192	125	1.90	0.92	0.59	0.39	0.39	0.37	0.36	0.26
17024	60	1.30	0.66	0.39	0.28	0.26	0.25	0.25	0.18
20480	50	1.21	0.58	0.36	0.26	0.26	0.23	0.24	0.16
61440	16.7	0.67	0.35	0.20	0.15	0.14	0.14	0.13	0.10
102400	10	0.50	0.29	0.15	0.11	0.11	0.11	0.12	0.07
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	128000	495.16	252.54	125.84	62.89	63.57	32.77	33.04	17.70
16	64000	77.33	38.98	20.79	12.25	12.30	9.67	9.76	6.55
24	42667	41.27	21.32	12.09	8.11	8.19	7.45	7.34	5.16
32	32000	32.99	16.83	9.84	6.83	6.92	6.32	6.48	4.51
64	16000	22.60	11.61	6.88	4.78	4.81	4.55	4.56	3.20
128	8000	15.83	8.43	4.84	3.40	3.42	3.16	3.14	2.25
256	4000	11.33	5.77	3.40	2.39	2.44	2.25	2.26	1.58
512	2000	8.06	4.08	2.41	1.72	1.69	1.59	1.59	1.13
640	1600	7.15	3.69	2.16	1.53	1.50	1.40	1.44	1.01
1024	1000	5.68	2.89	1.69	1.18	1.22	1.13	1.15	0.79
2048	500	4.07	2.02	1.21	0.85	0.85	0.80	0.79	0.55
4096	250	2.81	1.45	0.86	0.61	0.59	0.57	0.57	0.40
8192	125	2.04	1.04	0.61	0.43	0.40	0.39	0.40	0.28
17024	60	1.38	0.76	0.40	0.30	0.28	0.28	0.28	0.19
20480	50	1.30	0.65	0.38	0.27	0.28	0.23	0.27	0.17
61440	16.7	0.71	0.37	0.24	0.16	0.16	0.14	0.14	0.10
102400	10	0.54	0.36	0.19	0.12	0.14	0.11	0.13	0.07

Table 6-7. Input-referred Noise in μV_{RMS}, Speed Mode 3 (f_{MOD} = 1024kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 16 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		0.5	1	2	4	5	8	10	16
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	16000	25.74	13.43	7.79	5.51	5.44	5.12	5.12	3.55
128	8000	19.86	10.28	5.98	4.25	4.20	3.94	3.98	2.80
256	4000	14.70	7.59	4.40	3.16	3.16	2.91	2.89	2.05
512	2000	10.61	5.46	3.21	2.28	2.25	2.09	2.11	1.48
640	1600	9.49	4.88	2.88	2.01	2.04	1.87	1.89	1.33
1024	1000	7.67	3.95	2.28	1.60	1.61	1.51	1.50	1.06
2048	500	5.45	2.80	1.64	1.17	1.15	1.07	1.05	0.75
4096	250	3.79	2.02	1.16	0.81	0.79	0.74	0.74	0.55
8192	125	2.65	1.38	0.83	0.59	0.56	0.54	0.54	0.37
17024	60	1.93	0.91	0.57	0.38	0.40	0.39	0.38	0.26
20480	50	1.77	0.89	0.52	0.36	0.36	0.34	0.35	0.24
61440	16.7	1.01	0.54	0.33	0.22	0.22	0.19	0.20	0.13
102400	10	0.87	0.36	0.21	0.16	0.17	0.16	0.15	0.11
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
40960	25	1.35	0.67	0.40	0.30	0.29	0.29	0.26	0.20
51200	20	1.18	0.65	0.39	0.27	0.26	0.24	0.23	0.17

(1) Using f_{CLK} = 4.096MHz

Table 6-8. Input-referred Noise in μV_{RMS}, Speed Mode 3 (f_{MOD} = 1024kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	128000	13.38	8.66	8.56	4.93	4.89	3.59	3.52	2.81
16	64000	5.98	4.92	4.93	2.95	2.96	2.39	2.39	2.00
24	42667	4.82	3.94	4.05	2.47	2.44	1.96	1.99	1.67
32	32000	4.19	3.41	3.44	2.08	2.09	1.70	1.68	1.45
64	16000	2.95	2.46	2.46	1.50	1.51	1.22	1.22	1.03
128	8000	2.11	1.75	1.75	1.07	1.07	0.88	0.86	0.74
256	4000	1.47	1.25	1.24	0.75	0.75	0.62	0.60	0.52
512	2000	1.06	0.88	0.88	0.53	0.53	0.43	0.43	0.37
640	1600	0.92	0.79	0.78	0.48	0.47	0.38	0.39	0.32
1024	1000	0.74	0.63	0.63	0.38	0.39	0.31	0.31	0.26
2048	500	0.52	0.44	0.43	0.27	0.27	0.22	0.22	0.19
4096	250	0.37	0.31	0.31	0.19	0.19	0.15	0.16	0.13
8192	125	0.25	0.22	0.22	0.14	0.13	0.10	0.11	0.09
17024	60	0.18	0.15	0.15	0.10	0.09	0.08	0.08	0.06
20480	50	0.16	0.14	0.13	0.08	0.08	0.07	0.07	0.06
61440	16.7	0.10	0.08	0.07	0.05	0.05	0.04	0.04	0.04
102400	10	0.08	0.07	0.07	0.04	0.04	0.03	0.03	0.03
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 10000b)									
8	128000	17.76	10.67	10.66	5.87	5.84	3.98	4.05	3.06
16	64000	6.59	5.35	5.19	3.18	3.21	2.57	2.54	2.15
24	42667	5.15	4.30	4.33	2.60	2.60	2.09	2.09	1.76
32	32000	4.46	3.71	3.73	2.24	2.28	1.83	1.83	1.54
64	16000	3.16	2.63	2.66	1.61	1.64	1.31	1.31	1.13
128	8000	2.26	1.87	1.88	1.15	1.13	0.92	0.92	0.80
256	4000	1.58	1.34	1.33	0.81	0.81	0.66	0.66	0.56
512	2000	1.14	0.95	0.95	0.56	0.57	0.46	0.46	0.39
640	1600	1.01	0.85	0.85	0.51	0.50	0.42	0.41	0.36
1024	1000	0.78	0.67	0.67	0.40	0.41	0.33	0.32	0.28
2048	500	0.56	0.47	0.45	0.29	0.29	0.24	0.23	0.20
4096	250	0.39	0.34	0.34	0.20	0.20	0.16	0.17	0.14
8192	125	0.28	0.23	0.24	0.14	0.15	0.12	0.11	0.10
17024	60	0.20	0.17	0.16	0.10	0.10	0.08	0.08	0.07
20480	50	0.18	0.15	0.15	0.09	0.09	0.08	0.07	0.06
61440	16.7	0.10	0.08	0.09	0.06	0.05	0.04	0.05	0.03
102400	10	0.07	0.06	0.06	0.04	0.04	0.03	0.04	0.03

Table 6-8. Input-referred Noise in μV_{RMS}, Speed Mode 3 (f_{MOD} = 1024kHz) at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 20 to 256 (continued)

OSR	DATA RATE (SPS)(1)	GAIN							
		20	32	50	64	100	128	200	256
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11101b)									
64	16000	3.61	3.04	3.04	1.83	1.83	1.51	1.48	1.28
128	8000	2.78	2.36	2.34	1.43	1.42	1.16	1.15	0.99
256	4000	2.09	1.71	1.72	1.06	1.04	0.84	0.85	0.73
512	2000	1.47	1.24	1.24	0.76	0.75	0.61	0.61	0.53
640	1600	1.32	1.12	1.12	0.68	0.68	0.55	0.55	0.47
1024	1000	1.05	0.89	0.88	0.54	0.54	0.44	0.44	0.37
2048	500	0.74	0.63	0.63	0.38	0.38	0.31	0.31	0.27
4096	250	0.53	0.45	0.44	0.27	0.27	0.22	0.22	0.18
8192	125	0.38	0.32	0.30	0.18	0.19	0.15	0.16	0.13
17024	60	0.26	0.21	0.22	0.14	0.13	0.11	0.11	0.09
20480	50	0.25	0.20	0.19	0.12	0.12	0.09	0.10	0.08
61440	16.7	0.14	0.12	0.11	0.07	0.07	0.06	0.05	0.05
102400	10	0.10	0.09	0.09	0.05	0.06	0.04	0.04	0.04
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)									
40960	25	0.20	0.17	0.17	0.10	0.09	0.08	0.08	0.07
51200	20	0.18	0.16	0.16	0.10	0.09	0.07	0.07	0.06

(1) Using f_{CLK} = 4.096MHz

7 Detailed Description

7.1 Overview

The ADS1x4S1x are low-power, 16- and 24-bit, ΔΣ ADCs that offer many integrated features to reduce system cost and component count in the most common sensor measurement applications. The devices are available in a 7mm × 7mm TQFP-32 package.

Key integrated analog features include:

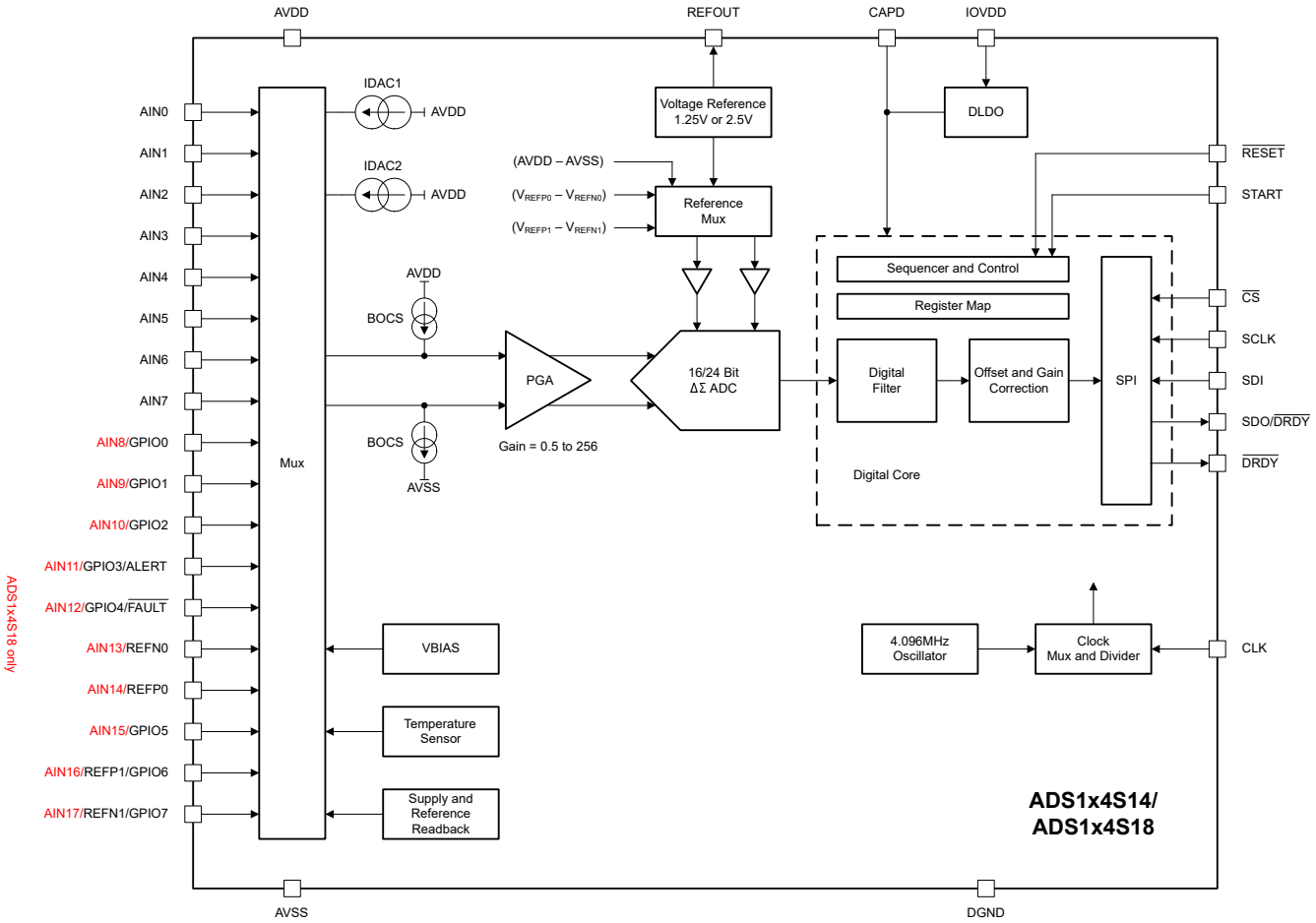
- A flexible input multiplexer which allows to select any of the 8 (ADS1x4S14) or 18 (ADS1x4S18) analog inputs, or AVSS as positive or negative input.
- A low-noise, high input-impedance PGA with programmable gain from 0.5 to 256.
  - Gain of 0.5 allows to measure signals which are larger than the selected reference voltage.
  - Single-ended measurements, where the negative input is connected to AVSS, are possible for gain settings between 0.5 and 10.
- A low-drift voltage reference programmable to 1.25V or 2.5V. A buffered version of the internal voltage reference is available on the REFOUT pin which can be used to bias external circuitry.
- Two external, differential reference input pairs (REFP0, REFN0 and REFP1, REFN1) with optional reference buffers that can be individually enabled and disabled.
- Two matched, sensor-excitation current sources (IDACs) which can be routed to any of the 8 (ADS1x4S14) or 18 (ADS1x4S18) analog inputs to bias resistive sensors, such as thermistors, resistance temperature detectors (RTDs), or bridge sensors. Excitation currents between 1µA and 1mA can be programmed with fine granularity.
- A set of programmable burn-out current sources that are used for sensor fault detection.
- A low-drift 4.096MHz oscillator which establishes the device main clock. Alternatively an external clock can be provided.
- A linear temperature sensor.
- A bias voltage generator (VBIAS) that is used to bias floating sensors, such as thermocouples.
- Analog supply and reference undervoltage monitors. Depending on the circuit implementation, the reference undervoltage monitor is especially helpful to detect open sensor conditions.
- Eight general-purpose input/output pins (GPIOs) which are shared with analog inputs on the ADS1x4S18. Push-pull or open-drain output configurations can be individually selected for each general-purpose output. The GPIOs use logic levels based on the analog supply.

The devices also include a variety of digital features to accommodate a wide range of applications:

- Four speed modes allow to optimize the power consumption and noise performance for each application.
- Depending on the selected speed mode, output data rates from 3.9SPS up to 128kSPS can be achieved by adjusting the oversampling ratio (OSR) of the integrated digital filter. At output data rates of 20SPS and 25SPS, the digital filter offers simultaneous 50Hz and 60Hz line-cycle rejection with single-cycle settling.
- A sequencer allows to scan through up to 24 individually programmable sequence step configurations without host controller interaction.
- A global-chop mode which reduces offset and offset drift to a minimum.
- User offset and gain calibration registers per sequence step.
- A digital comparator with configurable high and low thresholds per sequence step. Together with the sequencer, the digital comparator can for example be used for autonomous supply voltage monitoring. Use the dedicated digital comparator ALERT output pin to interrupt and notify the host controller of a tripped comparator.
- An SPI-compatible serial interface to read conversion and register data, as well as to configure and control the device. 3-wire SPI operation is possible when the $\overline{CS}$ pin is tied low permanently to reduce the number of required digital communication signals. The interface allows communication with multiple devices on one SPI bus in a daisy chain.
- Data integrity features, such as SPI CRC, register map CRC, and internal memory CRC to detect communication faults and unintended bit flips.

- Selection between two output data coding schemes: binary two's complement and unipolar straight binary format. The unipolar straight binary format is beneficial for applications where the differential input signal is always positive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs and Multiplexer

The ADS1x4S1x contain a flexible input multiplexer; see Figure 7-1. Select any of the 8 (ADS1x4S14) or 18 (ADS1x4S18) analog inputs as the positive or negative input for the PGA using the STEPx_AINP[4:0] and STEPx_AINN[4:0] bits. In addition, an internal AVSS connection can be selected as the positive or negative PGA input.

The multiplexer also routes the two integrated excitation current sources to any of the 8 (ADS1x4S14) or 18 (ADS1x4S18) analog input pins to bias resistive sensors (bridges, RTDs, and thermistors).

In addition, the ADS1x4S1x contain the following system monitor functions which can be selected for measurement through the multiplexer using the STEPx_SYS_MON[2:0] bits:

- The inputs of the PGA can be shorted together to mid-supply, (AVDD + AVSS) / 2, to measure and calibrate the input offset of the internal signal chain.
- An integrated temperature sensor that provides an output signal proportional to the device temperature.
- Any of the two attenuated external reference voltages, (V_{REFPx} – V_{REFNx}) / 8.
- The attenuated analog and digital supplies, ((AVDD – AVSS) / 8), (IOVDD / 8), and (V_{DLDO} / 4).

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 5:

$$AVSS - 0.3V < V_{AINx} < AVDD + 0.3V \quad (5)$$

External Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

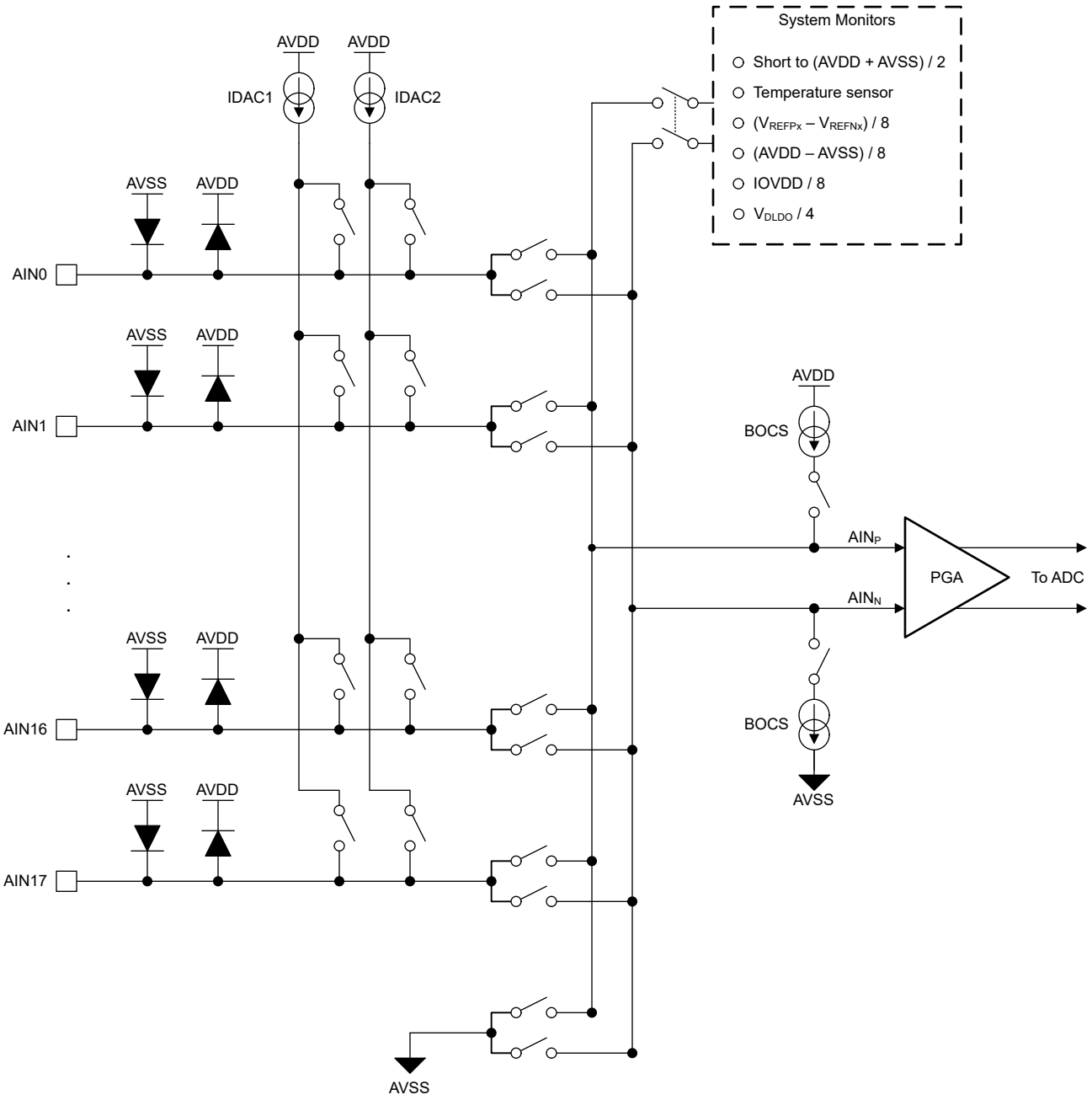


Figure 7-1. Input Multiplexer (ADS1x4S18)

7.3.2 Programmable Gain Amplifier (PGA)

The ADS1x4S1x integrate a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). Use the STEPx_GAIN[3:0] bits to configure the PGA for gains of 0.5, 1, 2, 4, 5, 8, 10, 16, 20, 32, 50, 64, 100, 128, 200, or 256. The full-scale input voltage range (FSR) of the PGA is defined by the gain setting, the reference voltage, and the conversion data coding setting, as shown in Equation 6 and Equation 7:

$$\text{Binary two's complement coding: FSR} = \pm V_{REF} / \text{Gain} \quad (6)$$

$$\text{Unipolar straight binary coding: FSR} = 0\text{V to} + V_{REF} / \text{Gain} \quad (7)$$

Table 7-1 shows the corresponding nominal full-scale ranges using binary two's complement coding for a 1.25V and a 2.5V reference voltage, respectively.

Table 7-1. PGA Full-Scale Range (Binary Two's Complement Coding)

GAIN SETTING	V_{REF} = 1.25V	V_{REF} = 2.5V
0.5	±2.5V	±5V
1	±1.25V	±2.5V
2	±0.625V	±1.25V
4	±0.313V	±0.625V
5	±0.25V	±0.5V
8	±0.156V	±0.313V
10	±0.125V	±0.25V
16	±78.125mV	±0.156V
20	±62.5mV	±0.125V
32	±39.063mV	±78.125mV
50	±25mV	±50mV
64	±19.531mV	±30.063mV
100	±12.5mV	±25mV
128	±9.766mV	±19.531mV
200	±6.25mV	±12.5mV
256	±4.883mV	±9.766mV

Depending on the gain setting, the PGA has certain voltage headroom requirements to stay within the linear operating range that must be met for the selected positive and negative analog inputs as specified by the *absolute input voltage* parameter in the *Recommended Operating Conditions*. Both the positive and negative PGA inputs need to stay within those voltage limits, even for FSR settings which in principle extend beyond those limits. For example, assume AVDD = 3.3V, AVSS = GND, gain = 0.5, V_{REF} = 2.5V, unipolar coding scheme, and AINN connected to GND. In this case AINP needs to stay between 0V and (3.3V – 0.35V) = 2.95V. Therefore only a portion of the full code range (FSR = 0V to 5V) is utilized.

For gain settings 0.5 to 10, the devices allow single-ended measurements with the negative analog input held at AVSS. The negative analog input can be connected to AVSS externally using one of the analog inputs or the internal AVSS connection of the multiplexer in this case. The devices offer a unipolar, straight binary conversion data coding scheme that can be selected using the STEPx_CODING bit. This coding scheme is beneficial for single-ended measurements, because the full code range is mapped to the 0V to $+V_{REF}$ / Gain voltage range.

For gain settings 16 to 256 the PGA requires some voltage headroom from AVSS and AVDD on both the positive and negative analog inputs.

The PGA remains active in idle mode, but turns off in standby and power-down mode.

7.3.3 Voltage Reference

The ADC requires a reference voltage for operation. The magnitude of the reference voltage together with the PGA gain setting establishes the ADC full-scale range. Use the STEPx_REF_SEL[1:0] bits to select from one of the following reference sources:

- Internal voltage reference
- External reference connected between the REFP0 and REFN0 pins ($V_{REF} = V_{REFP0} – V_{REFN0}$)
- External reference connected between the REFP1 and REFN1 pins ($V_{REF} = V_{REFP1} – V_{REFN1}$)
- Analog supply (V_{REF} = AVDD – AVSS)

7.3.3.1 Internal Reference

The devices integrate a precision, low-drift voltage reference. Select between a 1.25V and 2.5V reference voltage option using the REF_VAL bit. When changing the REF_VAL bit setting, allow at least 10ms for the device to switch the reference value before starting any conversions. The internal voltage reference requires a certain voltage headroom from the AVDD supply for operation as specified in the *Electrical Characteristics* table. Keep this headroom in mind when selecting the 2.5V reference value.

The internal reference is always enabled even when the external reference or the analog supply is selected as the reference source. The internal voltage reference only powers down in power-down mode.

The REFOUT pin provides a buffered version of the internal reference voltage. The REFOUT pin can both source and sink current to bias external circuitry. Connect a 100nF capacitor between REFOUT and AVSS. Larger capacitor values up to 1.3µF can be used to help filter more noise at the expense of a longer reference start-up time. The capacitor is required for the internal voltage reference stability, even when the REFOUT pin is not used to bias any external circuitry, and even when one of the external references or the analog supply is selected as the reference source. Keep the reference settling time in mind after device power-up, reset, or when coming out of power-down mode before starting any conversions.

7.3.3.2 External Reference

The devices provide two differential external reference input pairs, REFP0, REFN0 and REFP1, REFN1. The differential voltage between REFPx and REFNx (x = 0 or 1) establishes the reference voltage for the ADC, $V_{REF} = V_{REFPx} – V_{REFNx}$. The differential reference inputs allow freedom in the reference common-mode voltage. However, the polarity of the reference voltage must be positive. That is, V_{REFPx} needs to be larger than V_{REFNx}. Follow the requirements in the *Recommended Operating Conditions* for the absolute and differential reference input voltages.

On ADS1x4S18 REFP0, REFN0 and REFP1, REFN1 inputs are combined with the AIN14, AIN13 and AIN16, AIN17 pins, respectively. AIN13, AIN14, AIN16 and AIN17 can still be used as analog inputs, even when the inputs are configured as external reference inputs.

7.3.3.3 Reference Buffers

The devices provide two individually selectable reference input buffers to lower the reference input current. Use the STEPx_REFP_BUF_EN and STEPx_REFN_BUF_EN bits to enable or disable the positive and negative reference buffers respectively.

Disable the negative reference buffer when the selected external negative reference input (REFNx) is at AVSS. Disable the positive reference buffer when the selected external positive reference input (REFPx) is at AVDD. Disable both reference buffers when either the internal voltage reference or the analog supply is selected as the reference source.

The reference buffers remain active in idle mode, but turn off in standby and power-down mode.

7.3.4 Power-Scalable Speed Modes

The devices offer four speed modes to trade off power consumption, resolution, and data rate. Each speed mode corresponds to a specific modulator clock frequency and device bias current setting. Speed mode 3 (f_{MOD} = 1.024MHz) offers the highest data rates (up to 128kSPS) and the lowest noise at the 10SPS data rate setting. In contrast, speed mode 0 (f_{MOD} = 32kHz) minimizes power consumption at the expense of noise performance.

Select the speed mode using the SPEED_MODE[1:0] bits based on the desired data rate, resolution, and device power consumption requirements. The speed mode applies globally to the device and cannot be configured for each individual sequence step.

7.3.5 Clock Source

The ADS1x4S1x require a main clock for operation. The main clock is provided in one of two ways:

- The internal low-drift 4.096MHz oscillator or
- An external clock on the CLK input pin

Use the CLK_SEL bit to select the clock source. At device power-up or after device reset, the internal oscillator is selected as the clock source by default.

The modulator clock for the delta-sigma ADC is derived from the main clock. A clock divider divides the main clock frequency (f_{CLK}) by a division factor based on the selected speed mode to create the modulator frequency (f_{MOD} = f_{CLK} / DIV). Table 7-2 shows the respective clock divider settings per speed mode together with the nominal modulator frequencies.

Table 7-2. Clock Divider Settings

SPEED MODE	CLOCK DIVIDER (DIV)	MODULATOR FREQUENCY (f_{MOD})(1)
0	128	32kHz
1	16	256kHz
2	8	512kHz
3	4	1.024MHz

(1) Using a nominal clock frequency of f_{CLK} = 4.096MHz.

7.3.6 Delta-Sigma Modulator

The ADS1x4S1x use an inherently stable, third-order, delta-sigma modulator. The modulator samples the analog input voltage at the modulator frequency (f_{MOD} = 1 / t_{MOD}) and converts the analog input to a ones-density bitstream representing the ratio between the input signal and the reference voltage. The modulator shapes the noise of the converter to high frequency, where the noise is removed by the digital filter.

7.3.7 Digital Filter

The delta-sigma modulator bitstream feeds into a digital filter. The digital filter low-pass filters and decimates the low-resolution, high-speed modulator output to produce high-resolution ADC data at an output data rate of f_{DATA}. The decimation factor, defined as per Equation 8, is called the oversampling ratio (OSR).

$$OSR = f_{MOD} / f_{DATA} \quad (8)$$

The OSR determines the amount of averaging that is applied to the modulator output in the digital filter and, therefore, the filter bandwidth and conversion noise. Higher OSRs lead to lower filter bandwidth and better noise performance.

Use the STEPx_FLTR_OSR[4:0] bits to select the OSR, and together with the STEPx_FLTR_MODE bit to select between the following digital filter types:

- Sinc3 or Sinc4 filter with OSRs ranging from 8 to 102400.
- Sinc4 filter with a fixed OSR of 32, followed by a Sinc1 filter with OSRs ranging from 2 to 3200.
- Finite impulse response (FIR) filter with speed-mode independent data rate options of 20SPS and 25SPS, which offers simultaneous 50Hz and 60Hz line-cycle rejection.

Figure 7-2 shows the digital filter architecture.

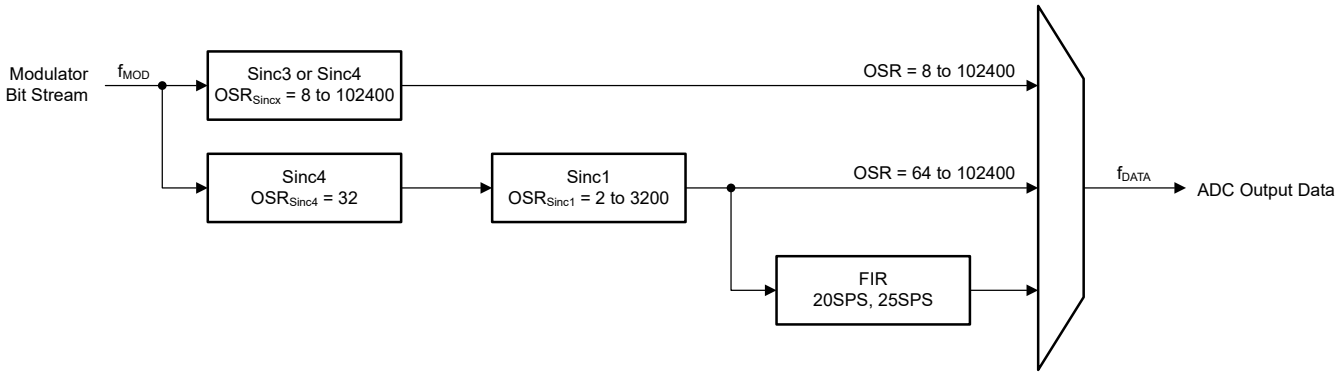


Figure 7-2. Digital Filter Architecture

7.3.7.1 Sinc3 and Sinc4 Filters

STEPx_FLTR_OSR[4:0] bit settings 00000b to 10000b determine the OSR settings for the Sinc3 or Sinc4 filter. Select the Sinc filter order (Sinc3 or Sinc4) using the STEPx_FLTR_MODE bit. The Sinc4 filter yields better noise performance compared to the Sinc3 filter at the expense of longer settling time. The STEPx_FLTR_MODE bit has no effect when using STEPx_FLTR_OSR[4:0] bit settings beyond 10000b.

For STEPx_FLTR_OSR[4:0] bit settings 00000b to 01100b, Table 7-3 provides an overview of the resulting output data rates for the various speed modes. The data rates scale with f_{CLK}.

Table 7-3. Sinc3 and Sinc4 Filter Output Data Rates

OSR	OUTPUT DATA RATE (f_{DATA})(1)			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
8	4kSPS	32kSPS	64kSPS	128kSPS
16	2kSPS	16kSPS	32kSPS	64kSPS
24	1.33kSPS	10.67kSPS	21.33kSPS	42.67kSPS
32	1kSPS	8kSPS	16kSPS	32kSPS
64	500SPS	4kSPS	8kSPS	16kSPS
128	250SPS	2kSPS	4kSPS	8kSPS
256	125SPS	1kSPS	2kSPS	4kSPS
512	62.5SPS	500SPS	1kSPS	2kSPS
640	50SPS	400SPS	800SPS	1.6kSPS
1024	31.25SPS	250SPS	500SPS	1kSPS
2048	15.63SPS	125SPS	250SPS	500SPS
4096	7.81SPS	62.5SPS	125SPS	250SPS
8192	3.91SPS	31.25SPS	62.5SPS	125SPS

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

For STEPx_FLTR_OSR[4:0] bit settings 01101b to 10000b, the device adjusts the OSR setting based on the selected speed mode to achieve the desired output data rates of 10SPS, 16.7SPS, 50SPS or 60SPS in each of the four speed modes. Table 7-4 lists the OSR settings for each speed mode. Because the output data rate scales with the clock frequency, use the internal oscillator or an external clock with a nominal frequency of f_{CLK} = 4.096MHz to achieve the listed data rates.

The digital filter offers 50Hz line-cycle rejection at output data rates of 16.7SPS and 50SPS. At 60SPS, the digital filter offers 60Hz line-cycle rejection. The digital filter rejects both 50Hz and 60Hz line-cycle frequencies at 10SPS. See the *50Hz and 60Hz Line Cycle Rejection* section for more details regarding the device's 50Hz and 60Hz line-cycle rejection capabilities.

Table 7-4. Sinc3 and Sinc4 Filter OSR Settings for Output Data Rates With Line-Cycle Rejection

OUTPUT DATA RATE[1] (f_{DATA})	OSR			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
10SPS	3200	25600	51200	102400
16.7SPS	1920	15360	30720	61440
50SPS	640	5120	10240	20480
60SPS	532	4256	8512	17024

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

The frequency response of the Sinc filters is given by Equation 9.

$$|H_{(f)}| = \left| \frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^{x} \quad (9)$$

where:

- f = Signal frequency
- f_{MOD} = Modulator frequency
- A = Sinc filter OSR
- x = Order of the Sinc filter (3 or 4)

Table 7-5 lists the –3dB frequencies for the two Sinc filter orders.

Table 7-5. Sinc Filter –3dB Frequencies

SINC FILTER ORDER	–3dB FREQUENCY
Sinc3	0.262× f_{DATA}
Sinc4	0.227× f_{DATA}

Figure 7-3 and Figure 7-4 show the filter frequency responses of the Sinc filters normalized to the output data rate. A Sinc filter has infinite attenuation at integer multiples of the output data rate except for integer multiples of f_{MOD}, as shown in Figure 7-4. As with all digital filters, the frequency response repeats at integer multiples of the modulator frequency, f_{MOD}. The digital filter provides no attenuation at input frequencies near n × f_{MOD} (n = 1, 2, 3, and so on). The data rate and filter notch frequencies scale with f_{MOD}.

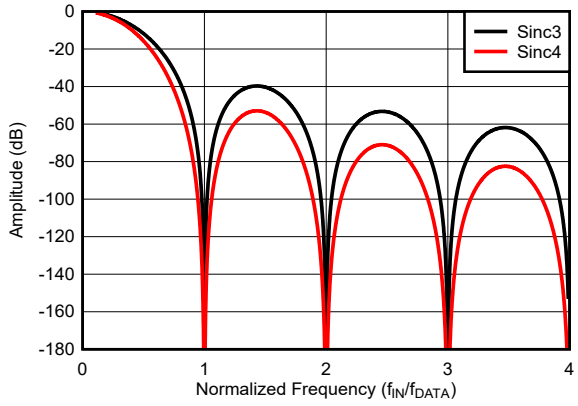


Figure 7-3. Sinc3 and Sinc4 Filter Frequency Response

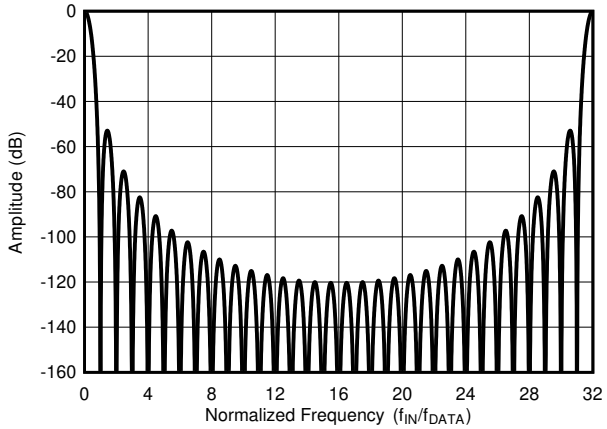


Figure 7-4. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

7.3.7.2 Sinc4 + Sinc1 Filter

STEPx_FLTR_OSR[4:0] bit settings 10001b to 11101b determine the OSR settings for the cascaded Sinc4 + Sinc1 filter path. The Sinc4 filter operates at a fixed OSR = 32 at those settings. The OSR settings of the Sinc1 filter range from 2 to 3200 to yield a combined OSR range from 64 to 102400. Compared to the Sinc3 or Sinc4 filter, the cascaded Sinc4 + Sinc1 filter path provides shorter settling time at the expense of degraded noise performance.

For STEPx_FLTR_OSR[4:0] bit settings 10001b to 11001b, Table 7-6 provides an overview of the resulting output data rates for the various speed modes based on the OSR setting. The data rates scale with f_{CLK}.

Table 7-6. Sinc4 + Sinc1 Filter Output Data Rates

OSR	–3dB Frequency	OUTPUT DATA RATE (f_{DATA})(1)			
		SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
64	0.342× f_{DATA}	500SPS	4kSPS	8kSPS	16kSPS
128	0.410× f_{DATA}	250SPS	2kSPS	4kSPS	8kSPS
256	0.434× f_{DATA}	125SPS	1kSPS	2kSPS	4kSPS
512	0.440× f_{DATA}	62.5SPS	500SPS	1kSPS	2kSPS
640	0.441× f_{DATA}	50SPS	400SPS	800SPS	1.6kSPS
1024	0.442× f_{DATA}	31.25SPS	250SPS	500SPS	1kSPS
2048	0.442× f_{DATA}	15.63SPS	125SPS	250SPS	500SPS
4096	0.442× f_{DATA}	7.81SPS	62.5SPS	125SPS	250SPS
8192	0.442× f_{DATA}	3.91SPS	31.25SPS	62.5SPS	125SPS

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

For STEPx_FLTR_OSR[4:0] bit settings 11010b to 11101b, the device adjusts the OSR setting based on the selected speed mode to achieve the desired output data rates of 10SPS, 16.7SPS, 50SPS or 60SPS in each of the four speed modes. Table 7-7 lists the OSR settings for each speed mode. Because the output data rate scales with the clock frequency, use the internal oscillator or an external clock with a nominal frequency of f_{CLK} = 4.096MHz to achieve the listed data rates.

The digital filter offers 50Hz line-cycle rejection at output data rates of 16.7SPS and 50SPS. At 60SPS, the digital filter offers 60Hz line-cycle rejection. The digital filter rejects both 50Hz and 60Hz line-cycle frequencies at 10SPS. See the *50Hz and 60Hz Line Cycle Rejection* section for more details regarding the device's 50Hz and 60Hz line-cycle rejection capabilities.

Table 7-7. Sinc4 + Sinc1 Filter OSR Settings for Output Data Rates With Line-Cycle Rejection

OUTPUT DATA RATE(1) (f_{DATA})	–3dB Frequency	OSR			
		SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
10SPS	4.4Hz	3200	25600	51200	102400
16.7SPS	7.4Hz	1920	15360	30720	61440
50SPS	22.1Hz	640	5120	10240	20480
60SPS	26.6Hz	544	4256	8544	17056

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

The –3dB frequencies for the various Sinc filter configurations are given in Table 7-6 and Table 7-7.

The frequency response of the combined Sinc4 + Sinc1 filter is given by Equation 10.

$$|H_{(f)}| = \left| \frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^4 \cdot \left| \frac{\sin\left[\frac{AB\pi f}{f_{MOD}}\right]}{B \sin\left[\frac{A\pi f}{f_{MOD}}\right]} \right| \quad (10)$$

where:

- f = Signal frequency
- f_{MOD} = Modulator frequency
- A = Sinc4 filter OSR = 32
- B = Sinc1 filter OSR

Figure 7-5 and Figure 7-6 show examples of the filter frequency responses of the cascaded Sinc4 + Sinc1 filter normalized to the output data rate for Sinc1 OSRs of 4, 8, 16 and 32. A Sinc filter has infinite attenuation at integer multiples of the output data rate except for integer multiples of f_{MOD}. As with all digital filters, the frequency response repeats at integer multiples of the modulator frequency, f_{MOD}. The digital filter provides no attenuation at input frequencies near n × f_{MOD} (n = 1, 2, 3, and so on). The data rate and filter notch frequencies scale with f_{MOD}.

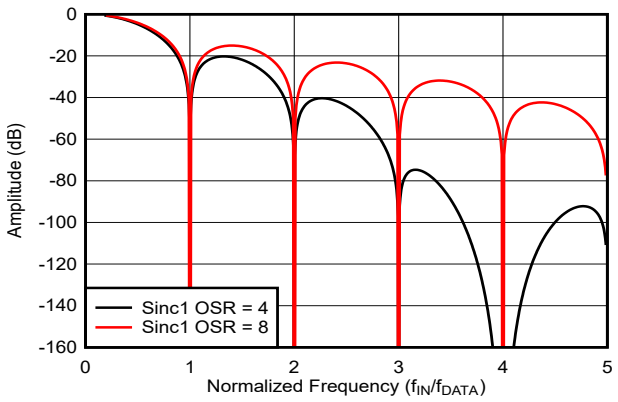


Figure 7-5. Sinc4 + Sinc1 Frequency Response (Sinc4 OSR = 32)

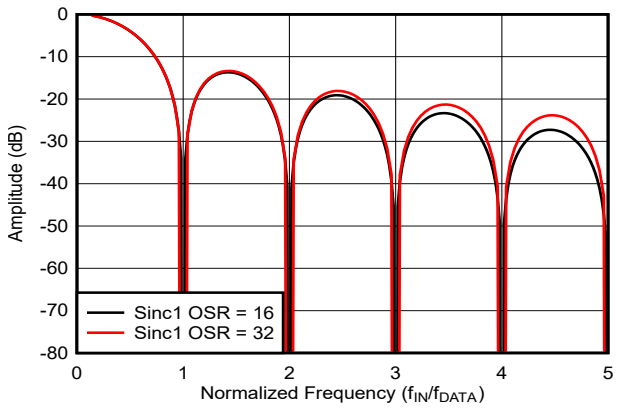


Figure 7-6. Sinc4 + Sinc1 Frequency Response (Sinc4 OSR = 32)

7.3.7.3 FIR Filter

In addition to the Sinc filters, the devices also provide two FIR filter options which offer simultaneous 50Hz and 60Hz line-cycle rejection, while also offering single-cycle settling behavior. Select between a 20SPS and 25SPS data rate option using the STEPx_FLTR_OSR[4:0] bits. The FIR filter adjusts the OSR based on the selected speed mode to provide data rates of 20SPS and 25SPS in all four speed modes as shown in Table 7-8. See the *50Hz and 60Hz Line Cycle Rejection* section for more details regarding the device's 50Hz and 60Hz line-cycle rejection capabilities when using the FIR filters.

Table 7-8. FIR Filter OSR Settings

OUTPUT DATA RATE(1)	–3dB Frequency	OSR			
		SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
20SPS	13.2Hz	1600	12800	25600	51200
25SPS	15.1Hz	1280	10240	20480	40960

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

Figure 7-7 to Figure 7-10 show the filter frequency responses for the two FIR filter configurations. The –3dB frequencies for the two FIR filters are given in Table 7-8.

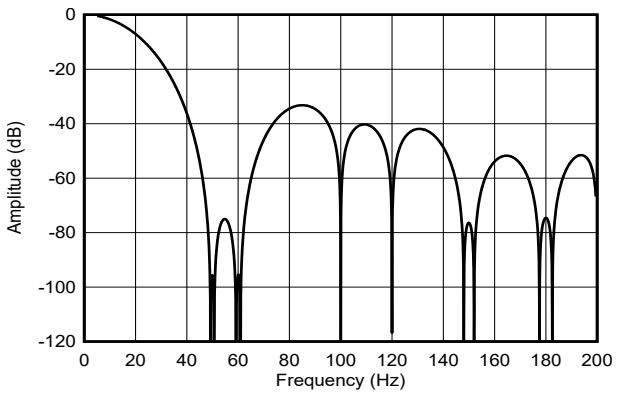


Figure 7-7. 20SPS Frequency Response

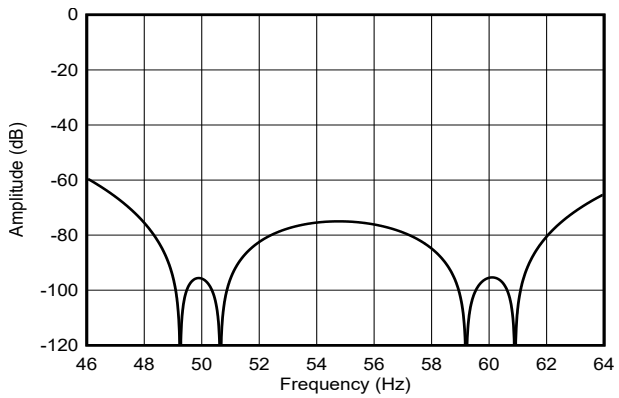


Figure 7-8. 20SPS Frequency Response (Zoomed)

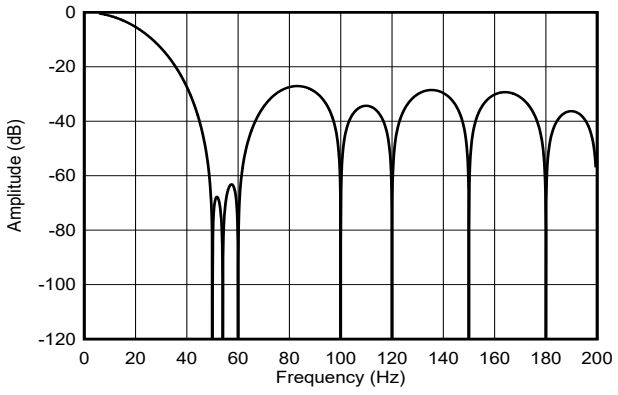


Figure 7-9. 25SPS Frequency Response

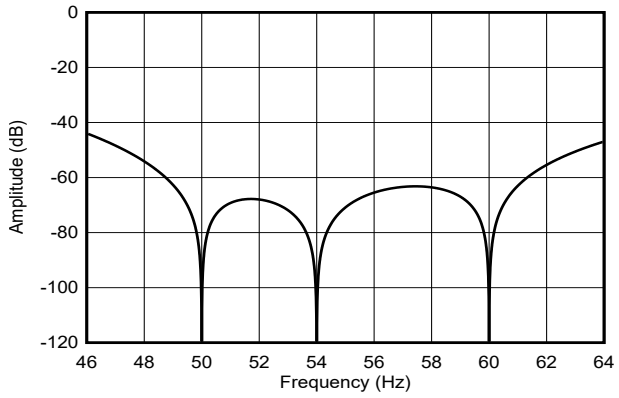


Figure 7-10. 25SPS Frequency Response (Zoomed)

7.3.7.4 50Hz and 60Hz Line Cycle Rejection

The digital filter rejects common 50Hz and 60Hz line-cycle frequencies at specific filter type and data rate settings. Table 7-9 summarizes the normal-mode rejection for those settings assuming a nominal device clock of 4.096MHz with no tolerance, and a line-cycle frequency variation of ±1Hz. When operating the device with the internal oscillator, take the oscillator tolerance into account as shown in the NMRR parameter specifications in the *Electrical Characteristics* table.

Table 7-9. 50Hz and 60Hz Line-Cycle Rejection

FILTER TYPE	OUTPUT DATA RATE(1) (f_{DATA})	NMRR	
		50Hz ±1Hz	60Hz ±1Hz
Sinc4	10SPS	136dB	142dB
	16.7SPS	135dB	86dB
	50SPS	135dB	–
	60SPS	–	137dB
Sinc3	10SPS	102dB	107dB
	16.7SPS	102dB	65dB
	50SPS	101dB	–
	60SPS	–	103dB
Sinc4 + Sinc1	10SPS	34dB	36dB
	16.7SPS	34dB	22dB
	50SPS	34dB	–
	60SPS	–	35dB
FIR	20SPS	95dB	102dB
	25SPS	63dB	63dB

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

7.3.7.5 Digital Filter Latency

When the sequencer selects a new sequence step for conversions, the digital filter resets and requires a certain amount of time to provide settled output data. This time is called the latency time. The ADS1x4S1x hide the unsettled data internally and only indicate when settled conversion data are available, by transitioning the $\overline{DRDY}$ pin low and setting the DRDY bit to 1b. The conversion period for the second and all subsequent conversions within a sequence step equals t_{DATA} = 1 / f_{DATA} = OSR / f_{MOD} as shown in Figure 7-11.

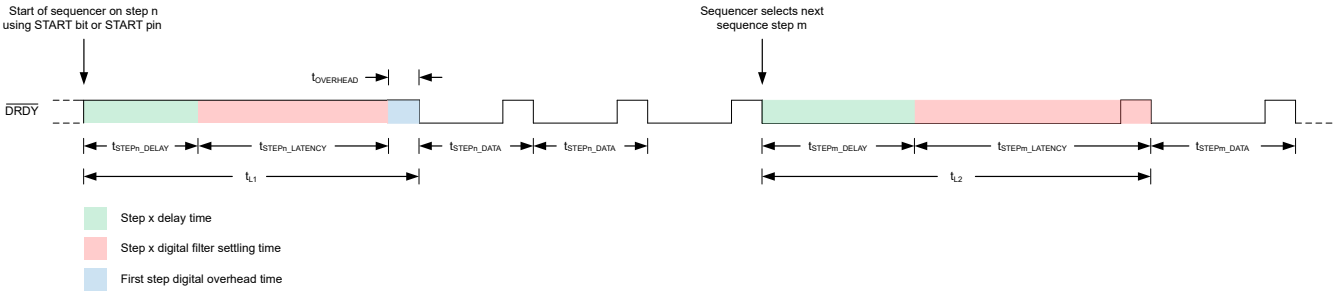


Figure 7-11. Latency Time and Conversion Period

The first conversion of the first sequence step after starting or restarting the sequencer using the START bit or START pin has a latency of t_{L1} as shown in Figure 7-11. Latency time t_{L1} is measured from the $\overline{CS}$ rising edge of the register write frame where the START bit is set to 1b or the START pin rising edge, to the first $\overline{DRDY}$ falling edge. Because the $\overline{CS}$ signal in the SPI clock domain is latched by the digital filter logic running on the modulator clock domain, the latency times calculated using Equation 11 have an uncertainty of ±1 t_{MOD}.

When operating the sequencer in mode SEQ_MOD[1:0] = 10b or 11b, the first conversion of the second and all subsequent sequence steps has a latency of t_{L2} as shown in Figure 7-11. Latency time t_{L2} is measured from the $\overline{DRDY}$ falling edge of the last conversion of the previous sequence step to the $\overline{DRDY}$ falling edge of the first conversion of the new sequence step as shown in Figure 7-11.

In addition, a per-step programmable delay time can be added to delay the start of the conversion cycle when the sequencer selects a new sequence step. This delay time allows for settling of external components, such as the voltage reference after exiting standby mode, or for additional settling time when the sequencer switches from one sequence step to the next one with a different device configuration. The delay time is only added before the first conversion of a sequence step as shown in Figure 7-11. Subsequent conversions within the sequence step are not delayed. Use the STEPx_DELAY[6:0] bits to configure individual delay times for each sequence step.

The time to complete the first conversion of the first sequence step after starting or restarting the sequencer follows Equation 11.

When using sequencer modes SEQ_MODE[1:0] = 10b or 11b, the time to complete the first conversion of the second and all subsequent sequence steps follows Equation 12.

$$t_{L1} = t_{STBY\_DELAY} + t_{STEPx\_DELAY} + t_{OVERHEAD} + t_{STEPx\_LATENCY} \quad (11)$$

$$t_{L2} = t_{STEPx\_DELAY} + t_{STEPx\_LATENCY} \quad (12)$$

where:

- $t_{STEPx\_LATENCY}$ is the latency time provided in Table 7-10 and Table 7-11
- t_{STEPx_DELAY} is the delay time determined by the STEPx_DELAY[6:0] bits
- t_{STBY_DELAY} = 0 when starting the sequencer from idle mode (STBY_MODE = 0b).
  When starting the sequencer from standby mode (STBY_MODE = 1b), the device adds a speed-mode dependent delay time before the user-programmable delay time to allow internal circuits to wake-up:
  - t_{STBY_DELAY} = 5 t_{MOD} (Speed Mode 0)
  - t_{STBY_DELAY} = 27 t_{MOD} (Speed Mode 1, Speed Mode 2)
  - t_{STBY_DELAY} = 35 t_{MOD} (Speed Mode 3)
- $t_{OVERHEAD}$ = 11 t_{MOD}

Table 7-10. Latency for Sinc Filters With OSR Settings

OSR	LATENCY IN t_{MOD} (1) (ABSOLUTE TIME(2))			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 00000b to 01100b)				
8	38 (1.188ms)	46 (0.180ms)	46 (0.090ms)	62 (0.061ms)
16	70 (2.188ms)	78 (0.305ms)	78 (0.152ms)	94 (0.092ms)
24	102 (3.188ms)	110 (0.430ms)	110 (0.215ms)	126 (0.123ms)
32	134 (4.188ms)	142 (0.555ms)	142 (0.277ms)	158 (0.154ms)
64	262 (8.188ms)	270 (1.055ms)	270 (0.527ms)	286 (0.279ms)
128	518 (16.19ms)	526 (2.055ms)	526 (1.027ms)	542 (0.529ms)
256	1030 (32.19ms)	1038 (4.055ms)	1038 (2.027ms)	1054 (1.029ms)
512	2054 (64.19ms)	2062 (8.055ms)	2062 (4.027ms)	2078 (2.029ms)
640	2566 (80.19ms)	2574 (10.05ms)	2574 (5.027ms)	2590 (2.529ms)
1024	4102 (128.2ms)	4110 (16.05ms)	4110 (8.027ms)	4126 (4.029ms)
2048	8198 (256.2ms)	8206 (32.05ms)	8206 (16.03ms)	8222 (8.029ms)
4096	16390 (512.2ms)	16398 (64.05ms)	16398 (32.03ms)	16414 (16.03ms)
8192	32774 (1024ms)	32782 (128.1ms)	32782 (64.03ms)	32798 (32.03ms)
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 00000b to 01100b)				
8	30 (0.938ms)	38 (0.148ms)	38 (0.074ms)	54 (0.053ms)
16	54 (1.688ms)	62 (0.242ms)	62 (0.121ms)	78 (0.076ms)
24	78 (2.438ms)	86 (0.336ms)	86 (0.168ms)	102 (0.100ms)
32	102 (3.188ms)	110 (0.430ms)	110 (0.215ms)	126 (0.123ms)
64	198 (6.188ms)	206 (0.805ms)	206 (0.402ms)	222 (0.217ms)
128	390 (12.19ms)	398 (1.555ms)	398 (0.777ms)	414 (0.404ms)
256	774 (24.19ms)	782 (3.055ms)	782 (1.527ms)	798 (0.779ms)
512	1542 (48.19ms)	1550 (6.055ms)	1550 (3.027ms)	1566 (1.529ms)
640	1926 (60.19ms)	1934 (7.555ms)	1934 (3.777ms)	1950 (1.904ms)
1024	3078 (96.19ms)	3086 (12.05ms)	3086 (6.027ms)	3102 (3.029ms)
2048	6150 (192.2ms)	6158 (24.05ms)	6158 (12.03ms)	6174 (6.029ms)
4096	12294 (384.2ms)	12302 (48.05ms)	12302 (24.03ms)	12318 (12.03ms)
8192	24582 (768.2ms)	24590 (96.05ms)	24590 (48.03ms)	24606 (24.03ms)
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 10001b to 11001b)				
64	166 (5.188ms)	174 (0.680ms)	174 (0.340ms)	190 (0.186ms)
128	230 (7.188ms)	238 (0.930ms)	238 (0.465ms)	254 (0.248ms)
256	358 (11.19ms)	366 (1.430ms)	366 (0.715ms)	382 (0.373ms)
512	614 (19.19ms)	622 (2.430ms)	622 (1.215ms)	638 (0.623ms)
640	742 (23.19ms)	750 (2.930ms)	750 (1.465ms)	766 (0.748ms)
1024	1126 (35.19ms)	1134 (4.430ms)	1134 (2.215ms)	1150 (1.123ms)
2048	2150 (67.19ms)	2158 (8.430ms)	2158 (4.215ms)	2174 (2.123ms)
4096	4198 (131.2ms)	4206 (16.43ms)	4206 (8.215ms)	4222 (4.123ms)
8192	8294 (259.2ms)	8302 (32.43ms)	8302 (16.21ms)	8318 (8.123ms)

(1) $t_{MOD} = 1 / f_{MOD}$.
(2) Based on a nominal clock frequency of f_{CLK} = 4.096MHz.

Table 7-11. Latency for Sinc and FIR Filters With Fixed Data Rate Settings

OUTPUT DATA RATE	LATENCY IN t_{MOD} (1) (ABSOLUTE TIME(2))			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
SINC4 FILTER (STEPx_FLTR_MODE = 0b, STEPx_FLTR_OSR[4:0] = 01101b to 10000b)				
10SPS	2134 (66.69ms)	17038 (66.55ms)	34062 (66.53ms)	68126 (66.53ms)
16.7SPS	2566 (80.19ms)	20494 (80.05ms)	40974 (80.03ms)	81950 (80.03ms)
50SPS	7686 (240.2ms)	61454 (240.1ms)	122894 (240.0ms)	245790 (240.0ms)
60SPS	12806 (400.2ms)	102414 (400.1ms)	204814 (400.0ms)	409630 (400.0ms)
SINC3 FILTER (STEPx_FLTR_MODE = 1b, STEPx_FLTR_OSR[4:0] = 01101b to 10000b)				
10SPS	1602 (50.06ms)	12782 (49.93ms)	25550 (49.90ms)	51102 (49.90ms)
16.7SPS	1926 (60.19ms)	15374 (60.05ms)	30734 (60.03ms)	61470 (60.03ms)
50SPS	5766 (180.2ms)	46094 (180.1ms)	92174 (180.0ms)	184350 (180.0ms)
60SPS	9606 (300.2ms)	76814 (300.1ms)	153614 (300.0ms)	307230 (300.0ms)
SINC4 + SINC1 FILTER (STEPx_FLTR_OSR[4:0] = 11010b to 11101b)				
10SPS	646 (20.19ms)	4366 (17.05ms)	8654 (16.90ms)	17182 (16.78ms)
16.7SPS	742 (23.19ms)	5230 (20.43ms)	10350 (20.21ms)	20606 (20.12ms)
50SPS	2022 (63.2ms)	15470 (60.4ms)	30830 (60.2ms)	61566 (60.1ms)
60SPS	3302 (103.2ms)	25710 (100.4ms)	51310 (100.2ms)	102526 (100.1ms)
FIR FILTER (STEPx_FLTR_OSR[4:0] = 11110b to 11111b)				
20SPS	1726 (53.94ms)	12934 (50.52ms)	25734 (50.26ms)	51350 (50.15ms)
25SPS	1406 (43.94ms)	10374 (40.52ms)	20614 (40.26ms)	41110 (40.15ms)

(1) $t_{MOD} = 1 / f_{MOD}$.
(2) Based on a nominal clock frequency of f_{CLK} = 4.096MHz.

7.3.7.6 Global-Chop Mode

The signal chain of the ADS1x4S1x uses a very low-drift, chopper-stabilized PGA and delta-sigma modulator to provide very low offset error and offset drift. However, a small amount of offset drift remains in normal measurement. For that reason, the devices incorporate an optional global-chop mode to reduce offset error and offset drift over both temperature and time to exceptionally low levels. When the global-chop mode is enabled by setting the GC_EN bit, the device performs two consecutive conversions with alternate input signal polarity to cancel offset error. The first conversion is taken with normal input polarity. The global-chop control logic inverts the input polarity and resets the digital filter for the second conversion. The average of the two conversions yields the final offset-corrected result. Figure 7-12 illustrates a block diagram of the global-chop implementation. V_{OFS} models the combined PGA and ADC internal offset voltage. Only this device-inherent offset voltage is reduced by the global-chop mode. Any offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.

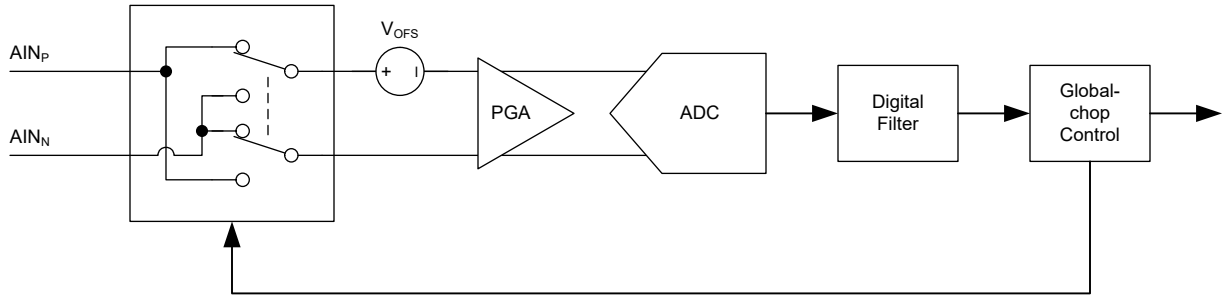


Figure 7-12. Global-Chop Mode Control Diagram

The operational sequence of global-chop mode is as follows:

- Conversion C1: $V_{AINP} – V_{AINN} – V_{OFS}$ → First conversion withheld after conversion start
- Conversion C2: $V_{AINN} – V_{AINP} – V_{OFS}$ → Output 1 = $(V_{C1} – V_{C2}) / 2 = V_{AINP} – V_{AINN}$
- Conversion C3: $V_{AINP} – V_{AINN} – V_{OFS}$ → Output 2 = $(V_{C3} – V_{C2}) / 2 = V_{AINP} – V_{AINN}$
- ...

The first conversion result (Output 1) of a new sequence step is available after the device performed two settled conversions. Consequently, the latency times, t_{GC_L1} and t_{GC_L2}, when global-chop mode is enabled are longer compared to the latency times when global-chop mode is disabled. The latency times are measured in the same way as explained in the *Digital Filter Latency* section.

The time to output the first conversion result of the first sequence step after starting or restarting the sequencer follows Equation 13.

When using sequencer modes SEQ_MODE[1:0] = 10b or 11b, the time to output the first conversion result of the second and all subsequent sequence steps follows Equation 14.

Subsequent conversions on the same sequence step complete in t_{GC_DATA}, as calculated by Equation 15.

$$t_{GC\_L1} = t_{STBY\_DELAY} + 2 \times (t_{STEPx\_DELAY} + t_{STEPx\_LATENCY}) + t_{OVERHEAD} \quad (13)$$

$$t_{GC\_L2} = 2 \times (t_{STEPx\_DELAY} + t_{STEPx\_LATENCY}) \quad (14)$$

$$t_{GC\_DATA} = t_{STEPx\_DELAY} + t_{STEPx\_LATENCY} \quad (15)$$

where:

- $t_{STEPx\_LATENCY}$ is the latency time provided in Table 7-10 and Table 7-11
- t_{STEPx_DELAY} is the delay time determined by the STEPx_DELAY[6:0] bits
- t_{STBY_DELAY} = 0 when starting the sequencer from idle mode (STBY_MODE = 0b).
  When starting the sequencer from standby mode (STBY_MODE = 1b), the device adds a speed-mode dependent delay time before the user-programmable delay time to allow internal circuits to wake-up:
  - t_{STBY_DELAY} = 5 t_{MOD} (Speed Mode 0)
  - t_{STBY_DELAY} = 27 t_{MOD} (Speed Mode 1, Speed Mode 2)
  - t_{STBY_DELAY} = 35 t_{MOD} (Speed Mode 3)
- $t_{OVERHEAD}$ = 11 t_{MOD}

The device waits the programmable delay time after inverting the input polarity before starting the next conversion, to allow for the internal circuitry to settle. In some cases, the programmable delay time must be increased to allow for settling of external components.

Global-chop mode reduces the ADC noise by a factor of $\sqrt{2}$ because two conversions are averaged. Divide the input-referred noise values in Table 6-1 to Table 6-8 by $\sqrt{2}$ to derive the noise performance when global-chop mode is enabled.

The digital filter notches do not change in global-chop mode. However, additional filter notches appear at multiples of f_{GC_DATA} / 2.

7.3.8 Excitation Current Sources (IDACs)

The devices incorporate two programmable, matched current sources (IDAC1 and IDAC2). The current sources provide excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing. Each current source is independently programmable to output values between 1µA to 1mA.

Use the STEPx_I1MAG[3:0] and STEPx_I2MAG[3:0] bits in combination with the STEPx_IUNIT[1:0] bit to set the desired output current for each IDAC. The STEPx_IUNIT bit sets the base current for both IDAC1 and IDAC2 to either 1µA or 10µA. The STEPx_I1MAG[3:0] and STEPx_I2MAG[3:0] bits act as multipliers of that base current to configure the individual IDAC1 and IDAC2 output currents.

Best matching between current sources is achieved when both IDACs are set to the same current value. In three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *Software-Configurable RTD Measurement Input* section for more details).

Each current source can be routed to any of the analog inputs AINx using the STEPx_I1MUX[4:0] and STEPx_I2MUX[4:0] bits. Both current sources can also be combined onto the same pin by setting STEPx_I1MUX[4:0] and STEPx_I2MUX[4:0] to the same bit values, if excitation current values up to 2mA are required. On ADS1x4S18, analog inputs AIN8 to AIN17 can be configured as analog inputs, reference inputs, or GPIOs irrespective of the IDAC routing. A pin that is selected as a current source output can still be used as an analog or reference input at the same time. Figure 7-1 shows the IDAC connections through the input multiplexer.

The current sources require voltage headroom to the AVDD supply to operate. This voltage headroom is also called the compliance voltage. When driving resistive loads, take care not to exceed the compliance voltage of the IDACs, otherwise the specified accuracy of the IDAC current is not always met. For the IDAC compliance voltage specifications, see the *Electrical Characteristics* table.

The IDACs remain active in idle mode, but turn off in standby and power-down mode.

7.3.9 Burn-Out Current Sources (BOCS)

To help detect potential sensor faults, the ADS1x4S1x provide a pair of programmable burn-out current sources (BOCS). Use the STEPx_BOCS[1:0] bits to enable the current sources and to set the values to 0.2µA, 1µA, or 10µA.

The BOCS connect to the PGA inputs after the internal multiplexer. When enabled, one BOCS sources current from AVDD to the selected positive analog input (AINP) and the other BOCS sinks current from the selected negative analog input (AINN) to AVSS.

In case of an open-circuit in the external sensor or a sensor wire disconnection, these BOCS pull the positive input toward AVDD and the negative input toward AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent.

A near-zero reading can indicate a shorted sensor. Distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. The current sources create a voltage drop across the external filter resistors and the residual resistance of the internal multiplexer. That means, even when the sensor is shorted, a small voltage is present at the PGA inputs and the ADC consequently outputs a voltage larger than zero. The residual resistance of the internal multiplexer typically ranges from about 400Ω at AVDD = 3.3V to 1.6kΩ at AVDD = 1.8V.

The ADC readings of a functional sensor can be corrupted when the burn-out current sources are enabled. Therefore, disable the burn-out current sources when performing precision measurements, and only enable the BOCS to test for sensor fault conditions during a dedicated diagnostic measurement.

Disable the BOCS when using global-chop mode (GC_EN = 1b). The burn-out current source function is not compatible with global-chop mode.

The burn-out current sources remain active in idle mode, but turn off in standby and power-down mode.

7.3.10 Bias Voltage Generator (VBIAS)

The ADS1x4S1x integrate a bias voltage generator, VBIAS, which provides a buffered voltage equal to half the analog supply voltage, (AVDD + AVSS) / 2. The bias voltage can be established on the analog inputs AIN0 to AIN7 using the VBIAS_AINx bits. VBIAS can be routed to multiple analog inputs at the same time. The purpose of the bias voltage is to shift the signal level of floating sensors, such as isolated thermocouples, to within the input range of the PGA. Connect one lead of the floating sensor to an analog input that has VBIAS enabled.

The start-up time of the bias voltage generator depends on the pin load capacitance. The total capacitance includes any capacitance connected from VBIAS to AVDD, AVSS, and ground. Table 7-12 lists typical VBIAS voltage settling times for various external load capacitances. Make sure the VBIAS voltage is fully settled before starting a conversion.

Table 7-12. VBIAS Settling Time

LOAD CAPACITANCE	SETTLING TIME
0.1µF	200µs
1µF	2.5ms
10µF	12ms

7.3.11 General Purpose IOs (GPIOs)

The ADS1x4S1x provide eight general purpose inputs and outputs (GPIOs). The logic levels of those GPIOs are referenced to the AVDD and AVSS supply. On ADS1x4S18 the GPIOs are shared with analog inputs. Use the GPIOx_CFG[1:0] (x = 0 to 7) bits to configure the pins as either analog inputs, digital inputs or digital outputs with either push-pull or open-drain characteristic.

Set the digital output levels of the GPIOs using the STEPx_GPIOx_DAT_OUT bits. The STEPx_GPIOx_DAT_OUT bit setting has no effect when GPIOx is configured as an analog or digital input.

The GPIOx_DAT_IN bits indicate the readback values at the GPIOx pins irrespective if the pins are configured as digital inputs or outputs. The GPIOx_DAT_IN bits read back 0b when GPIOx is configured as an analog input.

In addition, the following special functions are available:

- GPIO3 can be configured as a digital comparator ALERT output.
- GPIO4 can be configured as a $\overline{\text{FAULT}}$ indication output.

In power-down mode, any analog inputs configured as GPIO digital outputs transition into a Hi-Z state. To maintain a certain GPIO logic level during power-down, consider external pullup or pulldown resistors on the respective GPIO pins.

7.3.11.1 ALERT Output

Configure GPIO3 as the digital comparator ALERT output by setting GPIO3_CFG = 10b or 11b and GPIO3_SRC = 1b. The COMP_ALERTn flag determines the GPIO3/ALERT output state in that case. The ALERT pin can be configured as an active-low or active-high output depending on the application requirements. Select the polarity of the ALERT output pin using the ALERT_PIN_POL bit. See Table 7-13 for details.

Table 7-13. ALERT Output State Diagram

ALERT_PIN_POL BIT	COMP_ALERTn FLAG	ALERT OUTPUT
0b	0b	Low
1b	0b	High
0b	1b	High
1b	1b	Low

7.3.11.2 $\overline{\text{FAULT}}$ Output

Configure GPIO4 as a $\overline{\text{FAULT}}$ output by setting GPIO4_CFG = 10b or 11b and GPIO4_SRC = 1b. The $\overline{\text{FAULT}}$ pin is low when the SAD_FAULTn status bit is 0b to indicate a fault. Connect a pulldown resistor from GPIO4 to DGND to also detect potential device resets because the pin reverts back to a high-Z analog input during and after reset.

Use the FAULT_PIN_BEHAVIOR bit to select from the following $\overline{\text{FAULT}}$ output behaviors:

- Static output. The $\overline{\text{FAULT}}$ output is low when a fault occurred, otherwise the output is high.
- Heart beat output. The $\overline{\text{FAULT}}$ output is low when a fault occurred, otherwise the output is a 50% duty-cycle signal with a frequency of f_{MOD} / 256. The heart beat signal frequency can be monitored by the host to detect potential device clock faults.

7.3.12 Offset and Gain Calibration Coefficients

The ADS1x4S1x provide the ability to correct for offset and gain errors for each sequence step by using user-programmable offset and gain calibration registers (STEPx_OFFSET_CAL[23:0], STEPx_GAIN_CAL[15:0]). As shown in Figure 7-13, the 24-bit offset correction value is subtracted from the conversion data before being multiplied by the 16-bit gain correction value. The output data are rounded to the final resolution, 16 bit for the ADS114S1x or 24 bit for the ADS124S1x, and clipped to +FS and –FS code values after the scaling operation. The offset and gain calibration coefficients must be stored in external nonvolatile memory and programmed into the offset and gain calibration registers each time the device powers up or resets because the ADS1x4S1x registers are volatile.

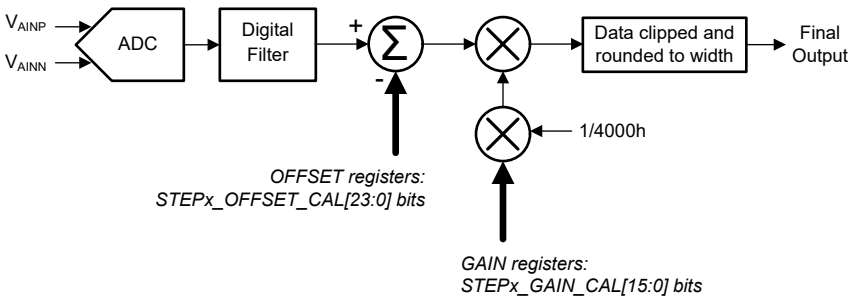


Figure 7-13. Calibration Logic Block Diagram

Equation 16 shows how conversion data are calibrated:

$$\text{Final Output Data} = (\text{Data} - \text{OFFSET}) \times \text{GAIN} / 4000\text{h} \quad (16)$$

The 24-bit offset calibration value is always provided in two's-complement format, irrespective of the STEPx_CODING bit setting, and programmed into the STEPx_OFFSET_CAL[23:0] bit field that spans across the STEPx_OFFSET_CAL_MSB, STEPx_OFFSET_CAL_ISB and STEPx_OFFSET_CAL_LSB registers. For the 16-bit devices, ADS114S1x, set the STEPx_OFFSET_CAL_LSB register to 00h. Table 7-14 shows example offset calibration values. The LSB size of the offset calibration value is calculated using Equation 17.

$$\text{Offset Calibration LSB Size} = (2 \times V_{REF}) / (2^{24}) \quad (17)$$

Table 7-14. Offset Calibration Value Examples

STEPx_OFFSET_CAL[23:0] VALUE	APPLIED OFFSET CORRECTION
000010h	–16LSB
000001h	–1LSB
FFFFFFh	1LSB
FFFFF0h	16LSB

The 16-bit gain calibration value is provided in straight binary format normalized to unity gain at 4000h. The gain calibration value is programmed into the STEPx_GAIN_CAL[15:0] bit field. One LSB of the gain calibration value equals a gain correction factor of $1/2^{16} = 0.000015$. For example, to correct a gain error greater than 1, the calculated gain calibration value is less than 4000h.

Table 7-15 shows example gain calibration values.

Table 7-15. Gain Calibration Value Examples

STEPx_GAIN_CAL[15:0] VALUE	APPLIED GAIN CORRECTION
FFFFh	3.999939
4333h	1.05
4001h	1.000015
4000h	1
3FFFh	0.999985
3CCCh	0.95

The devices ignore the STEPx_OFFSET_CAL[23:0] and STEPx_GAIN_CAL[15:0] values when a system monitor is selected for measurement of the respective sequence step. That is, when STEPx_SYS_MON[2:0] is set to a value other than 000b.

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to STEPx_OFFSET_CAL[23:0] = 000000h and STEPx_GAIN_CAL[15:0] = 4000h, respectively.
2. Perform an offset calibration by shorting the ADC inputs internally using the respective system monitor setting (STEPx_SYS_MON[2:0] = 001b), or short the inputs externally at the system level to include the offset error of the external filter stages. Acquire multiple conversion data and write the average value of the data into the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy. Remember to convert the measured offset value to binary two's complement format in case unipolar straight binary format is used for the measurement (STEPx_CODING = 1b).
3. Perform a gain calibration by applying a precision calibration signal to the ADC inputs or at the system level to include the gain error of the external filter stages. Select the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 2.4V calibration signal with V_{REF} = 2.5V. Use Equation 18 to calculate the gain calibration value.

$$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \times 4000h \quad (18)$$

For example, the expected output code for a 2.4V calibration voltage using a 2.5V reference voltage and gain = 1 is: (2.4V / LSB size) = 7AE148h, where LSB size = 2 × 2.5V / (2^{24}). If the actual measured output code is 75750h for example, then the gain calibration factor calculates to 1.05. The resulting gain calibration value to write into the STEPx_GAIN_CAL[15:0] bit field is: (1.05 – 1) / (1 / 2^{16}) = 4333h.

7.3.13 Digital Comparator

The ADS1x4S1x provide a digital comparator function that can be individually configured for every sequence step. Configure the comparator high and low thresholds using the STEPx_COMP_HIGH_TH[15:0] and STEPx_COMP_LOW_TH[15:0] bit fields. The STEPx_COMP_HIGH_TH_EN and STEPx_COMP_LOW_TH_EN bits determine which thresholds the comparator triggers on. Enable both the high and low threshold to implement a window comparator function.

The comparator compares each conversion result of a sequence step against the enabled threshold. If a conversion result exceeds the threshold, an internal alert counter increments. This internal alert counter resets whenever a conversion result of this step falls below the threshold. The alert counter also resets with the start of every sequence step or when the COMP_ALERTn flag is cleared. The digital comparator trips when the alert counter equals the number programmed in the STEPx_COMP_NUM[1:0] bit field. That means, the number

programmed in the STEPx_COMP_NUM[1:0] bit field determines how many *consecutive* conversions on one sequence step need to exceed the threshold before tripping the comparator. When the comparator on any of the sequence steps trips, the COMP_ALERTn bit sets to 0b and the COMP_ALERT_STEP_INDICATOR[4:0] indicates which sequence step triggered the comparator alert.

The COMP_ALERTn flag is latching. After the overrange condition is removed, the host needs to write 1b to the COMP_ALERTn bit to clear the bit to 1b. The COMP_ALERT_STEP_INDICATOR[4:0] clears to 11111b at the same time.

The SAD_FAULTn flag also sets to 0b when the COMP_ALERTn flag is 0b, unless the COMP_ALERTn_MASK bit is set to 1b to mask the COMP_ALERTn flag from driving the SAD_FAULTn flag.

Table 7-16 summarizes the register bits that control the digital comparator behavior. For more details see the respective bit field descriptions in the *Register Map* section.

Table 7-16. Digital Comparator Status and Configuration Bits

REGISTER BITS	DESCRIPTION
Status and General Configuration Page	
COMP_ALERTn	The digital comparator alert flag indicates that the digital comparator on one of the sequence steps tripped.
COMP_ALERT_STEP_INDICATOR[4:0]	The digital comparator alert step indicator indicates which sequence step caused the comparator overrange condition when the COMP_ALERTn flag is 0b.
COMP_ALERTn_MASK	The COMP_ALERTn fault mask bit determines whether the COMP_ALERTn flag contributes to the SAD_FAULTn flag or not.
Step x Configuration Pages	
STEPx_COMP_HIGH_TH_EN	Enables the digital comparator high threshold detection for sequence step x.
STEPx_COMP_LOW_TH_EN	Enables the digital comparator low threshold detection for sequence step x.
STEPx_COMP_HIGH_TH[15:0]	Sets the digital comparator high threshold for sequence step x. Conversion results larger than the high threshold increment the internal alert counter.
STEPx_COMP_LOW_TH[15:0]	Sets the digital comparator low threshold for sequence step x. Conversion results smaller than the low threshold increment the internal alert counter.
STEPx_COMP_NUM[1:0]	The comparator alert counter threshold determines the number of consecutive conversions the conversion results of sequence step x need to exceed the comparator threshold before the device indicates an alert through the COMP_ALERTn flag.

Figure 7-14 illustrates the digital comparator behavior for a sequence step with 16 conversions, the comparator high threshold enabled, and the comparator alert counter threshold set to 4 (STEPx_NUM_CONV[4:0] = 01111b, STEPx_COMP_HIGH_TH_EN = 1b, STEPx_COMP_NUM[1:0] = 10b).

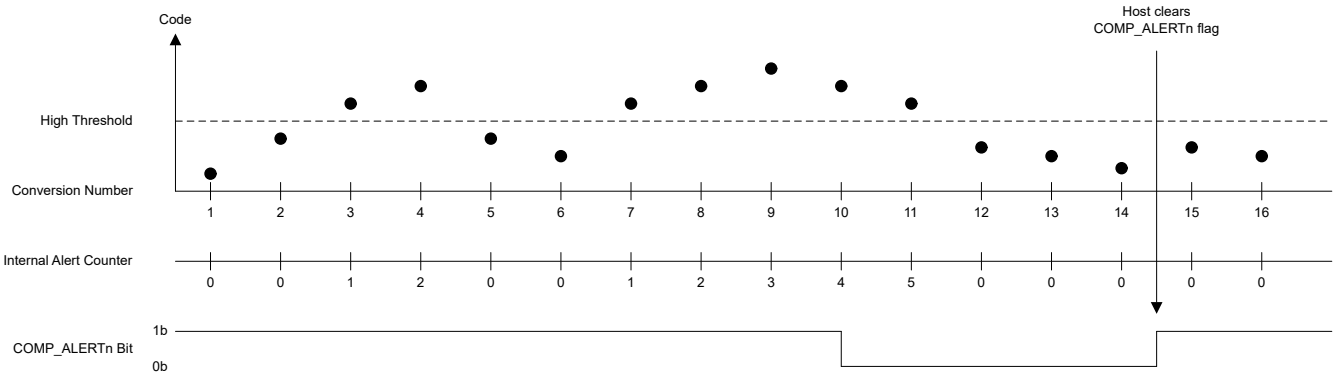


Figure 7-14. Digital Comparator Behavior

In addition to the COMP_ALERTn flag, GPIO3 can be configured as an ALERT output pin to indicate a tripped comparator as explained in the *ALERT Output* section.

7.3.14 System Monitors

The devices offer a set of system monitoring functions which can be routed to the PGA inputs internally for measurement through the input multiplexer. Use the STEPx_SYS_MON[2:0] bits to select from one of the following system monitors:

- The inputs of the PGA can be shorted together to mid-supply, (AVDD + AVSS) / 2, to measure and calibrate the input offset of the internal signal chain.
- An integrated temperature sensor that provides an output signal proportional to the device temperature.
- Any of the two attenuated external reference voltages, (V_{REFPx} – V_{REFNx}) / 8
- The attenuated analog and digital supplies, ((AVDD – AVSS) / 8), (IOVDD / 8), and (V_{DLDO} / 4).

The STEPx_AINP[4:0] and STEPx_AINN[4:0] bits have no effect and the analog inputs are disconnected from the PGA when one of the system monitors is selected. The voltage reference selected by the STEPx_REF_SEL[1:0] bits is used for the system monitor measurements. When monitoring one of the external voltage references or the analog supply, select a voltage reference which is different from the monitored voltage. Select an appropriate gain setting using the STEPx_GAIN[3:0] bits for each measurement.

The user offset and gain calibration register values (STEPx_OFFSET_CAL[23:0], STEPx_GAIN_CAL[15:0]) are not applied to the conversion results when measuring one of the system monitors.

7.3.14.1 Internal Short (Offset Calibration)

The system monitor offers the option to short both PGA inputs (AINP and AINN) to mid-supply, (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset. Take multiple readings with the inputs shorted and average the result to reduce the effect of noise. Store the measured offset value in the STEPx_OFFSET_CAL[23:0] bit field. The device then automatically subtracts the value from each conversion result of sequence step x. Alternatively, store the offset value in a microcontroller and consequently subtract the value from each conversion result.

7.3.14.2 Internal Temperature Sensor

The ADS1x4S1x provide an integrated temperature sensor (TS) to measure the die temperature. The temperature sensor outputs a voltage that is proportional to the die temperature. The output voltage characteristic (TS_{Offset}, TS_{TC}) of the temperature sensor is specified in the *Electrical Characteristics* table.

Equation 19 shows how to convert the measured temperature sensor output voltage to die temperature:

$$\text{Die temperature [°C]} = 25°C + (\text{Measured voltage} - TS_{Offset}) / TS_{TC} \quad (19)$$

Select a gain setting for the PGA so that the maximum temperature sensor output voltage that can occur in the application is smaller than V_{REF} / Gain.

7.3.14.3 External Reference Voltage Readback

The system monitor allows to monitor either of the two external reference voltages connected between the REFP0 and REFN0, or REFP1 and REFN1 pins. For this purpose, select the according attenuated external reference voltage, (V_{REFPx} – V_{REFNx}) / 8 for measurement.

7.3.14.4 Power-Supply Readback

The system monitor allows to monitor both the analog and digital supplies. For this purpose, select either the attenuated analog supply ((AVDD – AVSS) / 8), the attenuated digital IO supply (IOVDD / 8), or the digital core supply (V_{DLDO} / 4) for measurement.

7.3.15 Monitors and Status Flags

The ADS1x4S1x provide a set of monitors with corresponding status flags to detect and indicate specific device or system faults to the host. Table 7-17 provides an overview of the available monitors. Some monitors need to be enabled using a dedicated monitor enable bit. If a monitor detects a fault, the according low-active fault flag is set to 0b. Except for the communication-related monitor fault flags, the fault flags must be cleared to 1b by the host after the fault condition is removed. The monitor fault flags are available in the various STATUS registers for readout.

Table 7-17. Monitor Overview

MONITOR NAME	MONITOR ENABLE BIT	MONITOR FAULT FLAG	FAULT FLAG RESET MECHANISM
Reset	N/A	RESETn	Write 1b to clear bit to 1b
AVDD Undervoltage	N/A	AVDD_UVn	Write 1b to clear bit to 1b
Reference Undervoltage	REF_UV_EN	REF_UVn	Write 1b to clear bit to 1b
SPI CRC	SPI_CRC_EN	SPI_CRC_FAULTn	Updates in every new SPI frame based on the CRC result of the previous SPI frame
Register Map CRC	REG_MAP_CRC_EN	REG_MAP_CRC_FAULTn	Write 1b to clear bit to 1b
Memory Map CRC	N/A	MEM_FAULTn	Reset or power-cycle the device
Register Write Fault	N/A	REG_WRITE_FAULTn	Updates with the next register write command
Digital Comparator	STEPx_COMP_LOW_TH_EN, STEPx_COMP_HIGH_TH_EN	COMP_ALERTn	Write 1b to clear bit to 1b

In addition to the monitor flags, the various STATUS registers include additional status and indicator bits as listed in Table 7-18. See the respective bit descriptions in the *Status and General Configuration Page Registers* section for more details.

Table 7-18. Status and Indicator Bits Overview

NAME	BITs	DESCRIPTION
Supply, ADC, and Digital Fault Aggregate Flag	SAD_FAULTn	Indicates if any of the individual fault flags in the SUPPLY_STATUS, ADC_STATUS, or DIGITAL_STATUS registers are set.
DRDY Indicator	DRDY	Indicates if the conversion data read within the current SPI frame are new or are repeated data from the last read operation.
Sequencer Step Indicator	STEP_INDICATOR[4:0]	Indicates the step page configuration that was used for the latest conversion result, which is currently available for readout.
Conversion Counter	CONV_COUNT[3:0]	A counter that increments with every new conversion to keep track of the conversion which is currently available for readout.
Sequence Counter	SEQ_COUNT[3:0]	When SEQ_MODE[1:0] = 11b, the sequence counter indicates which sequence run the latest conversion result belongs to, which is currently available for readout.
Sequencer Active Flag	SEQ_ACTIVE	Indicates if conversions are currently ongoing or if the sequencer stopped and the device is in idle, standby or power-down mode.
Register Map CRC Fault Page Pointer	CRC_FAULT_PAGE[4:0]	Indicates which register page shows a CRC error when the REG_MAP_CRC_FAULTn indicates a CRC fault.
Digital Comparator Alert Step Indicator	COMP_ALERT_STEP_ INDICATOR[4:0]	Indicates which sequence step had a comparator overrange when the COMP_ALERTn flag is set.
Register Page Indicator	PAGE_INDICATOR[7:0]	Indicates which register page is currently selected by the device for reading and writing registers.

Instead of reading the STATUS_MSB or STATUS_LSB registers on demand using a register read command, the devices can output a STATUS header as the first two bytes of every frame on SDO. Enable the STATUS header transmission using the STATUS_EN bit. The 16-bit STATUS header is a concatenation of the STATUS_MSB[7:0] and STATUS_LSB[7:0] register bits.

In addition to the SAD_FAULTn flag, GPIO4 can be configured as a $\overline{\text{FAULT}}$ output pin to indicate any device faults as explained in the *$\overline{\text{FAULT}}$ Output* section.

7.3.15.1 Reset (RESETn flag)

The RESETn flag indicates if a device reset happened since the last time the bit was cleared to 1b. Write 1b to clear the RESETn bit to 1b.

The RESETn flag is 0b after device power-up.

7.3.15.2 AVDD Undervoltage Monitor (AVDD_UVn flag)

The AVDD undervoltage monitor sets the AVDD_UVn bit to 0b if the analog supply dropped below the AVDD undervoltage threshold (TH_{AVDD_UV}). Write 1b to clear the AVDD_UVn bit to 1b.

The AVDD_UVn flag is 0b after device power-up.

The AVDD undervoltage monitor is always active, except in power-down mode. AVDD_UVn sets to 0b when entering power-down mode even when the AVDD supply did not drop below the AVDD undervoltage threshold. The AVDD_UVn bit can set to 0b unintentionally when changing the internal voltage reference value using the REF_VAL bit.

The device does not reset when the analog supply drops below the AVDD threshold as long as the IOVDD supply is still present.

7.3.15.3 Reference Undervoltage Monitor (REF_UVn flag)

The reference undervoltage monitor sets the REF_UVn bit to 0b if the reference voltage selected by the STEPx_REF_SEL[1:0] bits on a certain sequence step dropped below the reference undervoltage threshold (TH_{REF_UV}). Use the REF_UV_SEL bit to select between two different undervoltage thresholds. Enable the reference undervoltage monitor using the REF_UV_EN bit. Write 1b to clear the REF_UVn bit to 1b.

The monitor only detects reference undervoltage conditions when the device is *converting* and is inactive during the conversion start delay period, or when the device is in idle, standby, or power-down mode.

7.3.15.4 SPI CRC Fault (SPI_CRC_FAULTn flag)

The SPI_CRC_FAULTn flag indicates if a SPI CRC fault occurred on SDI in the previous SPI frame. The execution of the command in the frame where the SPI CRC fault occurred is blocked. Instead, a no operation command is executed. Commands in following frames are not blocked. The SPI_CRC_FAULTn bit updates in every new SPI frame based on the CRC result of the previous SPI frame. Enable the SPI CRC using the SPI_CRC_EN bit. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI CRC faults. See the *SPI CRC* section for details about the SPI CRC implementation.

7.3.15.5 Register Map CRC Fault (REG_MAP_CRC_FAULTn flag)

The REG_MAP_CRC_FAULTn flag indicates if a register map CRC fault occurred due to an unintended register bit flip. In addition, the CRC_FAULT_PAGE[4:0] bits indicate which register page shows a CRC error. If multiple register pages have a CRC error, then the indicator points to the first register page address where a CRC error exists. Enable the register map CRC using the REG_MAP_CRC_EN bit. However, the register map CRC stops in standby and power-down mode irrespective of the REG_MAP_CRC_EN bit setting. Write 1b to clear the REG_MAP_CRC_FAULTn bit to 1b. See the *Register Map CRC* section for details about the register map CRC implementation.

7.3.15.6 Internal Memory Fault (MEM_FAULTn flag)

The MEM_FAULTn flag indicates if a memory map CRC fault occurred. Similar to the register map CRC, the devices use a memory map CRC to check the internal memory for unintended bit changes. Changes to the internal memory bits can cause undetermined device behavior or degraded device performance. The memory map CRC is always enabled, except in standby and power-down mode, and constantly calculates the CRC value across the internal memory map. The devices compare the calculation result against a memory map CRC value that is stored in the memory map in production. If the internal calculation result and the stored memory map CRC value do not match, the MEM_FAULTn flag is set to 0b. No other action is taken by the device in the event of a memory map CRC fault. Perform a power cycle or reset the device when the MEM_FAULTn bit is 0b.

7.3.15.7 Register Write Fault (REG_WRITE_FAULTn flag)

The REG_WRITE_FAULTn flag indicates if a write access to an invalid register address occurred. This flag sets when an invalid register address is written to, and updates at the next register write command.

Reading from an invalid register address does not set the flag, but can be detected from the address indication byte inside the SPI frame of the read command. The address indication byte reads FFh in this case.

The device does not detect if an invalid register page address is written to the PAGE_POINTER register. However, any register write attempt on an invalid register page triggers the REG_WRITE_FAUTLn flag.

7.3.15.8 Digital Comparator Alert (COMP_ALERTn flag)

The digital comparator sets the COMP_ALERTn bit to 0b if the comparator on any of the sequence steps tripped. Write 1b to clear the COMP_ALERTn bit to 1b. See the *Digital Comparator* section for more details.

7.4 Device Functional Modes

7.4.1 Power-up and Reset

The ADS1x4S1x is reset in one of four ways:

- Power-on reset (POR)
- Taking the $\overline{\text{RESET}}$ pin low (hardware reset).
- Writing to the RESET_CODE[7:0] bit field (software reset)
- Sending the SPI reset pattern (software reset)

After a reset occurs, the user registers reset to the respective default settings and the device is in idle mode; no conversions are started. SPI communication with the device is possible after the reset process completes. See the *Timing Requirements* for timing specifications to consider after the various reset events before starting communication with the device.

A low-to-high transition on the $\overline{\text{DRDY}}$ pin indicates that the SPI is ready for communication as shown in Figure 7-15 and Figure 7-16. The device ignores any SPI communication before this point and SDO stays low.

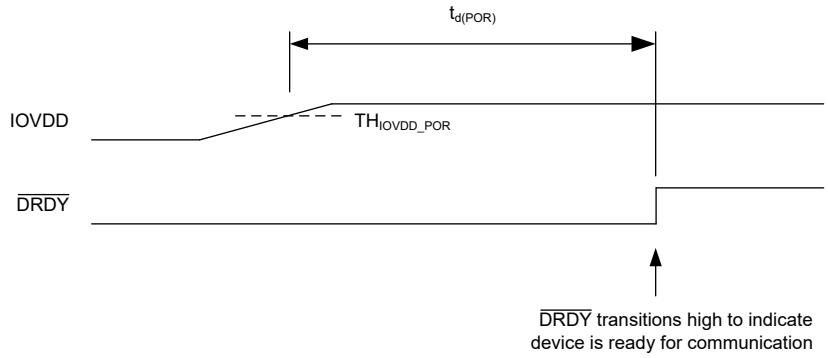


Figure 7-15. $\overline{\text{DRDY}}$ Pin Behavior After POR

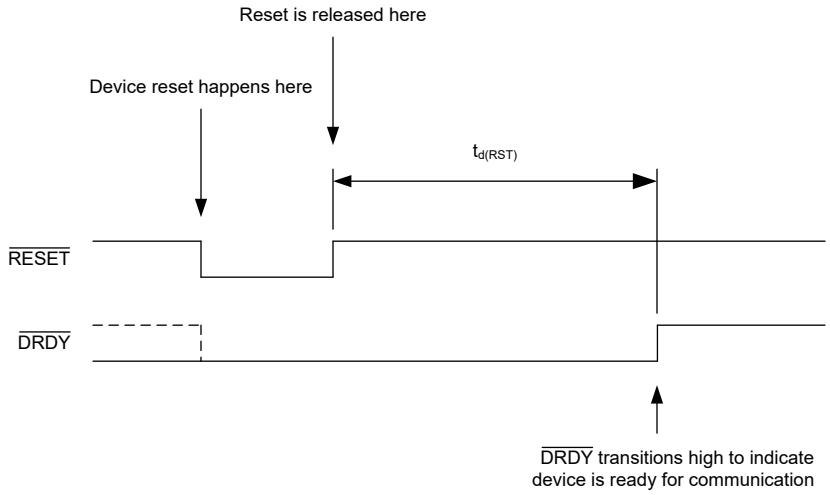


Figure 7-16. $\overline{\text{DRDY}}$ Pin Behavior After Device Reset Using the $\overline{\text{RESET}}$ Pin

The RESETn bit indicates if a reset occurred since the last time the RESETn bit was cleared to 1b. Clear the RESETn bit to 1b right after a device reset to get notified of unintended device resets during operation.

7.4.1.1 Power-On Reset (POR)

A power-on reset (POR) circuit holds the device in reset until the IOVDD supply exceeds the POR threshold (TH_{IOVDD_POR}). The power-on reset circuit is also designed such that the device starts operating in a known good state in case a brown-out event occurred, where the IOVDD supply dipped below the IOVDD POR threshold. An undervoltage event on AVDD does not cause a device reset, but is indicated by the AVDD_UVn flag.

7.4.1.2 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is an active low input. The ADC is reset by taking $\overline{\text{RESET}}$ low then back high. Because the $\overline{\text{RESET}}$ pin has an internal 20kΩ pullup resistor, the $\overline{\text{RESET}}$ pin can be left unconnected if not used. The $\overline{\text{RESET}}$ pin is a Schmitt-triggered input designed to reduce noise sensitivity.

7.4.1.3 Reset by Register Write

Initiate a software reset by writing 01011010b (5Ah) to the RESET_CODE[7:0] bit field. Writing any other value to this bit field does not result in reset. In 4-wire SPI mode, reset takes effect at the end of the frame at the time $\overline{\text{CS}}$ is taken high. In 3-wire SPI mode, reset takes effect on the last SCLK falling edge of the register write operation. Reset in 3-wire SPI mode requires that the SPI is synchronized to the SPI host. If SPI synchronization is not assured, use the pattern described in the *Reset by SPI Input Pattern* section to reset the device.

7.4.1.4 Reset by SPI Input Pattern

The device is also reset through SPI operation by inputting a special bit pattern on SDI. The input pattern does not follow the regular SPI command format. Two input patterns are available to reset the ADC.

Pattern 1 consists of a *minimum* 1023 consecutive ones followed by one zero. The device resets on the falling edge of SCLK when the final zero is shifted in. This pattern can be used in either 3- or 4-wire SPI mode. Figure 7-17 shows a pattern 1 reset example.

Reset pattern 2 is only for use with 4-wire SPI mode. To reset, input a *minimum* of 1024 consecutive ones (no ending zero value), followed by taking $\overline{\text{CS}}$ high at which time the reset occurs. Use pattern 2 when multiple devices are connected in a daisy-chain. Figure 7-18 shows a pattern 2 reset example.

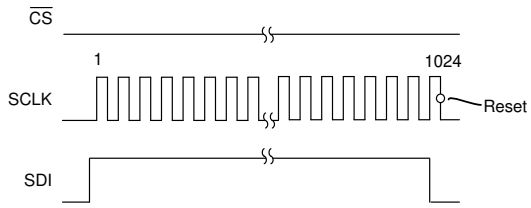


Figure 7-17. Reset Pattern 1 (3-Wire or 4-Wire SPI Mode)

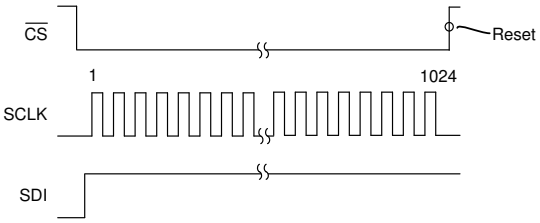


Figure 7-18. Reset Pattern 2 (4-Wire SPI Mode)

7.4.2 Operating Modes

The ADS1x4S1x offer four operating modes: standby, idle, power-down, and sequencer mode. Figure 7-19 shows how the device transitions between the different operating modes.

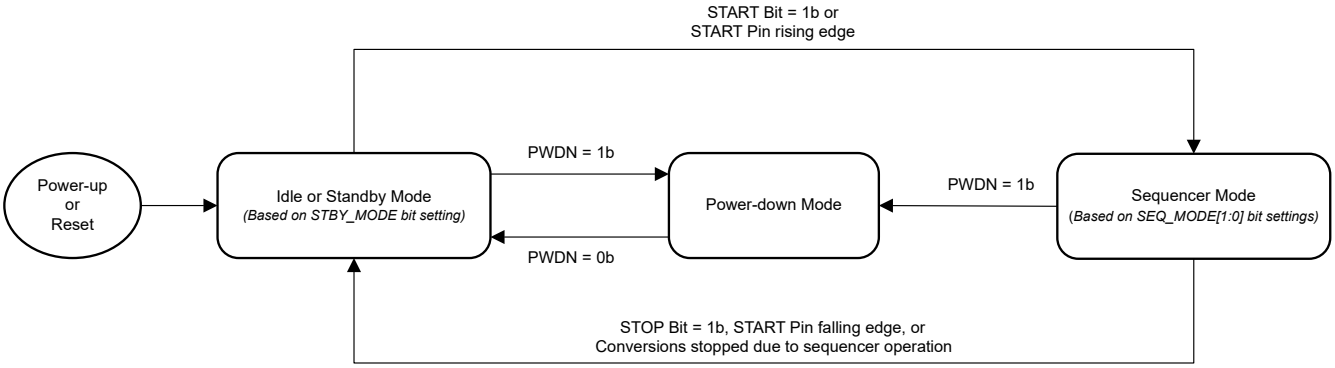


Figure 7-19. Operating Mode State Diagram

7.4.2.1 Idle and Standby Mode

After reset, the device is in idle mode. All analog circuitry is powered up, based on the respective register bit default settings, but no conversions are ongoing, and the digital filter is held in reset.

Set the START bit to 1b or take the START pin high for the device to exit idle or standby mode and to start the sequencer. When the sequencer stops, the device transitions to either idle or standby mode depending on the STBY_MODE bit setting. The STEP_INIT[4:0] pointer determines the step page configuration that is used whenever the device is in idle or standby mode, regardless if the respective step page is enabled or not (STEP_x_EN bit setting is ignored). Selecting the appropriate step page when the sequencer stops is important in case the IDACs needs to be configured in a certain way during idle periods or any GPIO configured as a digital output needs to drive a certain output level.

In standby mode, the ADC, PGA, IDACs, BOCS, reference buffers, register map CRC, and memory map CRC power down, irrespective of the register bit settings. The internal voltage reference and oscillator stay powered-up in standby mode.

Use standby mode to save power when the sequencer stops. When starting the sequencer from standby mode, the latency time for the first conversion is longer compared to the latency time when starting the sequencer from idle mode as explained in the *Digital Filter Latency* section.

See the *Starting and Stopping the Sequencer* section for additional details.

7.4.2.2 Power-Down Mode

In power-down mode, all analog and digital circuitry are powered off, except for circuitry which is required to retain the user register settings. SPI communication is still possible. Set the PWDN bit to 1b to power the device down immediately; any ongoing conversions are aborted. In power-down mode:

- the AVDD_UVn bit sets to 0b
- the conversion data clears to zero
- the conversion counter (CONV_COUNT[3:0]) resets to Fh
- the sequence step indicator (STEP_INDICATOR[4:0]) resets to 00h
- the sequence counter (SEQ_COUNT[3:0]) resets to 0h
- any analog inputs configured as GPIO digital outputs transition into a Hi-Z state. To maintain a certain GPIO logic level during power-down, consider external pullup resistors to AVDD or pulldown resistors to AVSS on the respective GPIO pins.

The START bit and START pin are ignored in power-down mode. Set the PWDN bit to 0b to exit power-down mode. Allow the internal voltage reference to start up and settle when coming out of power-down mode before starting any conversions.

7.4.2.3 Sequencer Mode

Conversions of the ADS1x4S1x are controlled by means of a *sequencer* together with the START and STOP bits or the START pin. The sequencer schedules conversions based on the sequencer mode configuration (SEQ_MODE[1:0] bit settings).

The devices offer up to 24 unique configuration settings (steps x = 0 to 23), which can be programmed during device initialization into the sequencer *step configuration register pages*. Each step configuration page allows the user to select device settings such as the input multiplexer, PGA gain, voltage reference source, digital filter type and OSR, excitation current source magnitude and routing, GPIO data output, and digital comparator thresholds. See the *Step Configuration Page Registers* section for details on all available configuration options per sequence step.

Table 7-19 describes how the SEQ_MODE[1:0] bits determine the sequencer operation when the host starts the sequencer.

Table 7-19. Sequencer Modes

SEQ_MODE[1:0]	SEQUENCER OPERATION
00b	The device executes the sequence step defined by the STEP_INIT[4:0] pointer one time. The step enable bits (STEP_x_EN) are ignored in this sequencer mode. The STEPx_NUM_CONV[4:0] bits determine the number of consecutive conversions that are performed for this sequence step. If STEPx_NUM_CONV[4:0] = 00000b, a single conversion is executed. This is commonly referred to as single-shot conversion mode in TI ADCs that do not offer a sequencer. After the number of conversions defined by the STEPx_NUM_CONV[4:0] bits are converted, the device returns to idle or standby mode, depending on the STBY_MODE bit setting. See Figure 7-20 for a detailed sequencer operation flow chart.
01b	The device continuously converts the sequence step defined by the STEP_INIT[4:0] pointer. This is commonly referred to as continuous-conversion mode in TI ADCs that do not offer a sequencer. The step enable bits (STEP_x_EN) and STEPx_NUM_CONV[4:0] bits are ignored in this sequencer mode. Stop conversions by setting the STOP bit to 1b or by taking the START pin low. See Figure 7-21 for a detailed sequencer operation flow chart.
10b	The device executes a sequence of all enabled steps between the step defined by the STEP_INIT[4:0] pointer and step 23 one time. Use the STEP_x_EN bits to include a step in the sequence. The sequence does not execute if the step defined by the STEP_INIT[4:0] pointer is disabled. After completing the conversions of the last enabled sequence step, the device returns to idle or standby mode, depending on the STBY_MODE bit setting. See Figure 7-22 for a detailed sequencer operation flow chart.
11b	The device executes the complete sequence of enabled steps and repeats the sequence continuously, starting with the step defined by the STEP_INIT[4:0] pointer. After completing conversions of the last enabled step in the sequence, the device executes a new sequence run starting with the first enabled step. The first enabled step can be different from the step defined in the STEP_INIT[4:0] pointer. Use the STEP_x_EN bits to include a step in the sequence. The sequence does not execute if the step defined by the STEP_INIT[4:0] pointer is disabled. Stop the sequencer by setting the STOP bit to 1b or by taking the START pin low. See Figure 7-22 for a detailed sequencer operation flow chart.

Figure 7-20, Figure 7-21, and Figure 7-22 illustrate the sequencer behavior for the different sequencer modes. The flow charts show the behavior when using the START and STOP bits to control the sequencer. The START pin can be used instead as explained in the *Starting and Stopping the Sequencer (START/STOP bits and START pin)* section.

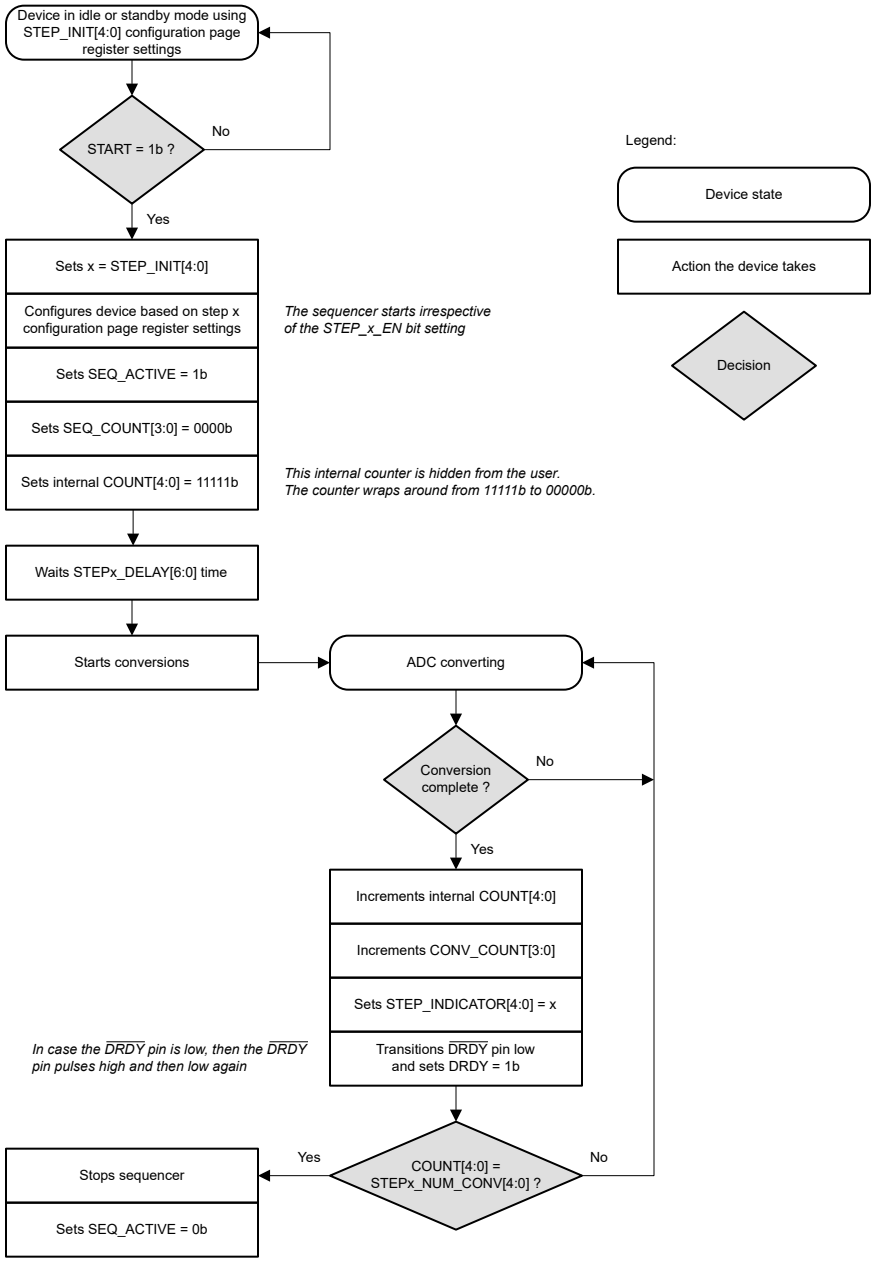


Figure 7-20. Sequencer Operation Flow Chart (SEQ_MODE[1:0] = 00b)

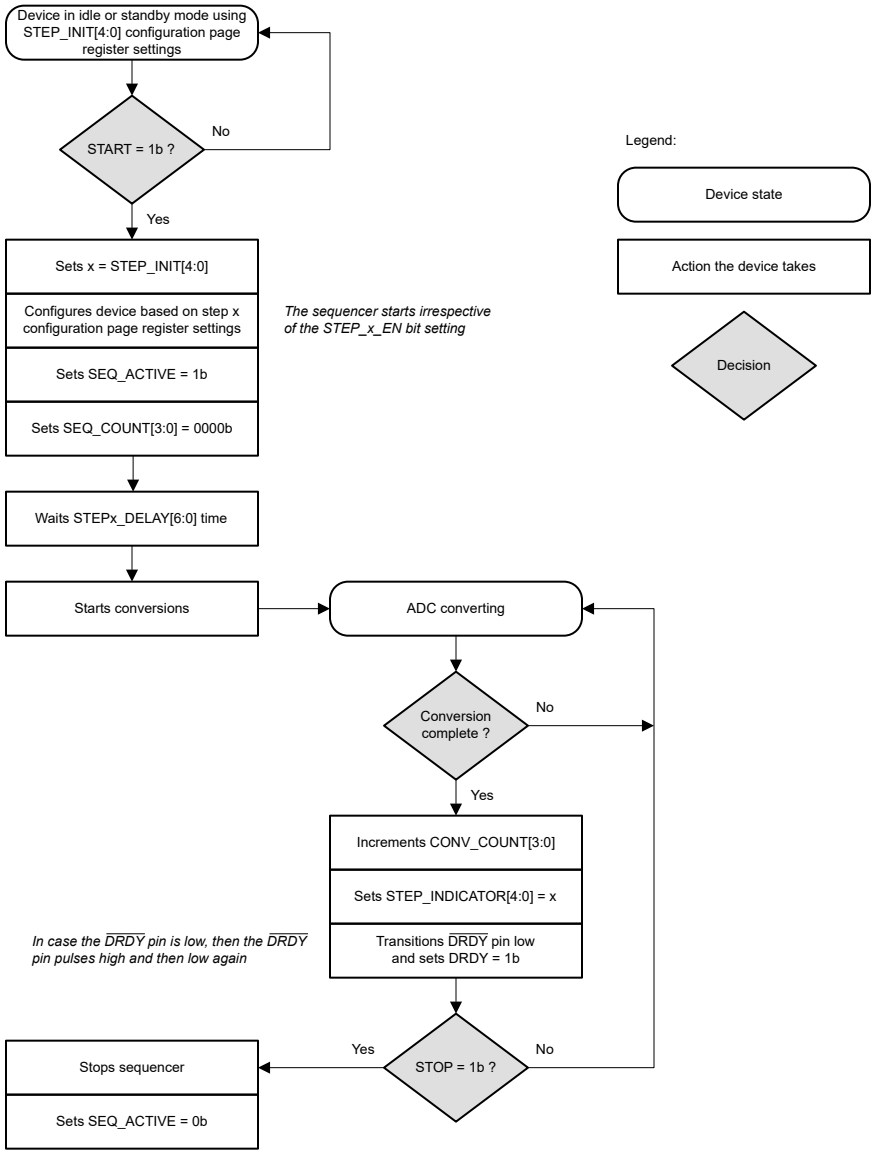


Figure 7-21. Sequencer Operation Flow Chart (SEQ_MODE[1:0] = 01b)

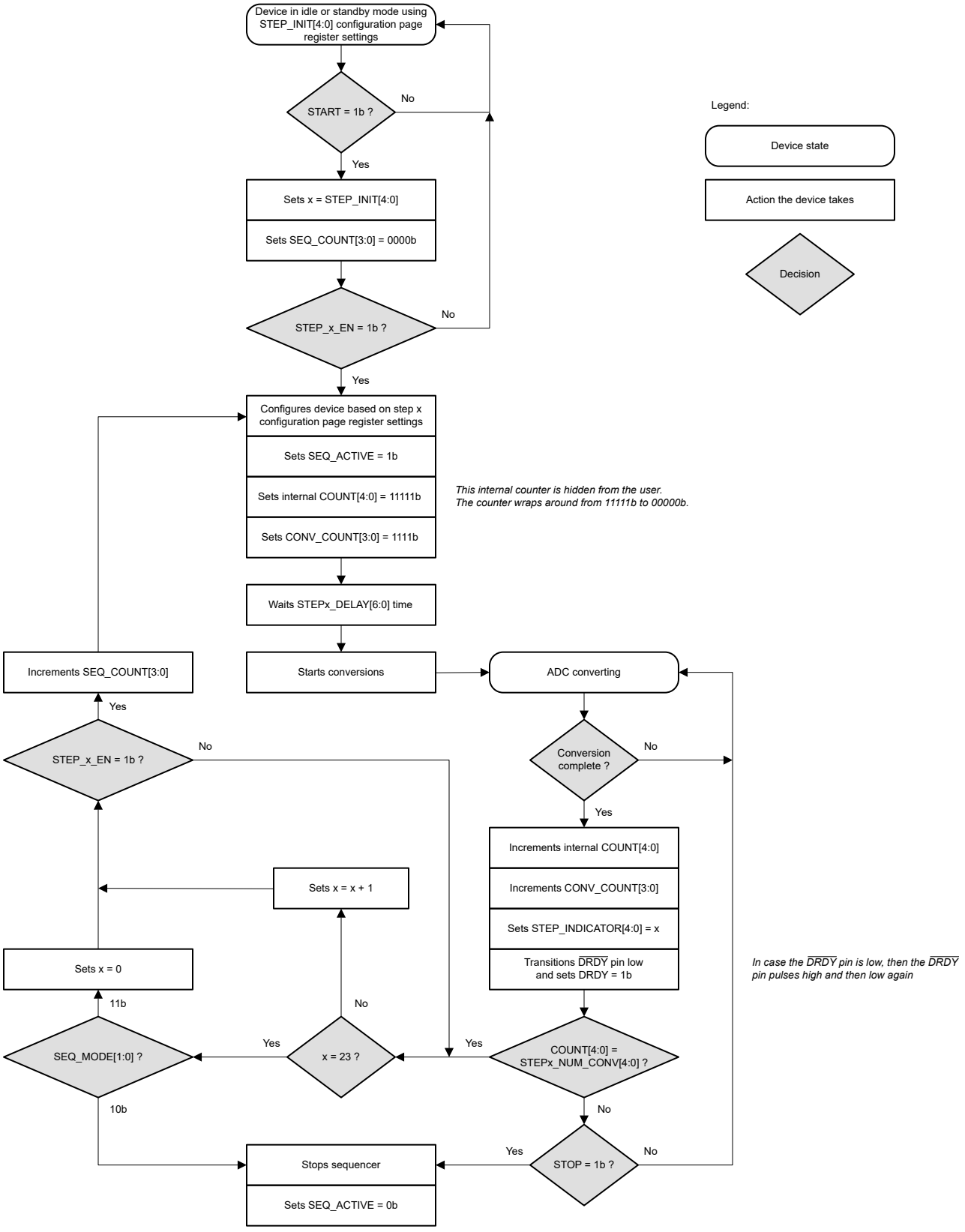


Figure 7-22. Sequencer Operation Flow Chart (SEQ_MODE[1:0] = 10b or 11b) (STOP_BEHAVIOR[1:0] = 01b)

7.4.2.3.1 Configuring the Sequencer

Configure the sequencer operation and behavior using the various bits summarized in Table 7-20. For more details see the respective bit field descriptions in the *Register Map* section.

Table 7-20. Sequencer Configuration Bits

REGISTER BITS[1]	DESCRIPTION
Status and General Configuration Page	
STEP_INIT[4:0]	This pointer determines the step page configuration that is used for the first conversion when the sequencer starts. In idle or standby mode, this pointer selects the active step page configuration, irrespective if the page is enabled or disabled by the respective STEP_x_EN bit.
SEQ_MODE[1:0]	Selects the sequencer operation as described in the *Sequencer Mode* section.
STOP_BEHAVIOR[1:0]	Determines how the sequencer stops when the host requests to stop the sequencer.
STEP_x_EN	The individual enable bits select a step to be included within the sequence when SEQ_MODE[1:0] = 10b or 11b. These bits are ignored when SEQ_MODE[1:0] = 00b or 01b.
Step x Configuration Pages	
STEPx_NUM_CONV[4:0]	Determines how many consecutive conversions the sequencer executes on the respective sequence step. The digital filter does not reset between those consecutive conversions of a step. These bits are ignored when SEQ_MODE[1:0] = 01b.
STEPx_DELAY[6:0]	Determines how long the sequencer waits after selecting a step configuration page before starting conversions. This is to allow for any settling of the selected measurement signal. The digital filter is held in reset during this delay time.

(1) x = 0 to 23 refers to the individual step page configurations.

See the *Register Map* section for details on how to access the various register pages for configuration. Section *Device Initialization and Starting the Sequencer* shows an example of how to configure the sequencer.

Do not change any register settings on the individual step configuration pages while the sequencer is active. Any write operation to any of the step configuration pages stops the sequencer immediately.

7.4.2.3.2 Starting and Stopping the Sequencer (START/STOP bits and START pin)

To start the sequencer, write 1b to the START bit or take the START pin high. The value written to the STEP_INIT[4:0] bit field determines which sequence step configuration the sequencer selects for the first conversion. STEP_INIT[4:0] = 00000b points to step configuration page 0, while STEP_INIT[4:0] = 10111b points to the last available step configuration page 23. Figure 9-4 illustrates how to start the sequencer using a flow chart.

The START bit takes effect at the $\overline{CS}$ rising edge (4-wire SPI mode), or the last SCLK falling edge (3-wire SPI mode) of the SPI frame where the CONVERSION_CTRL register is written. See the *Write Register Command* section for details on the SPI frame of a register write command.

Set the STOP bit to 1b or take the START pin low to stop the sequencer. The STOP_BEHAVIOR[1:0] bits determine how the sequencer stops. See the STOP_BEHAVIOR[1:0] bit field description for details. The last conversion result is still available for readout after the sequencer stopped. The conversion results only clear after a device reset, in power-down mode, or are overwritten when a new conversion result becomes available.

When the sequencer stops, the device returns to idle or standby mode, depending on the STBY_MODE bit setting. The STEP_INIT[4:0] bit field determines the step configuration page that is used whenever the device is in idle or standby mode, regardless if the respective step page is enabled or not (STEP_x_EN bit setting is ignored). That means, when coming out of power-down mode, or when conversions stop, the device transitions to the step page configuration determined by the STEP_INIT[4:0] bit field. If the STEP_INIT[4:0] pointer is set to an invalid value between 18h and 1Fh in standby or idle mode, then the configuration of step 23 takes effect. Selecting the appropriate step page when the sequencer stops is important in case the IDACs needs to be configured in a certain way during idle periods or any GPIO configured as a digital output needs to drive a certain output level. In idle or standby mode, register bit changes on the page pointed to by the STEP_INIT[4:0] pointer take effect immediately.

Keep the following device behavior in mind when controlling the sequencer:

- Writing 1b to both the START and STOP bits at the same time has no effect.
- Keep the START pin low when controlling the sequencer through the START and STOP bits. Similarly, do not use the START and STOP bits when controlling the sequencer using the START pin.
- The START pin is generally *edge* sensitive. A START pin rising edge is equivalent to setting the START bit to 1b, and a START pin falling edge is equivalent to setting the STOP bit to 1b. However, the START pin becomes *level* sensitive at power-up, during device reset, and when writing device registers that stop the sequencer. Therefore keep the START pin low during these events to avoid unintended sequencer starts.
- After writing to the SEQUENCER_CFG register, another SPI transaction, for example a no-operation command, is required before the START pin can be used to start conversions. The START bit does not have this limitation and can be written immediately after writing to the SEQUENCER_CFG register to start conversions.
- Setting the START bit to 1b or pulsing the START pin low and high again while conversions are ongoing aborts the ongoing conversion and restarts the sequencer using the step configuration page indicated in the STEP_INIT[4:0] bit field.
- If $\overline{\text{DRDY}}$ is low, the device drives the $\overline{\text{DRDY}}$ pin high when the sequencer starts, however the old conversion data can still be read until the new conversions become available.
- Any write operation to the following registers stops the sequencer immediately irrespective of the sequencer stopping behavior selected by the STOP_BEHAVIOR[1:0] bits:
  - Any register on the status and general configuration page between register addresses 10h to 1Fh, with the exception of register at address 17h.
  - Any register on any of the step configuration pages.

7.4.2.3.3 Sequencer Status Bits

The step indicator (STEP_INDICATOR[4:0]), conversion counter (CONV_COUNT[3:0]), and sequence counter (SEQ_COUNT[3:0]) provide information about the latest conversion result that is currently available for readout as described in Table 7-18 and the respective register bit descriptions.

When the sequencer is active and conversions are ongoing, the SEQ_ACTIVE status bit reads 1b.

7.5 Programming

7.5.1 Serial Interface (SPI)

The serial interface is used to read conversion data, configure device registers, and control ADC conversions.

The serial interface consists of four lines: $\overline{CS}$, SCLK, SDI, and SDO/$\overline{DRDY}$. In addition, a dedicated $\overline{DRDY}$ output pin is available. The host always drives SCLK and the device acts as a peripheral. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low, and data update on SCLK rising edges and are latched on SCLK falling edges.

The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously. The interface also supports daisy-chain connection of multiple ADCs.

7.5.2 Serial Interface Signals

7.5.2.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the interface for communication. A communication frame starts by taking $\overline{CS}$ low and ends by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends the frame by interpreting the last 16 bits of input data (24 bits when SPI CRC is enabled) regardless of the total number of bits shifted in. When $\overline{CS}$ is high, the SPI resets, commands are blocked, and SDO/$\overline{DRDY}$ enters a high-impedance state. The dedicated $\overline{DRDY}$ pin is an active output regardless of the state of $\overline{CS}$. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode.

7.5.2.2 Serial Clock (SCLK)

SCLK is the serial clock input used to shift data into and out of the ADC. Data on SDO update on the rising edge of SCLK and data on SDI are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series termination resistor at the SCLK driver can reduce ringing.

7.5.2.3 Serial Data Input (SDI)

SDI is the serial interface data input. SDI is used to input data to the device. Input data are latched on the falling edge of SCLK. Idle SDI high or low when not active.

7.5.2.4 Serial Data Output/Data Ready (SDO/$\overline{DRDY}$)

SDO/$\overline{DRDY}$ is a dual-function output pin. This pin is programmable to provide output data only, or to provide output data and the data-ready indication. The SDO_MODE bit selects the mode. The dual-function mode multiplexes output data and data-ready operations on a single pin. This mode can replace the function of the dedicated $\overline{DRDY}$ pin to reduce the number of SPI I/O lines required to interface to the host.

Output data update on the rising edge of SCLK. The SDO/$\overline{DRDY}$ pin is in a high-impedance state when $\overline{CS}$ is high.

When programmed to dual-function mode (SDO_MODE = 1b) and when $\overline{CS}$ is low, SDO/$\overline{DRDY}$ mirrors $\overline{DRDY}$ until the first rising edge of SCLK, at which time the pin changes mode to provide data output. When the data read operation is complete, the pin reverts back to mirroring $\overline{DRDY}$. Figure 7-23 illustrates the behavior of the SDO/$\overline{DRDY}$ pin.

In output data only mode (SDO_MODE = 0b), SDO stays at the level of the last bit sent if the host does not send any extra SCLK pulses after the last data is shifted out on SDO, as shown in Figure 7-23.

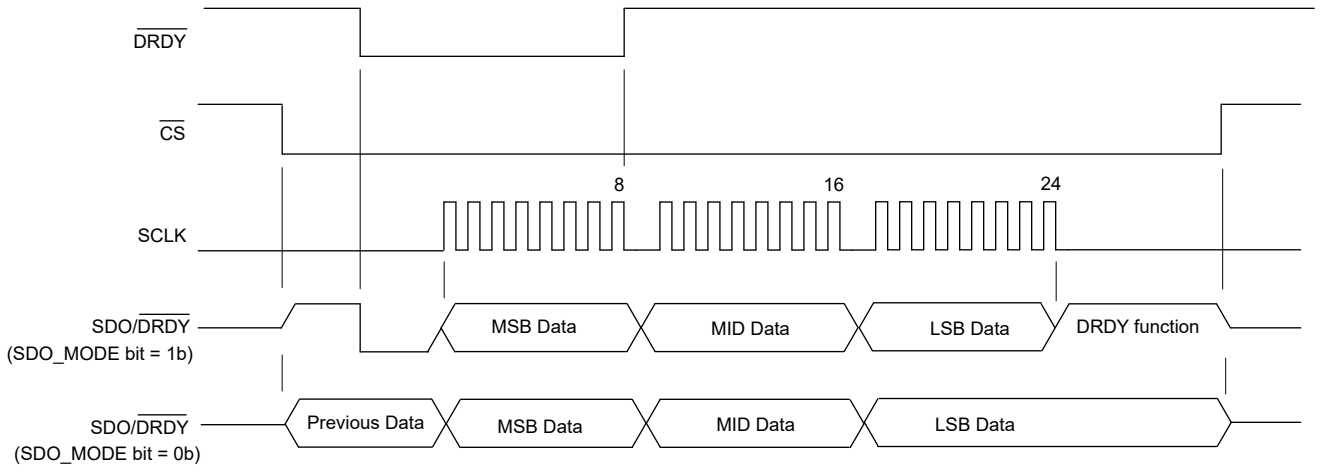


Figure 7-23. SDO/DRDY and DRDY Behavior (24-bit Device, STATUS header and CRC disabled)

7.5.2.5 Data Ready (DRDY) Pin

A falling edge on the DRDY pin indicates the completion of new conversion data. The DRDY output is always driven even when CS is high. DRDY drives high when the sequencer starts, and drives low when conversion data are ready. DRDY drives back high at the eighth SCLK falling edge of the MSB conversion data read as shown in Figure 7-23. If conversion data are not read, DRDY pulses high $t_{W(DRH)}$ before the next falling edge. Whenever the device is programmed to enter standby mode (STBY_MODE bit = 1b) after conversions stopped, DRDY is driven back high 4 t_{MOD} after transitioning low.

See the *DRDY Pin Behavior* section for further details on the DRDY pin operation.

7.5.3 Serial Interface Communication Structure

7.5.3.1 SPI Frame

Communication through the serial interface is based on the concept of frames. A frame consists of a prescribed number of SCLKs required to shift data in on SDI, or out on SDO. A frame starts by taking $\overline{CS}$ low and ends by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device interprets the last 16 bits (or 24 bits when SPI CRC is enabled) of input data regardless of the amount of data shifted into the device.

The interface is full duplex, meaning that the interface is capable of transmitting data on SDO while simultaneously receiving data on SDI. Typically, the input frame is sized to match the output frame by padding the frame with leading zeros if needed. However, if only writing to the device while ignoring the data on SDO, the frame can be shortened to the minimum size of 16 bits (or 24 bits when SPI CRC is enabled). Figure 7-24 and Figure 7-25 show typical communication frame structures for the 16-bit and 24-bit devices, respectively. In these examples, conversion data are shifted out on SDO. As illustrated, command bytes on SDI (plus the optional CRC-IN byte) are always right aligned within a frame. Data bytes on SDO (plus the optional STATUS header and CRC-OUT byte) are always left aligned within a frame.

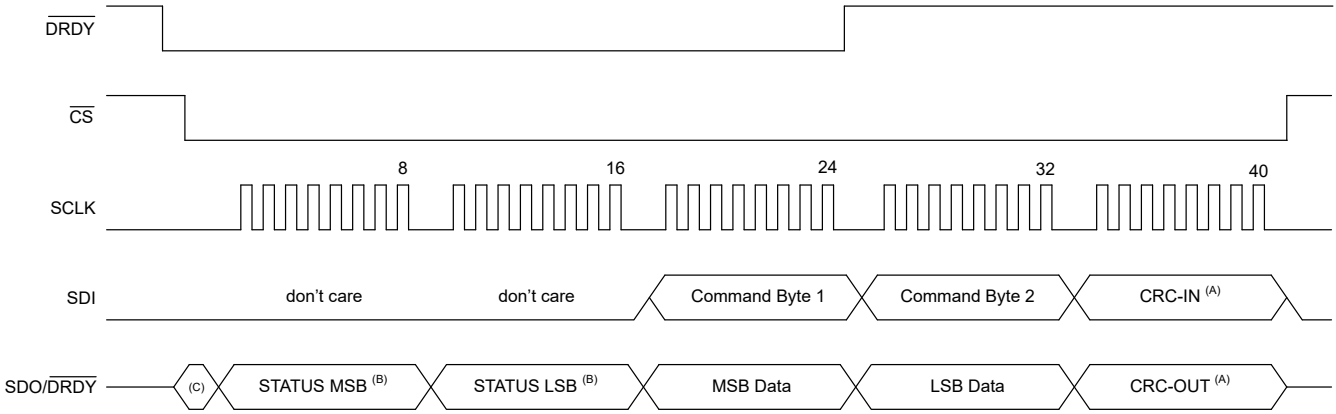
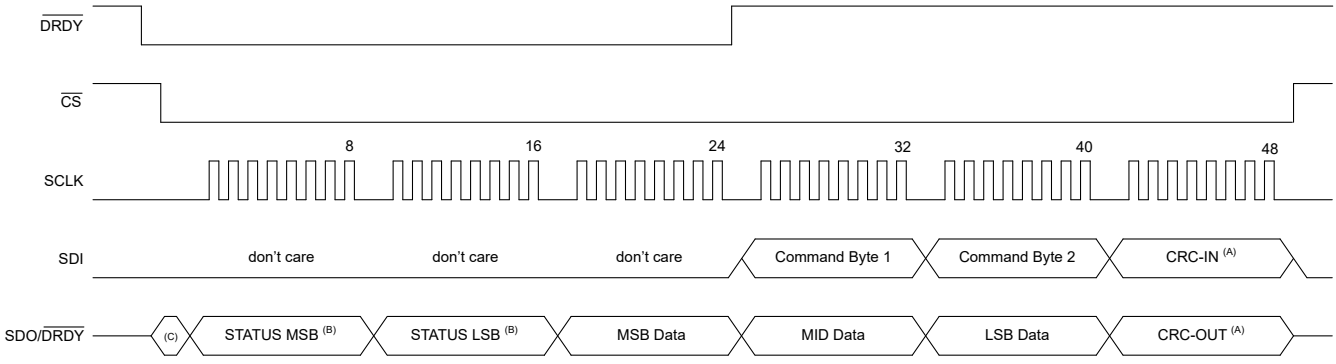


Figure 7-24. Typical Communication Frame (16-Bit Device)



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-25. Typical Communication Frame (24-Bit Device)

The output frame size, as given in Table 7-21, depends on the data resolution (16 or 24 bits), the optional STATUS header (two bytes), and the optional CRC byte.

Table 7-21. Output Frame Size

RESOLUTION	STATUS HEADER	CRC BYTE	FRAME SIZE
16 bit	No	No	16 bit
16 bit	No	Yes	24 bit
16 bit	Yes	No	32 bit
16 bit	Yes	Yes	40 bit
24 bit	No	No	24 bit
24 bit	No	Yes	32 bit
24 bit	Yes	No	40 bit
24 bit	Yes	Yes	48 bit

In 4-wire SPI mode, when extending the frame beyond the frame size given in Table 7-21, the device starts shifting out data on SDO which was shifted in on SDI at the beginning of the frame. This behavior is to support daisy-chain operation as explained in the *Daisy-Chain Operation* section.

A continuous-read mode is available in 4-wire SPI mode, where an arbitrary number of register data can be retrieved without any transitions of $\overline{CS}$, and the frame extends to accommodate the additional data. See the *Continuous-Read Mode* section for details. In continuous-read mode, the output frame size is unlimited.

In 3-wire SPI mode, the input frame must match the size of the output frame as given in Table 7-21 for the SPI to remain synchronized. See the *3-Wire SPI Mode* section for details.

7.5.3.2 STATUS Header

The ADS1x4S1x output an optional STATUS header as the first two bytes of every frame on SDO. Enable the STATUS header transmission using the STATUS_EN bit. The 16-bit STATUS header is a concatenation of the STATUS_MSB[7:0] and STATUS_LSB[7:0] register bits. Some of the fault flags, the DRDY bit, the conversion counter, and sequence step indicator are all part of these bits. See the *Monitors and Status Flags* section and the respective register bit descriptions in the *Status and General Configuration Page Registers* section for details.

7.5.3.3 SPI CRC

The SPI cyclic redundancy check (CRC) is a check code used to detect transmission errors to and from the host controller. A CRC-IN byte is transmitted with the ADC input data by the host on SDI and a CRC-OUT byte is transmitted with the output data by the device on SDO. Use the SPI_CRC_EN bit to enable the SPI CRC. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI input CRC faults.

The CRC-IN code is calculated by the host over the two command bytes. Any input bytes padded to the start of the frame are not included in the CRC-IN calculation. The ADC checks the input command CRC-IN code against an internal code calculated over the two received input command bytes. If the CRC-IN codes do not match, the command is not executed and the SPI_CRC_FAULTn bit is set to 0b.

The SPI_CRC_FAULTn bit is output as part of the STATUS header to provide immediate indication that a CRC error occurred in the previous frame. The SPI_CRC_FAULTn bit clears automatically in the next SPI frame, assuming no SPI CRC error occurred in the current frame.

The number of bytes used to calculate the output CRC code depends on the amount of data bytes transmitted in the frame on SDO. Table 7-22 shows the number of bytes included in the output CRC calculation.

Table 7-22. Data Covered by Output CRC

ACTION	DEVICE RESOLUTION	STATUS HEADER ENABLED	BYTE COUNT	DATA COVERD BY OUTPUT CRC
Conversion data read	16 bit	No	2	16 bits of conversion data
Conversion data read	16 bit	Yes	4	16 bits STATUS header + 16 bits of conversion data
Register data read	16 bit	No	2	8 bits of register data + 8 bits address byte
Register data read	16 bit	Yes	4	16 bits STATUS header + 8 bits of register data + 8 bits address byte
Conversion data read	24 bit	No	3	24 bits of conversion data
Conversion data read	24 bit	Yes	5	16 bits STATUS header + 24 bits of conversion data
Register data read	24 bit	No	3	8 bits of register data + 8 bits address byte + 8 bits of 00h padding
Register data read	24 bit	Yes	5	16 bits STATUS header + 8 bits of register data + 8 bits address byte + 8 bits of 00h padding

The CRC code calculation is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the variable length argument with the CRC polynomial. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. The CRC calculation is initialized to all 1s to detect errors in the event that SDI and SDO/$\overline{\text{DRDY}}$ are either stuck high or low.

Figure 7-26 shows a visual representation of the CRC calculation. The following procedure calculates the CRC value:

- Preload the 8-bit shift register, which has XOR blocks located at positions that correspond to the CRC polynomial (07h), with the seed value of FFh.
- Shift in all data bits starting with the most-significant bit (MSB) and re-compute the shift-register value after each bit.
- The resulting shift-register value after all data bits have been shifted in is the computed CRC value.

The example C code available for download *here* includes a potential CRC implementation.

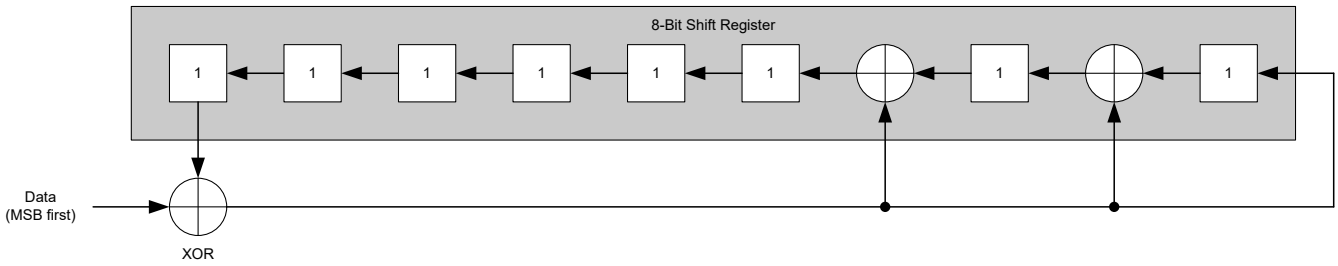


Figure 7-26. Visual Representation of CRC Calculation

7.5.4 Device Commands

Commands are used to read and write register data. The register map consists of a series of one-byte (8 bit) registers, accessible by read and write operations. The minimum frame length of the input command sequence is 16 bit (24 bit when SPI CRC is enabled). If desired, the input command sequence can be padded with leading zeros to match the length of the output data frame. When the SPI CRC is enabled, the device interprets the two bytes preceding the CRC-IN byte at the end of the frame as the command bytes. Table 7-23 shows the ADS1x4S1x commands.

Table 7-23. SPI Commands

DESCRIPTION	BYTE 1	BYTE 2	BYTE 3 (Optional CRC-IN Byte)
No operation (read conversion data)	00h	00h	D7h
Read register command	40h + address [5:0]	Don't care	CRC-IN of byte 1 and byte 2
Write register command	80h + address [5:0]	Register data	CRC -IN of byte 1 and byte 2

The device supports special extended-length bit patterns that are longer than the standard command length. These patterns are used to reset the ADC and to reset the frame in 3-wire SPI mode. The extended bit patterns are explained in the *Reset by SPI Input Pattern* and *3-Wire SPI Mode Frame Re-Alignment* sections.

The instance where the commands are latched by the device depend on the SPI mode:

- 4-wire SPI mode: The rising edge of $\overline{CS}$
- 3-wire SPI mode: The last SCLK falling edge of the SPI frame (including the CRC-OUT byte in CRC mode)

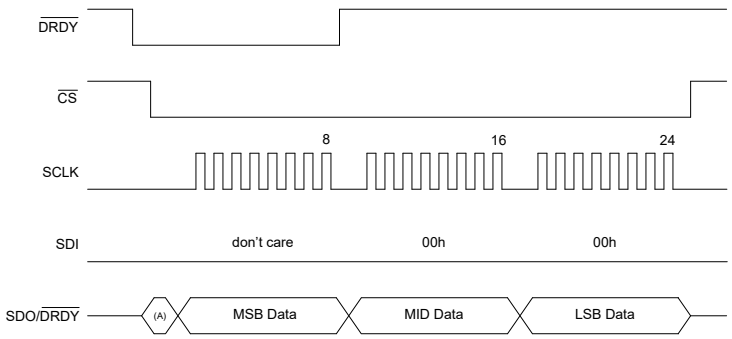
7.5.4.1 No Operation (Read Conversion Data)

The no-operation command bytes are 00h and 00h. Use this command to read conversion data when not sending a read or write register command at the same time. If the SPI CRC check is enabled, the CRC byte is required (byte 3), which is always D7h for bytes 00h and 00h. SDI can be held low during data readback, but in CRC mode the SPI_CRC_FAULTn bit sets to 0b. The SPI_CRC_FAULTn flag can be ignored while reading conversion data, and is updated in every new SPI frame.

Conversion data are buffered, which allows data to be read up to one f_{MOD} clock cycle before the next $\overline{DRDY}$ falling edge. Conversion data can be read multiple times until the next conversion data are ready, and are never corrupted. Register data replace the conversion data if the register read command is sent in the previous frame.

$\overline{DRDY}$ is driven back high at the eighth SCLK falling edge during conversion data read, that is when the transmission of the conversion data MSB byte is complete.

Figure 7-27 shows an example of reading 24-bit conversion data with the STATUS header and CRC byte disabled.

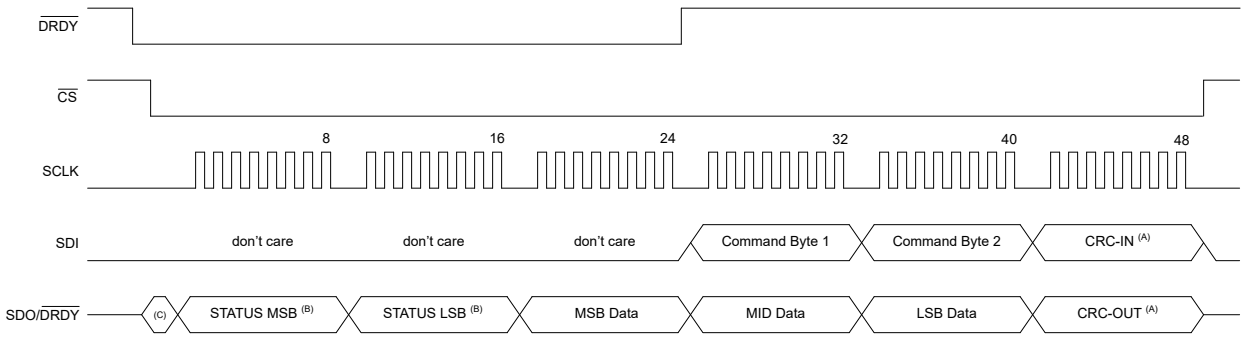


A. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-27. Read Conversion Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-28 is an example of a read conversion data operation when the STATUS header and the CRC byte are enabled. This example also shows the optional use of a full-duplex transmission when a command is input at the same time the conversion data are output. If no input command is desired, the input bytes are 00h, 00h, and D7h. The output CRC (CRC-OUT) code computation includes the STATUS header.

$\overline{\text{DRDY}}$ is driven back high at the 24th SCLK falling edge, when the transmission of the conversion data MSB byte is complete. This is also true if the data is not completely read, that is if the read operation is stopped any time after the transmission of the conversion data MSB byte, but before the end of the frame.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-28. Read Conversion Data (24-Bit Device, STATUS Header and CRC Enabled)

Conversion data can be read asynchronous to $\overline{\text{DRDY}}$. However, when conversion data are read close to the $\overline{\text{DRDY}}$ falling edge, there is uncertainty whether previous data or new data are output. If the SCLK shift operation starts at least one f_{MOD} clock cycle before the $\overline{\text{DRDY}}$ falling edge, then old data are provided. If the shift operation starts at least one f_{MOD} clock cycle *after* $\overline{\text{DRDY}}$, then new data are output. In either case, data are not corrupted. When the STATUS header transmission is enabled, the DRDY bit indicates if the data transmitted in the current frame are old (previously read data, DRDY = 0b) or new (DRDY = 1b).

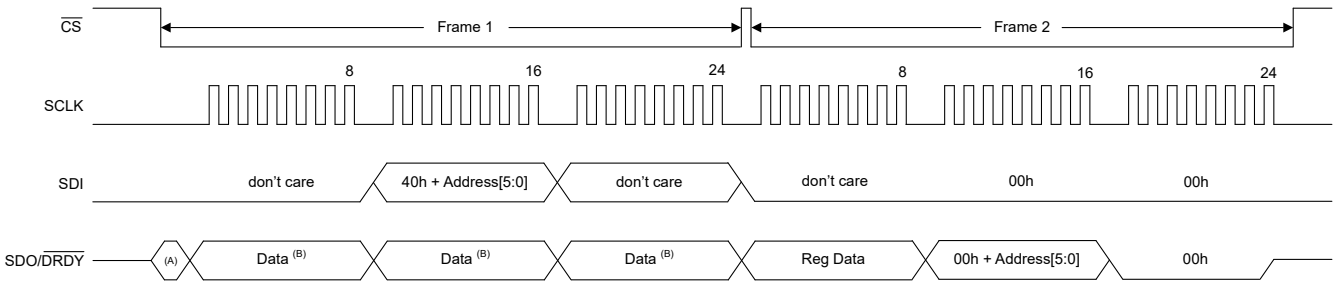
7.5.4.2 Read Register Command

Use the read register command to read register data. The command follows a two-frame protocol in which the read command is sent in one frame and the ADC responds with register data in the next frame. The first byte of the command is the base command value (40h) added to the 6-bit register address. The value of the second command byte is arbitrary, but is used together with the first byte for the CRC calculation.

Figure 7-29 shows an example of reading register data for the 24-bit device with the STATUS header and CRC disabled. Frame 1 is the command frame and frame 2 is the data response frame. The frames are delimited by taking $\overline{\text{CS}}$ high. The data response frame returns the requested register data byte, followed by the register address indication byte, and a 00h padded byte to complete the 24-bit frame. The register data is most-significant-bit first aligned. The 6-bit register address is right-aligned within the register address indication byte (padded with 00b at the MSB position). If desired, the data response frame can be shortened after the register data byte by taking $\overline{\text{CS}}$ high.

Reading from a register address outside the valid address range returns 00h as the register data and FFh in the register address indication byte to indicate an error.

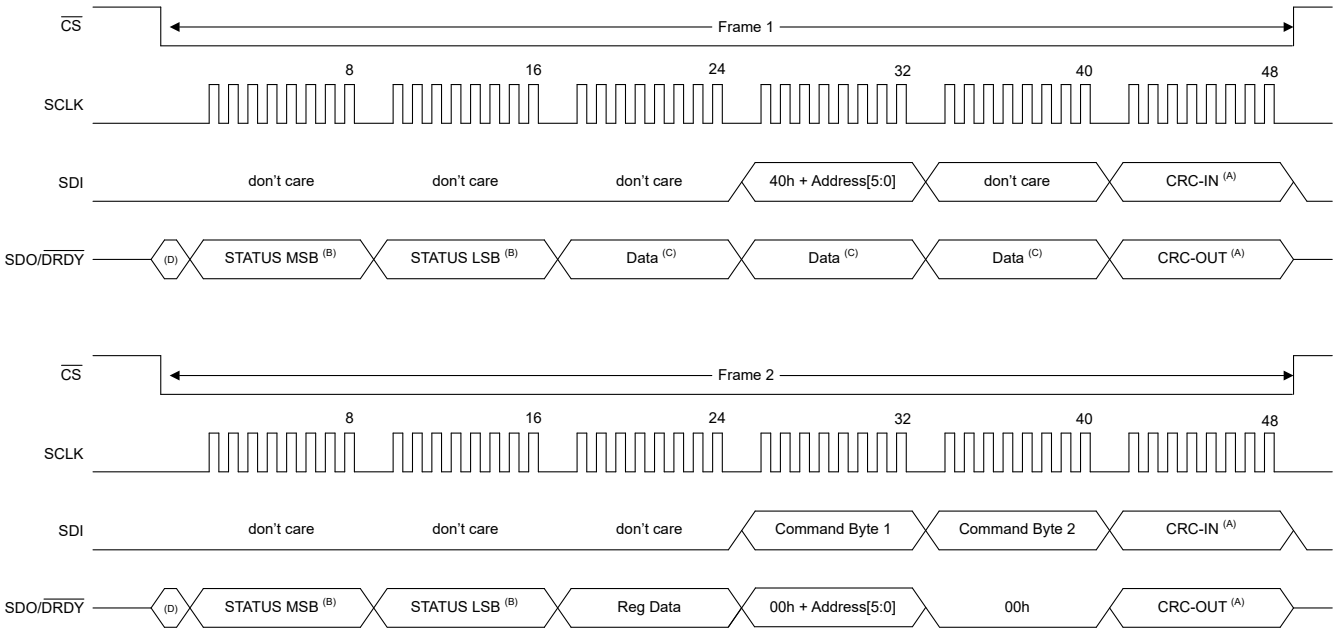
When reading multiple registers, full-duplex operation can be used to double the throughput of the read register operations by inputting the next read register command during the data response frame of the previous register.



A. Previous state of SDO/$\overline{\text{DRDY}}$ before first SCLK.
B. Data are either 24 bits of conversion data, or if the read register command is sent in the prior frame, the data field is the register data byte + address indication byte + 00h padding.

Figure 7-29. Read Register Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-30 shows an example of a register read operation for the 24-bit device with the STATUS header and CRC enabled. In frame 1, conversion data are output at the same time as the read register command is input (when the previous frame is not a read register command). The input command is padded with three don't care bytes to match the length of the output data frame. The padded input bytes are excluded from the CRC-IN code calculation. Frame 2 shows the input of the next command concurrent with the output of the requested register data. The CRC-OUT code includes all preceding bytes within the data output frame.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. Depending on the previous operation, the data field is either conversion data or the register data byte + address indication byte + 00h padding.
D. Previous state of SDO/$\overline{\text{DRDY}}$ before the first SCLK.

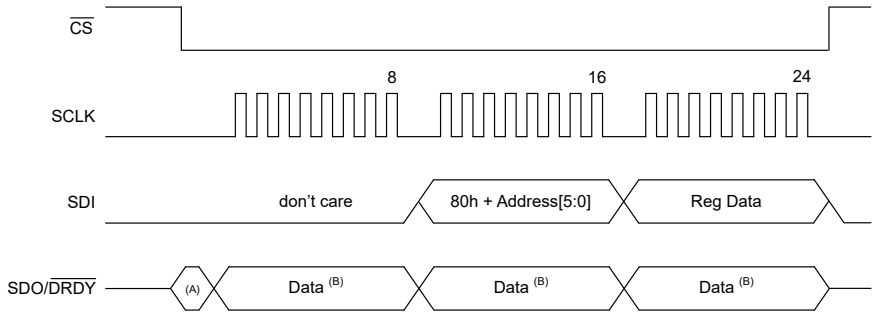
Figure 7-30. Read Register Data (24-Bit Device, STATUS Header and CRC Enabled)

7.5.4.3 Write Register Command

Use the write register command to write register data. The write register operation is performed in a single frame. The first byte of the command is the base value (80h) added to the 6-bit register address. The second byte of the command is the register data.

Writing to registers outside the valid address range is ignored and the REG_WRITE_FAULTn bit is set to 0b to indicate an error.

Figure 7-31 shows an example of a register write operation for the 24-bit device with the STATUS header and CRC disabled. A shortened 16-bit frame can be used to increase throughput if a series of registers need to be configured without reading out conversion data at the same time. Shortened SPI frames cannot be used in 3-wire SPI mode or when operating the device in a daisy-chain.

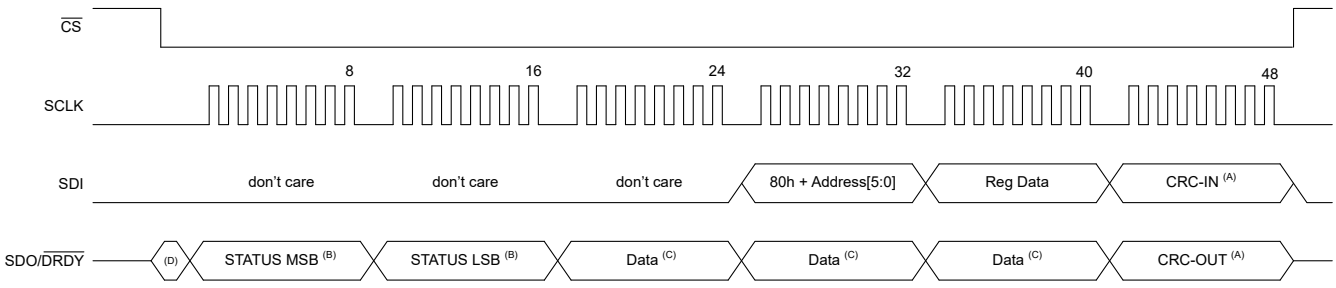


A. Previous state of SDO/DRDY before the first SCLK.
B. Data are either the conversion data, or if the read register command was sent in a prior frame, the data field is register data byte + address indication byte + 00h padding.

Figure 7-31. Write Register Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-32 shows an example of a write register operation for the 24-bit device with the STATUS header and CRC enabled. Full-duplex operation is also illustrated to show simultaneous input of a command and output of conversion data. The input frame is prefixed with three *don't care* bytes to match the output frame so all conversion data bytes are transmitted. A shortened 24-bit frame can be used to increase throughput if a series of registers need to be configured without reading out conversion data at the same time.

Verify successful register write operations by either reading back the register data, or by checking the SPI_CRC_FAULTn bit for input CRC errors. If an SPI CRC input error occurred, the SPI_CRC_FAULTn flag reads 0b in the following frame and the write operation is ignored.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. The data field is either conversion data, or if the read register command was sent in the prior frame, register data byte + address indication byte + 00h padding.
D. Previous state of SDO/DRDY before the first SCLK.

Figure 7-32. Write Register Data (24-Bit Device, STATUS Header and CRC Enabled)

7.5.5 Continuous-Read Mode

The ADS1x4S1x offer a continuous-read mode. In continuous-read mode, an arbitrary number of register data can be retrieved without any transitions of $\overline{CS}$, and the frame extends to accommodate the additional data. This simplifies the process of reading a large amount of register data, and reduces the overhead on the microcontroller peripheral which controls the $\overline{CS}$ line.

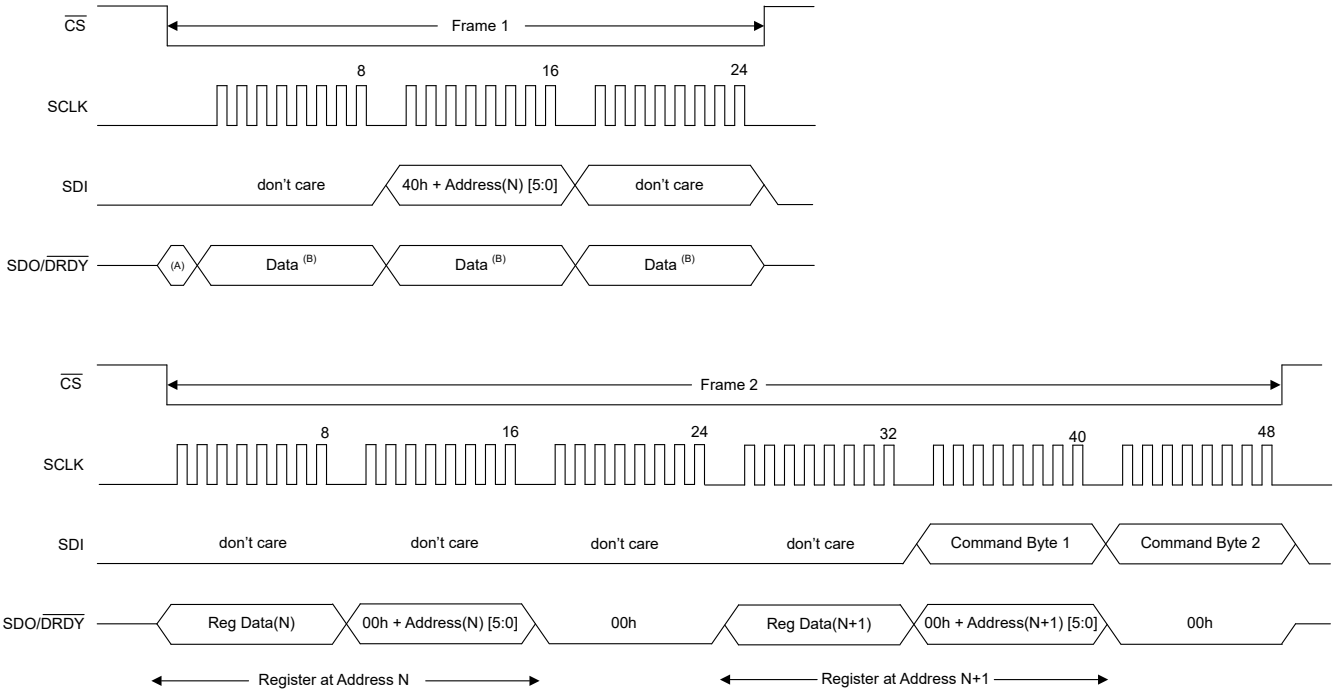
Setting the CONT_READ_EN bit enables continuous-read mode. The SPI switches to continuous-read mode in the next frame following the SPI frame which changed the CONT_READ_EN bit from 0b to 1b.

The SPI returns to the single-read mode by setting the CONT_READ_EN bit back to 0b.

7.5.5.1 Read Registers in Continuous-Read Mode

In continuous-read mode, use the same command frame to read register data as explained in the *Read Register Command* section. The data response frame returns one or multiple register data bytes depending on when $\overline{CS}$ is driven back high. The first register data byte is read from the address specified in the command frame. The register address is then automatically incremented by 1 for each subsequent register read. This is also true if the next register address points to an invalid register. The response to registers outside the valid address range is 00h for the data byte, and FFh for the address indicator byte.

Figure 7-33 shows an example of reading register data in continuous-read mode for the 24-bit device with the STATUS header and CRC disabled. This example shows reading of two consecutive registers N and N+1, however an arbitrary number of registers can be read when holding $\overline{CS}$ low for additional clock periods.

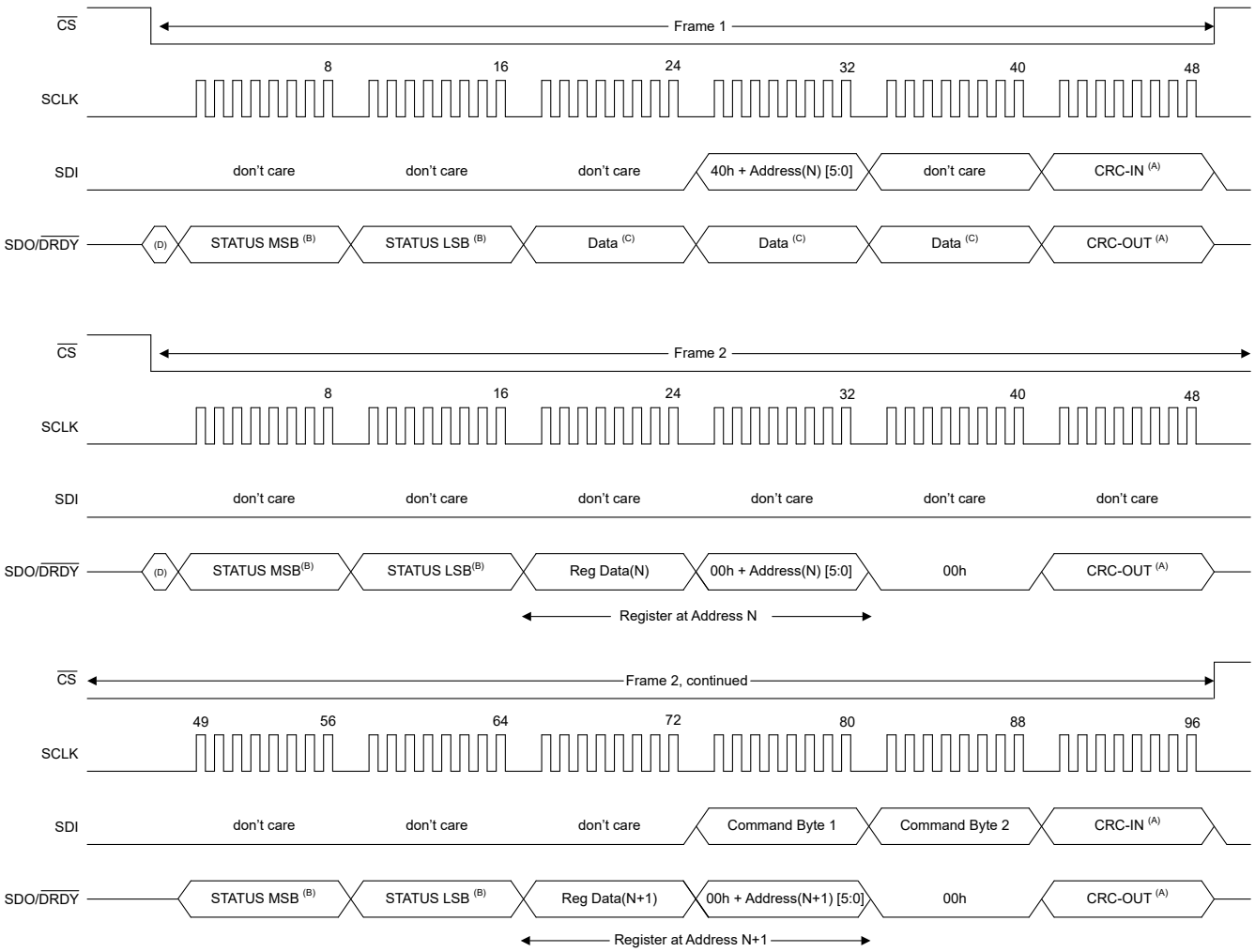


A. Previous state of SDO/$\overline{DRDY}$ before first SCLK.

B. Depending on the previous operation, the data field is either conversion data or the register data byte + address byte + 00h padding.

Figure 7-33. Read Register Data in Continuous-Read Mode (24-Bit Device, STATUS header and CRC Disabled)

Figure 7-34 shows an example of the register read operation in continuous-read mode for the 24-bit device with the STATUS header and CRC enabled. In the input and output frame, don't care bytes and 00h pad bytes are used to match the data frame protocol as explained in the *Read Register Command* section. This example shows reading of two consecutive registers N and N+1, however an arbitrary number of registers can be read when holding $\overline{CS}$ low for additional clock periods.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. Depending on the previous operation, the data field is either conversion data or the register data byte + address byte + 00h padding.
D. Previous state of SDO/$\overline{\text{DRDY}}$ before first SCLK.

Figure 7-34. Read Register Data in Continuous-Read Mode (24-Bit Device, STATUS header and CRC Enabled)

7.5.6 Daisy-Chain Operation

In systems using multiple ADCs, the devices can be connected in a daisy-chain string to reduce the number of SPI connections. A daisy-chain connection links together the SPI output (SDO) of one device to the SPI input (SDI) of the next device so the devices in the chain appear as a single logical device to the host controller. There is no special programming required for daisy-chain operation. Apply additional shift clocks to access all devices in the chain. For simplified operation, program the same SPI frame size for each device (for example, when enabling the CRC option of all devices, thus producing a 24-bit (16-bit device), or 32-bit (24-bit device) frame size).

Figure 7-35 shows four devices connected in a daisy-chain configuration. SDI of ADS1x4S1x (1) connects to the host SPI data output, and SDO/$\overline{\text{DRDY}}$ of ADS1x4S1x (4) connects to the host SPI data input. The shift operation is simultaneous for all devices in the chain. After each ADC shifts out the conversion data, the data of SDI appears on SDO/$\overline{\text{DRDY}}$ to drive the SDI of the next device in the chain. The shift operation continues until the last device in the chain is reached. The SPI frame ends when $\overline{\text{CS}}$ is taken high, at which time the data shifted into each device is interpreted. For daisy-chain operation, program the SDO/$\overline{\text{DRDY}}$ pin to data output only mode (SDO_MODE = 0b) and disable continuous-read mode (CONT_READ_EN = 0b).

Connect a pullup resistor on the SDO/$\overline{\text{DRDY}}$ pin of each device to IOVDD. When $\overline{\text{CS}}$ is high, SDO/$\overline{\text{DRDY}}$ goes high-Z. The pullup resistors are therefore used to avoid a floating SDI input on the next device in the chain when $\overline{\text{CS}}$ is high.

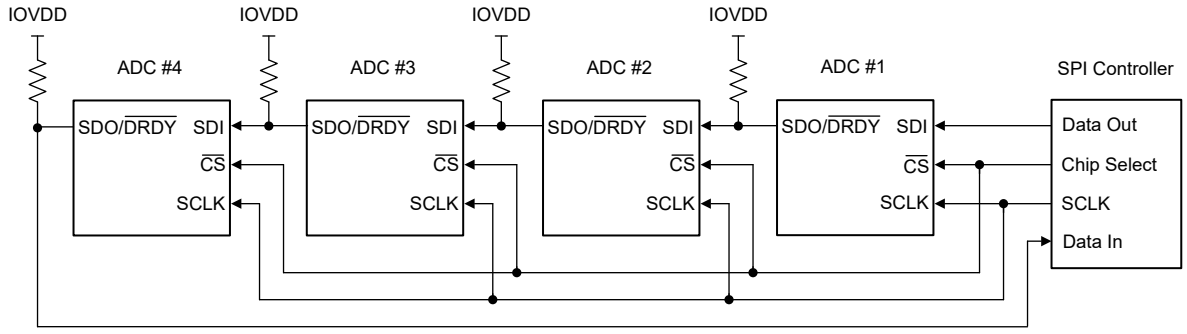


Figure 7-35. Daisy-Chain Connection

Figure 7-36 shows the frame structure for four 24-bit devices connected in a daisy-chain with the STATUS header and CRC disabled.

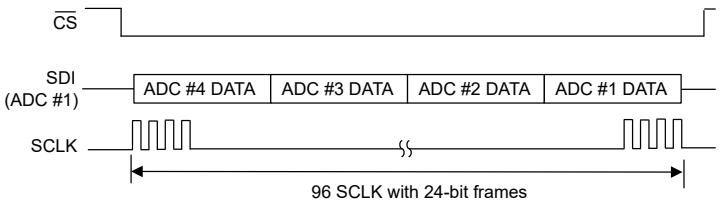
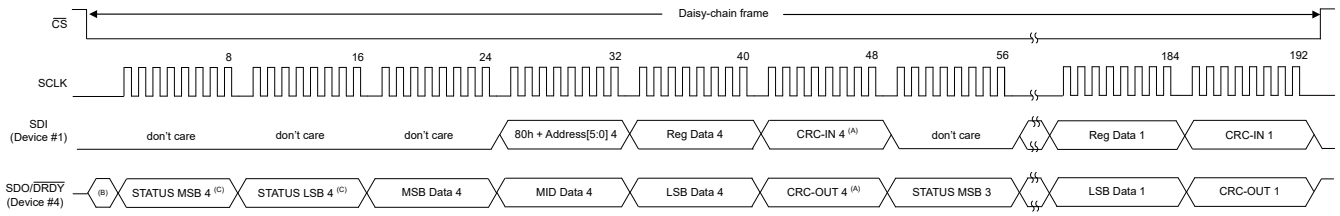


Figure 7-36. Daisy-Chain Data Input Sequence (Four 24-Bit Devices, STATUS Header and CRC Disabled)

To input data, the host first shifts in the data intended for the last device in the chain. The number of input bytes for each ADC is sized to match the output frame size. The default frame size is 24 bits (for a 24-bit device), so initially each ADC requires three bytes by prefixing a pad byte in front of the two command bytes. The input data of ADC #4 is shifted in first, followed by the input data of ADC #3, and so forth.

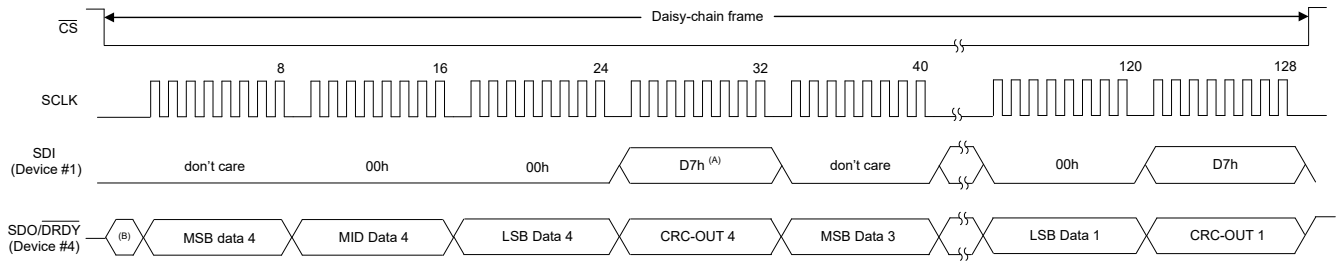
Figure 7-37 shows the detailed input data sequence for the daisy-chain write register operation of Figure 7-35. 48-bit frames for each ADC are shown (24 bits of data, with the STATUS header and CRC enabled). Command operations can be different for each ADC. A register read operation requires a second frame operation to read out the register data.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.
C. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.

Figure 7-37. Write Register Data in Daisy-Chain Connection (Four 24-Bit Devices, STATUS Header and CRC Enabled)

Figure 7-38 shows the data sequence to read conversion data from the device connection provided in Figure 7-35. This example illustrates a 32-bit output frame (24 bits of data, with CRC enabled). The conversion data of ADC (4) is shifted out first in the sequence, followed by the data of ADC (3), and so on. The total number of SCLKs required to shift out the data is given by the number of bits per frame × the number of devices in the chain. In this example, 32-bit output frames × four devices result in 128 total clocks.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.

Figure 7-38. Read Conversion Data in Daisy-Chain Connection (Four 24-Bit Devices, STATUS Header Disabled, CRC Enabled)

As shown in Equation 20, the maximum number of devices connected in a daisy-chain configuration is limited by the SCLK signal frequency, the selected data rate, and the number of bits per frame.

$$\text{Maximum devices in a chain} = \lfloor f_{SCLK} / (f_{DATA} \times \text{bits per frame}) \rfloor \quad (20)$$

For example, if f_{SCLK} = 10MHz, f_{DATA} = 64kSPS, and 32-bit frames are used, the maximum number of daisy-chain connected devices is the floor of: $\lfloor 10\text{MHz} / (64\text{kHz} \times 32) \rfloor = 4$.

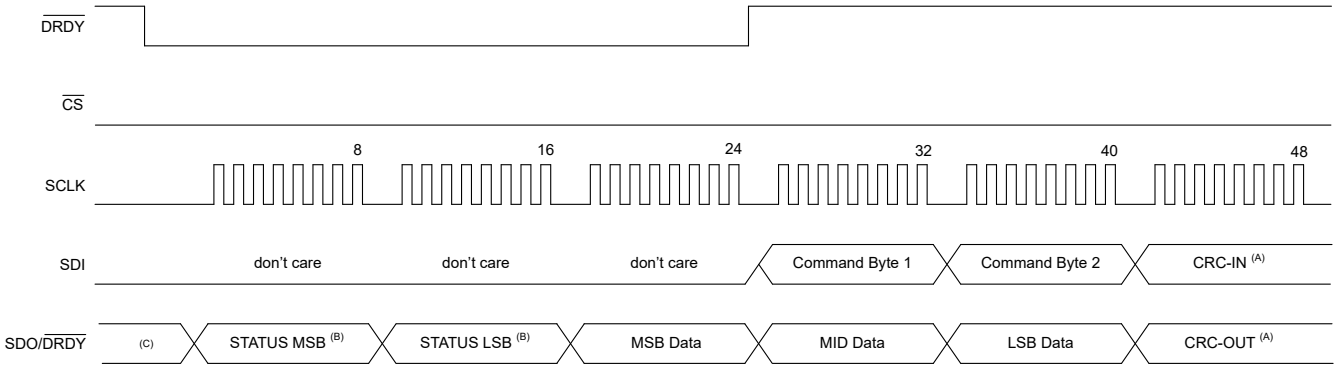
7.5.7 3-Wire SPI Mode

The device can be operated in 3-wire SPI mode by tying the $\overline{CS}$ pin permanently to GND. When $\overline{CS}$ is tied low at power-up or after reset, the device operates in 3-wire SPI mode. The device changes to 4-wire SPI mode any time $\overline{CS}$ is taken high.

Because $\overline{CS}$ no longer controls the frame length in 3-wire SPI mode, SCLKs are counted by the ADC to determine the beginning and ending of a frame. The number of SCLKs must be controlled by the host and must match the size of the output frame. The number of bits per frame depend on the device resolution and configuration. The size of the output frame is shown in Table 7-21. Because frame timing is determined by the number of SCLKs, avoid inadvertent SCLK transitions, such as those possibly occurring at power up.

3-wire SPI mode supports the same command format and clocking as the 4-wire mode, except there is no $\overline{CS}$ toggling. Figure 7-39 shows an example for reading conversion data in 3-wire SPI mode.

Daisy-chain connection of devices is not possible in 3-wire SPI mode, and also continuous-read mode is not available.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-39. Read Conversion Data in 3-Wire SPI Mode (24-Bit Device, STATUS Header and CRC Enabled)

7.5.7.1 3-Wire SPI Mode Frame Re-Alignment

In 3-wire SPI mode, an unintended SCLK can misalign the frame, resulting in loss of frame synchronization to the host. As shown in Figure 7-40, the SPI is resynchronized without requiring a device reset by sending an SPI re-align pattern. The re-align pattern is a minimum of 63 consecutive 1s followed by one 0 at the 64th SCLK. The 65th SCLK starts a new SPI frame. The device also accepts a re-align pattern with more than 63 consecutive 1s followed by one 0. In that case, the new frame starts with the SCLK rising edge following the 0. Optionally, the ADC can be completely reset by toggling the $\overline{RESET}$ pin or by using the reset pattern shown in the *Reset by SPI Input Pattern* section.

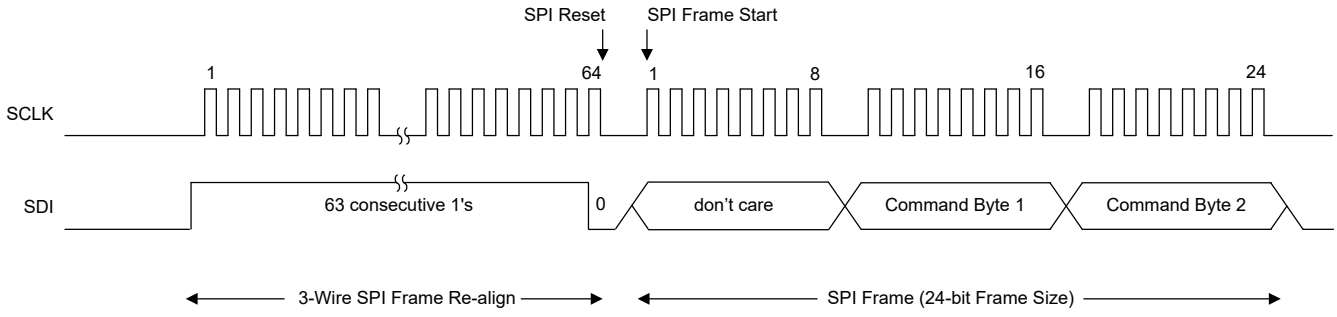


Figure 7-40. 3-Wire Mode SPI Re-Align Pattern (24-Bit Device)

7.5.8 Monitoring for New Conversion Data

There are several methods available to determine when new conversion data are ready for retrieval.

1. Monitor the $\overline{\text{DRDY}}$ or the SDO/$\overline{\text{DRDY}}$ pin.
2. Evaluate the DRDY bit and conversion counter transmitted as part of the STATUS header.
3. Clock counting using an external clock: Count the number of ADC main clocks to predict when data are ready.

7.5.8.1 $\overline{\text{DRDY}}$ Pin or SDO/$\overline{\text{DRDY}}$ Pin Monitoring

$\overline{\text{DRDY}}$ is a dedicated data-ready output pin, and the SDO/$\overline{\text{DRDY}}$ pin is a dual-function output pin. See the *Data Ready ($\overline{\text{DRDY}}$) Pin* section for a description of the $\overline{\text{DRDY}}$ pin and the *Serial Data Output/Data Ready (SDO/$\overline{\text{DRDY}}$)* section for a description of the SDO/$\overline{\text{DRDY}}$ pin.

A falling edge on the $\overline{\text{DRDY}}$ pin indicates that a new conversion completed. Connect the $\overline{\text{DRDY}}$ pin to a falling edge triggered interrupt-capable GPIO of the host controller. After the host detected the falling $\overline{\text{DRDY}}$ signal edge, the host reads the conversion data before the next $\overline{\text{DRDY}}$ falling edge. If an interrupt-capable GPIO is not available, the host can monitor the $\overline{\text{DRDY}}$ pin level. A logic low level indicates that the latest available conversion result has not been read. A logic high level indicates that no new conversion results are available, and that the latest conversion result has been read previously. Conversion data can be read at any time without concern of data corruption.

The SDO/$\overline{\text{DRDY}}$ pin can be used in a similar fashion as the dedicated $\overline{\text{DRDY}}$ pin when the dual function is enabled using the SDO_MODE = 1b setting. However, in contrast to the $\overline{\text{DRDY}}$ pin, the SDO/$\overline{\text{DRDY}}$ pin is only driven when $\overline{\text{CS}}$ is low. That means, the host has to drop the $\overline{\text{CS}}$ line to evaluate the SDO/$\overline{\text{DRDY}}$ signal.

7.5.8.2 Reading DRDY Bit and Conversion Counter

A software method to determine when new data are available for readout is to evaluate the DRDY bit as part of the STATUS header. For that purpose, enable the STATUS header transmission on SDO using the STATUS_EN bit. Two methods to evaluate the DRDY bit can be used:

- The host periodically reads a full SPI frame to receive the STATUS header together with the conversion data. If the DRDY bit in that frame reads 1b, the received conversion data are new. If the DRDY bit is 0b, the host discards the conversion data received in that frame because the same conversion result has been read previously.
- The host periodically sends a short 8-bit SPI frame to read the DRDY bit which is transmitted within the first byte on SDO. Only if the DRDY bit reads 1b, the host sends a full SPI frame to receive the STATUS header together with the new conversion data. This method of short-cycling the SPI frame cannot be used in 3-wire SPI mode or when operating the device in a daisy-chain.

To avoid missing data, evaluate the DRDY bit at least as often as the output data rate.

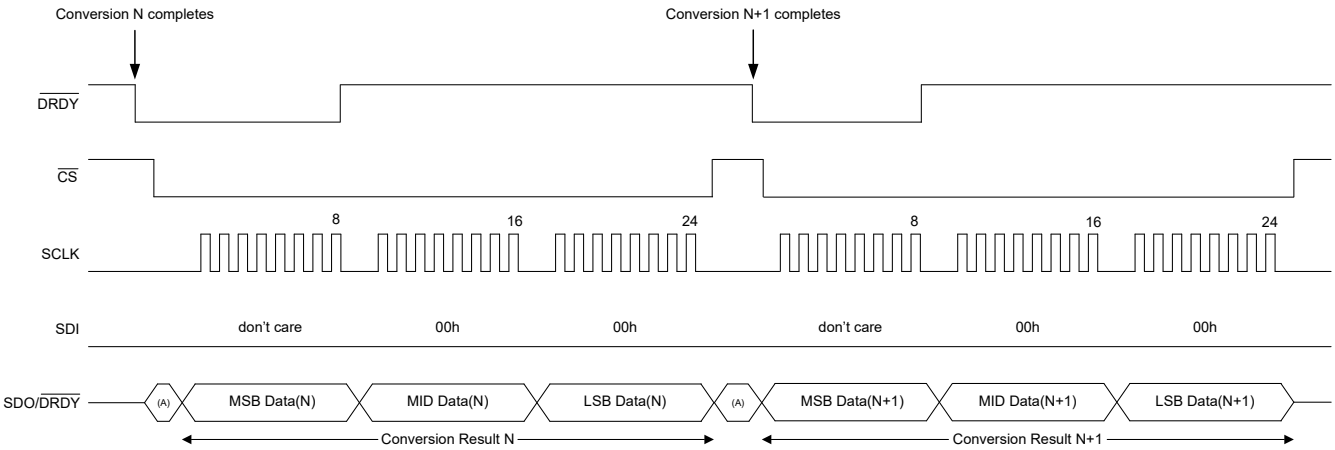
In addition, the conversion counter transmitted as part of the STATUS header indicates the count of the conversion that is retrieved within the current SPI frame. The host evaluates the conversion counter to understand if the host read the same conversion result multiple times or if the host missed to read a conversion result.

7.5.8.3 Clock Counting

Another method to determine when new data are ready is to count ADC main clock cycles, because each conversion requires a deterministic amount of clock cycles. This method is only possible when using an external clock because the internal clock oscillator is not observable. When the sequencer selects a new sequence step for conversion, the number of clock cycles required for the first conversion to complete is larger compared to the clock cycles required for all following conversions of this sequence step. See the *Digital Filter Latency* section for details.

7.5.9 $\overline{DRDY}$ Pin Behavior

This section provides details about the $\overline{DRDY}$ pin behavior in various scenarios. $\overline{DRDY}$ transitions low whenever new conversion data complete. As shown in Figure 7-41, $\overline{DRDY}$ transitions high at the eighth SCLK falling edge of the conversion data MSB read.

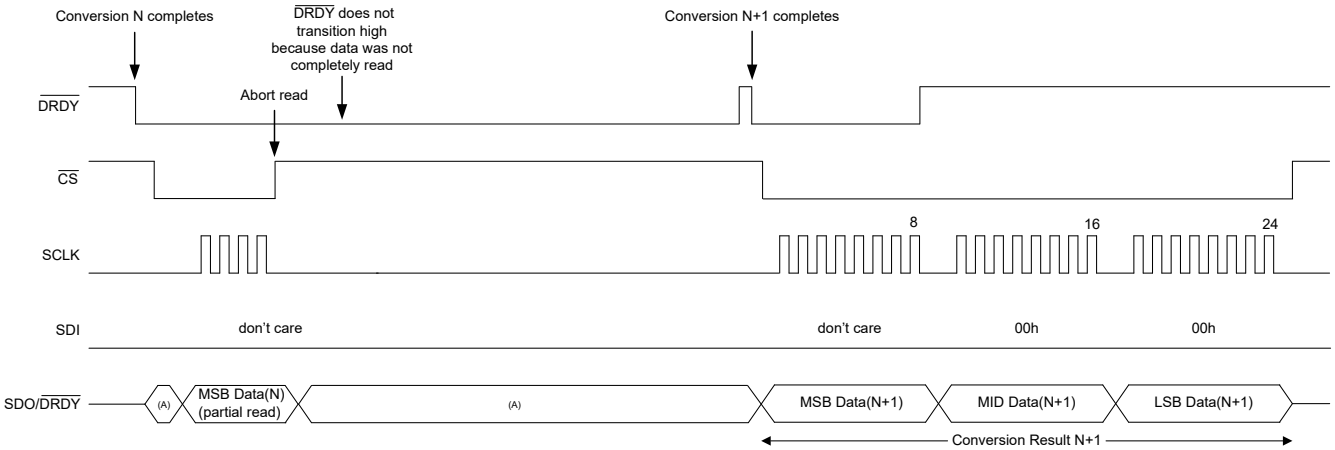


A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-41. $\overline{DRDY}$ Pin Behavior: Reading Latest Available Conversion Data

If $\overline{DRDY}$ is low when a new conversion completes, then $\overline{DRDY}$ drives high $t_{w(DRH)}$ before the $\overline{DRDY}$ falling edge (see Figure 7-42).

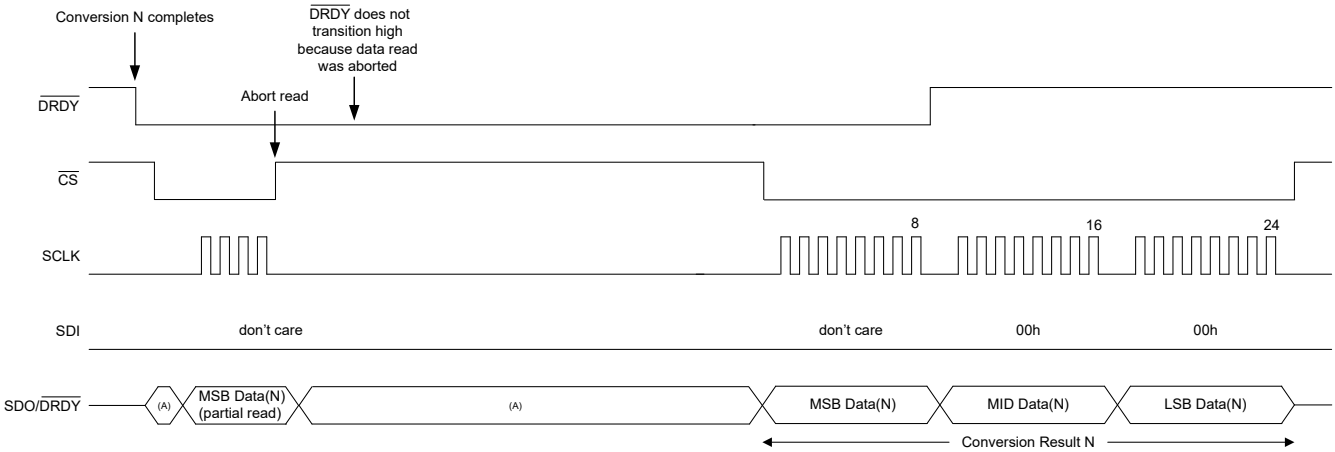
If $\overline{CS}$ is driven high before the eighth SCLK of the conversion data MSB read, then $\overline{DRDY}$ stays low, indicating that conversion data were not read (see Figure 7-42 and Figure 7-43).



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-42. $\overline{DRDY}$ Pin Behavior: Incomplete Read of Conversion Data Before New Conversion Completes

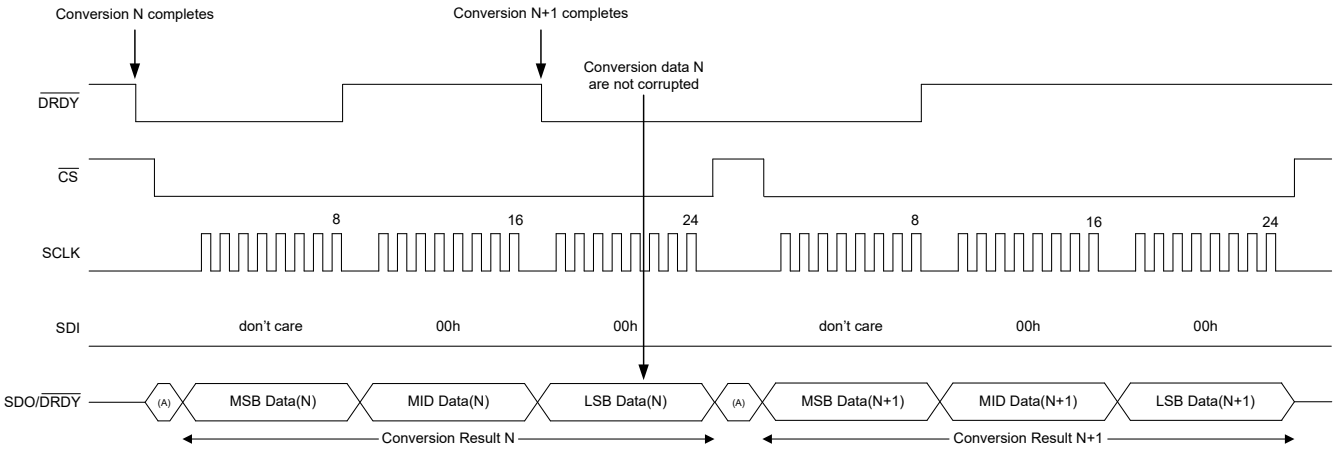
Figure 7-43 shows that the same conversion data can be read multiple times until new conversions complete. The conversion counter (CONV_COUNT[3:0] bits in the STATUS_LSB register) indicates if the same data are read again or if new data are read.



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-43. $\overline{\text{DRDY}}$ Pin Behavior: Incomplete Read of Conversion Data Followed by Complete Read of Same Conversion Data

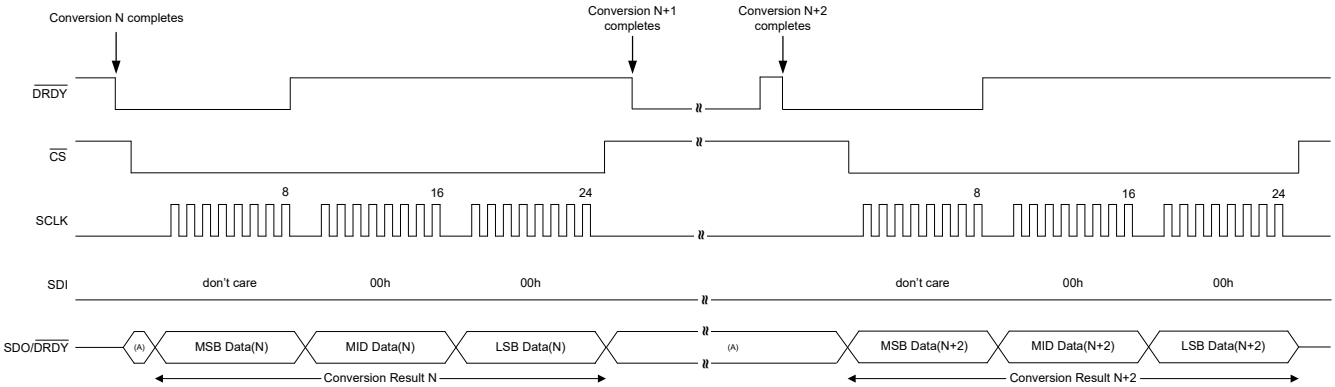
The device avoids data corruption if new conversions N+1 complete while conversion data N are being read. Conversion data N+1 are held in an internal buffer until the read of conversion data N is complete. In the following frame, conversion data N+1 are loaded into the SDO output buffer. $\overline{\text{DRDY}}$ does not transition high after conversion data N have been read in this case to indicate that new conversion data N+1 are available for readout (see Figure 7-44).



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-44. $\overline{\text{DRDY}}$ Pin Behavior: Reading Conversion Data While New Conversion Completes

Figure 7-45 illustrates that conversion data N+1 are lost when the host does not read the data before conversions N+2 complete. The conversion counter is helpful in this situation to detect if the host missed reading the intermediate conversion results.



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-45. $\overline{\text{DRDY}}$ Pin Behavior: Missed Reading Intermediate Conversion Results

Whenever the device is programmed to enter standby mode (STBY_MODE bit = 1b) after conversions stopped, $\overline{\text{DRDY}}$ is driven back high 4 t_{MOD} after transitioning low. Figure 7-46 shows an example of the $\overline{\text{DRDY}}$ pin behavior when entering standby mode.

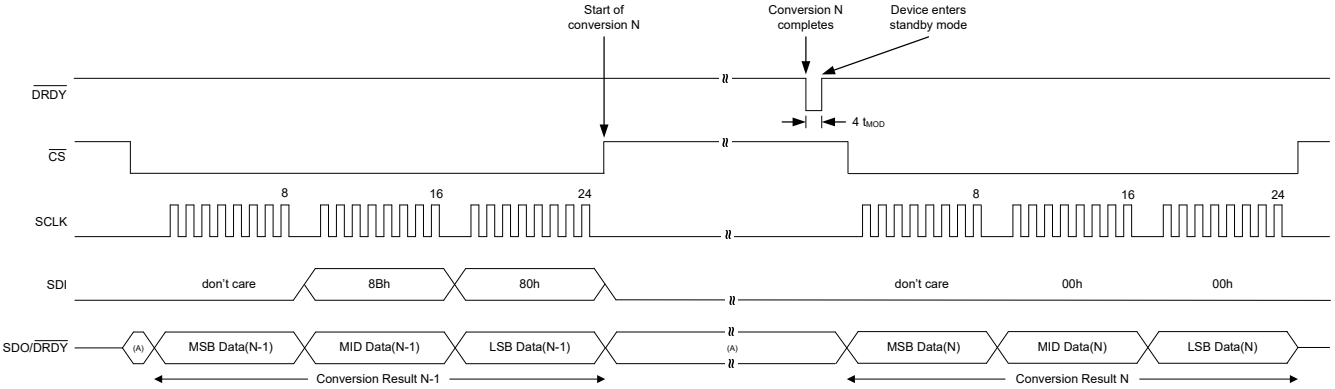


Figure 7-46. $\overline{\text{DRDY}}$ Pin Behavior: Entering Standby Mode

Polling the DRDY bit or the *state* of the $\overline{\text{DRDY}}$ pin to check for the completion of the conversion is not practical in this particular scenario (STBY_MODE bit = 1b) because of the short period the $\overline{\text{DRDY}}$ pin is low. Use one of the other available options to determine when new data are available, such as the $\overline{\text{DRDY}}$ pin falling edge, polling the conversion counter, or waiting a fixed amount of time equal to or longer than the conversion period.

7.5.10 Register Map CRC

The register map CRC detects unintended bit changes in the register map contents. Enable the register map CRC using the REG_MAP_CRC_EN bit. When the register map CRC is enabled, the device constantly calculates an individual 8-bit CRC value for each of the 24 register pages and compares the internal CRC calculation results against the CRC values provided by the user in the GENERAL_CFG_REG_MAP_CRC_VALUE[7:0] and STEPx_REG_MAP_CRC_VAL[7:0] bit fields. If the internal CRC calculation result and the respective user-provided register map CRC value on one or more pages do not match, the REG_MAP_CRC_FAULTn flag sets to 0b and the CRC_FAULT_PAGE[4:0] bit field points to the first register page where a CRC error occurred on. No other action is taken by the device in the event of a register map CRC fault.

Table 7-24 shows which register address spaces the register map CRC covers per page.

Table 7-24. Register Address Space covered by Register Map CRC per Register Page

REGISTER PAGE	COVERED REGISTER ADDRESS SPACE	USER-PROVIDED REGISTER MAP CRC VALUE BIT FIELD
Status and General Configuration	10h to 1Fh	GENERAL_CFG_REG_MAP_CRC_VALUE[7:0]
Step x Configuration (x = 0 to 23)	00h to 14h	STEPx_REG_MAP_CRC_VAL[7:0]

The CRC calculation on each page begins with the MSB of the first covered register and ends with the LSB of the last covered register using the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. See the *SPI CRC* section for details on the CRC calculation. The CRC calculation is initialized with the seed value of FFh.

The REG_MAP_CRC_FAULTn flag does not indicate unintended bit changes immediately because the CRC calculation is implemented serially. Up to $t_{p(REG\_MAP\_CRC)}$ = 208 t_{MOD} cycles can elapse for the REG_MAP_CRC_FAULTn flag to indicate a fault.

Use the following procedure to change register bits without accidentally causing a REG_MAP_CRC_FAULTn indication:

- Disable the register map CRC by setting REG_MAP_CRC_EN = 0b
- Wait the fault response time $t_{p(REG\_MAP\_CRC)}$
- If the REG_MAP_CRC_FAULTn flag is set to 0b, clear the fault flag by writing 1b to the REG_MAP_CRC_FAULTn bit
- Optional: Verify the REG_MAP_CRC_FAULTn fault flag is cleared to 1b
- Change the device register bits as needed
- Update the GENERAL_CFG_REG_MAP_CRC_VALUE[7:0] and STEPx_REG_MAP_CRC_VAL[7:0] bit fields based on the new register map settings. Remember to calculate the GENERAL_CFG_REG_MAP_CRC_VALUE[7:0] based on the REG_MAP_CRC_EN bit being 1b.
- Enable the register map CRC by setting REG_MAP_CRC_EN = 1b

Register bits can also be changed while the register map CRC is enabled, as discussed in the following procedure, but can cause unintended REG_MAP_CRC_FAULTn indications.

- Change the register bits as needed while the register map CRC is enabled
- Update the GENERAL_CFG_REG_MAP_CRC_VALUE[7:0] and STEPx_REG_MAP_CRC_VAL[7:0] bit fields based on the new register map settings
- Wait the fault response time $t_{p(REG\_MAP\_CRC)}$
- If the REG_MAP_CRC_FAULTn flag is set to 0b, clear the fault flag by writing 1b to the REG_MAP_CRC_FAULTn bit
- Optional: Verify the REG_MAP_CRC_FAULTn fault flag is cleared to 1b

The register map CRC stops in standby and power-down mode irrespective of the REG_MAP_CRC_EN bit setting.

7.5.11 Conversion Data Format

Conversion data are coded depending on the STEPx_CODING bit setting. By default, conversion data are coded in binary two's-complement format, MSB first (sign bit). Set the STEPx_CODING bit to 1b for unipolar straight binary format. Table 7-25 and Table 7-26 show the output code for the 16-bit and 24-bit device, respectively. In binary two's-complement format, the conversion data clips to positive and negative full-scale codes when the input signal exceeds the respective positive and negative full-scale values. In unipolar straight binary format, conversion data clips to the full-scale code when the input signal exceeds the full-scale value, or to the zero code when the input signal value is below zero.

Table 7-25. Ideal Output Code Versus Input Signal (16-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT (CODING = 0b)	UNIPOLAR STRAIGHT BINARY FORMAT (CODING = 1b)
≥ FSR × (2^{16} – 1) / 2^{16}	7FFFh	FFFFh
≥ FSR × (2^{15} – 1) / 2^{15}		FFFEh
FSR / 2^{15}	0001h	0002h
0	0000h	0000h
–FSR / 2^{15}	FFFFh	
–FSR × (2^{15} – 1) / 2^{15}	8001h	
≤ –FSR	8000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

Table 7-26. Ideal Output Code Versus Input Signal (24-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT (CODING = 0b)	UNIPOLAR STRAIGHT BINARY FORMAT (CODING = 1b)
≥ FSR × (2^{24} – 1) / 2^{24}	7FFFFFh	FFFFFFh
≥ FSR × (2^{23} – 1) / 2^{23}		FFFFFEh
FSR / 2^{23}	000001h	000002h
0	000000h	000000h
–FSR / 2^{23}	FFFFFFh	
–FSR × (2^{23} – 1) / 2^{23}	800001h	
≤ –FSR	800000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

8 Register Map

The ADS1x4S1x register space is organized in multiple register pages as shown in Table 8-1.

Table 8-1. Register Pages Overview

PAGE ADDRESS	PAGE NAME
00h	Status and General Configuration
01h	Step 0 Configuration
02h	Step 1 Configuration
...	...
18h	Step 23 Configuration

The "Status and General Configuration Page" (page 0) holds status information and general configuration settings that apply globally to the device across all sequence steps. See the *Status and General Configuration Page Registers* section for the register map of the Status and General Configuration page.

A separate register page exists for each sequence step configuration (pages 1 to 24), referred to as the "Step Configuration Pages". All step configuration registers and bit fields use the prefix "STEPx", where x = 0 to 23 indicates the sequence step number. See the *Step Configuration Page Registers* section for the register map of a Step Configuration page x.

Use the PAGE_POINTER register, which is located at register address 3Fh on every page, to select a register page for configuration. After power-up and reset, page 0 is selected. To select another page for configuration, write the address of the new register page into the PAGE_POINTER[7:0] bit field. Thereafter, the device selects the new page and all following register read and write operations take effect on that new page. Read back the PAGE_INDICATOR register to confirm the device switched to the correct page address.

8.1 Status and General Configuration Page Registers

Table 8-2 lists the memory-mapped registers for the Status and General Configuration Page Registers registers. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-2. Register Map

Address	Acronym	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID Registers - not covered by register map CRC										
00h	DEVICE_ID	XXh	RESERVED		CH_CNT[1:0]		DEV_ID[3:0]			
01h	REVISION_ID	XXh	REV_ID[7:0]							
Status Registers (Aggregate Bits) - not covered by register map CRC										
02h	STATUS_MSB	00h	STEP_INDICATOR[4:0]					SAD_FAULTn	RESETn	DRDY
03h	STATUS_LSB	FFh	CONV_COUNT[3:0]				RESERVED		REG_WRITE_FAULTn	SPI_CRC_FAULTn
Status Registers (Individual Bits) - not covered by register map CRC										
04h	SUPPLY_STATUS	BFh	RESERVED	AVDD_UVn	RESERVED					
05h	ADC_STATUS	FFh	COMP_ALERTn	RESERVED		REF_UVn	RESERVED			
06h	DIGITAL_STATUS	FFh	MEM_FAULTn	RESERVED	CRC_FAULT_PAGE[4:0]					REG_MAP_CRC_FAULTn
07h	COMP_ALERT_STATUS	FFh	RESERVED			COMP_ALERT_STEP_INDICATOR[4:0]				
Status Register (GPIOs) - not covered by register map CRC										
08h	GPIO_DATA_INPUT	00h	GPIO7_DAT_IN	GPIO6_DAT_IN	GPIO5_DAT_IN	GPIO4_DAT_IN	GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	GPIO0_DAT_IN
Status Registers (Sequencer) - not covered by register map CRC										
09h	SEQ_STATUS	07h	SEQ_ACTIVE	SEQ_COUNT[3:0]				RESERVED		
0Ah	RESERVED	00h	RESERVED							
Conversion Control and Reset Registers - not covered by register map CRC										
0Bh	CONVERSION_CTRL	00h	START	STEP_INIT[4:0]					RESERVED	STOP
0Ch	RESET	00h	RESET_CODE[7:0]							
General Configuration Registers										
10h	ADC_CFG	00h	RESERVED	REF_VAL	CLK_SEL	GC_EN	SPEED_MODE[1:0]		STBY_MODE	PWDN
11h	DIGITAL_CFG	00h	SPARE[4:0]					STATUS_EN	SDO_MODE	CONT_READ_EN
12h	VBIAS	00h	VBIAS_AIN7	VBIAS_AIN6	VBIAS_AIN5	VBIAS_AIN4	VBIAS_AIN3	VBIAS_AIN2	VBIAS_AIN1	VBIAS_AIN0
13h	GPIO_CFG0	00h	GPIO3_CFG[1:0]		GPIO2_CFG[1:0]		GPIO1_CFG[1:0]		GPIO0_CFG[1:0]	
14h	GPIO_CFG1	00h	GPIO7_CFG[1:0]		GPIO6_CFG[1:0]		GPIO5_CFG[1:0]		GPIO4_CFG[1:0]	
15h	GPIO_CFG2	08h	RESERVED			COMP_ALERT_MASK	FAULT_PIN_BEHAVIOR	ALERT_PIN_POL	GPIO4_SRC	GPIO3_SRC
16h	MONITOR_CFG	04h	RESERVED				REF_UV_EN	REF_UV_SEL	REG_MAP_CRC_EN	SPI_CRC_EN
17h	RESERVED	00h	RESERVED							
18h	SPARE	00h	SPARE[7:0]							
Sequencer Configuration Registers										
19h	SEQUENCER_CFG	50h	SEQ_MODE[1:0]		STOP_BEHAVIOR[1:0]		RESERVED			
1Ah	SEQUENCE_STEP_EN_0	01h	STEP_7_EN	STEP_6_EN	STEP_5_EN	STEP_4_EN	STEP_3_EN	STEP_2_EN	STEP_1_EN	STEP_0_EN
1Bh	SEQUENCE_STEP_EN_1	00h	STEP_15_EN	STEP_14_EN	STEP_13_EN	STEP_12_EN	STEP_11_EN	STEP_10_EN	STEP_9_EN	STEP_8_EN
1Ch	SEQUENCE_STEP_EN_2	00h	STEP_23_EN	STEP_22_EN	STEP_21_EN	STEP_20_EN	STEP_19_EN	STEP_18_EN	STEP_17_EN	STEP_16_EN
Reserved Registers										
1Dh	RESERVED	00h	RESERVED							
1Eh	RESERVED	00h	RESERVED							
1Fh	RESERVED	00h	RESERVED							
Register Map CRC Value Register										
3Dh	REG_MAP_CRC	00h	GENERAL_CFG_REG_MAP_CRC_VALUE[7:0]							
Page Indicator and Pointer Registers										
3Eh	PAGE_INDICATOR	00h	PAGE_INDICATOR[7:0]							

Table 8-2. Register Map (continued)

Address	Acronym	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Fh	PAGE_POINTER	00h	PAGE_POINTER[7:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-3 shows the codes that are used for access types in this section.

Table 8-3. Status and General Configuration Page Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 DEVICE_ID Register (Address = 00h) [Reset = XXh]

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Figure 8-1. DEVICE_ID Register

7	6	5	4	3	2	1	0
RESERVED		CH_CNT[1:0]		DEV_ID[3:0]			
R-00b		R-xxb		R-xxxxb			

Table 8-4. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00b	Reserved Always reads 00b.
5:4	CH_CNT[1:0]	R	xxb	Channel count 11b = 18 analog inputs 10b = 8 analog inputs
3:0	DEV_ID[3:0]	R	xxxxb	Device ID 0010b = 16 bit 0011b = 24 bit

8.1.2 REVISION_ID Register (Address = 01h) [Reset = XXh]

Return to the Summary Table.

Figure 8-2. REVISION_ID Register

7	6	5	4	3	2	1	0
REV_ID[7:0]							
R-xxxxxxxxb							

Table 8-5. REVISION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Revision ID Values are subject to change without notice.

8.1.3 STATUS_MSB Register (Address = 02h) [Reset = 00h]

Return to the Summary Table.

Figure 8-3. STATUS_MSB Register

7	6	5	4	3	2	1	0
STEP_INDICATOR[4:0]					SAD_FAULTn	RESETn	DRDY
R-00000b					R-0b	R/W-0b	R-0b

Table 8-6. STATUS_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	STEP_INDICATOR[4:0]	R	00000b	Sequence step indicator Indicates the step page configuration that was used for the latest conversion result, which is currently available for readout. The step indicator resets to 00h after a device reset, in power-down mode, or when writing to the SEQUENCER_CFG register. At the same time the conversion counter (CONV_COUNT[3:0]) resets to Fh, the sequence counter (SEQ_COUNT[3:0]) resets to 0h, and the conversion data clears.
2	SAD_FAULTn	R	0b	Supply, ADC, and digital fault flag Indicates if any of the individual fault flags in the SUPPLY_STATUS, ADC_STATUS, or DIGITAL_STATUS registers are set. For this bit to clear, all bits in the SUPPLY_STATUS, ADC_STATUS, and DIGITAL_STATUS registers must be cleared to 1b. The COMP_ALERTn bit can be masked from setting the SAD_FAULTn flag in case the COMP_ALERTn bit is 0b using the COMP_ALERTn_MASK bit. 0b = Fault occurred 1b = No fault occurred
1	RESETn	R/W	0b	Reset flag Indicates a device reset occurred. Write 1b to clear bit to 1b. 0b = Reset occurred 1b = No reset occurred
0	DRDY	R	0b	Data-ready indication bit The DRDY bit is the inverse of the $\overline{\text{DRDY}}$ pin. Enable the transmission of the STATUS header using the STATUS_EN bit to leverage the DRDY bit indication. The DRDY bit indicates if the conversion data read within the current SPI frame are new or are repeated data from the last read operation. Polling the DRDY bit using the register read command is not reliable, because the DRDY bit returns to 0b during the first frame of the read register command transmission already. 0b = Data are not new 1b = Data are new

8.1.4 STATUS_LSB Register (Address = 03h) [Reset = FFh]

Return to the Summary Table.

Figure 8-4. STATUS_LSB Register

7	6	5	4	3	2	1	0
CONV_COUNT[3:0]				RESERVED		REG_WRITE_FAULTn	SPI_CRC_FAULTn
R-1111b				R-11b		R-1b	R-1b

Table 8-7. STATUS_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CONV_COUNT[3:0]	R	1111b	Conversion counter The conversion counter increments every time a new conversion completes. After reaching a counter value of Fh, the counter rolls over to 0h with the completion of the next conversion. The counter only resets to Fh in power-down mode, after a device reset, or when writing to the SEQUENCER_CFG register. At the same time the sequence step indicator (STEP_INDICATOR[4:0]) resets to 00h, the sequence counter (SEQ_COUNT[3:0]) resets to 0h, and the conversion data clears. At the completion of the first conversion after reset, power-down, or after writing to the SEQUENCER_CFG register, the counter reads 0h. When SEQ_MODE[1:0] = 10b or 11b, the counter always reads 0h for the first conversion of a step. When SEQ_MODE[1:0] = 00b or 01b, the counter value does not return to 0h when conversions on a new step page configuration complete. Reset the counter to Fh by writing to the SEQUENCER_CFG register before starting a conversion with a new step page configuration if desired. When the conversion counter is output as part of the STATUS header (STATUS_EN = 1b), the devices make sure that the conversion counter value always matches to the ADC conversion result that is output in the same frame.
3:2	RESERVED	R	11b	Reserved Always reads 11b.
1	REG_WRITE_FAULTn	R	1b	Register write access fault flag Indicates a write access to an invalid register address occurred during the last register write operation. This flag sets when an invalid register address is written to, and updates at the next register write command. Reading from an invalid register address does not set the flag, but can be detected from the address indication inside the SPI frame of the read command. 0b = Fault occurred 1b = No fault occurred
0	SPI_CRC_FAULTn	R	1b	SPI CRC fault flag Indicates a SPI CRC fault occurred on SDI in the previous SPI frame. The execution of the command in the frame where the SPI CRC fault occurred is blocked. Instead, a no operation command is executed. Commands in following frames are not blocked. This bit updates in every new SPI frame based on the CRC result of the previous SPI frame. Enable the SPI CRC using the SPI_CRC_EN bit. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI CRC faults. 0b = Fault occurred 1b = No fault occurred

8.1.5 SUPPLY_STATUS Register (Address = 04h) [Reset = BFh]

Return to the Summary Table.

Figure 8-5. SUPPLY_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	AVDD_UVn	RESERVED					
R-1b	R/W-0b	R-111111b					

Table 8-8. SUPPLY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1b	Reserved Always reads 1b.
6	AVDD_UVn	R/W	0b	AVDD undervoltage fault flag Indicates the AVDD supply voltage dropped below the AVDD undervoltage threshold. AVDD_UVn always sets to 0b when entering power-down mode even when the AVDD supply did not drop below the AVDD undervoltage threshold. Write 1b to clear bit to 1b. 0b = Fault occurred 1b = No fault occurred
5:0	RESERVED	R	111111b	Reserved Always reads 111111b.

8.1.6 ADC_STATUS Register (Address = 05h) [Reset = FFh]

Return to the Summary Table.

Figure 8-6. ADC_STATUS Register

7	6	5	4	3	2	1	0
COMP_ALERTn	RESERVED		REF_UVn	RESERVED			
R/W-1b	R-11b		R/W-1b	R-1111b			

Table 8-9. ADC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMP_ALERTn	R/W	1b	Digital comparator alert flag Indicates the digital comparator on one of the sequence steps tripped. The COMP_ALERT_STEP_INDICATOR[4:0] bit field indicates which sequence step caused the alert. Write 1b to clear bit to 1b. Clearing this bit also resets the ALERT output in case GPIO3 is configured as ALERT output. This flag contributes to the SAD_FAULTn unless COMP_ALERTn_MASK is set to 1b. This flag always drives the ALERT output, regardless of the state of COMP_ALERTn_MASK. 0b = Alert occurred 1b = No alert occurred
6:5	RESERVED	R	11b	Reserved Always reads 11b.
4	REF_UVn	R/W	1b	Reference voltage undervoltage fault flag Indicates the reference voltage selected by the STEPx_REF_SEL[1:0] bits on a certain sequence step dropped below the selected reference undervoltage threshold. Enable the reference undervoltage monitor using the REF_UV_EN bit. Select the reference undervoltage threshold using the REF_UV_SEL bit. Write 1b to clear bit to 1b. 0b = Fault occurred 1b = No fault occurred
3:0	RESERVED	R	1111b	Reserved Always reads 1111b.

8.1.7 DIGITAL_STATUS Register (Address = 06h) [Reset = FFh]

Return to the Summary Table.

Figure 8-7. DIGITAL_STATUS Register

7	6	5	4	3	2	1	0
MEM_FAULTn	RESERVED	CRC_FAULT_PAGE[4:0]					REG_MAP_CRC_FAULTn
R/W-1b	R-1b	R-11111b					R/W-1b

Table 8-10. DIGITAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MEM_FAULTn	R/W	1b	Internal memory fault flag Indicates a memory map CRC fault in the internal memory occurred. Perform a power cycle or reset the device when the bit is 0b. 0b = Fault occurred 1b = No fault occurred
6	RESERVED	R	1b	Reserved Always reads 1b.
5:1	CRC_FAULT_PAGE[4:0]	R	11111b	Register map CRC fault page indicator Indicates which register page shows a CRC error when the REG_MAP_CRC_FAULTn indicates a CRC fault. If multiple register pages have a CRC error, then the indicator points to the first register page address where a CRC error exists. When the CRC error on the page which was indicated by the CRC_FAULT_PAGE[4:0] bit field is corrected by providing a correct register map CRC value, and another CRC error on another register page exists, the CRC_FAULT_PAGE[4:0] bit field does not update automatically. After writing 1b to the REG_MAP_CRC_FAULTn bit field, the REG_MAP_CRC_FAULTn sets to 0b again, and the CRC_FAULT_PAGE[4:0] bit field points to the next remaining first page address which has a register map CRC error. This bit field clears to 11111b when the REG_MAP_CRC_FAULTn flag is cleared to 1b.
0	REG_MAP_CRC_FAULTn	R/W	1b	Register map CRC fault flag Indicates a register map CRC fault on the Status and General Configuration page (register address space from 10h to 1Fh) or on any of the Step Configuration pages (register addresses 00h to 14h) occurred. Enable the register map CRC using the REG_MAP_CRC_EN bit. Write 1b to clear bit to 1b. 0b = Fault occurred 1b = No fault occurred

8.1.8 COMP_ALERT_STATUS Register (Address = 07h) [Reset = FFh]

Return to the Summary Table.

Figure 8-8. COMP_ALERT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			COMP_ALERT_STEP_INDICATOR[4:0]				
R-111b			R-11111b				

Table 8-11. COMP_ALERT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	111b	Reserved Always reads 111b.
4:0	COMP_ALERT_STEP_INDICATOR[4:0]	R	11111b	Digital comparator alert step indicator Indicates which sequence step had a comparator overrange condition when the COMP_ALERTn flag is set. Bits clear to 11111b when the COMP_ALERTn bit is cleared to 1b.

8.1.9 GPIO_DATA_INPUT Register (Address = 08h) [Reset = 00h]

Return to the Summary Table.

Figure 8-9. GPIO_DATA_INPUT Register

7	6	5	4	3	2	1	0
GPIO7_DAT_IN	GPIO6_DAT_IN	GPIO5_DAT_IN	GPIO4_DAT_IN	GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	GPIO0_DAT_IN
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-12. GPIO_DATA_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO7_DAT_IN	R	0b	GPIO7 data Read back value of GPIO7 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO7_CFG[1:0] = 00b). 0b = Low 1b = High
6	GPIO6_DAT_IN	R	0b	GPIO6 data Read back value of GPIO6 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO6_CFG[1:0] = 00b). 0b = Low 1b = High
5	GPIO5_DAT_IN	R	0b	GPIO5 data Read back value of GPIO5 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO5_CFG[1:0] = 00b). 0b = Low 1b = High
4	GPIO4_DAT_IN	R	0b	GPIO4 data Read back value of GPIO4 when configured as digital input, digital output, or static $\overline{\text{FAULT}}$ output. Bit reads 0b when the GPIO function is disabled (GPIO4_CFG[1:0] = 00b) or when GPIO4 is configured as $\overline{\text{FAULT}}$ output with heart beat function (GPIO4_CFG[1:0] = 10b or 11b, GPIO4_SRC = 1b, FAULT_PIN_BEHAVIOR = 1b). 0b = Low 1b = High
3	GPIO3_DAT_IN	R	0b	GPIO3 data Read back value of GPIO3 when configured as digital input, digital output, or ALERT output. Bit reads 0b when the GPIO function is disabled (GPIO3_CFG[1:0] = 00b). 0b = Low 1b = High
2	GPIO2_DAT_IN	R	0b	GPIO2 data Read back value of GPIO2 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO2_CFG[1:0] = 00b). 0b = Low 1b = High
1	GPIO1_DAT_IN	R	0b	GPIO1 data Read back value of GPIO1 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO1_CFG[1:0] = 00b). 0b = Low 1b = High
0	GPIO0_DAT_IN	R	0b	GPIO0 data Read back value of GPIO0 when configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO0_CFG[1:0] = 00b). 0b = Low 1b = High

8.1.10 SEQ_STATUS Register (Address = 09h) [Reset = 07h]

Return to the Summary Table.

Figure 8-10. SEQ_STATUS Register

7	6	5	4	3	2	1	0
SEQ_ACTIVE	SEQ_COUNT[3:0]				RESERVED		
R-0b	R-0000b				R-111b		

Table 8-13. SEQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SEQ_ACTIVE	R	0b	Sequencer active flag Indicates if conversions are currently ongoing or if conversions stopped and the device is in idle, standby or power-down mode. 0b = Sequencer not active; no conversions ongoing 1b = Sequencer active; conversions ongoing
6:3	SEQ_COUNT[3:0]	R	0000b	Sequence counter When SEQ_MODE[1:0] = 11b, the sequence counter indicates which sequence run the latest conversion result belongs to, which is currently available for readout. The sequence counter increments with the completion of the first conversion of a new sequence run. At the completion of the first conversion of the first sequence run, the counter reads 0h. At the completion of the first conversion of the second sequence run, the counter reads 1h. After reaching a counter value of Fh, the counter rolls over to 0h with the completion of the first conversion of the next sequence run. The counter resets to 0h at the completion of the first conversion after setting the START bit to 1b or at the rising edge of the START pin. When writing to the SEQUENCER_CFG register, in power-down mode, or after a device reset, the counter resets to 0h immediately. At the same time the sequence step indicator (STEP_INDICATOR[4:0]) resets to 00h, the conversion counter (CONV_COUNT[3:0]) resets to Fh, and the conversion data clears. The sequence counter always reads 0h when SEQ_MODE[1:0] = 00b, 01b, or 10b.
2:0	RESERVED	R	111b	Reserved Always reads 111b.

8.1.11 CONVERSION_CTRL Register (Address = 0Bh) [Reset = 00h]

Return to the Summary Table.

Figure 8-11. CONVERSION_CTRL Register

7	6	5	4	3	2	1	0
START	STEP_INIT[4:0]					RESERVED	STOP
R/W-0b	R/W-00000b					R-0b	R/W-0b

Table 8-14. CONVERSION_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	START	R/W	0b	Start or re-start ADC conversions Write 1b to start or re-start conversions using the step configuration page indicated in the STEP_INIT[4:0] bit field. The SEQ_MODE[1:0] bits determine the conversion and sequencer behavior. Writing 1b to both the START and STOP bits has no effect. The START bit is self-clearing and always reads 0b. 0b = No operation 1b = Start or restart conversions
6:2	STEP_INIT[4:0]	R/W	00000b	Initial execution step selector Determines the sequence step configuration the sequencer selects for the first conversion when setting the START bit to 1b, or when taking the START pin high. If STEP_INIT[4:0] is set to a value between 18h and 1Fh, no conversion or sequence is started. The STEP_INIT[4:0] bit field also determines the step configuration page that is used whenever the device is in idle or standby mode, regardless if the respective step page is enabled or not (STEP_x_EN bit setting is ignored). That means, when coming out of power-down mode, or when conversions stop, the device transitions to the step page configuration determined by the STEP_INIT[4:0] bit field. If STEP_INIT[4:0] is set to a value between 18h and 1Fh in standby or idle mode, then the configuration of step 23 takes effect.
1	RESERVED	R	0b	Reserved Always reads 0b.
0	STOP	R/W	0b	Stop ADC conversions Write 1b to stop conversions. The STOP_BEHAVIOR[1:0] bits determine the stopping behavior. Writing 1b to both the START and STOP bits has no effect. The STOP bit clears to 0b after conversions stopped or when the START bit is set before the ongoing conversions stopped. 0b = No operation 1b = Stop conversions

8.1.12 RESET Register (Address = 0Ch) [Reset = 00h]

Return to the Summary Table.

Figure 8-12. RESET Register

7	6	5	4	3	2	1	0
RESET_CODE[7:0]							
R/W-00000000b							

Table 8-15. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESET_CODE[7:0]	R/W	00000000b	Device reset register Write 01011010b to reset the ADC. These bits always read 00000000b.

8.1.13 ADC_CFG Register (Address = 10h) [Reset = 00h]

Return to the Summary Table.

Figure 8-13. ADC_CFG Register

7	6	5	4	3	2	1	0
RESERVED	REF_VAL	CLK_SEL	GC_EN	SPEED_MODE[1:0]		STBY_MODE	PWDN
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b

Table 8-16. ADC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved Always reads 0b.
6	REF_VAL	R/W	0b	Internal reference voltage value selection Selects the voltage of the internal reference. The internal voltage reference is always enabled. 0b = 1.25V 1b = 2.5V
5	CLK_SEL	R/W	0b	Clock selection Selects the clock source for the device. 0b = Internal oscillator 1b = External clock provided at the CLK pin
4	GC_EN	R/W	0b	Global-chop mode enable Enables global-chop mode. When enabled, the device automatically swaps the analog inputs and takes the average of two consecutive conversions to cancel the internal offset voltage. 0b = Disabled 1b = Enabled
3:2	SPEED_MODE[1:0]	R/W	00b	Speed mode selection Selects the speed mode for the device. 00b = Speed mode 0 (f_{MOD} = 32kHz) 01b = Speed mode 1 (f_{MOD} = 256kHz) 10b = Speed mode 2 (f_{MOD} = 512kHz) 11b = Speed mode 3 (f_{MOD} = 1024kHz)
1	STBY_MODE	R/W	0b	Standby mode selection This bit enables the auto engagement of the low-power standby mode after conversions are stopped. 0b = Idle mode; device remains fully powered when conversions stop. 1b = Standby mode; device transitions to a low-power standby mode when conversions stop. Standby mode is exited when conversions restart.
0	PWDN	R/W	0b	Power-down mode selection Powers down all circuitry except for circuitry necessary to retain the user register settings. SPI communication is still possible. In power-down mode, the step indicator (STEP_INDICATOR[4:0]) resets to 00h, the conversion counter (CONV_COUNT[3:0]) resets to Fh, the sequence counter (SEQ_COUNT[3:0]) resets to 0h, the conversion data clears, and the START bit and START pin are ignored. Setting the PWDN bit to 1b powers the device down immediately; any ongoing conversions are aborted. Any analog inputs configured as GPIO digital outputs transition into a Hi-Z state in power-down mode. To maintain a certain logic level during power-down, consider external pullup or pulldown resistors on the respective GPIO pins. 0b = Active mode 1b = Power-down mode

8.1.14 DIGITAL_CFG Register (Address = 11h) [Reset = 00h]

Return to the Summary Table.

Figure 8-14. DIGITAL_CFG Register

7	6	5	4	3	2	1	0
SPARE[4:0]					STATUS_EN	SDO_MODE	CONT_READ_EN
R/W-00000b					R/W-0b	R/W-0b	R/W-0b

Table 8-17. DIGITAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	SPARE[4:0]	R/W	00000b	Spare register bits Provided as R/W bits as a means to check the register map CRC. Bit settings have no effect.
2	STATUS_EN	R/W	0b	STATUS header output enable Enables the STATUS header (STATUS_MSB + STATUS_LSB registers) transmission on SDO as the first two bytes of every SPI frame. 0b = Disabled 1b = Enabled
1	SDO_MODE	R/W	0b	SDO/$\overline{\text{DRDY}}$ mode selection Selects the mode of the SDO/$\overline{\text{DRDY}}$ pin to either data-output function only, or to dual-mode function of data output and data ready. Use the data-output only mode when operating the device in a daisy chain. 0b = Data-output only mode 1b = Dual mode: data output and data ready
0	CONT_READ_EN	R/W	0b	Continuous-read mode enable Enables continuous-read mode to allow reading multiple consecutive registers within a single SPI frame in 4-wire SPI mode. Disable continuous-read mode when operating the device in a daisy chain or in 3-wire SPI mode. 0b = Disabled 1b = Enabled

8.1.15 VBIAS Register (Address = 12h) [Reset = 00h]

Return to the Summary Table.

Figure 8-15. VBIAS Register

7	6	5	4	3	2	1	0
VBIAS_AIN7	VBIAS_AIN6	VBIAS_AIN5	VBIAS_AIN4	VBIAS_AIN3	VBIAS_AIN2	VBIAS_AIN1	VBIAS_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-18. VBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBIAS_AIN7	R/W	0b	AIN7 VBIAS selection Enables VBIAS on the AIN7 pin. 0b = Disabled 1b = Enabled
6	VBIAS_AIN6	R/W	0b	AIN6 VBIAS selection Enables VBIAS on the AIN6 pin. 0b = Disabled 1b = Enabled
5	VBIAS_AIN5	R/W	0b	AIN5 VBIAS selection Enables VBIAS on the AIN5 pin. 0b = Disabled 1b = Enabled
4	VBIAS_AIN4	R/W	0b	AIN4 VBIAS selection Enables VBIAS on the AIN4 pin. 0b = Disabled 1b = Enabled
3	VBIAS_AIN3	R/W	0b	AIN3 VBIAS selection Enables VBIAS on the AIN3 pin. 0b = Disabled 1b = Enabled
2	VBIAS_AIN2	R/W	0b	AIN2 VBIAS selection Enables VBIAS on the AIN2 pin. 0b = Disabled 1b = Enabled
1	VBIAS_AIN1	R/W	0b	AIN1 VBIAS selection Enables VBIAS on the AIN1 pin. 0b = Disabled 1b = Enabled
0	VBIAS_AIN0	R/W	0b	AIN0 VBIAS selection Enables VBIAS on the AIN0 pin. 0b = Disabled 1b = Enabled

8.1.16 GPIO_CFG0 Register (Address = 13h) [Reset = 00h]

Return to the Summary Table.

Figure 8-16. GPIO_CFG0 Register

7	6	5	4	3	2	1	0
GPIO3_CFG[1:0]		GPIO2_CFG[1:0]		GPIO1_CFG[1:0]		GPIO0_CFG[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-19. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	GPIO3_CFG[1:0]	R/W	00b	GPIO3 configuration Configures the GPIO3 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
5:4	GPIO2_CFG[1:0]	R/W	00b	GPIO2 configuration Configures the GPIO2 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
3:2	GPIO1_CFG[1:0]	R/W	00b	GPIO1 configuration Configures the GPIO1 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
1:0	GPIO0_CFG[1:0]	R/W	00b	GPIO0 configuration Configures the GPIO0 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)

8.1.17 GPIO_CFG1 Register (Address = 14h) [Reset = 00h]

Return to the Summary Table.

Figure 8-17. GPIO_CFG1 Register

7	6	5	4	3	2	1	0
GPIO7_CFG[1:0]		GPIO6_CFG[1:0]		GPIO5_CFG[1:0]		GPIO4_CFG[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-20. GPIO_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	GPIO7_CFG[1:0]	R/W	00b	GPIO7 configuration Configures the GPIO7 pin behavior. 00b = ADS1x4S18: Pin operates as analog or REFN1 input. ADS1x4S14: Pin operates as REFN1 input. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
5:4	GPIO6_CFG[1:0]	R/W	00b	GPIO6 configuration Configures the GPIO6 pin behavior. 00b = ADS1x4S18: Pin operates as analog or REFP1 input. ADS1x4S14: Pin operates as REFP1 input. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
3:2	GPIO5_CFG[1:0]	R/W	00b	GPIO5 configuration Configures the GPIO5 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
1:0	GPIO4_CFG[1:0]	R/W	00b	GPIO4 configuration Configures the GPIO4 pin behavior. 00b = ADS1x4S18: Pin operates as analog input. ADS1x4S14: Pin is High-Z. 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)

8.1.18 GPIO_CFG2 Register (Address = 15h) [Reset = 08h]

Return to the Summary Table.

Figure 8-18. GPIO_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED			COMP_ALERTn_MASK	FAULT_PIN_BEHAVIOR	ALERT_PIN_POL	GPIO4_SRC	GPIO3_SRC
R-000b			R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 8-21. GPIO_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000b	Reserved Always reads 0000b.
4	COMP_ALERTn_MASK	R/W	0b	Comparator alert mask Determines whether the COMP_ALERTn contributes to the SAD_FAULTn or not. When GPIO3 is configured as ALERT output, COMP_ALERTn triggers the ALERT pin regardless of the status of this mask bit. 0b = Mask disabled. COMP_ALERTn triggers SAD_FAULTn. 1b = Mask enabled. COMP_ALERTn does not trigger SAD_FAULTn, but still triggers ALERT pin.
3	FAULT_PIN_BEHAVIOR	R/W	1b	$\overline{\text{FAULT}}$ pin behavior selection Selects the behavior of the $\overline{\text{FAULT}}$ pin, when GPIO4 is configured as $\overline{\text{FAULT}}$ output (GPIO4_CFG[1:0] = 10b or 11b, GPIO4_SRC = 1b). 0b = Static. Output is low when a fault occurred, otherwise output is high. 1b = Heart beat. Output is low when a fault occurred, otherwise output is a 50% duty-cycle signal with a frequency of $f_{MOD}/256$.
2	ALERT_PIN_POL	R/W	0b	ALERT pin polarity selection Selects the polarity of the ALERT output pin, when GPIO3 is configured as ALERT output (GPIO3_CFG[1:0] = 10b or 11b, GPIO3_SRC = 1b). 0b = Active low 1b = Active high
1	GPIO4_SRC	R/W	0b	GPIO4 data source selection Selects the data source of the GPIO4 pin when GPIO4 is configured as digital output. The $\overline{\text{FAULT}}$ pin is low when the SAD_FAULTn flag is 0b. 0b = GPIO4_DAT_OUT bit 1b = SAD_FAULTn flag. Pin acts as $\overline{\text{FAULT}}$ output.
0	GPIO3_SRC	R/W	0b	GPIO3 data source selection Selects the data source of the GPIO3 pin when GPIO3 is configured as digital output. 0b = GPIO3_DAT_OUT bit 1b = COMP_ALERTn flag. Pin acts as digital comparator ALERT output.

8.1.19 MONITOR_CFG Register (Address = 16h) [Reset = 04h]

Return to the Summary Table.

Figure 8-19. MONITOR_CFG Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED	REF_UV_EN	REF_UV_SEL	REG_MAP_CRC_EN	SPI_CRC_EN
R-000b			R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b

Table 8-22. MONITOR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000b	Reserved Always reads 000b.
4	RESERVED	R/W	0b	Reserved Always write 0b.
3	REF_UV_EN	R/W	0b	Reference undervoltage monitor enable Enables the voltage reference monitor to detect when the selected voltage reference using the STEPx_REF_SEL[1:0] bits on a certain sequence step drops below the undervoltage monitor threshold. 0b = Disabled 1b = Enabled
2	REF_UV_SEL	R/W	1b	Voltage reference undervoltage monitor threshold selection Selects the voltage reference undervoltage monitor threshold. 0b = 550 mV 1b = 1 V
1	REG_MAP_CRC_EN	R/W	0b	Register map CRC enable Enables the register map CRC for the Status and General Configuration page (register addresses 10h to 1Fh) and the Step Configuration pages (register addresses 00h to 14h). 0b = Disabled 1b = Enabled
0	SPI_CRC_EN	R/W	0b	SPI CRC enable Enables the SPI CRC on SDI and SDO. 0b = Disabled 1b = Enabled

8.1.20 SPARE Register (Address = 18h) [Reset = 00h]

Return to the Summary Table.

Figure 8-20. SPARE Register

7	6	5	4	3	2	1	0
SPARE[7:0]							
R/W-00000000b							

Table 8-23. SPARE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPARE[7:0]	R/W	00000000b	Spare register bits Provided as R/W bits as a means to check the register map CRC. Bit settings have no effect.

8.1.21 SEQUENCER_CFG Register (Address = 19h) [Reset = 50h]

Return to the Summary Table.

Figure 8-21. SEQUENCER_CFG Register

7	6	5	4	3	2	1	0
SEQ_MODE[1:0]		STOP_BEHAVIOR[1:0]		RESERVED		RESERVED	
R/W-01b		R/W-01b		R-00b		R/W-00b	

Table 8-24. SEQUENCER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SEQ_MODE[1:0]	R/W	01b	Sequencer mode selection Selects the operating mode of the sequencer. When STEP_INIT[4:0] is set to a value between 18h and 1Fh no conversion or sequence is started in any of the sequencer modes. 00b = Execute the sequence step defined by the STEP_INIT[4:0] pointer one time. Step enable bits (STEP_x_EN) are ignored in this sequencer mode. The STEPx_NUM_CONV[4:0] bits determine the number of consecutive conversions for this sequence step. 01b = Continuously convert the sequence step defined by the STEP_INIT[4:0] pointer. Step enable bits (STEP_x_EN) and STEPx_NUM_CONV[4:0] bits are ignored in this sequencer mode. 10b = Execute a sequence of all enabled steps between the step defined by the STEP_INIT[4:0] pointer and step 23 one time. Use the STEP_x_EN bits to include a step in the sequence. The sequence does not execute if the step defined by the STEP_INIT[4:0] pointer is disabled. 11b = Execute the sequence of all enabled steps and repeat the sequence continuously, starting with the step defined by the STEP_INIT[4:0] pointer. Use the STEP_x_EN bits to include a step in the sequence. The sequence does not execute if the step defined by the STEP_INIT[4:0] pointer is disabled.
5:4	STOP_BEHAVIOR[1:0]	R/W	01b	Sequence stop behavior selection Selects the device behavior when setting the STOP bit to 1b or when a falling edge on the START pin occurs. 00b = Stop immediately. Any ongoing conversion is aborted. 01b = Stop after current conversion completes. 10b = Stop after current sequence step completes. If SEQ_MODE[1:0] = 01b when using this mode, then stop after current conversion completes. 11b = Stop after full sequence completes. If SEQ_MODE[1:0] = 00b when using this mode, then stop after current sequence step completes. If SEQ_MODE[1:0] = 01b when using this mode, then stop after current conversion completes.
3:2	RESERVED	R	00b	Reserved Always reads 00b.
1:0	RESERVED	R/W	00b	Reserved Always write 00b.

8.1.22 SEQUENCE_STEP_EN_0 Register (Address = 1Ah) [Reset = 01h]

Return to the Summary Table.

Figure 8-22. SEQUENCE_STEP_EN_0 Register

7	6	5	4	3	2	1	0
STEP_7_EN	STEP_6_EN	STEP_5_EN	STEP_4_EN	STEP_3_EN	STEP_2_EN	STEP_1_EN	STEP_0_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 8-25. SEQUENCE_STEP_EN_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEP_7_EN	R/W	0b	Sequencer step 7 enable 0b = Step disabled 1b = Step enabled
6	STEP_6_EN	R/W	0b	Sequencer step 6 enable 0b = Step disabled 1b = Step enabled
5	STEP_5_EN	R/W	0b	Sequencer step 5 enable 0b = Step disabled 1b = Step enabled
4	STEP_4_EN	R/W	0b	Sequencer step 4 enable 0b = Step disabled 1b = Step enabled
3	STEP_3_EN	R/W	0b	Sequencer step 3 enable 0b = Step disabled 1b = Step enabled
2	STEP_2_EN	R/W	0b	Sequencer step 2 enable 0b = Step disabled 1b = Step enabled
1	STEP_1_EN	R/W	0b	Sequencer step 1 enable 0b = Step disabled 1b = Step enabled
0	STEP_0_EN	R/W	1b	Sequencer step 0 enable 0b = Step disabled 1b = Step enabled

8.1.23 SEQUENCE_STEP_EN_1 Register (Address = 1Bh) [Reset = 00h]

Return to the Summary Table.

Figure 8-23. SEQUENCE_STEP_EN_1 Register

7	6	5	4	3	2	1	0
STEP_15_EN	STEP_14_EN	STEP_13_EN	STEP_12_EN	STEP_11_EN	STEP_10_EN	STEP_9_EN	STEP_8_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-26. SEQUENCE_STEP_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEP_15_EN	R/W	0b	Sequencer step 15 enable 0b = Step disabled 1b = Step enabled
6	STEP_14_EN	R/W	0b	Sequencer step 14 enable 0b = Step disabled 1b = Step enabled
5	STEP_13_EN	R/W	0b	Sequencer step 13 enable 0b = Step disabled 1b = Step enabled
4	STEP_12_EN	R/W	0b	Sequencer step 12 enable 0b = Step disabled 1b = Step enabled
3	STEP_11_EN	R/W	0b	Sequencer step 11 enable 0b = Step disabled 1b = Step enabled
2	STEP_10_EN	R/W	0b	Sequencer step 10 enable 0b = Step disabled 1b = Step enabled
1	STEP_9_EN	R/W	0b	Sequencer step 9 enable 0b = Step disabled 1b = Step enabled
0	STEP_8_EN	R/W	0b	Sequencer step 8 enable 0b = Step disabled 1b = Step enabled

8.1.24 SEQUENCE_STEP_EN_2 Register (Address = 1Ch) [Reset = 00h]

Return to the Summary Table.

Figure 8-24. SEQUENCE_STEP_EN_2 Register

7	6	5	4	3	2	1	0
STEP_23_EN	STEP_22_EN	STEP_21_EN	STEP_20_EN	STEP_19_EN	STEP_18_EN	STEP_17_EN	STEP_16_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-27. SEQUENCE_STEP_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEP_23_EN	R/W	0b	Sequencer step 23 enable 0b = Step disabled 1b = Step enabled
6	STEP_22_EN	R/W	0b	Sequencer step 22 enable 0b = Step disabled 1b = Step enabled
5	STEP_21_EN	R/W	0b	Sequencer step 21 enable 0b = Step disabled 1b = Step enabled
4	STEP_20_EN	R/W	0b	Sequencer step 20 enable 0b = Step disabled 1b = Step enabled
3	STEP_19_EN	R/W	0b	Sequencer step 19 enable 0b = Step disabled 1b = Step enabled
2	STEP_18_EN	R/W	0b	Sequencer step 18 enable 0b = Step disabled 1b = Step enabled
1	STEP_17_EN	R/W	0b	Sequencer step 17 enable 0b = Step disabled 1b = Step enabled
0	STEP_16_EN	R/W	0b	Sequencer step 16 enable 0b = Step disabled 1b = Step enabled

8.1.25 REG_MAP_CRC Register (Address = 3Dh) [Reset = 00h]

Return to the Summary Table.

Figure 8-25. REG_MAP_CRC Register

7	6	5	4	3	2	1	0
GENERAL_CFG_REG_MAP_CRC_VALUE[7:0]							
R/W-00000000b							

Table 8-28. REG_MAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GENERAL_CFG_REG_MAP_CRC_VALUE[7:0]	R/W	00000000b	Register map CRC value for the Status and General Configuration page This value is the user-calculated CRC value of registers 10h to 1Fh.

8.1.26 PAGE_INDICATOR Register (Address = 3Eh) [Reset = 00h]

Return to the Summary Table.

Figure 8-26. PAGE_INDICATOR Register

7	6	5	4	3	2	1	0
PAGE_INDICATOR[7:0]							
R-00000000b							

Table 8-29. PAGE_INDICATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE_INDICATOR[7:0]	R	00000000b	Register page indicator Read the register page indicator to verify the register page which is currently selected for reading and writing registers.

8.1.27 PAGE_POINTER Register (Address = 3Fh) [Reset = 00h]

Return to the Summary Table.

Figure 8-27. PAGE_POINTER Register

7	6	5	4	3	2	1	0
PAGE_POINTER[7:0]							
R/W-00000000b							

Table 8-30. PAGE_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE_POINTER[7:0]	R/W	00000000b	Register page pointer Write the register page pointer to select the desired register page for reading and writing registers.

8.2 Step Configuration Page Registers

Table 8-31 lists the memory-mapped registers for the Step Configuration Page Registers registers. All register offset addresses not listed in Table 8-31 should be considered as reserved locations and the register contents should not be modified.

Table 8-31. Register Map

Address	Acronym	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Multiplexer Configuration Registers										
00h	STEPx_AINP_CFG	12h	RESERVED			STEPx_AINP[4:0]				
01h	STEPx_AINN_CFG	12h	RESERVED			STEPx_AINN[4:0]				
ADC Configuration Registers										
02h	STEPx_GAIN_REF_CFG	01h	STEPx_REFP_BUF_EN	STEPx_REFN_BUF_EN	STEPx_REF_SEL[1:0]		STEPx_GAIN[3:0]			
03h	STEPx_DIGITAL_CFG	00h	SPARE[1:0]		STEPx_CODING	STEPx_NUM_CONV[4:0]				
Digital Filter Configuration Registers										
04h	STEPx_FLTR_CFG	01h	SPARE[1:0]		STEPx_FLTR_MODE	STEPx_FLTR_OSR[4:0]				
05h	STEPx_DELAY_CFG	00h	RESERVED	STEPx_DELAY[6:0]						
Offset and Gain Calibration Coefficient Registers										
06h	STEPx_OFFSET_CAL_MSB	00h	STEPx_OFFSET_CAL[23:16]							
07h	STEPx_OFFSET_CAL_ISB	00h	STEPx_OFFSET_CAL[15:8]							
08h	STEPx_OFFSET_CAL_LSB	00h	STEPx_OFFSET_CAL[7:0]							
09h	STEPx_GAIN_CAL_MSB	40h	STEPx_GAIN_CAL[15:8]							
0Ah	STEPx_GAIN_CAL_LSB	00h	STEPx_GAIN_CAL[7:0]							
System Monitor Register										
0Bh	STEPx_SYSMON_CFG	00h	RESERVED		STEPx_BOCS[1:0]		RESERVED	STEPx_SYS_MON[2:0]		
Excitation Current Sources Configuration Registers										
0Ch	STEPx_IDAC_MAG_CFG	00h	STEPx_I2MAG[3:0]				STEPx_I1MAG[3:0]			
0Dh	STEPx_IDAC1_MUX_CFG	1Fh	STEPx_IUNIT	RESERVED		STEPx_I1MUX[4:0]				
0Eh	STEPx_IDAC2_MUX_CFG	1Fh	RESERVED			STEPx_I2MUX[4:0]				
GPIO Output Data Register										
0Fh	STEPx_GPIO_DATA_OUT	00h	STEPx_GPIO7_DAT_OUT	STEPx_GPIO6_DAT_OUT	STEPx_GPIO5_DAT_OUT	STEPx_GPIO4_DAT_OUT	STEPx_GPIO3_DAT_OUT	STEPx_GPIO2_DAT_OUT	STEPx_GPIO1_DAT_OUT	STEPx_GPIO0_DAT_OUT
Digital Comparator Configuration Registers										
10h	STEPx_COMPARATOR_HIGH_THRESHOLD_MSB	00h	STEPx_COMP_HIGH_TH[15:8]							
11h	STEPx_COMPARATOR_HIGH_THRESHOLD_LSB	00h	STEPx_COMP_HIGH_TH[7:0]							
12h	STEPx_COMPARATOR_LOW_THRESHOLD_MSB	00h	STEPx_COMP_LOW_TH[15:8]							
13h	STEPx_COMPARATOR_LOW_THRESHOLD_LSB	00h	STEPx_COMP_LOW_TH[7:0]							
14h	STEPx_COMPARATOR_CFG	00h	RESERVED				STEPx_COMP_NUM[1:0]		STEPx_COMP_HIGH_TH_EN	STEPx_COMP_LOW_TH_EN
Register Map CRC Value Register										
3Dh	STEPx_REG_MAP_CRC	0Eh	STEPx_REG_MAP_CRC_VALUE[7:0]							
Page Indicator and Pointer Registers										
3Eh	STEPx_PAGE_INDICATOR	00h	STEPx_PAGE_INDICATOR[7:0]							

Table 8-31. Register Map (continued)

Address	Acronym	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Fh	STEPx_PAGE_POINTER	00h	STEPx_PAGE_POINTER[7:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-32 shows the codes that are used for access types in this section.

Table 8-32. Step Configuration Page Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 STEPx_AINP_CFG Register (Address = 00h) [Reset = 12h]

Return to the Summary Table.

Figure 8-28. STEPx_AINP_CFG Register

7	6	5	4	3	2	1	0
RESERVED			STEPx_AINP[4:0]				
R-000b			R/W-10010b				

Table 8-33. STEPx_AINP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000b	Reserved Always reads 000b.
4:0	STEPx_AINP[4:0]	R/W	10010b	Positive multiplexer input selection Selects the positive analog input for the ADC. Analog inputs AIN13, AIN14, AIN16, and AIN17 on ADS1x4S18 can still be used as analog inputs, even when the inputs are configured as REFPx and REFNx inputs. When an analog input is configured as GPIO, the analog input can still be selected by the multiplexer and used to measure back the voltage on the GPIO pin. The STEPx_AINP bit settings are ignored if any of the system monitors are enabled. That is, when STEPx_SYS_MON[3:0] is set to anything other than 0000b. 00000b = AIN0 00001b = AIN1 00010b = AIN2 00011b = AIN3 00100b = AIN4 00101b = AIN5 00110b = AIN6 00111b = AIN7 01000b = AIN8 (ADS1x4S18), AVSS (ADS1x4S14) 01001b = AIN9 (ADS1x4S18), AVSS (ADS1x4S14) 01010b = AIN10 (ADS1x4S18), AVSS (ADS1x4S14) 01011b = AIN11 (ADS1x4S18), AVSS (ADS1x4S14) 01100b = AIN12 (ADS1x4S18), AVSS (ADS1x4S14) 01101b = AIN13 (ADS1x4S18), AVSS (ADS1x4S14) 01110b = AIN14 (ADS1x4S18), AVSS (ADS1x4S14) 01111b = AIN15 (ADS1x4S18), AVSS (ADS1x4S14) 10000b = AIN16 (ADS1x4S18), AVSS (ADS1x4S14) 10001b = AIN17 (ADS1x4S18), AVSS (ADS1x4S14) 10010b = AVSS 10011b = AVSS 10100b = AVSS 10101b = AVSS 10110b = AVSS 10111b = AVSS 11000b = AVSS 11001b = AVSS 11010b = AVSS 11011b = AVSS 11100b = AVSS 11101b = AVSS 11110b = AVSS 11111b = Open

8.2.2 STEPx_AINN_CFG Register (Address = 01h) [Reset = 12h]

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Figure 8-29. STEPx_AINN_CFG Register

7	6	5	4	3	2	1	0
RESERVED			STEPx_AINN[4:0]				
R-000b			R/W-10010b				

Table 8-34. STEPx_AINN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000b	Reserved Always reads 000b.
4:0	STEPx_AINN[4:0]	R/W	10010b	Negative multiplexer input selection Selects the negative analog input for the ADC. Analog inputs AIN13, AIN14, AIN16, and AIN17 on ADS1x4S18 can still be used as analog inputs, even when the inputs are configured as REFPx and REFNx inputs. When an analog input is configured as GPIO, the analog input can still be selected by the multiplexer and used to measure back the voltage on the GPIO pin. The STEPx_AINN bit settings are ignored if any of the system monitors are enabled. That is, when STEPx_SYS_MON[3:0] is set to anything other than 0000b. 00000b = AIN0 00001b = AIN1 00010b = AIN2 00011b = AIN3 00100b = AIN4 00101b = AIN5 00110b = AIN6 00111b = AIN7 01000b = AIN8 (ADS1x4S18), AVSS (ADS1x4S14) 01001b = AIN9 (ADS1x4S18), AVSS (ADS1x4S14) 01010b = AIN10 (ADS1x4S18), AVSS (ADS1x4S14) 01011b = AIN11 (ADS1x4S18), AVSS (ADS1x4S14) 01100b = AIN12 (ADS1x4S18), AVSS (ADS1x4S14) 01101b = AIN13 (ADS1x4S18), AVSS (ADS1x4S14) 01110b = AIN14 (ADS1x4S18), AVSS (ADS1x4S14) 01111b = AIN15 (ADS1x4S18), AVSS (ADS1x4S14) 10000b = AIN16 (ADS1x4S18), AVSS (ADS1x4S14) 10001b = AIN17 (ADS1x4S18), AVSS (ADS1x4S14) 10010b = AVSS 10011b = AVSS 10100b = AVSS 10101b = AVSS 10110b = AVSS 10111b = AVSS 11000b = AVSS 11001b = AVSS 11010b = AVSS 11011b = AVSS 11100b = AVSS 11101b = AVSS 11110b = AVSS 11111b = Open

8.2.3 STEPx_GAIN_REF_CFG Register (Address = 02h) [Reset = 01h]

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Figure 8-30. STEPx_GAIN_REF_CFG Register

7	6	5	4	3	2	1	0
STEPx_REFP_BUF_EN	STEPx_REFN_BUF_EN	STEPx_REF_SEL[1:0]		STEPx_GAIN[3:0]			
R/W-0b	R/W-0b	R/W-00b		R/W-0001b			

Table 8-35. STEPx_GAIN_REF_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEPx_REFP_BUF_EN	R/W	0b	Positive reference buffer enable Enables the positive reference buffer. Disable the positive reference buffer when the internal reference or the analog supply is selected as the reference source. 0b = Disabled 1b = Enabled
6	STEPx_REFN_BUF_EN	R/W	0b	Negative reference buffer enable Enables the negative reference buffer. Disable the negative reference buffer when the internal reference or the analog supply is selected as the reference source. 0b = Disabled 1b = Enabled
5:4	STEPx_REF_SEL[1:0]	R/W	00b	Reference voltage selection Selects the reference voltage for the ADC. Set GPIO6_CFG[1:0] = 00b and GPIO7_CFG[1:0] = 00b when the external voltage reference input pair, REFP1 and REFN1, is selected. 00b = Internal voltage reference 01b = External voltage reference (REFP0, REFN0) 10b = External voltage reference (REFP1, REFN1) 11b = AVDD – AVSS
3:0	STEPx_GAIN[3:0]	R/W	0001b	PGA gain selection Selects the gain of the PGA. 0000b = 0.5 0001b = 1 0010b = 2 0011b = 4 0100b = 5 0101b = 8 0110b = 10 0111b = 16 1000b = 20 1001b = 32 1010b = 50 1011b = 64 1100b = 100 1101b = 128 1110b = 200 1111b = 256

8.2.4 STEPx_DIGITAL_CFG Register (Address = 03h) [Reset = 00h]

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Figure 8-31. STEPx_DIGITAL_CFG Register

7	6	5	4	3	2	1	0
SPARE[1:0]		STEPx_CODING	STEPx_NUM_CONV[4:0]				
R/W-00b		R/W-0b	R/W-00000b				

Table 8-36. STEPx_DIGITAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SPARE[1:0]	R/W	00b	Spare register bits Provided as R/W bits as a means to check the register map CRC. Bit settings have no effect.
5	STEPx_CODING	R/W	0b	Conversion data coding selection Selects the coding of the conversion data. 0b = Binary two's complement 1b = Unipolar straight binary
4:0	STEPx_NUM_CONV[4:0]	R/W	00000b	Conversion number selection Determines the number of consecutive conversion to perform for this sequence step. The device can take between one (00000b) and 32 (11111b) conversions per step. Bit field has no effect when SEQ_MODE[1:0] = 01b.

8.2.5 STEPx_FLTR_CFG Register (Address = 04h) [Reset = 01h]

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Figure 8-32. STEPx_FLTR_CFG Register

7	6	5	4	3	2	1	0
SPARE[1:0]		STEPx_FLTR_MODE	STEPx_FLTR_OSR[4:0]				
R/W-00b		R/W-0b	R/W-00001b				

Table 8-37. STEPx_FLTR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SPARE[1:0]	R/W	00b	Spare register bits Provided as R/W bits as a means to check the register map CRC. Bit settings have no effect.
5	STEPx_FLTR_MODE	R/W	0b	Digital filter mode selection Selects the first stage digital filter type. 0b = Sinc4 1b = Sinc3
4:0	STEPx_FLTR_OSR[4:0]	R/W	00001b	Digital filter OSR or data rate selection Selects the OSR of the digital filter or the output data rate. For settings where an OSR is stated, the output data rate calculates to $f_{DATA} = f_{MOD}$ / OSR. The used sinc filter type is specified in parenthesis. Sincx is either the sinc3 or sinc4 filter based on the STEPx_FLTR_MODE setting. For settings where an output data rate (f_{DATA}) is specified, the digital filter adjusts the OSR automatically based on the selected speed mode. The stated output data rates are valid for a nominal clock frequency of f_{CLK} = 4.096MHz. The data rates scale proportional with the clock frequency. At output data rates of 20SPS and 25SPS the digital filter provides 50Hz and 60Hz line-cycle rejection with single-cycle settling. 00000b = OSR = 8 (Sincx) 00001b = OSR = 16 (Sincx) 00010b = OSR = 24 (Sincx) 00011b = OSR = 32 (Sincx) 00100b = OSR = 64 (Sincx) 00101b = OSR = 128 (Sincx) 00110b = OSR = 256 (Sincx) 00111b = OSR = 512 (Sincx) 01000b = OSR = 640 (Sincx) 01001b = OSR = 1024 (Sincx) 01010b = OSR = 2048 (Sincx) 01011b = OSR = 4096 (Sincx) 01100b = OSR = 8192 (Sincx) 01101b = f_{DATA} = 60SPS (Sincx) 01110b = f_{DATA} = 50SPS (Sincx) 01111b = f_{DATA} = 16.7SPS (Sincx) 10000b = f_{DATA} = 10SPS (Sincx) 10001b = OSR = 64 (Sinc4 OSR = 32 + Sinc1 OSR = 2) 10010b = OSR = 128 (Sinc4 OSR = 32 + Sinc1 OSR = 4) 10011b = OSR = 256 (Sinc4 OSR = 32 + Sinc1 OSR = 8) 10100b = OSR = 512 (Sinc4 OSR = 32 + Sinc1 OSR = 16) 10101b = OSR = 640 (Sinc4 OSR = 32 + Sinc1 OSR = 20) 10110b = OSR = 1024 (Sinc4 OSR = 32 + Sinc1 OSR = 32) 10111b = OSR = 2048 (Sinc4 OSR = 32 + Sinc1 OSR = 64) 11000b = OSR = 4096 (Sinc4 OSR = 32 + Sinc1 OSR = 128) 11001b = OSR = 8192 (Sinc4 OSR = 32 + Sinc1 OSR = 256) 11010b = f_{DATA} = 60SPS (Sinc4 OSR = 32 + Sinc1) 11011b = f_{DATA} = 50SPS (Sinc4 OSR = 32 + Sinc1) 11100b = f_{DATA} = 16.7SPS (Sinc4 OSR = 32 + Sinc1) 11101b = f_{DATA} = 10SPS (Sinc4 OSR = 32 + Sinc1) 11110b = f_{DATA} = 25SPS (FIR) 11111b = f_{DATA} = 20SPS (FIR)

8.2.6 STEPx_DELAY_CFG Register (Address = 05h) [Reset = 00h]

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Figure 8-33. STEPx_DELAY_CFG Register

7	6	5	4	3	2	1	0
RESERVED	STEPx_DELAY[6:0]						
R-0b	R/W-0000000b						

Table 8-38. STEPx_DELAY_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved Always reads 0b.
6:0	STEPx_DELAY[6:0]	R/W	0000000b	Conversion-start delay time selection Determines the delay time that the sequencer adds before the start of the first conversion of a sequence step. The delay also applies to every conversion in global-chop mode when the input polarity is switched. n = STEPx_DELAY[6:0] bit value (ranges from 0 to 127) Additional delay time = n^2 x t_{MOD} For n = 0 no additional delay time is added. Only the device inherent delay time is applied. For n ≥ 1 the programmed delay time is added to the device inherent delay time.

8.2.7 STEPx_OFFSET_CAL_MSB Register (Address = 06h) [Reset = 00h]

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Figure 8-34. STEPx_OFFSET_CAL_MSB Register

7	6	5	4	3	2	1	0
STEPx_OFFSET_CAL[23:16]							
R/W-00000000b							

Table 8-39. STEPx_OFFSET_CAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_OFFSET_CAL[23:16]	R/W	00000000b	Offset calibration coefficient, MSB Offset calibration bits [23:16]. Provide the STEPx_OFFEST_CAL[23:0] value in two's complement format irrespective of the STEPx_CODING bit setting.

8.2.8 STEPx_OFFSET_CAL_ISB Register (Address = 07h) [Reset = 00h]

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Figure 8-35. STEPx_OFFSET_CAL_ISB Register

7	6	5	4	3	2	1	0
STEPx_OFFSET_CAL[15:8]							
R/W-00000000b							

Table 8-40. STEPx_OFFSET_CAL_ISB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_OFFSET_CAL[15:8]	R/W	00000000b	Offset calibration coefficient, ISB Offset calibration bits [15:8]. Provide the STEPx_OFFEST_CAL[23:0] value in two's complement format irrespective of the STEPx_CODING bit setting.

8.2.9 STEPx_OFFSET_CAL_LSB Register (Address = 08h) [Reset = 00h]

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Figure 8-36. STEPx_OFFSET_CAL_LSB Register

7	6	5	4	3	2	1	0
STEPx_OFFSET_CAL[7:0]							
R/W-00000000b							

Table 8-41. STEPx_OFFSET_CAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_OFFSET_CAL[7:0]	R/W	00000000b	Offset calibration coefficient, LSB Offset calibration bits [7:0]. Provide the STEPx_OFFEST_CAL[23:0] value in two's complement format irrespective of the STEPx_CODING bit setting. For 16-bit device versions (ADS114S1x), set the STEPx_OFFSET_CAL[7:0] bits to 00h.

8.2.10 STEPx_GAIN_CAL_MSB Register (Address = 09h) [Reset = 40h]

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Figure 8-37. STEPx_GAIN_CAL_MSB Register

7	6	5	4	3	2	1	0
STEPx_GAIN_CAL[15:8]							
R/W-01000000b							

Table 8-42. STEPx_GAIN_CAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_GAIN_CAL[15:8]	R/W	01000000b	Gain calibration coefficient, MSB Gain calibration bits [15:8]. Provide the STEPx_GAIN_CAL[15:0] value in straight binary format. The device divides the STEPx_GAIN_CAL[15:0] register value by 4000h and then multiplies the result with the conversion data.

8.2.11 STEPx_GAIN_CAL_LSB Register (Address = 0Ah) [Reset = 00h]

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Figure 8-38. STEPx_GAIN_CAL_LSB Register

7	6	5	4	3	2	1	0
STEPx_GAIN_CAL[7:0]							
R/W-00000000b							

Table 8-43. STEPx_GAIN_CAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_GAIN_CAL[7:0]	R/W	00000000b	Gain calibration coefficient, LSB Gain calibration bits [7:0]. Provide the STEPx_GAIN_CAL[15:0] value in straight binary format. The device divides the STEPx_GAIN_CAL[15:0] register value by 4000h and then multiplies the result with the conversion data.

8.2.12 STEPx_SYSMON_CFG Register (Address = 0Bh) [Reset = 00h]

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Figure 8-39. STEPx_SYSMON_CFG Register

7	6	5	4	3	2	1	0
RESERVED		STEPx_BOCS[1:0]		RESERVED	STEPx_SYS_MON[2:0]		
R-00b		R/W-00b		R/W-0b	R/W-000b		

Table 8-44. STEPx_SYSMON_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00b	Reserved Always reads 00b.
5:4	STEPx_BOCS[1:0]	R/W	00b	Burnout current source and sink selection Enables and selects the value of the burnout current source and sink. Disable the burnout current sources when using global-chop mode (GC_EN = 1b). 00b = Disabled 01b = 0.2µA 10b = 1µA 11b = 10µA
3	RESERVED	R/W	0b	Reserved Always write 0b
2:0	STEPx_SYS_MON[2:0]	R/W	000b	System monitor input selection Selects one of the system monitors as the inputs for the PGA. The STEPx_AINP[4:0] and STEPx_AINN[4:0] bits have no effect when one of the system monitors is selected. The analog inputs are disconnected from the PGA when a system monitor is selected. The voltage reference selected by the STEPx_REF_SEL[1:0] bits is used for the system monitor measurements. For STEPx_SYS_MON[3:0] = 0011b (or 0100b respectively) select STEPx_REF_SEL[1:0] other than 01b (or 10b respectively). For STEPx_SYS_MON[3:0] = 0101b select STEPx_REF_SEL[1:0] other than 11b. Select an appropriate gain setting using the STEPx_GAIN[3:0] bits for each measurement. The STEPx_OFFSET_CAL[23:0] and STEPx_GAIN_CAL[15:0] values are ignored when a system monitor is selected for measurement. 000b = Disabled (monitors not selected) 001b = Internal short of positive and negative PGA inputs to (AVDD + AVSS) / 2 010b = Internal temperature sensor 011b = External (V_{REFP0} – V_{REFN0}) / 8 100b = External (V_{REFP1} – V_{REFN1}) / 8 101b = (AVDD – AVSS) / 8 110b = (IOVDD – DGND) / 8 111b = V_{DLDO} / 4

8.2.13 STEPx_IDAC_MAG_CFG Register (Address = 0Ch) [Reset = 00h]

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Figure 8-40. STEPx_IDAC_MAG_CFG Register

7	6	5	4	3	2	1	0
STEPx_I2MAG[3:0]				STEPx_I1MAG[3:0]			
R/W-0000b				R/W-0000b			

Table 8-45. STEPx_IDAC_MAG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	STEPx_I2MAG[3:0]	R/W	0000b	IDAC2 magnitude selection Selects the value of the excitation current source, IDAC2. 0000b = Disabled 0001b = 1x IUNIT 0010b = 10x IUNIT 0011b = 20x IUNIT 0100b = 30x IUNIT 0101b = 40x IUNIT 0110b = 50x IUNIT 0111b = 60x IUNIT 1000b = 70x IUNIT 1001b = 80x IUNIT 1010b = 90x IUNIT 1011b = 100x IUNIT 1100b = 100x IUNIT 1101b = 100x IUNIT 1110b = 100x IUNIT 1111b = 100x IUNIT
3:0	STEPx_I1MAG[3:0]	R/W	0000b	IDAC1 magnitude selection Selects the value of the excitation current source, IDAC1. 0000b = Disabled 0001b = 1x IUNIT 0010b = 10x IUNIT 0011b = 20x IUNIT 0100b = 30x IUNIT 0101b = 40x IUNIT 0110b = 50x IUNIT 0111b = 60x IUNIT 1000b = 70x IUNIT 1001b = 80x IUNIT 1010b = 90x IUNIT 1011b = 100x IUNIT 1100b = 100x IUNIT 1101b = 100x IUNIT 1110b = 100x IUNIT 1111b = 100x IUNIT

8.2.14 STEPx_IDAC1_MUX_CFG Register (Address = 0Dh) [Reset = 1Fh]

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Figure 8-41. STEPx_IDAC1_MUX_CFG Register

7	6	5	4	3	2	1	0
STEPx_IUNIT	RESERVED		STEPx_I1MUX[4:0]				
R/W-0b	R-00b		R/W-11111b				

Table 8-46. STEPx_IDAC1_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEPx_IUNIT	R/W	0b	IDAC unit current selection Selects the unit current for the excitation current sources, IDAC1 and IDAC2. 0b = IUNIT = 1µA 1b = IUNIT = 10µA
6:5	RESERVED	R	00b	Reserved Always reads 00b.
4:0	STEPx_I1MUX[4:0]	R/W	11111b	IDAC1 output pin selection Selects the output pin for IDAC1. IDAC1 and IDAC2 can be routed to the same pin if needed. An analog input that is used as an IDAC1 output, can still be used as an analog or reference input. 00000b = AIN0 00001b = AIN1 00010b = AIN2 00011b = AIN3 00100b = AIN4 00101b = AIN5 00110b = AIN6 00111b = AIN7 01000b = AIN8 (ADS1x4S18), Disconnected (ADS1x4S14) 01001b = AIN9 (ADS1x4S18), Disconnected (ADS1x4S14) 01010b = AIN10 (ADS1x4S18), Disconnected (ADS1x4S14) 01011b = AIN11 (ADS1x4S18), Disconnected (ADS1x4S14) 01100b = AIN12 (ADS1x4S18), Disconnected (ADS1x4S14) 01101b = AIN13 (ADS1x4S18), Disconnected (ADS1x4S14) 01110b = AIN14 (ADS1x4S18), Disconnected (ADS1x4S14) 01111b = AIN15 (ADS1x4S18), Disconnected (ADS1x4S14) 10000b = AIN16 (ADS1x4S18), Disconnected (ADS1x4S14) 10001b = AIN17 (ADS1x4S18), Disconnected (ADS1x4S14) 10010b = Disconnected 10011b = Disconnected 10100b = Disconnected 10101b = Disconnected 10110b = Disconnected 10111b = Disconnected 11000b = Disconnected 11001b = Disconnected 11010b = Disconnected 11011b = Disconnected 11100b = Disconnected 11101b = Disconnected 11110b = Disconnected 11111b = Disconnected

8.2.15 STEPx_IDAC2_MUX_CFG Register (Address = 0Eh) [Reset = 1Fh]

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Figure 8-42. STEPx_IDAC2_MUX_CFG Register

7	6	5	4	3	2	1	0
RESERVED			STEPx_I2MUX[4:0]				
R-000b			R/W-11111b				

Table 8-47. STEPx_IDAC2_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000b	Reserved Always reads 000b.
4:0	STEPx_I2MUX[4:0]	R/W	11111b	IDAC2 output pin selection Selects the output pin for IDAC2. IDAC1 and IDAC2 can be routed to the same pin if needed. An analog input that is used as an IDAC2 output, can still be used as an analog or reference input. 00000b = AIN0 00001b = AIN1 00010b = AIN2 00011b = AIN3 00100b = AIN4 00101b = AIN5 00110b = AIN6 00111b = AIN7 01000b = AIN8 (ADS1x4S18), Disconnected (ADS1x4S14) 01001b = AIN9 (ADS1x4S18), Disconnected (ADS1x4S14) 01010b = AIN10 (ADS1x4S18), Disconnected (ADS1x4S14) 01011b = AIN11 (ADS1x4S18), Disconnected (ADS1x4S14) 01100b = AIN12 (ADS1x4S18), Disconnected (ADS1x4S14) 01101b = AIN13 (ADS1x4S18), Disconnected (ADS1x4S14) 01110b = AIN14 (ADS1x4S18), Disconnected (ADS1x4S14) 01111b = AIN15 (ADS1x4S18), Disconnected (ADS1x4S14) 10000b = AIN16 (ADS1x4S18), Disconnected (ADS1x4S14) 10001b = AIN17 (ADS1x4S18), Disconnected (ADS1x4S14) 10010b = Disconnected 10011b = Disconnected 10100b = Disconnected 10101b = Disconnected 10110b = Disconnected 10111b = Disconnected 11000b = Disconnected 11001b = Disconnected 11010b = Disconnected 11011b = Disconnected 11100b = Disconnected 11101b = Disconnected 11110b = Disconnected 11111b = Disconnected

8.2.16 STEPx_GPIO_DATA_OUT Register (Address = 0Fh) [Reset = 00h]

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Figure 8-43. STEPx_GPIO_DATA_OUT Register

7	6	5	4	3	2	1	0
STEPx_GPIO7_DAT_OUT	STEPx_GPIO6_DAT_OUT	STEPx_GPIO5_DAT_OUT	STEPx_GPIO4_DAT_OUT	STEPx_GPIO3_DAT_OUT	STEPx_GPIO2_DAT_OUT	STEPx_GPIO1_DAT_OUT	STEPx_GPIO0_DAT_OUT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-48. STEPx_GPIO_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STEPx_GPIO7_DAT_OUT	R/W	0b	GPIO7 data Write value of GPIO7 when configured as digital output. Bit setting has no effect when GPIO7 is configured as digital input. 0b = Low 1b = High
6	STEPx_GPIO6_DAT_OUT	R/W	0b	GPIO6 data Write value of GPIO6 when configured as digital output. Bit setting has no effect when GPIO6 is configured as digital input. 0b = Low 1b = High
5	STEPx_GPIO5_DAT_OUT	R/W	0b	GPIO5 data Write value of GPIO5 when configured as digital output. Bit setting has no effect when GPIO5 is configured as digital input. 0b = Low 1b = High
4	STEPx_GPIO4_DAT_OUT	R/W	0b	GPIO4 data Write value of GPIO4 when configured as digital output. Bit setting has no effect when GPIO4 is configured as digital input or as digital output with $\overline{\text{FAULT}}$ as the data source. 0b = Low 1b = High
3	STEPx_GPIO3_DAT_OUT	R/W	0b	GPIO3 data Write value of GPIO3 when configured as digital output. Bit setting has no effect when GPIO3 is configured as digital input or as digital output with ALERT as the data source. 0b = Low 1b = High
2	STEPx_GPIO2_DAT_OUT	R/W	0b	GPIO2 data Write value of GPIO2 when configured as digital output. Bit setting has no effect when GPIO2 is configured as digital input. 0b = Low 1b = High
1	STEPx_GPIO1_DAT_OUT	R/W	0b	GPIO1 data Write value of GPIO1 when configured as digital output. Bit setting has no effect when GPIO1 is configured as digital input. 0b = Low 1b = High
0	STEPx_GPIO0_DAT_OUT	R/W	0b	GPIO0 data Write value of GPIO0 when configured as digital output. Bit setting has no effect when GPIO0 is configured as digital input. 0b = Low 1b = High

8.2.17 STEPx_COMPARATOR_HIGH_THRESHOLD_MSB Register (Address = 10h) [Reset = 00h]

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Figure 8-44. STEPx_COMPARATOR_HIGH_THRESHOLD_MSB Register

7	6	5	4	3	2	1	0
STEPx_COMP_HIGH_TH[15:8]							
R/W-00000000b							

Table 8-49. STEPx_COMPARATOR_HIGH_THRESHOLD_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_COMP_HIGH_TH[15:8]	R/W	00000000b	Comparator high threshold, MSB Comparator high threshold bits [15:8]. The STEPx_COMP_HIGH_TH[15:0] value sets the digital comparator high threshold for sequence step x. Conversion results larger than the high threshold increment the alert counter. Enable the high threshold using the STEPx_COMP_HIGH_TH_EN bit. The coding of the threshold value follows the STEPx_CODING bit. Unipolar straight binary: LSB size = (V_{REF}) / (Gain x 2^{16}) Bipolar two's complement: LSB size = (2 x V_{REF}) / (Gain x 2^{16})

8.2.18 STEPx_COMPARATOR_HIGH_THRESHOLD_LSB Register (Address = 11h) [Reset = 00h]

Return to the Summary Table.

Figure 8-45. STEPx_COMPARATOR_HIGH_THRESHOLD_LSB Register

7	6	5	4	3	2	1	0
STEPx_COMP_HIGH_TH[7:0]							
R/W-00000000b							

Table 8-50. STEPx_COMPARATOR_HIGH_THRESHOLD_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_COMP_HIGH_TH[7:0]	R/W	00000000b	Comparator high threshold, LSB Comparator high threshold bits [7:0]. The STEPx_COMP_HIGH_TH[15:0] value sets the digital comparator high threshold for sequence step x. Conversion results larger than the high threshold increment the alert counter. Enable the high threshold using the STEPx_COMP_HIGH_TH_EN bit. The coding of the threshold value follows the STEPx_CODING bit. Unipolar straight binary: LSB size = (V_{REF}) / (Gain x 2^{16}) Bipolar two's complement: LSB size = (2 x V_{REF}) / (Gain x 2^{16})

8.2.19 STEPx_COMPARATOR_LOW_THRESHOLD_MSB Register (Address = 12h) [Reset = 00h]

Return to the Summary Table.

Figure 8-46. STEPx_COMPARATOR_LOW_THRESHOLD_MSB Register

7	6	5	4	3	2	1	0
STEPx_COMP_LOW_TH[15:8]							
R/W-00000000b							

Table 8-51. STEPx_COMPARATOR_LOW_THRESHOLD_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_COMP_LOW_TH[15:8]	R/W	00000000b	Comparator low threshold, MSB Comparator low threshold bits [15:8]. The STEPx_COMP_LOW_TH[15:0] value sets the digital comparator low threshold for sequence step x. Conversion results smaller than the low threshold increment the alert counter. Enable the low threshold using the STEPx_COMP_LOW_TH_EN bit. The coding of the threshold value follows the STEPx_CODING bit. Unipolar straight binary: LSB size = (V_{REF}) / (Gain x 2^{16}) Bipolar two's complement: LSB size = (2 x V_{REF}) / (Gain x 2^{16})

8.2.20 STEPx_COMPARATOR_LOW_THRESHOLD_LSB Register (Address = 13h) [Reset = 00h]

Return to the Summary Table.

Figure 8-47. STEPx_COMPARATOR_LOW_THRESHOLD_LSB Register

7	6	5	4	3	2	1	0
STEPx_COMP_LOW_TH[7:0]							
R/W-00000000b							

Table 8-52. STEPx_COMPARATOR_LOW_THRESHOLD_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_COMP_LOW_TH[7:0]	R/W	00000000b	Comparator low threshold, LSB Comparator low threshold bits [7:0]. The STEPx_COMP_LOW_TH[15:0] value sets the digital comparator low threshold for sequence step x. Conversion results smaller than the low threshold increment the alert counter. Enable the low threshold using the STEPx_COMP_LOW_TH_EN bit. The coding of the threshold value follows the STEPx_CODING bit. Unipolar straight binary: LSB size = (V_{REF}) / (Gain x 2^{16}) Bipolar two's complement: LSB size = (2 x V_{REF}) / (Gain x 2^{16})

8.2.21 STEPx_COMPARATOR_CFG Register (Address = 14h) [Reset = 00h]

Return to the Summary Table.

Figure 8-48. STEPx_COMPARATOR_CFG Register

7	6	5	4	3	2	1	0
RESERVED				STEPx_COMP_NUM[1:0]		STEPx_COMP_HIGH_TH_EN	STEPx_COMP_LOW_TH_EN
R-0000b				R/W-00b		R/W-0b	R/W-0b

Table 8-53. STEPx_COMPARATOR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0000b	Reserved Always reads 0000b.
3:2	STEPx_COMP_NUM[1:0]	R/W	00b	Comparator alert counter threshold Number of consecutive conversions the conversion results of sequence step x need to exceed the comparator threshold before an alert is indicated by the COMP_ALERTn flag. The internal alert counter resets whenever the sequence step starts or when a conversion result falls below the threshold. 00b = 1 01b = 2 10b = 4 11b = 8
1	STEPx_COMP_HIGH_TH_EN	R/W	0b	Comparator high threshold enable Enables the high threshold of the digital comparator. 0b = Disabled 1b = Enabled
0	STEPx_COMP_LOW_TH_EN	R/W	0b	Comparator low threshold enable Enables the low threshold of the digital comparator. 0b = Disabled 1b = Enabled

8.2.22 STEPx_REG_MAP_CRC Register (Address = 3Dh) [Reset = 0Eh]

Return to the Summary Table.

Figure 8-49. STEPx_REG_MAP_CRC Register

7	6	5	4	3	2	1	0
STEPx_REG_MAP_CRC_VALUE[7:0]							
R/W-00001110b							

Table 8-54. STEPx_REG_MAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_REG_MAP_CRC_VALUE[7:0]	R/W	00001110b	Register map CRC value for the Step x Configuration page This value is the user-calculcated CRC value of registers 00h to 14h.

8.2.23 STEPx_PAGE_INDICATOR Register (Address = 3Eh) [Reset = 00h]

Return to the Summary Table.

Figure 8-50. STEPx_PAGE_INDICATOR Register

7	6	5	4	3	2	1	0
STEPx_PAGE_INDICATOR[7:0]							
R-00000000b							

Table 8-55. STEPx_PAGE_INDICATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_PAGE_INDICATOR[7:0]	R	00000000b	Register page indicator Read the register page indicator to verify the register page which is currently selected for reading and writing registers.

8.2.24 STEPx_PAGE_POINTER Register (Address = 3Fh) [Reset = 00h]

Return to the Summary Table.

Figure 8-51. STEPx_PAGE_POINTER Register

7	6	5	4	3	2	1	0
STEPx_PAGE_POINTER[7:0]							
R/W-00000000b							

Table 8-56. STEPx_PAGE_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STEPx_PAGE_POINTER[7:0]	R/W	00000000b	Register page pointer Write the register page pointer to select the desired register page for reading and writing registers.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Serial Interface Connections

Figure 9-1 shows the basic interface connections for the ADS1x4S1x. Dotted lines indicate optional connections. The CLK pin is tied to DGND in this example to show operation with the internal oscillator.

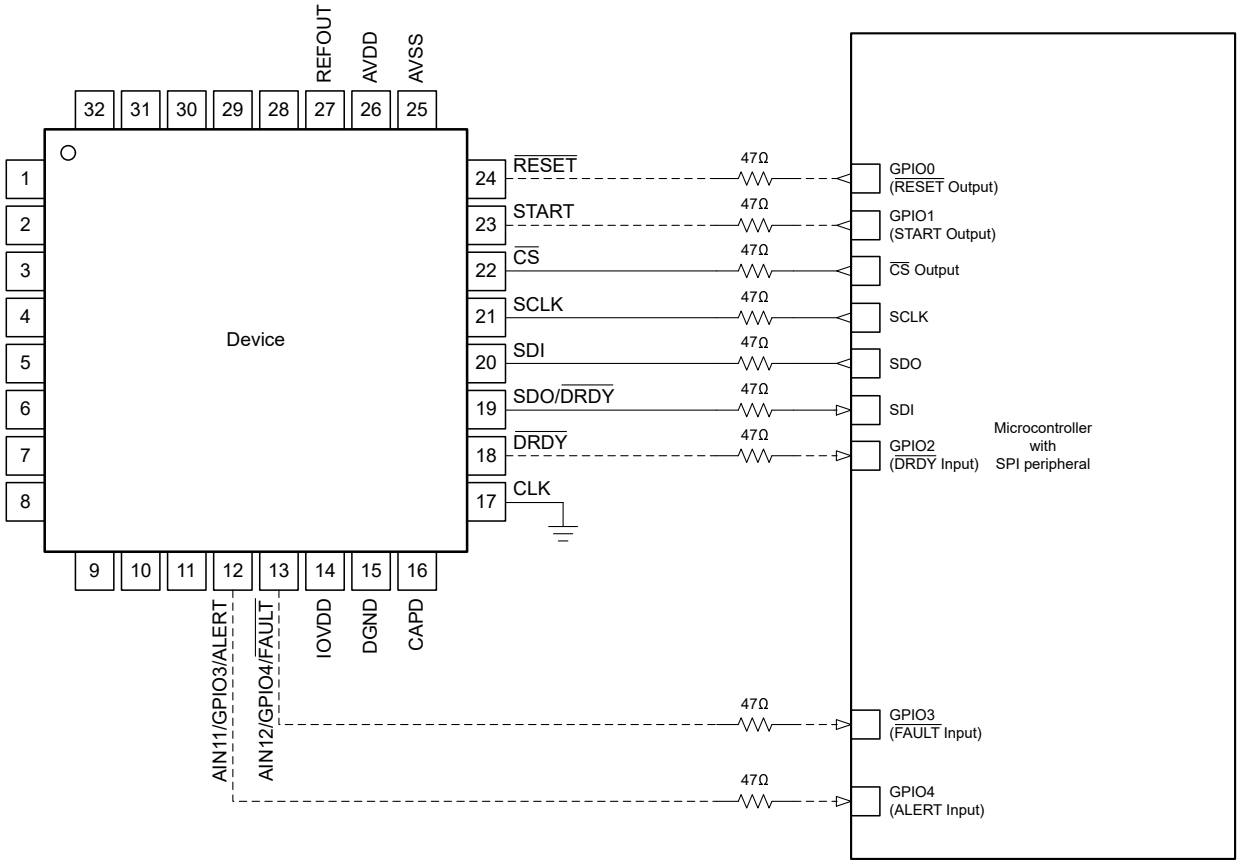

Figure 9-1. Serial Interface Connections

Most microcontroller SPI peripherals can interface with the device. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low and data are launched or changed on SCLK rising edges; data are latched or read on SCLK falling edges.

The $\overline{CS}$ pin can be tied to DGND permanently to operate the device in 3-wire SPI mode.

The following pin connections are optional:

- $\overline{RESET}$ pin
- START pin
- Route the dedicated $\overline{DRDY}$ pin to a falling edge triggered interrupt-capable GPIO of the host controller in case new data ready indication through an interrupt is desired.

- Interface the $\overline{\text{FAULT}}$ pin to the host controller in case fault indication through a pin is desired besides the fault indication through the fault flags. For that purpose, configure the GPIO4/$\overline{\text{FAULT}}$ pin as a $\overline{\text{FAULT}}$ output (GPIO4_CFG = 10b or 11b and GPIO4_SRC = 1b). Add a pullup resistors at the $\overline{\text{FAULT}}$ pin to IOVDD in case the pin is configured as an open-drain output.
- Interface the ALERT pin to the host controller in case the digital comparator status indication through a pin is desired besides the indication through the COMP_ALERTn flag. For that purpose, configure the GPIO3/ALERT pin as an ALERT output (GPIO3_CFG = 10b or 11b and GPIO3_SRC = 1b). Add a pullup resistors at the ALERT pin to IOVDD in case the pin is configured as an open-drain output.

Follow the guidelines in the *Unused Inputs and Outputs* section in case any of the above mentioned optional pins are not used.

Pullup or pulldown resistors can be placed on the digital input and output signal lines in case certain signal levels need to be driven during power up of the device or the microcontroller.

Optionally, place resistors in series with all digital input and output pins. Typical series resistor values range from 10Ω to 50Ω. This resistance smooths sharp signal transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitance present on the digital signal lines.

9.1.2 Unused Inputs and Outputs

Follow these guidelines for unused device pin connections:

- Leave any unused analog inputs (AINx) floating or connect the unused analog inputs to AVSS.
- Leave any unused reference inputs (REFPx, REFNx) floating or connect the unused reference inputs to AVSS.
- Tie the CLK pin to DGND if the internal oscillator is used.
- Tie the START pin to DGND if conversion starts are controlled through SPI.
- Leave the $\overline{\text{DRDY}}$ pin floating if unused or connect the $\overline{\text{DRDY}}$ pin to IOVDD with a weak pullup resistor.
- Tie the $\overline{\text{RESET}}$ pin to IOVDD if the host does not drive the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin also has an internal pullup resistor to IOVDD.
- Configure unused GPIOx (x = 0 to 7) pins as High-Z inputs using the GPIOx_CONFIG[1:0] bits and leave the unused GPIO pins floating or connect the unused GPIO pins to AVSS.

9.1.3 Interfacing With Multiple Devices

The ADS1x4S1x offer two methods to operate multiple devices on a single SPI bus:

- Daisy-chaining using a single $\overline{CS}$ signal for all devices as explained in the *Daisy-Chain Operation* section. The host serial data output connects to SDI of the first device in the chain to transmit data. The SDO signal of the first device in the chain connects to the SDI signal of the next device, and so on. The host controller receives data from the SDO signal of the last device in the chain. All devices share the same SCLK signal. This method allows the host to talk to all devices in the chain at the same time. However, depending on the number of devices connected in the chain, the SPI frame can get very long.
- Using a dedicated $\overline{CS}$ signal for each device as shown in Figure 9-2. All devices share the SCLK, SDI and SDO/$\overline{DRDY}$ signals in this case. Only the device with $\overline{CS}$ low drives the SDO/$\overline{DRDY}$ pin. The SDO/$\overline{DRDY}$ outputs of all other devices, which have $\overline{CS}$ high, are in a high-Z state to avoid contention on the SDO line. The host controller interfaces with each device one at a time.

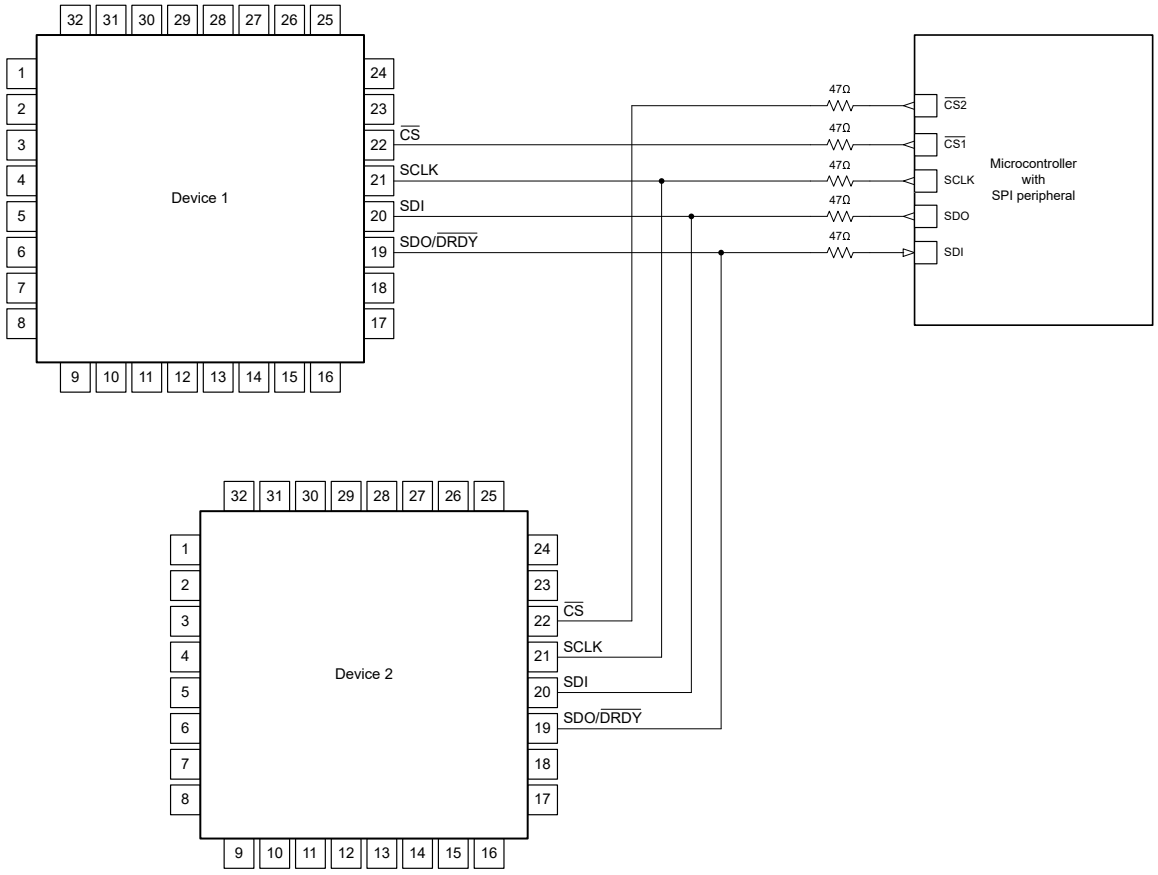

Figure 9-2. Multiple Device Serial Interface Connections Using Individual $\overline{CS}$ Signals

9.1.4 Device Initialization and Starting the Sequencer

Figure 9-3 and Figure 9-4 illustrate the sequence steps required to initialize the ADS1x4S1x and to start the sequencer, respectively. In this example:

- the STATUS header output is enabled
- sequencer mode SEQ_MODE[1:0] = 11b is used with two enabled sequence steps (step 0 and step 1)
- the device uses the dedicated $\overline{\text{DRDY}}$ pin to indicate availability of new conversion data to the host controller

Configure the SPI of the host controller to CPOL = 0 and CPHA = 1. Configure the host controller GPIO connected to the device $\overline{\text{DRDY}}$ pin as a falling edge triggered interrupt input.

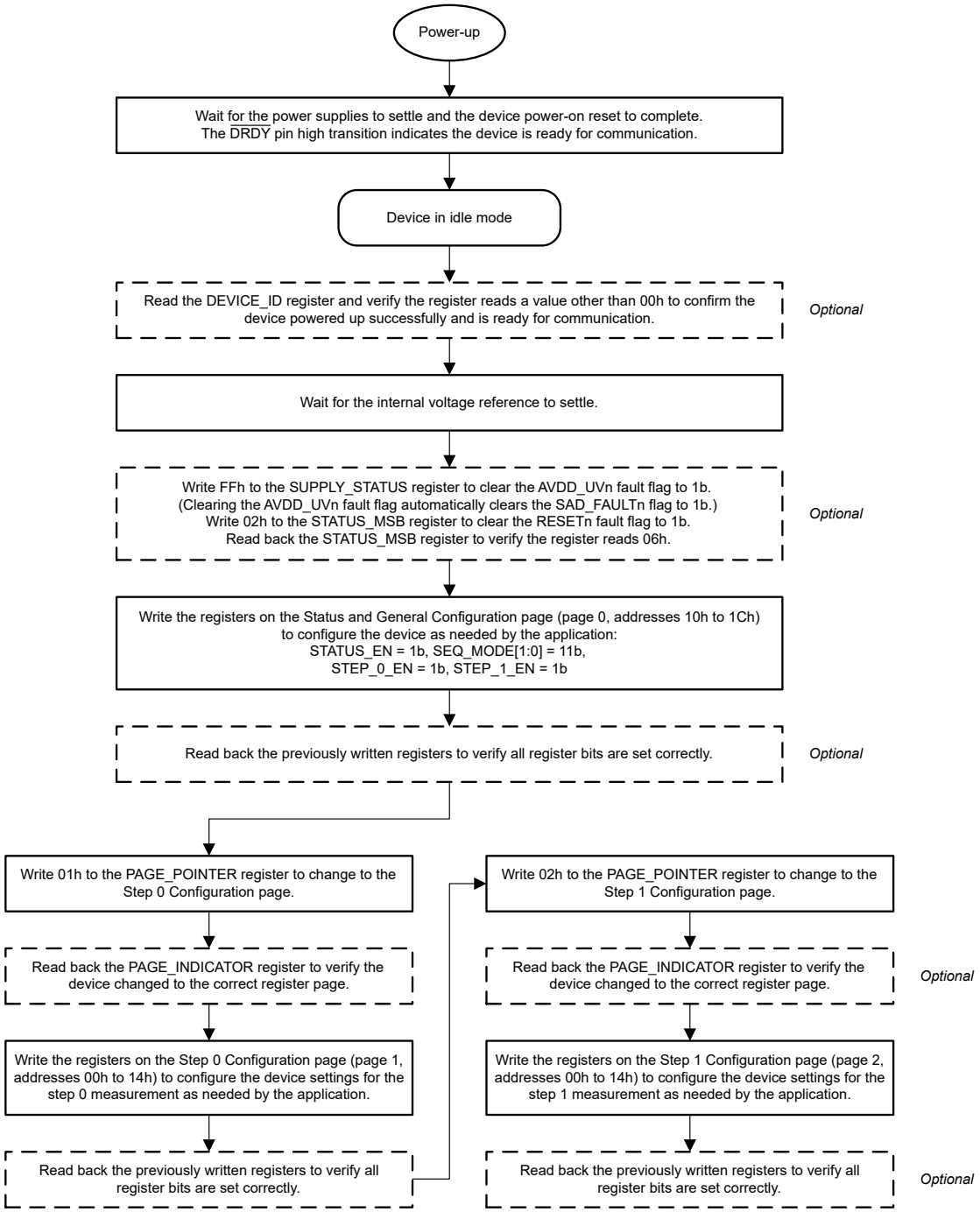

Figure 9-3. Device Initialization Flow Chart

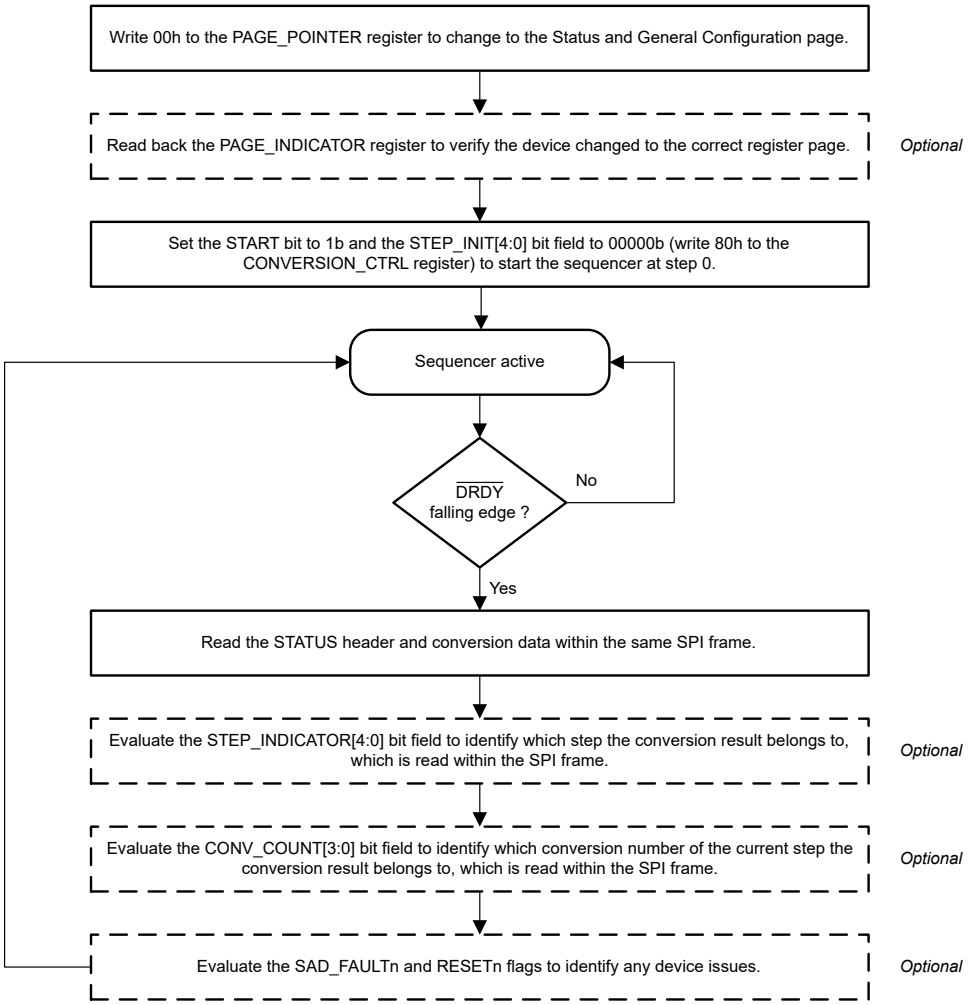

Figure 9-4. Starting the Sequencer and Reading Conversion Data Flow Chart

9.1.5 Sequencer Configuration Strategy Example

The following section explains two strategies for configuring the sequencer in case one step configuration needs to be measured more frequently than the other sequence step configurations. Assume the application requires three different measurements (A, B, C), where each measurement requires a different step configuration. Configuration A needs to be measured twice as often as configurations B and C. That means, the desired measurement sequence is A-B-A-C. Furthermore, ten consecutive measurements need to be taken with configuration A, while configurations B and C only require a single measurement each. This example sequence can be implemented in one of two ways:

1. Configure the step configuration pages as follows:
   - Step 0 = Configuration A (with STEP0_NUM_CONV[4:0] = 01001b)
   - Step 1 = Configuration B (with STEP1_NUM_CONV[4:0] = 00000b)
   - Step 2 = Configuration A (with STEP2_NUM_CONV[4:0] = 01001b)
   - Step 3 = Configuration C (with STEP3_NUM_CONV[4:0] = 00000b)

   Enable steps 0 to 3 using the STEP_0_EN to STEP_3_EN bits and configure the sequencer for mode SEQ_MODE[1:0] = 11b. Then start the sequencer from step 0. The sequencer executes the sequence A-B-A-C-A-B-A-C... until stopped by the host.
2. Configure the step configuration pages as follows:
   - Step 0 = Configuration A (with STEP0_NUM_CONV[4:0] = 01001b)
   - Step 1 = Configuration B (with STEP1_NUM_CONV[4:0] = 00000b)
   - Step 2 = Configuration C (with STEP2_NUM_CONV[4:0] = 00000b)

   Enable steps 0 to 2 using the STEP_0_EN to STEP_2_EN bits and configure the sequencer for mode SEQ_MODE[1:0] = 00b. The host starts each sequence step individually to execute the desired sequence:
   - Start step 0 (write 80h to the CONVERSION_CTRL register) and read the following ten conversion results.
   - Start step 1 (write 84h to the CONVERSION_CTRL register) and read the following conversion result.
   - Start step 0 (write 80h to the CONVERSION_CTRL register) and read the following ten conversion results.
   - Start step 2 (write 88h to the CONVERSION_CTRL register) and read the following conversion result.
   - Start step 0 and so on.

   Use this second option in case the 24 sequence steps that the device offers are not sufficient to implement the specific sequence requirements of the application using the first option. Another reason to use this second option is when the programmable user delay doesn't offer the granularity or flexibility to implement the desired sequence step timing.

9.2 Typical Applications

9.2.1 Software-Configurable RTD Measurement Input

The ADS1x4S1x integrate all necessary features (such as excitation current sources, buffered external reference inputs, and a PGA) to implement a ratiometric RTD measurement input module, which accommodates 2-, 3-, and 4-wire RTDs by means of software configuration. Figure 9-5 shows an example implementation for such a software-configurable RTD measurement input module.

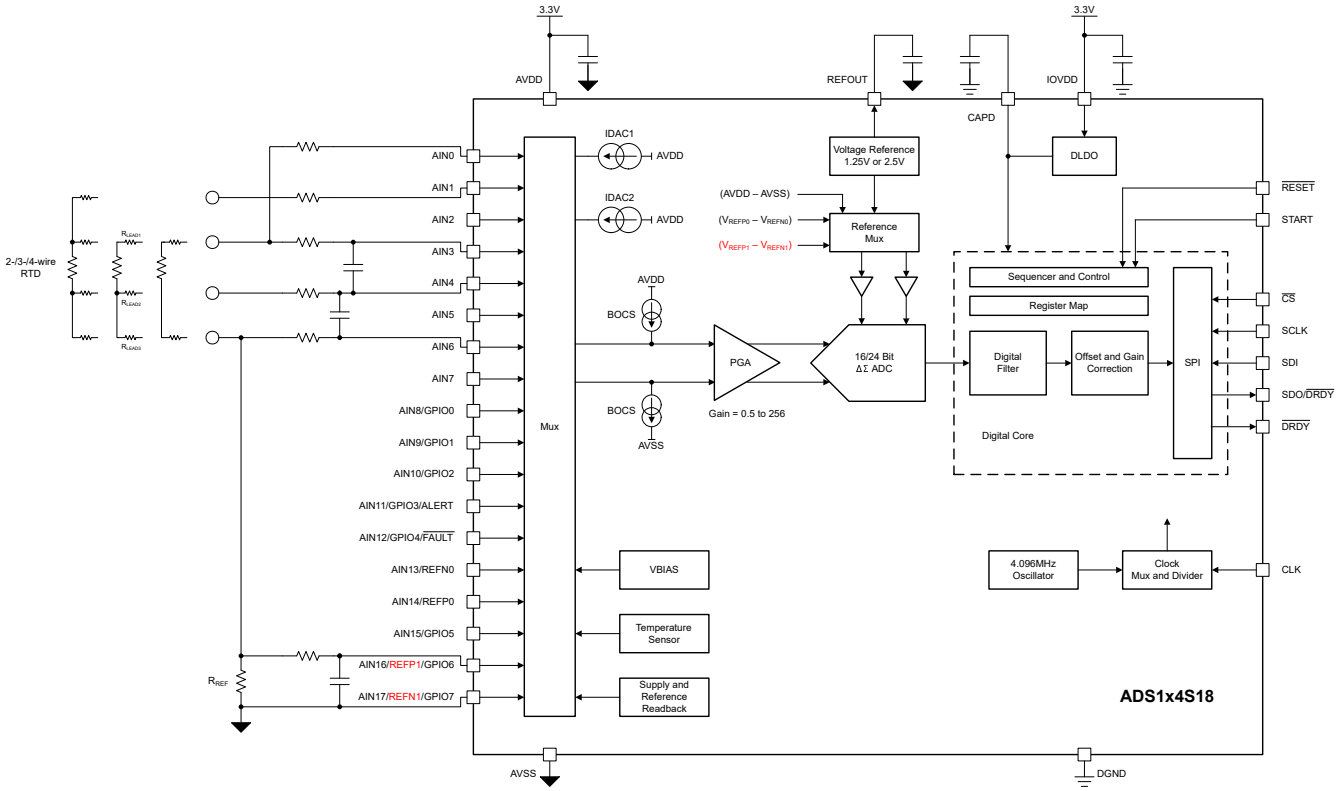

Figure 9-5. Software-Configurable RTD Measurement Input

9.2.1.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	3.3V
Supported RTD types	2-, 3-, 4-wire Pt100
Current consumption	500µA (max)
Temperature measurement range	–200°C to +850°C
Measurement accuracy at T_A = 25°C	±0.1°C
Line-cycle rejection at 50Hz or 60Hz (±1Hz)	80dB (min)
Maximum overvoltage at the RTD terminals	±10V

9.2.1.2 Detailed Design Procedure

The circuit in Figure 9-5 employs a ratiometric measurement configuration. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise of the excitation source cancel because these errors are common to both the sensor signal and the reference.

To implement a ratiometric RTD measurement using the device, route IDAC1 to either AIN1 (for a 4-wire RTD connection) or to AIN0 (for 2- and 3-wire RTD connections) using the STEPx_I1MUX[4:0] bits. Select the excitation current source value using the STEPx_IUNIT and STEPx_I1MAG[3:0] bits. The excitation current flows through the RTD and a precision, low-drift reference resistor, R_{REF} to ground. The voltage, V_{REF}, generated across the reference resistor (as shown in Equation 21) is used as the ADC reference voltage. For that purpose, select the external voltage reference between pins REFP1 and REFN1 using the STEPx_REF_SEL[1:0] bits.

$$V_{REF} = I_{IDAC1} \times R_{REF} \quad (21)$$

To simplify the following discussion, the individual lead resistance values of the RTDs (R_{LEADx}) are set to zero. As Equation 22 shows, IDAC1 excites the RTD to produce a voltage (V_{RTD}) proportional to the temperature-dependent RTD value and the IDAC1 value.

$$V_{RTD} = R_{RTD} \times I_{IDAC1} \quad (22)$$

Select the analog inputs using the STEPx_AINP[4:0] and STEPx_AINN[4:0] bits to measure V_{RTD} based on the RTD type:

- For a 2-wire RTD, measure between AIN_P = AIN3 and AIN_N = AIN6.
- For a 3- or 4-wire RTD, measure between AIN_P = AIN3 and AIN_N = AIN4.

The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code according to Equation 23.

$$Code / 2^n = V_{RTD} \times Gain / V_{REF} = (R_{RTD} \times I_{IDAC1} \times Gain) / (I_{IDAC1} \times R_{REF}) \quad (23)$$

$$Code / 2^n = (R_{RTD} \times Gain) / R_{REF} \quad (24)$$

Where n depends on the selected coding scheme and the ADC resolution:

- n = 15 (16 bit ADC, binary two's complement format)
- n = 16 (16 bit ADC, unipolar straight binary format)
- n = 23 (24 bit ADC, binary two's complement format)
- n = 24 (24 bit ADC, unipolar straight binary format)

As shown in Equation 24, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly affects the measurement result, selecting a reference resistor with good initial accuracy and very low temperature coefficient is important to limit measurement errors introduced by R_{REF}.

The reference resistor R_{REF} not only serves to generate the reference voltage for the device, but also sets the voltages at the leads of the RTD to within the specified absolute input voltage range of the PGA. This is important in case PGA gains greater than 10 are used, because the PGA needs headroom from GND to operate when using gains greater than 10.

When designing the circuit, care must also be taken to meet the compliance voltage requirement of the IDAC. The IDAC requires that the maximum voltage drop developed across the current path to GND be equal to or less than the specified compliance voltage to operate accurately.

As stated in the *Design Requirements*, this design example describes the circuit implementation for a Pt100 element measuring temperatures ranging from –200°C to +850°C. The excitation current for the Pt100 is selected as I_{IDAC1} = 400µA to meet the required power budget of this example. As mentioned previously, besides creating the reference voltage for the ADC, the voltage across R_{REF} also sets the absolute input voltages for the RTD measurement. In general, select the largest reference voltage possible that maintains the compliance voltage of the IDAC and meets the absolute input voltage requirement of the PGA. Setting the common-mode voltage at or below half the analog supply is a good starting point for a design. 1.6V is used as the target

common-mode voltage in this example. Consequently, use Equation 25 to calculate the value for R_{REF}. The stability of R_{REF} is critical to achieve good measurement accuracy over temperature and time.

$$R_{REF} = V_{REF} / I_{IDAC1} = 1.6V / 400\mu A = 4k\Omega \quad (25)$$

As a last step, select the PGA gain to match the maximum input signal to the FSR of the ADC. The resistance of a Pt100 increases with temperature. Therefore, the maximum voltage to be measured (V_{INMAX}) occurs at the positive temperature extreme. At 850°C, a Pt100 has an equivalent resistance of approximately 391Ω as per the NIST tables. The voltage across the Pt100 equates to Equation 26:

$$V_{INMAX} = V_{RTD\ (at\ 850°C)} = R_{RTD\ (at\ 850°C)} \times I_{IDAC1} = 391\Omega \times 400\mu A = 156.4mV \quad (26)$$

The maximum gain that can be applied when using a 1.6V reference is then calculated as (1.6V / 156.4mV) = 10.23. The next smaller PGA gain setting available in the ADS1x4S1x is 10. At a gain of 10, the device offers an FSR value as described in Equation 27:

$$FSR = \pm V_{REF} / Gain = \pm 1.6V / 10 = \pm 160mV \quad (27)$$

This range allows for margin with respect to initial accuracy and drift of the IDAC and reference resistor.

To keep the ADC power consumption at a minimum, speed mode 0 (f_{MOD} = 32kHz) is selected using the SPEED_MODE[1:0] bits. And to meet the line-cycle rejection requirement at 50Hz and 60Hz, the 20SPS output data rate is selected using the STEPx_FLTR_OSR[4:0] bits. The measurement *resolution* (determined by the ADC noise) increases at the expense of higher power consumption, when selecting a faster speed mode with the same 20SPS output data rate setting. However the measurement *accuracy* (determined by the ADC DC errors, such as gain and offset error) is largely unaffected by the speed mode setting.

The primary purpose of the series resistors at the analog and positive reference inputs is to protect the device inputs from any overvoltage conditions. In case overvoltage conditions at the RTD terminals can occur in the application, select the series resistor value such that the currents into the analog and positive reference inputs get limited to less than 10mA. Series resistor values of 2.2kΩ are selected in this example to limit the input currents to less than 5mA when overvoltages up to ±10V are present at the RTD terminals. Consider the interaction of the series resistors with the input currents into the analog and reference inputs when selecting the resistor values. The voltage drop created across the series resistors causes a potential offset error. In addition, the series resistors together with the input capacitors form first order RC antialiasing filters. The exact corner frequency of the RC filters is not very critical with this delta-sigma ADC. A general recommendation is to select a corner frequency which is at least 10 times lower than the modulator frequency of the ADC.

After selecting the values for the IDAC, R_{REF}, PGA gain, and the series resistors, make sure to double check that the settings meet the absolute input voltage requirements of the PGA and the compliance voltage of the IDAC. Include the voltage drop created by IDAC1 across the RTD lead resistances and the series resistor at the IDAC1 output pin in the calculations.

Lead-wire compensation for 3-wire RTDs in this example is achieved by implementing a two-step measurement approach.

1. In step one, measure the voltage (V_1) between AIN3 and AIN4.
2. In a second measurement step, measure the voltage (V_2) between AIN3 and AIN6.

Equation 28 and Equation 29 represent the two measurements.

$$V_1 = I_{IDAC1} (R_{LEAD1} + R_{RTD}) \quad (28)$$

$$V_2 = I_{IDAC1} (R_{LEAD1} + R_{RTD} + R_{LEAD3}) \quad (29)$$

To assume that all three lead resistances have the same value, R_{LEAD}, is reasonable. Consequently, use Equation 30 to calculate the lead-wire compensated RTD voltage.

$$V_{RTD} = 2 \times V_1 – V_2 = 2 \times [I_{IDAC1} (R_{LEAD} + R_{RTD})] – I_{IDAC1} (2 \times R_{LEAD} + R_{RTD}) = I_{IDAC1} \times R_{RTD} \quad (30)$$

Table 9-2 shows the critical register bit settings for the various measurements in this design example.

Table 9-2. RTD Measurement Register Bit Settings

REGISTER BITS	2-WIRE RTD	3-WIRE RTD		4-WIRE RTD
		V_1	V_2	
SPEED_MODE[1:0]	00b (Speed Mode 0)			
STEPx_FLTR_OSR[4:0]	11111b (f_{DATA} = 20SPS)			
STEPx_GAIN[3:0]	0110b (Gain = 10)			
STEPx_REFP_BUF_EN	1b (REFP buffer enabled)			
STEPx_REFN_BUF_EN	0b (REFN buffer disabled)			
STEPx_REF_SEL[1:0]	10b (External reference between REFP1 and REFN1)			
STEPx_IUNIT	1b (IUNIT = 10µA)			
STEPx_I1MAG[3:0]	0101b (I_{IDAC1} = 40 × IUNIT)			
STEPx_I1MUX[4:0]	00000b (AIN0)	00000b (AIN0)	00000b (AIN0)	00001b (AIN1)
STEPx_AINP[4:0]	00011b (AIN3)	00011b (AIN3)	00011b (AIN3)	00011b (AIN3)
STEPx_AINN[4:0]	00110b (AIN6)	00100b (AIN4)	00110b (AIN6)	00100b (AIN4)

For more information about RTD measurement circuits and the implementation using TI ADCs see the *A Basic Guide to RTD Measurements* application note. Various strategies for sensor fault detection using features similar to the ones integrated in ADS1x4S1x are discussed in the *RTD Wire-Break Detection Using Precision Delta-Sigma ADCs* application note. A software library using C code showing how to implement the RTD linearization algorithm in the host controller is available *here*.

9.2.1.3 Application Performance Plots

Figure 9-6 and Figure 9-7 show the measurement results for a 4-wire Pt100. The measurements are taken at T_A = 25°C using precision resistors instead of a 4-wire Pt100. Figure 9-6 shows both the resistance measurement error without any calibration and after a system offset and gain calibration. The respective temperature measurement error in Figure 9-7 is calculated from the offset and gain error corrected data in Figure 9-6 using the NIST tables.

The design meets the required temperature measurement accuracy given in the *Design Requirements*. However, the measurement error shown in Figure 9-7 does not include the error of the RTD.

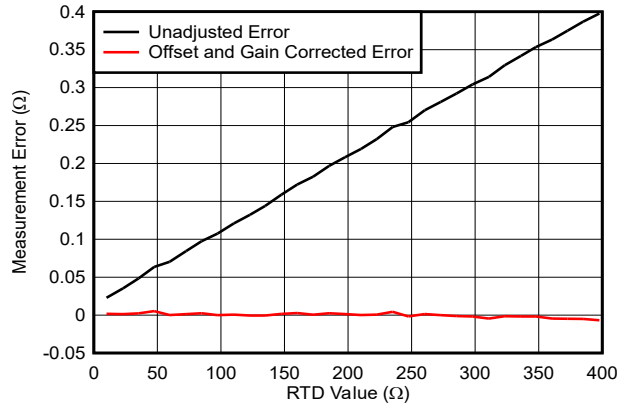

Figure 9-6. Resistance Measurement Error vs RTD Resistance

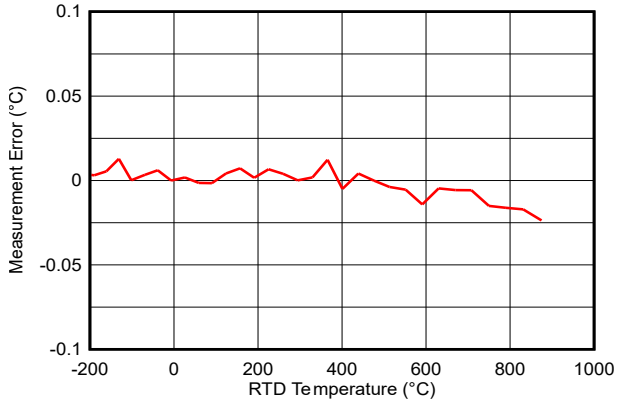

Figure 9-7. Temperature Measurement Error vs RTD Temperature

9.2.1.4 Design Variant – 3-Wire RTD Measurement With Automatic Lead-Wire Compensation Using Two IDACs

The circuit implementation shown in Figure 9-5 requires two measurements to compensate for the lead-wire resistance of a 3-wire RTD. Alternatively, leverage the second IDAC to implement automatic 3-wire RTD lead-wire compensation as shown in Figure 9-8, which does not require a separate lead wire resistance measurement step.

For that purpose, route IDAC2 to AIN7 and connect AIN7 to the point where the terminal connects to the series resistor in front of AIN4. Change both excitation current values from 400µA to 200µA (or the reference resistor value from 4kΩ to 2kΩ) in this configuration and the PGA gain from 10 to 20. A single measurement between AIN3 and AIN4 is sufficient to get a lead-wire compensated RTD value. Use Equation 31 to calculate the resistance of the 3-wire RTD in this implementation.

$$\text{Code} / 2^{n} = (R_{RTD} \times \text{Gain}) / (2 \times R_{REF}) \quad (31)$$

Where n follows the guidelines of Equation 24.

For more details see the *A Basic Guide to RTD Measurements* application note.

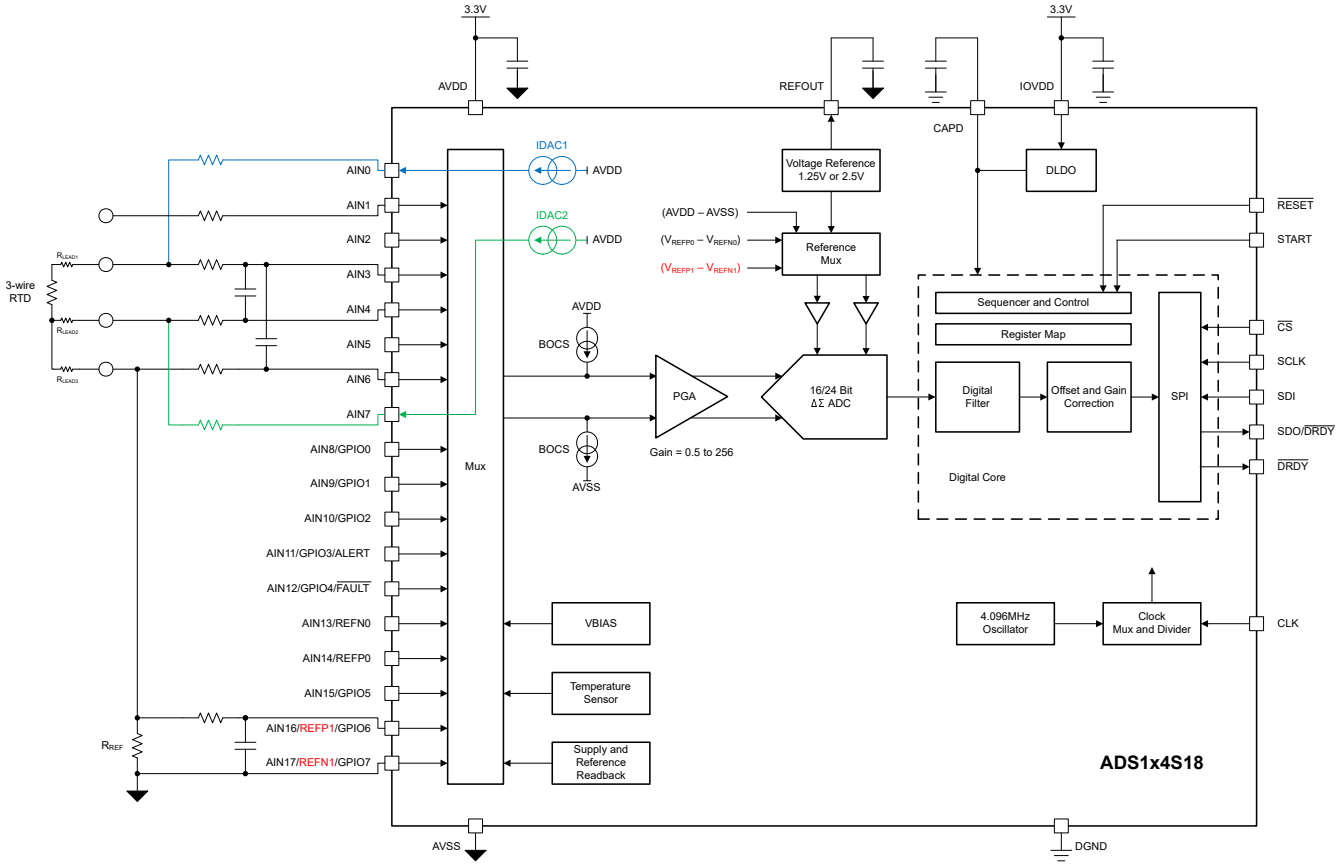

Figure 9-8. 3-wire RTD Measurement Implementation Using Two IDACs for Automatic Lead-Wire Compensation

9.2.2 Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire RTD

Figure 9-9 shows the implementation of a thermocouple measurement using a 2-wire RTD for cold-junction temperature measurement. Other ways to measure the cold-junction temperature can be used with the ADS1x4S1x as well, such as a thermistor (for example TMP61), an analog output temperature sensor (for example LMT70A), or using the integrated temperature sensor.

Equation 32 provides the relationship between ADC codes and the thermocouple voltage (V_{TC}) measured between AIN4 and AIN5.

$$\text{Code} / 2^n = (V_{TC} \times \text{Gain}) / V_{REF} \quad (32)$$

Where n follows the guidelines of Equation 24.

An important aspect of the circuit implementation is the biasing of the thermocouple so that the voltages at the thermocouple terminals meet the input voltage requirements of the ADS1x4S1x. In this example pullup and pulldown resistors (typically in the range of 1MΩ to 10MΩ) in front of the RC filter are used to bias the thermocouple output voltage to AVDD / 2. At the same time, the pullup and pulldown resistors serve as a means to detect an open sensor connection. In case of an open sensor connection, the positive analog input (AIN4) is pulled to AVDD, and the negative analog input (AIN5) to GND. This condition leads to a measurement result which is outside the normal measurement range for the thermocouple.

Many other ways to bias the thermocouple can be used as well. For example the reference output voltage can be used by connecting REFOUT to the negative thermocouple terminal instead of the pulldown resistor. For more information about thermocouple measurement circuits and the implementation using TI ADCs see the *A Basic Guide to Thermocouple Measurements* application note. A software library using C code showing how to implement the thermocouple linearization and cold-junction compensation algorithms in the host controller is available *here*.

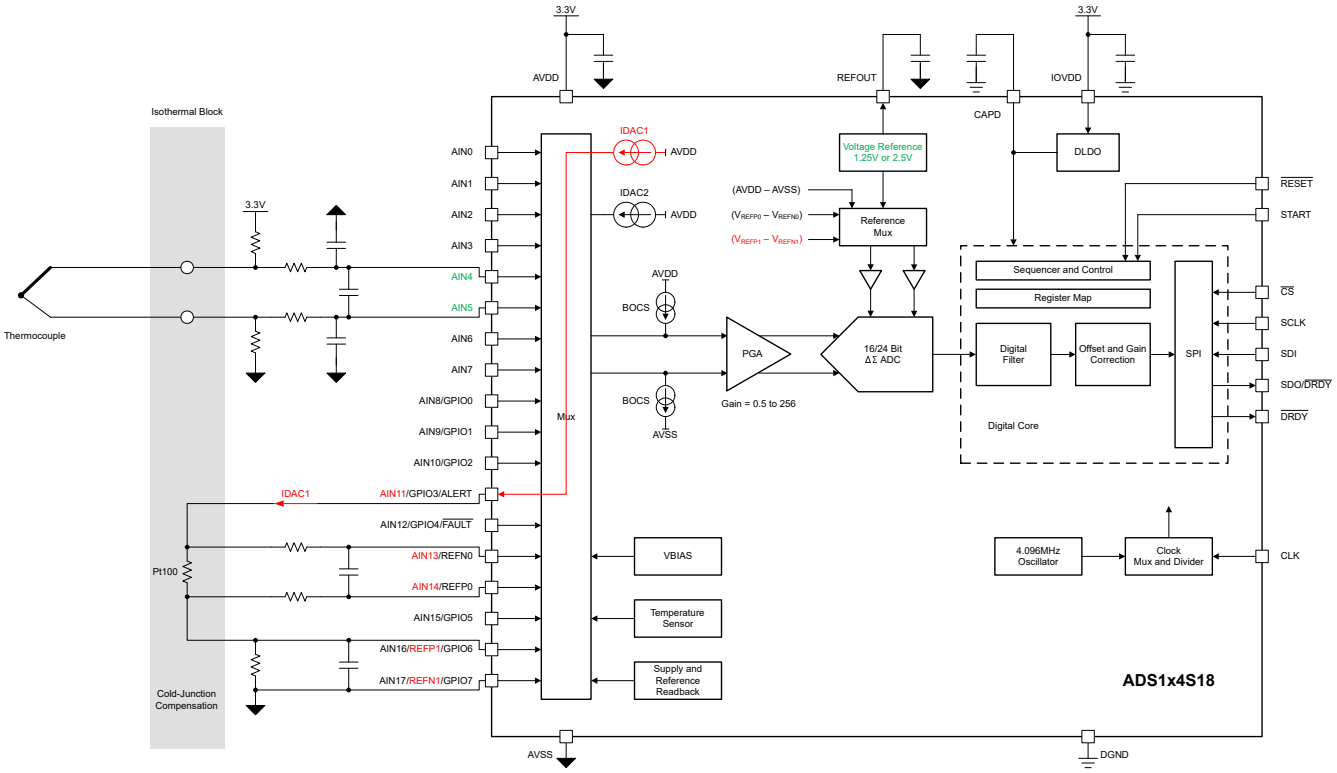

Figure 9-9. Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire RTD

9.2.3 Resistive Bridge Sensor Measurement With Temperature Compensation

Figure 9-10 and Figure 9-11 show two examples of how to implement a resistive bridge sensor measurement with temperature compensation using the ADS1x4S1x. The bridge temperature is typically used in the host controller to compensate for the bridge temperature drift.

The circuit implementation in Figure 9-10 uses the analog supply to excite the bridge sensor. Use the bridge excitation voltage as the external reference voltage for the ADC to implement a *ratiometric* bridge measurement. Instead of the analog supply, one of the integrated excitation current sources can be used to excite the bridge as well. Equation 33 through Equation 35 show how to derive the relationship between ADC output codes and the applied bridge signal using a pressure sensor as an example. Equation 35 shows that the output codes are independent of the excitation voltage in this ratiometric circuit implementation.

$$V_{Bridge} = V_{AIN6} - V_{AIN7} = (Pressure_{APL} / Pressure_{MAX}) \times Sensitivity \times V_{Excitation} \quad (33)$$

$$Code / 2^n = V_{Bridge} \times Gain / V_{REF} \quad (34)$$

$$Code / 2^n = (Pressure_{APL} / Pressure_{MAX}) \times Sensitivity \times Gain \quad (35)$$

Where:

- $V_{Excitation} = V_{REF} = AVDD$
- $Pressure_{APL}$ = the applied pressure
- $Pressure_{MAX}$ = the maximum capacity of the pressure sensor. Means the pressure where the bridge sensor outputs the full-scale output signal
- Sensitivity = the sensitivity of the bridge sensor typically given in mV/V of bridge excitation
- n follows the guidelines of Equation 24

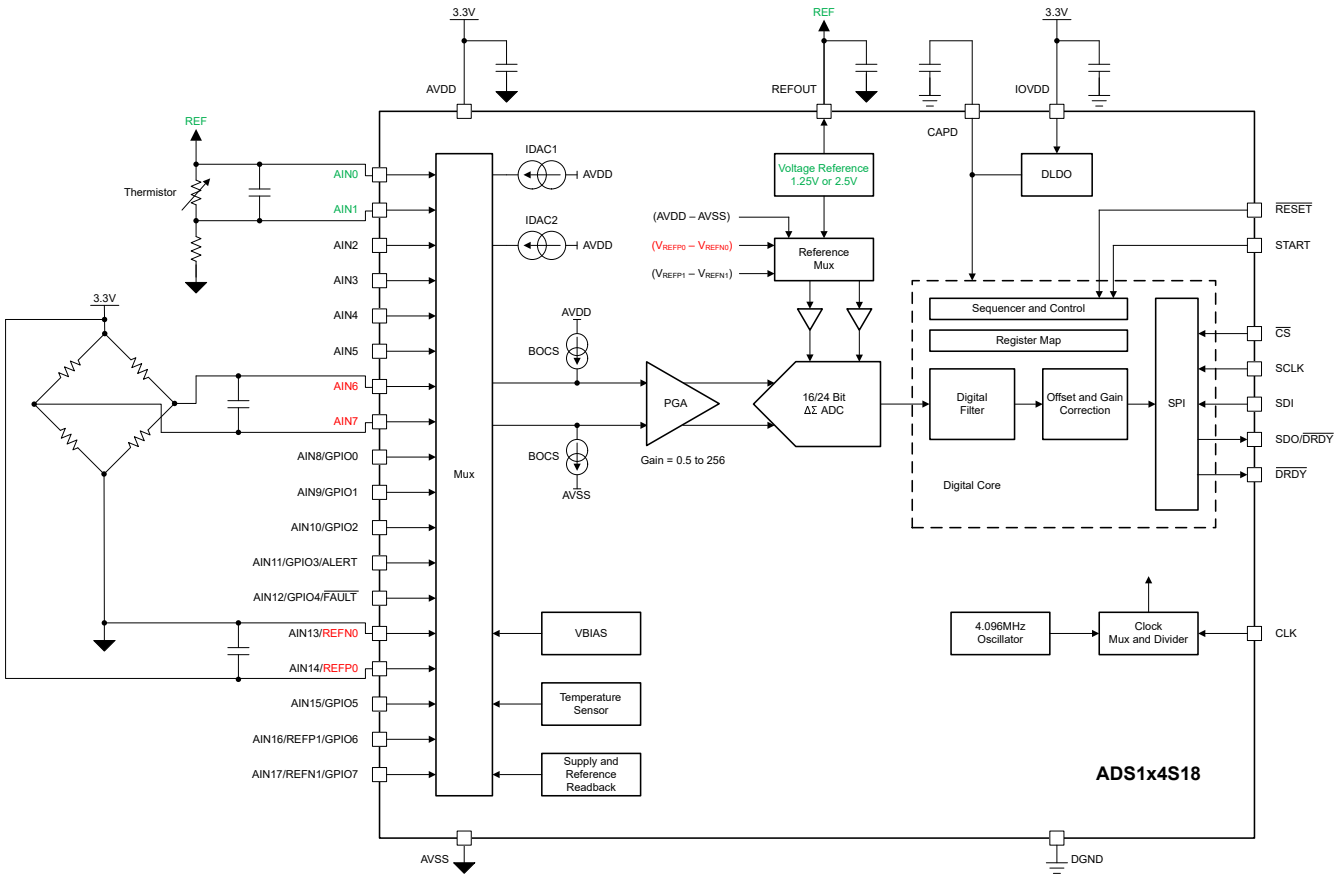

Figure 9-10. Resistive Bridge Sensor Measurement Example 1 (Using the Analog Supply as Bridge Excitation and a Thermistor for Bridge Temperature Measurement)

The example shows a thermistor to measure the bridge temperature. The reference voltage output is used in this case to implement a *ratiometric* thermistor measurement. The conversion result according to Equation 37 is only dependent on the bias resistor (R_{BIAS}) and the PGA gain setting.

$$V_{Thermistor} = V_{AIN0} - V_{AIN1} = V_{REF} \times R_{Thermistor} / (R_{Thermistor} + R_{BIAS}) \quad (36)$$

$$Code / 2^n = (V_{Thermistor} \times Gain) / V_{REF} = (R_{Thermistor} \times Gain) / (R_{Thermistor} + R_{BIAS}) \quad (37)$$

Where n follows the guidelines of Equation 24.

Figure 9-11 shows an alternative circuit implementation where the reference output is used to excite the bridge and the measurement of the temperature-dependent bridge resistance (measurement between AIN0 and AIN5) is used to determine the bridge temperature. Similar to the thermistor measurement above, the bridge resistance measurement is ratiometric and only dependent on the bias resistor and the PGA gain setting as shown in Equation 38.

$$Code / 2^n = (R_{Bridge} \times Gain) / (R_{Bridge} + R_{BIAS}) \quad (38)$$

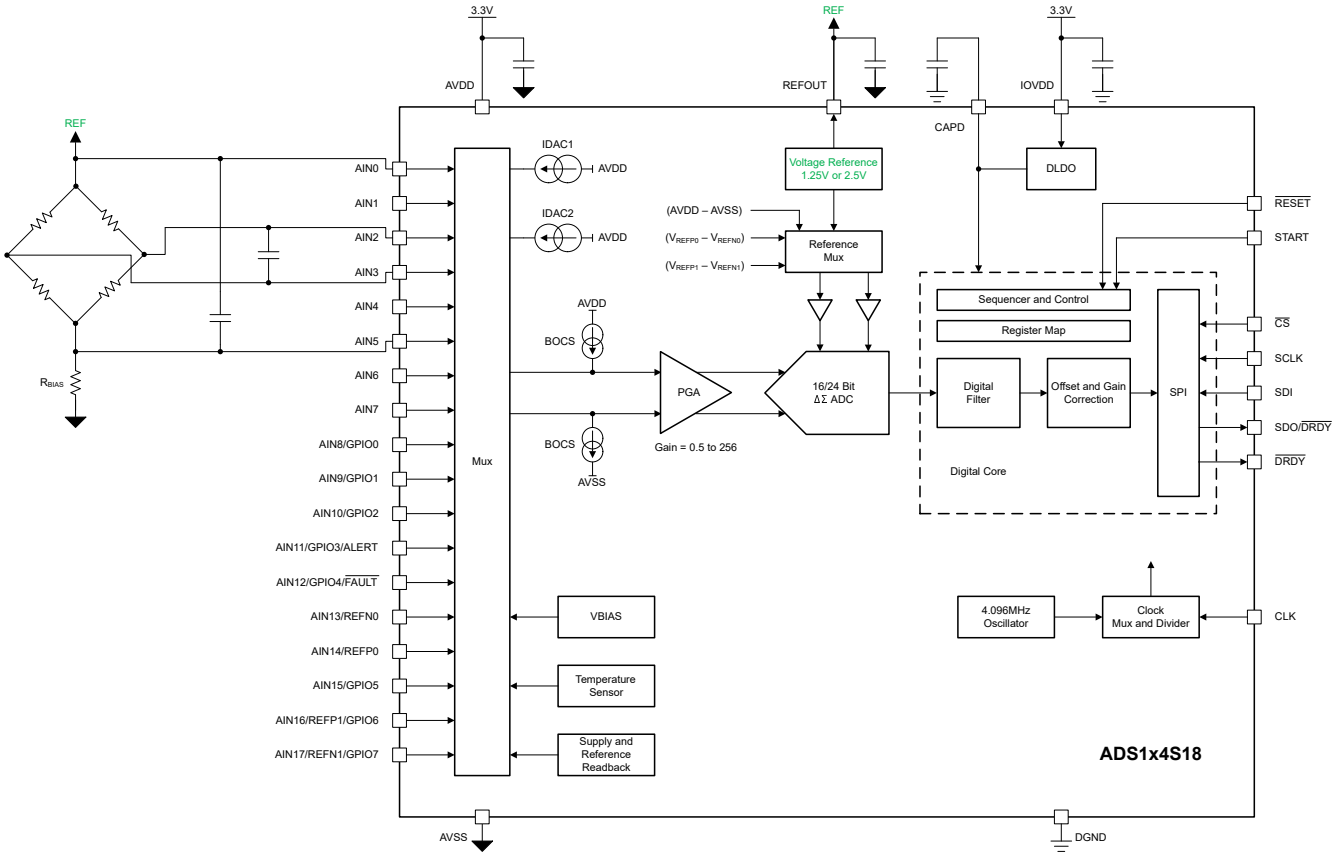

Figure 9-11. Resistive Bridge Sensor Measurement Example 2 (Using the Reference Output as Bridge Excitation and the Bridge Resistance as Temperature Measurement)

Use one of the GPIO outputs to control a switch placed between the bridge sensor and GND for applications where the bridge sensor needs to be powered down periodically to save power.

For more information about resistive bridge sensor measurement circuits and the implementation using TI ADCs see the *A Basic Guide to Bridge Measurements* application note.

9.2.4 Autonomous Power Supply Monitoring

The ADS1x4S1x are an excellent choice to implement autonomous power supply monitoring functions due to the integrated sequencer and digital comparator. Figure 9-12 shows an example configuration that monitors three supply rails leveraging the digital comparator ALERT output to notify the host of any supply over- or undervoltage conditions. The host configures the ADS114S18 after power-up and starts the sequencer. Thereafter, no host interaction with the device is required. The host only monitors the ALERT pin to get notified of any supply fault conditions.

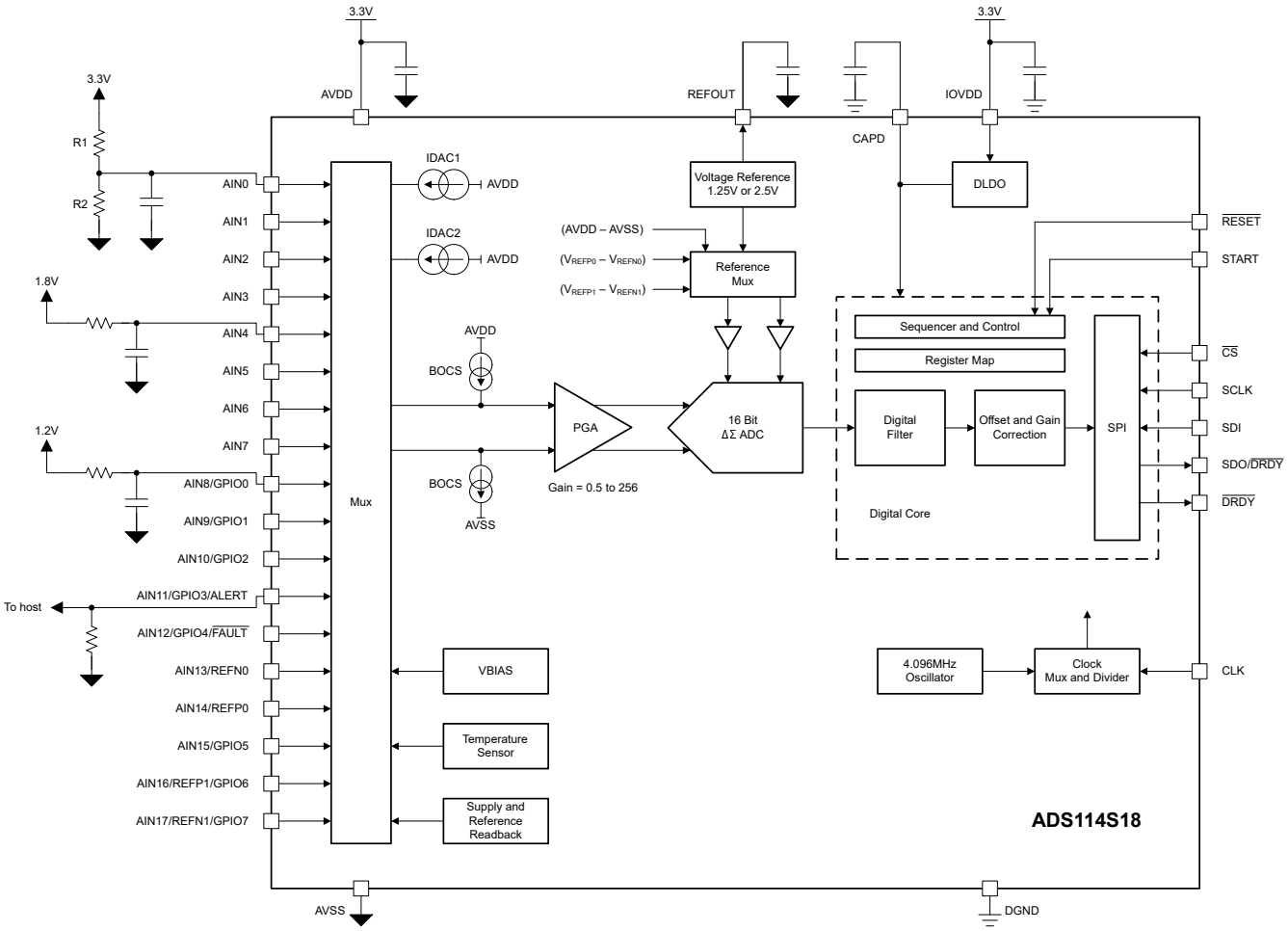

Figure 9-12. Power Supply Monitoring Example

9.2.4.1 Design Requirements

Table 9-3. Design Parameters

DESIGN PARAMETER	VALUE
Overvoltage threshold (3.3V rail)	3.5V
Undervoltage threshold (3.3V rail)	3.1V
Undervoltage threshold (1.8V rail)	1.69V
Undervoltage threshold (1.2V rail)	1.13V

9.2.4.2 Detailed Design Procedure

Monitoring a 3.3V rail while using a 3.3V AVDD supply for the ADS114S18 requires to attenuate the rail voltage before feeding the signal to the ADC inputs due to the device input voltage limitations. See the maximum *absolute input voltage* specification in the *Recommended Operating Conditions* table. To allow for margin in the design, the resistor divider values, R1 and R2, are chose such that at a 3.6V rail voltage the input signal at the analog input is less than 2.5V. In this configuration, the ADS114S18 can use gain = 1 and the internal 2.5V reference to measure rail voltages exceeding the overvoltage threshold of 3.5V. Using R1 = 50kΩ and R2 = 100kΩ sets the nominal ADC input voltage for a 3.3V rail to 2.2V. The 3.5V overvoltage threshold yields an input voltage of 2.33V, and the 3.1V undervoltage threshold and input voltage of 2.07V.

The device can measure the 1.8V and 1.2V rails directly using gain = 1 and the internal 2.5V reference without the need for any attenuation.

As a next step in the system design, calculate the digital comparator thresholds for the three rails. The design leverages the unipolar straight binary coding of the ADS114S18 because only positive input voltages need to be measured. With that, the LSB size using gain = 1 and the internal 2.5V reference calculates to:

$$\text{LSB size} = V_{REF} / (\text{Gain} \times 2^{16}) = 2.5V / 2^{16} = 38.15\mu V \quad (39)$$

Use Equation 40 to calculate the digital comparator high and low threshold code values for the three rails.

$$\text{Threshold Code} = V_{Threshold} / \text{LSB size} \quad (40)$$

As an example, set the digital comparator low threshold value for the 3.3V rail undervoltage detection to 2.07V / 38.15µV = 54176, which equates to a HEX code of D3A0h.

Next, select the sequencer operation. This example uses three sequence steps, one step for each supply rail measurement. Use sequencer mode SEQ_MODE[1:0] = 11b to implement an autonomous rail monitor that does not require any host interaction. This monitoring system example takes four consecutive measurements of each rail before switching to the next rail measurement. The comparator alert counter threshold is set to two so that two consecutive measurements on each step need to exceed the threshold before tripping the comparator.

The required speed mode and digital filter settings depend on the required fault detection time of the system.

Configure GPIO3 as an active-low, push-pull ALERT output as described in the *ALERT Output* section. In addition, add a pull-down resistor at the ALERT pin. This way, a low-level on the ALERT pin signals a supply fault to the host even when the ADS114S18 loses power or got reset, because GPIO3 reverts back to a High-Z input during device reset.

Table 9-4 summarizes the critical device register bit settings for this example.

Table 9-4. Supply Monitoring Register Bit Settings

REGISTER BITS	SEQUENCE STEP 0 3.3V RAIL	SEQUENCE STEP 1 1.8V RAIL	SEQUENCE STEP 2 1.2V RAIL
Status and General Configuration Page			
REF_VAL	1b (2.5V internal reference)		
GPIO3_CFG[1:0]	10b (GPIO3 configured as push-pull digital output)		
ALERT_PIN_POL	0b (ALERT output is active low)		
GPIO3_SRC	1b (COMP_ALERTn flag controls the GPIO3 output)		
SEQ_MODE[1:0]	11b (Sequencer continuously starts new sequence runs)		
STEP_INIT[4:0]	00000b (Start initial sequence at sequence step 0)		
STEP_x_EN	STEP_0_EN = 1b	STEP_1_EN = 1b	STEP_2_EN = 1b

Table 9-4. Supply Monitoring Register Bit Settings (continued)

REGISTER BITS	SEQUENCE STEP 0 3.3V RAIL	SEQUENCE STEP 1 1.8V RAIL	SEQUENCE STEP 2 1.2V RAIL
Step x Configuration Pages			
STEPx_AINP[4:0]	00000b (AIN0)	00100b (AIN4)	01000b (AIN8)
STEPx_AINN[4:0]	10010b (Internal AVSS connection selected as negative input)		
STEPx_REF_SEL[1:0]	00b (Internal voltage reference)		
STEPx_GAIN[3:0]	0001b (Gain = 1)		
STEPx_CODING	1b (Unipolar straight binary coding)		
STEPx_NUM_CONV[4:0]	00011b (Four consecutive conversions per step)		
STEPx_COMP_HIGH_TH[15:0]	EEEFh (2.33V)	Don't care	Don't care
STEPx_COMP_LOW_TH[15:8]	D3A0h (2.07V)	AD0Eh (1.69V)	73B6h (1.13V)
STEPx_COMP_NUM[1:0]	01b (Two consecutive conversions exceeding the threshold trigger the digital comparator)		
STEPx_COMP_HIGH_TH_EN	1b	0b	0b
STEPx_COMP_LOW_TH_EN	1b		

9.3 Power Supply Recommendations

9.3.1 Power Supplies

The device requires two external power supplies: analog (AVDD to AVSS) and digital (IOVDD to DGND). The analog power supply can be independently chosen from the digital power supply. Furthermore, the analog supply offers both unipolar (for example, AVDD = 3.3V, AVSS = 0V), and bipolar supply capability (for example, AVDD = 1.5V and AVSS = –1.5V). A non-symmetrical bipolar analog supply can also be used, for example AVDD = 2V and AVSS = –1V.

The IOVDD supply sets the logic levels for the serial interface pins ($\overline{CS}$, SCLK, SDI, SDO/$\overline{DRDY}$) and the START, $\overline{RESET}$, $\overline{DRDY}$, and CLK pins. The AVDD supply sets the logic levels for the GPIOs (GPIO0 to GPIO7).

The integrated DLDO creates the 1.4V digital core supply for the device.

9.3.2 Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage and current limits. Wait $t_{d(POR)}$ after the IOVDD supply stabilized before communicating with the device to allow the power-on reset process to complete.

9.3.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum device performance. AVDD must be decoupled with at least a 100nF capacitor to AVSS. IOVDD must be decoupled with at least a 100nF capacitor to DGND. In addition, the internal DLDO output requires a 100nF capacitor from CAPD to DGND. Figure 9-13 and Figure 9-14 show typical power-supply decoupling examples for unipolar and bipolar analog supply operation, respectively.

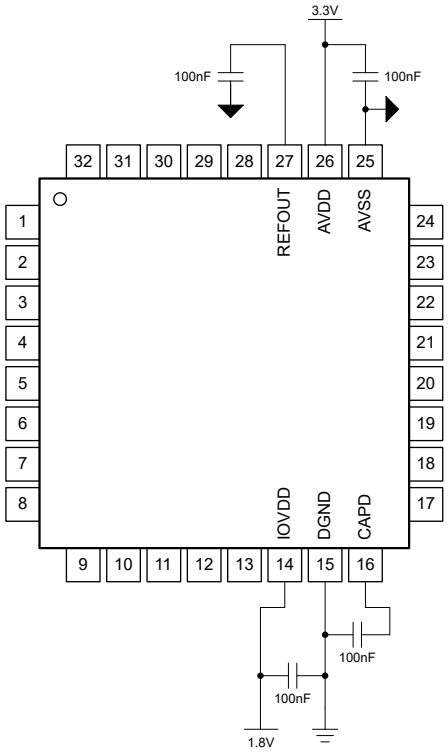

Figure 9-13. Power Supply Decoupling Unipolar Analog Supply

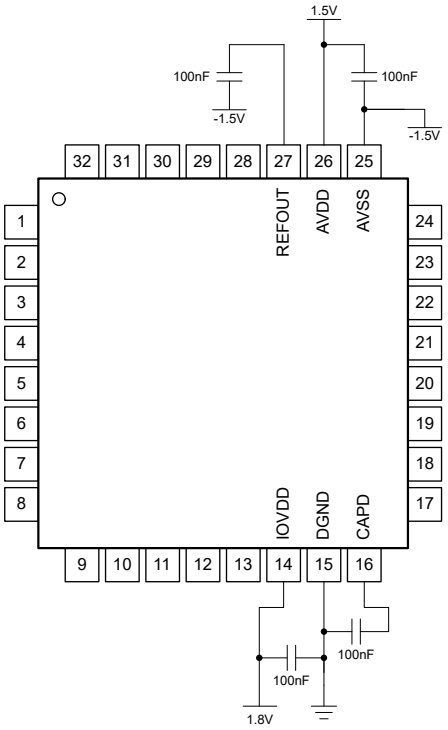

Figure 9-14. Power Supply Decoupling Bipolar Analog Supply

Place the supply bypass capacitors as close to the device power-supply pins as possible using low-impedance connections. Use multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer enhanced noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

9.4 Layout

9.4.1 Layout Guidelines

The following basic recommendations for the ADS1x4S1x layout help achieve the best possible performance of the ADC.

- For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer.
- Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. Placing the bypass capacitors on the same layer as close to the device yields the best results.
- Route digital traces away from all analog inputs and associated components to minimize interference.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Use C0G capacitors for the RC filters on the analog inputs.
- Fill void areas on signal layers with ground fill.
- When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

9.4.2 Layout Example

Figure 9-15 shows a basic layout example for the ADS1x4S1x using a unipolar analog power supply.

The following guidelines are used in this layout example:

- A single common GND plane is used for AVSS and DGND.
- C20 and C22 are the power supply decoupling capacitors. Place C20 and C22 as close as possible to the respective supply pins.
- Route the AVSS and DGND pin connections through the decoupling capacitors to the ground plane.
- C21 is the required capacitor at the CAPD pin to DGND. Place C21 as close as possible to the CAPD pin.
- C23 is the required capacitor at the REFOUT pin to AVSS. Place C23 as close as possible to the REFOUT pin.
- Differential and common-mode anti-aliasing RC-filters are shown for the differential analog input pairs AIN0-AIN1, AIN2-AIN3, AIN4-AIN5, AIN6-AIN7, AIN8-AIN9, AIN10-AIN11, AIN13-AIN14, and AIN16-AIN17.
- AIN12 and AIN15 are configured for single-ended measurements with respect to the internal AVSS connection.
- Optional series resistors (R15, R16, R17, R18, R19, R21) are shown for the digital signal lines. The series resistors help to reduce overshoot and ringing on the digital lines by smoothing the signal edges.
- The CLK pin is tied to DGND because the internal oscillator is used.

- The START pin is tied to DGND because the sequencer is controlled using the START and STOP bits.
- The $\overline{CS}$ pin has an optional pullup resistor to IOVDD to keep $\overline{CS}$ high during system power-up.
- The $\overline{RESET}$ pin has an optional pullup resistor to IOVDD.

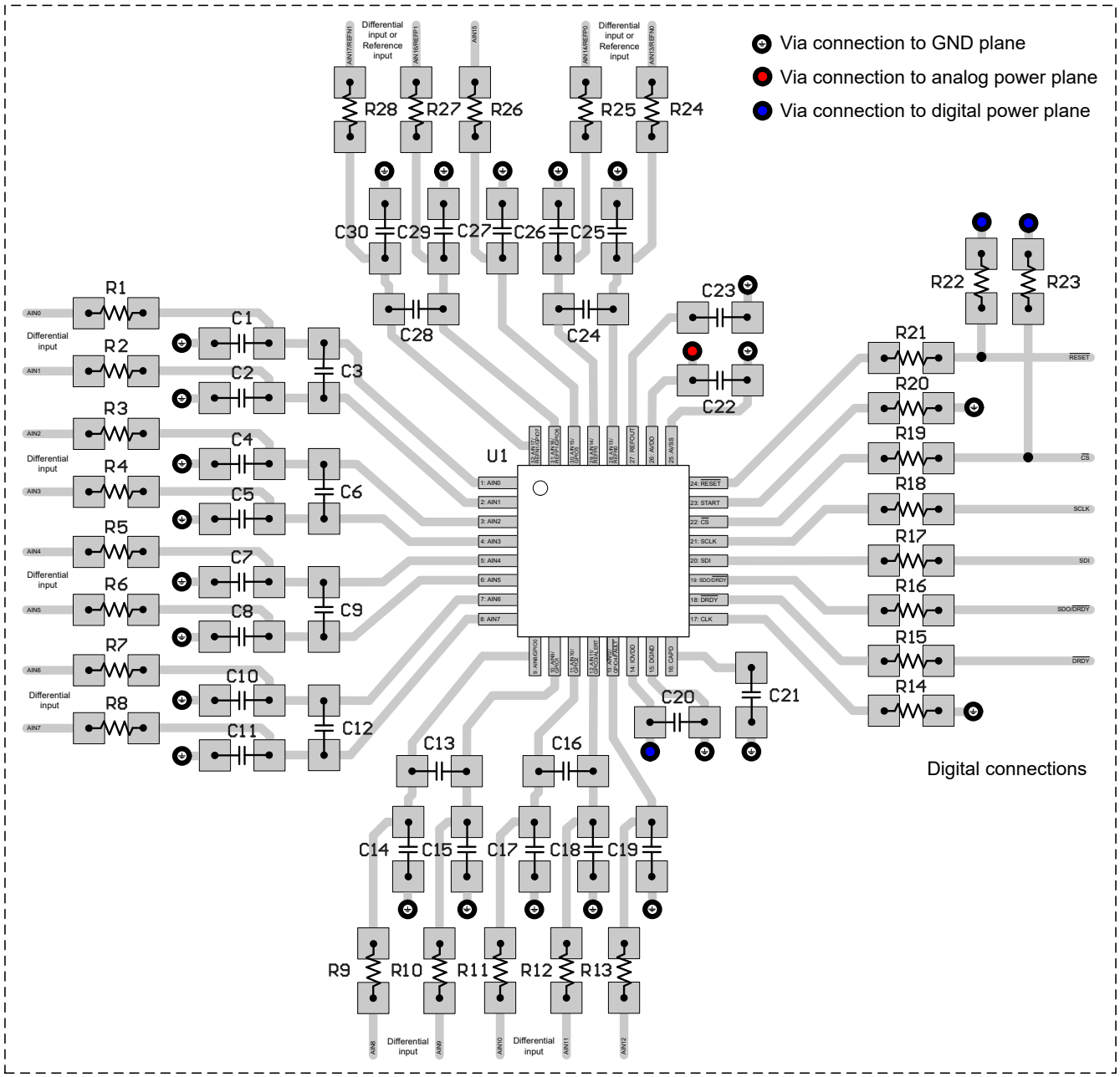

Figure 9-15. Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Related Documentation

1. Texas Instruments, *A Basic Guide to RTD Measurements* application note
2. Texas Instruments, *RTD Wire-Break Detection Using Precision Delta-Sigma ADCs* application note
3. Texas Instruments, *A Basic Guide to Thermocouple Measurements* application note
4. Texas Instruments, *A Basic Guide to Bridge Measurements* application note
5. Texas Instruments, *Temperature-sensor (RTD, thermocouple, thermistor) firmware for precision ADCs* tool page

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS124S18IPBSR	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	A124S18

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

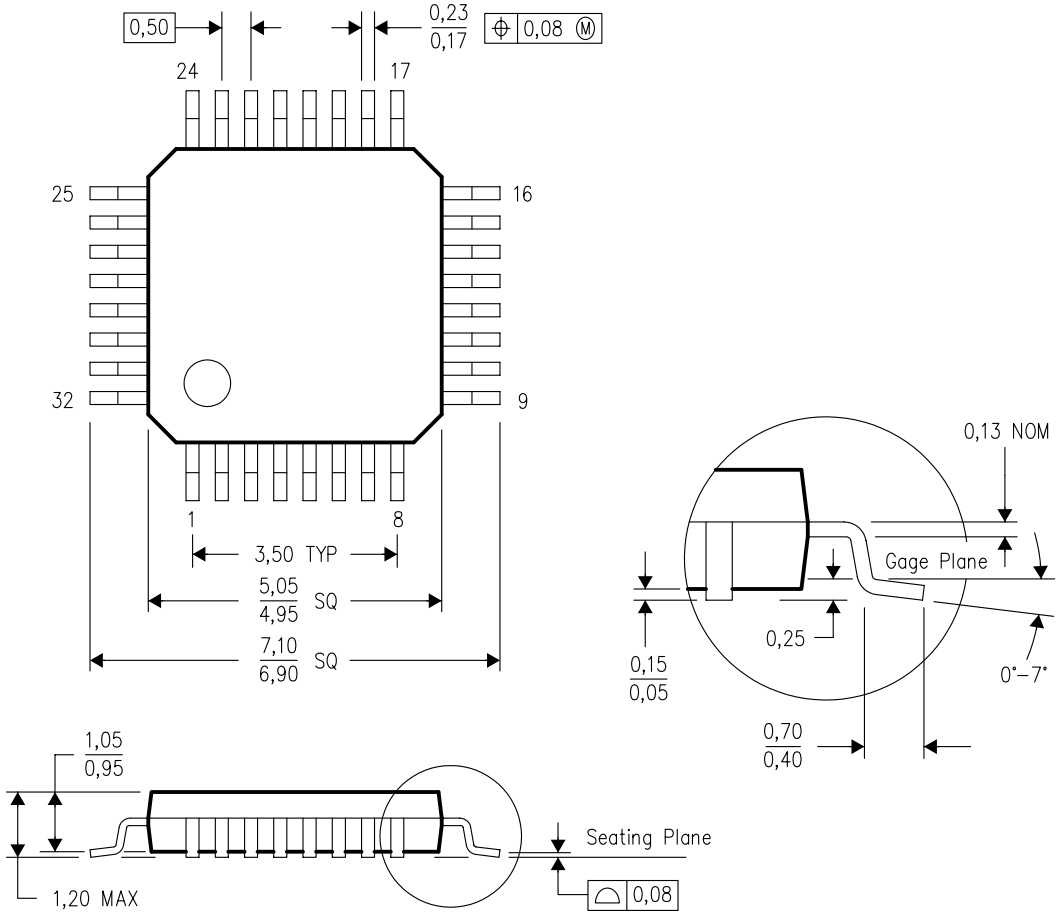
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

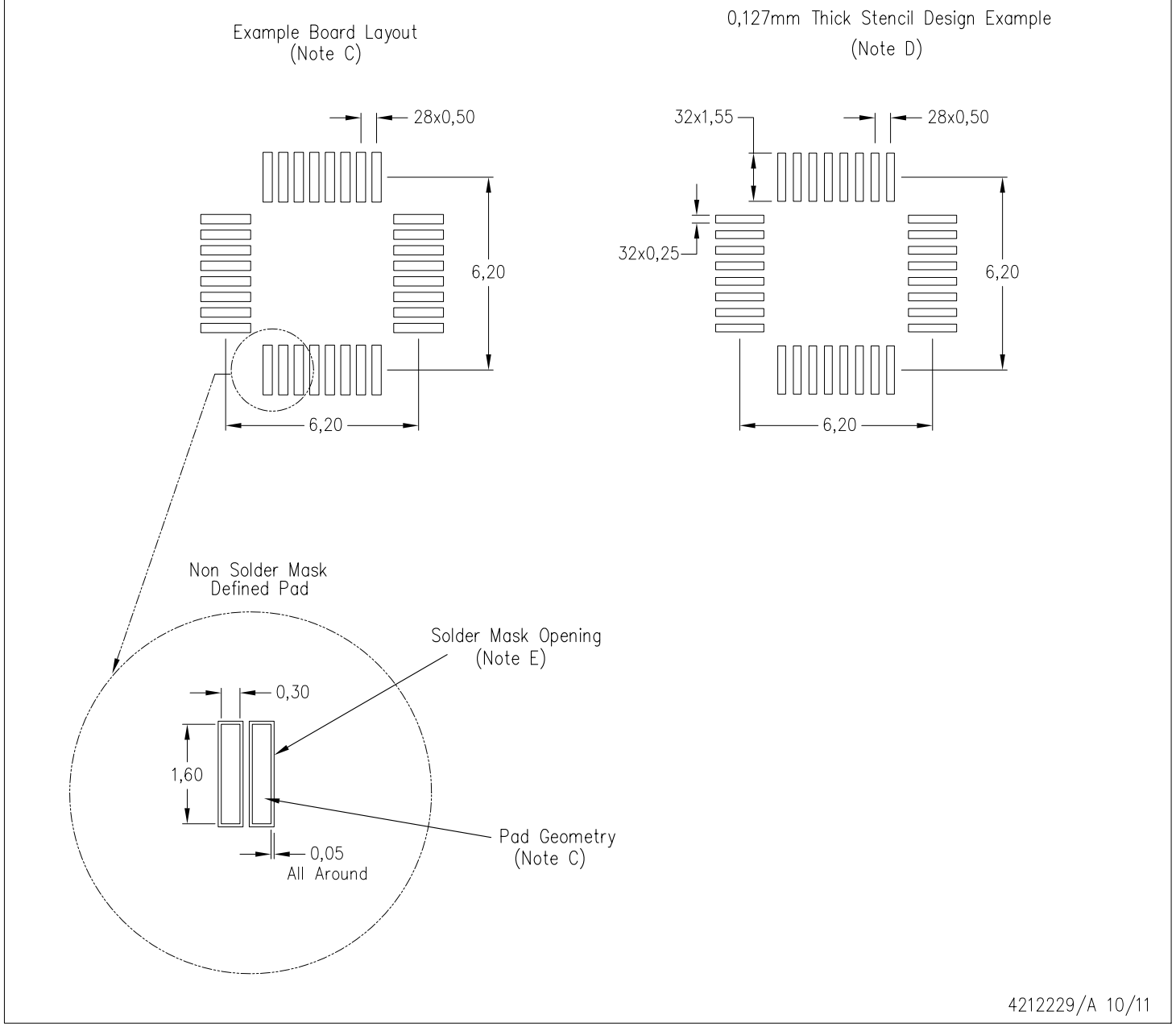
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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