ADS912x 16-Bit, 20MSPS SAR ADCs With Fully Differential ADC Input Driver

1 Features

- High-speed and low-power:
  - ADS9129: 20MSPS, 274mW
  - ADS9128: 10MSPS, 83mW
  - ADS9127: 5MSPS, 59mW
- Feature integration:
  - Integrated ADC driver
  - Integrated precision reference
  - Common-mode voltage output buffer
- High performance:
  - 16-bit no missing codes
  - INL: ±0.3LSB, DNL: ±0.3LSB
  - SNR: 93.9dB
- Wide input bandwidth:
  - ADS9129 and ADS9128: 90MHz (–3dB)
  - ADS9127: 45MHz (–3dB)
- Serial LVDS interface:
  - SDR and DDR output modes
  - Synchronous clock and data output
- Extended operating range: –40°C to +125°C

2 Applications

- Power analyzers
- Source measurement units (SMU)
- Marine equipment
- Servo drive position feedback
- DC power supplies, AC sources, electronic loads

3 Description

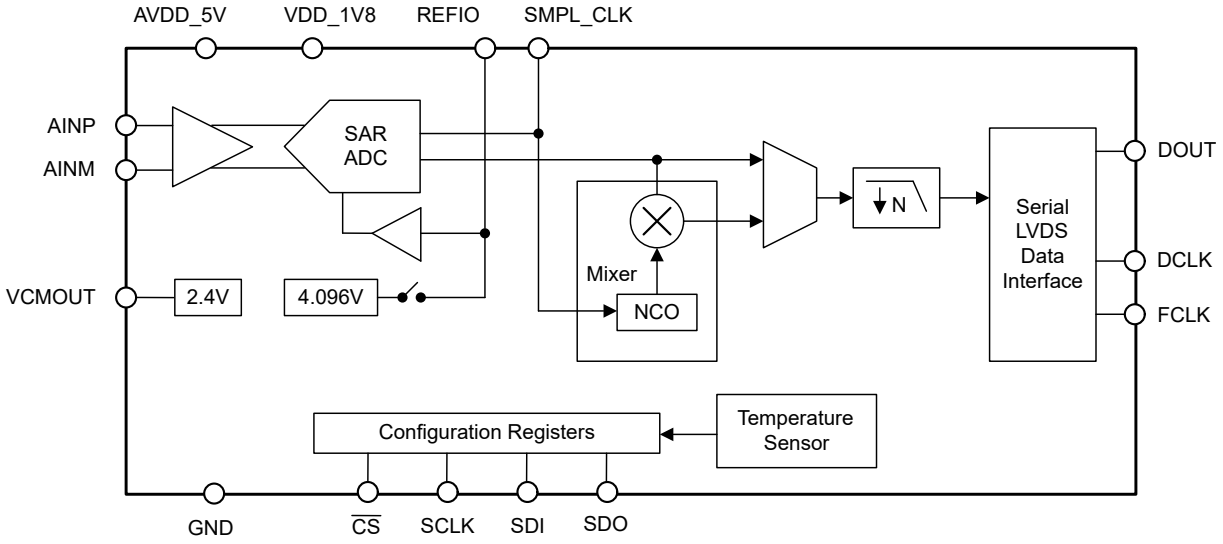
The ADS912x is a family of 16-bit, high-speed, analog-to-digital converters (ADCs) with an integrated driver for the ADC inputs. The integrated ADC driver simplifies the signal chain, reduces power consumption for precision applications, and supports high-frequency signals beyond 1MHz. By not requiring an external decoupling capacitor, the integrated ADC reference buffer is optimized for wide bandwidth applications.

The ADS912x uses a serial LVDS (SLVDS) data interface that enables high-speed digital communication while minimizing digital switching noise. Read the ADC data using separate SLVDS outputs per ADC channel or one SLVDS output for both ADC channels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS9129, ADS9128, ADS9127	RHA (VQFN, 40)	6mm × 6mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Device Block Diagram

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4 Pin Configuration and Functions

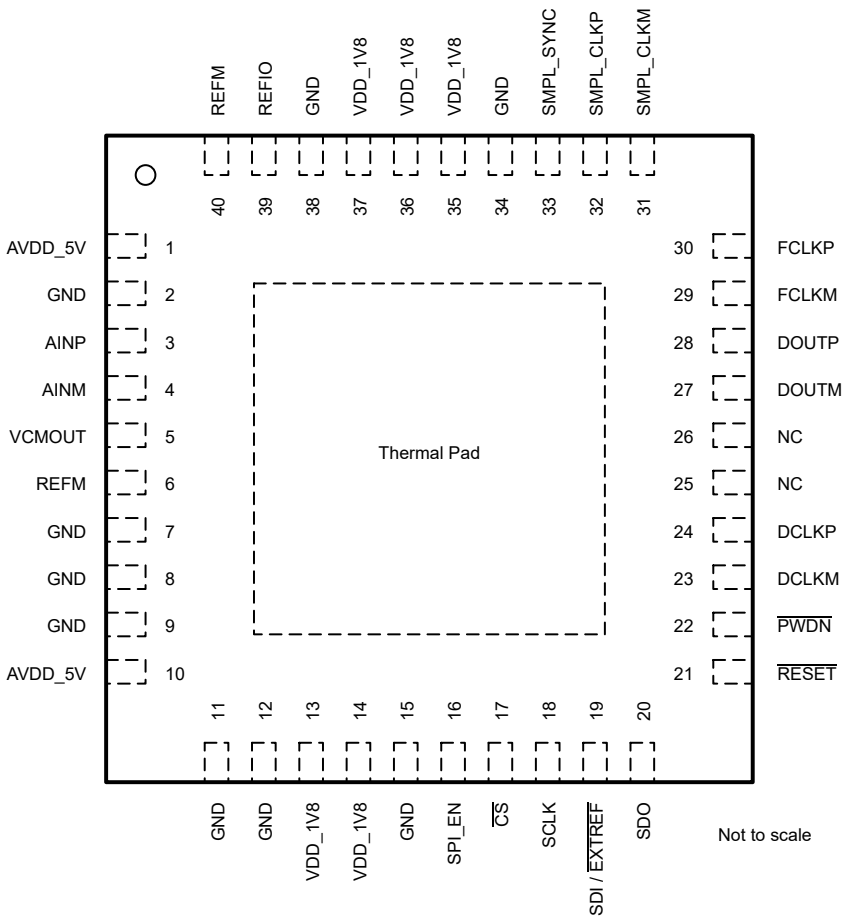

Figure 4-1. RHA Package, 6mm × 6mm, 40-Pin VQFN (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AINM	4	I	Negative analog input for ADC.
AINP	3	I	Positive analog input for ADC.
AVDD_5V	1, 10	P	5V analog power-supply pin.
$\overline{CS}$	17	I	Chip-select input pin for the interface configuration; active low.
DCLKM	23	O	Negative differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver.
DCLKP	24	O	Positive differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver.

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DOUTM	27	O	Negative differential data output. Connect a 100Ω resistor between DOUTP and DOUTM close to the receiver.
DOUTP	28	O	Positive differential data output. Connect a 100Ω resistor between DOUTP and DOUTM close to the receiver.
FCLKM	29	O	Negative differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver.
FCLKP	30	O	Positive differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver.
GND	2, 7, 8, 9, 11, 12, 15, 34, 38	P	Ground.
NC	25, 26	–	No external connection. Leave floating.
$\overline{\text{PWDN}}$	22	I	Power-down control; active low. Connect to VDD_1V8 if unused.
REFIO	39	I/O	Internal reference voltage output. External reference voltage input. Connect a 10µF decoupling capacitor to REFM.
REFM	6, 40	P	Reference ground. Connect to GND.
$\overline{\text{RESET}}$	21	I	Reset input; active low. Connect to VDD_1V8 if unused.
SCLK	18	I	Serial clock input for the interface configuration.
SDI/$\overline{\text{EXTREF}}$	19	I	SDI is a multifunction logic input; pin function is determined by the SPI_EN pin. SDI has an internal 100kΩ pulldown resistor to GND. SPI_EN = 0b: SDI is the logic input to select between the internal or external reference. Connect SDI to GND for the external reference. Connect SDI to IOVDD for the internal reference. SPI_EN = 1b: Serial data input for the interface configuration.
SDO	20	O	Serial data output for the configuration interface.
SMPL_CLKM	31	I	ADC sampling clock input. Negative differential input for the LVDS sampling clock. Connect this pin to GND for the CMOS sampling clock.
SMPL_CLKP	32	I	ADC sampling clock input. Positive differential input for the LVDS sampling clock. Clock input for the CMOS sampling clock.
SMPL_SYNC	33	I	Synchronization input for internal averaging filter. Connect to GND if unused. See the *Synchronizing Multiple ADCs* section on how to use the SMPL_SYNC pin.
SPI_EN	16	I	Control to enable the SPI configuration; active high. Connect a pullup resistor to VDD_1V8 to keep the configuration interface enabled. Connect to GND if the SPI configuration is unused.
Thermal Pad	—	P	Exposed thermal pad. Connect to GND.
VCMOUT	5	O	Common-mode voltage output. Use VCMOUT to set the common-mode voltage at the ADC inputs. Connect a 1µF decoupling capacitor to GND.
VDD_1V8	13, 14, 35, 36, 37	P	1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
VDD_1V8 to GND	–0.3	2.1	V
AVDD_5V to GND	–0.3	5.5	V
AINP and AINM to GND	–0.3	AVDD_5V + 0.3	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
Digital inputs to GND	–0.3	VDD_1V8 + 0.3	V
REFM to GND	–0.3	0.3	V
Input current to any pin except supply pins[2]	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins AINP and AINM[1]	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]	±1000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply AVDD_5V to GND	ADS9127	4.5	5	5.5	V
		ADS9128, ADS9129	4.75	5	5.25	
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.076	4.096	4.116	V
ANALOG INPUTS						
V_{IN}	Absolute input voltage	AINP and AINM to GND	V_{CM} – 1.6		V_{CM} + 1.6	V
FSR	Full-scale input range	AINP – AINM	–3.2		3.2	V
V_{CM}	Common-mode input range(1)	(AINP + AINM) / 2	V_{CMOUT} – 0.07		V_{CMOUT} + 0.07	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) ADC channel is powered down if the input common-mode voltage exceeds specifications.

5.4 Thermal Information

THERMAL METRIC(1)		ADS912x RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9129, and ADS9128, and AVDD_5V = 4.5V to 5.5V for ADS9127, VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_B	Input bias current			0.1		nA
	Input bias current thermal drift	T_A = 0°C to 70°C		0.02		nA/°C
		T_A = –40°C to 125°C		0.1		
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		–0.9	±0.3	0.9	LSB
INL	Integral nonlinearity	T_A = °C to 70°C, all devices	–0.4	±0.3	0.4	LSB
		ADS9128, ADS9127	–0.75	±0.3	0.75	
		ADS9129	–1	±0.3	1	
$V_{(OS)}$	Input offset error			±10		LSB
dV_{OS}/dT	Input offset error thermal drift			0.25	1	ppm/°C
G_E	Gain error[(1)]		–0.05	±0.01	0.05	%FSR
dG_E/dT	Gain error thermal drift[(1)]			0.5	2	ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2kHz	92	93.8		dB
		f_{IN} = 1MHz		92.9		
SNR	Signal-to-noise ratio	f_{IN} = 2kHz	92.3	93.9		dBFS
		f_{IN} = 1MHz		93.3		
THD	Total harmonic distortion	f_{IN} = 2kHz		–120		dB
		f_{IN} = 1MHz		–104		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		120		dB
		f_{IN} = 1MHz		104		
	Isolation crosstalk	f_{IN} = 2kHz		120		dB
SAMPLING DYNAMICS						
	Aperture Jitter	SIngle-ended CMOS clock on SMPL_CLKP		0.3		ps_{RMS}
		Differential LVDS sampling clock		0.8		
BW	Input-bandwidth	ADS9129, ADS9128		90		MHz
		ADS9127		45		
INTERNAL REFERENCE						
V_{REF} [(2)]	Voltage on REFIO pin (configured as output)	1µF capacitor on REFIO pin, T_A = 25°C	4.092	4.096	4.1	V
	Reference temperature drift			6	20	ppm/°C
COMMON-MODE OUTPUT BUFFER						
V_{CMOUT}	Common-mode output voltage	ADS9129	2.2	2.460	2.65	V
		ADS9128	2.2	2.410	2.65	
		ADS9127	2.2	2.385	2.65	
	Output current drive		0		5	µA
LVDS RECEIVER (SMPL_CLK)						
V_{TH}	High-level input voltage (P – M)	AC coupled	100			mV
		DC coupled	300			

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5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75V to 5.25V for ADS9129, and ADS9128, and AVDD_5V = 4.5V to 5.5V for ADS9127, VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TL}	Low-level input voltage (P – M)	AC coupled			–100	mV
		DC coupled			–300	
V_{ICM}	Input common-mode voltage		0.5	1.2	1.4	V
LVDS OUTPUT (CLKOUT and DOUT)						
V_{ODIFF}	Differential output voltage	R_L = 100Ω	200	350	500	mV
V_{OCM}	Output common-mode voltage	R_L = 100Ω	0.88	1.1	1.32	V
CMOS INPUTS ($\overline{CS}$, SCLK, and SDI)						
V_{IL}	Input low logic level		–0.1		0.5	V
V_{IH}	Input high logic level		1.3		VDD_1V8	V
CMOS OUTPUT (SDO)						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	1.4		VDD_1V8	V
POWER SUPPLY						
I_{AVDD_5V}	Supply current from AVDD_5V	at 20 MSPS throughput (ADS9129)		31	34	mA
		At 10 MSPS throughput (ADS9128)		17	21	
		At 5 MSPS throughput (ADS9127)		10	13	
		Power-down			2	
I_{VDD_1V8}	Supply current from VDD_1V8	at 20 MSPS throughput (ADS9129)		66	69	mA
I_{VDD_1V8}	Supply current from VDD_1V8	At 10 MSPS throughput (ADS9128)		45	47	
		At 5 MSPS throughput (ADS9127)		37.5	41	
		Power-down			2	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.
(2) Does not include the variation in voltage resulting from solder shift effects.

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5.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V for ADS9129, and ADS9128, and AVDD_5V = 4.5V to 5.5V for ADS9127, VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling frequency	ADS9129	7	20	MHz
		ADS9128	3.9	10	
		ADS9127	3.9	5	
t_{CYCLE}	ADC cycle time period		1 / f_{CYCLE}		s
$t_{PL_SMPLCLK}$	Sample clock low time		0.4	0.6	t_{CYCLE}
$t_{PH_SMPLCLK}$	Sample clock high time		0.4	0.6	t_{CYCLE}
f_{CLK}	Maximum SCLK frequency			10	MHz
t_{CLK}	Minimum SCLK time period		100		ns
SPI TIMINGS					
t_{hi_CSZ}	Pulse duration: $\overline{CS}$ high		220		ns
t_{PH_CK}	SCLK high time		0.48	0.52	t_{CLK}
t_{PL_CK}	SCLK low time		0.48	0.52	t_{CLK}
t_{d_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK rising edge		20		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge		10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI		5		ns
t_{d_CKCS}	Delay time: last SCLK falling edge to $\overline{CS}$ rising		5		ns

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5.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9129, and ADS9128, and AVDD_5V = 4.5V to 5.5V for ADS9127, VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			25	ms
LVDS DATA INTERFACE					
t_{RT}	Rise time	With 50Ω transmission line of length = 20mm, differential R_L = 100Ω, and C_L = 1pF		600	ps
t_{FT}	Fall time			600	ps
t_{CYCLE}	Sampling clock period	ADS9129	50		ns
		ADS9128	100		
		ADS9127	200		
t_{DCLK}	Clock output		4.167		ns
	Clock duty cycle		45	55	%
t_{d_DCLKDO}	Time delay: DCLKP rising to corresponding data valid	SDR mode	–0.35	0.35	ns
$t_{off_DCLKDO_r}$	Time offset: DCLKP rising to corresponding data valid	DDR mode	t_{DCLK} / 4 – 0.35	t_{DCLK} / 4 + 0.35	ns
$t_{off_DCLKDO_f}$	Time offset: DCLKP falling to corresponding data valid	DDR mode	t_{DCLK} / 4 – 0.35	t_{DCLK} / 4 + 0.35	ns
t_{PD}	Time delay: SMPL_CLK falling to DCLKP rising			t_{DCLK}	ns
$t_{PU_SMPL_CLK}$	Time delay: Free-running clock connected to SMPL_CLK to ADC data valid			100	µs
t_{LAT} (1)	Time delay: Internal digital delay to MSB of data output		3	12	ns
SPI TIMINGS					
t_{den_CKDO}	Time delay: 8th SCLK rising edge to SDO enable			30	ns
t_{dz_CKDO}	Time delay: 24th SCLK rising edge to SDO going Hi-Z			30	ns
t_{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			30	ns
t_{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		2		ns

(1) See section on *ADC Sampling Clock Input* for more details on data output latency.

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5.8 Timing Diagrams

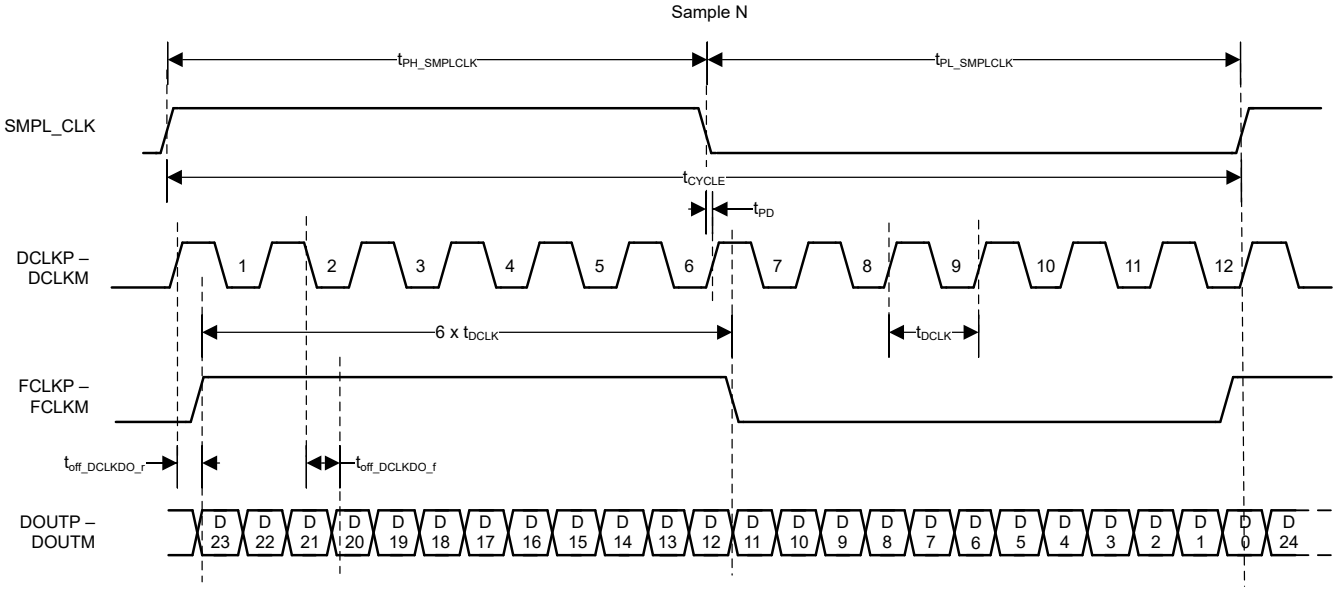


Figure 5-1. LVDS Data Interface: DDR

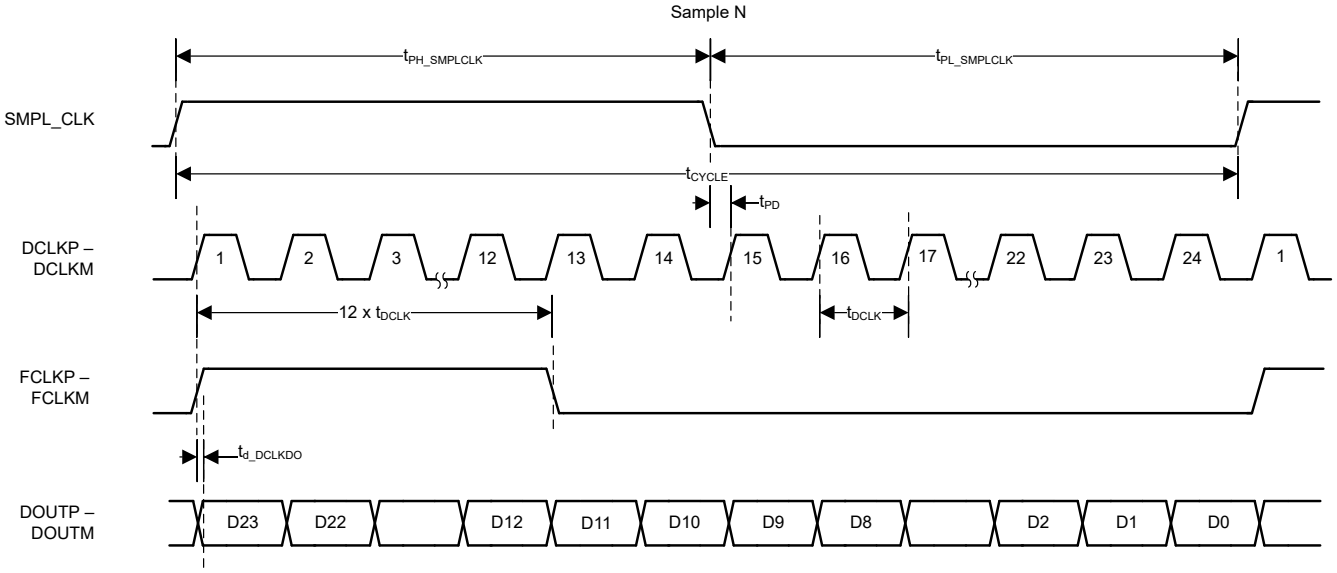


Figure 5-2. LVDS Data Interface: SDR

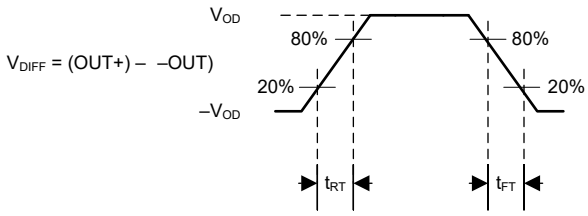


Figure 5-3. LVDS Output Transition Times

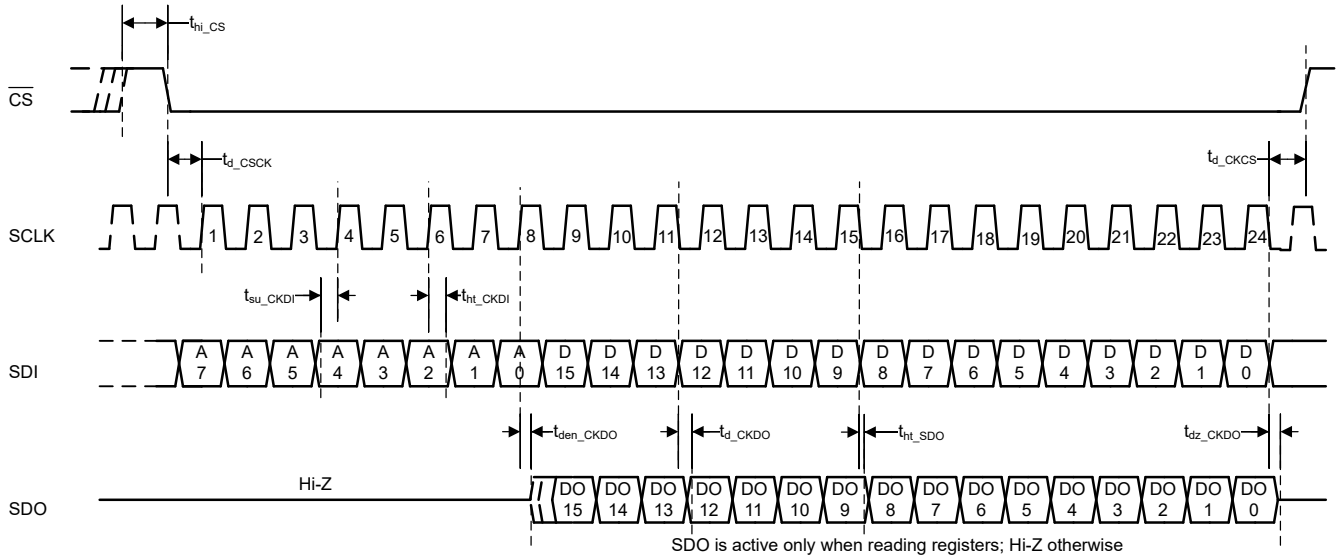


Figure 5-4. Configuration SPI

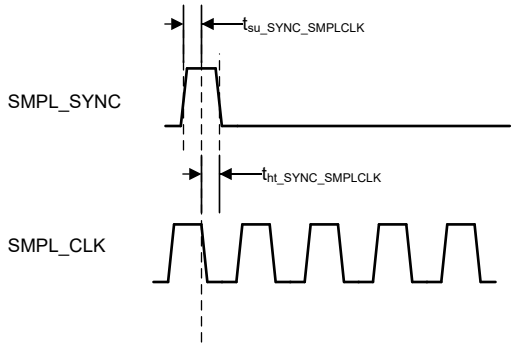
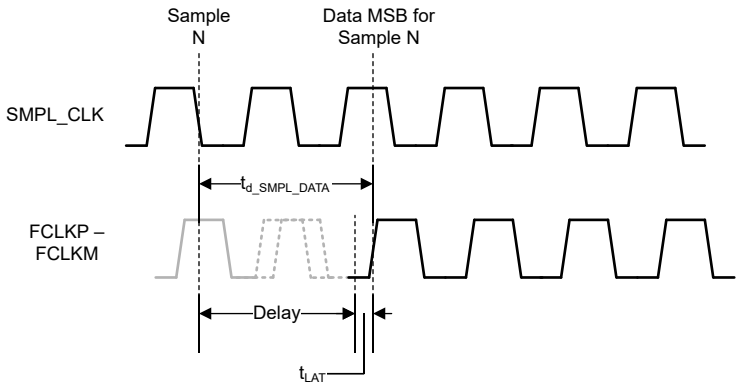


Figure 5-5. SMPL_SYNC Timing



1. See the *ADC Sampling Clock Input* section for more details.

Figure 5-6. Sampling Edge to Corresponding Data MSB Output Timing

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5.9 Typical Characteristics: All Devices

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

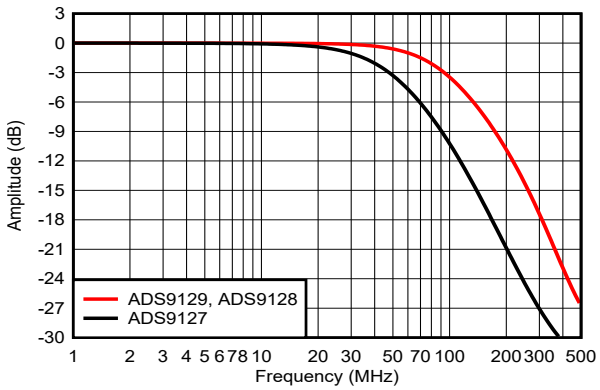

Figure 5-7. Typical Analog Input Bandwidth

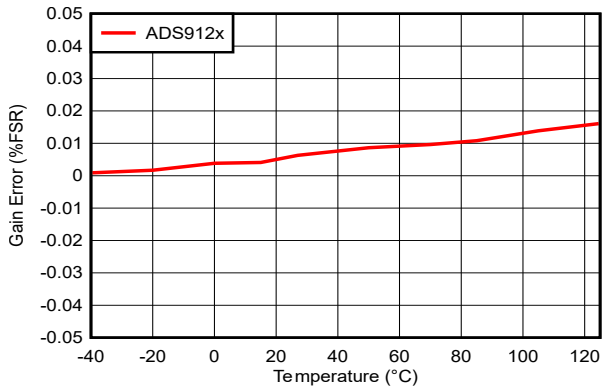

Figure 5-8. Gain Error vs Temperature

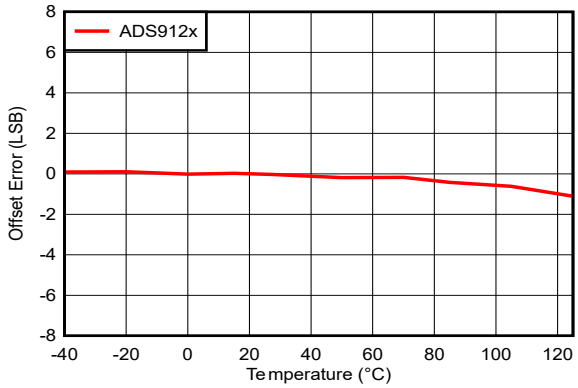

Figure 5-9. Offset Error vs Temperature

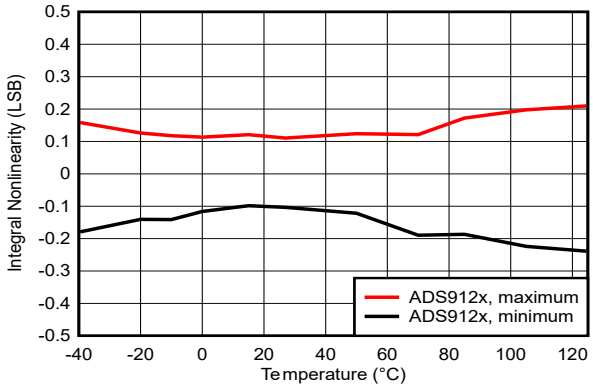

Figure 5-10. INL vs Temperature

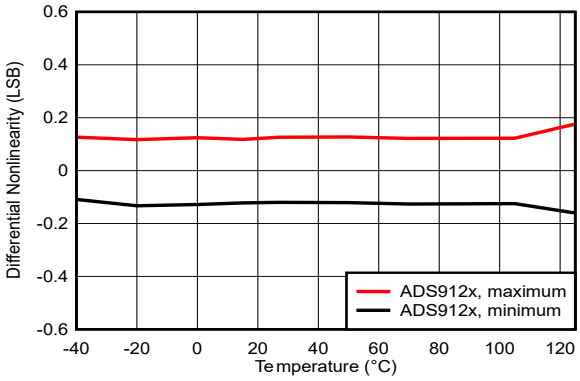

Figure 5-11. DNL vs Temperature

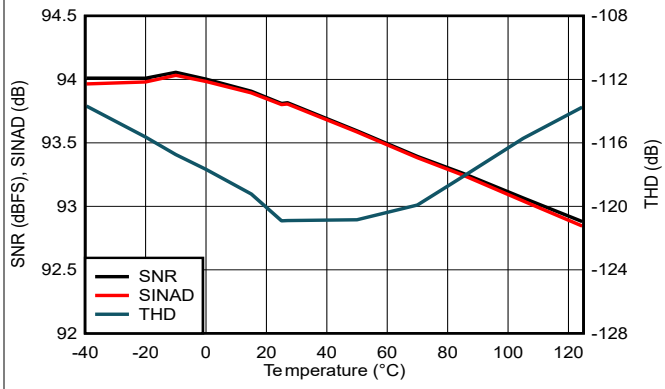

Figure 5-12. SNR, SINAD, and THD vs Temperature

5.9 Typical Characteristics: All Devices (continued)

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

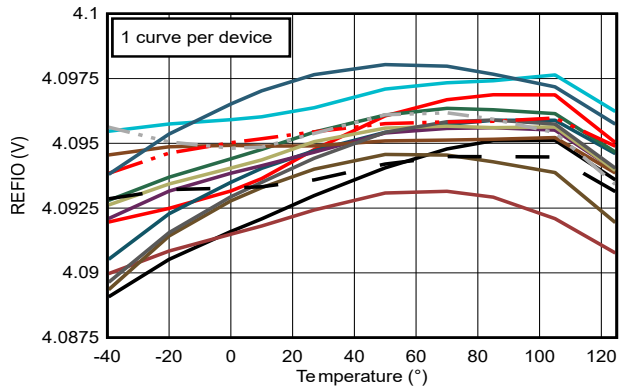

Figure 5-13. REFIO Voltage vs Temperature

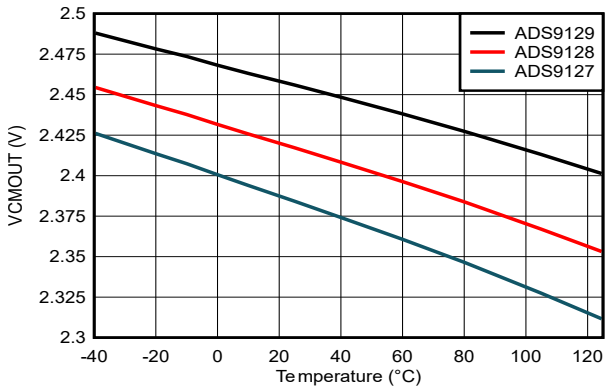

Figure 5-14. V_{CMOUT} Voltage vs Temperature

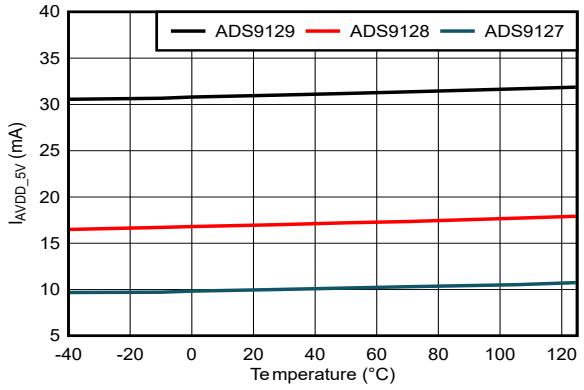

Figure 5-15. AVDD_5V Current vs Temperature

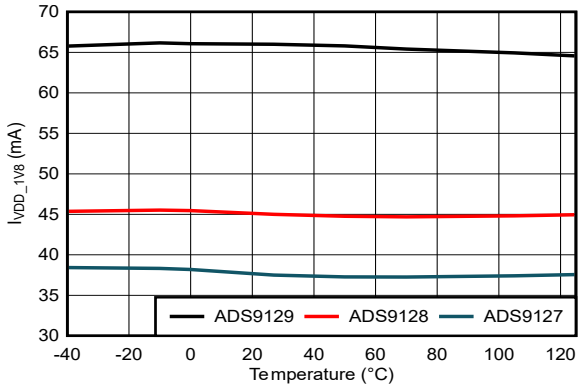

Figure 5-16. VDD_1V8 Current vs Temperature

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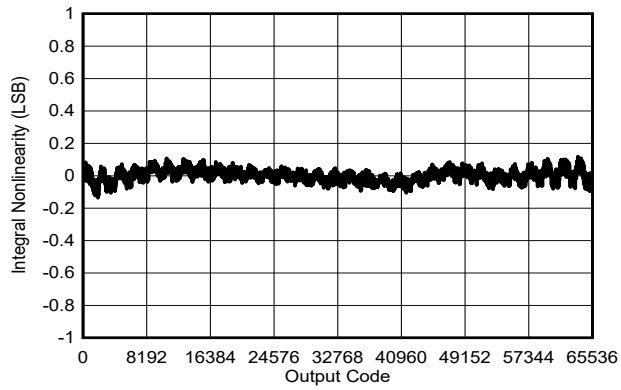
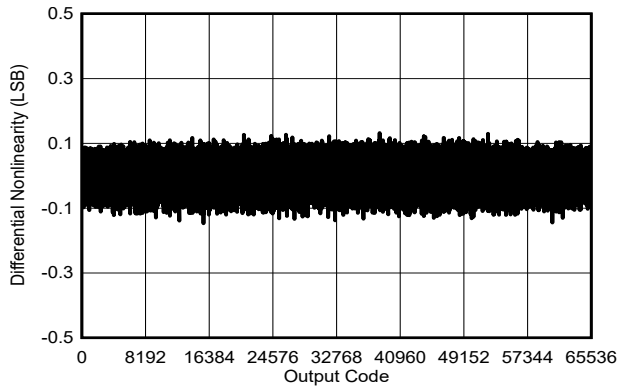
5.10 Typical Characteristics: ADS9129

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



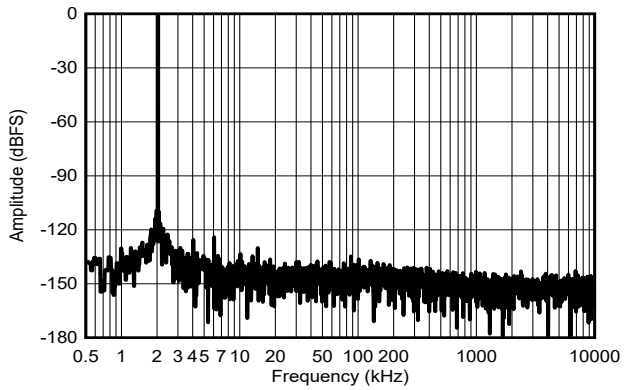
Typical INL = ±0.15LSB

Figure 5-17. Typical INL



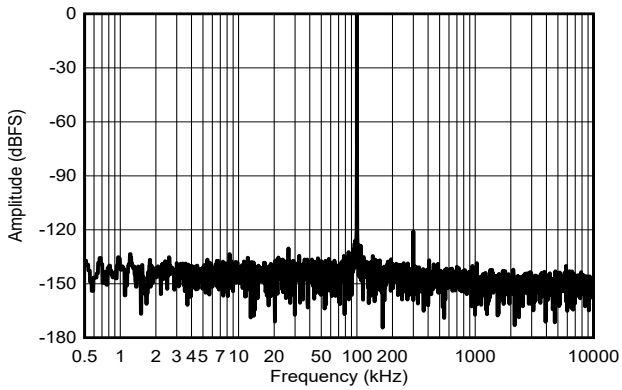
Typical DNL = ±0.15LSB

Figure 5-18. Typical DNL: ADS9129



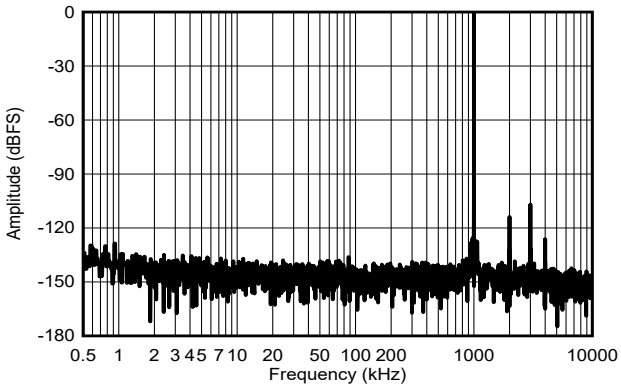
f_{IN} = 2kHz, SNR = 93.5dBFS, THD = –120dB

Figure 5-19. Typical FFT for f_{IN} = 2kHz



f_{IN} = 100kHz, SNR = 93.5dBFS, THD = –118dB

Figure 5-20. Typical FFT for f_{IN} = 100kHz

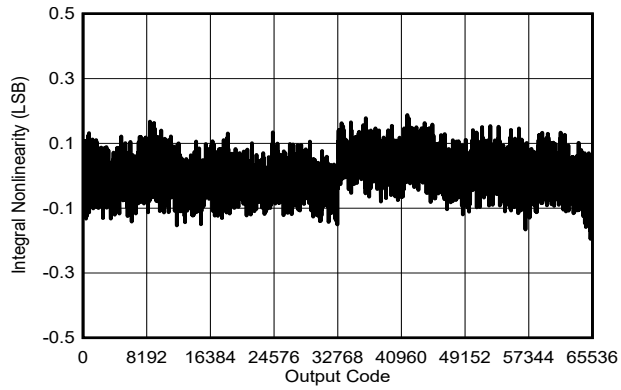


f_{IN} = 1MHz, SNR = 93.3dBFS, THD = –104.2dB

Figure 5-21. Typical FFT for f_{IN} = 1MHz

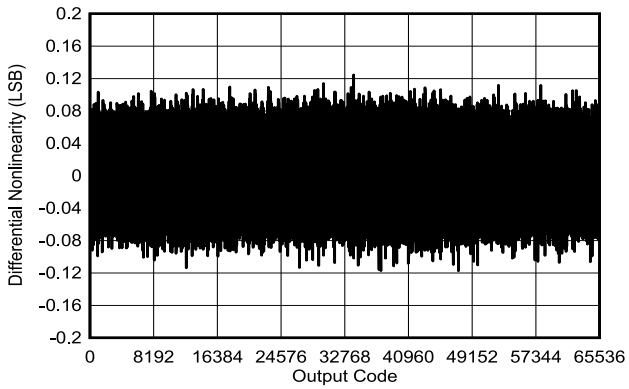
5.11 Typical Characteristics: ADS9128

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



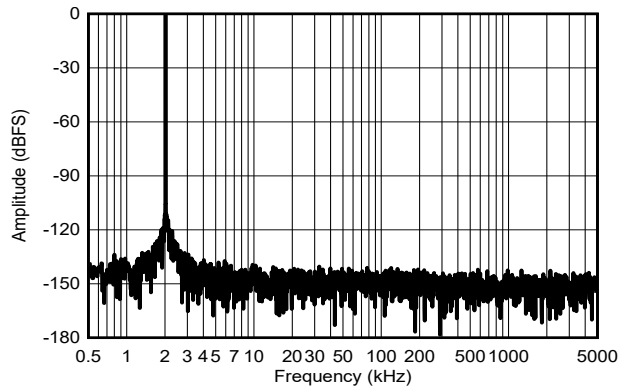
Typical INL = ±0.2LSB

Figure 5-22. Typical INL



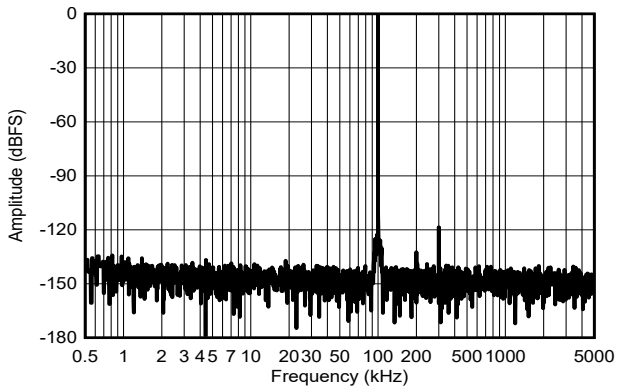
Typical DNL = ±0.15LSB

Figure 5-23. Typical DNL



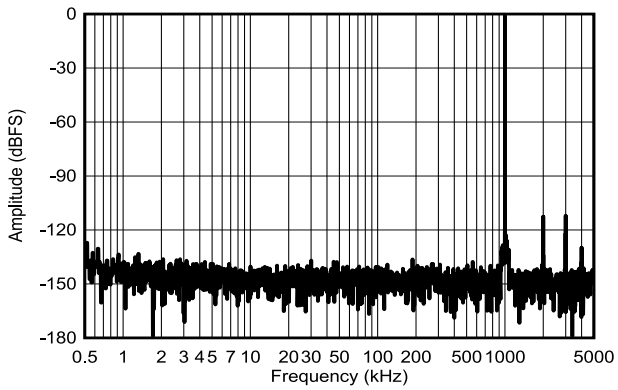
f_{IN} = 2kHz, SNR = 93.9dBFS, THD = –122dB

Figure 5-24. Typical FFT for f_{IN} = 2kHz



f_{IN} = 100kHz, SNR = 93.8dBFS, THD = –118dB

Figure 5-25. Typical FFT for f_{IN} = 100kHz



f_{IN} = 1MHz, SNR = 93.3dBFS, THD = –104dB

Figure 5-26. Typical FFT for f_{IN} = 1MHz

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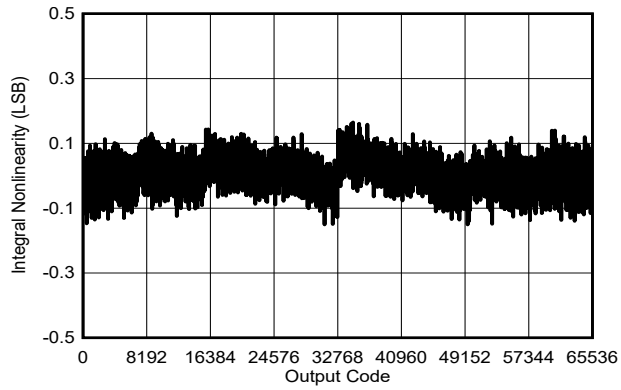
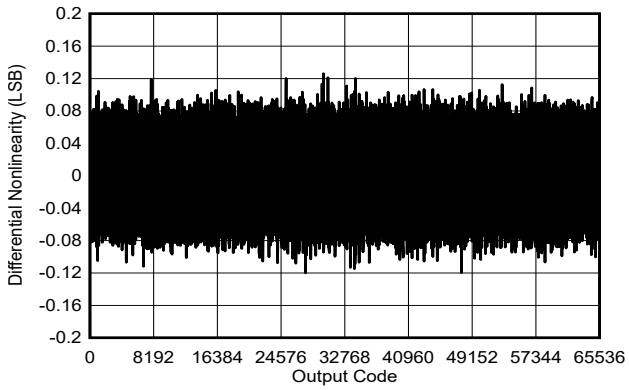
5.12 Typical Characteristics: ADS9127

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



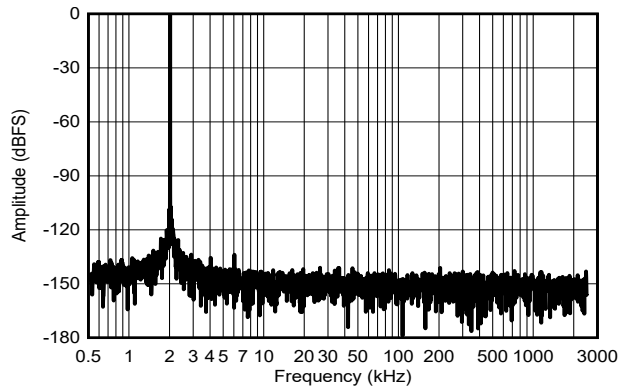
Typical INL = ±0.2LSB

Figure 5-27. Typical INL



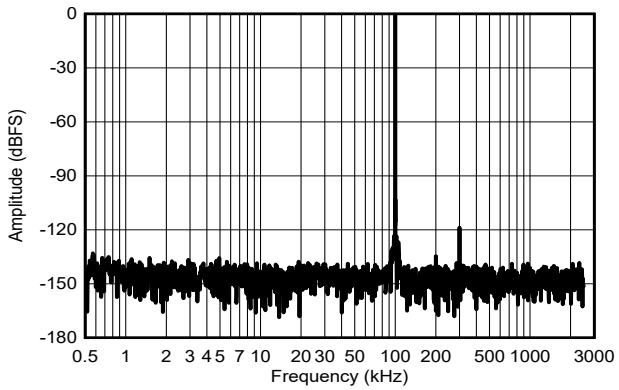
Typical DNL = ±0.15LSB

Figure 5-28. Typical DNL



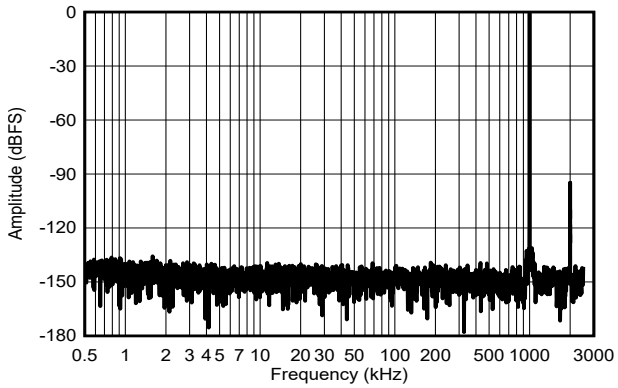
f_{IN} = 2kHz, SNR = 93.9dBFS, THD = –122.5dB

Figure 5-29. Typical FFT for f_{IN} = 2kHz



f_{IN} = 100kHz, SNR = 93.8dBFS, THD = –119dB

Figure 5-30. Typical FFT for f_{IN} = 100kHz



f_{IN} = 1MHz, SNR = 93.3dBFS, THD = –104.5dB

Figure 5-31. Typical FFT for f_{IN} = 1MHz

6 Detailed Description

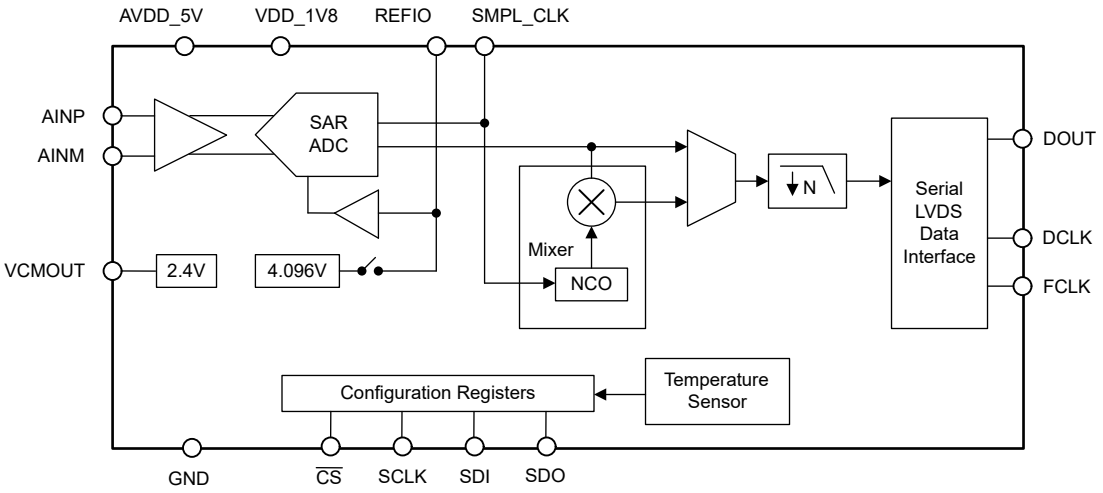
6.1 Overview

The ADS912x is 16-bit, 20MSPS analog-to-digital converter (ADC). The ADS912x integrates a high-impedance buffer at the ADC inputs, voltage reference, reference buffer, and common-mode voltage output buffer. The ADS9129 supports unipolar differential analog input signals. The buffer at the ADC inputs is optimized for low-distortion and low-power operation.

For DC level shifting of the analog input signals, the device has a common-mode voltage output buffer. The common-mode voltage is derived from the output of the integrated reference buffer. When a conversion is initiated, the differential input between the (AINP – AINM) pins is sampled. The ADS912x uses a clock input on the SMPL_CLKP pin to initiate conversions.

The ADS912x consumes only 274mW of power when operating at 20MSPS. This value includes the buffer power dissipation at the ADC inputs. The serial LVDS (SLVDS) digital interface simplifies board layout, timing, firmware, and supports full throughput at lower clock speeds.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Analog Inputs

The ADS912x supports both AC-coupled and DC-coupled differential analog inputs. Make sure the input common-mode voltage of the analog inputs matches the voltage level on the VCMOUT pin. Figure 6-1 shows the equivalent input network diagram of the device.

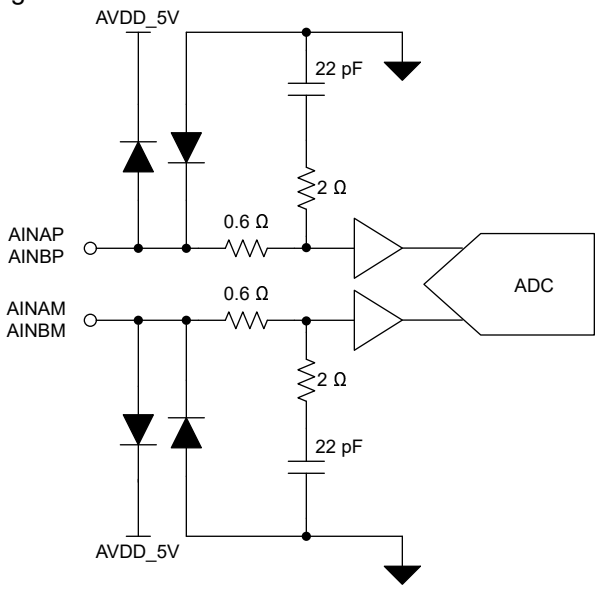

Figure 6-1. Equivalent Input Network

6.3.2 Analog Input Bandwidth

Figure 5-7 illustrates the analog full-power input bandwidth of the ADS912x. The –3dB bandwidth is 90MHz for the ADS9129 and ADS9128, and 45MHz for the ADS9127.

6.3.3 ADC Transfer Function

The ADS912x supports a ±3.2V differential input range. The device outputs 16-bit conversion data in either straight-binary or binary two's-complement format. As shown in Table 6-1, the format for the output codes is the same across all analog channels. Configure the format for the output codes with the DATA_FORMAT field in register address 0x0D. The least significant bit (LSB) for the ADC is given by 1LSB = 6.4V / 2^{16}.

Table 6-1. Transfer Characteristics

INPUT VOLTAGE	DESCRIPTION	ADC OUTPUT IN 2's-COMPLEMENT FORMAT	ADC OUTPUT IN STRAIGHT-BINARY FORMAT
≤ –3.2V + 1LSB	Negative full-scale code	0x8000	0x0000
0V + 1LSB	Mid-code	0x0000	0x7FFF
≥ 3.2V – 1LSB	Positive full-scale code	0x7FFF	0xFFFF

6.3.4 Reference Voltage

The ADS912x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise (as shown in Figure 6-2) by connecting a 10µF ceramic bypass capacitor to the REFIO pin. As shown in Figure 6-3, connect an external reference at the REFIO pin. When using an external reference, disable the internal reference voltage by writing PD_REF = 1b in address 0xC1 of register bank 1.

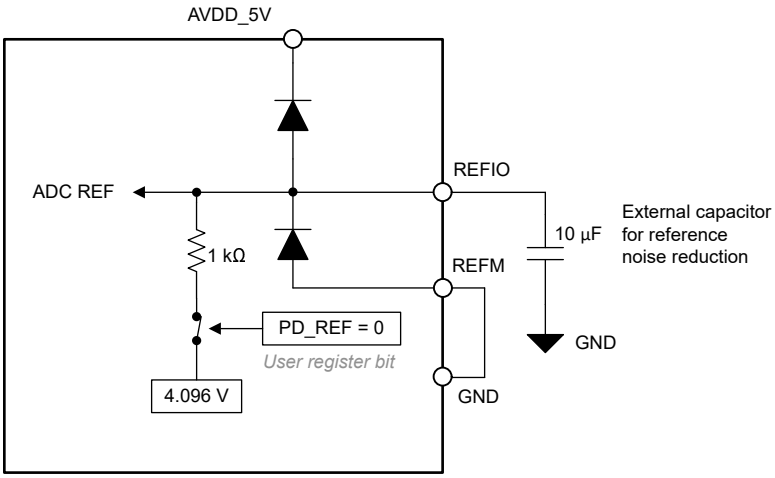

Figure 6-2. Internal Reference Voltage

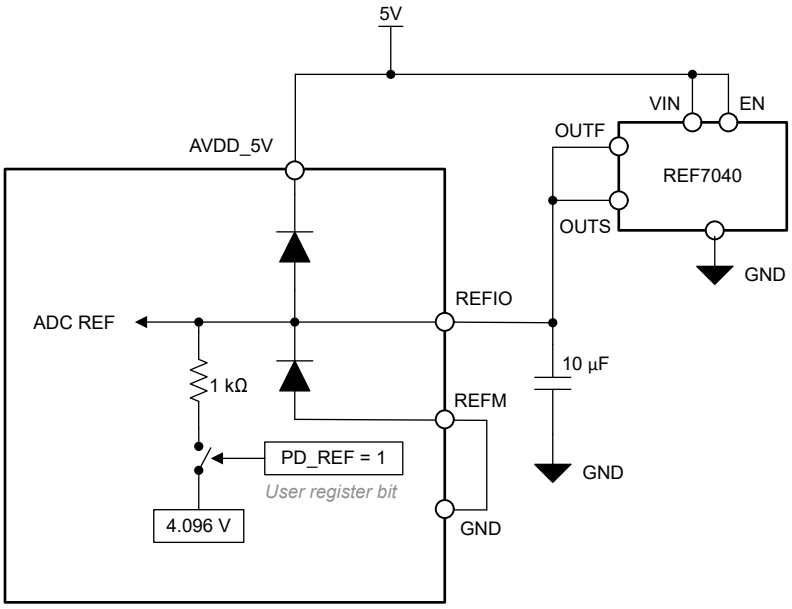

Figure 6-3. External Reference Voltage

6.3.5 Temperature Sensor

The ADS912x features a 10-bit temperature sensor for measuring temperature inside the device. Follow the sequence listed in Table 6-2 to read the temperature sensor output with the SPI. Read the temperature sensor data at anytime independent of the ADC data interface.

Equation 1 calculates the transfer function for the temperature sensor.

$$\text{Temperature} = -85.0172 + (10\text{ bit output} \times 0.24918)\ ^\circ\text{C} \quad (1)$$

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Table 6-2. Sequence to Read Temperature Sensor Output

REGISTER ADDRESS	REGISTER BANK	VALUE	COMMENT
0x90	1	0x4000	Write register to load temperature sensor output in address 0x91
0x91	1	10-bit temperature sensor data	Read register for temperature sensor output
0x90	1	0x0000	Write register

6.3.6 Data Averaging

The ADS912x features a built-in decimation filter that averages the conversion results from the ADC. The output data rate is reduced with higher data averaging. Table 6-3 shows the register settings corresponding to oversampling ratios.

As shown in Figure 6-4, a pulse on the SMPL_SYNC pin resets the decimation filter. A pulse on SMPL_SYNC synchronizes multiple ADS912x devices when using the decimation filter.

Table 6-3. Register Map Settings for OSR

DECIMATION	REGISTER	VALUE
OSR initialization	CLK3 (0xC5[9])	1
	OSR_INIT1 (0xC0[11:10])	1
	OSR_INIT2 (0xC4[5:4])	2
	OSR_INIT3 (0xC4[1])	1
	OSR_EN (0x0D[6])	1
2	OSR (0x0D[5:2])	0
	OSR_CLK (0xC0[9:7])	0
4	OSR (0x0D[5:2])	1
	OSR_CLK (0xC0[9:7])	4
8	OSR (0x0D[5:2])	2
	OSR_CLK (0xC0[9:7])	5
16	OSR (0x0D[5:2])	3
	OSR_CLK (0xC0[9:7])	6

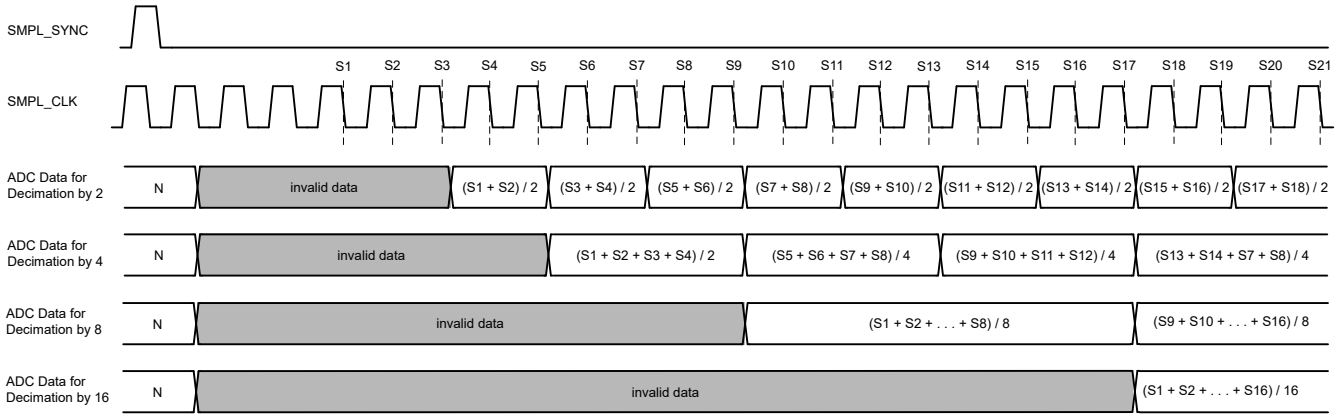

Figure 6-4. Data Output With Decimation

6.3.7 Digital Down Converter

The ADS912x includes an optional on-chip digital down conversion (DDC) that is enabled by SPI register settings. As shown in Figure 6-5, the DDC includes a digital mixer and a 24-bit, numerically controlled oscillator (NCO). The digital mixer generates 24-bit I and Q outputs that represent complex mixing of ADC output data with the NCO output frequency. The ADC generates a 48-bit output corresponding to the 24-bit I and Q outputs, respectively, from the digital mixer.

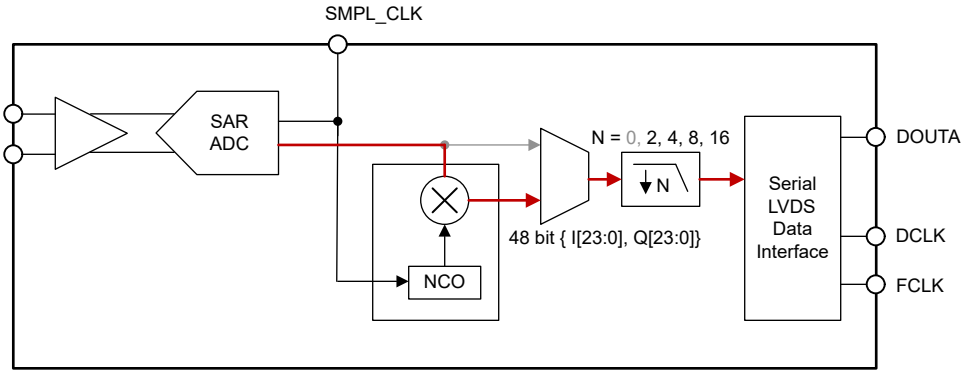

Figure 6-5. Data Path When Using a Digital Down Converter

The output frequency of the NCO, given by Equation 2, is configured using the NCO_FREQUENCY register (address 0xFD and 0xFE).

$$f_{NCO} = \frac{f_{SMPL_CLK}}{2^{24}} \times (\text{NCO_FREQUENCY}[23:0] \,\&\, 0\text{xFFFFF0})\ \text{Hz} \tag{2}$$

The output phase of the NCO is reset by applying a pulse on the SMPL_SYNC pin, see Figure 5-5. As shown in Equation 3 and Table 6-4, the initial phase of the NCO output is configured using the NCO_PHASE register (address 0xFC and 0xFD).

$$\text{NCO_PHASE}[23:0] = \left(\frac{\text{Initial phase}}{2\pi} \times 2^{24}\right) \& \ 0\text{xFFFFF0} \tag{3}$$

Table 6-4. Initial NCO Phase

NCO_PHASE[23:0]	INITIAL PHASE
0x000000	0
0x7FFFF0	π
0xFFFFF0	2π

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Use a decimation factor of either 2, 4, 8, or 16 with the DDC. Table 6-5 shows the register configuration for decimating the DDC output.

Table 6-5. Decimation Settings for the DDC

DECIMATION	REGISTER	VALUE
2	OSR_EN (0x0D[6])	1
	OSR (0x0D[5:2]	0
	OSR_CLK (0xC0[9:7])	0
Common settings for decimation factors 4, 8, and 16	CLK3 (0xC5[9])	1
	OSR_INIT1 (0xC0[11:10])	1
	OSR_INIT2 (0xC4[5:4])	2
	OSR_INIT3 (0xC4[1])	1
	OSR_EN (0x0D[6])	1
4	OSR (0x0D[5:2]	1
	OSR_CLK (0xC0[9:7])	0
8	OSR (0x0D[5:2]	2
	OSR_CLK (0xC0[9:7])	4
16	OSR (0x0D[5:2]	3
	OSR_CLK (0xC0[9:7])	5

6.3.8 Data Interface

The ADS912x features a high-speed, serial LVDS data interface with output data frame width to 20 bits or 24 bits with the single-data rate (SDR) and double-data rate (DDR) modes.

Configure the INIT_1 register field before writing to other register fields, as described in Table 6-6 and Table 6-7.

Table 6-6. Register Map Settings for Output Data Interface for the ADS9127

DATA FRAME WIDTH (Bits)	DATA RATE	INIT_1 0x04[3:0]	DATA_LANES 0x12[2:0]	DATA_RATE 0xC1[8]	CLK1 0xC0[12]	CLK2 0xC1[0]	CLK3 0xC5[9]	CLK4 0xC5[3:2]	CLK5 0xFB[1]	CLK6 0x1C[7:6]
20	SDR	0x000B	0	1	0	1	0	3	0	3
20	DDR	0x000B	0	0	0	1	0	3	0	3
24	SDR	0x0000	2	1	0	0	0	0	0	0
24	DDR	0x0000	2	0	0	0	0	0	0	0

Table 6-7. Register Map Settings for Output Data Interface for the ADS9129 and ADS9128

DATA FRAME WIDTH (Bits)	DATA RATE	INIT_1 0x04[3:0]	DATA_LANES 0x12[2:0]	DATA_RATE 0xC1[8]	CLK1 0xC0[12]	CLK2 0xC1[0]	CLK3 0xC5[9]	CLK4 0xC5[3:2]	CLK5 0xFB[1]	CLK6 0x1C[7:6]
20	SDR	—	Not supported							
20	DDR	—	Not supported							
24	SDR	—	2	1	0	0	0	0	0	0
24	DDR	—	2	0	0	0	0	0	0	0

The ADS912x generates a data clock DCLK that is a multiple of the ADC sampling clock SMPL_CLK. The data clock frequency depends on the data frame width and data rate. The data frame width is 20 or 24 bits and the data rate is SDR or DDR. The following equation calculates the DCLK speed. Table 6-8 lists the possible values for the output data clock frequency.

$$\text{DCLK speed} = \frac{\text{Data Frame Width (24 bit or 20 bit)}}{\text{Data Rate(SDR} = 1,\ \text{DDR} = 2)} \times \text{SMPL_CLK} \quad (4)$$

Table 6-8. Data Clock (DCLK) Speed

DATA FRAME WIDTH (Bits)	DATA RATE (1 = SDR, 2 = DDR)	SMPL_CLK MULTIPLIER	DCLK (SMPL_CLK = 5MHz)	DCLK (SMPL_CLK = 10MHz)	DCLK (SMPL_CLK = 20MHz)
24	1	24	120MHz	—	—
	2	12	60MHz	120MHz	240MHz
20	1	20	100MHz	—(1)	—(1)
	2	10	50MHz	—(1)	—(1)

(1) A 20-bit data frame width is not supported for the ADS9129 or ADS9128.

6.3.8.1 Data Frame Width

As shown in Figure 6-6, the ADS912x supports 24-bit and 20-bit data frame width options. Configure the DATA_WIDTH field in address 0x12 to select the data frame width. The default output data frame width is 24 bits. The ADC resolution is 18 bits, represented by 20 bits.

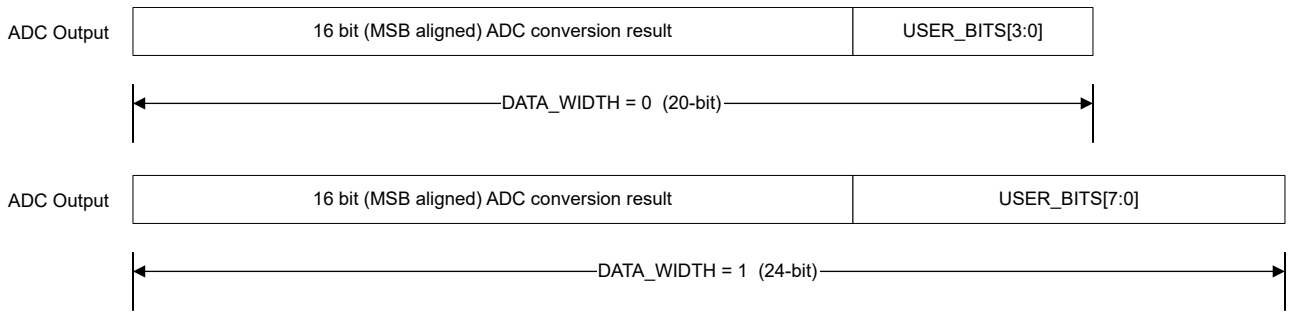

Figure 6-6. Data Frame Width Composition

6.3.8.2 Synchronizing Multiple ADCs

Drive the SMPL_CLK pins of the respective ADS912x devices with a common sampling clock. Match the timing delay on the clock path external to the ADCs by using identical PCB trace lengths for SMPL_CLK for the respective ADCs.

Use the SMPL_SYNC pin to synchronize multiple ADCs when using the internal decimation filter. The SMPL_SYNC pin is latched by the falling edge of the sampling clock. A pulse on SMPL_SYNC resets the internal decimation filter.

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6.3.8.3 Test Patterns for Data Interface

The ADS912x features test patterns (Figure 6-7) used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. Enable the test patterns by configuring the corresponding register addresses 0x13 through 0x16 in bank 1.

Table 6-9 lists the test patterns supported by the ADS912x.

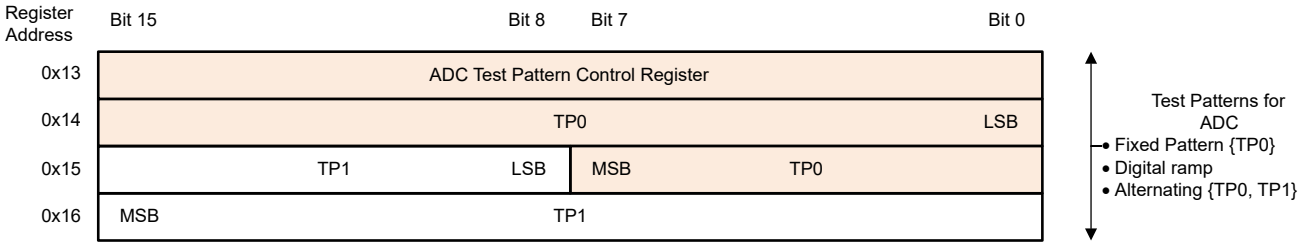

Figure 6-7. Register Bank for Test Patterns

Table 6-9. Test Pattern Configurations

ADC OUTPUT	TP_EN	TP_MODE	SECTION	RESULT
ADC conversion result	0			
Fixed pattern	1	0 or 1	*Fixed Pattern*	ADC output = TP0
Digital ramp	1	2	*Digital Ramp*	ADC output = Digital ramp
Alternating test patterns	1	3	*Alternating Test Pattern*	ADC output = TP0, TP1

6.3.8.3.1 Fixed Pattern

The ADC outputs fixed patterns defined in the TP0 register in place of the ADC data.

- Configure the test patterns in TP0
- Set TP_EN = 1 and TP_MODE = 0 (address = 0x13)

6.3.8.3.2 Alternating Test Pattern

The ADC outputs alternating test patterns defined in the TP0 and TP1 registers in place of the ADC data.

- Configure the test patterns in TP0 and TP1
- Set TP_EN = 1 and TP_MODE = 3 (address = 0x13)

6.3.8.3.3 Digital Ramp

The ADC outputs digital ramp values with increments specified in the RAMP_INC register in place of the ADC data.

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC (address = 0x13) register. The digital ramp increments by N + 1, where N is the value configured in the RAMP_INC register.
- Set TP_EN = 1 and TP_MODE = 2 (address = 0x13).

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6.3.9 ADC Sampling Clock Input

Use a low-jitter external clock with a high slew rate to maximize SNR performance. Operate the ADS912x with a differential or single-ended clock input. Clock amplitude impacts the ADC aperture jitter and, consequently, SNR. For maximum SNR performance, provide a clock signal with fast slew rates that maximizes swing between VDD_1V8 and GND levels.

Make sure the sampling clock is a free-running continuous clock. The ADC generates a valid output data, data clock, and frame clock $t_{PU_SMPL_CLK}$, as specified in the *Switching Characteristics* after a free-running sampling clock is applied. When the sampling clock is stopped, the ADC is in power-down and the output data, data clock, and frame clock are invalid.

Figure 6-8 shows a diagram of the differential sampling clock input. For this configuration, connect the differential sampling clock input to the SMPL_CLKP and SMPL_CLKM pins. Figure 6-9 shows a diagram of the single-ended sampling clock input. In this configuration, connect the single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

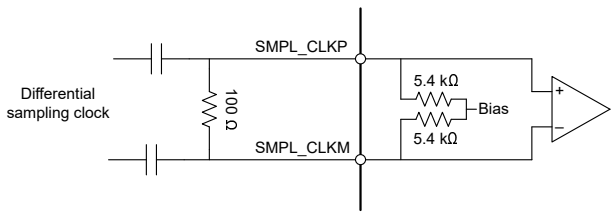

Figure 6-8. AC-Coupled Differential Sampling Clock

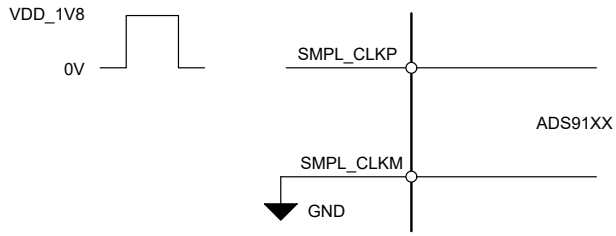

Figure 6-9. Single-Ended Sampling Clock

Figure 5-6 shows the latency from analog input sampling instant to corresponding data MSB output marked by the FCLK rising edge. The equations for data output latency depend on the output data frame width and are given in Table 6-10.

Table 6-10. Data Output Latency

DEVICE	24-BIT DATA FRAME	20-BIT DATA FRAME
ADS9129	$2 \times t_{SMPL_CLK} + t_{LAT}$	Not supported
ADS9128	$1.83 \times t_{SMPL_CLK} + t_{LAT}$	Not supported
ADS9127	$1.83 \times t_{SMPL_CLK} + t_{LAT}$	$2 \times t_{SMPL_CLK} + t_{LAT}$

1. For t_{LAT}, see the *Switching Characteristics* table.

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6.4 Device Functional Modes

6.4.1 Reset

Power down the ADS912x with a logic 0 on the $\overline{\text{RESET}}$ pin or write 1b to the RESET field (address 0x00, register bank 0). The device registers are initialized to the default values after reset. Initialize the device with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.2 Power-Down Options

Power down the ADS912x with a logic 0 on the $\overline{\text{PWDN}}$ pin or write 11b to the PD_CH field (address 0xC0, register bank 1). The device registers are initialized to the default values after power-up. Initialize the device with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.3 Normal Operation

In normal operating mode, the ADS912x powers up and digitizes the analog inputs at the sampling clock falling edge. The ADC outputs the data clock, frame clock, and MSB-aligned, 16-bit conversion result.

6.4.4 Initialization Sequence

The ADS912x register map is initialized with default values on power-up. Table 6-11 lists the steps to enable gain error calibration (recommended) and change the output data interface. For the ADS9129 only, follow the initialization steps in Table 6-12.

Table 6-11. User-Defined Configuration for the ADS9129, ADS9128, and ADS9127

STEP NUMBER	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	1	0x0D	User defined	Enable gain error calibration and select ADC output data format
2	1	0x33	0x2040	Enable gain error calibration
3	0	0x04	0x0000 for data frame width = 24 bits 0x000B for data frame width = 20	

Table 6-12. Initialization Configuration for the ADS9129 Only

STEP NUMBER	REGISTER		
	BANK	ADDRESS	VALUE[15:0]
1	1	0x0D [9:8]	0x3
2	1	0x34 [1]	0x1

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6.5 Programming

6.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 are selected for read or write operation by configuring the PAGE_SEL0 and PAGE_SEL1 bits, respectively. Registers in bank 0 are always accessible, irrespective of the PAGE_SELx bits. The register addresses in bank 0 are unique and are not used in register banks 1 and 2.

As shown in Figure 6-10, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

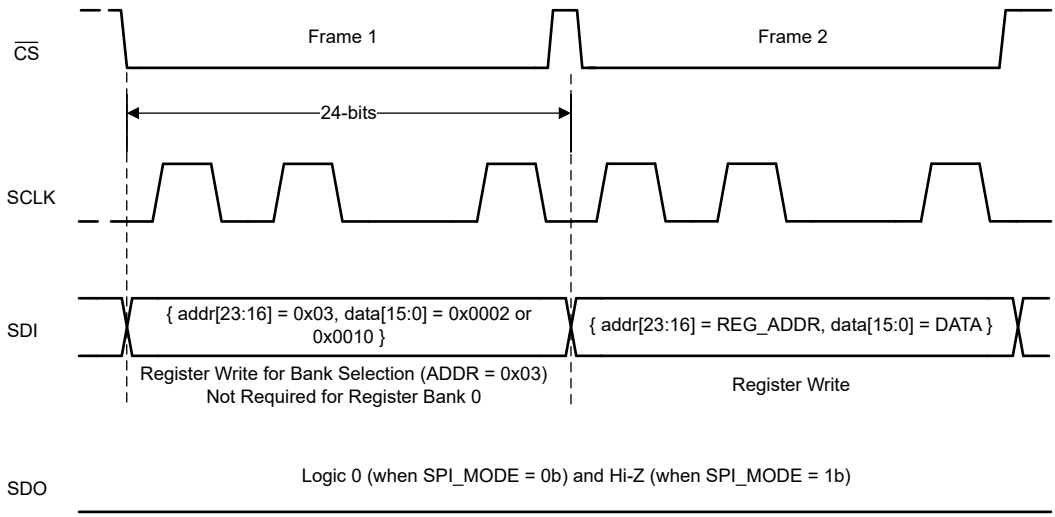

Figure 6-10. Register Write

6.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Set SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0 to enable register read access. As illustrated in Figure 6-11, read registers with two 24-bit SPI frames after setting SPI_RD_EN and SPI_MODE. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 6-11, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

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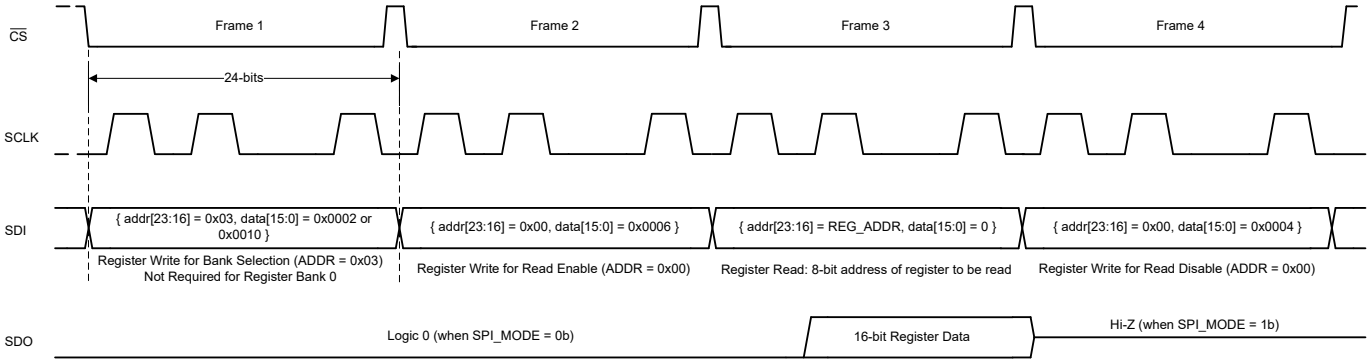

Figure 6-11. Register Read

6.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration

Figure 6-12 shows a typical connection diagram showing multiple devices in a daisy-chain topology.

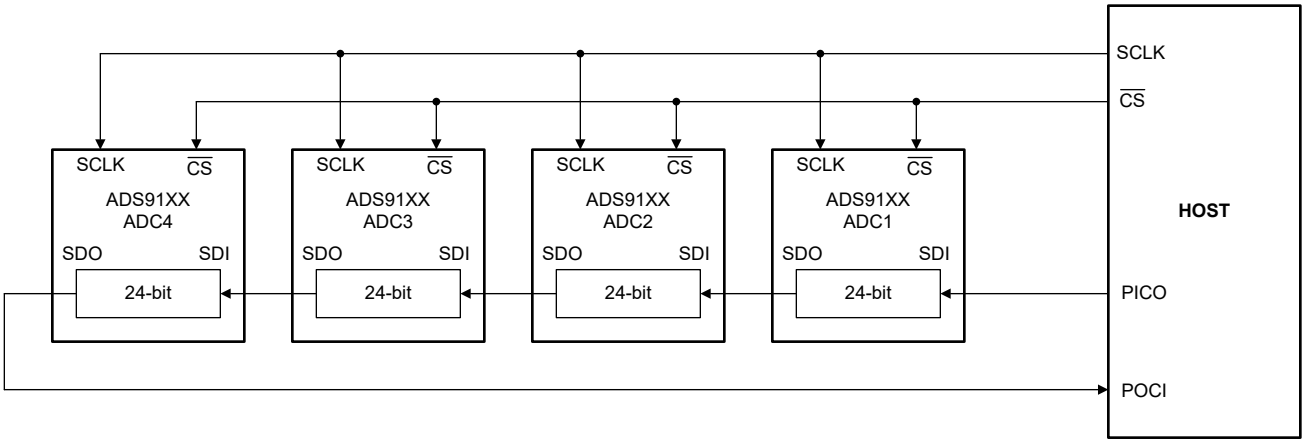

Figure 6-12. Daisy-Chain Connections for SPI Configuration

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller. The SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

Enable daisy-chain mode after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LENGTH register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain, excluding ADC1. In Figure 6-12, the DAISY_CHAIN_LENGTH is 3.

6.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain configuration requires N × 24 SCLKs in one SPI frame. Register writes in a daisy-chain configuration containing four ADCs, as illustrated in Figure 6-12, requires 96 SCLKs.

Daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LENGTH field to enable daisy-chain mode. Repeat the waveform in Figure 6-13 N times, where N is the number of ADCs in the daisy chain. Figure 6-14 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

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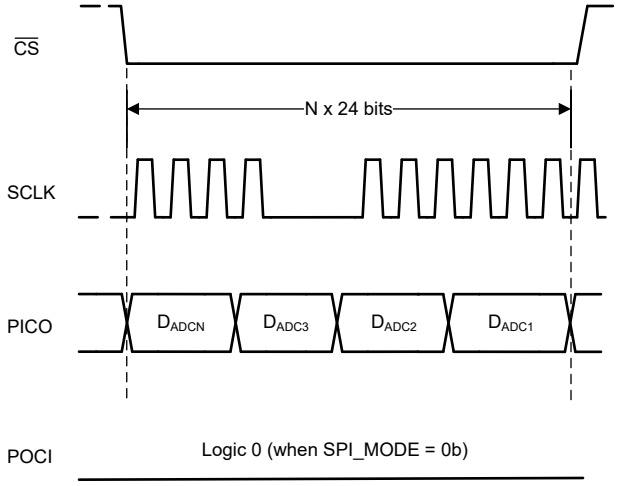

Figure 6-13. Register Write With Daisy-Chain

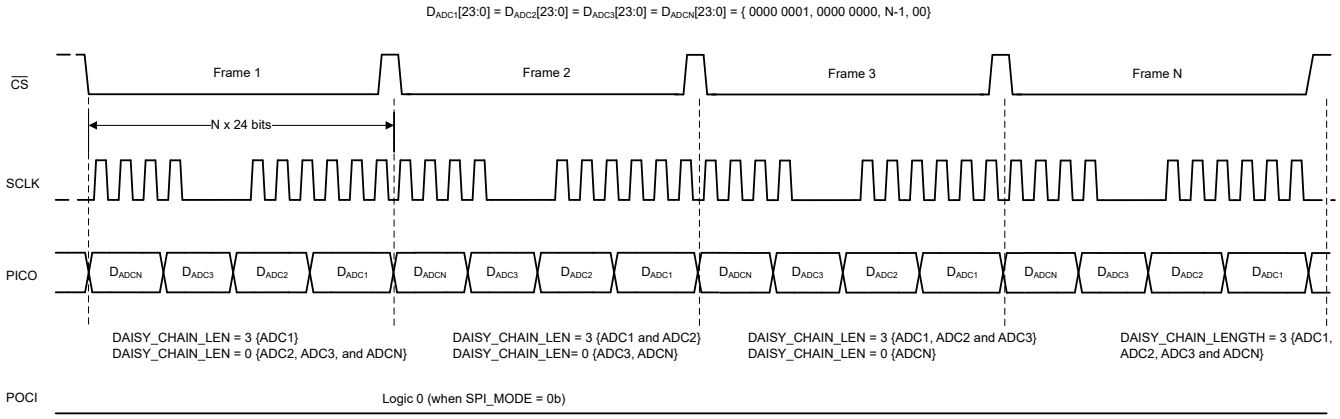

Figure 6-14. Register Write to Configure Daisy-Chain Length

6.5.3.2 Register Read With Daisy-Chain

Figure 6-15 illustrates an SPI waveform for reading registers in daisy-chain configuration. Steps for reading registers from N ADCs connected in a daisy-chain are:

1. Register read is enabled by writing to the following registers:
   a. Write to PAGE_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller reads register data by:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N times (0xFE, 0x00, 8-bit register address)
   b. N × 24-bit SPI frame to read out register data: N times (0xFF, 0xFF, 0xFF)

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

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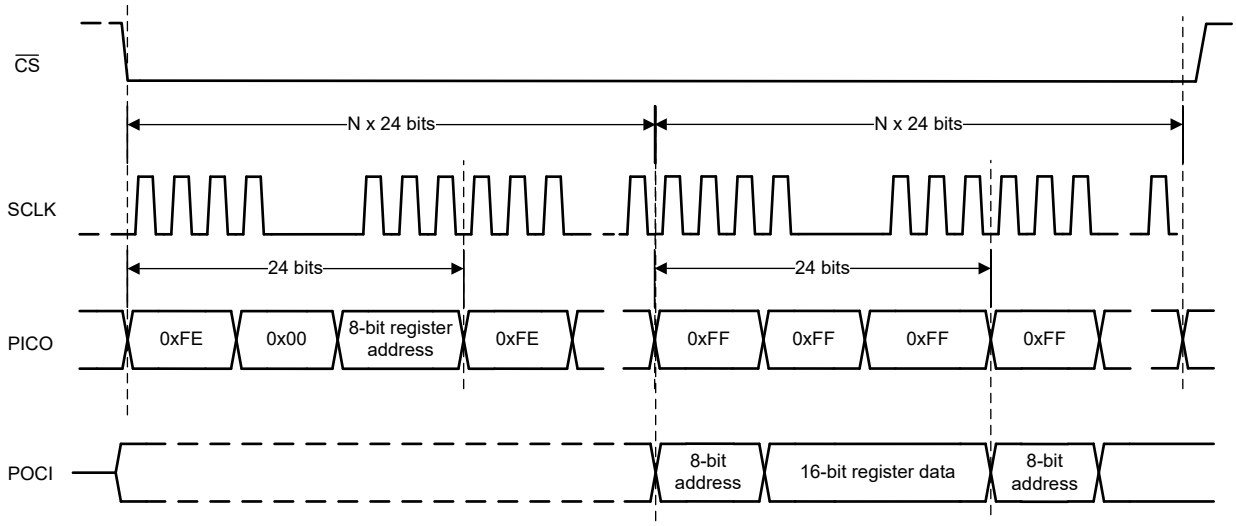

Figure 6-15. Register Read With Daisy-Chain Configuration

7 Register Map

7.1 Register Bank 0

Figure 7-1. Register Bank 0 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESERVED													SPI_MODE	SPI_RD_EN	RESET
01h	RESERVED									DAISY_CHAIN_LEN					RESERVED	
03h	RESERVED								REG_BANK_SEL							
04h	RESERVED												INIT_1			
06h	REG_00H_READBACK															

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.1.2 Register 00h (offset = 0h) [reset = 0h]

Figure 7-2. Register 00h

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED					SPI_MODE	SPI_RD_EN	RESET
W-0h					W-0h	W-0h	W-0h

Figure 7-3. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from the default reset value.
2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface to enable register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1	SPI_RD_EN	W	0h	Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode. 0 : Register read disabled 1 : Register read enabled
0	RESET	W	0h	ADC reset control. 0 : Normal device operation 1 : Resets the ADC and all registers

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7.1.3 Register 01h (offset = 1h) [reset = 0h]

Figure 7-4. Register 01h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	DAISY_CHAIN_LEN					RESERVED	
R/W-0h	R/W-0h					R/W-0h	

Figure 7-5. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-2	DAISY_CHAIN_LEN	R/W	0h	Configure the number of ADCs connected in daisy-chain for the SPI configuration. 0 : 1 ADC 1 : 2 ADCs 31 : 32 ADCs
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.1.4 Register 03h (offset = 3h) [reset = 2h]

Figure 7-6. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
REG_BANK_SEL							
R/W-2h							

Figure 7-7. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select register bank 0 2 : Select register bank 1 16 : Select register bank 2

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7.1.5 Register 04h (offset = 4h) [reset = 0h]

Figure 7-8. Register 04h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				INIT_1			
R/W-0h							

Figure 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
3-0	INIT_1	R/W	0h	INIT_1 field for device initialization. Write 1011b during the initialization sequence. See the *Data Interface* section for more details.

7.1.6 Register 06h (offset = 6h) [reset = 2h]

Figure 7-10. Register 06h

15	14	13	12	11	10	9	8
REG_00H_READBACK							
R-0h							
7	6	5	4	3	2	1	0
REG_00H_READBACK							
R-5h							

Figure 7-11. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	REG_00H_READ BACK	R	2h	This register is a copy of the register address 0x00 for readback. The register address 0x00 is write-only. The default readback value is 2h because SPI_RD_EN in address 0x00 is set to 1 for register reads.

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7.2 Register Bank 1

Figure 7-12. Register Bank 1 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	RESERVED		DATA_FORMAT	RESERVED			LAT_INC		GE_CAL_EN1	OSR_EN	OSR				RESERVED	
10h	RESERVED															HI_FREQ
12h	RESERVED												XOR_EN	DATA_LANES		
13h	RESERVED								RAMP_INC				TP_MODE		TP_EN	RESERVED
14h	TP0															
15h	TP1								TP0							
16h	TP1															
1Ch	RESERVED										USER_BITS_ADC_A					
33h	RESERVED		GE_CAL_EN3	RESERVED						GE_CAL_EN2	RESERVED					
34h	RESERVED											LAT_EN	RESERVED			
90h	RESERVED	TS_LD	RESERVED													
91h	RESERVED						TEMPERATURE_SENSOR									
C0h	RESERVED			CLK1	OSR_INIT1		OSR_CLK			RESERVED					PD_CH	
C1h	RESERVED				PD_REF	RESERVED		DATA_RATE	RESERVED							CLK2
C4h	RESERVED										OSR_INIT2		RESERVED		OSR_INIT3	PD_CHIP
C5h	RESERVED		HI_FREQ_EN	RESERVED			CLK3	RESERVED		RD_CLK		RESERVED	CLK4		RESERVED	
FBh	RESERVED												NCO_SYSREF	XOR_MODE	CLK5	MIXER_EN
FCh	NCO_PHASE_COUNT[15:0]															
FDh	NCO_FREQUENCY[7:0]								NCO_PHASE_COUNT[23:16]							
FEh	NCO_FREQUENCY[23:8]															

Table 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

Figure 7-13. Register 0Dh

15	14	13	12	11	10	9	8
RESERVED		DATA_FORMAT	RESERVED			LAT_INC	
R/W-0h		R/W-1h	R/W-0h			R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GE_CAL_EN1	OSR_EN	OSR				RESERVED	
R/W-0h	R/W-0h	R/W-0h				R/W-2h	

Figure 7-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	DATA_FORMAT	R/W	1h	Select data format for the ADC conversion result. 0 : Straight-binary format 1 : Two's-complement format
12-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-8	LAT_INC	R/W	0h	For the ADS9129, set this field to 11b for optimum INL performance.
7	GE_CAL_EN1	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled 1 : Gain error calibration enabled
6	OSR_EN	R/W	0h	Control for data averaging depth. 0 : Data averaging disabled 1 : Data averaging enabled
5-2	OSR	R/W	0h	Control for enabling data averaging. 0 : 2 samples averaged 1 : 4 samples averaged 2 : 8 samples averaged 3 : 16 samples averaged
1-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

7.2.2 Register 10h (offset = 10h) [reset = 0h]

Figure 7-15. Register 10h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RESERVED
R/W-0h							R/W-0h

Figure 7-16. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	HI_FREQ	R/W	0h	Analog input fast slew rate control 0: Normal slew rate. 1: Fast slew rate. Fast analog input control enabled. Recommended for input frequencies >2MHz. Also see the HI_FREQ_EN register bit.

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7.2.3 Register 12h (offset = 12h) [reset = 2h]

Figure 7-17. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				XOR_EN	DATA_LANES		
R/W-0h				R/W-0h	R/W-2h		

Figure 7-18. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	XOR_EN	R/W	0h	Enables XOR operation on ADC conversion result. 0 : XOR operation is disabled 1 : ADC conversion result is bit-wise XOR with the PRBS bit by default
2-0	DATA_LANES	R/W	2h	Selects the number of output data lanes and number of data bits per output lane. 0 : 20 bits per data output frame on DOUT. 2 : 24 bits per data output frame on DOUT.

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7.2.4 Register 13h (offset = 13h) [reset = 0h]

Figure 7-19. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC				TP_MODE		TP_EN	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-20. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TP_MODE	R/W	0h	Select digital test pattern for ADC. 0 : Fixed pattern from the TP0 register 1 : Fixed pattern from the TP0 register 2 : Digital ramp output 3 : Alternate fixed pattern output from the TP0 and TP1 registers
1	TP_EN	R/W	0h	Enable digital test pattern for data corresponding to ADC. 0 : Data output is the ADC conversion result 1 : Data output is the digital test pattern for ADC
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.5 Register 14h (offset = 14h) [reset = 0h]

Figure 7-21. Register 14h

15	14	13	12	11	10	9	8
TP0[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0[15:0]							
R/W-0h							

Figure 7-22. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP0[15:0]	R/W	0h	Lower 16 bits of test pattern 0

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7.2.6 Register 15h (offset = 15h) [reset = 0h]

Figure 7-23. Register 15h

15	14	13	12	11	10	9	8
TP1[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0[23:16]							
R/W-0h							

Figure 7-24. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TP1[7:0]	R/W	0h	Lower eight bits of test pattern 1
7-0	TP0[23:16]	R/W	0h	Upper eight bits of test pattern 0

7.2.7 Register 16h (offset = 16h) [reset = 0h]

Figure 7-25. Register 16h

15	14	13	12	11	10	9	8
TP1[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TP1[23:8]							
R/W-0h							

Figure 7-26. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP1[23:8]	R/W	0h	Upper 16 bits of test pattern 1

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7.2.8 Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-27. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		USER_BITS_ADC_A					
R/W-0h		R/W-0h					

Figure 7-28. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
5-0	USER_BITS	R/W	0h	User-defined bits appended to the ADC conversion result.

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7.2.9 Register 33h (offset = 33h) [reset = 0h]

Figure 7-29. Register 33h

15	14	13	12	11	10	9	8
RESERVED		GE_CAL_EN3	RESERVED				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	GE_CAL_EN2	RESERVED					
R/W-0h	R/W-0h	R/W-0h					

Figure 7-30. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	GE_CAL_EN3	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
12-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6	GE_CAL_EN2	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
5-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.10 Register 34h (offset = 34h) [reset = 0h]

Figure 7-31. Register 34h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			LAT_EN	RESERVED			
R/W-0h			R/W-0h	R/W-0h			

Figure 7-32. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
4	LAT_EN	R/W	0h	For the ADS9129, set this field to 11b for optimum INL performance.
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.11 Register 90h (offset = 90h) [reset = 0h]

Figure 7-33. Register 90h

15	14	13	12	11	10	9	8
RESERVED	TS_LD	RESERVED					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Figure 7-34. Register 90h Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
14	TS_LD	R/W	0h	Trigger to load the temperature sensor output in address 0x91. Transition from 0 to 1 if this bit triggers the data load operation.
13-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.12 Register 91h (offset = 91h) [reset = 00h]

Figure 7-35. Register 91h

15	14	13	12	11	10	9	8
RESERVED						TEMPERATURE_SENSOR	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
TEMPERATURE_SENSOR							
R/W-0h							

Figure 7-36. Register 91h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-0	TEMPERATURE_SENSOR	R/W	0h	10-bit temperature sensor output. See the *Temperature Sensor* section.

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7.2.13 Register C0h (offset = C0h) [reset = 0h]

Figure 7-37. Register C0h

15	14	13	12	11	10	9	8
RESERVED			CLK1	OSR_INIT1		OSR_CLK	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OSR_CLK	RESERVED					PD_CH	
R/W-0h	R/W-0h					R/W-0h	

Figure 7-38. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
12	CLK1	R/W	0h	Selects the clock configuration based on output data lanes. See the *Data Interface* section for more details. 0 : Configuration for DATA_LANES = 0 or 2 1 : Not recommended
11-10	OSR_INIT1	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
9-7	OSR_CLK	R/W	0h	Data output clock configuration for data averaging. See Table 6-3 for more details.
6-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1-0	PD_CH	R/W	0h	Power-down control for the analog input channels. 0 : Normal operation 1 : ADC powered down 2 : No effect 3 : ADC powered down

7.2.14 Register C1h (offset = C1h) [reset = 0h]

Figure 7-39. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED		DATA_RATE
R/W-0h				R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CLK2
R/W-0h							R/W-0h

Figure 7-40. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	PD_REF	R/W	0h	ADC reference voltage source selection. 0 : Internal reference enabled. 1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin.
10-9	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double data rate (DDR) 1 : Single data rate (SDR)
7-1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	CLK2	R/W	0h	Select data rate for the data interface. See the *Data Interface* section for more details. 0 : Configuration for DATA_LANES = 2 or 7

7.2.15 Register C4h (offset = C4h) [reset = 0h]

Figure 7-41. Register C4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		OSR_INIT2		RESERVED		OSR_INIT3	PD_CHIP
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h

Figure 7-42. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
5-4	OSR_INIT2	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 2 : Configuration for enabling data averaging
3-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	OSR_INIT3	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
0	PD_CHIP	R/W	0h	Full chip power-down control. 0 : Normal device operation 1 : Full device powered down

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7.2.16 Register C5h (offset = C5h) [reset = 0h]

Figure 7-43. Register C5h

15	14	13	12	11	10	9	8
RESERVED		HI_FREQ_EN	RESERVED			CLK3	RESERVED
R/W-0h		R/W-0h	R/W-0h			R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RESERVED	RD_CLK		RESERVED	CLK4		RESERVED	
R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h	

Figure 7-44. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	HI_FREQ_EN	R/W	0h	Fast analog input slew rate enable. 0: Normal slew rate, 1: Fast analog input control enabled. Recommended for input frequencies >2MHz. Also see the HI_FREQ register bit.
12-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	CLK3	R/W	0h	Select data rate for the data interface. See the *Data Interface* section for more details. 0 : Configuration for DATA_LANES = 0 or 2
8 - 7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-5	RD_CLK	R/W	0h	Data output clock control for data averaging. See the *Data Averaging* section for more details.
4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3 - 2	CLK4	R/W	0h	Clock configuration for ADS9127. See the *Data Interface* section for details. Not applicable for the ADS9129 and ADS9128. 0 : 24-bit mode 3 : All other modes
1 - 0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

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7.2.17 Register FBh (offset = FBh) [reset = 0h]

Figure 7-45. Register FBh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				NCO_SYSREF	XOR_MODE	CLK5	MIXER_EN
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 7-46. Register FBh Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	NCO_SYSREF	R/W	0h	Set to 1b when applying periodic pulses on the SMPL_SYNC pin. 0: Synchronize the NCO with one pulse on the SMPL_SYNC pin. 1: Synchronize the NCO with the first pulse on the SMPL_SYNC pin when using periodic pulses.
2	XOR_MODE	R/W	0h	Selects the bit with which the ADC output data is XORed when XOR output mode is enabled. 0 : The PRBS bit is output after the ADC LSB. ADC output data are XORed with the PRBS bit. 1 : ADC output data are XORed with the LSB of the conversion result.
1	CLK5	R/W	0h	Clock configuration for the ADS9129 and ADS9128. See the *Data Interface* section for details. Not applicable for the ADS9127. 0 : 24-bit SDR and DDR modes 1 : Not recommended
0	MIXER_EN	R/W	0h	0: Digital down converter disabled 1: Digital down converter enabled

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7.2.18 Register FCh (offset = FCh) [reset = 0h]

Figure 7-47. Register FCh

15	14	13	12	11	10	9	8
NCO_PHASE_COUNT							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_PHASE_COUNT							
R/W-0h							

Figure 7-48. Register FCh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_PHASE_COUNT[15:0]	R/W	0h	Lower 15 bits of the NCO phase count. See the *Digital Down Converter* section.

7.2.19 Register FDh (offset = FDh) [reset = 0h]

Figure 7-49. Register FDh

15	14	13	12	11	10	9	8
NCO_FREQUENCY							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_PHASE_COUNT							
R/W-0h							

Figure 7-50. Register FDh Field Descriptions

Bit	Field	Type	Reset	Description
15-8	NCO_FREQUENCY[7:0]	R/W	0h	Lower eight bits of the NCO phase count. See the *Digital Down Converter* section.
7-0	NCO_PHASE_COUNT[23:16]	R/W	0h	Upper eight bits of the NCO phase count. See the *Digital Down Converter* section.

7.2.20 Register FEh (offset = FEh) [reset = 0h]

Figure 7-51. Register FEh

15	14	13	12	11	10	9	8
NCO_FREQUENCY							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_FREQUENCY							
R/W-0h							

Figure 7-52. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_FREQUENCY	R/W	0h	Upper 16 bits of the NCO phase count. See the *Digital Down Converter* section.

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7.3 Register Bank 2

Figure 7-53. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	RESERVED								CLK6		RESERVED					

Table 7-3. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-54. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
CLK6		RESERVED					
R/W-0h		R/W-0h					

Figure 7-55. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-6	CLK6	R/W	0h	Clock configuration for ADS9127. See the *Data Interface* section for details. Not applicable for the ADS9129 and ADS9128. 0 : 24-bit 2-lane mode 3 : All other modes
5-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADS912x features an integrated ADC driver, low latency, high speed, low AC and DC errors, and low temperature drift. These features make the ADS912x a high-performance signal-chain for applications requiring precision measurements with low latency. The following section provides example circuits and recommendations for using the ADS912x device family in a data acquisition (DAQ) system.

8.2 Typical Applications

8.2.1 Data Acquisition (DAQ) Circuit for a ≤20kHz Input Signal Bandwidth

Figure 8-1 shows a signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS912x with the fully differential amplifier (FDA) THS4551.

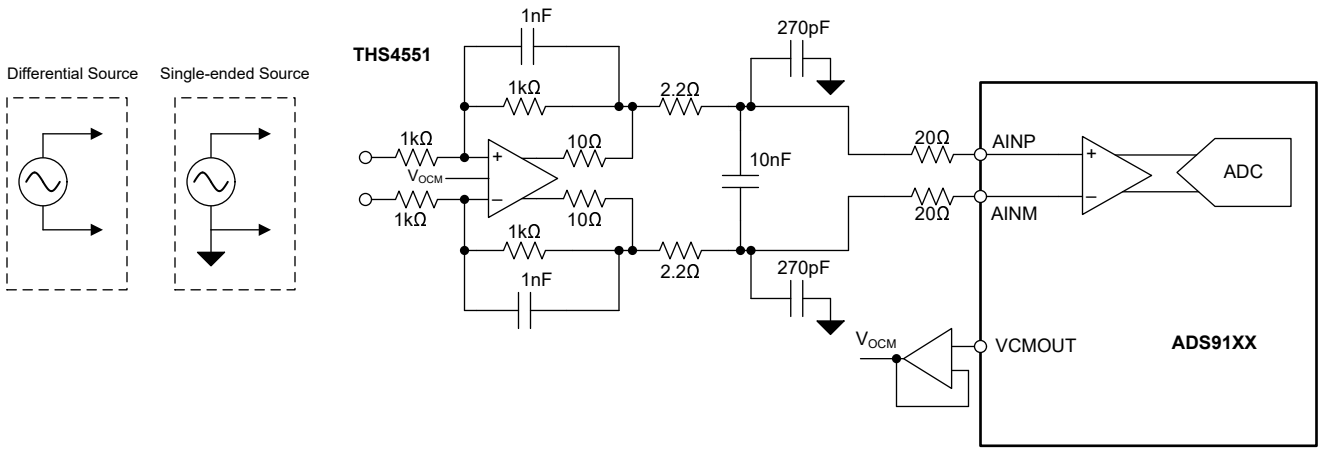

Figure 8-1. Data Acquisition (DAQ) Circuit for a ≤20kHz Input Signal Bandwidth

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Parameters

PARAMETER	VALUE
SNR	≥ 92dB
THD	≤ –110dB
Input signal frequency	≤ 20kHz

8.2.1.2 Detailed Design Procedure

Use the procedure discussed in this section for any ADS912x application circuit.

- All ADS912x applications require supply decoupling, as provided in the *Power Supply Recommendations* section.
- Make sure the values provided in the *Typical Applications* section meet the maximum throughput and input signal frequency design requirements. Use a lower bandwidth signal chain when lower noise performance is required.

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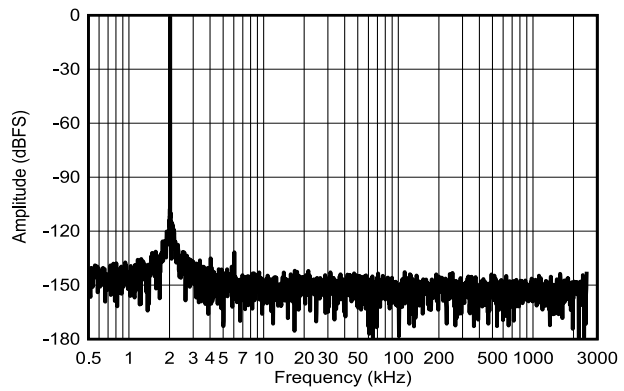
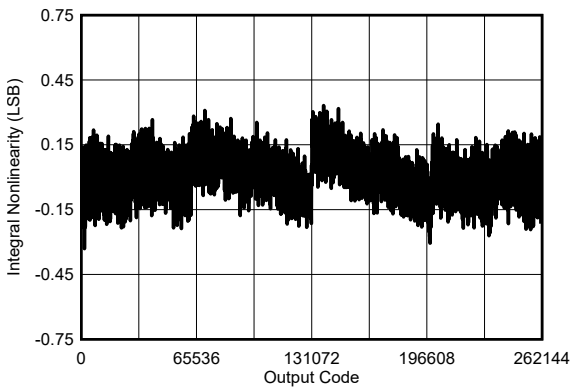
8.2.1.3 Application Curves

Figure 8-2 and Figure 8-3 show the SNR and INL performance for the circuit in Figure 8-1, respectively.



f_{IN} = 2kHz, SNR = 93.8dBFS, THD = –130dB

Figure 8-2. Typical FFT at 5MSPS: ADS9127



f_{IN} = 2kHz, INL = ±0.5LSB

Figure 8-3. Typical INL at 5MSPS: ADS9127

8.2.2 Data Acquisition (DAQ) Circuit for a ≤100kHz Input Signal Bandwidth

Figure 8-4 shows a signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS912x with the fully differential amplifier (FDA) THS4551.

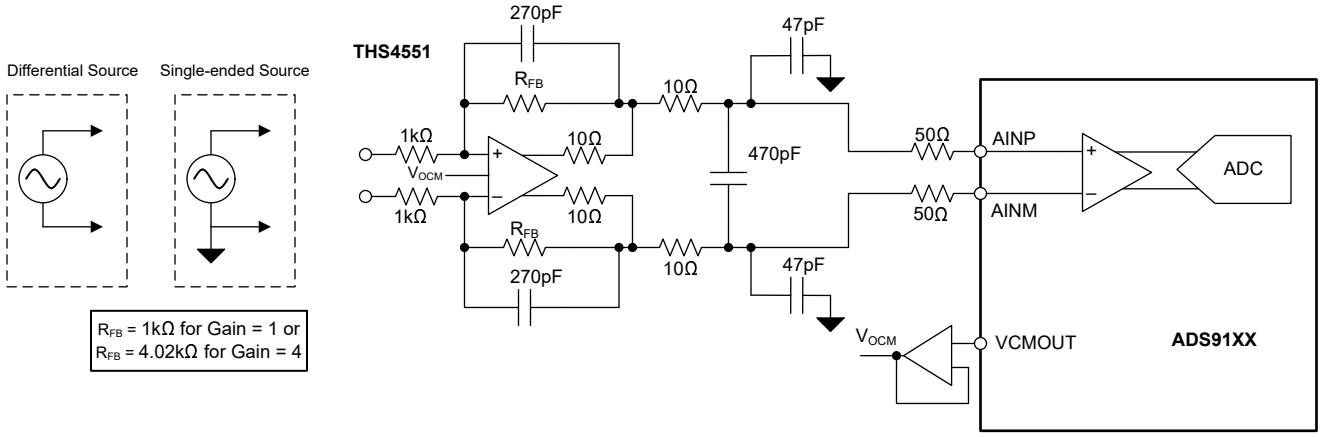


Figure 8-4. Data Acquisition (DAQ) Circuit for a ≤100kHz Input Signal Bandwidth

8.2.2.1 Design Requirements

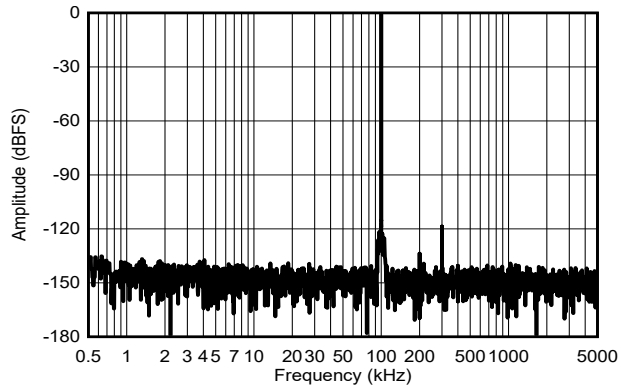
Table 8-2 lists the parameters for this typical application.

Table 8-2. Design Parameters

PARAMETER	VALUE
SNR	≥ 91dB
THD	≤ –110dB
Input signal frequency	≤ 100kHz

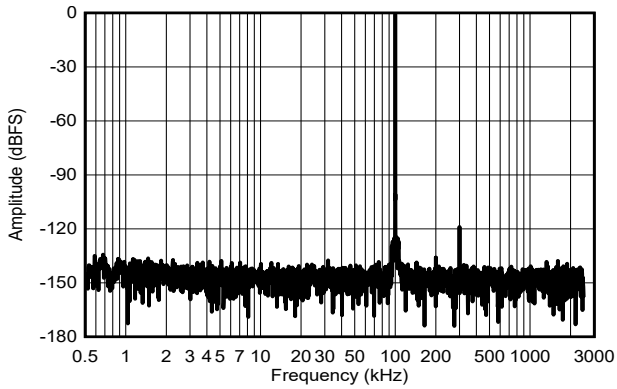
8.2.2.2 Application Curves

Figure 8-5 and Figure 8-6 show the FFT plots for the circuit in Figure 8-4.



f_{IN} = 100kHz, SNR = 93.8dBFS, THD = –118.2dB

Figure 8-5. Typical FFT at 10MSPS: ADS9128



f_{IN} = 100kHz, SNR = 93.6dBFS, THD = –120dB

Figure 8-6. Typical FFT at 5MSPS: ADS9127

8.2.3 Data Acquisition (DAQ) Circuit for a ≤1MHz Input Signal Bandwidth

Figure 8-7 shows a solution with minimum external components. This signal-chain significantly reduces signal-chain size by driving the ADS9129 with the THS4541, which enables low-distortion performance with low power over wide signal bandwidth.

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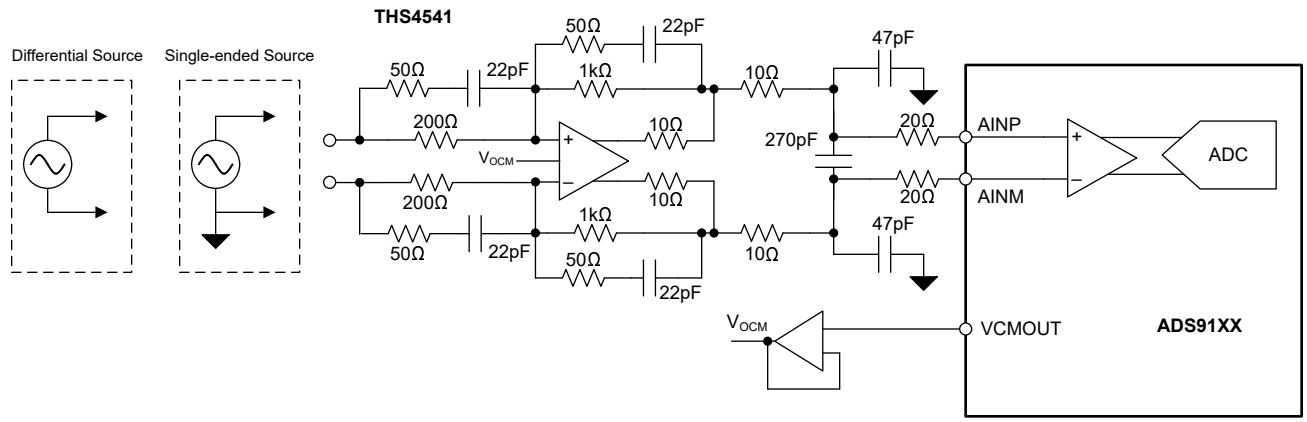


Figure 8-7. Data Acquisition (DAQ) Circuit for a ≤1MHz Input Signal Bandwidth

8.2.3.1 Design Requirements

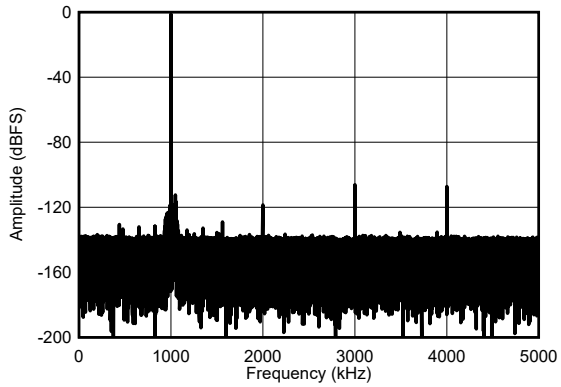
Table 8-3 lists the parameters for this typical application.

Table 8-3. Design Parameters

PARAMETER	VALUE
SNR	≥ 80dB
THD	≤ –100dB
Input signal frequency	≤ 1MHz

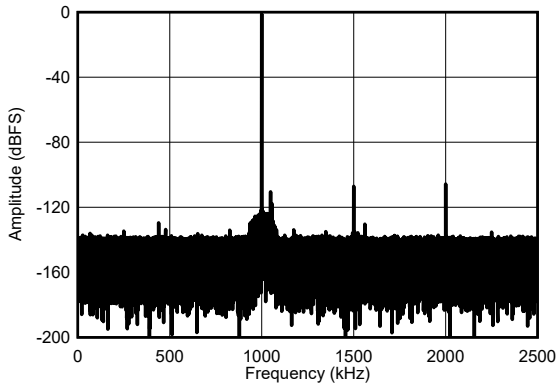
8.2.3.2 Application Curves

Figure 8-8 and Figure 8-9 show the FFT plots for the circuit in Figure 8-7.



f_{IN} = 1MHz, SNR = 93.2dB, THD = –104dB

Figure 8-8. Typical FFT at 10MSPS: ADS9128



f_{IN} = 1MHz, SNR = 93.3dB, THD = –104.2dB

Figure 8-9. Typical FFT at 5MSPS: ADS9127

8.3 Power Supply Recommendations

The ADS912x has two independent power supplies, AVDD_5V and VDD_1V8. The AVDD_5V supply provides power to the ADC driver. The VDD_1V8 supply provides power to the analog circuits and the digital interface. Set the AVDD_5 and VDD_1V8 supplies independently to voltages within the permissible range. Figure 8-10 shows how to decouple the power supplies.

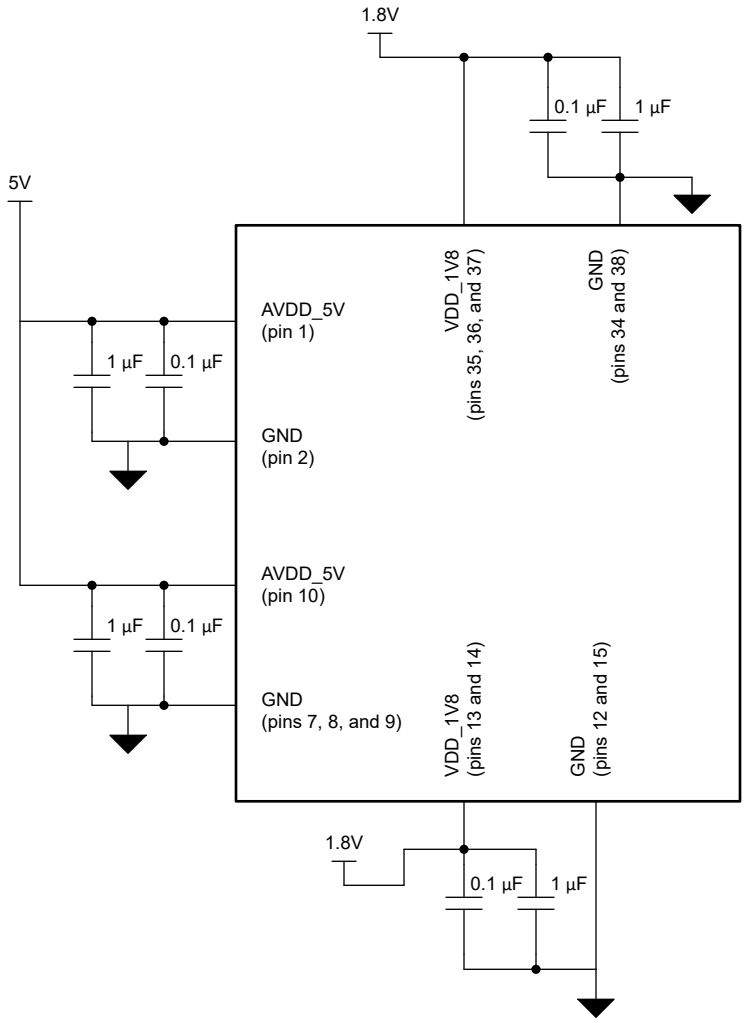


Figure 8-10. Power-Supply Decoupling

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8.4 Layout

8.4.1 Layout Guidelines

Figure 8-11 shows a board layout example for the ADS912x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 0.1µF ceramic bypass capacitors in close proximity to the analog (AVDD_5V and VDD_1V8) and digital (VDD_1V8) power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors. Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

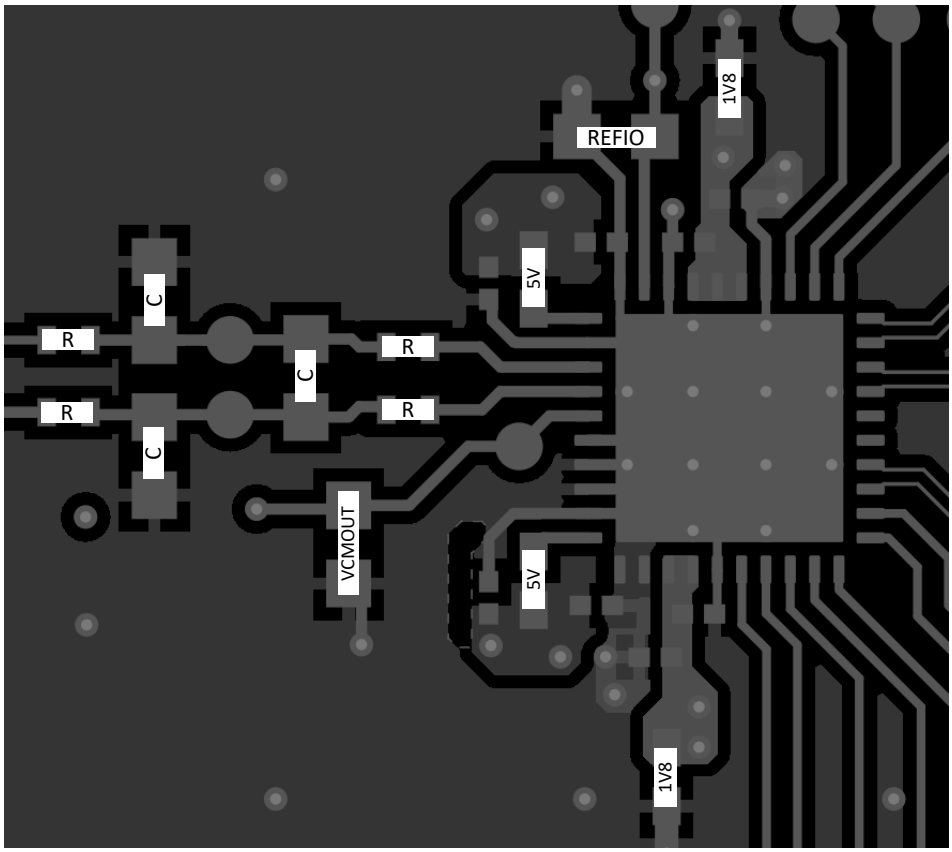

Figure 8-11. Example Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *REF70 2 ppm/°C Maximum Drift, 0.23 ppm$_{p-p}$ 1/f Noise, Precision Voltage Reference* data sheet
- Texas Instruments, *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier* data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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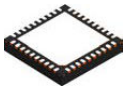
11.1 Mechanical Data

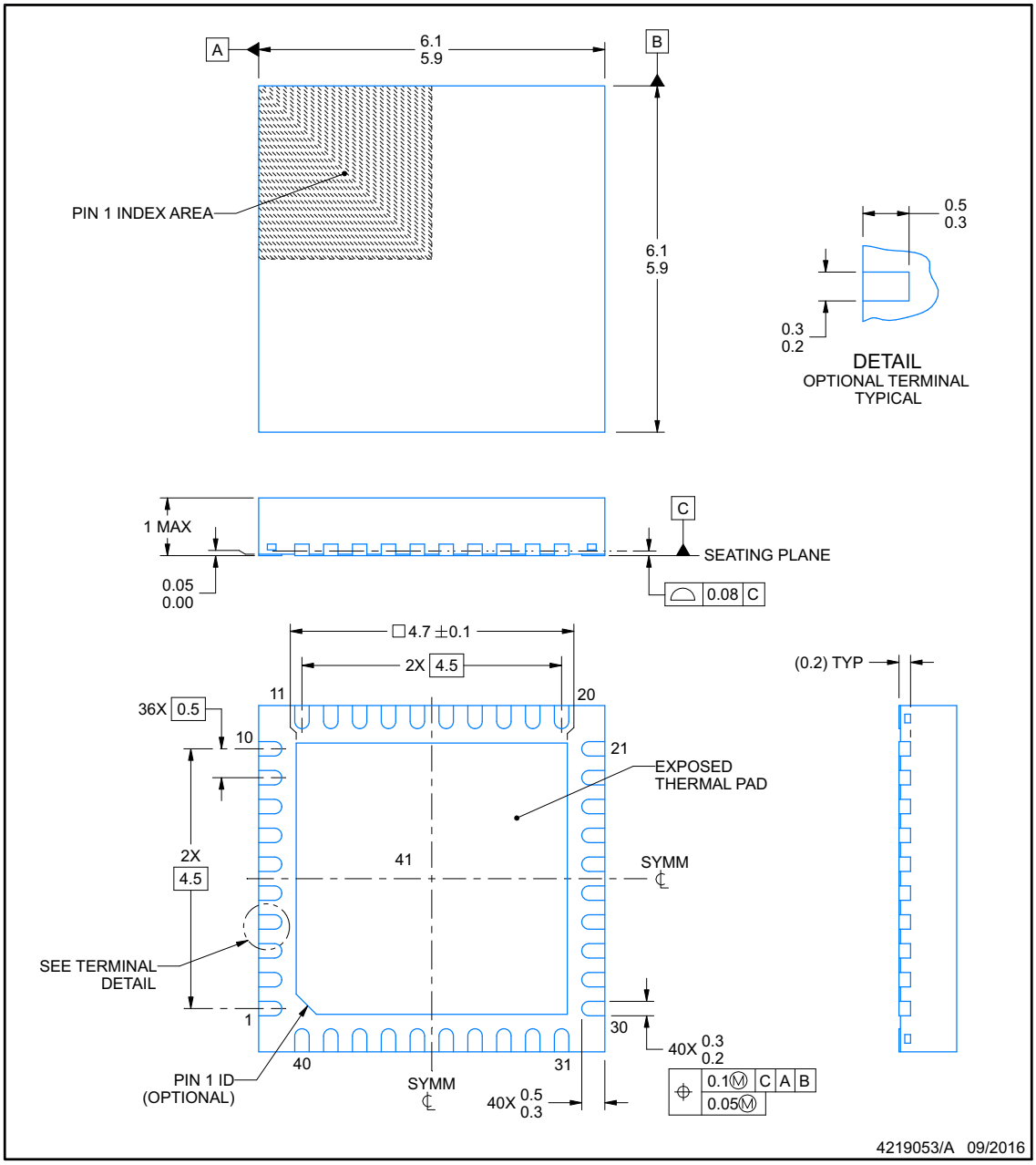


PACKAGE OUTLINE

RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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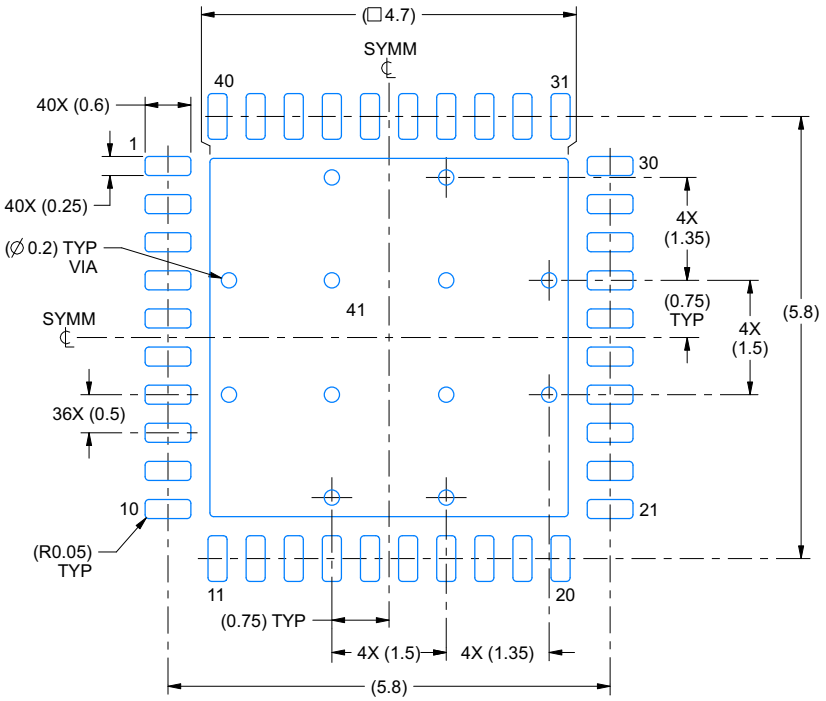
EXAMPLE BOARD LAYOUT

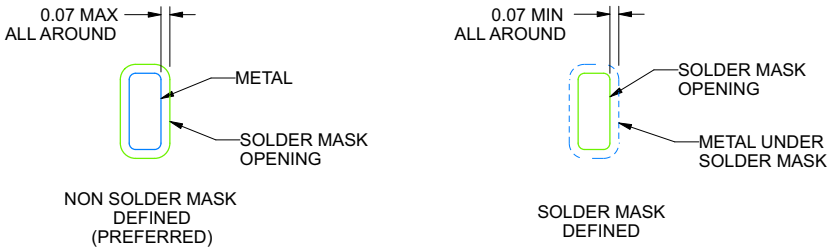
RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4219053/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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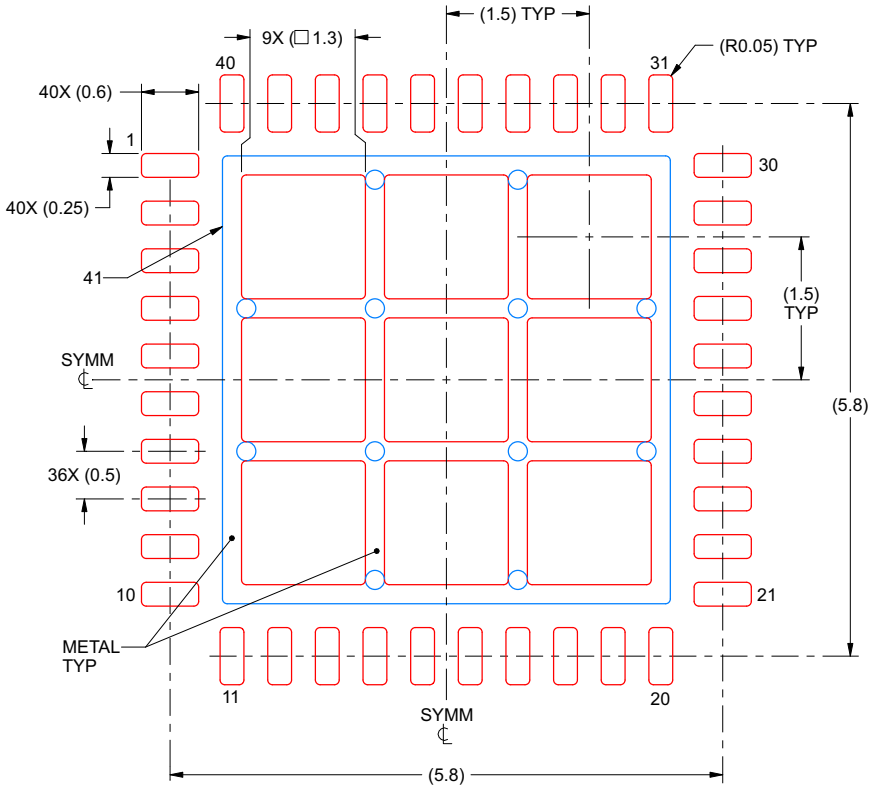
EXAMPLE STENCIL DESIGN

RHA0040C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS9127RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9127
ADS9128RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9128
ADS9129RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9129

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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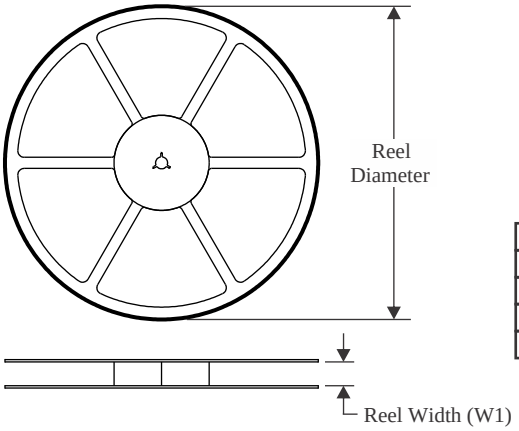
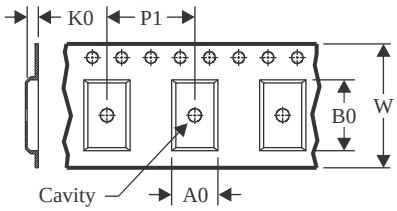
TAPE AND REEL INFORMATION

REEL DIMENSIONS

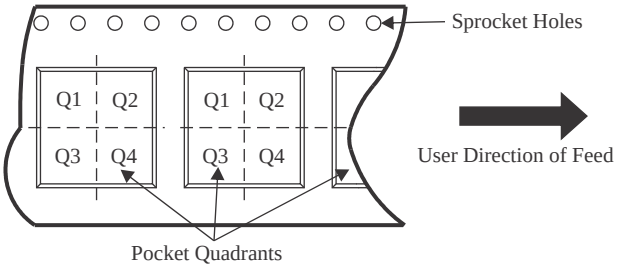


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

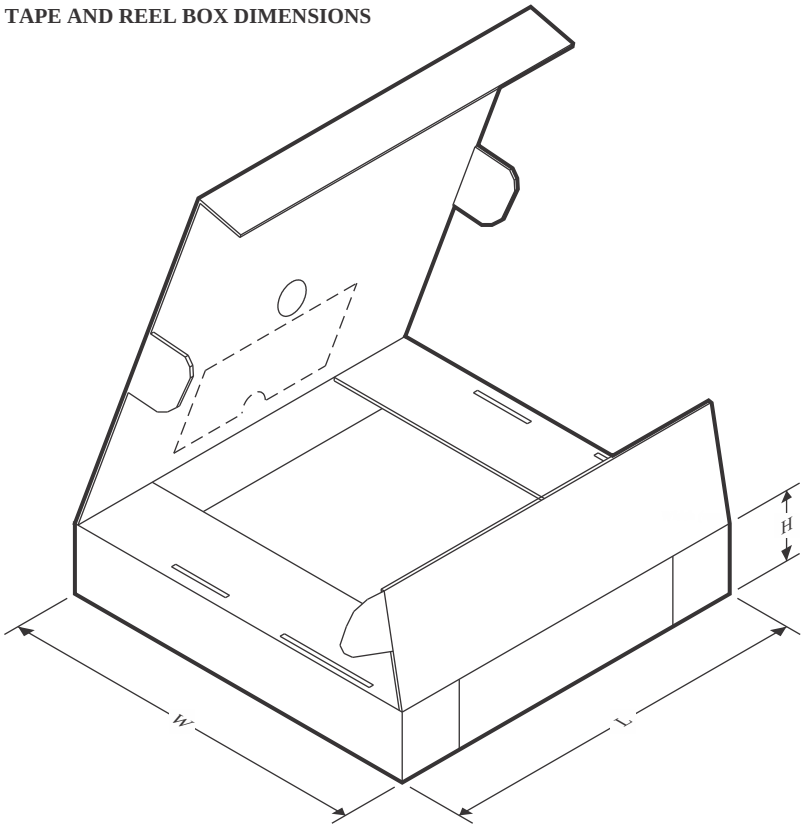
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS9127RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
ADS9128RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
ADS9129RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS9127RHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
ADS9128RHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
ADS9129RHAR	VQFN	RHA	40	2500	360.0	360.0	36.0

GENERIC PACKAGE VIEW

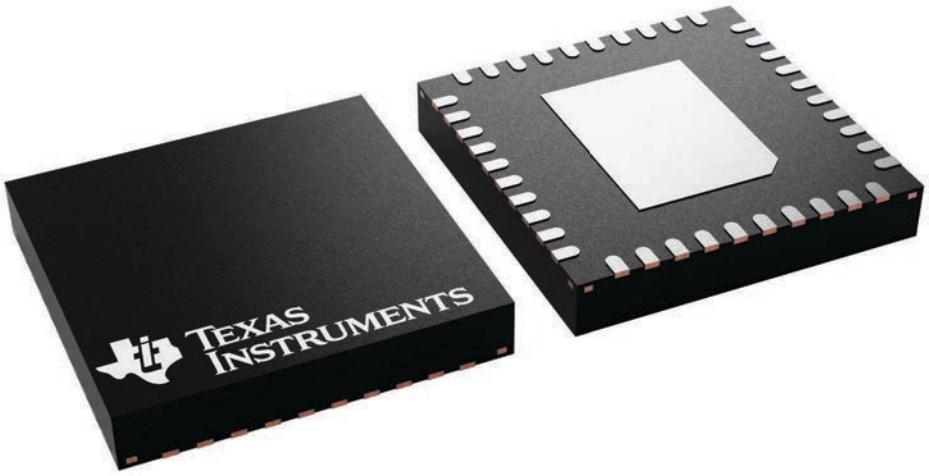
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

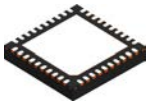
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

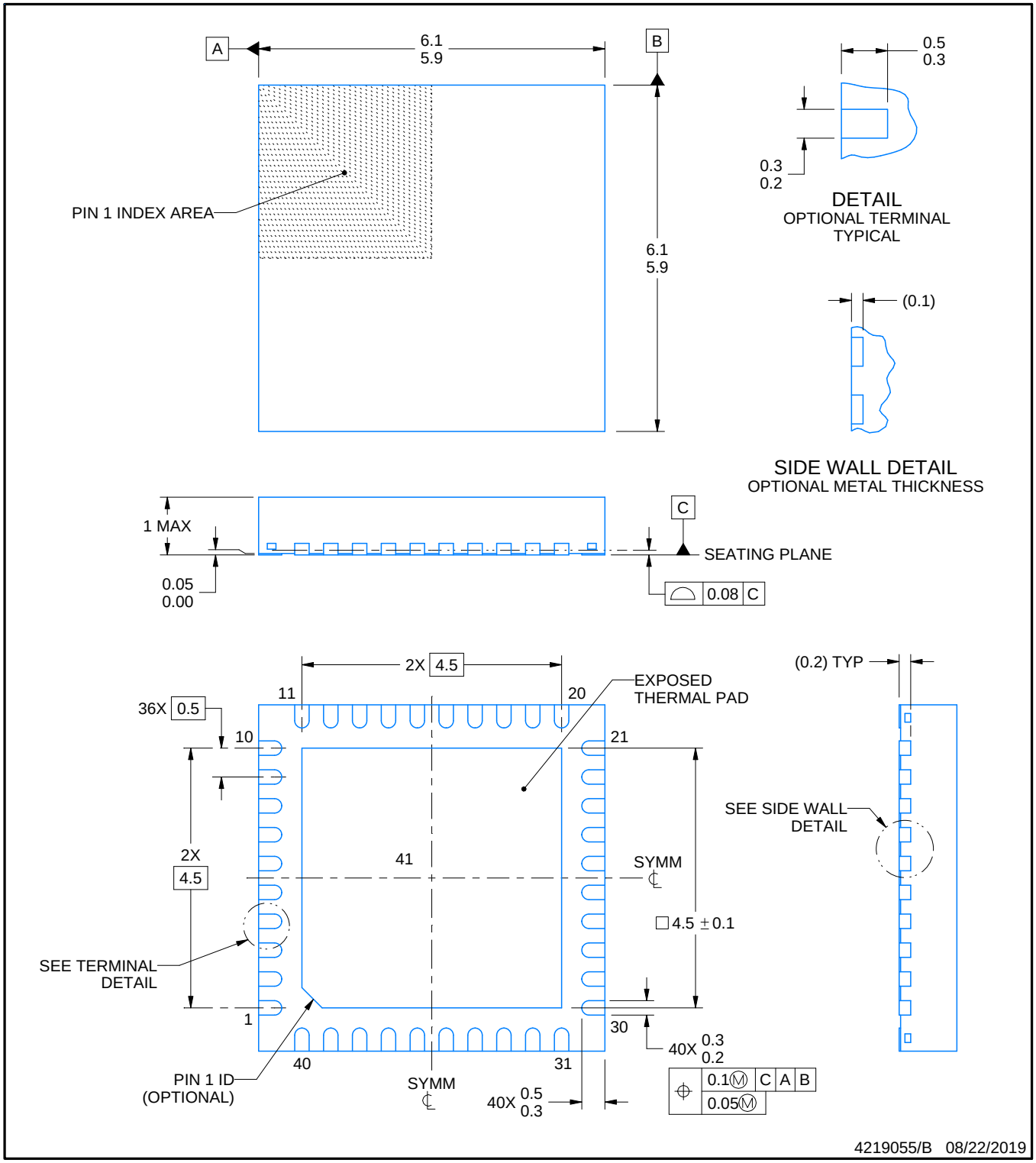
RHA0040H



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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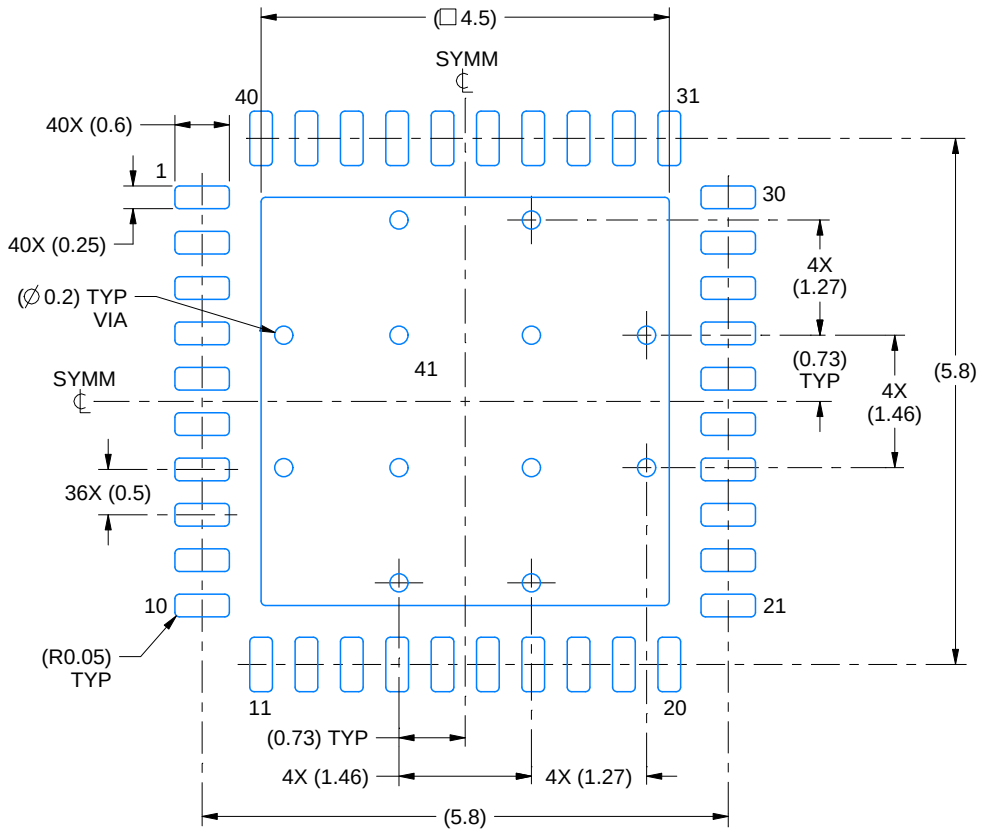
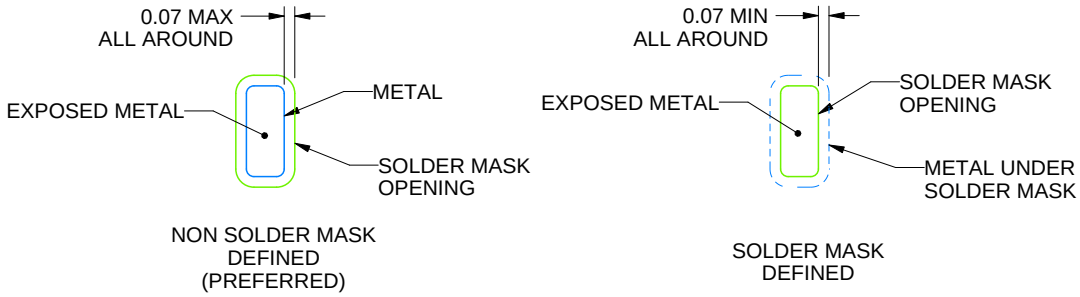


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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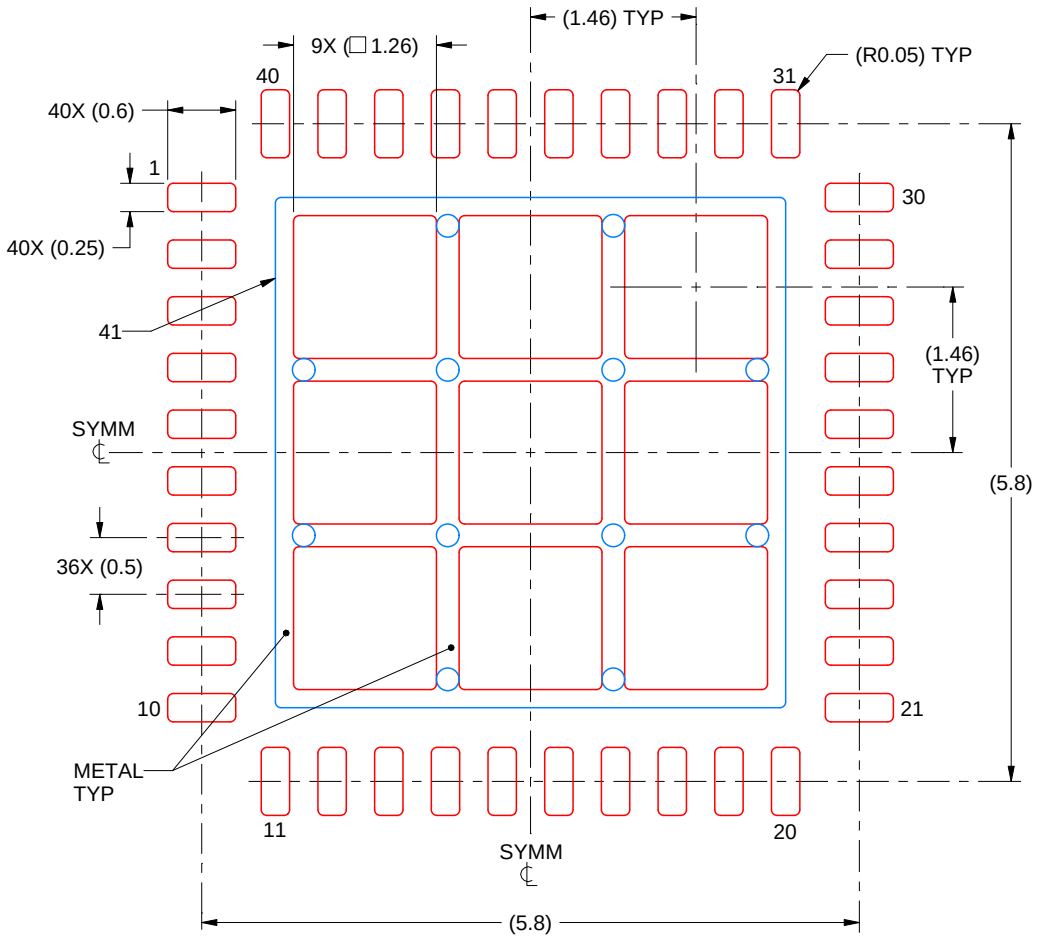

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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