ADS921x Dual, Simultaneous Sampling, 18-Bit, 10-MSPS SAR ADC With Fully Differential ADC Input Driver

1 Features

- High-speed, 10-MSPS/ch sampling rate
  – ADS9218: 10 MSPS/ch
  – ADS9217: 5 MSPS/ch
- 2-channel, simultaneous sampling
- Feature integration:
  – Integrated ADC driver
  – Integrated precision reference
  – Common-mode voltage output buffer
- High-performance
  – 18-bit no missing codes
  – INL: ±1 LSB, DNL: ±0.75 LSB
  – SNR: 95 dB, THD: –115 dB at f_{IN} = 2 kHz
- Wide input bandwidth:
  – ADS9218: 90 MHz (–3 dB)
  – ADS9217: 45 MHz (–3 dB)
- Low-power 180 mW/ch at 10 MSPS/ch
- Serial LVDS interface:
  – SDR and DDR output modes
  – Synchronous clock and data output
- Extended operating range: –40°C to +125°C
- 6-mm × 6-mm VQFN package

2 Applications

- Power analyzers
- Source measurement units (SMU)
- Marine equipment
- Servo drive position feedback
- DC power supplies, AC sources, electronic loads

3 Description

The ADS921x is an 18-bit, 10-MSPS/ch, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated driver for the ADC inputs. The ADC consumes only 180 mW/ch at 10 MSPS/ch and the power consumption scales with lower sampling rates.

The ADS921x uses a serial low-voltage differential signaling (SLVDS) data interface that enables high-speed digital interface while minimizing digital switching noise. The device comes in a space-saving, 6-mm × 6-mm, VQFN package.

The ADS921x is specified for the extended temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
ADS9218	RHA (VQFN, 40)	6.0 mm × 6.0 mm
ADS9217(2)	RHA (VQFN, 40)	6.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview information (not Production Data).

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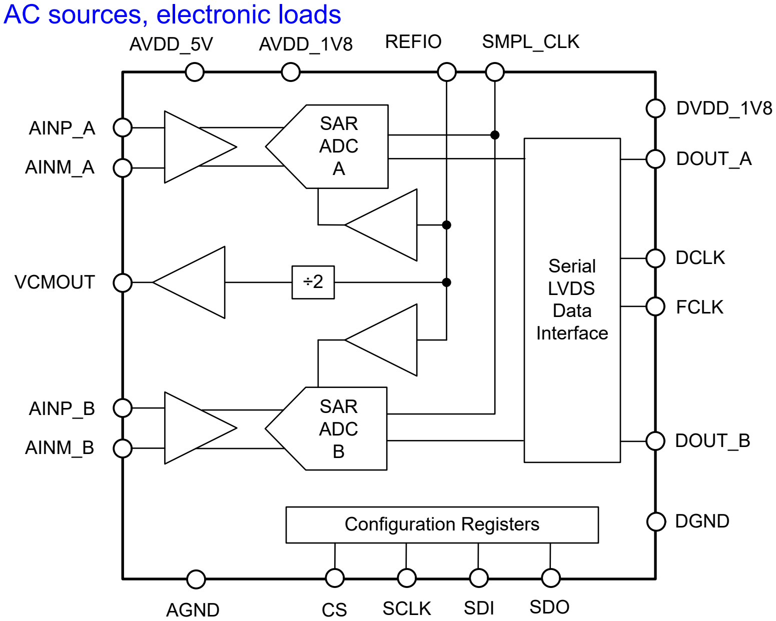

Device Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial Release

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5 Pin Configuration and Functions

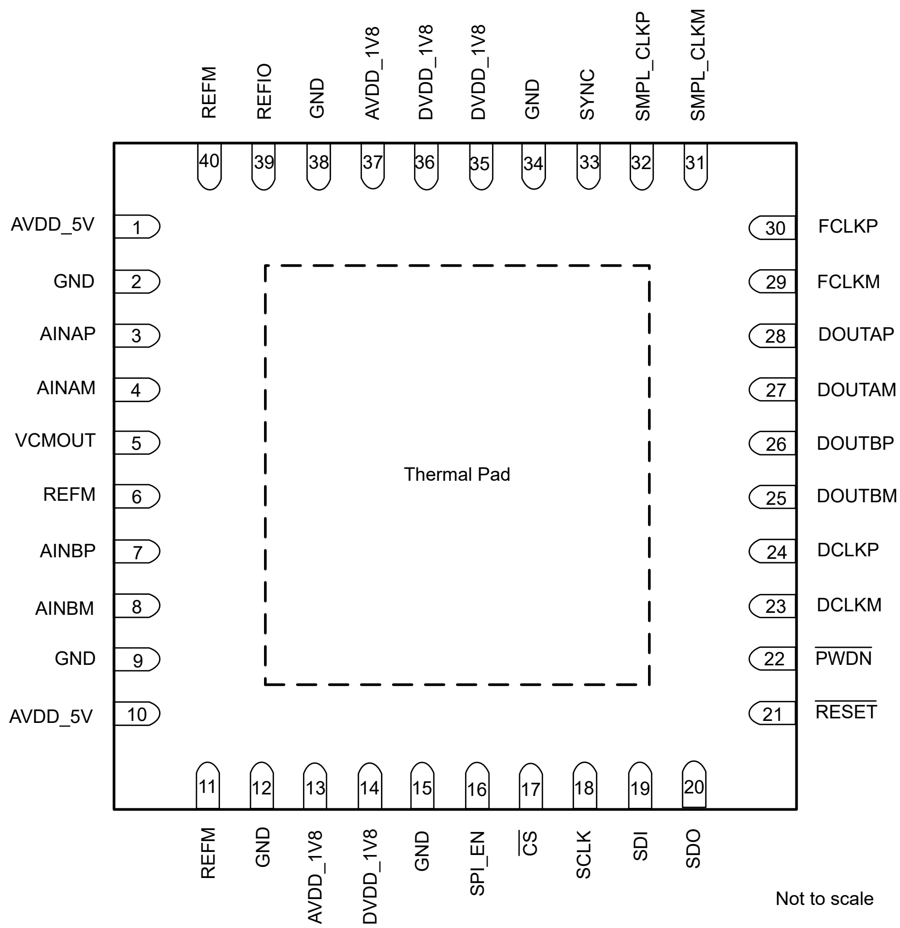

Figure 5-1. RHA Package, 6-mm × 6-mm, 40-Pin VQFN (Top View)

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AINAM	4	I	Negative analog input for ADC A.
AINAP	3	I	Positive analog input for ADC A.
AINBM	8	I	Negative analog input for ADC B.
AINBP	7	I	Positive analog input for ADC B.
AVDD_1V8	13, 37	P	1.8-V analog power-supply pin.
AVDD_5V	1, 10	P	5-V analog power-supply pin.
CS	17	I	Chip-select input pin for the configuration interface; active low.
DCLKM	23	O	Negative differential data clock output. Connect a 100-Ω resistor between DCLKP and DCLKM close to the receiver.
DCLKP	24	O	Positive differential data clock output. Connect a 100-Ω resistor between DCLKP and DCLKM close to the receiver.
DOUTAM	27	O	Negative differential data output. Connect a 100-Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.

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Pin Functions (continued)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
DOUTAP	28	O	Positive differential data output corresponding to ADC A. Connect a 100-Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.
DOUTBM	25	O	Positive differential data output corresponding to ADC B in 2-lane mode. Connect a 100-Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
DOUTBP	26	O	Negative differential data output corresponding to ADC B in 2-lane mode. Connect a 100-Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
DVDD_1V8	14, 35, 36	P	1.8-V digital power supply.
FCLKM	29	O	Negative differential data frame clock output. Connect a 100-Ω resistor between FCLKP and FCLKM close to the receiver.
FCLKP	30	O	Positive differential data frame clock output. Connect a 100-Ω resistor between FCLKP and FCLKM close to the receiver.
GND	2, 9, 12, 15, 34, 38	P	Ground.
$\overline{\text{PWDN}}$	22	I	Power-down control; active low. Connect to DVDD_1V8 if unused.
REFIO	39	I/O	Internal reference voltage output. External reference voltage input. Connect a 10-μF decoupling capacitor to REFM.
REFM	6, 11, 40	P	Reference ground. Connect to GND.
$\overline{\text{RESET}}$	21	I	Reset input; active low. Connect to DVDD_1V8 if unused.
SCLK	18	I	Serial clock input for the configuration interface.
SDI	19	I	Serial data input for the configuration interface.
SDO	20	O	Serial data output for the configuration interface.
SMPL_CLKM	31	I	ADC sampling clock input. Connect this pin to GND for the CMOS sampling clock.
SMPL_CLKP	32	I	ADC sampling clock input. Clock input for the CMOS sampling clock.
SPI_EN	16	I	Control to enable configuration of the SPI interface; active high. Connect a pullup resistor to DVDD_1V8 to keep the configuration interface enabled. Connect to GND if SPI configuration is unused.
SYNC	33	I	Synchronization input for internal averaging filter. Connect to GND if unused.
VCMOUT	5	O	Common-mode voltage output. Use this output to set the common-mode voltage at the ADC inputs. Connect a 1-μF decoupling capacitor to GND.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
DVDD_1V8 to GND	–0.3	2.1	V
AVDD_1V8 to GND	–0.3	2.1	V
AVDD_5V to GND	–0.3	5.5	V
AINAP, AINAM, AINBP, and AINBM to GND	GND – 0.3	AVDD_5V + 0.3	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
Digital inputs to GND	GND – 0.3	DVDD_1V8 + 0.3	V
REFM to GND	–0.3	0.3	V
Input current to any pin except supply pins[2]	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins AINAP, AINAM, AINBP, and AINBM[1]	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]	±1000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		ADS92XX RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND	4.75	5	5.25	V
AVDD_1V8	Analog power supply	AVDD_1V8 to GND	1.75	1.8	1.85	V
DVDD_1V8	Digital power supply	DVDD_1V8 to GND	1.75	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.076	4.096	4.116	V
ANALOG INPUTS						
V_{IN}	Absolute input voltage	AINx[1] to GND	0.7		4.1	V
FSR	Full-scale input range	(AINAP – AINAM) and (AINBP – AINBM)	–3.2		3.2	V
V_{CM}	Common-mode input range	(AINAP – AINAM) / 2 and (AINBP – AINBM) / 2	V_{CMOUT} – 0.025		V_{CMOUT} + 0.025	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.

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6.5 Electrical Characteristics

at AVDD_5V = 4.75 V to 5.25 V, AVDD_1V8 = 1.75 V to 1.85 V, DVDD_1V8 = 1.75 V to 1.85 V, internal V_{REF} = 4.096 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_B	Input bias current			0.5	TBD	µA
I_B	Input bias current thermal drift			1		nA/°C
DC PERFORMANCE						
	Resolution	No missing codes		18		Bits
DNL	Differential nonlinearity		–0.75	±0.4	0.75	LSB
INL	Integral nonlinearity		–4	±1	4	LSB
$V_{(OS)}$	Input offset error			±2		LSB
dV_{OS}/dT	Input offset error thermal drift			±1		ppm/°C
	Offset error match	$V_{(OS)}$ (ADC_A – ADC_B)		0.5		LSB
G_E	Gain error(1)		–0.05	±0.01	0.05	%FSR
dG_E/dT	Gain error thermal drift(1)			±1		ppm/°C
	Gain error match	G_E (ADC_A – ADC_B)		±0.001		%FSR
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2 kHz		95		dB
		f_{IN} = 1 MHz		94		
SNR	Signal-to-noise ratio	f_{IN} = 2 kHz		95.1		dB
		f_{IN} = 1 MHz		94.1		
THD	Total harmonic distortion	f_{IN} = 2 kHz		–115		dB
		f_{IN} = 1 MHz		–102		
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		120		dB
		f_{IN} = 1 MHz		102		
	Isolation crosstalk	f_{IN} = 1 MHz		TBD		dB
	Aperture Jitter			0.3		ps_{RMS}
BW	Input Bandwidth (–3-dB)	ADS9218		90		MHz
		ADS9217		45		
COMMON-MODE OUTPUT BUFFER						
V_{CMOUT}	Common-mode output voltage			2.4		V
	Output current drive		0		5	µA
LVDS OUTPUT (CLKOUT, DOUTA, and DOUTB)						
V_{ODIFF}	Differential output voltage	R_L = 100Ω	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_L = 100Ω	1.08	1.1	1.32	V
CMOS INPUTS ($\overline{CS}$, SCLK, and SDI)						
V_{IL}	Input low logic level		–0.3		0.3 DVDD	V
V_{IH}	Input high logic level		0.7 DVDD		DVDD	V
CMOS OUTPUT (SDO)						
V_{OL}	Output low logic level	I_{OL} = 200 µA sink	0		0.2 DVDD	V
V_{OH}	Output high logic level	I_{OH} = 200 µA source	0.8 DVDD		DVDD	V
POWER SUPPLY						
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput		36	TBD	mA
		No conversion, external reference			TBD	

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6.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75 V to 5.25 V, AVDD_1V8 = 1.75 V to 1.85 V, DVDD_1V8 = 1.75 V to 1.85 V, internal V_{REF} = 4.096 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVDD_1V8}	Supply current from AVDD_1V8	Maximum throughput		67	TBD	mA
		No conversion, external reference			TBD	mA
I_{DVDD_1V8}	Supply current from DVDD_1V8	Maximum throughput		34	TBD	mA
		No conversion, external reference		5	TBD	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.

6.6 Timing Requirements

at AVDD_5V = 4.75 V to 5.25 V, AVDD_1V8 = 1.75 V to 1.85 V, DVDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = -40°C to +125°C; typical values at T_A = 25°C.

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling frequency	ADS9218		10	MSPS
		ADS9217		5	
t_{CYCLE}	ADC cycle-time period		$1/f_{CYCLE}$		s
$t_{PL\_SMPLCLK}$	Sample clock low time		0.48	0.52	t_{CYCLE}
$t_{PH\_SMPLCLK}$	Sample clock high time		0.48	0.52	t_{CYCLE}
f_{CLK}	Maximum SCLK frequency			10	MHz
t_{CLK}	Minimum SCLK time period		100		ns
SPI INTERFACE TIMINGS					
t_{hi_CSZ}	Pulse duration: $\overline{CS}$ high		220		ns
t_{PH_CK}	SCLK high time		0.48	0.52	t_{CLK}
t_{PL_CK}	SCLK low time		0.48	0.52	t_{CLK}
t_{d_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK rising edge		20		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge		10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI		5		ns
t_{d_CKCS}	Delay time: last SCLK falling edge to $\overline{CS}$ rising		5		ns

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6.7 Switching Characteristics

at AVDD_5V = 4.75 V to 5.25 V, AVDD_1V8 = 1.75 V to 1.85 V, DVDD_1V8 = 1.75 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = -40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			25	ms
LVDS DATA INTERFACE					
t_{RT}	Rise time	with 50Ω transmission line of length = 20 mm, differential R_L = 100Ω, and C_L = 1 pF		600	ps
t_{FT}	Fall time			600	ps
t_{CYCLE}	Sampling clock period	ADS9218	100		ns
		ADS9217	200		ns
t_{DCLK}	Clock output		4.167		ns
	Clock duty cycle		45	55	%
t_{d_DCLKDO}	Time delay: DCLKP rising to corresponding data valid	at 5Msps, SDR mode	–0.8	0.8	ns
$t_{off\_DCLKDO\_r}$	Time offset: DCLKP rising to corresponding data valid	at 5Msps, DDR mode	t_{DCLK}/4 – 0.8	t_{DCLK}/4 + 0.8	ns
$t_{off\_DCLKDO\_f}$	Time offset: DCLKP falling to corresponding data valid	at 5Msps, DDR mode	t_{DCLK}/4 – 0.8	t_{DCLK}/4 + 0.8	ns
t_{PD}	Time delay: SMPL_CLK falling to DCLKP rising			t_{DCLK}	ns
$t_{PU\_SMPL\_CLK}$	Time delay: free running clock connected to SMPL_CLK to ADC data valid			100	µs
SPI INTERFACE TIMINGS					
t_{den_CKDO}	Time delay: 8th SCLK rising edge to SDO enable			30	ns
t_{dz_CKDO}	Time delay: 24th SCLK rising edge to SDO going Hi-Z			30	ns
t_{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			20	ns
t_{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		2		ns

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6.8 Timing Diagrams

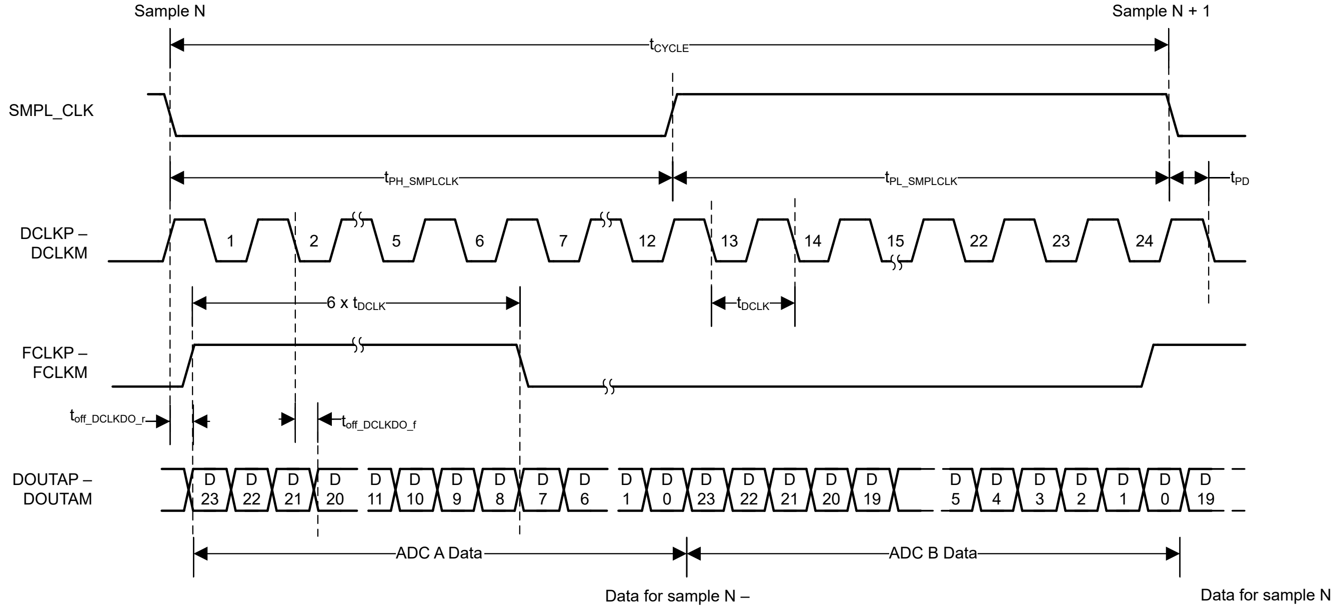

Figure 6-1. LVDS Data Interface: 1-Lane DDR

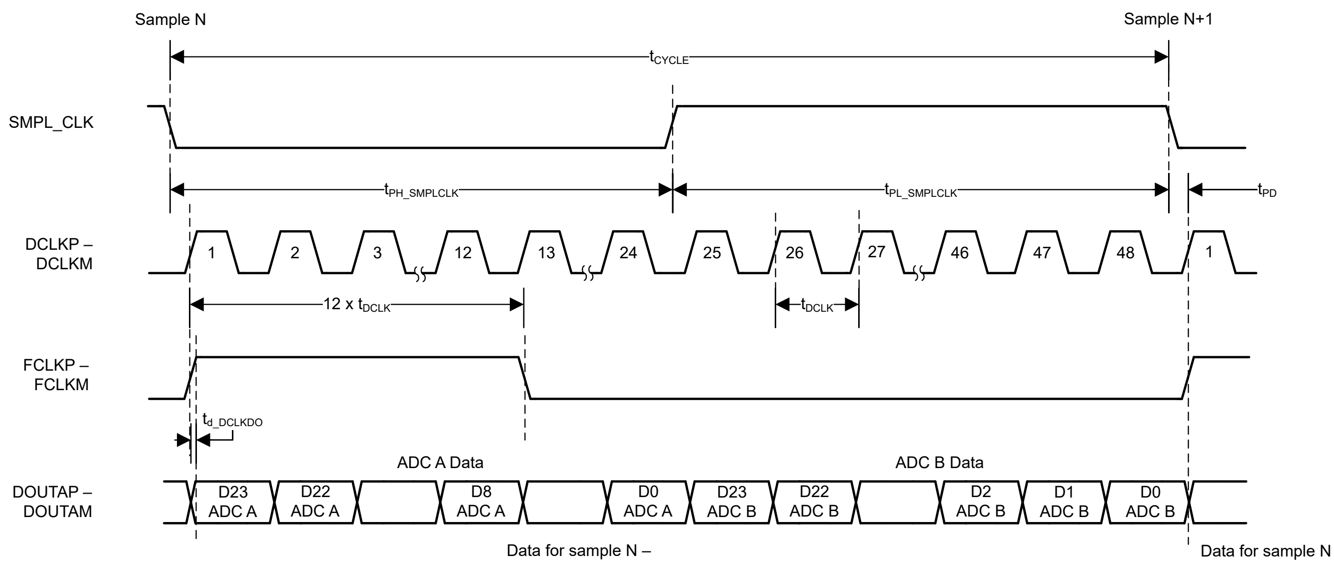

Figure 6-2. LVDS Data Interface: 1-Lane SDR

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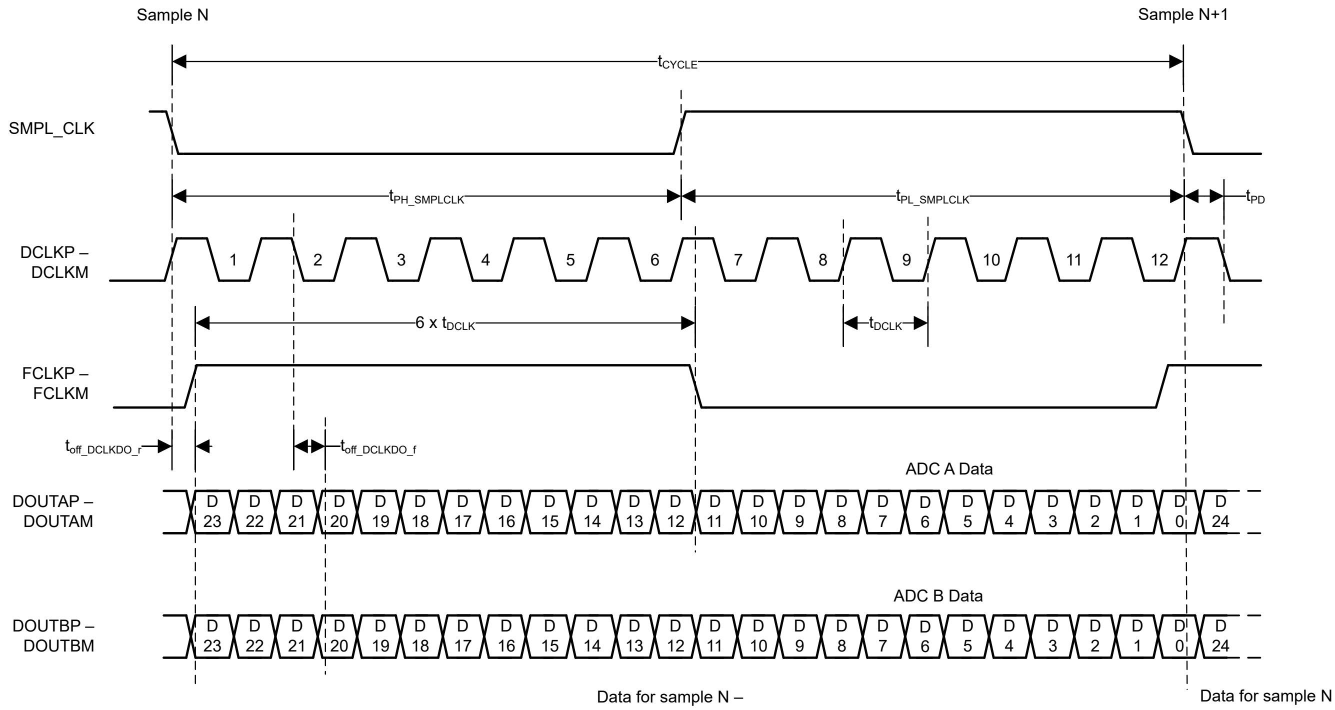

Figure 6-3. LVDS Data Interface: 2-Lane DDR

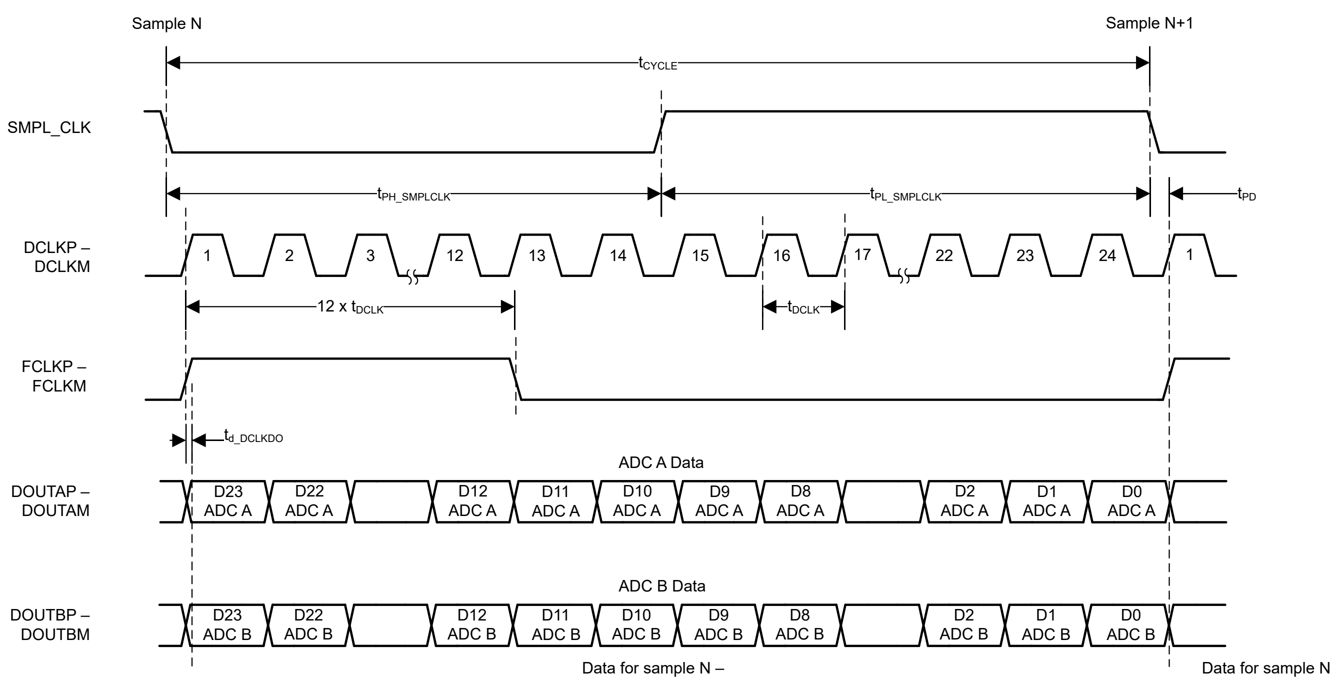

Figure 6-4. LVDS Data Interface: 2-Lane SDR

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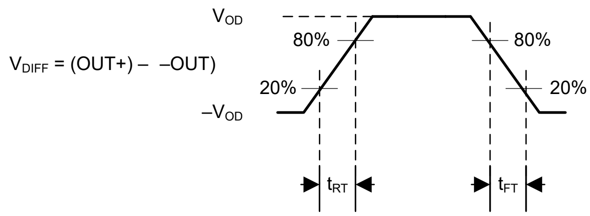

Figure 6-5. LVDS Output Transition Times

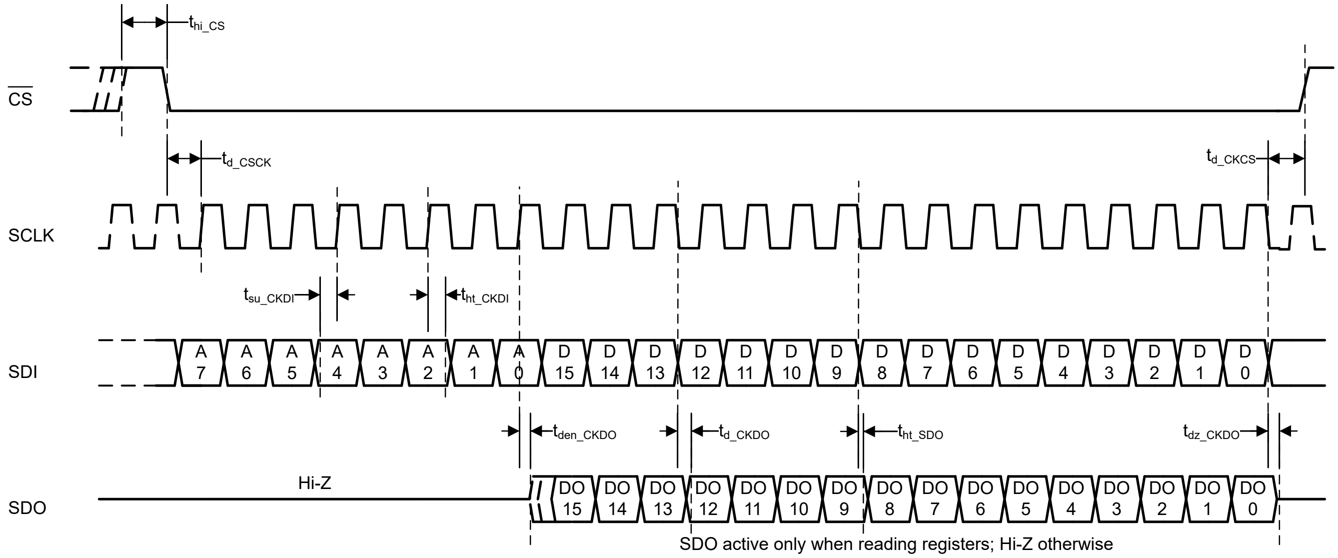

Figure 6-6. Configuration SPI Interface

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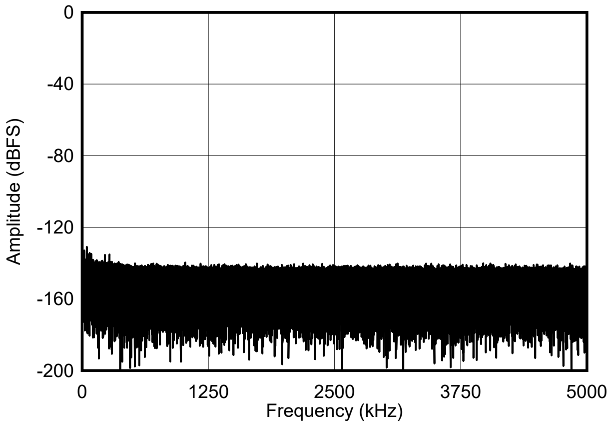
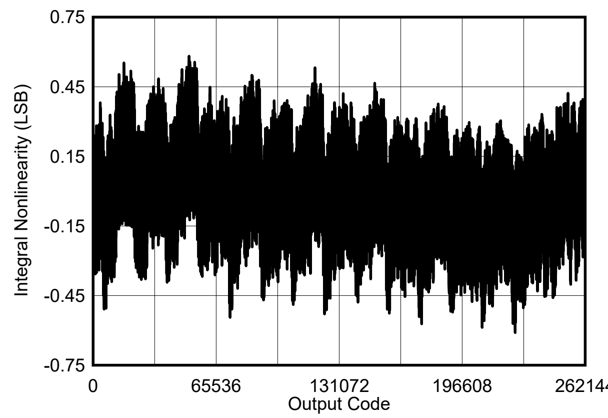
6.9 Typical Characteristics: ADS9218

at T_A = 25°C, AVDD_5V = 5 V, AVDD_1V8 = 1.8 V, DVDD_1V8 = 1.8 V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



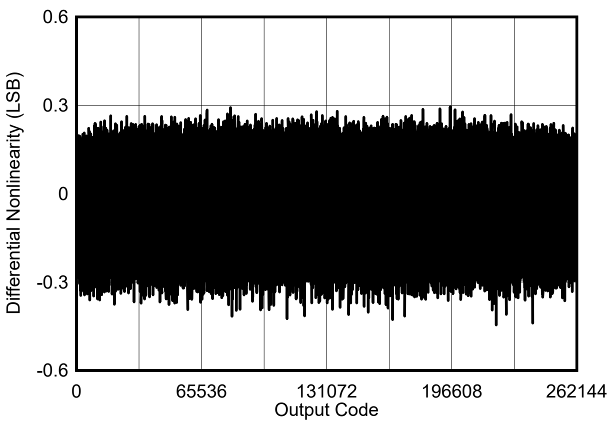
f_{IN} = 2 kHz, SNR = 94.8 dB, THD = –115.1 dB

Figure 6-7. Typical FFT



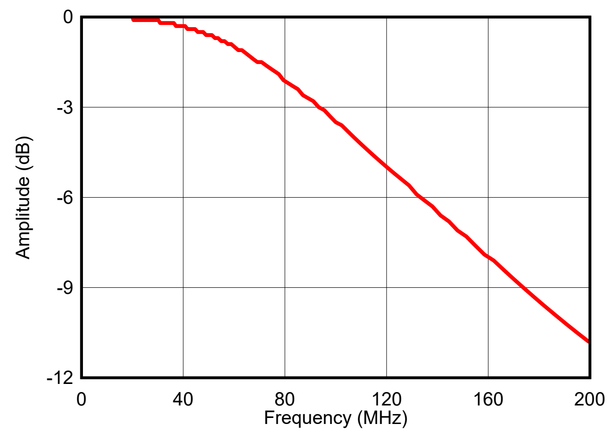
Typical INL = ±0.6 LSB

Figure 6-8. Typical INL



Typical DNL = ±0.4 LSB

Figure 6-9. Typical DNL



Typical BW (–3 dB) = 90 MHz

Figure 6-10. Typical Analog Input Bandwidth

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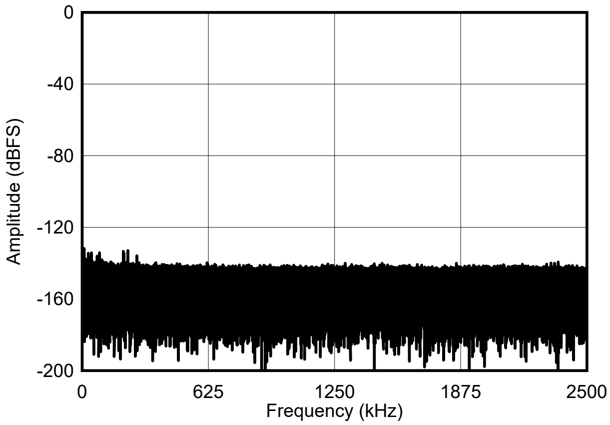
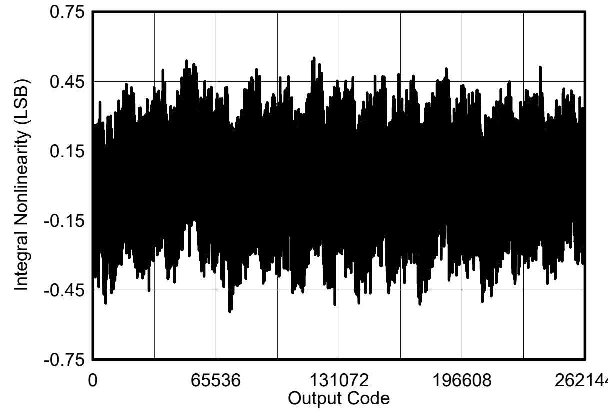
6.10 Typical Characteristics: ADS9217

at T_A = 25°C, AVDD_5V = 5 V, AVDD_1V8 = 1.8 V, DVDD_1V8 = 1.8 V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



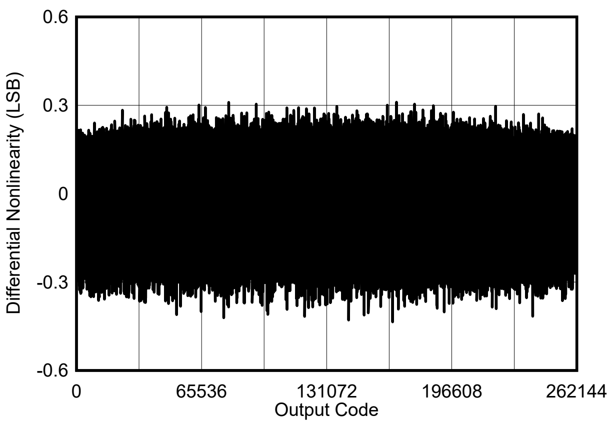
f_{IN} = 2 kHz, SNR = 94.8 dB, THD = –115.2 dB

Figure 6-11. Typical FFT



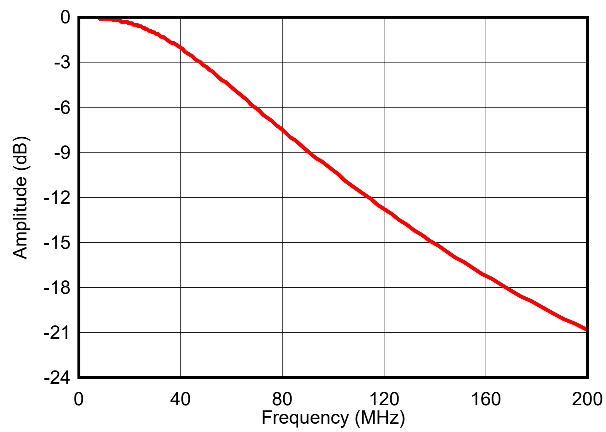
Typical INL = ±0.6 LSB

Figure 6-12. Typical INL



Typical DNL = ±0.4 LSB

Figure 6-13. Typical DNL



Typical BW (–3 dB) = 45 MHz

Figure 6-14. Typical Analog Input Bandwidth

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7 Detailed Description

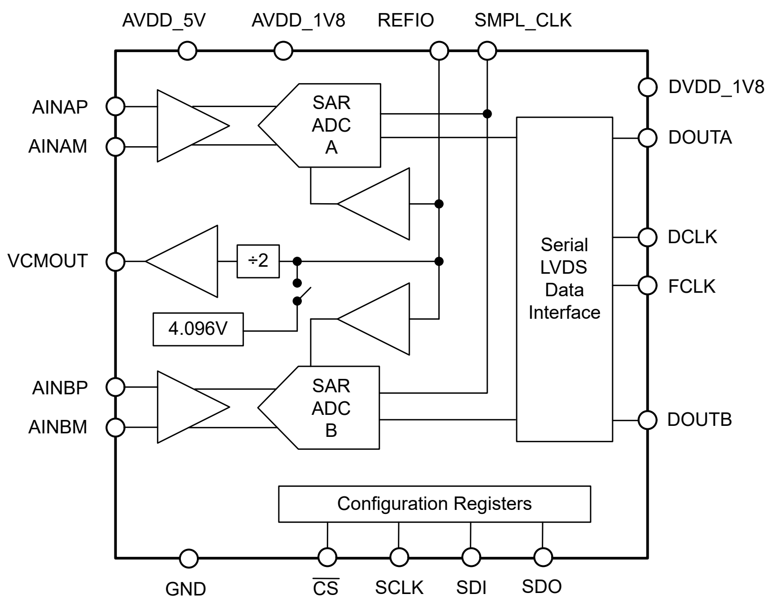
7.1 Overview

The ADS921x is an 18-bit, 10-MSPS/ch, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC). The ADS921x integrates a high-impedance buffer at the ADC inputs, voltage reference, reference buffer, and common-mode voltage output buffer. The ADS9218 supports unipolar differential analog input signals. The buffer at the ADC inputs is optimized for low-distortion and low-power operation.

For DC level shifting of the analog input signals, the device has a common-mode voltage output buffer. The common-mode voltage is derived from the output of the integrated reference buffer. When a conversion is initiated, the differential input between the (AINAP – AINAM) and (AINBP – AINBM) pins is sampled. The ADS921x uses a clock input on the SMPL_CLKP pin to initiate conversions.

The ADS921x consumes only 180 mW/ch of power when operating at 10 MSPS/ch, which includes the power dissipation of the buffer at the ADC inputs. The serial LVDS (SLVDS) digital interface simplifies board layout, timing, firmware, and supports full throughput at lower clock speeds.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Analog Inputs

The analog inputs of the ADS921x are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common-mode voltage that must be equal to the voltage on the VCMOUT pin. DC-coupled input signals must have a common-mode voltage that meets the device input common-mode voltage range. Figure 7-1 shows an equivalent input network diagram.

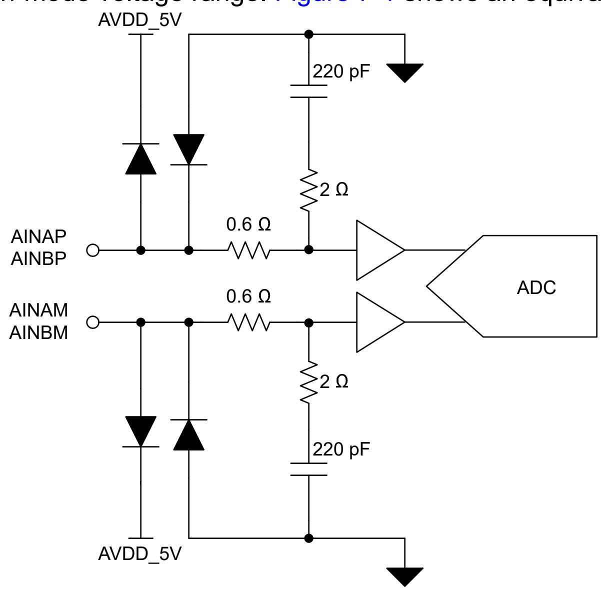

Figure 7-1. Equivalent Input Network

7.3.2 Analog Input Bandwidth

Figure 6-10 and Figure 6-14 illustrate the analog full-power input bandwidth of the ADS921x device family. The –3-dB bandwidth is 90 MHz and 45 MHz for the ADS9218 and ADS9217, respectively.

7.3.3 ADC Transfer Function

The ADS921x supports a ±3.2-V differential input range. The device outputs 18-bit conversion data in either straight-binary or binary two's-complement formats. As shown in Table 7-1, the format for the output codes is the same across all analog channels. The format for the output codes can be configured using the DATA_FORMAT field in register address 0x0D. The least significant bit (LSB) for the ADC is given by 1 LSB = 6.4 V / 2^{18} .

Table 7-1. Transfer Characteristics

INPUT VOLTAGE	DESCRIPTION	ADC OUTPUT IN TWO'S-COMPLEMENT FORMAT	ADC OUTPUT IN STRAIGHT-BINARY FORMAT
≤ –3.2 V + 1 LSB	Negative full-scale code	0x80000	0x00000
0 V + 1 LSB	Mid-code	0x00000	0x1FFFF
≥ 3.2 V – 1 LSB	Positive full-scale code	0x1FFFF	0x3FFFF

7.3.4 Reference

The ADS921x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 10-µF ceramic bypass capacitor to the REFIO pin. An external reference can also be connected at the REFIO pin with the internal reference voltage disabled by writing to PD_REF field in register address 0xC1.

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7.3.4.1 Internal Reference Voltage

The ADS921x features an internal reference voltage with a nominal output voltage of 4.096 V. On power-up, the internal reference is enabled by default. Place a minimum 10-µF decoupling capacitor between the REFIO and REFM pins. Figure 7-2 shows a block diagram of the internal reference voltage.

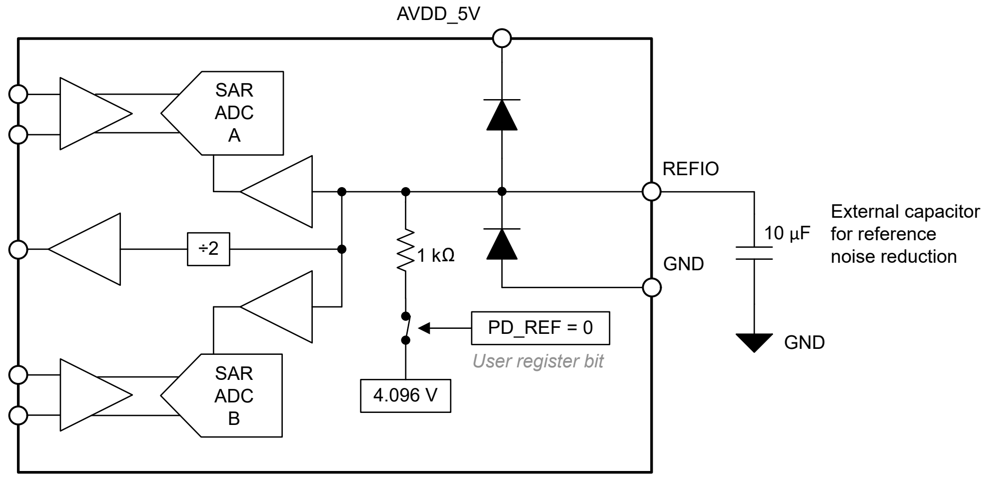

Figure 7-2. Internal Reference Voltage

7.3.4.2 External Reference Voltage

An external 4.096-V reference voltage can be connected at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, the REF7040 is recommended. To disable the internal reference, set PD_REF = 1b in address 0xC1 in register bank 1. The REFIO pin has electrostatic discharge (ESD) protection diodes connected to the AVDD_5V and REFM pins. Figure 7-3 shows an external reference diagram.

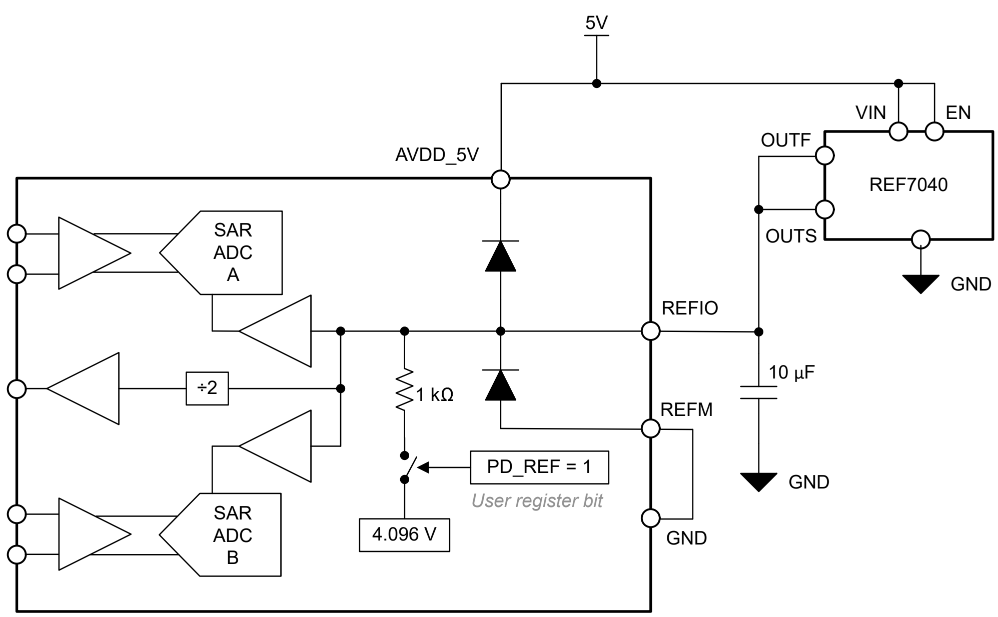

Figure 7-3. External Reference Voltage

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7.3.5 Data Interface

The ADS921x features a high-speed serial LVDS data interface with 2-lane and 1-lane options for data output. The host can configure the output data frame width to 20 bits or 24 bits with the single-data rate (SDR) and double-data rate (DDR) modes.

The ADS921x generates a data clock DCLK that is a multiple of the ADC sampling clock SMPL_CLK. The data clock frequency depends on the number of data output lanes (1 or 2), data frame width (20 bit or 24 bit) and data rate (SDR or DDR). Equation 1 calculates the DCLK speed. Table 7-2 lists the possible values for the output data clock frequency.

$$\text{DCLK speed} = \frac{2\ \text{ADC channels}\ \times \text{Data Frame Width (24 bit or 20 bit)}}{\text{Data Lanes (1 or 2)} \times \text{Data Rate(SDR = 1, DDR = 2)}} \times \text{SMPL\_CLK} \quad (1)$$

Table 7-2. Data Clock (DCLK) Speed[(1)]

ADC CHANNELS	DATA FRAME WIDTH (Bits)	DATA RATE (1 = SDR, 2 = DDR)	OUTPUT LANES	SMPL_CLK MULTIPLIER	DCLK (SMPL_CLK = 5 MHz)	DCLK (SMPL_CLK = 10 MHz)
2	24	1	1	48	240 MHz	480 MHz
			2	24	120 MHz	240 MHz
		2	1	24	120 MHz	240 MHz
			2	12	60 MHz	120 MHz
	20	1	1	40	200 MHz	400 MHz
			2	20	100 MHz	200 MHz
		2	1	20	100 MHz	200 MHz
			2	10	50 MHz	100 MHz

(1) The LVDS output data and clock are specified up to 600 MHz. Faster speeds are not supported.

7.3.5.1 Data Frame Width

As shown in Figure 7-4, the ADS921x supports 24-bit and 20-bit data frame width options. Configure the DATA_WIDTH field in address 0x12 to select the data frame width. The default output data frame width is 24 bits. The ADC resolution is 18 bits, represented by 20 bits. The two extra lower bits in the 20-bit data can be ignored.

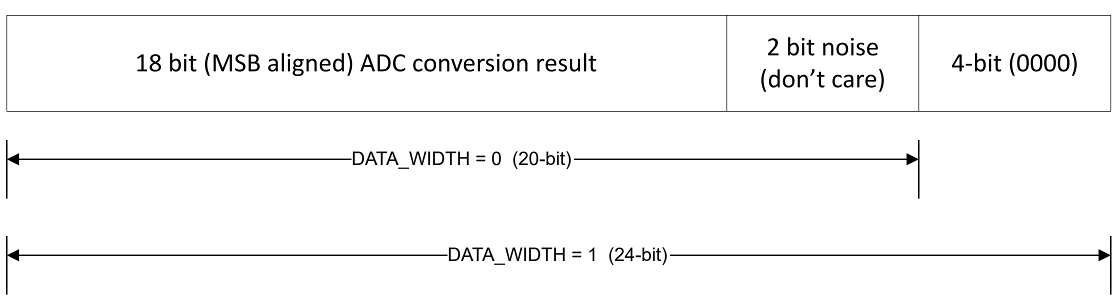

Figure 7-4. Data Frame Width Composition

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7.3.5.2 Test Patterns for Data Interface

The ADS921x features test patterns that can be used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. The test patterns can be enabled by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

The ADS921x supports the following test patterns:

- User-defined output: User-defined, 24-bit pattern. Separate patterns for ADC A and ADC B; see the *User-Defined Test Pattern* section.
- Ramp output: Digital ramp output with a user-defined increment between two steps. There are separate ramp outputs for ADC A and ADC B; see the *Ramp Test Pattern* section.
- Alternate output: User-defined, 24-bit outputs that alternate between ADC A and ADC B user-defined patterns; see the *User-Defined Alternating Test Pattern* section.

To disable the test patterns, set TEST_PAT_EN_CHA and TEST_PAT_EN_CHB to 0b.

7.3.5.2.1 User-Defined Test Pattern

The user-defined test pattern allows the host to specify a fixed 24-bit value that is output by the ADS921x. Configure the registers in bank 1 to enable the user-defined test pattern:

- Configure the test patterns in TEST_PAT0_CHA (address = 0x14, 0x15) and TEST_PAT0_CHB (address = 0x19, 0x1A)
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 0 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 0 (address = 0x18)

The ADS921x outputs the TEST_PAT0_CHA and TEST_PAT0_CHB register values in place of the ADC A and ADC B data, respectively.

7.3.5.2.2 User-Defined Alternating Test Pattern

The user-defined alternating test pattern allows the host to specify two fixed 24-bit values that are output by the ADS921x alternately. Configure the registers in bank 1 to enable the user-defined alternating test pattern:

- Configure the test patterns in TEST_PAT0_CHA (address = 0x14, 0x15), TEST_PAT1_CHA (address = 0x15, 0x16) and TEST_PAT0_CHB (address = 0x19, 0x1A), TEST_PAT1_CHB (address = 0x1A, 0x1B)
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 3 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 3 (address = 0x18)

The ADS921x outputs the TEST_PAT0_CHA and TEST_PAT0_CHB register values in place of the ADC A and ADC B data, respectively, in one output frame and the TEST_PAT1_CHA and TEST_PAT1_CHB register values in the next frame.

7.3.5.2.3 Ramp Test Pattern

The ramp test pattern allows the host to specify a digital ramp that is output by the ADS921x. Configure the registers in bank 1 to enable the ramp test pattern:

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_CHA (address = 0x13) and RAMP_INC_CHB (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 2 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 2 (address = 0x18).

The ADS921x outputs digital ramp values in place of the ADC A and ADC B data, respectively.

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7.3.6 ADC Sampling Clock Input

Use a low jitter external clock with a high slew rate to maximize the ADC SNR performance. The ADS921x can be operated using a single-ended clock input where the single-ended clock consumes less power consumption. Clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, a large clock signal with fast slew rates must be provided.

The sampling clock must be a free-running continuous clock. The ADC generates valid output data, a data clock, and a frame clock $t_{PU\_SMPL\_CLK}$, as specified in the *Switching Characteristics* section after a free-running sampling clock is applied. ADC output data, the data clock, and the frame clock are invalid when the sampling clock is stopped.

Figure 7-5 shows a diagram of the single-ended sampling clock. Connect a single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

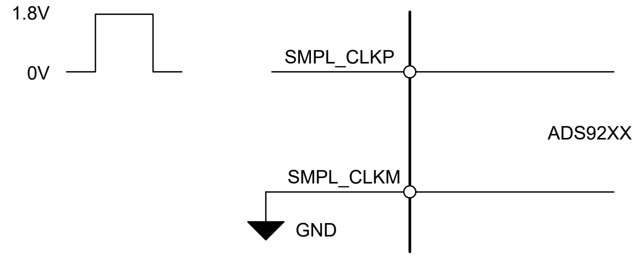

Figure 7-5. Single-Ended Sampling Clock

7.4 Device Functional Modes

7.4.1 Normal Operation

In normal operating mode, the ADS921x is powered-up and digitizes the analog inputs at the falling edge of the sampling clock. The ADC outputs the data clock, frame clock, and MSB-aligned, 18-bit conversion result.

7.4.2 Power-Down Options

Power-down mode can be enabled by a register write or with the $\overline{PWDN}$ pin. The $\overline{PWDN}$ pin has an internal pullup resistor to DVDD_1V8. The $\overline{PWDN}$ pin must be pulled low to enable power-down mode.

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7.5 Programming

7.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 can be selected for read or write operation by configuring the PAGE_SEL0 and PAGE_SEL1 bits, respectively. Registers in bank 0 are always accessible, irrespective of the PAGE_SELx bits because the register addresses are unique and are not used in register banks 1 and 2.

As shown in Figure 7-6, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

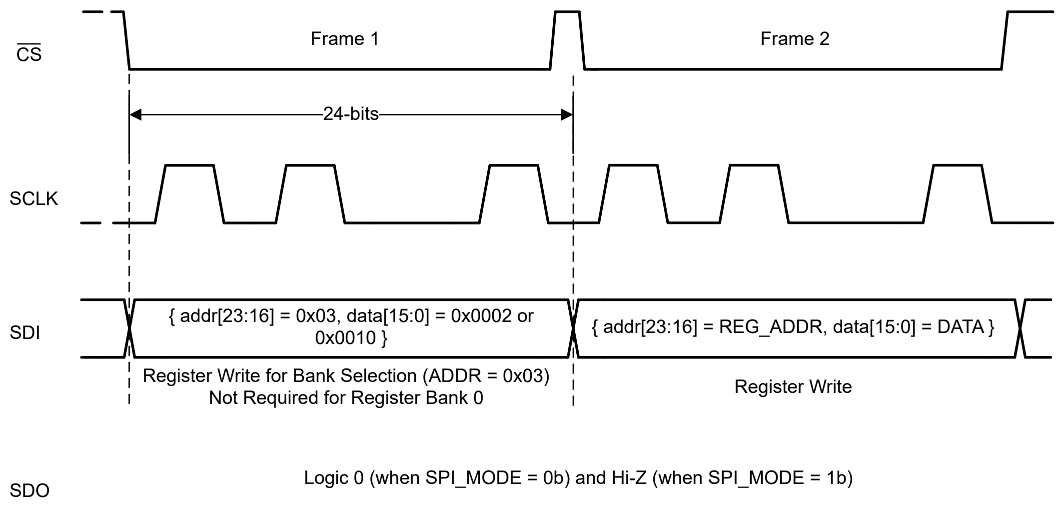

Figure 7-6. Register Write

7.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in Figure 7-7, registers can be read using two 24-bit SPI frames after SPI_RD_EN and SPI_MODE are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 7-7, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

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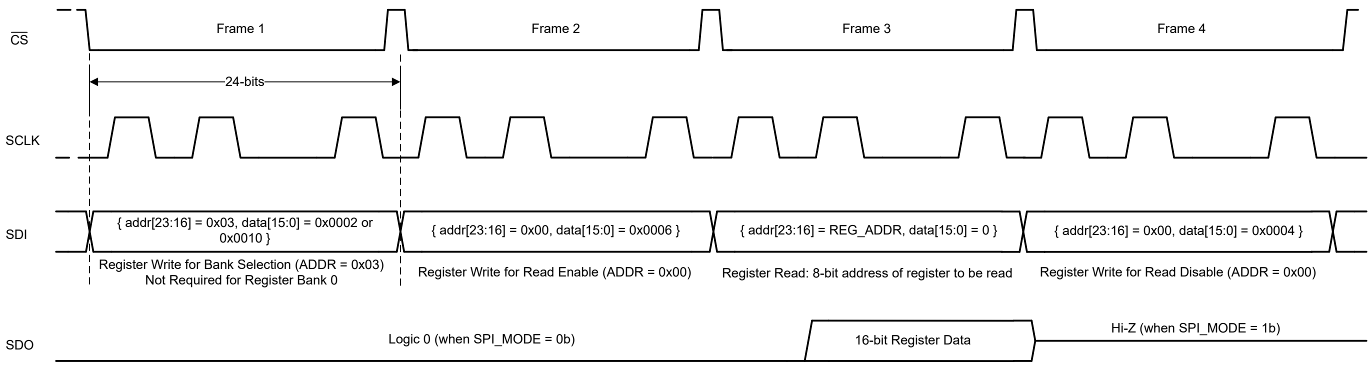

Figure 7-7. Register Read

7.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration

Figure 7-8 shows a typical connection diagram showing multiple devices in a daisy-chain topology.

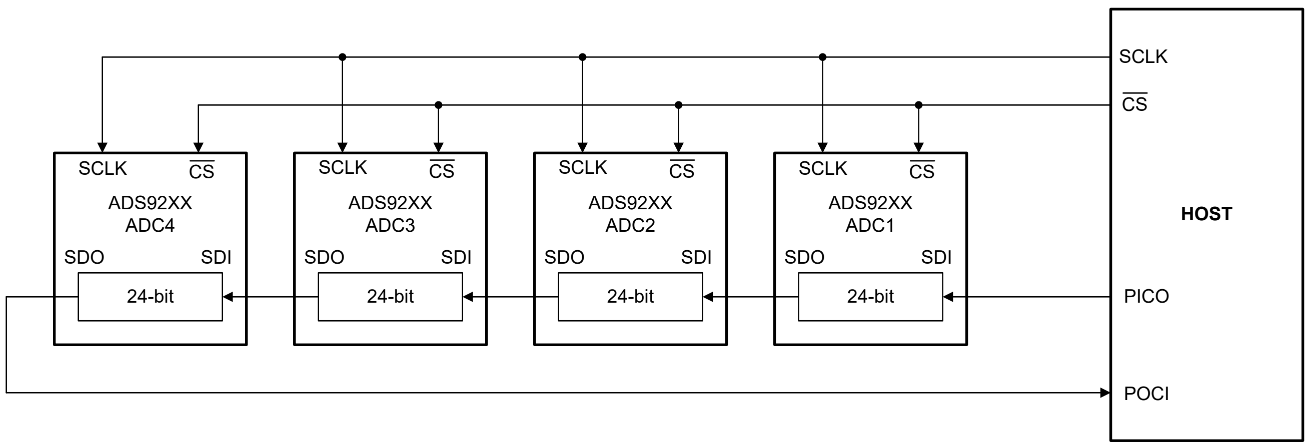

Figure 7-8. Daisy-Chain Connections for SPI Configuration

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and are controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller, the SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

The daisy-chain mode must be enabled after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LENGTH register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain, excluding ADC1. In Figure 7-8, the DAISY_CHAIN_LENGTH is 3.

7.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain configuration requires N × 24 SCLKs in one SPI frame. Register writes in a daisy-chain configuration containing four ADCs, as shown in Figure 7-8, requires 96 SCLKs.

The daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LENGTH field to enable daisy-chain mode. The waveform in Figure 7-9 must be repeated N times, where N is the number of ADCs in the daisy-chain. Figure 7-10 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

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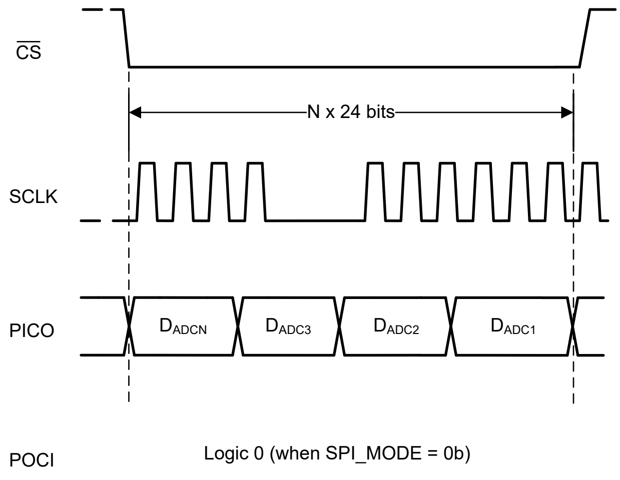

Figure 7-9. Register Write With Daisy-Chain

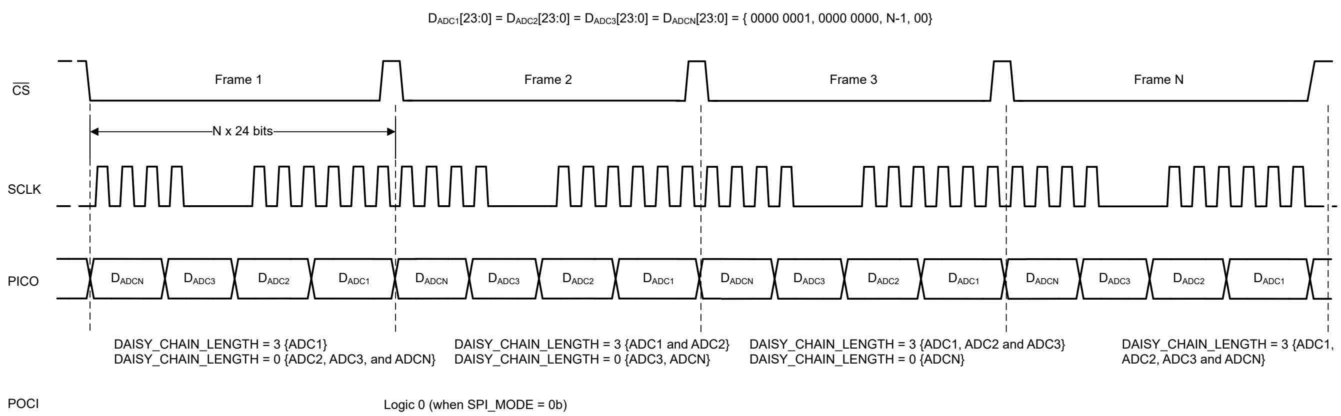

Figure 7-10. Register Write to Configure Daisy-Chain Length

7.5.3.2 Register Read With Daisy-Chain

Figure 7-11 illustrates an SPI waveform for reading registers in daisy-chain configuration. Steps for reading registers from N ADCs connected in daisy-chain are:

1. Register read is enabled by writing to the following registers:
   a. Write to PAGE_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller can read register data by:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N times (0xFE, 0x00, 8-bit register address)
   b. N × 24-bit SPI frame to read out register data: N times (0xFF, 0xFF, 0xFF)

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

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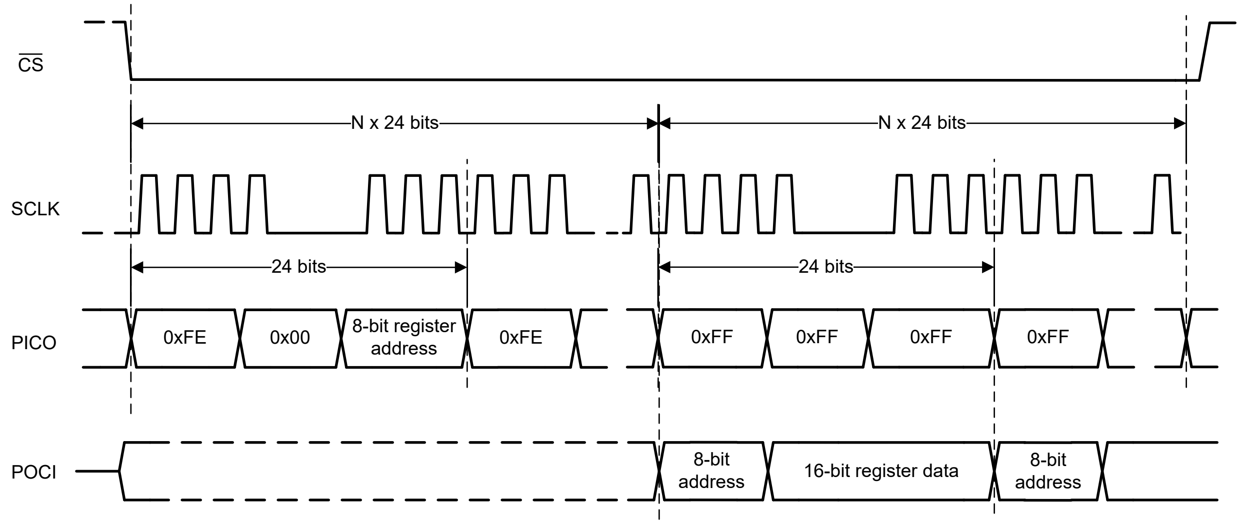

Figure 7-11. Register Read With Daisy-Chain

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7.6 Register Map

7.6.1 Register Bank 0

Figure 7-12. Register Bank 0 Map

<table>
<tr><th>ADD</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00h</td><td colspan="13">RESERVED</td><td>SPI_MODE</td><td>SPI_RD_EN</td><td>SOFT_RESET</td></tr>
<tr><td>01h</td><td colspan="9">RESERVED</td><td colspan="5">DAISY_CHAIN_LEN</td><td colspan="2">RESERVED</td></tr>
<tr><td>03h</td><td colspan="8">RESERVED</td><td colspan="8">REG_BANK_SEL</td></tr>
</table>

7.6.1.1 Register 0h (offset = 0h) [reset = 0h]

Figure 7-13. Register 0h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>SPI_MODE</td><td>SPI_RD_EN</td><td>SOFT_RESET</td></tr>
<tr><td colspan="5">W-0h</td><td>W-0h</td><td>W-0h</td><td>W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-14. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from default reset value.
2-2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1-1	SPI_RD_EN	W	0h	Enable register read access 0 : Register read disabled. 1 : Register read enabled.
0-0	SOFT_RESET	W	0h	Software reset all registers to default values 0 : Normal operation 1 : Reset device registers

7.6.1.2 Register 1h (offset = 1h) [reset = 0h]

Figure 7-15. Register 1h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="5">DAISY_CHAIN_LEN</td><td colspan="2">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="5">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-16. Register 01 Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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Figure 7-16. Register 01 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-2	DAISY_CHAIN_LEN	R/W	0h	Configure the number of devices connected in daisy-chain for the configuration SPI interface. 0 : 1 device in daisy-chain 1 : 2 devices in daisy-chain 2 : 3 devices in daisy-chain 31 : 32 devices in daisy-chain
1-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.1.3 Register 3h (offset = 3h) [reset = 2h]

Figure 7-17. Register 3h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
REG_BANK_SEL							
R/W-2h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-18. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select Register Bank 0 2 : Select Register Bank 1 16 : Select Register Bank 2

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7.6.2 Register Bank 1

Figure 7-19. Register Bank 1 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
08h	RESERVED	TMP_REG_L8_3					TMP_REG_L8_2					TMP_REG_L8_1				
0Bh	RESERVED											TMP_REG_LB_1				
0Ch	RESERVED						TMP_REG_LC_1					RESERVED				
0Dh	RESERVED		DATA_FORMAT	TMP_REG_LD_2					TMP_REG_LD_1	RESERVED						
11h	RESERVED			TMP_REG_L11_5	TMP_REG_L11_4	TMP_REG_L11_3	TMP_REG_L11_2	RESERVED						TMP_REG_L11_1		
12h	RESERVED												XOR_EN	DATA_WIDTH		DATA_LANES
13h	RESERVED								RAMP_INC_CH0				TEST_PAT_MODE_CH0		TEST_PAT_EN_CH0	RESERVED
14h	TEST_PAT0_CH0															
15h	TEST_PAT1_CH0								TEST_PAT0_CH0							
16h	TEST_PAT1_CH0															
18h	RESERVED								RAMP_INC_CH1				TEST_PAT_MODE_CH1		TEST_PAT_EN_CH1	RESERVED
19h	TEST_PAT0_CH1															
1Ah	TEST_PAT1_CH1								TEST_PAT0_CH1							
1Bh	TEST_PAT1_CH1															
33h	RESERVED	TMP_REG_L33_4	TMP_REG_L33_3	RESERVED						TMP_REG_L33_2	RESERVED		TMP_REG_L33_1	RESERVED		
34h	RESERVED											TMP_REG_L34_3	RESERVED		TMP_REG_L34_2	TMP_REG_L34_1
50h	RESERVED	TMP_REG_L50_3					TMP_REG_L50_2					TMP_REG_L50_1				
51h	RESERVED	TMP_REG_L51_3					TMP_REG_L51_2					TMP_REG_L51_1				
52h	RESERVED						TMP_REG_L52_2					TMP_REG_L52_1				
C0h	DCLK_CFG2		DCLK_CFG4		DCLK_CFG1		RESERVED								PD_ADC	
C1h	RESERVED				PD_REF	RESERVED		DATA_RATE	RESERVED				DCLK_CFG3			

7.6.2.1 Register 8h (offset = 8h) [reset = 0h]

Figure 7-20. Register 8h

15	14	13	12	11	10	9	8
RESERVED	TMP_REG_L8_3					TMP_REG_L8_2	
R/W-0h	R/W-0h					R/W-0h	

7	6	5	4	3	2	1	0
TMP_REG_L8_2			TMP_REG_L8_1				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-21. Register 08 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
14-10	TMP_REG_L8_3	R/W	0h	Temporary register. 0 : Normal device operation.

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Figure 7-21. Register 08 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-5	TMP_REG_L8_2	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 8 : Use for 40-bit 1-lane mode. 10 : Use for 48-bit 1-lane mode.
4-0	TMP_REG_L8_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 4 : Use for 40-bit 1-lane, and 48-bit 1-lane modes.

7.6.2.2 Register Bh (offset = Bh) [reset = 0h]

Figure 7-22. Register Bh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			TMP_REG_LB_1				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-23. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
4-0	TMP_REG_LB_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 6 : Use for 40-bit 1-lane, and 40-bit 1-lane modes.

7.6.2.3 Register Ch (offset = Ch) [reset = 0h]

Figure 7-24. Register Ch

15	14	13	12	11	10	9	8
RESERVED						TMP_REG_LC_1	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
TMP_REG_LC_1			RESERVED				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-25. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
9-5	TMP_REG_LC_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 1 : Use for 40-bit 1-lane, and 48-bit 1-lane modes.
4-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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7.6.2.4 Register Dh (offset = Dh) [reset = 2002h]

Figure 7-26. Register Dh

15	14	13	12	11	10	9	8
RESERVED		DATA_FORMAT	TMP_REG_LD_2				
R/W-0h		R/W-1h	R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMP_REG_LD_1	RESERVED						
R/W-0h	R/W-2h						

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-27. Register 0D Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
13-13	DATA_FORMAT	R/W	1h	Select output data format for ADC conversion result. 0 : Straight binary 1 : 2's compliment
12-8	TMP_REG_LD_2	R/W	0h	Temporary register. Write 00000b for normal device operation. 0 : Normal device operation.
7-7	TMP_REG_LD_1	R/W	0h	Temporary register. 1 : Normal device operation.
6-0	RESERVED	R/W	2h	Reserved. Do not change from default reset value.

7.6.2.5 Register 11h (offset = 11h) [reset = A02h]

Figure 7-28. Register 11h

15	14	13	12	11	10	9	8
RESERVED			TMP_REG_L11_5	TMP_REG_L11_4	TMP_REG_L11_3	TMP_REG_L11_2	RESERVED
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TMP_REG_L11_1		
R/W-0h					R/W-2h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-29. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
12-12	TMP_REG_L11_5	R/W	0h	Temporary register. 0 : Normal device operation.
11-11	TMP_REG_L11_4	R/W	1h	Temporary register. 0 : Normal device operation.
10-10	TMP_REG_L11_3	R/W	0h	Temporary register. 0 : Normal device operation.
9-9	TMP_REG_L11_2	R/W	1h	Temporary register. 0 : Normal device operation.
8-3	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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Figure 7-29. Register 11 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	TMP_REG_L11_1	R/W	2h	Temporary register. Write 100b for normal device operation. 4 : Normal device operation.

7.6.2.6 Register 12h (offset = 12h) [reset = Ah]

Figure 7-30. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				XOR_EN	DATA_WIDTH		DATA_LANES
R/W-0h				R/W-1h	R/W-1h		R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-31. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
3-3	XOR_EN	R/W	1h	Enables XOR function on ADC conversion result. 0 : XOR function is disabled 1 : Data output corresponding to ADC conversion result is launched as {D[23:5] xor D[4], D[4]}
2-1	DATA_WIDTH	R/W	1h	Select the output data frame width. 0 : 20-bit output frame. Use with 2-lane output mode (DATA_LANES = 0). ADC A and ADC B data are output in 20-bit format on DOUTA and DOUTB respectively. 1 : 24-bit output frame. Use with 2-lane output mode (DATA_LANES = 0). ADC A and ADC B data are output in 24-bit format on DOUTA and DOUTB respectively. 2 : 40-bit output frame. Use with 1-lane output mode (DATA_LANES = 1). ADC A and ADC B data are output in 20-bit format. 3 : 48-bit output frame. Use with 1-lane output mode (DATA_LANES = 1). ADC A and ADC B data are output in 24-bit format.
0-0	DATA_LANES	R/W	0h	Select number of LVDS output lanes 0 : 2-lane mode. ADC A data is output on DOUTA LVDS pair and ADC B data is output on DOUTB LVDS pair. 1 : 1-lane mode. ADC A data followed by ADC B data are output on DOUTA LVDS pair.

7.6.2.7 Register 13h (offset = 13h) [reset = 0h]

Figure 7-32. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RAMP_INC_CH0				TEST_PAT_MODE_CH0		TEST_PAT_EN_CH0	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

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LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-33. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
7-4	RAMP_INC_CH0	R/W	0h	Increment value for the ramp pattern output. The output ramp will increment by N+1 where N is the value configured in this register.
3-2	TEST_PAT_MODE_CH0	R/W	0h	0 : Fixed pattern as configured in TEST_PAT0_CH0 register 1 : Fixed pattern as configured in TEST_PAT1_CH0 register 2 : Ramp output 3 : Alternate fixed pattern output as configured in TEST_PAT0_CH0 and TEST_PAT1_CH0 registers
1-1	TEST_PAT_EN_CH0	R/W	0h	Enable digital test pattern for data for data corresponding to channel 1, 2, 3, and 4. 0 : Normal operation. ADC data will be launched on the data interface. 1 : Digital test pattern will be launched corresponding to channels 1, 2, 3, and 4 on the data interface.
0-0	RESERVED	R/W	0h	Reserved bit. Do not change from default reset value.

7.6.2.8 Register 14h (offset = 14h) [reset = 0h]

Figure 7-34. Register 14h

15	14	13	12	11	10	9	8
TEST_PAT0_CH0[23:8]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT0_CH0[23:8]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-35. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_CH0[23:8]	R/W	0h	Test pattern 0 for channel 0.

7.6.2.9 Register 15h (offset = 15h) [reset = 0h]

Figure 7-36. Register 15h

15	14	13	12	11	10	9	8
TEST_PAT1_CH0[23:16]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT0_CH0[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

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Figure 7-37. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_CH0[23:16]	R/W	0h	Test pattern 1 for channel 0.
7-0	TEST_PAT0_CH0[7:0]	R/W	0h	Test pattern 0 for channel 0.

7.6.2.10 Register 16h (offset = 16h) [reset = 0h]

Figure 7-38. Register 16h

15	14	13	12	11	10	9	8
TEST_PAT1_CH0[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT1_CH0[15:0]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-39. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_CH0[15:0]	R/W	0h	Test pattern 1 for channel 0.

7.6.2.11 Register 18h (offset = 18h) [reset = 0h]

Figure 7-40. Register 18h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC_CH1				TEST_PAT_MODE_CH1		TEST_PAT_EN_CH1	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-41. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
7-4	RAMP_INC_CH1	R/W	0h	Increment value for the ramp pattern output. The output ramp will increment by N+1 where N is the value configured in this register.
3-2	TEST_PAT_MODE_CH1	R/W	0h	0 : Fixed pattern as configured in TEST_PAT0_CH1 register 1 : Fixed pattern as configured in TEST_PAT1_CH1 register 2 : Ramp output 3 : Alternate fixed pattern output as configured in TEST_PAT0_CH1 and TEST_PAT1_CH1 registers

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Figure 7-41. Register 18 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-1	TEST_PAT_EN_CH1	R/W	0h	Enable digital test pattern for data corresponding to channels 5, 6, 7, and 8. 0 : Normal operation. ADC data will be launched on the data interface. 1 : Digital test pattern will be launched corresponding to channels 5, 6, 7, and 8 on the data interface.
0-0	RESERVED	R/W	0h	Reserved bit. Do not change from default reset value.

7.6.2.12 Register 19h (offset = 19h) [reset = 0h]

Figure 7-42. Register 19h

15	14	13	12	11	10	9	8
TEST_PAT0_CH1[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_CH1[23:8]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-43. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_CH1[23:8]	R/W	0h	Test pattern 0 for channel 1.

7.6.2.13 Register 1Ah (offset = 1Ah) [reset = 0h]

Figure 7-44. Register 1Ah

15	14	13	12	11	10	9	8
TEST_PAT1_CH1[23:16]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_CH1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-45. Register 1A Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_CH1[23:16]	R/W	0h	Test pattern 1 for channel 1.
7-0	TEST_PAT0_CH1[7:0]	R/W	0h	Test pattern 0 for channel 1.

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7.6.2.14 Register 1Bh (offset = 1Bh) [reset = 0h]

Figure 7-46. Register 1Bh

15	14	13	12	11	10	9	8
TEST_PAT1_CH1[15:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT1_CH1[15:0]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-47. Register 1B Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_CH1[15:0]	R/W	0h	Test pattern 1 for channel 1.

7.6.2.15 Register 33h (offset = 33h) [reset = 0h]

Figure 7-48. Register 33h

15	14	13	12	11	10	9	8
RESERVED	TMP_REG_L33_4	TMP_REG_L33_3	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TMP_REG_L33_2	RESERVED		TMP_REG_L33_1	RESERVED		
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-49. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
14-14	TMP_REG_L33_4	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 1 : Use for 40-bit 1-lane, and 48-bit 1-lane modes.
13-13	TMP_REG_L33_3	R/W	0h	Temporary register in the user address space.Write 1b to this register for normal device operation. 0 : Not recommended 1 : Normal device operation
12-7	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
6-6	TMP_REG_L33_2	R/W	0h	Temporary register in the user address space.Write 1b to this register for normal device operation. 0 : Not recommended. 1 : Normal device operation.
5-4	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
3-3	TMP_REG_L33_1	R/W	0h	Temporary register in the user address space.Write 1b to this register for normal device operation. 0 : Not recommended. 1 : Normal device operation.
2-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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7.6.2.16 Register 34h (offset = 34h) [reset = 0h]

Figure 7-50. Register 34h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TMP_REG_L34_3	RESERVED		TMP_REG_L34_2	TMP_REG_L34_1
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-51. Register 34 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
4-4	TMP_REG_L34_3	R/W	0h	Temporary register. 0 : Not recommended. 1 : Recommended. Normal device operation.
3-2	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
1-1	TMP_REG_L34_2	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 1 : Use for 48-bit 1-lane, and 40-bit 1-lane modes.
0-0	TMP_REG_L34_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 1 : Use for 40-bit 1-lane, and 48-bit 1-lane modes.

7.6.2.17 Register 50h (offset = 50h) [reset = 0h]

Figure 7-52. Register 50h

15	14	13	12	11	10	9	8
RESERVED	TMP_REG_L50_3					TMP_REG_L50_2	
R/W-0h	R/W-0h					R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMP_REG_L50_2			TMP_REG_L50_1				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-53. Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
14-10	TMP_REG_L50_3	R/W	0h	Temporary register. Write 00000b for normal device operation. 0 : Use for 20-bit 2-lane, 24-bit 2-lane, and 40-bit 1-lane modes. 10 : Use for 48-bit 1-lane mode.
9-5	TMP_REG_L50_2	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 6 : Use for 40-bit 1-lane mode, and 48-bit 1-lane modes.
4-0	TMP_REG_L50_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 4 : Use for 40-bit 1-lane mode, and 48-bit 1-lane modes.

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7.6.2.18 Register 51h (offset = 51h) [reset = 0h]

Figure 7-54. Register 51h

15	14	13	12	11	10	9	8
RESERVED	TMP_REG_L51_3					TMP_REG_L51_2	
R/W-0h	R/W-0h					R/W-0h	

7	6	5	4	3	2	1	0
TMP_REG_L51_2			TMP_REG_L51_1				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-55. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
14-10	TMP_REG_L51_3	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 4 : Use for 40-bit 1-lane mode, and 48-bit 1-lane modes.
9-5	TMP_REG_L51_2	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 4 : Use for 40-bit 1-lane mode, and 48-bit 1-lane modes.
4-0	TMP_REG_L51_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 4 : Use for 40-bit 1-lane, and 48-bit 1-lane modes.

7.6.2.19 Register 52h (offset = 52h) [reset = 0h]

Figure 7-56. Register 52h

15	14	13	12	11	10	9	8
RESERVED						TMP_REG_L52_2	
R/W-0h						R/W-0h	

7	6	5	4	3	2	1	0
TMP_REG_L52_2			TMP_REG_L52_1				
R/W-0h			R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-57. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
9-5	TMP_REG_L52_2	R/W	0h	Temporary register. Write 00000b for normal device operation. 0 : Normal device operation.
4-0	TMP_REG_L52_1	R/W	0h	Temporary register. Write 00000b for normal device operation. 0 : Normal device operation.

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7.6.2.20 Register C0h (offset = C0h) [reset = 0h]

Figure 7-58. Register C0h

15	14	13	12	11	10	9	8
DCLK_CFG2		DCLK_CFG4		DCLK_CFG1		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

7	6	5	4	3	2	1	0
RESERVED						PD_ADC	
R/W-0h						R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-59. Register C0 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DCLK_CFG2	R/W	0h	Data clock configuration 2. 1 : Normal device operation.
13-12	DCLK_CFG4	R/W	0h	Data clock configuration 4. 0 : Use for 24-bit 2-lane, and 20-bit 2-lane modes. 1 : Use for 48-bit 1-lane, and 40-bit 1-lane modes.
11-10	DCLK_CFG1	R/W	0h	Data clock configuration 1. 0 : Use for 40-bit 1-lane mode. 1 : Use for 24-bit 2-lane, 20-bit 2-lane, and 48-bit 1-lane modes.
9-2	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
1-0	PD_ADC	R/W	0h	Power-down control for ADC channels 0 : Normal device operation. 1 : ADC A power down. 2 : ADC B power down. 3 : ADC A and ADC B power down.

7.6.2.21 Register C1h (offset = C1h) [reset = 0h]

Figure 7-60. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED		DATA_RATE
R/W-0h				R/W-0h	R/W-0h		R/W-0h

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	DCLK_CFG3			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-61. Register C1 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
11-11	PD_REF	R/W	0h	ADC reference selection 0 : Internal reference enabled 1 : Internal reference disabled. Connect external reference at REFIO pin.
10-9	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
8-8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double Data Rate (DDR) 1 : Single Data Rate (SDR)

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Figure 7-61. Register C1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
3-0	DCLK_CFG3	R/W	0h	Data clock configuration 3. 8 : Use for 24-bit 2-lane, and 48-bit 1-lane modes. 9 : Use for 20-bit 2-lane, and 40-bit 1-lane modes.

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7.6.3 Register Bank 2

Figure 7-62. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	RESERVED							TMP_REG_L1C_1	RESERVED							
22h	RESERVED			TMP_REG_L22_2	TMP_REG_L22_1	RESERVED										
33h	RESERVED					TMP_REG_L33_1	RESERVED									
52h	RESERVED														TMP_REG_L52_2	TMP_REG_L52_1
53h	RESERVED															TMP_REG_L53_1
54h	TMP_REG_L54_5	TMP_REG_L54_4	TMP_REG_L54_3	TMP_REG_L54_2	TMP_REG_L54_1	RESERVED										
56h	RESERVED	TMP_REG_L56_3	TMP_REG_L56_2	TMP_REG_L56_1	RESERVED											
57h	RESERVED				TMP_REG_L57_1	RESERVED										
60h	TMP_REG_L60_1	RESERVED														

7.6.3.1 Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-63. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED							TMP_REG_L1C_1
R/W-0h							R/W-0h

7	6	5	4	3	2	1	0
RESERVED							
R/W-0							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-64. Register 1C Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
8-8	TMP_REG_L1C_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
7-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.2 Register 22h (offset = 22h) [reset = 0h]

Figure 7-65. Register 22h

15	14	13	12	11	10	9	8
RESERVED			TMP_REG_L22_2	TMP_REG_L22_1	RESERVED		
R/W-0h			R/W-0h	R/W-0h	R/W-0h		

7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

ADVANCE INFORMATION

ADVANCE INFORMATION

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-66. Register 22 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
12-12	TMP_REG_L22_2	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
11-11	TMP_REG_L22_1	R/W	0h	Temporary Register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
10-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.3 Register 33h (offset = 33h) [reset = 0h]

Figure 7-67. Register 33h

15	14	13	12	11	10	9	8
RESERVED					TMP_REG_L33_1	RESERVED	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-68. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
10-10	TMP_REG_L33_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
9-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.4 Register 52h (offset = 52h) [reset = 0h]

Figure 7-69. Register 52h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TMP_REG_L52_2	TMP_REG_L52_1
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-70. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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Figure 7-70. Register 52 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-1	TMP_REG_L52_2	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
0-0	TMP_REG_L52_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation

7.6.3.5 Register 53h (offset = 53h) [reset = 0h]

Figure 7-71. Register 53h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
R/W-0h							TMP_REG_L53_1
R/W-0h							R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-72. Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
0-0	TMP_REG_L53_1	R/W	0h	Temporary register. 0 : Normal device operation 1 : Not recommended

7.6.3.6 Register 54h (offset = 54h) [reset = 0h]

Figure 7-73. Register 54h

15	14	13	12	11	10	9	8
TMP_REG_L54_5	TMP_REG_L54_4	TMP_REG_L54_3	TMP_REG_L54_2	TMP_REG_L54_1	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-74. Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	TMP_REG_L54_5	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 48-bit 1-lane modes. 1 : Use for 40-bit 1-lane, and 20-bit 2-lane modes.
14-14	TMP_REG_L54_4	R/W	0h	Temporary register. Write 0b for normal device operation. 0 : Normal device operation 1 : Not recommended

ADVANCE INFORMATION

Figure 7-74. Register 54 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-13	TMP_REG_L54_3	R/W	0h	Temporary register. Write 0b for normal device operation. 0 : Normal device operation 1 : Not recommended
12-12	TMP_REG_L54_2	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 48-bit 1-lane modes. 1 : Use for 40-bit 1-lane, and 20-bit 2-lane modes.
11-11	TMP_REG_L54_1	R/W	0h	Temporary register. 0 : Use for 24-bit 2-lane, and 48-bit 1-lane modes. 1 : Use for 40-bit 1-lane, and 20-bit 2-lane modes.
10-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.7 Register 56h (offset = 56h) [reset = 0h]

Figure 7-75. Register 56h

15	14	13	12	11	10	9	8
RESERVED	TMP_REG_L56_3	TMP_REG_L56_2	TMP_REG_L56_1	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-76. Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
14-14	TMP_REG_L56_3	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
13-13	TMP_REG_L56_2	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
12-12	TMP_REG_L56_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
11-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.8 Register 57h (offset = 57h) [reset = 0h]

Figure 7-77. Register 57h

15	14	13	12	11	10	9	8
RESERVED				TMP_REG_L57_1	RESERVED		
R/W-0h				R/W-0h	R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

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LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-78. Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from default reset value.
11-11	TMP_REG_L57_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
10-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

7.6.3.9 Register 60h (offset = 60h) [reset = 0h]

Figure 7-79. Register 60h

15	14	13	12	11	10	9	8
TMP_REG_L60_1	RESERVED						
R/W-0h	R/W-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-80. Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	TMP_REG_L60_1	R/W	0h	Temporary register. Write 1b for normal device operation. 0 : Not recommended 1 : Normal device operation
14-0	RESERVED	R/W	0h	Reserved. Do not change from default reset value.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The integrated ADC driver, low-latency, high-speed, low AC and DC errors, and low temperature drift make the ADS921x a high-performance solution for applications where precision measurements with low-latency are required. The following section gives an example circuit and recommendations for using the ADS921x device family in a data acquisition (DAQ) system.

8.2 Typical Applications

8.2.1 Data Acquisition (DAQ) Circuit for ≤20-kHz Input Signal Bandwidth

Figure 8-1 shows a 2-channel solution with minimum external components. This solution significantly reduces solution size by driving the ADS921x with the 2-channel, fully differential amplifier (FDA) THS4552.

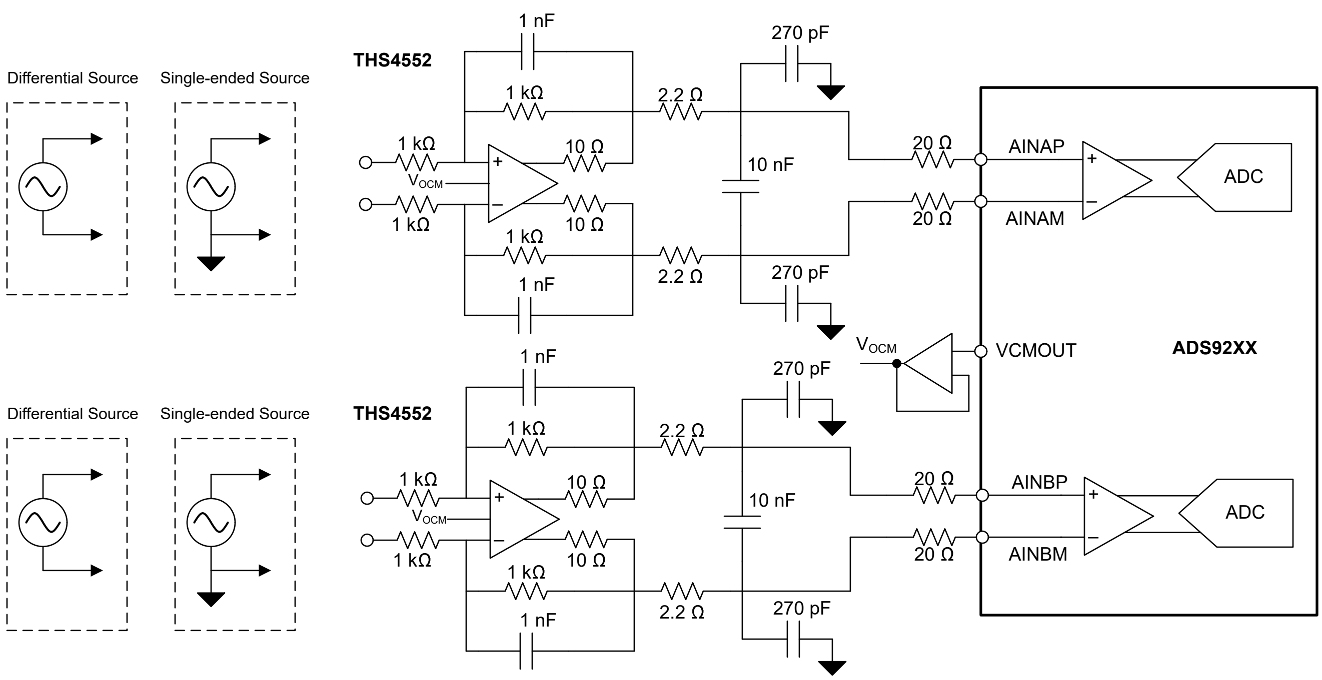

Figure 8-1. Data Acquisition (DAQ) Circuit for ≤20-kHz Input Signal Bandwidth

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Parameters

PARAMETER	VALUE
SNR	≥ 92 dB
THD	≤ –110 dB
Input signal frequency	≤ 20 kHz

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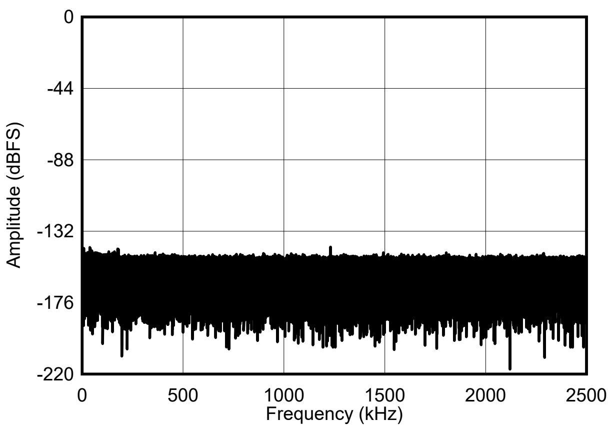
8.2.1.2 Detailed Design Procedure

The procedure discussed in this section can be used for any ADS921x application circuit.

- All ADS921x applications require the supply decoupling as given in the *Power Supply Recommendations* section.
- The values given in this section must meet the maximum throughput and input signal frequency design requirements given. A lower bandwidth solution can be used in cases where lower noise performance is required.

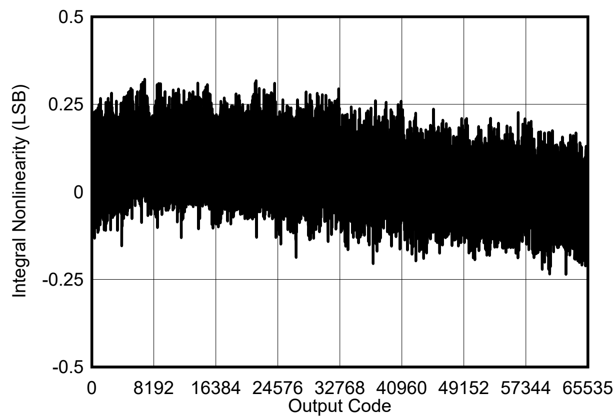
8.2.1.3 Application Curves

Figure 8-2 and Figure 8-3 show the SNR and INL performance for the circuit in Figure 8-1, respectively.



f_{IN} = 2 kHz, SNR = 94.5 dB, THD = –120 dB

Figure 8-2. Typical FFT at 5 MSPS/Channel: ADS9217



f_{IN} = 2 kHz, INL = ±0.3 LSB

Figure 8-3. Typical INL at 5 MSPS/Channel: ADS9217

ADVANCE INFORMATION

8.2.2 Data Acquisition (DAQ) Circuit for ≤100-kHz Input Signal Bandwidth

Figure 8-1 shows a 2-channel solution with minimum external components. This solution significantly reduces solution size by driving the ADS921x with the 2-channel, fully differential amplifier (FDA) THS4552.

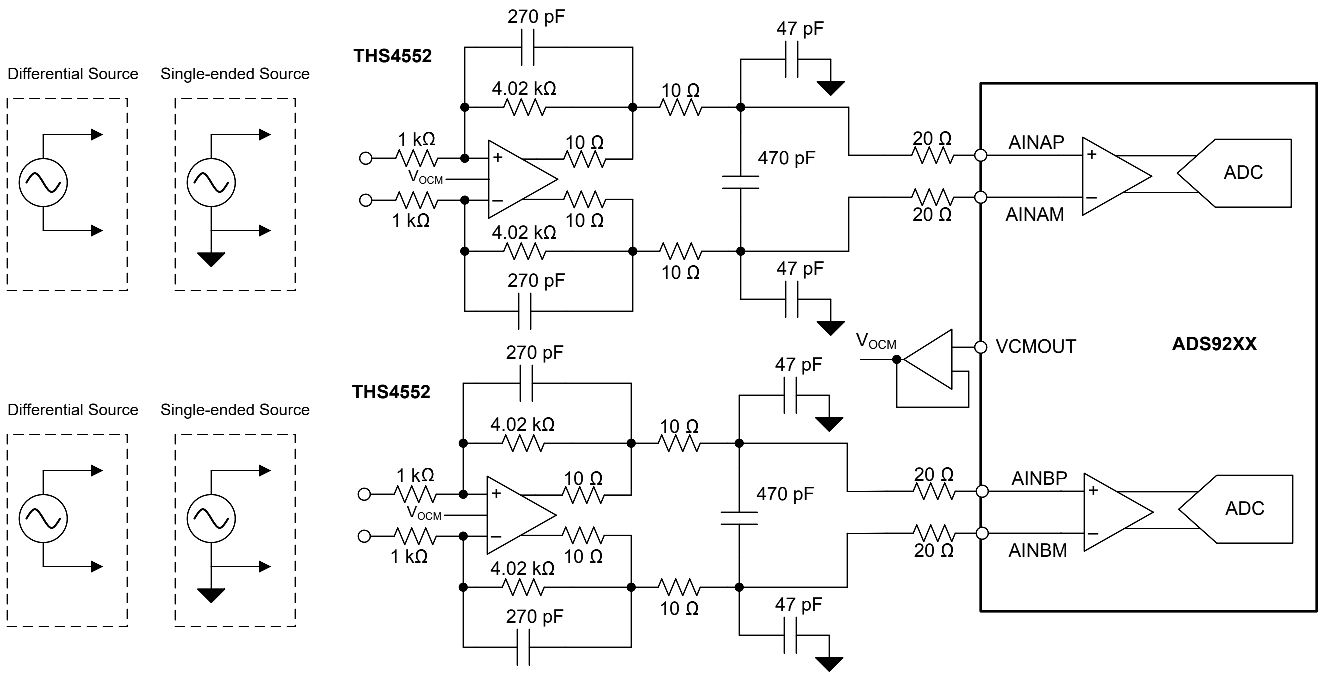


Figure 8-4. Data Acquisition (DAQ) Circuit for ≤100-kHz Input Signal Bandwidth

8.2.2.1 Design Requirements

Table 8-2 lists the parameters for this typical application.

Table 8-2. Design Parameters

PARAMETER	VALUE
SNR	≥ 91 dB
THD	≤ –110 dB
Input signal frequency	≤ 100 kHz

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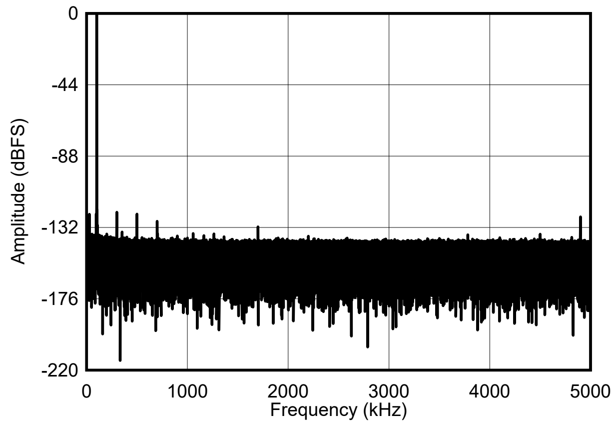
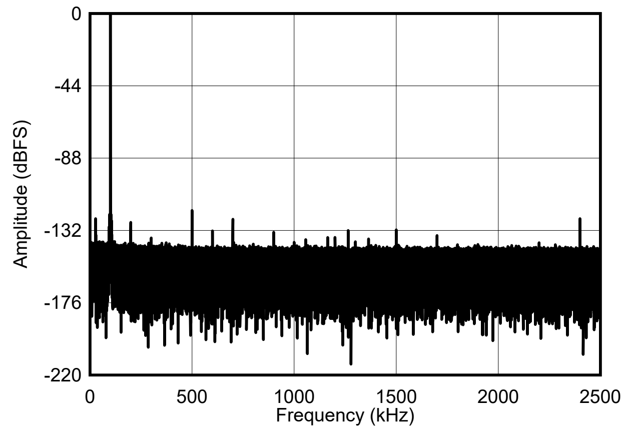
8.2.2.2 Application Curves

Figure 8-5 and Figure 8-6 show the FFT plots for the circuit in Figure 8-4.



f_{IN} = 100 kHz, SNR = 92 dB, THD = –117 dB

Figure 8-5. Typical FFT at 10 MSPS/Channel: ADS9218



f_{IN} = 100 kHz, SNR = 92 dB, THD = –117 dB

Figure 8-6. Typical FFT at 5 MSPS/Channel: ADS9217

8.2.3 Data Acquisition (DAQ) Circuit for ≤1-MHz Input Signal Bandwidth

Figure 8-1 shows a 2-channel solution with minimum external components. This solution significantly reduces solution size by driving the ADS9218 with the THS4541, which enables low-distortion performance with low power over wide signal bandwidth.

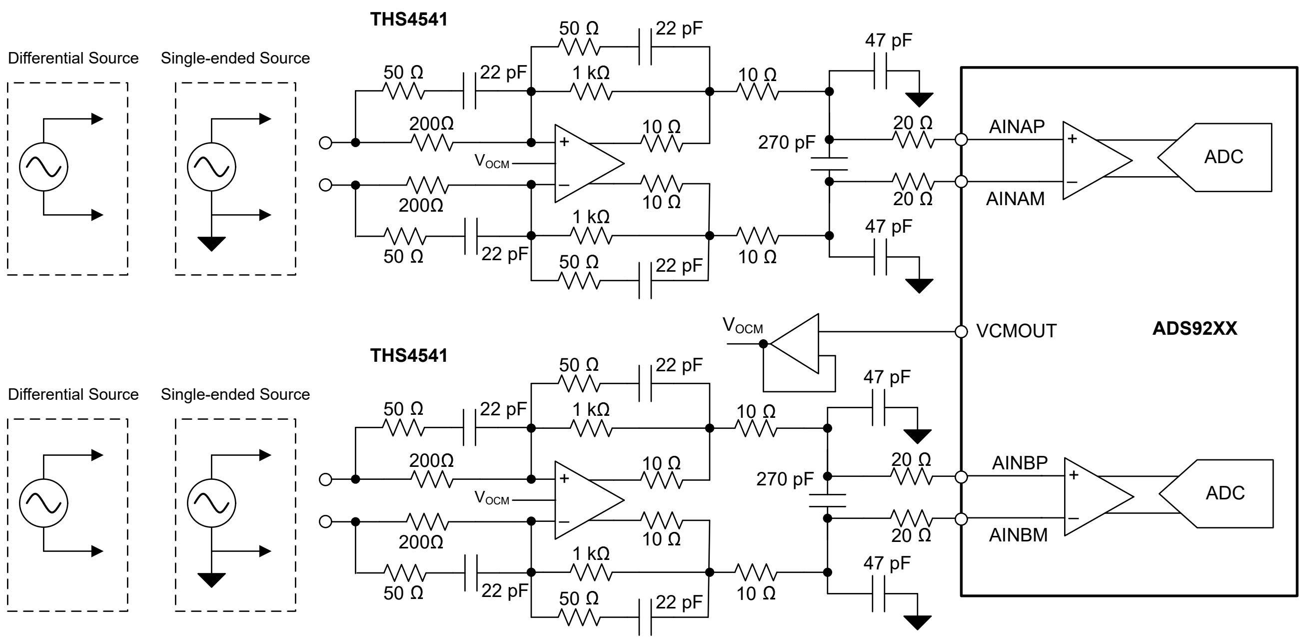


Figure 8-7. Data Acquisition (DAQ) Circuit for ≤1-MHz Input Signal Bandwidth

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8.2.3.1 Design Requirements

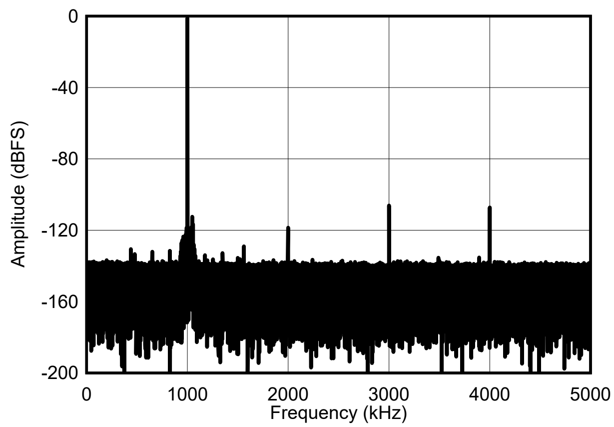
Table 8-3 lists the parameters for this typical application.

Table 8-3. Design Parameters

PARAMETER	VALUE
SNR	≥ 80 dB
THD	≤ –100 dB
Input signal frequency	≤ 1 MHz

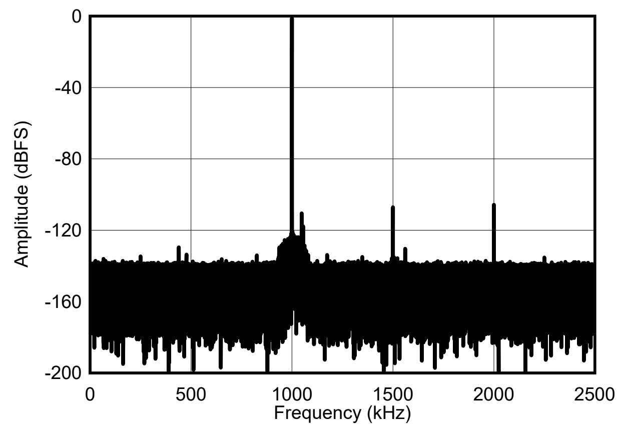
8.2.3.2 Application Curves

Figure 8-8 and Figure 8-9 show the FFT plots for the circuit in Figure 8-7.



f_{IN} = 1 MHz, SNR = 90.6 dB, THD = –104 dB

Figure 8-8. Typical FFT at 10 MSPS/Channel: ADS9218



f_{IN} = 1 MHz, SNR = 90.5 dB, THD = –104.2 dB

Figure 8-9. Typical FFT at 5 MSPS/Channel: ADS9217

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8.3 Power Supply Recommendations

The ADS921x has three independent power supplies, AVDD_5V, AVDD_1V8, and DVDD_1V8. The AVDD_5V supply provides power to the ADC driver. The AVDD_1V8 provides power to the analog circuits. The DVDD_1V8 supply provides power to the digital interface. The AVDD_5, AVDD_1V8, and DVDD_1V8 supplies can be set independently to voltages within the permissible range. Figure 8-10 shows how to decouple the power supplies.

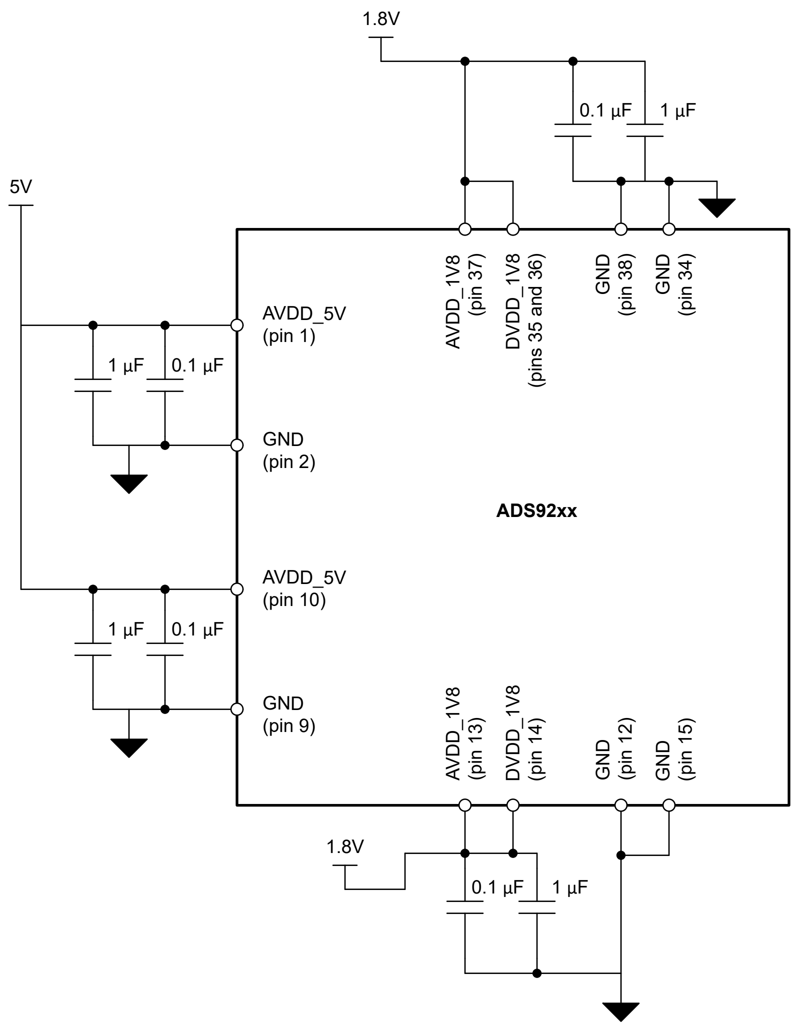

Figure 8-10. Power-Supply Decoupling

ADVANCE INFORMATION

ADVANCE INFORMATION

8.4 Layout

8.4.1 Layout Guidelines

Figure 8-11 shows a board layout example for the ADS921x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 0.1-µF ceramic bypass capacitors in close proximity to the analog (AVDD_5V and AVDD_1V8), and digital (DVDD_1V8) power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors. Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

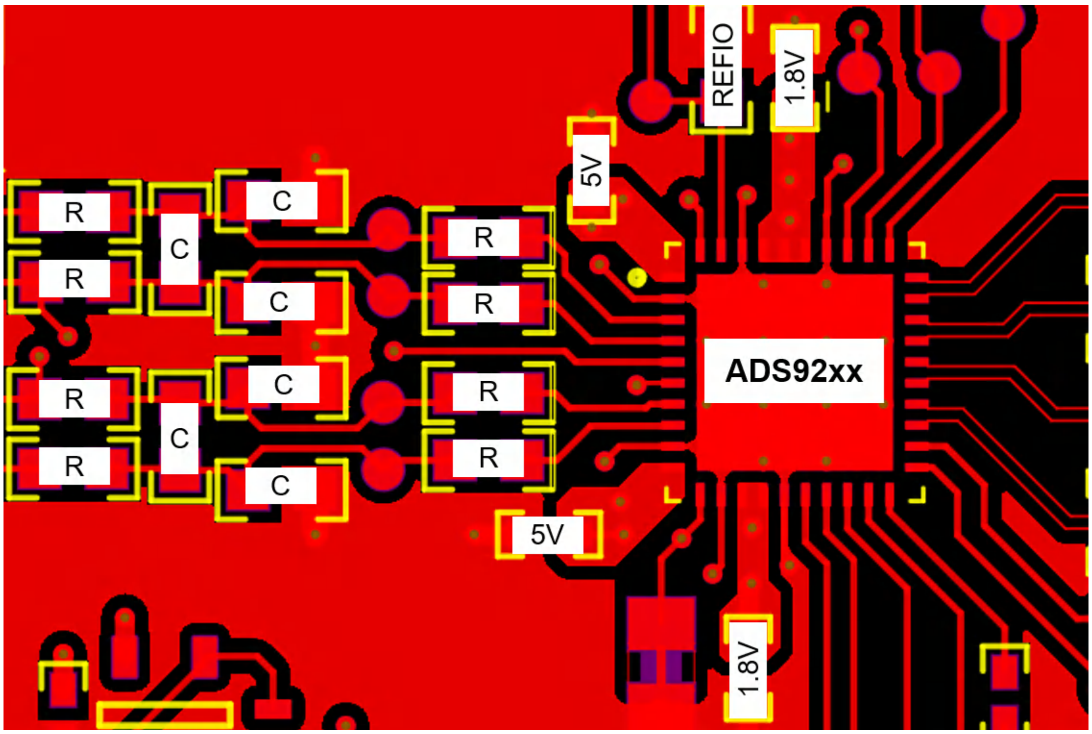

Figure 8-11. Example Layout

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *REF70 2 ppm/°C Maximum Drift, 0.23 ppm$_{p\text{-}p}$ 1/f Noise, Precision Voltage Reference* data sheet
- Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier* data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

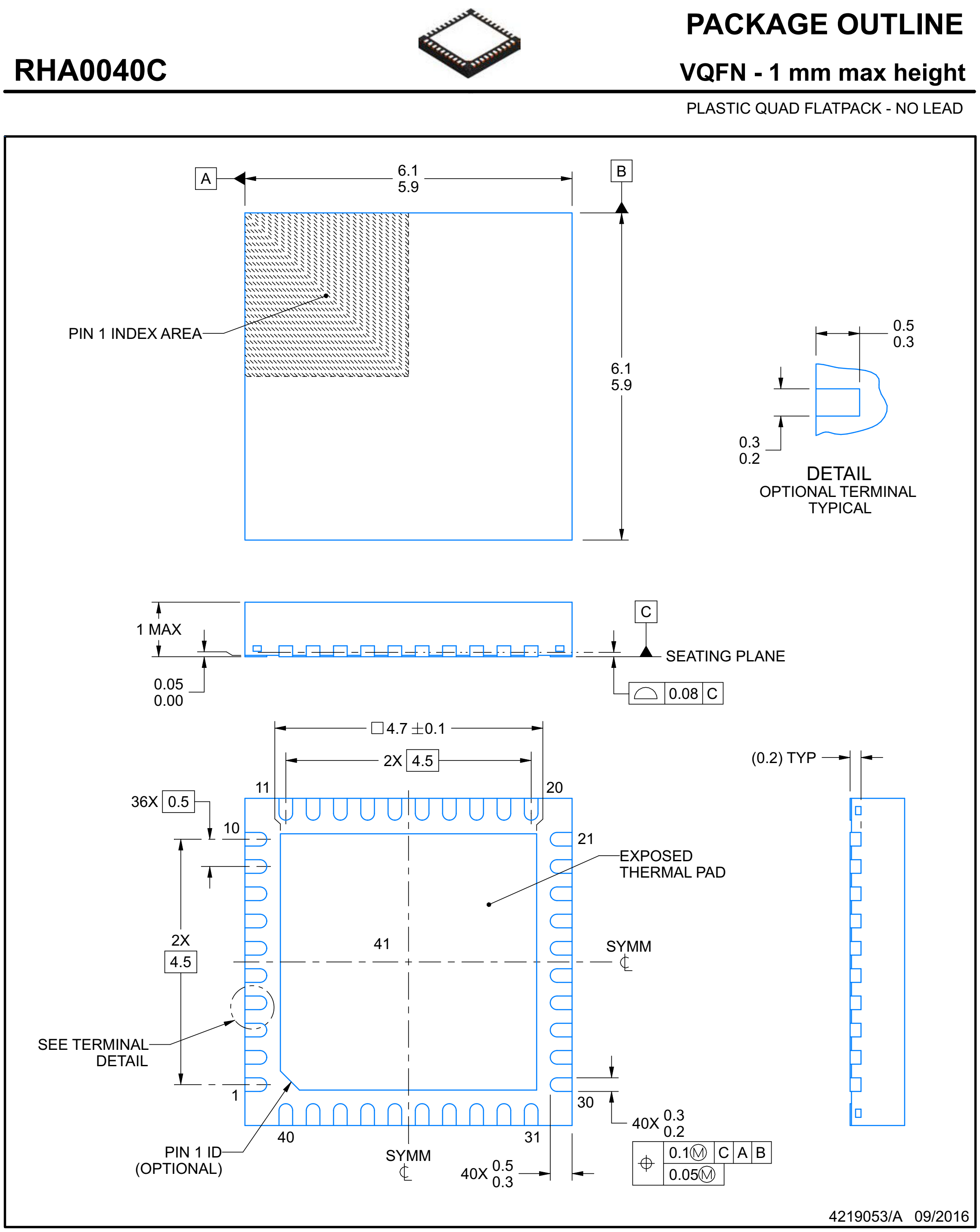
TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

10.1 Mechanical Data



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

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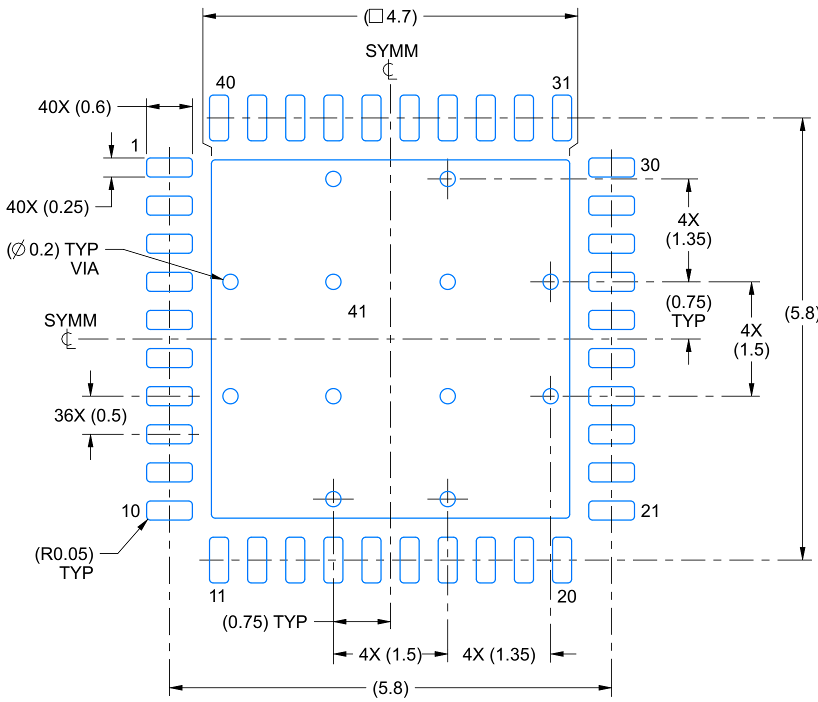
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

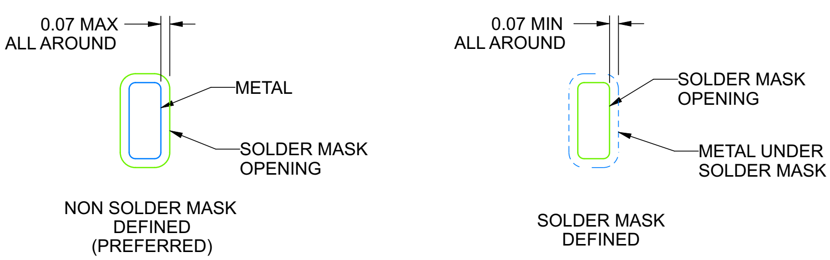
RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4219053/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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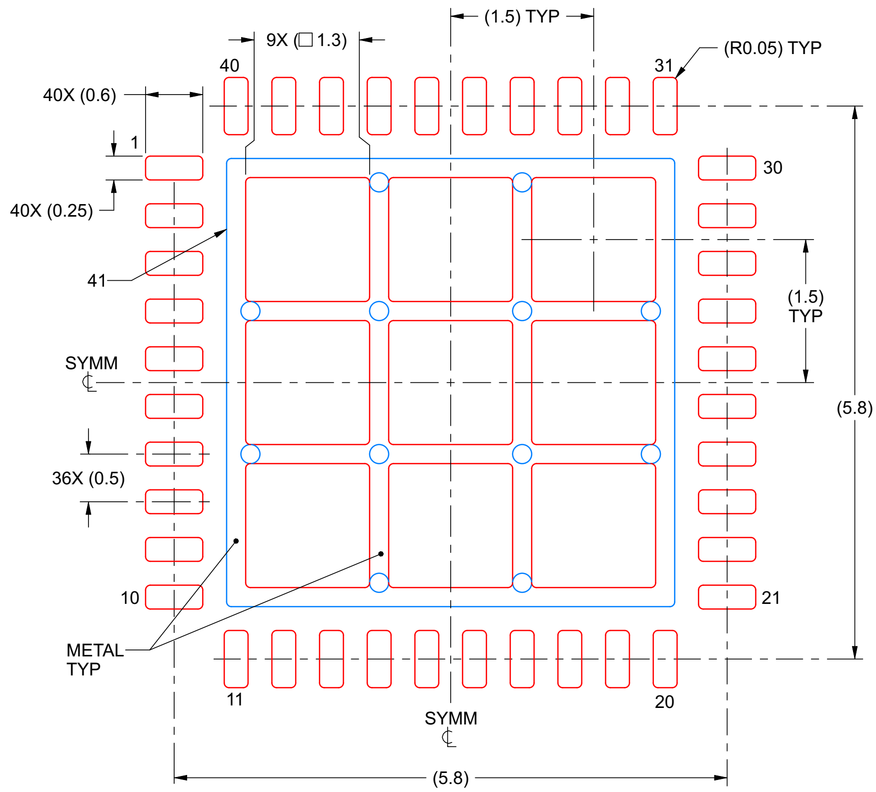
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PADS9218RHAT	ACTIVE	VQFN	RHA	40	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

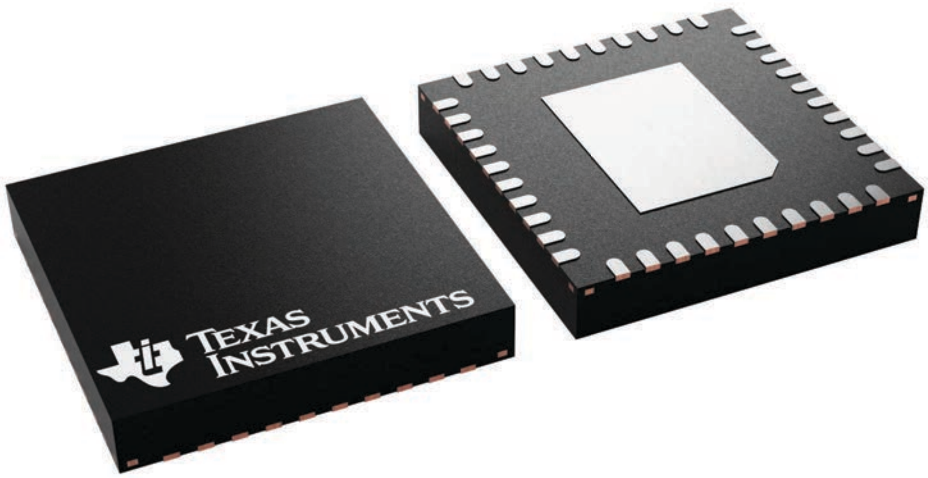
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

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