# ADS922x Dual, Simultaneous-Sampling, 16-Bit, 20MSPS SAR ADCs With Fully Differential ADC Input Driver

## 1 Features

- High-speed sampling rate: 20MSPS/ch
  - ADS9229: 20MSPS/ch, 230mW/ch
  - ADS9228: 10MSPS/ch, 146mW/ch
  - ADS9227: 5MSPS/ch, 95mW/ch
- 2-channel, simultaneous sampling
- Feature integration:
  - Integrated ADC driver
  - Integrated precision reference
  - Common-mode voltage output buffer
- High-performance:
  - 16-bit no missing codes
  - INL: ±0.3LSB, DNL: ±0.3LSB
  - SNR: 93.9dB
- Wide input bandwidth (–3dB):
  - ADS9229 and ADS9228: 90MHz
  - ADS9227: 45MHz
- Serial LVDS interface:
  - SDR and DDR output modes
  - Synchronous clock and data output
- Extended operating range: –40°C to +125°C

## 2 Applications

- Power analyzers
- Source measurement units (SMU)
- Marine equipment
- Servo drive position feedback
- DC power supplies, AC sources, electronic loads

## 3 Description

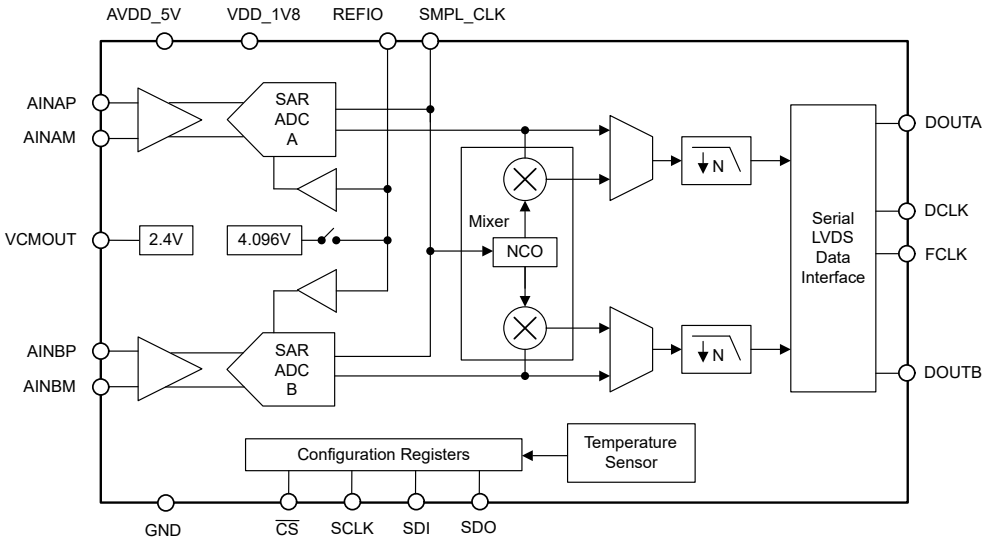
The ADS922x is a family of 16-bit, high-speed, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated driver for the ADC inputs. The integrated ADC driver simplifies the signal chain, reduces power consumption for precision applications, and supports high-frequency signals beyond 1MHz. By not requiring an external decoupling capacitor, the integrated ADC reference buffer is optimized for wide bandwidth applications.

The ADS922x uses a serial LVDS (SLVDS) data interface that enables high-speed digital interface while minimizing digital switching noise. Read the dual-channel ADC data using separate SLVDS outputs per ADC channel or one SLVDS output for both ADC channels.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| ADS9227 | RHA (VQFN, 40) | 6mm × 6mm |
| ADS9228 | | |
| ADS9229 | | |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Device Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Device Comparison Table**....3
**5 Pin Configuration and Functions**....4
**6 Specifications**....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 Thermal Information....6
6.4 Recommended Operating Conditions....7
6.5 Electrical Characteristics....8
6.6 Timing Requirements....10
6.7 Switching Characteristics....11
6.8 Timing Diagrams....12
6.9 Typical Characteristics: All Devices....15
6.10 Typical Characteristics: ADS9229....17
6.11 Typical Characteristics: ADS9228....18
6.12 Typical Characteristics: ADS9227....19
**7 Detailed Description**....20
7.1 Overview....20
7.2 Functional Block Diagram....20
7.3 Feature Description....21
7.4 Device Functional Modes....31
7.5 Programming....32
**8 Register Map**....36
8.1 Register Bank 0....36
8.2 Register Bank 1....39
8.3 Register Bank 2....54
**9 Application and Implementation**....55
9.1 Application Information....55
9.2 Typical Applications....55
9.3 Power Supply Recommendations....60
9.4 Layout....61
**10 Device and Documentation Support**....62
10.1 Documentation Support....62
10.2 Receiving Notification of Documentation Updates....62
10.3 Support Resources....62
10.4 Trademarks....62
10.5 Electrostatic Discharge Caution....62
10.6 Glossary....62
**11 Revision History**....63
**12 Mechanical, Packaging, and Orderable Information**....63


Copyright © 2025 Texas Instruments Incorporated

## 4 Device Comparison Table

| PART NUMBER | CHANNELS | RESOLUTION | SPEED |
|---|---|---|---|
| ADS9219 | 2 | 18 | 20MSPS |
| ADS9218 | | | 10MSPS |
| ADS9217 | | | 5MSPS |
| ADS9229 | | 16 | 20MSPS |
| ADS9228 | | | 10MSPS |
| ADS9227 | | | 5MSPS |
| ADS9119 | 1 | 18 | 20MSPS |
| ADS9118 | | | 10MSPS |
| ADS9117 | | | 5MSPS |
| ADS9129 | | 16 | 20MSPS |
| ADS9128 | | | 10MSPS |
| ADS9127 | | | 5MSPS |

Copyright © 2025 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

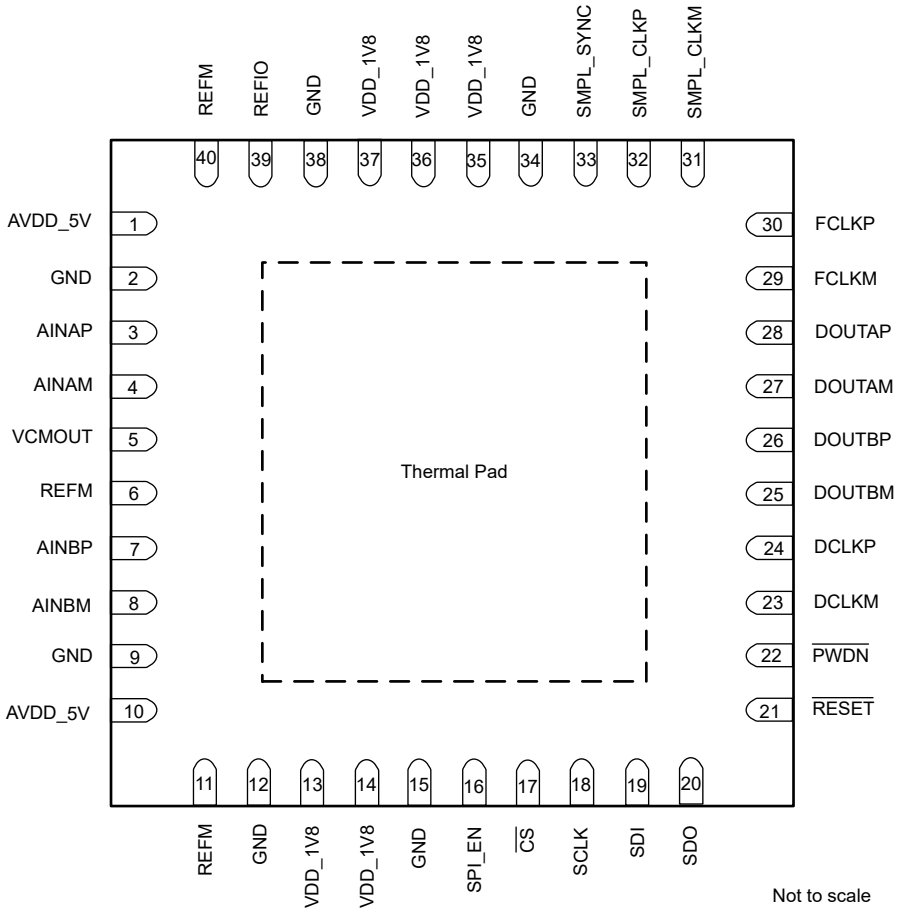



**Figure 5-1. RHA Package, 6mm × 6mm, 40-Pin VQFN (Top View)**

**Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AINAM | 4 | I | Negative analog input for ADC A. |
| AINAP | 3 | I | Positive analog input for ADC A. |
| AINBM | 8 | I | Negative analog input for ADC B. |
| AINBP | 7 | I | Positive analog input for ADC B. |
| AVDD_5V | 1, 10 | P | 5V analog power-supply pin. |
| $\overline{CS}$ | 17 | I | Chip-select input pin for the configuration interface; active low. |
| DCLKM | 23 | O | Negative differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver. |
| DCLKP | 24 | O | Positive differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver. |
| DOUTAM | 27 | O | Negative differential data output. Connect a 100Ω resistor between DOUTAP and DOUTAM close to the receiver.<br>Transmits ADC A data in 2-lane mode.<br>Transmits ADC A and ADC B data in 1-lane mode. |
| DOUTAP | 28 | O | Positive differential data output corresponding to ADC A. Connect a 100Ω resistor between DOUTAP and DOUTAM close to the receiver.<br>Transmits ADC A data in 2-lane mode.<br>Transmits ADC A and ADC B data in 1-lane mode. |


Copyright © 2025 Texas Instruments Incorporated

## Pin Functions (continued)

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DOUTBM | 25 | O | Negative differential data output corresponding to ADC B in 2-lane mode. Connect a 100Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode. |
| DOUTBP | 26 | O | Positive differential data output corresponding to ADC B in 2-lane mode. Connect a 100Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode. |
| FCLKM | 29 | O | Negative differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver. |
| FCLKP | 30 | O | Positive differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver. |
| GND | 2, 9, 12, 15, 34, 38 | P | Ground. |
| $\overline{\text{PWDN}}$ | 22 | I | Power-down control; active low. Connect to VDD_1V8 if unused. |
| REFIO | 39 | I/O | Internal reference voltage output. External reference voltage input. Connect a 10µF decoupling capacitor to REFM. |
| REFM | 6, 11, 40 | P | Reference ground. Connect to GND. |
| $\overline{\text{RESET}}$ | 21 | I | Reset input; active low. Connect to VDD_1V8 if unused. |
| SCLK | 18 | I | Serial clock input for the configuration interface. |
| SDI / $\overline{\text{EXTREF}}$ | 19 | I | SDI is a multifunction logic input; pin function is determined by the SPI_EN pin. SDI has an internal 100kΩ pulldown resistor to GND. SPI_EN = 0b: SDI is the logic input to select between the internal or external reference. Connect SDI to GND for the external reference. Connect SDI to VDD_1V8 for the internal reference. SPI_EN = 1b: Serial data input for the configuration interface |
| SDO | 20 | O | Serial data output for the configuration interface. |
| SMPL_CLKM | 31 | I | ADC sampling clock input. Negative differential input for the LVDS sampling clock. Connect this pin to GND for the CMOS sampling clock. |
| SMPL_CLKP | 32 | I | ADC sampling clock input. Positive differential input for the LVDS sampling clock. Clock input for the CMOS sampling clock. |
| SMPL_SYNC | 33 | I | Synchronization input for internal averaging filter.<br>Connect to GND if unused. See the *Synchronizing Multiple ADCs* section on how to use the SMPL_SYNC pin. |
| SPI_EN | 16 | I | Control to enable configuration of the SPI interface; active high.<br>Connect a pullup resistor to VDD_1V8 to keep the configuration interface enabled. Connect to GND if SPI configuration is unused. When SPI_EN = 0, select the reference voltage with the SDI/$\overline{\text{EXTREF}}$ pin. |
| Thermal Pad | — | P | Exposed thermal pad. Connect to GND. |
| VCMOUT | 5 | O | Common-mode voltage output. Use VCMOUT to set the common-mode voltage at the ADC inputs. Connect a 1µF decoupling capacitor to GND. |
| VDD_1V8 | 13, 14, 35, 36, 37 | P | 1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND. |

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

Copyright © 2025 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VDD_1V8 to GND | –0.3 | 2.1 | V |
| AVDD_5V to GND | –0.3 | 5.5 | V |
| AINAP, AINAM, AINBP, and AINBM to GND | GND – 0.3 | AVDD_5V + 0.3 | V |
| REFIO to REFM | REFM – 0.3 | AVDD_5V + 0.3 | V |
| Digital inputs to GND | GND – 0.3 | VDD_1V8 + 0.3 | V |
| REFM to GND | –0.3 | 0.3 | V |
| Input current to any pin except supply pins(2) | –10 | 10 | mA |
| Junction temperature, $T_J$ | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | –60 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10 mA or less.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins AINAP, AINAM, AINBP, and AINBM(1) | ±2000 | V |
| | | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1) | ±1000 | |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | ADS922x RHA (VQFN) 40 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 25.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 13.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 7.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.


Copyright © 2025 Texas Instruments Incorporated

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| AVDD_5V | Analog power supply AVDD_5V to GND | ADS9227 | 4.5 | 5 | 5.5 | V |
| | | ADS9228, ADS9229 | 4.75 | 5 | 5.25 | |
| VDD_1V8 | Power supply | VDD_1V8 to GND | 1.75 | 1.8 | 1.85 | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference voltage to the ADC | External reference | 4.076 | 4.096 | 4.116 | V |
| **ANALOG INPUTS** | | | | | | |
| $V_{IN}$ | Absolute input voltage | AINx(1) to GND | $V_{CM}$ – 1.6 | | $V_{CM}$ + 1.6 | V |
| FSR | Full-scale input range | (AINAP – AINAM) and (AINBP – AINBM) | –3.2 | | 3.2 | V |
| $V_{CM}$ | Common-mode input range(2) | (AINAP + AINAM) / 2 and (AINBP + AINBM) / 2 | $V_{CMOUT}$ – 0.07 | | $V_{CMOUT}$ + 0.07 | V |
| **TEMPERATURE RANGE** | | | | | | |
| $T_A$ | Ambient temperature | | –40 | 25 | 125 | °C |

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.
(2) ADC channel is powered down if the input common-mode voltage exceeds specifications.

Copyright © 2025 Texas Instruments Incorporated

## 6.5 Electrical Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9229, and ADS9228, and AVDD_5V = 4.5V to 5.5V for ADS9227, VDD_1V8 = 1.75V to 1.85V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | | |
| $I_B$ | Input bias current | | | 0.1 | | nA |
| | Input bias current thermal drift | $T_A$ = 0°C to 70°C | | 0.02 | | nA/°C |
| | | $T_A$ = –40°C to 125°C | | 0.1 | | |
| **DC PERFORMANCE** | | | | | | |
| | Resolution | No missing codes | | 16 | | Bits |
| DNL | Differential nonlinearity | | –0.9 | ±0.3 | 0.9 | LSB |
| INL | Integral nonlinearity | $T_A$ = °C to 70°C, all devices | –0.4 | ±0.3 | 0.4 | LSB |
| | | ADS9228, ADS9227 | –0.75 | ±0.3 | 0.75 | |
| | | ADS9229 | –1 | ±0.3 | 1 | |
| $V_{(OS)}$ | Input offset error | | | ±10 | | LSB |
| $dV_{OS}/dT$ | Input offset error thermal drift | | | 0.25 | 1 | ppm/°C |
| $G_E$ | Gain error(1) | | –0.05 | ±0.01 | 0.05 | %FSR |
| $dG_E/dT$ | Gain error thermal drift(1) | | | 0.5 | 2 | ppm/°C |
| **AC PERFORMANCE** | | | | | | |
| SINAD | Signal-to-noise + distortion ratio | $f_{IN}$ = 2kHz | 92 | 93.8 | | dB |
| | | $f_{IN}$ = 1MHz | | 92.9 | | |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 2kHz | 92.3 | 93.9 | | dBFS |
| | | $f_{IN}$ = 1MHz | | 93.3 | | |
| THD | Total harmonic distortion | $f_{IN}$ = 2kHz | | –120 | | dB |
| | | $f_{IN}$ = 1MHz | | –104 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 2kHz | | 120 | | dB |
| | | $f_{IN}$ = 1MHz | | 104 | | |
| | Isolation crosstalk | $f_{IN}$ = 2kHz | | 120 | | dB |
| **SAMPLING DYNAMICS** | | | | | | |
| | Aperture Jitter | SIngle-ended CMOS clock on SMPL_CLKP | | 0.3 | | $ps_{RMS}$ |
| | | Differential LVDS sampling clock | | 0.8 | | |
| BW | Input-bandwidth | ADS9229, ADS9228 | | 90 | | MHz |
| | | ADS9227 | | 45 | | |
| **INTERNAL REFERENCE** | | | | | | |
| $V_{REF}$ (2) | Voltage on REFIO pin (configured as output) | 1µF capacitor on REFIO pin, $T_A$ = 25°C | 4.092 | 4.096 | 4.1 | V |
| | Reference temperature drift | | | 6 | 20 | ppm/°C |
| **COMMON-MODE OUTPUT BUFFER** | | | | | | |
| $V_{CMOUT}$ | Common-mode output voltage | ADS9229 | 2.2 | 2.460 | 2.65 | V |
| | | ADS9228 | 2.2 | 2.410 | 2.65 | |
| | | ADS9227 | 2.2 | 2.385 | 2.65 | |
| | Output current drive | | 0 | | 5 | µA |
| **LVDS RECEIVER (SMPL_CLK)** | | | | | | |
| $V_{TH}$ | High-level input voltage (P – M) | AC coupled | 100 | | | mV |
| | | DC coupled | 300 | | | |


Copyright © 2025 Texas Instruments Incorporated

## 6.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75V to 5.25V for ADS9229, and ADS9228, and AVDD_5V = 4.5V to 5.5V for ADS9227, VDD_1V8 = 1.75V to 1.85V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{TL}$ | Low-level input voltage (P – M) | AC coupled | | | –100 | mV |
| | | DC coupled | | | –300 | |
| $V_{ICM}$ | Input common-mode voltage | | 0.5 | 1.2 | 1.4 | V |
| **LVDS OUTPUT (CLKOUT, DOUTA, and DOUTB)** | | | | | | |
| $V_{ODIFF}$ | Differential output voltage | $R_L$ = 100Ω | 200 | 350 | 500 | mV |
| $V_{OCM}$ | Output common-mode voltage | $R_L$ = 100Ω | 0.88 | 1.1 | 1.32 | V |
| **CMOS INPUTS ($\overline{CS}$, SCLK, and SDI)** | | | | | | |
| $V_{IL}$ | Input low logic level | | –0.1 | | 0.5 | V |
| $V_{IH}$ | Input high logic level | | 1.3 | | VDD_1V8 | V |
| **CMOS OUTPUT (SDO)** | | | | | | |
| $V_{OL}$ | Output low logic level | $I_{OL}$ = 200µA sink | 0 | | 0.4 | V |
| $V_{OH}$ | Output high logic level | $I_{OH}$ = 200µA source | 1.4 | | VDD_1V8 | V |
| **POWER SUPPLY** | | | | | | |
| $I_{AVDD_5V}$ | Supply current from AVDD_5V | at 20 MSPS throughput (ADS9229) | | 55 | 59 | mA |
| | | At 10 MSPS throughput (ADS9228) | | 33 | 40 | |
| | | At 5 MSPS throughput (ADS9227) | | 20 | 24 | |
| | | Power-down | | | 2 | |
| $I_{VDD_1V8}$ | Supply current from VDD_1V8 | at 20 MSPS throughput (ADS9229) | | 103 | 110 | mA |
| $I_{VDD_1V8}$ | Supply current from VDD_1V8 | At 10 MSPS throughput (ADS9228) | | 70.5 | 89 | |
| | | At 5 MSPS throughput (ADS9227) | | 50 | 66 | |
| | | Power-down | | | 2 | |

(1) These specifications include full temperature range variation but not the error contribution from internal reference.
(2) Does not include the variation in voltage resulting from solder shift effects.

Copyright © 2025 Texas Instruments Incorporated

## 6.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V for ADS9229, and ADS9228, and AVDD_5V = 4.5V to 5.5V for ADS9227, VDD_1V8 = 1.75V to 1.85V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **CONVERSION CYCLE** | | | | | |
| $f_{CYCLE}$ | Sampling frequency | ADS9229 | 7 | 20 | MHz |
| | | ADS9228 | 3.9 | 10 | |
| | | ADS9227 | 3.9 | 5 | |
| $t_{CYCLE}$ | ADC cycle time period | | 1 / $f_{CYCLE}$ | | s |
| $t_{PL_SMPLCLK}$ | Sample clock low time | | 0.4 | 0.6 | $t_{CYCLE}$ |
| $t_{PH_SMPLCLK}$ | Sample clock high time | | 0.4 | 0.6 | $t_{CYCLE}$ |
| $f_{CLK}$ | Maximum SCLK frequency | | | 10 | MHz |
| $t_{CLK}$ | Minimum SCLK time period | | 100 | | ns |
| **SPI TIMINGS** | | | | | |
| $t_{hi_CSZ}$ | Pulse duration: $\overline{CS}$ high | | 220 | | ns |
| $t_{PH_CK}$ | SCLK high time | | 0.48 | 0.52 | $t_{CLK}$ |
| $t_{PL_CK}$ | SCLK low time | | 0.48 | 0.52 | $t_{CLK}$ |
| $t_{d_CSCK}$ | Setup time: $\overline{CS}$ falling to the first SCLK rising edge | | 20 | | ns |
| $t_{su_CKDI}$ | Setup time: SDI data valid to the corresponding SCLK rising edge | | 10 | | ns |
| $t_{ht_CKDI}$ | Hold time: SCLK rising edge to corresponding data valid on SDI | | 5 | | ns |
| $t_{d_CKCS}$ | Delay time: last SCLK falling edge to $\overline{CS}$ rising | | 5 | | ns |


Copyright © 2025 Texas Instruments Incorporated

## 6.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9229, and ADS9228, and AVDD_5V = 4.5V to 5.5V for ADS9227, VDD_1V8 = 1.75V to 1.85V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **RESET** | | | | | |
| $t_{PU}$ | Power-up time for device | | | 25 | ms |
| **LVDS DATA INTERFACE** | | | | | |
| $t_{RT}$ | Rise time | With 50Ω transmission line of length = 20mm, differential $R_L$ = 100Ω, and $C_L$ = 1pF | | 600 | ps |
| $t_{FT}$ | Fall time | | | 600 | ps |
| $t_{CYCLE}$ | Sampling clock period | ADS9229 | 50 | | ns |
| | | ADS9228 | 100 | | |
| | | ADS9227 | 200 | | |
| $t_{DCLK}$ | Clock output | | 4.167 | | ns |
| | Clock duty cycle | | 45 | 55 | % |
| $t_{d_DCLKDO}$ | Time delay: DCLKP rising to corresponding data valid | SDR mode | –0.35 | 0.35 | ns |
| $t_{off_DCLKDO_r}$ | Time offset: DCLKP rising to corresponding data valid | DDR mode | $t_{DCLK}$ / 4 – 0.35 | $t_{DCLK}$ / 4 + 0.35 | ns |
| $t_{off_DCLKDO_f}$ | Time offset: DCLKP falling to corresponding data valid | DDR mode | $t_{DCLK}$ / 4 – 0.35 | $t_{DCLK}$ / 4 + 0.35 | ns |
| $t_{PD}$ | Time delay: SMPL_CLK falling to DCLKP rising | | | $t_{DCLK}$ | ns |
| $t_{PU_SMPL_CLK}$ | Time delay: Free-running clock connected to SMPL_CLK to ADC data valid | | | 100 | µs |
| $t_{d_SMPL_DATA}$ | Time delay: SMPL_CLK falling to FCLKP rising | ADS9229 | 370 | 378 | ns |
| | | ADS9228 | 186 | 196 | |
| | | ADS9227 | 103 | 112 | |
| **SPI TIMINGS** | | | | | |
| $t_{den_CKDO}$ | Time delay: 8$^{th}$ SCLK rising edge to SDO enable | | | 30 | ns |
| $t_{dz_CKDO}$ | Time delay: 24$^{th}$ SCLK rising edge to SDO going Hi-Z | | | 30 | ns |
| $t_{d_CKDO}$ | Time delay: SCLK launch edge to corresponding data valid on SDO | | | 30 | ns |
| $t_{ht_CKDO}$ | Hold time: SCLK launch edge to previous data valid on SDO | | 2 | | ns |

Copyright © 2025 Texas Instruments Incorporated

## 6.8 Timing Diagrams

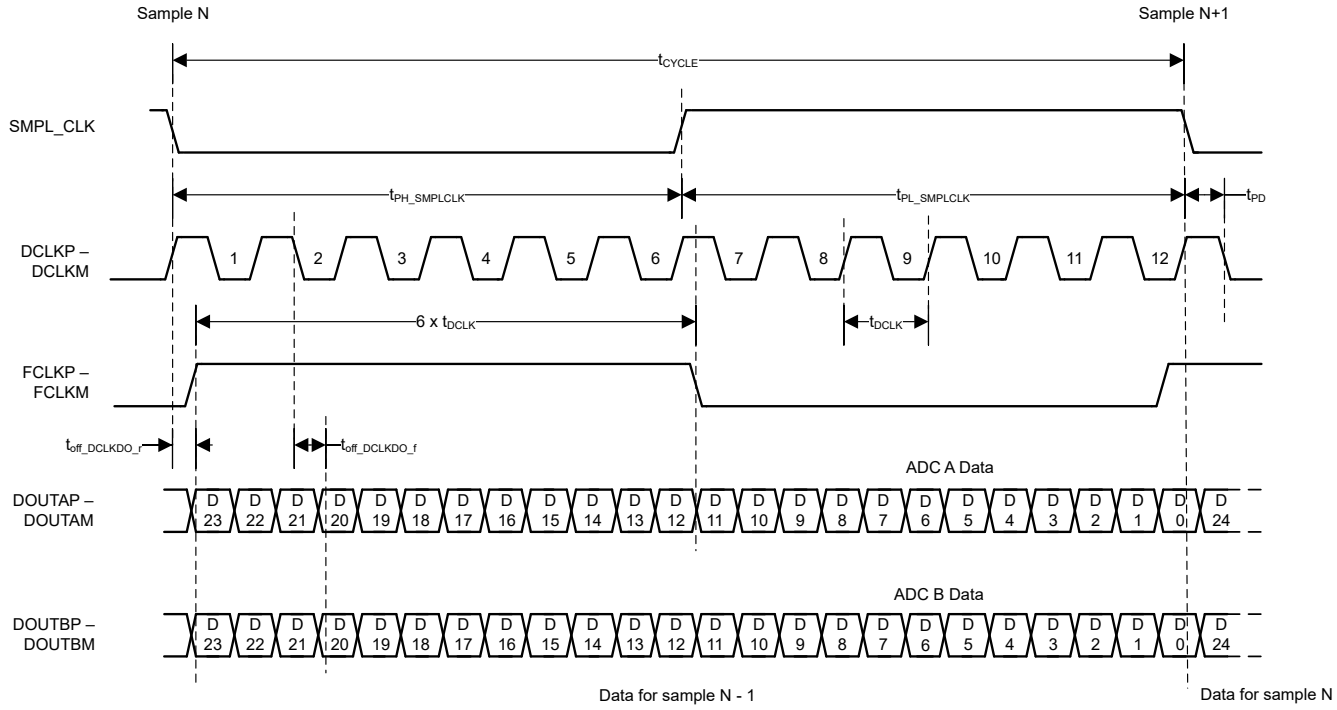



**Figure 6-1. LVDS Data Interface: 2-Lane DDR**

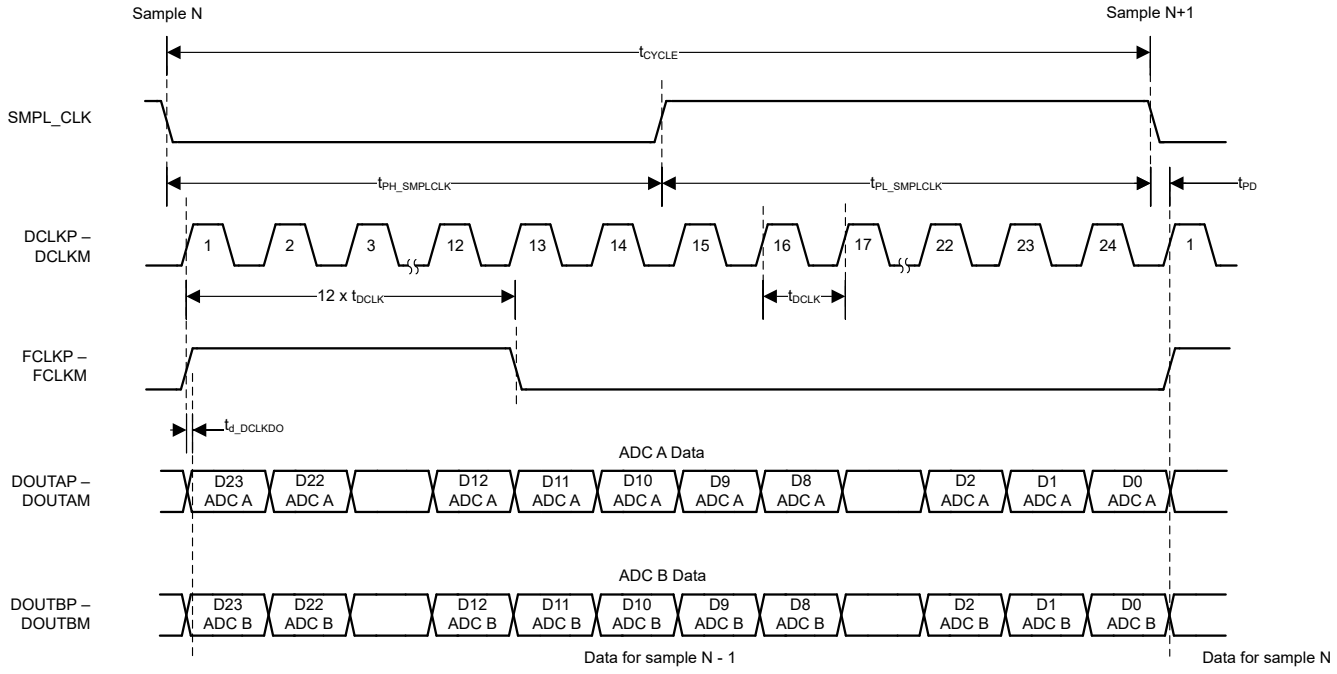



**Figure 6-2. LVDS Data Interface: 2-Lane SDR**


Copyright © 2025 Texas Instruments Incorporated

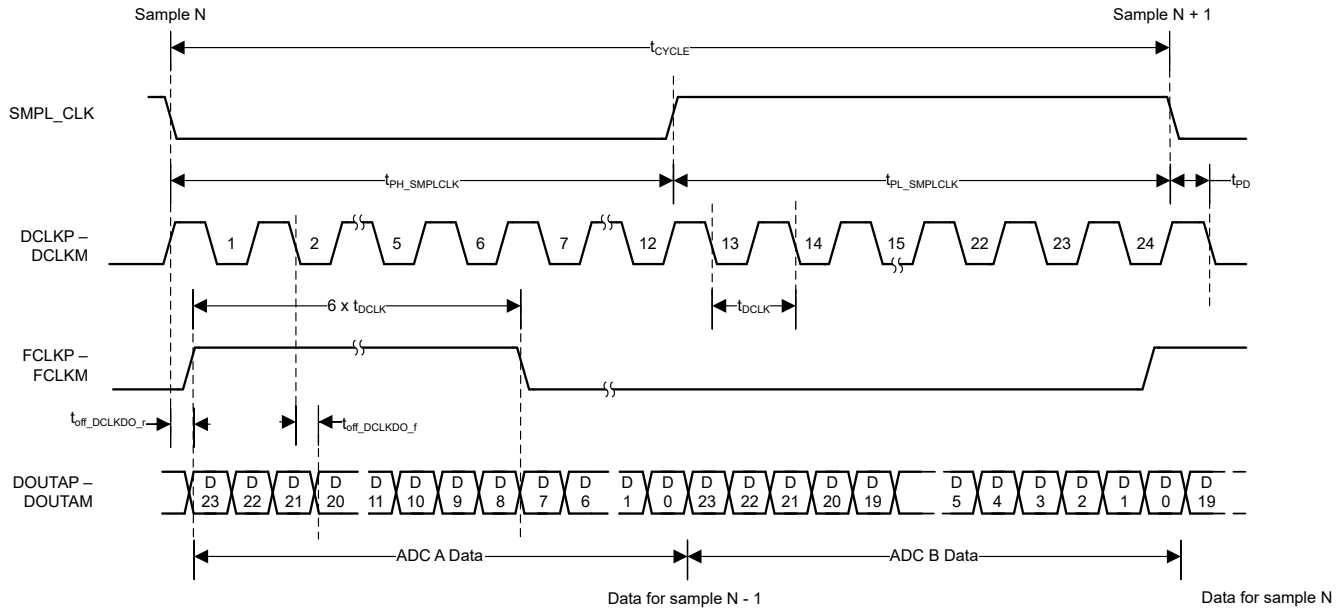



**Figure 6-3. LVDS Data Interface: 1-Lane DDR**

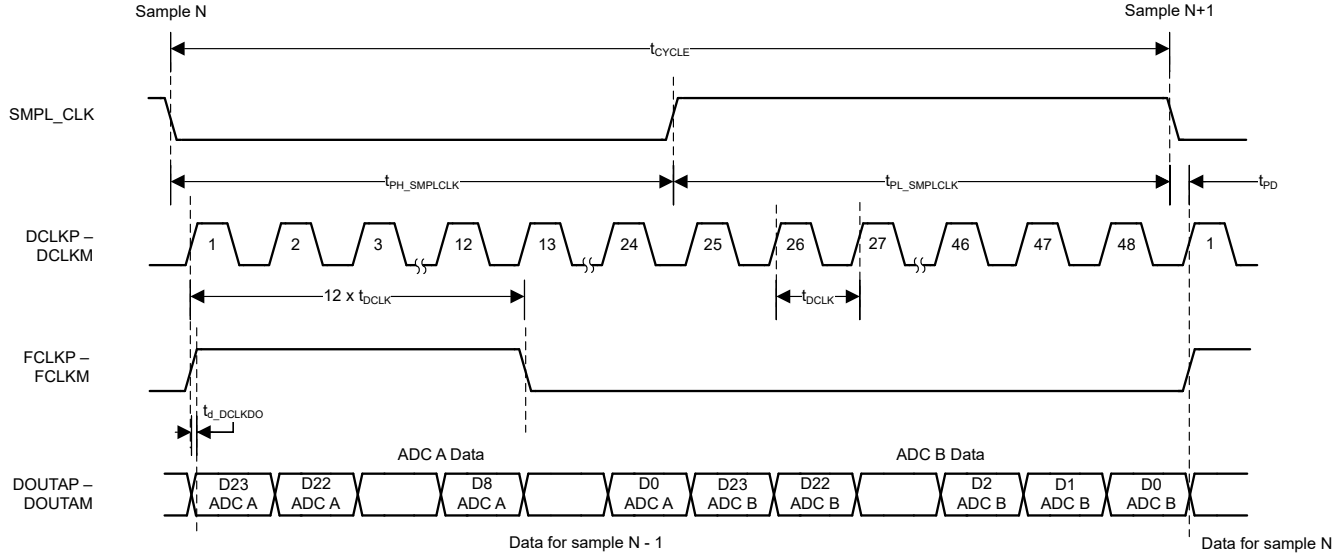



**Figure 6-4. LVDS Data Interface: 1-Lane SDR**

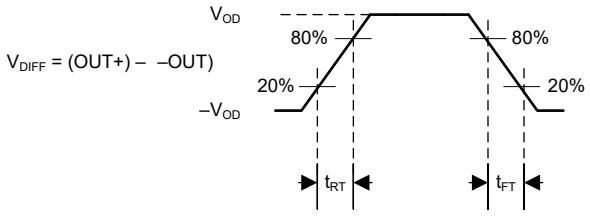



**Figure 6-5. LVDS Output Transition Times**

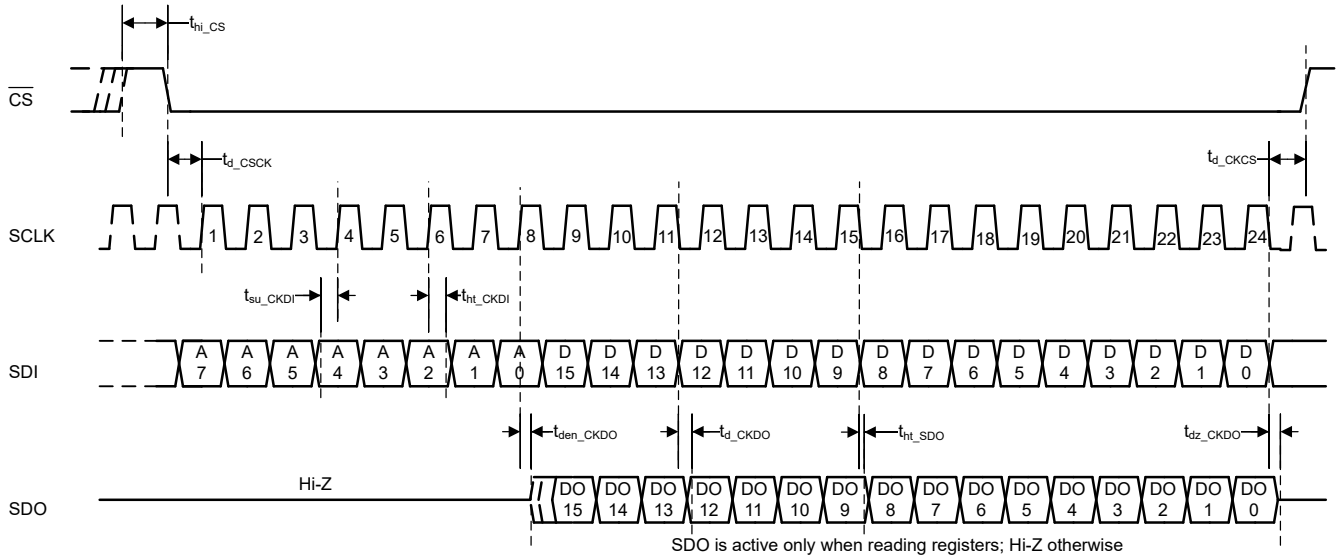



**Figure 6-6. Configuration SPI**

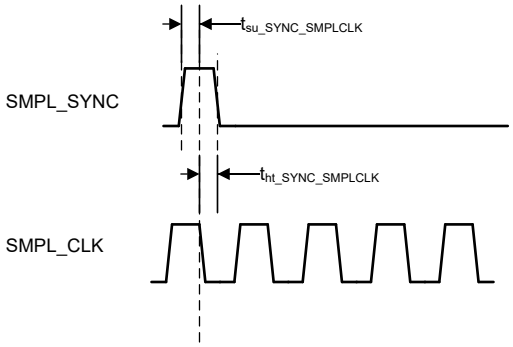



**Figure 6-7. SMPL_SYNC Timing**

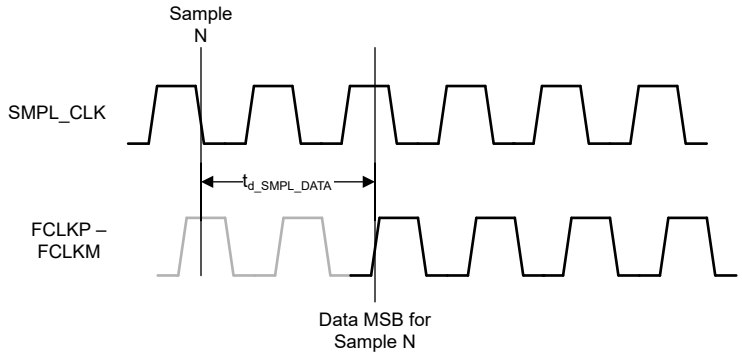



**Figure 6-8. Sampling Edge to Corresponding Data MSB Output Timing**


Copyright © 2025 Texas Instruments Incorporated

## 6.9 Typical Characteristics: All Devices

at $T_A$ = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted)

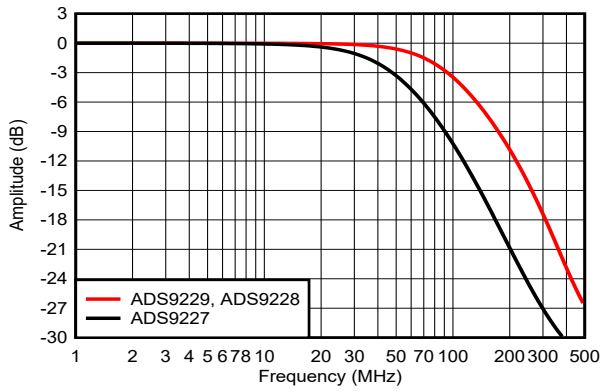



**Figure 6-9. Typical Analog Input Bandwidth**

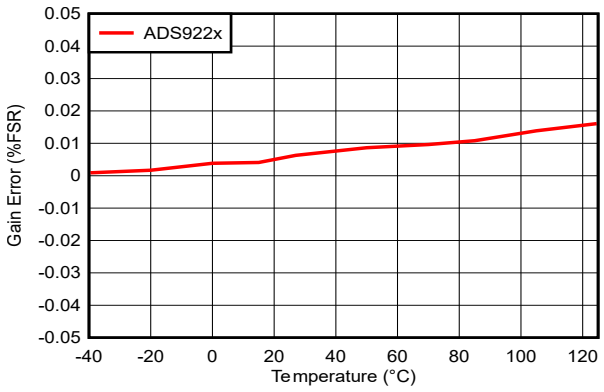



**Figure 6-10. Gain Error vs Temperature**

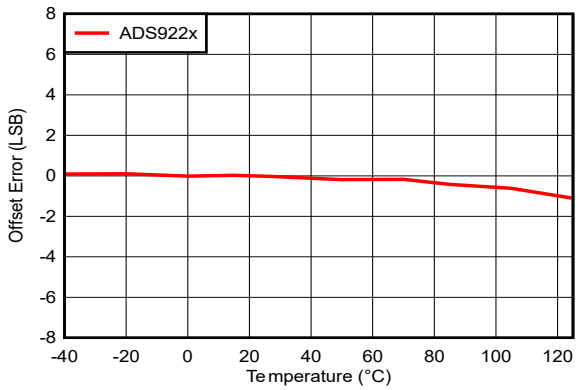



**Figure 6-11. Offset Error vs Temperature**

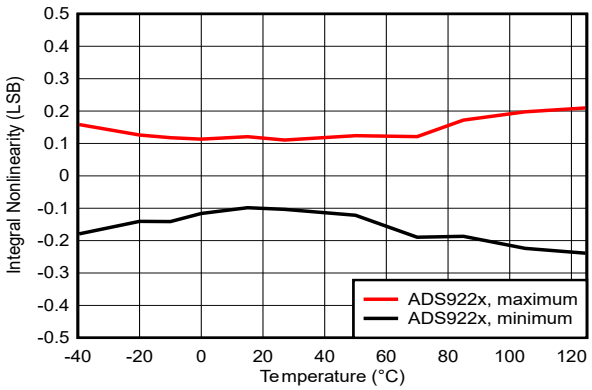



**Figure 6-12. INL vs Temperature**

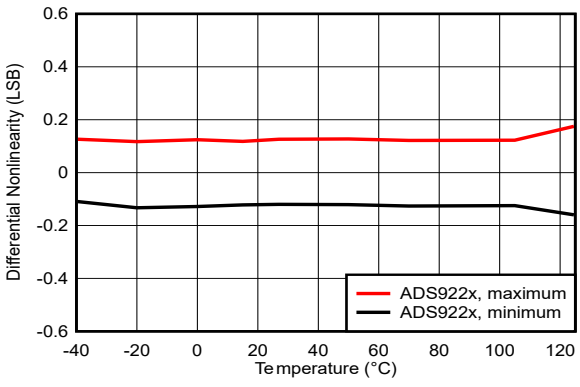



**Figure 6-13. DNL vs Temperature**

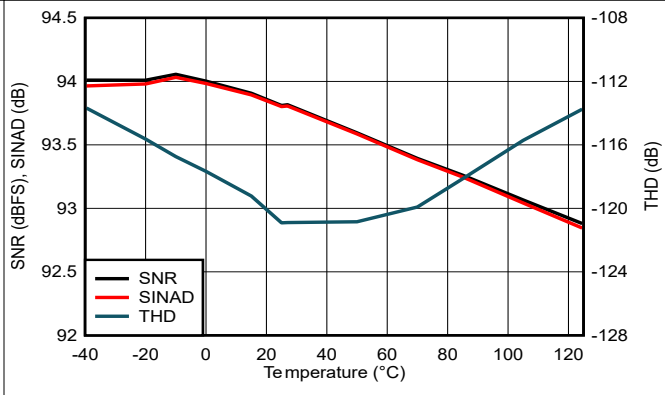



**Figure 6-14. SNR, SINAD, and THD vs Temperature**

Copyright © 2025 Texas Instruments Incorporated

## 6.9 Typical Characteristics: All Devices (continued)

at $T_A$ = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted)

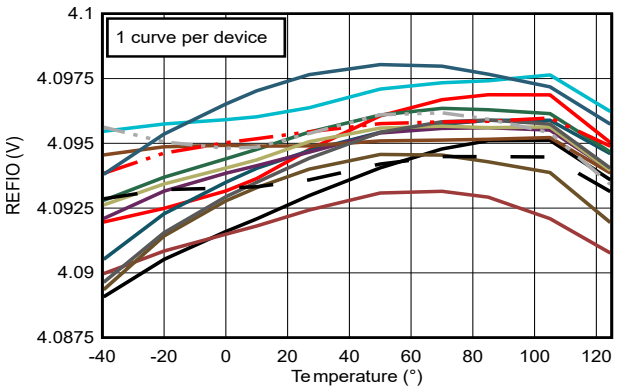



**Figure 6-15. REFIO Voltage vs Temperature**

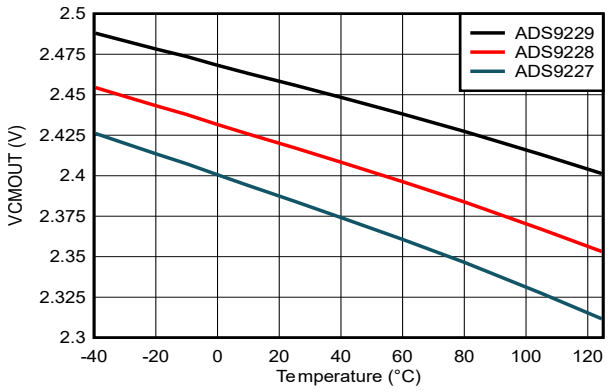



**Figure 6-16. $V_{CMOUT}$ Voltage vs Temperature**

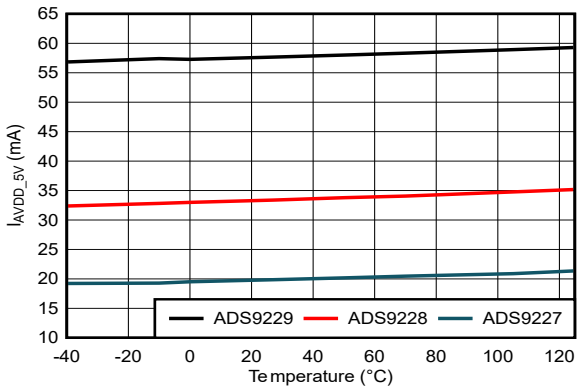



**Figure 6-17. AVDD_5V Current vs Temperature**

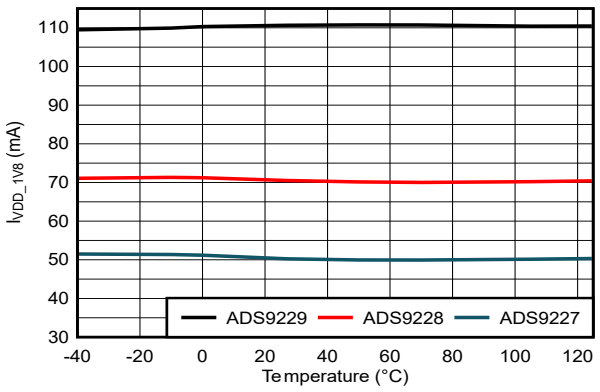
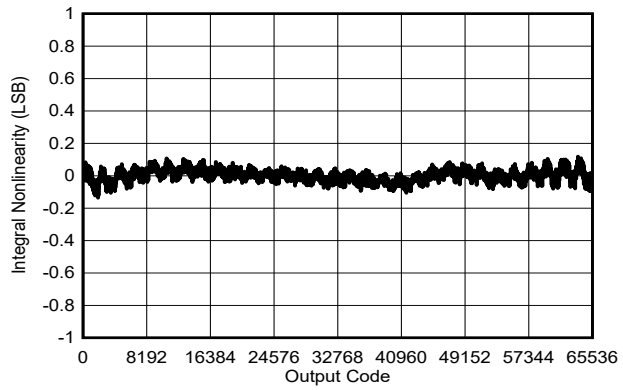



**Figure 6-18. VDD_1V8 Current vs Temperature**


Copyright © 2025 Texas Instruments Incorporated

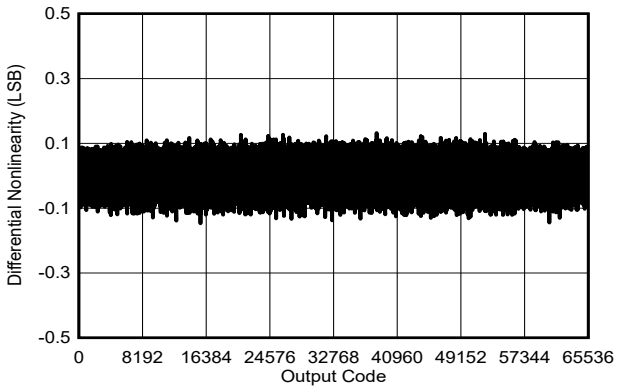
## 6.10 Typical Characteristics: ADS9229

at $T_A$ = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted)



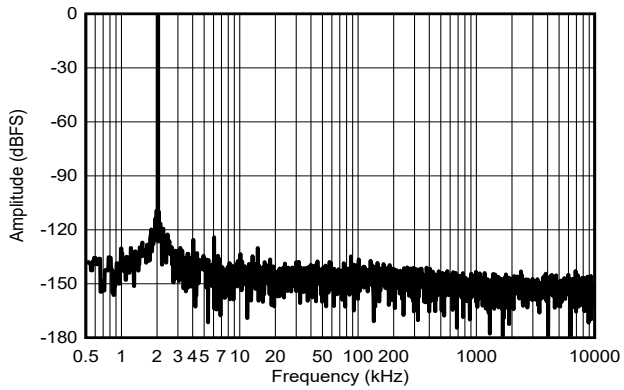

Typical INL = ±0.15LSB

**Figure 6-19. Typical INL**



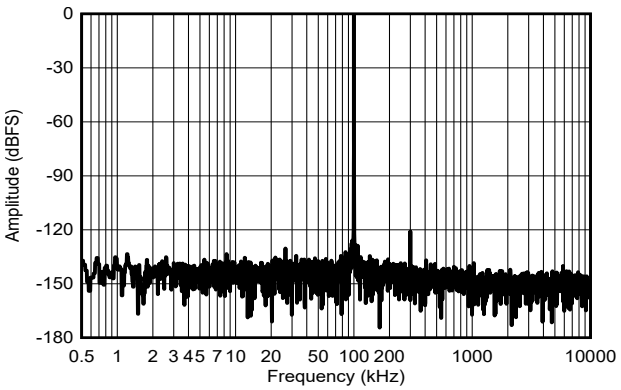

Typical DNL = ±0.15LSB

**Figure 6-20. Typical DNL: ADS9229**



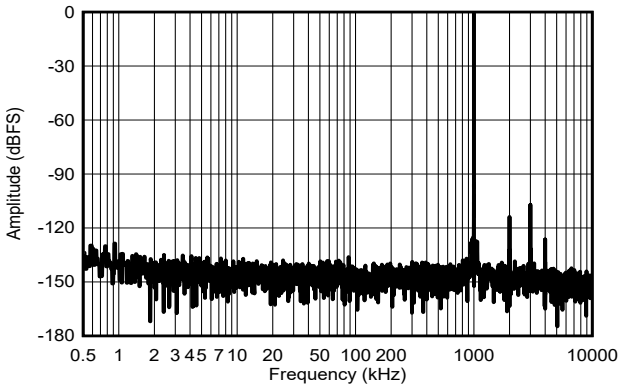

$f_{IN}$ = 2kHz, SNR = 93.5dBFS, THD = –120dB

**Figure 6-21. Typical FFT for $f_{IN}$ = 2kHz**




$f_{IN}$ = 100kHz, SNR = 93.5dBFS, THD = –118dB

**Figure 6-22. Typical FFT for $f_{IN}$ = 100kHz**



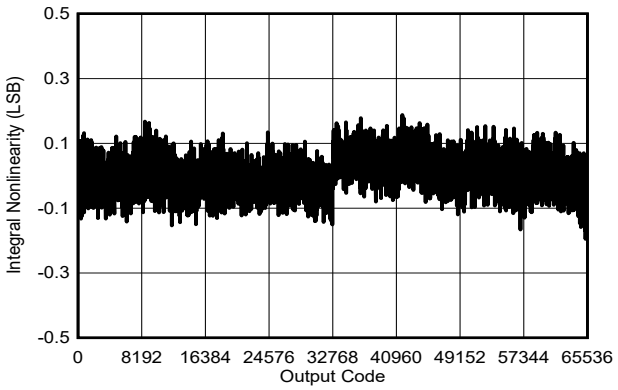

$f_{IN}$ = 1MHz, SNR = 93.3dBFS, THD = –104.2dB

**Figure 6-23. Typical FFT for $f_{IN}$ = 1MHz**

Copyright © 2025 Texas Instruments Incorporated

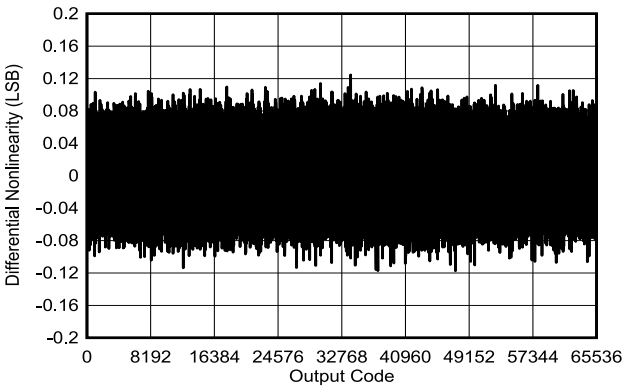
## 6.11 Typical Characteristics: ADS9228

at $T_A$ = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted)



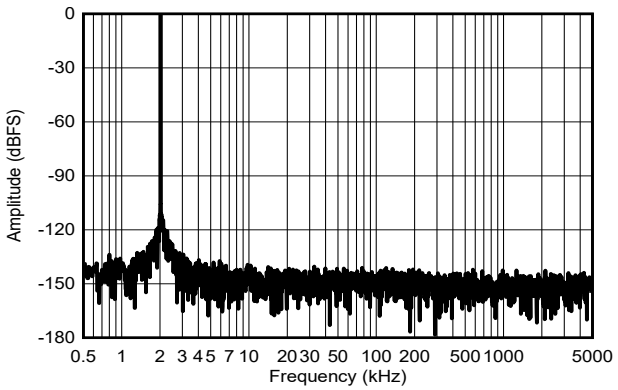

Typical INL = ±0.2LSB

**Figure 6-24. Typical INL**



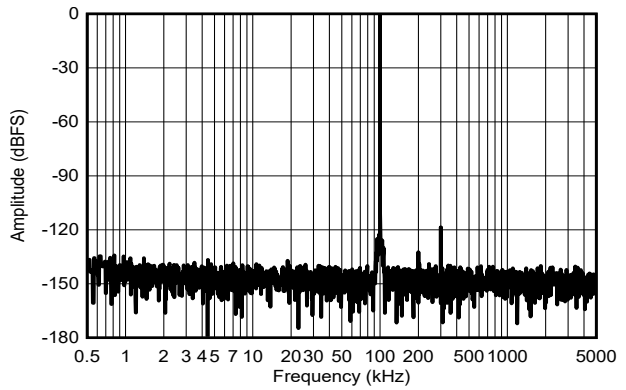

Typical DNL = ±0.15LSB

**Figure 6-25. Typical DNL**



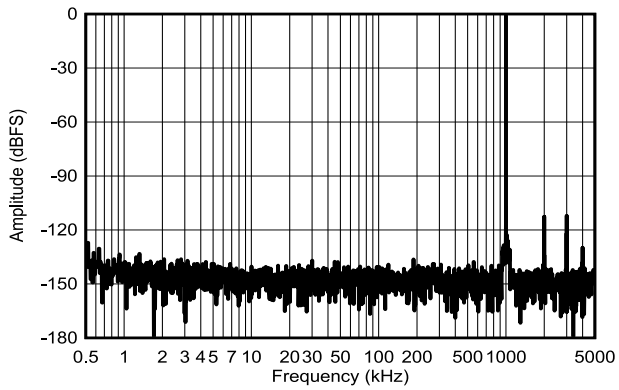

$f_{IN}$ = 2kHz, SNR = 93.9dBFS, THD = –122dB

**Figure 6-26. Typical FFT for $f_{IN}$ = 2kHz**




$f_{IN}$ = 100kHz, SNR = 93.8dBFS, THD = –118dB

**Figure 6-27. Typical FFT for $f_{IN}$ = 100kHz**



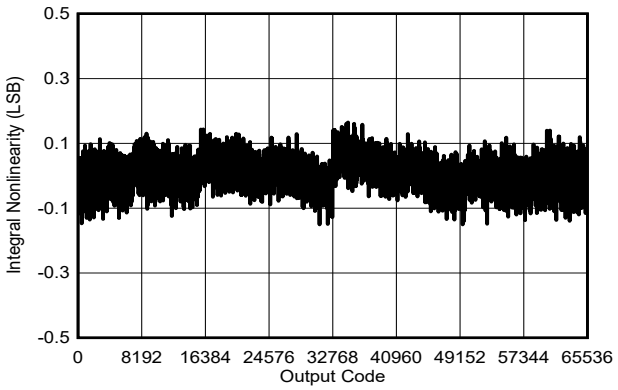

$f_{IN}$ = 1MHz, SNR = 93.3dBFS, THD = –104dB

**Figure 6-28. Typical FFT for $f_{IN}$ = 1MHz**


Copyright © 2025 Texas Instruments Incorporated

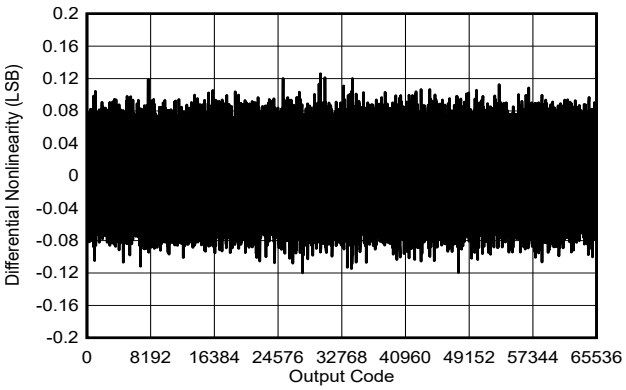
## 6.12 Typical Characteristics: ADS9227

at $T_A$ = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, internal $V_{REF}$ = 4.096V, and maximum throughput (unless otherwise noted)



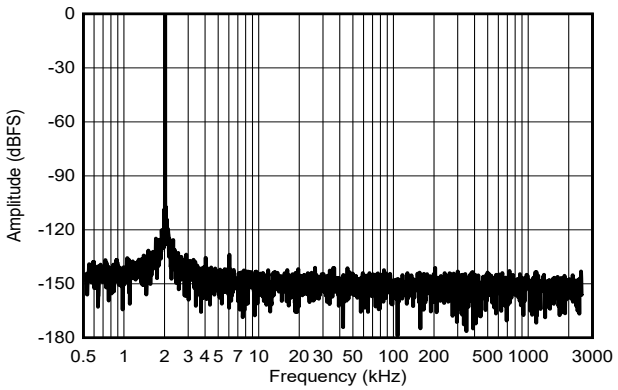

Typical INL = ±0.2LSB

**Figure 6-29. Typical INL**



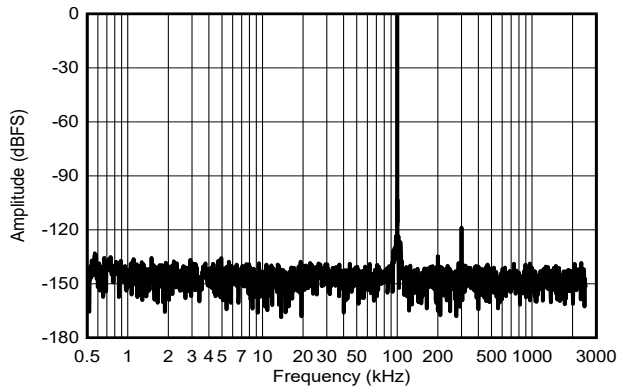

Typical DNL = ±0.15LSB

**Figure 6-30. Typical DNL**



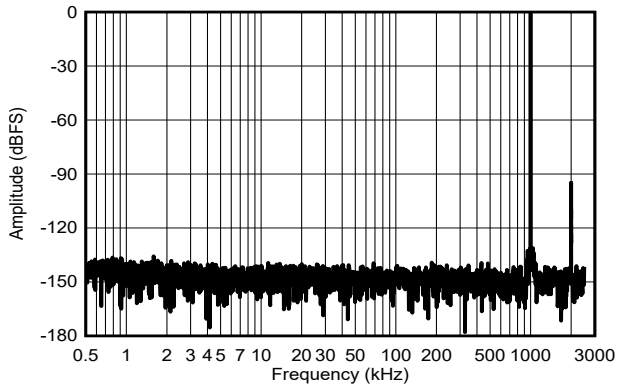

$f_{IN}$ = 2kHz, SNR = 93.9dBFS, THD = –122.5dB

**Figure 6-31. Typical FFT for $f_{IN}$ = 2kHz**




$f_{IN}$ = 100kHz, SNR = 93.8dBFS, THD = –119dB

**Figure 6-32. Typical FFT for $f_{IN}$ = 100kHz**




$f_{IN}$ = 1MHz, SNR = 93.3dBFS, THD = –104.5dB

**Figure 6-33. Typical FFT for $f_{IN}$ = 1MHz**

Copyright © 2025 Texas Instruments Incorporated

# 7 Detailed Description

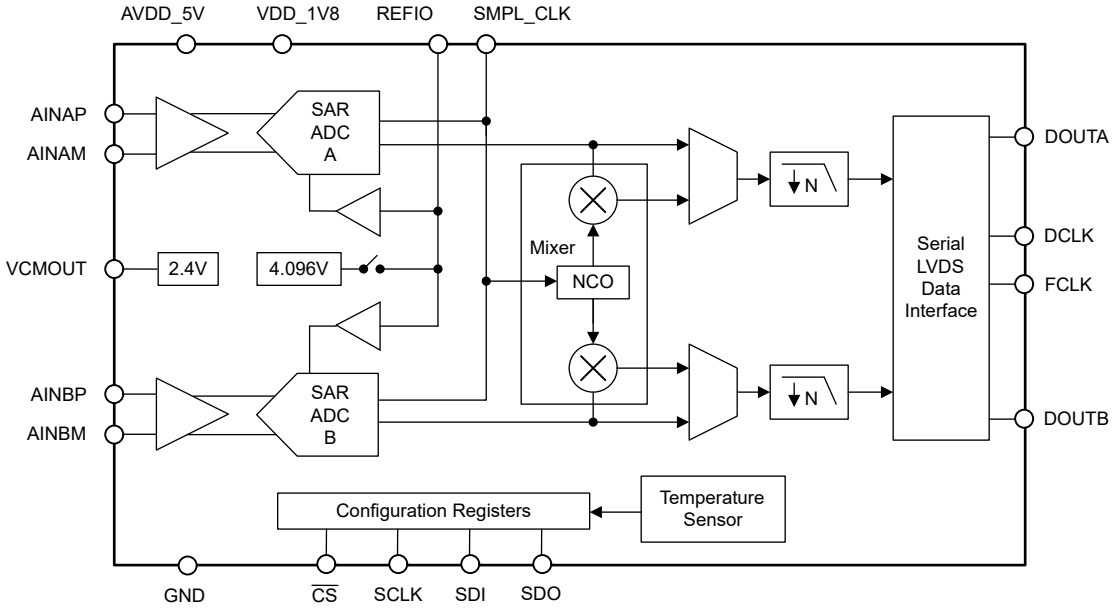
## 7.1 Overview

The ADS922x is a 16-bit, 20MSPS/ch, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC). The ADS922x integrates a high-impedance buffer at the ADC inputs, voltage reference, reference buffer, and common-mode voltage output buffer. The ADS9229 supports unipolar differential analog input signals. The buffer at the ADC inputs is optimized for low-distortion and low-power operation.

For DC level shifting of the analog input signals, the device has a common-mode voltage output buffer. The common-mode voltage is derived from the output of the integrated reference buffer. When a conversion is initiated, the differential input between the (AINAP – AINAM) and (AINBP – AINBM) pins is sampled. The ADS922x uses a clock input on the SMPL_CLKP pin to initiate conversions.

The ADS922x consumes only 230mW/ch of power when operating at 20MSPS/ch, which includes the buffer power dissipation at the ADC inputs. The serial LVDS (SLVDS) digital interface simplifies board layout, timing, firmware, and supports full throughput at lower clock speeds.

## 7.2 Functional Block Diagram





Copyright © 2025 Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Analog Inputs

The ADS922x supports both AC-coupled and DC-coupled differential analog inputs. Make sure the input common-mode voltage of the analog inputs matches the voltage level on the VCMOUT pin. Figure 7-1 shows the equivalent input network diagram of the device.

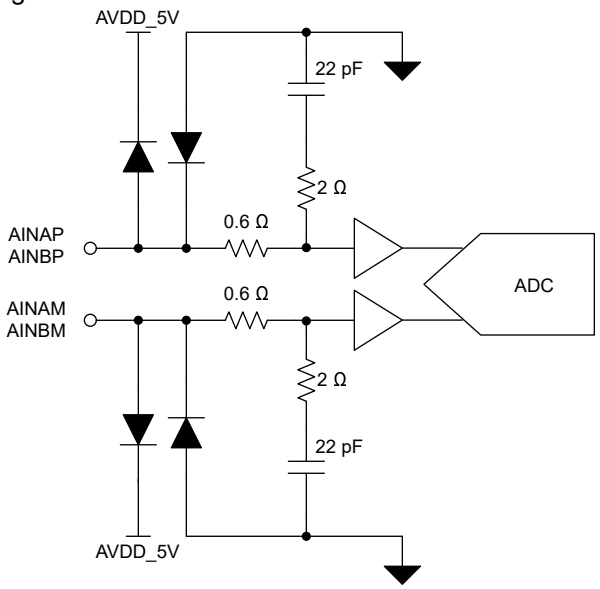



**Figure 7-1. Equivalent Input Network**

### 7.3.2 Analog Input Bandwidth

Figure 6-9 illustrates the analog full-power input bandwidth of the ADS922x device family. The –3dB bandwidth is 90MHz for the ADS9229 and ADS9228, and 45MHz for the ADS9227.

### 7.3.3 ADC Transfer Function

The ADS922x supports a ±3.2V differential input range. The device outputs 16-bit conversion data in either straight-binary or binary two's-complement formats. As shown in Table 7-1, the format for the output codes is the same across all analog channels. Configure the format for the output codes with the DATA_FORMAT field in register address 0x0D. The least significant bit (LSB) for the ADC is given by 1LSB = 6.4V / $2^{16}$.

**Table 7-1. Transfer Characteristics**

| INPUT VOLTAGE | DESCRIPTION | ADC OUTPUT IN 2's-COMPLEMENT FORMAT | ADC OUTPUT IN STRAIGHT-BINARY FORMAT |
|---|---|---|---|
| ≤ –3.2V + 1LSB | Negative full-scale code | 0x8000 | 0x0000 |
| 0V + 1LSB | Mid-code | 0x0000 | 0x7FFF |
| ≥ 3.2V – 1LSB | Positive full-scale code | 0x7FFF | 0xFFFF |

### 7.3.4 Reference

The ADS922x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 10µF ceramic bypass capacitor to the REFIO pin. Connect an external reference at the REFIO pin with the internal reference voltage disabled by writing to the PD_REF field in register address 0xC1.

Copyright © 2025 Texas Instruments Incorporated

#### 7.3.4.1 Internal Reference Voltage

The ADS922x features an internal reference voltage with a nominal output voltage of 4.096V. On power-up, the internal reference is enabled by default. Place a minimum 10µF decoupling capacitor between the REFIO and REFM pins. Figure 7-2 shows a block diagram of the internal reference voltage.

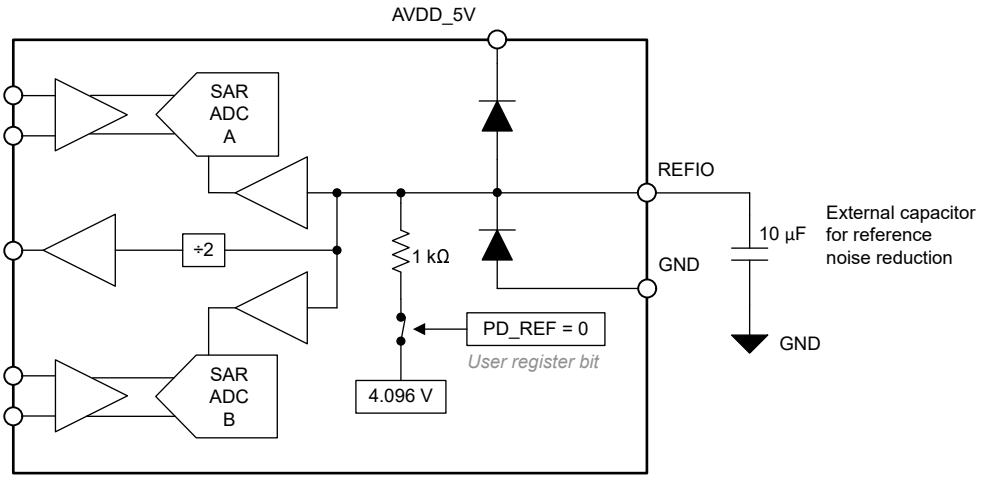



**Figure 7-2. Internal Reference Voltage**

#### 7.3.4.2 External Reference Voltage

Connect an external 4.096V reference voltage at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, the REF7040 is recommended. To disable the internal reference, set PD_REF = 1b in address 0xC1 in register bank 1. The REFIO pin has electrostatic discharge (ESD) protection diodes connected to the AVDD_5V and REFM pins. Figure 7-3 shows an external reference diagram.

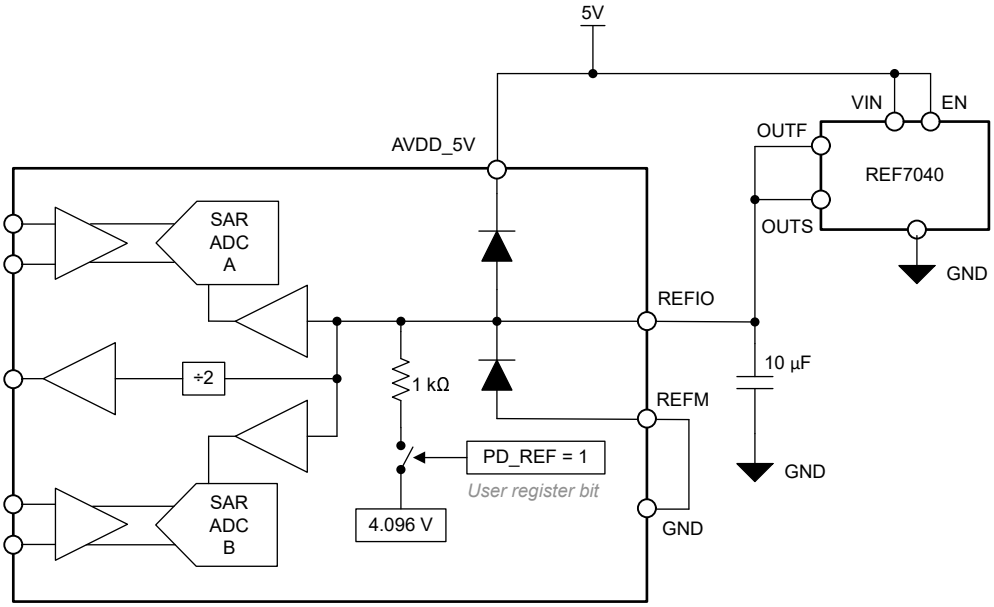



**Figure 7-3. External Reference Voltage**


Copyright © 2025 Texas Instruments Incorporated

### 7.3.5 Temperature Sensor

The ADS922x features a 10-bit temperature sensor for measuring temperature inside the device. Follow the sequence listed in Table 7-2 to read the temperature sensor output with the SPI. Read the temperature sensor data at anytime independent of the ADC data interface.

The transfer function for the temperature sensor is given by Equation 1:

$$\text{Temperature} = -85.0172 + (10\text{ bit output} \times 0.24918)\ ^{\circ}\text{C} \quad (1)$$

**Table 7-2. Sequence to Read Temperature Sensor Output**

| REGISTER ADDRESS | REGISTER BANK | VALUE | COMMENT |
|---|---|---|---|
| 0x90 | 1 | 0x4000 | Write register to load temperature sensor output in address 0x91 |
| 0x91 | 1 | 10 bit temperature sensor data | Read register for temperature sensor output |
| 0x90 | 1 | 0x0000 | Write register |

### 7.3.6 Data Averaging

The ADS922x features a built-in decimation filter that averages the conversion results from the ADC. The output data rate is reduced with higher data averaging. Table 7-3 compares the ADC output speed against SNR and OSR. The improvement in SNR with averaging in Table 7-4 shows the register settings corresponding to oversampling ratios.

**Table 7-3. SNR vs OSR**

| OSR | SNR (dBFS) | ADC OUTPUT SPEED |
|---|---|---|
| 1 | 93.8 | $f_{CYCLE}$ |
| 2 | 94.9 | $f_{CYCLE}$ / 2 |
| 4 | 95.9 | $f_{CYCLE}$ / 4 |
| 8 | 96.6 | $f_{CYCLE}$ / 8 |
| 16 | 97.0 | $f_{CYCLE}$ / 16 |

**Table 7-4. Register Map Settings for OSR**

| DECIMATION | REGISTER | INTERFACE MODES[1] | |
|---|---|---|---|
| | | 2-LANE SDR AND DDR[2] | 1-LANE SDR AND DDR[3] |
| OSR initialization | CLK3 (0xC5[9]) | 1 | 0 for OSR = 2<br>1 for OSR = 4, 8, and 16 |
| | OSR_INIT1 (0xC0[11:10]) | 0 for DATA_LANES = 5 or 7<br>1 for DATA_LANES = 0 or 2 | |
| | OSR_INIT2 (0xC4[5:4]) | 2 | 0 for OSR = 2<br>2 for OSR = 4, 8, and 16 |
| | OSR_INIT3 (0xC4[1]) | 1 | 0 for OSR = 2<br>1 for OSR = 4, 8, and 16 |
| | OSR_EN (0x0D[6]) | 1 | 1 |
| | OSR_RD (0xC5[6:5]) | 1 | 0 for OSR = 2<br>1 for OSR = 4, 8, and 16 |
| 2 | OSR (0x0D[5:2]) | 0 | 0 |
| | OSR_CLK (0xC0[9:7]) | 0 | 0 |
| 4 | OSR (0x0D[5:2]) | 1 | 1 |
| | OSR_CLK (0xC0[9:7]) | 4 | 0 |
| 8 | OSR (0x0D[5:2]) | 2 | 2 |
| | OSR_CLK (0xC0[9:7]) | 5 | 4 |

Copyright © 2025 Texas Instruments Incorporated

**Table 7-4. Register Map Settings for OSR (continued)**

| DECIMATION | REGISTER | INTERFACE MODES(1) | |
|---|---|---|---|
| | | 2-LANE SDR AND DDR(2) | 1-LANE SDR AND DDR(3) |
| 16 | OSR (0x0D[5:2]) | 3 | 3 |
| | OSR_CLK (0xC0[9:7]) | 6 | 5 |

(1) See Table 7-7 and Table 7-8 for DATA_LANES configuration.
(2) The ADS9227 functions with all data interface modes.
(3) Not applicable for the ADS9227.

As shown in Figure 7-4, a pulse on the SMPL_SYNC pin resets the decimation filter. A pulse on SMPL_SYNC synchronizes multiple ADS922x devices when using the decimation filter.

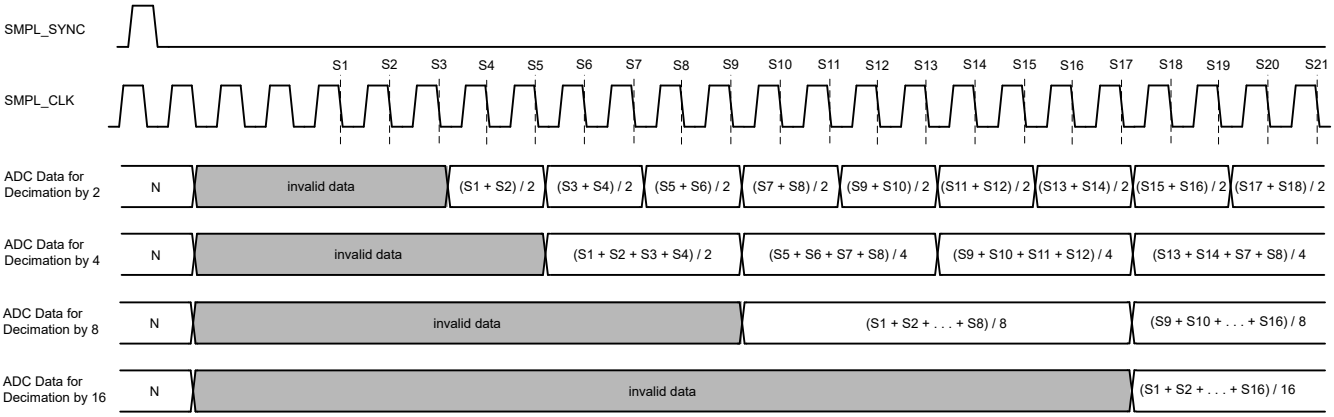



**Figure 7-4. Data Output With Decimation**

### *7.3.7 Digital Down Converter*

The ADS922x includes an optional on-chip digital down conversion (DDC) that is configured by register addresses FBh through FEh. As shown in Figure 7-5, the DDC includes a digital mixer and a 24-bit, numerically controlled oscillator (NCO). The digital mixer generates 24-bit I and Q outputs that represent complex mixing of ADC output data with the NCO output frequency. Each channel of the ADC generates a 48-bit output corresponding to the 24-bit I and Q outputs, respectively, from the digital mixer.

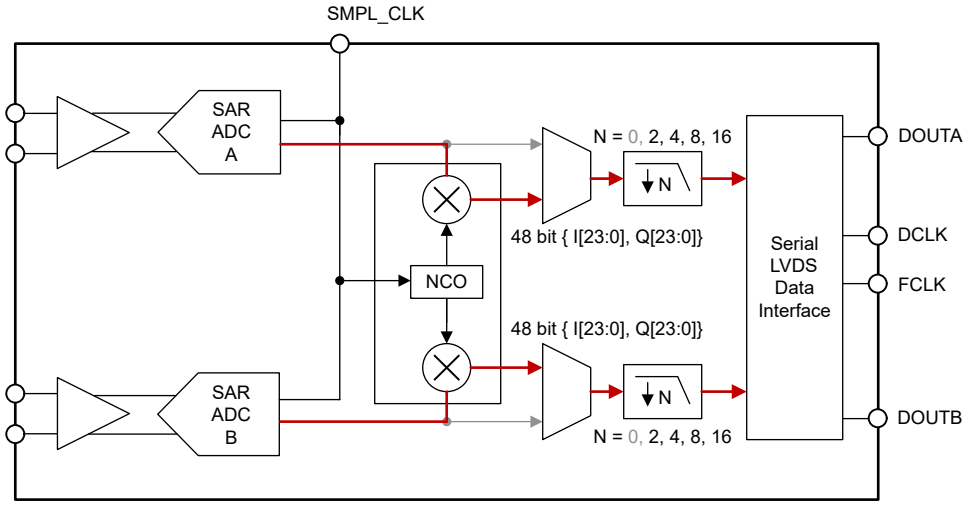



**Figure 7-5. Data Path When Using a Digital Down Converter**


Copyright © 2025 Texas Instruments Incorporated

The NCO is common for both ADC A and ADC B. The output frequency of the NCO, given by Equation 2, is configured using the NCO_FREQUENCY register (address 0xFD and 0xFE).

$$f_{NCO} = \frac{f_{SMPL_CLK}}{2^{24}} \times (NCO_FREQUENCY[23:0] \,\&\, 0xFFFFF0)\ Hz \quad (2)$$

The output phase of the NCO is reset by applying a pulse on the SMPL_SYNC pin, see Figure 6-7. As shown in Equation 3 and Table 7-5, the initial phase of the NCO output is configured using the NCO_PHASE register (address 0xFC and 0xFD).

$$NCO_PHASE[23:0] = \left(\frac{\text{Initial phase}}{2\pi} \times 2^{24}\right) \& \ 0xFFFFF0 \quad (3)$$

**Table 7-5. Initial NCO Phase**

| NCO_PHASE[23:0] | INITIAL PHASE |
|---|---|
| 0x000000 | 0 |
| 0x7FFFF0 | π |
| 0xFFFFF0 | 2π |

Use a decimation factor of either 2, 4, 8, or 16 with the DDC. Table 7-6 shows the register configuration for decimating the DDC output.

**Table 7-6. Decimation Settings for the DDC**

| DECIMATION | REGISTER | VALUE |
|---|---|---|
| 2 | OSR_EN (0x0D[6]) | 1 |
| | OSR (0x0D[5:2] | 0 |
| | OSR_CLK (0xC0[9:7]) | 0 |
| Common settings for decimation factors 4, 8, and 16 | CLK3 (0xC5[9]) | 1 |
| | OSR_INIT1 (0xC0[11:10]) | 1 |
| | OSR_INIT2 (0xC4[5:4]) | 2 |
| | OSR_INIT3 (0xC4[1]) | 1 |
| | OSR_EN (0x0D[6]) | 1 |
| | OSR_RD (0xC5[6:5]) | 1 |
| 4 | OSR (0x0D[5:2] | 1 |
| | OSR_CLK (0xC0[9:7]) | 0 |
| 8 | OSR (0x0D[5:2] | 2 |
| | OSR_CLK (0xC0[9:7]) | 4 |
| 16 | OSR (0x0D[5:2] | 3 |
| | OSR_CLK (0xC0[9:7]) | 5 |

Copyright © 2025 Texas Instruments Incorporated

### 7.3.8 Data Interface

The ADS922x features a high-speed, serial LVDS data interface with 2-lane and 1-lane options for data output. The host configures the output data frame width to 20 bits or 24 bits with the single-data rate (SDR) and double-data rate (DDR) modes. Table 7-7 and Table 7-8 configuration.

Configure the INIT_1 register field before writing to other register fields, as described in Table 7-7 and Table 7-8.

**Table 7-7. Register Map Settings for Output Data Interface for the ADS9227**

| DATA FRAME WIDTH (Bits) | DATA RATE | OUTPUT LANES | INIT_1 0x04[3:0] | DATA_LANES 0x12[2:0] | DATA_RATE 0xC1[8] | CLK1 0xC0[12] | CLK2 0xC1[0] | CLK3 0xC5[9] | CLK4 0xC5[3:2] | CLK5 0xFB[1] | CLK6 0x1C[7:6] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | SDR | 1 | 0x000B | 5 | 1 | 1 | 1 | 1 | 3 | 0 | 3 |
| 20 | SDR | 2 | 0x000B | 0 | 1 | 0 | 1 | 0 | 3 | 0 | 3 |
| 20 | DDR | 1 | 0x000B | 5 | 0 | 1 | 1 | 1 | 3 | 0 | 3 |
| 20 | DDR | 2 | 0x000B | 0 | 0 | 0 | 1 | 0 | 3 | 0 | 3 |
| 24 | SDR | 1 | 0x000B | 7 | 1 | 1 | 0 | 1 | 3 | 0 | 3 |
| 24 | SDR | 2 | 0x0000 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | DDR | 1 | 0x000B | 7 | 0 | 1 | 0 | 1 | 3 | 0 | 3 |
| 24 | DDR | 2 | 0x0000 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 7-8. Register Map Settings for Output Data Interface for the ADS9229 and ADS9228**

| DATA FRAME WIDTH (Bits) | DATA RATE | OUTPUT LANES | INIT_1 0x04[3:0] | DATA_LANES 0x12[2:0] | DATA_RATE 0xC1[8] | CLK1 0xC0[12] | CLK2 0xC1[0] | CLK3 0xC5[9] | CLK4 0xC5[3:2] | CLK5 0xFB[1] | CLK6 0x1C[7:6] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | SDR | 1 | – | Not supported | | | | | | | |
| 20 | SDR | 2 | – | Not supported | | | | | | | |
| 20 | DDR | 1 | – | Not supported | | | | | | | |
| 20 | DDR | 2 | – | Not supported | | | | | | | |
| 24 | SDR | 1 | – | 2 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 24 | SDR | 2 | – | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | DDR | 1 | – | 2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 24 | DDR | 2 | – | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The ADS922x generates a data clock DCLK that is a multiple of the ADC sampling clock SMPL_CLK. The data clock frequency depends on the number of data output lanes (1 or 2), data frame width, and data rate. The data frame width is 20 or 24 bits and the data rate is SDR or DDR. Equation 4 calculates the DCLK speed. Table 7-9 lists the possible values for the output data clock frequency.

$$\text{DCLK speed} = \frac{2\ \text{ADC channels} \times \text{Data Frame Width (24 bit or 20 bit)}}{\text{Data Lanes (1 or 2)} \times \text{Data Rate(SDR} = 1,\ \text{DDR} = 2)} \times \text{SMPL_CLK} \quad (4)$$


Copyright © 2025 Texas Instruments Incorporated

**Table 7-9. Data Clock (DCLK) Speed**

| ADC CHANNELS | DATA FRAME WIDTH (Bits) | DATA RATE (1 = SDR, 2 = DDR) | OUTPUT LANES(1) | SMPL_CLK MULTIPLIER | DCLK (SMPL_CLK = 5MHz) | DCLK (SMPL_CLK = 10MHz) | DCLK (SMPL_CLK = 20MHz) |
|---|---|---|---|---|---|---|---|
| 2 | 24 | 1 | 1 | 48 | 240MHz | — | — |
| | | | 2 | 24 | 120MHz | —(2) | —(2) |
| | | 2 | 1 | 24 | 120MHz | 240MHz | 480MHz |
| | | | 2 | 12 | 60MHz | 120MHz | 240MHz |
| | 20 | 1 | 1 | 40 | 200MHz | —(3) | —(3) |
| | | | 2 | 20 | 100MHz | —(3) | —(3) |
| | | 2 | 1 | 20 | 100MHz | —(3) | —(3) |
| | | | 2 | 10 | 50MHz | —(3) | —(3) |

(1) The LVDS output data and clock are specified up to 600MHz. Faster speeds are not supported.
(2) For the ADS9229 and ADS9228, 1-lane data output is supported only when data averaging is enabled. See the *Data Averaging* section.
(3) A 20-bit data frame width is not supported for the ADS9229 or ADS9228.

#### 7.3.8.1 Data Frame Width

As shown in Figure 7-6, the ADS922x supports 24-bit and 20-bit data frame width options. Configure the DATA_WIDTH field in address 0x12 to select the data frame width. The default output data frame width is 24 bits. The ADC resolution is 16-bit, represented by 20 bits.

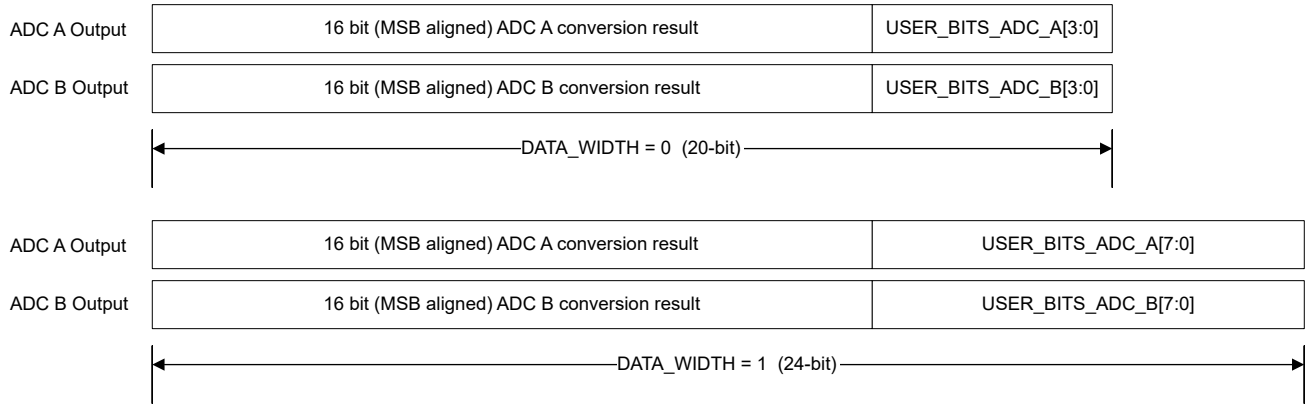



**Figure 7-6. Data Frame Width Composition**

#### 7.3.8.2 ADC Output Data Randomizer

The ADS922x features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR). Figure 7-7 illustrates a diagram of such an XOR operation. Either the LSB of the conversion result (Figure 7-9) or XOR_PRBS bit (default) is appended to the ADC data output (Figure 7-8). The LSB of the ADC conversion result and XOR_PRBS have equal probability of being either 1 or 0. As a result of the XOR operation, the data output from the ADS922x is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce.

Copyright © 2025 Texas Instruments Incorporated

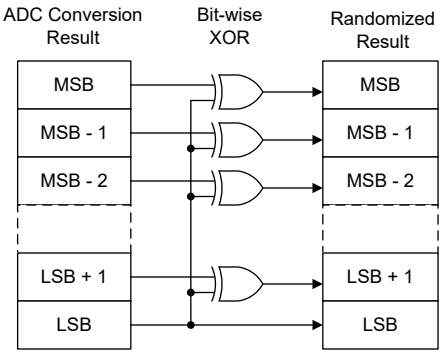



**Figure 7-7. Bit-Wise XOR Operation**

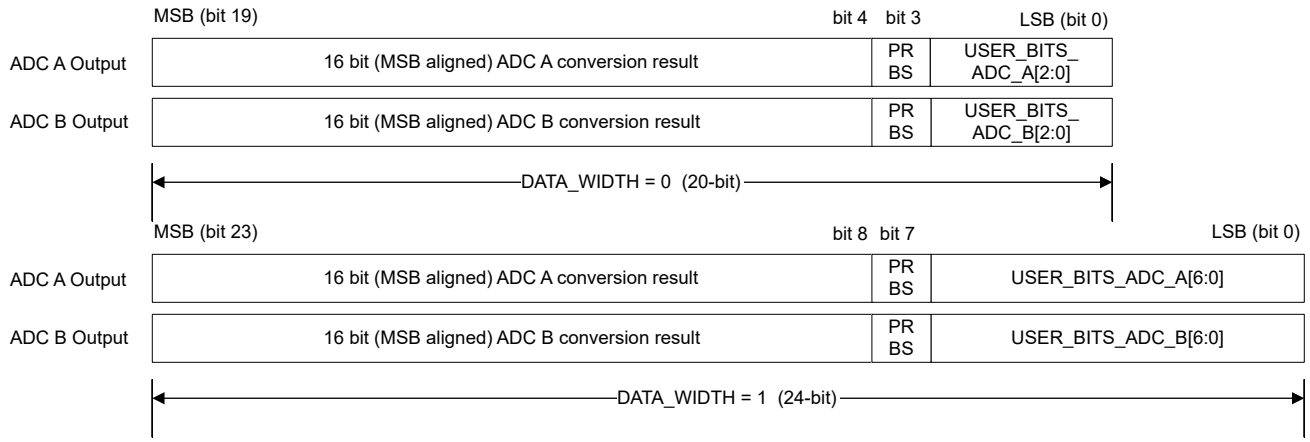



**Figure 7-8. Data Frame Width Composition With PRBS XOR Enabled**

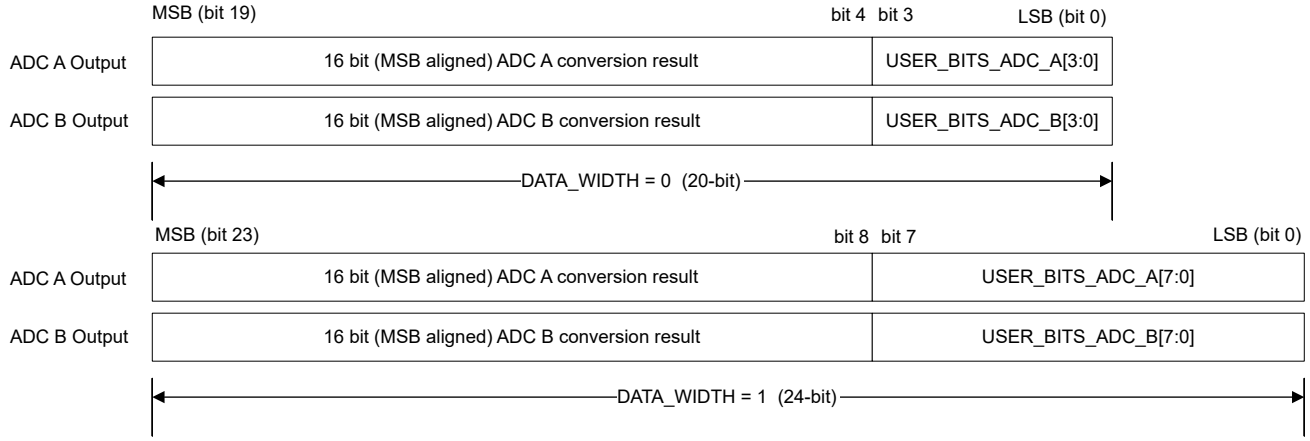



**Figure 7-9. Data Frame Width Composition With LSB XOR Enabled**

#### 7.3.8.3 Synchronizing Multiple ADCs

Drive the SMPL_CLK pins of the respective ADS922x devices with a common sampling clock. Match the timing delay on the clock path external to the ADCs by using identical PCB trace lengths for SMPL_CLK for the respective ADCs.

Use the SMPL_SYNC pin to synchronize multiple ADCs when using the internal decimation filter. The SMPL_SYNC pin is latched by the falling edge of the sampling clock. A pulse on SMPL_SYNC resets the internal decimation filter.


Copyright © 2025 Texas Instruments Incorporated

### 7.3.9 Test Patterns for Data Interface

The ADS922x features test patterns (Figure 7-10) used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. Enable the test patterns by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

Table 7-10 lists the test patterns supported by the ADS922x.

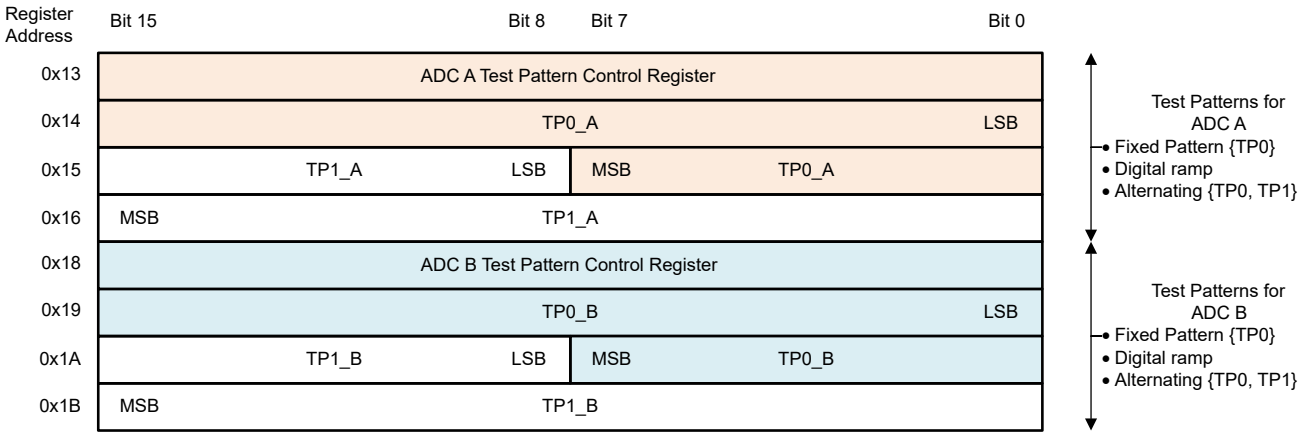



**Figure 7-10. Register Bank for Test Patterns**

**Table 7-10. Test Pattern Configurations**

| ADC OUTPUT | TP_EN_CHA<br>TP_EN_CHB | TP_MODE_CHA<br>TP_MODE_CHB | SECTION | RESULT[1] |
|---|---|---|---|---|
| ADC conversion result | 0 | — | — | — |
| Fixed pattern | 1 | 0 or 1 | *Fixed Pattern* | ADC A = TP0_A<br>ADC B = TP0_B |
| Digital ramp | 1 | 2 | *Digital Ramp* | ADC A = Digital ramp<br>ADC B = Digital ramp |
| Alternating test patterns | 1 | 3 | *Alternating Test Pattern* | ADC A = TP0_A, TP1_A<br>ADC B = TP0_B, TP1_B |

**Note**

1. Configure the test patterns for two separate channel groups ADC A and ADC B.

#### 7.3.9.1 Fixed Pattern

The ADC outputs fixed patterns defined in the TP0_A and TP0_B registers in place of the ADC A and ADC B data, respectively.

- Configure the test patterns in TP0_A and TP0_B
- Set TP_EN_A = 1, TP_MODE_A = 0 (address = 0x13), TP_EN_B = 1, and TP_MODE_B = 0 (address = 0x18)

#### 7.3.9.2 Digital Ramp

The ADC outputs digital ramp values with increments specified in the RAMP_INC_A and RAMP_INC_B registers in place of ADC A and ADC B data, respectively.

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_A (address = 0x13) and RAMP_INC_B (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TP_EN_A = 1, TP_MODE_A = 2 (address = 0x13), TP_EN_B = 1, and TP_MODE_B = 2 (address = 0x18)

Copyright © 2025 Texas Instruments Incorporated

#### 7.3.9.3 Alternating Test Pattern

The ADC outputs alternating test patterns defined in the TP0_A, TP1_A and TP0_B, TP1_B registers in place of ADC A and ADC B data, respectively.

- Configure the test patterns in TP0_A, TP1_A, TP0_B, and TP1_B
- Set TP_EN_A = 1, TP_MODE_A = 3 (address = 0x13), TP_EN_B = 1, and TP_MODE_B = 3 (address = 0x18)

### *7.3.10 ADC Sampling Clock Input*

Use a low-jitter external clock with a high slew rate to maximize SNR performance. Operate the ADS922x with a differential or single-ended clock input. Clock amplitude impacts the ADC aperture jitter and, consequently, the SNR. For maximum SNR performance, provide a clock signal with fast slew rates that maximizes swing between VDD_1V8 and GND levels.

Make sure the sampling clock is a free-running continuous clock. The ADC generates a valid output data, data clock, and frame clock $t_{PU_SMPL_CLK}$, as specified in the *Switching Characteristics* after a free-running sampling clock is applied. When the sampling clock is stopped, the ADC is in power-down and the output data, data clock, and frame clock are invalid.

Figure 7-11 shows a diagram of the differential sampling clock input. For this configuration, connect the differential sampling clock input to the SMPL_CLKP and SMPL_CLKM pins. Figure 7-12 shows a diagram of the single-ended sampling clock input. In this configuration, connect the single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

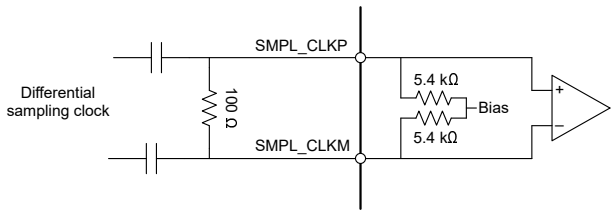



**Figure 7-11. AC-Coupled Differential Sampling Clock**

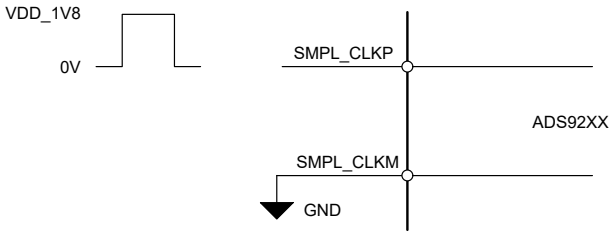



**Figure 7-12. Single-Ended Sampling Clock**


Copyright © 2025 Texas Instruments Incorporated

## 7.4 Device Functional Modes

### 7.4.1 Reset

Power down the ADS922x with a logic 0 on the $\overline{\text{RESET}}$ pin or write 1b to the RESET field (address 0x00, register bank 0). The device registers are initialized to the default values after reset. Register write operations are not required for initializing the ADS9228.

### 7.4.2 Power-Down Options

Power down the ADS922x with a logic 0 on the $\overline{\text{PWDN}}$ pin or write 11b to the PD_CH field (address 0xC0, register bank 1). The device registers are initialized to the default values after power-up. Register write operations are not required for initializing the ADS9228.

### 7.4.3 Normal Operation

In normal operating mode, the ADS922x is powered-up and digitizes the analog inputs at the falling edge of the sampling clock. The ADC outputs the data clock, frame clock, and MSB-aligned, 16-bit conversion result.

### 7.4.4 Initialization Sequence

The ADS922x register map is initialized with default values on power-up. Table 7-11 lists the steps to enable gain-error calibration (recommended) and change the output data interface. For the ADS9229 only, follow the initialization steps in Table 7-12.

**Table 7-11. User-Defined Configuration for the ADS9229, ADS9228, and ADS9227**

| STEP NUMBER | REGISTER | | | COMMENT |
|---|---|---|---|---|
| | BANK | ADDRESS | VALUE[15:0] | |
| 1 | 1 | 0x0D | User defined | Enable gain error calibration and select ADC output data format |
| 2 | 1 | 0x33 | 0x2040 | Enable gain error calibration |
| 3 | 0 | 0x04 | 0x0000 for data frame width = 24 bits and output lanes = 2<br>0x000B for other combinations of data frame width and output lanes | |

**Table 7-12. Initialization Configuration for the ADS9229 Only**

| STEP NUMBER | REGISTER | | |
|---|---|---|---|
| | BANK | ADDRESS | VALUE[15:0] |
| 1 | 1 | 0x0D [9:8] | 0x3 |
| 2 | 1 | 0x34 [1] | 0x1 |

Copyright © 2025 Texas Instruments Incorporated

## 7.5 Programming

### 7.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 are selected for read or write operation by configuring the REG_BANK_SEL bits. Registers in bank 0 are always accessible, irrespective of the REG_BANK_SEL bits. The register addresses in bank 0 are unique and are not used in register banks 1 and 2.

As shown in Figure 7-13, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

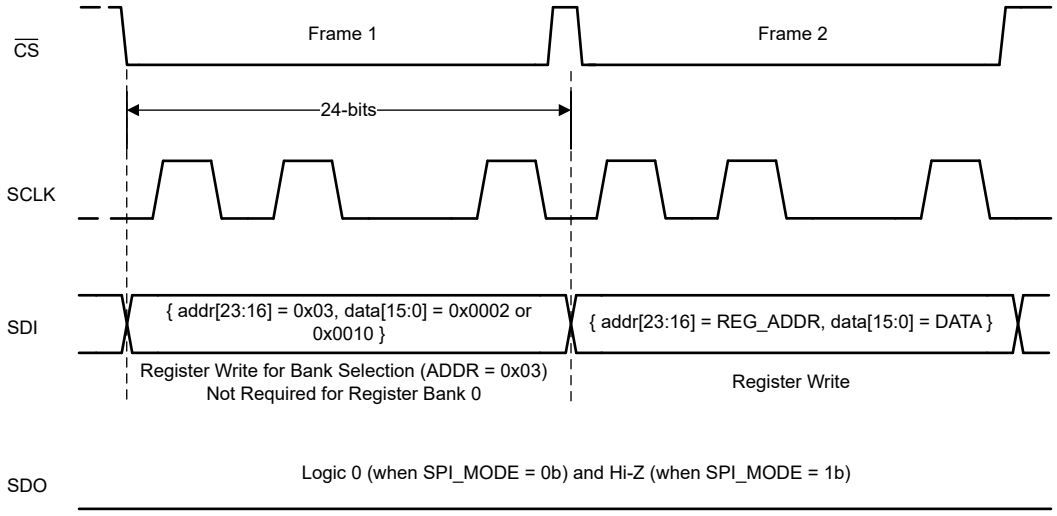



**Figure 7-13. Register Write**

### 7.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in Figure 7-14, registers are read using two 24-bit SPI frames after SPI_RD_EN and SPI_MODE are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 7-14, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.


Copyright © 2025 Texas Instruments Incorporated

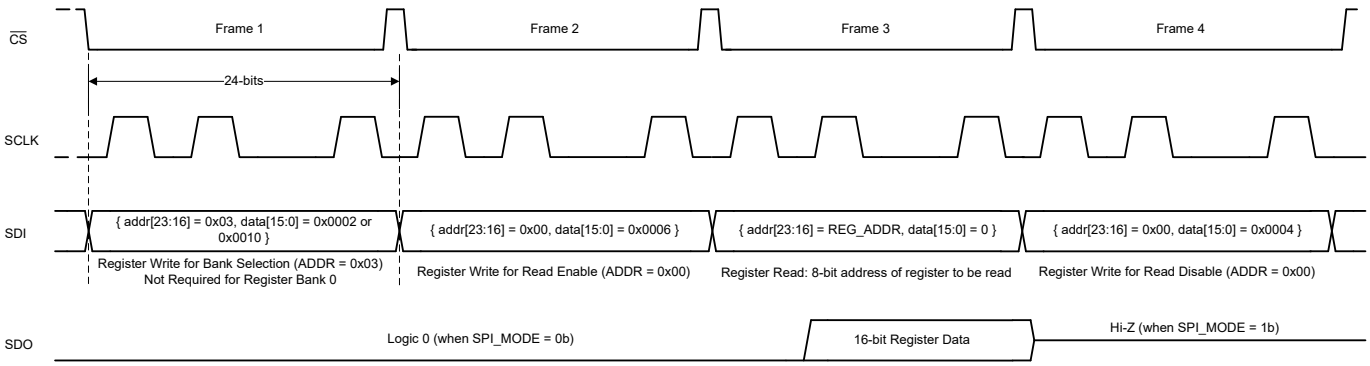



**Figure 7-14. Register Read**

### *7.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration*

Figure 7-15 shows a typical connection diagram with multiple devices in a daisy-chain topology.

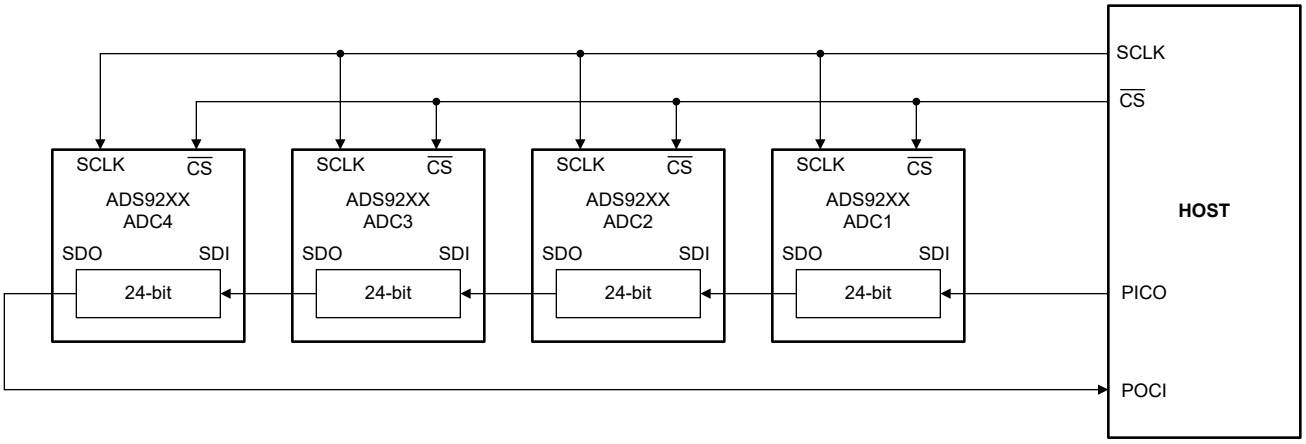



**Figure 7-15. Daisy-Chain Connections for SPI Configuration**

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller. The SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

Enable daisy-chain mode after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LEN register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain, excluding ADC1. In Figure 7-15, the DAISY_CHAIN_LEN is 3.

#### 7.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain configuration requires N × 24 SCLKs in one SPI frame. Register writes in a daisy-chain configuration containing four ADCs, as illustrated in Figure 7-15, requires 96 SCLKs.

The daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LEN field to enable daisy-chain mode. Repeat the waveform in Figure 7-16 N times, where N is the number of ADCs in the daisy chain. Figure 7-17 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

Copyright © 2025 Texas Instruments Incorporated

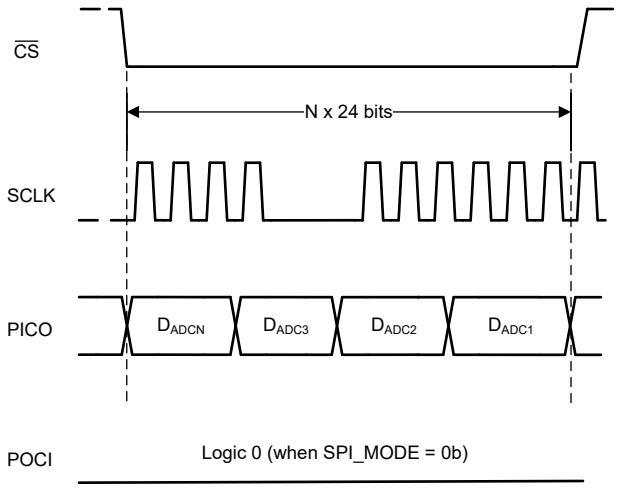



**Figure 7-16. Register Write With Daisy-Chain**

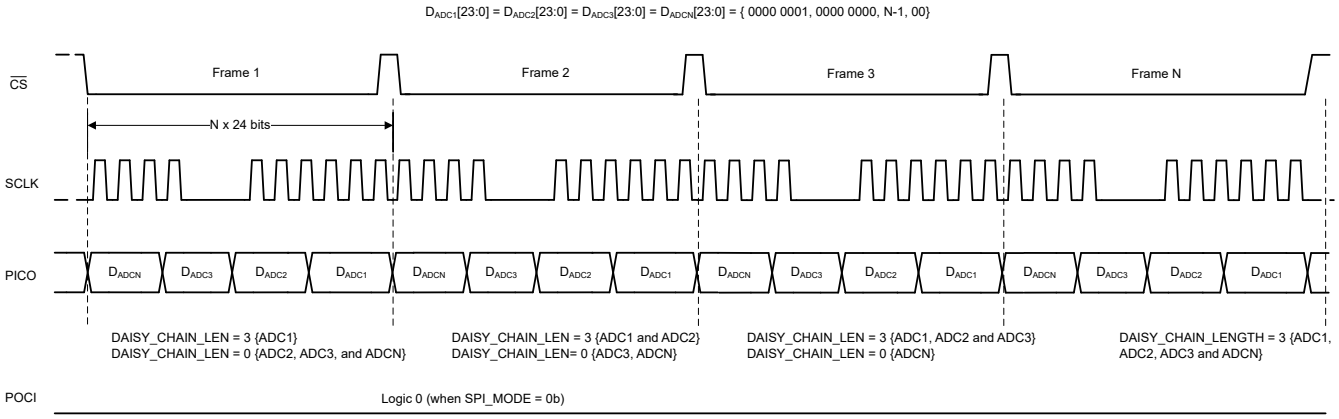



**Figure 7-17. Register Write to Configure Daisy-Chain Length**

#### 7.5.3.2 Register Read With Daisy-Chain

Figure 7-18 illustrates an SPI waveform for reading registers in daisy-chain configuration. Steps for reading registers from N ADCs connected in daisy-chain are:

1. Register read is enabled by writing to the following registers:
   a. Write to REG_BANK_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller reads register data by:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N times (0xFE, 0x00, 8-bit register address)
   b. N × 24-bit SPI frame to read out register data: N times (0xFF, 0xFF, 0xFF)

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.


Copyright © 2025 Texas Instruments Incorporated

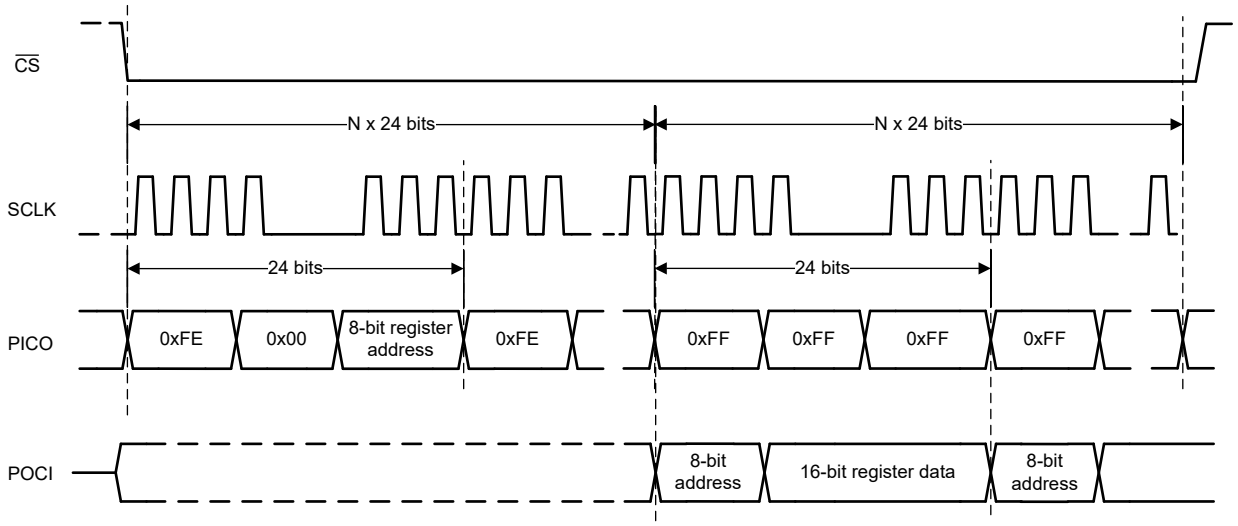



**Figure 7-18. Register Read With Daisy-Chain Configuration**

# 8 Register Map

## 8.1 Register Bank 0

**Figure 8-1. Register Bank 0 Map**

| ADD | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | RESERVED | | | | | | | | | | | | | SPI_MODE | SPI_RD_EN | RESET |
| 01h | RESERVED | | | | | | | | | DAISY_CHAIN_LEN | | | | | RESERVED | |
| 03h | RESERVED | | | | | | | | | REG_BANK_SEL | | | | | | |
| 04h | RESERVED | | | | | | | | | | | | | INIT_1 | | |
| 06h | REG_00H_READBACK | | | | | | | | | | | | | | | |

**Table 8-1. Register Section/Block Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| W | W | Write |
| R/W | R/W | Read or write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 8.1.2 Register 00h (offset = 0h) [reset = 0h]

**Figure 8-2. Register 00h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | SPI_MODE | SPI_RD_EN | RESET |
| W-0h | | | | | W-0h | W-0h | W-0h |

**Figure 8-3. Register 00h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-3 | RESERVED | W | 0h | Reserved. Do not change from the default reset value. |
| 2 | SPI_MODE | W | 0h | Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access.<br>0 : Daisy-chain SPI mode<br>1 : Legacy SPI mode |
| 1 | SPI_RD_EN | W | 0h | Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode.<br>0 : Register read disabled<br>1 : Register read enabled |
| 0 | RESET | W | 0h | ADC reset control.<br>0 : Normal device operation<br>1 : Reset all registers |


Copyright © 2025 Texas Instruments Incorporated

### 8.1.3 Register 01h (offset = 1h) [reset = 0h]

**Figure 8-4. Register 01h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | DAISY_CHAIN_LEN | | | | | RESERVED | |
| R/W-0h | R/W-0h | | | | | R/W-0h | |

**Figure 8-5. Register 01h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-7 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 6-2 | DAISY_CHAIN_LEN | R/W | 0h | Configure the number of ADCs connected in daisy-chain for the SPI configuration.<br>0 : 1 ADC<br>1 : 2 ADCs<br>31 : 32 ADCs |
| 1-0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |

### 8.1.4 Register 03h (offset = 3h) [reset = 2h]

**Figure 8-6. Register 03h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REG_BANK_SEL | | | | | | | |
| R/W-2h | | | | | | | |

**Figure 8-7. Register 03h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 7-0 | REG_BANK_SEL | R/W | 2h | Register bank selection for read and write operations.<br>0 : Select register bank 0<br>2 : Select register bank 1<br>16 : Select register bank 2 |

Copyright © 2025 Texas Instruments Incorporated

### 8.1.5 Register 04h (offset = 4h) [reset = 0h]

**Figure 8-8. Register 04h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INIT_1 | | | |
| R/W-0h | | | | | | | |

**Figure 8-9. Register 04h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | INIT_1 | R/W | 0h | INIT_1 field for device initialization. Write 1011b during the initialization sequence. Write 0000b for normal operation. |

### 8.1.6 Register 06h (offset = 6h) [reset = 2h]

**Figure 8-10. Register 06h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| REG_00H_READBACK | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REG_00H_READBACK | | | | | | | |
| R-5h | | | | | | | |

**Figure 8-11. Register 06h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | REG_00H_READBACK | R | 2h | This register is a copy of the register address 0x00 for readback. The register address 0x00 is write-only. The default readback value is 2h because SPI_RD_EN in address 0x00 is required to be set to 1 for register reads. |


Copyright © 2025 Texas Instruments Incorporated

## 8.2 Register Bank 1

**Figure 8-12. Register Bank 1 Map**

| ADD | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Dh | RESERVED | | DATA_FORMAT | RESERVED | | | LAT_INC | | GE_CAL_EN1 | OSR_EN | OSR | | | | RESERVED | |
| 10h | RESERVED | | | | | | | | | | | | | | | HI_FREQ |
| 12h | RESERVED | | | | | | | | | | | | XOR_EN | DATA_LANES | | |
| 13h | RESERVED | | | | | | | | RAMP_INC_A | | | | TP_MODE_CHA | | TP_EN_CHA | RESERVED |
| 14h | TP0_A | | | | | | | | | | | | | | | |
| 15h | TP1_A | | | | | | | | TP0_A | | | | | | | |
| 16h | TP1_A | | | | | | | | | | | | | | | |
| 18h | RESERVED | | | | | | | | RAMP_INC_B | | | | TP_MODE_CHB | | TP_EN_CHB | RESERVED |
| 19h | TP0_B | | | | | | | | | | | | | | | |
| 1Ah | TP1_B | | | | | | | | TP0_B | | | | | | | |
| 1Bh | TP1_B | | | | | | | | | | | | | | | |
| 1Ch | USER_BITS_ADC_B | | | | | | | | USER_BITS_ADC_A | | | | | | | |
| 33h | RESERVED | | GE_CAL_EN3 | RESERVED | | | | | | GE_CAL_EN2 | RESERVED | | | | | |
| 34h | RESERVED | | | | | | | | | | | LAT_EN | RESERVED | | | |
| 90h | RESERVED | TS_LD | RESERVED | | | | | | | | | | | | | |
| 91h | RESERVED | | | | | | TEMPERATURE_SENSOR | | | | | | | | | |
| C0h | RESERVED | | | CLK1 | OSR_INIT1 | | OSR_CLK | | | RESERVED | | | | | PD_CH | |
| C1h | RESERVED | | | | PD_REF | RESERVED | | DATA_RATE | RESERVED | | | | | | | CLK2 |
| C4h | RESERVED | | | | | | | | | | OSR_INIT2 | | RESERVED | | OSR_INIT3 | PD_CHIP |
| C5h | RESERVED | | HI_FREQ_EN | RESERVED | | | CLK3 | RESERVED | | RD_CLK | | RESERVED | CLK4 | | RESERVED | |
| FBh | RESERVED | | | | | | | | | | | | NCO_SYSREF | XOR_MODE | CLK5 | MIXER_EN |
| FCh | NCO_PHASE_COUNT[15:0] | | | | | | | | | | | | | | | |
| FDh | NCO_FREQUENCY[7:0] | | | | | | | | NCO_PHASE_COUNT[23:16] | | | | | | | |
| FEh | NCO_FREQUENCY[23:8] | | | | | | | | | | | | | | | |

**Table 8-2. Register Section/Block Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| W | W | Write |
| R/W | R/W | Read or write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 8.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

**Figure 8-13. Register 0Dh**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | DATA_FORMAT | RESERVED | | | LAT_INC | |
| R/W-0h | | R/W-1h | R/W-0h | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GE_CAL_EN1 | OSR_EN | OSR | | | | RESERVED | |
| R/W-0h | R/W-0h | R/W-0h | | | | R/W-2h | |

**Figure 8-14. Register 0Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 13 | DATA_FORMAT | R/W | 1h | Select data format for the ADC conversion result.<br>0 : Straight binary format<br>1 : Two's-complement format |
| 12-10 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 9-8 | LAT_INC | R/W | 0h | For ADS9229, set this field to 11b for optimum INL performance. |
| 7 | GE_CAL_EN1 | R/W | 0h | Global control for gain error calibration.<br>0 : Gain error calibration disabled for all channels<br>1 : Gain error calibration enabled for all channels |
| 6 | OSR_EN | R/W | 0h | Control for data averaging depth.<br>0 : Data averaging disabled<br>1 : Data averaging enabled |
| 5-2 | OSR | R/W | 0h | Control for enabling data averaging.<br>0 : 2 samples averaged<br>1 : 4 samples averaged<br>2 : 8 samples averaged<br>3 : 16 samples averaged |
| 1-0 | RESERVED | R/W | 2h | Reserved. Do not change from the default reset value. |

### 8.2.2 Register 10h (offset = 10h) [reset = 0h]

**Figure 8-15. Register 10h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | RESERVED |
| R/W-0h | | | | | | | R/W-0h |

**Figure 8-16. Register 10h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-1 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 0 | HI_FREQ | R/W | 0h | Analog input fast slew rate control<br>0: Normal slew rate<br>1: Fast slew rate. Fast analog input control enabled. Recommended for input frequencies >2MHz.See also HI_FREQ_EN. |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.3 Register 12h (offset = 12h) [reset = 2h]

**Figure 8-17. Register 12h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | XOR_EN | DATA_LANES | | |
| R/W-0h | | | | R/W-0h | R/W-2h | | |

**Figure 8-18. Register 12h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-4 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 3 | XOR_EN | R/W | 0h | Enables XOR operation on ADC conversion result.<br>0 : XOR operation is disabled<br>1 : ADC conversion result is bit-wise XOR with the PRBS bit by default |
| 2-0 | DATA_LANES | R/W | 2h | Selects the number of output data lanes and number of data bits per output lane. Enables XOR operation on ADC conversion result.<br>0 : ADC A and B data output on DOUTA and DOUTB respectively; 20 bits per ADC.<br>2 : ADC A and B data output on DOUTA and DOUTB respectively; 24 bits per ADC.<br>5 : ADC A and B data output on DOUTA; 20 bits per ADC.<br>7 : ADC A and B data output on DOUTA; 24 bits per ADC. |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.4 Register 13h (offset = 13h) [reset = 0h]

**Figure 8-19. Register 13h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMP_INC_A | | | | TP_MODE_A | | TP_EN_A | RESERVED |
| R/W-0h | | | | R/W-0h | | R/W-0h | R/W-0h |

**Figure 8-20. Register 13h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 7-4 | RAMP_INC_A | R/W | 0h | Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register. |
| 3-2 | TP_MODE_A | R/W | 0h | Select digital test pattern for ADC A.<br>0 : Fixed pattern from the TP0_A register<br>1 : Fixed pattern from the TP0_A register<br>2 : Digital ramp output<br>3 : Alternate fixed pattern output from the TP0_A and TP1_A registers |
| 1 | TP_EN_A | R/W | 0h | Enable digital test pattern for data corresponding to ADC A.<br>0 : Data output is the ADC conversion result<br>1 : Data output is the digital test pattern for ADC A |
| 0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |

### 8.2.5 Register 14h (offset = 14h) [reset = 0h]

**Figure 8-21. Register 14h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TP0_A[15:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TP0_A[15:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-22. Register 14h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | TP0_A[15:0] | R/W | 0h | Lower 16 bits of test pattern 0 |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.6 Register 15h (offset = 15h) [reset = 0h]

**Figure 8-23. Register 15h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TP1_A[7:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TP0_A[23:16] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-24. Register 15h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | TP1_A[7:0] | R/W | 0h | Lower eight bits of test pattern 1 |
| 7-0 | TP0_A[23:16] | R/W | 0h | Upper eight bits of test pattern 0 |

### 8.2.7 Register 16h (offset = 16h) [reset = 0h]

**Figure 8-25. Register 16h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TP1_A[23:8] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TP1_A[23:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-26. Register 16h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | TP1_A[23:8] | R/W | 0h | Upper 16 bits of test pattern 1 |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.8 Register 18h (offset = 18h) [reset = 0h]

**Figure 8-27. Register 18h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMP_INC_B | | | | TP_MODE_B | | TP_EN_B | RESERVED |
| R/W-0h | | | | R/W-0h | | R/W-0h | R/W-0h |

**Figure 8-28. Register 18h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 7-4 | RAMP_INC_B | R/W | 0h | Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register. |
| 3-2 | TP_MODE_B | R/W | 0h | Select digital test pattern for ADC B.<br>0 : Fixed pattern from the TP0_B register<br>1 : Fixed pattern from the TP0_B register<br>2 : Digital ramp output<br>3 : Alternate fixed pattern output from the TP0_B and TP1_B registers |
| 1 | TP_EN_B | R/W | 0h | Enable digital test pattern for data corresponding to ADC B.<br>0 : Data output is the ADC conversion result<br>1 : Data output is the digital test pattern |
| 0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |

### 8.2.9 Register 19h (offset = 19h) [reset = 0h]

**Figure 8-29. Register 19h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TP0_B[15:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TP0_B[15:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-30. Register 19h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | TP0_B[15:0] | R/W | 0h | Lower 16 bits of test pattern 0 |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.10 Register 1Ah (offset = 1Ah) [reset = 0h]

**Figure 8-31. Register 1Ah**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TP1_B[7:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TP0_B[23:16] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-32. Register 1Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | TP1_B[7:0] | R/W | 0h | Lower eight bits of test pattern 1 |
| 7-0 | TP0_B[23:16] | R/W | 0h | Upper eight bits of test pattern 0 |

### 8.2.11 Register 1Ch (offset = 1Ch) [reset = 0h]

**Figure 8-33. Register 1Ch**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| USER_BITS_ADC_B | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| USER_BITS_ADC_A | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-34. Register 1Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | USER_BITS_ADC_B | R/W | 0h | User-defined bits appended to the ADC conversion result from ADC B. |
| 7-0 | USER_BITS_ADC_A | R/W | 0h | User-defined bits appended to the ADC conversion result from ADC A. |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.12 Register 33h (offset = 33h) [reset = 0h]

**Figure 8-35. Register 33h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | GE_CAL_EN3 | RESERVED | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | GE_CAL_EN2 | RESERVED | | | | | |
| R/W-0h | R/W-0h | R/W-0h | | | | | |

**Figure 8-36. Register 33h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 13 | GE_CAL_EN3 | R/W | 0h | Global control for gain error calibration.<br>0 : Gain error calibration disabled for all channels<br>1 : Gain error calibration enabled for all channels |
| 12-7 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 6 | GE_CAL_EN2 | R/W | 0h | Global control for gain error calibration.<br>0 : Gain error calibration disabled for all channels<br>1 : Gain error calibration enabled for all channels |
| 5-0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |

### 8.2.13 Register 34h (offset = 34h) [reset = 0h]

**Figure 8-37. Register 34h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | LAT_EN | RESERVED | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |

**Figure 8-38. Register 34h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-5 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 4 | LAT_EN | R/W | 0h | For ADS9229, set this field to 11b for optimum INL performance. |
| 3-0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.14 Register 90h (offset = 90h) [reset = 0h]

**Figure 8-39. Register 90h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | TS_LD | RESERVED | | | | | |
| R/W-0h | R/W-0h | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-40. Register 90h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 14 | TS_LD | R/W | 0h | Trigger to load temperature sensor output in address 0x91. Transition from 0 to 1 if this bit triggers the data load operation. |
| 13-0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |

### 8.2.15 Register 91h (offset = 91h) [reset = 00h]

**Figure 8-41. Register 91h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | TEMPERATURE_SENSOR | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMPERATURE_SENSOR | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-42. Register 91h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-10 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 9-0 | TEMPERATURE_SENSOR | R/W | 0h | 10-bit temperature sensor output. See the *Temperature Sensor* section. |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.16 Register C0h (offset = C0h) [reset = 0h]

**Figure 8-43. Register C0h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | CLK1 | OSR_INIT1 | | OSR_CLK | |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OSR_CLK | RESERVED | | | | | PD_CH | |
| R/W-0h | R/W-0h | | | | | R/W-0h | |

**Figure 8-44. Register C0h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-13 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 12 | CLK1 | R/W | 0h | Selects the clock configuration based on output data-lanes.<br>0 : Configuration for DATA_LANES = 0 or 2<br>1 : Configuration for DATA_LANES = 5 or 7 |
| 11-10 | OSR_INIT1 | R/W | 0h | Initialization for data averaging.<br>0 : Configuration for disabling data averaging<br>1 : Configuration for enabling data averaging |
| 9-7 | OSR_CLK | R/W | 0h | Data output clock configuration for data averaging. See Table 7-4 for more details. |
| 6-2 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 1-0 | PD_CH | R/W | 0h | Power-down control for the analog input channels.<br>0 : Normal operation<br>1 : ADC A powered down<br>2 : ADC B powered down<br>3 : ADC A and B powered down |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.17 Register C1h (offset = C1h) [reset = 0h]

**Figure 8-45. Register C1h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PD_REF | RESERVED | | DATA_RATE |
| R/W-0h | | | | R/W-0h | R/W-0h | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | CLK2 |
| R/W-0h | | | | | | | R/W-0h |

**Figure 8-46. Register C1h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-12 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 11 | PD_REF | R/W | 0h | ADC reference voltage source selection.<br>0 : Internal reference enabled.<br>1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin. |
| 10-9 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 8 | DATA_RATE | R/W | 0h | Select data rate for the data interface.<br>0 : Double data rate (DDR)<br>1 : Single data rate (SDR) |
| 7-1 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 0 | CLK2 | R/W | 0h | Select data rate for the data interface.<br>0 : Configuration for DATA_LANES = 2 or 7<br>1 : Configuration for DATA_LANES = 0 or 5 |

### 8.2.18 Register C4h (offset = C4h) [reset = 0h]

**Figure 8-47. Register C4h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | OSR_INIT2 | | RESERVED | | OSR_INIT3 | PD_CHIP |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | R/W-0h |

**Figure 8-48. Register C4h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-6 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 5-4 | OSR_INIT2 | R/W | 0h | Initialization for data averaging.<br>0 : Configuration for disabling data averaging<br>2 : Configuration for enabling data averaging |
| 3-2 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 1 | OSR_INIT3 | R/W | 0h | Initialization for data averaging.<br>0 : Configuration for disabling data averaging<br>1 : Configuration for enabling data averaging |
| 0 | PD_CHIP | R/W | 0h | Full chip power-down control.<br>0 : Normal device operation<br>1 : Full device powered-down |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.19 Register C5h (offset = C5h) [reset = 0h]

**Figure 8-49. Register C5h**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | HI_FREQ_EN | RESERVED | | | CLK3 | RESERVED |
| R/W-0h | | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | RD_CLK | | RESERVED | CLK4 | | RESERVED | |
| R/W-0h | R/W-0h | | R/W-0h | R/W-0h | | R/W-0h | |

**Figure 8-50. Register C5h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 13 | HI_FREQ_EN | R/W | 0h | Fast analog input slew rate enable.<br>0: Normal slew rate<br>1: Fast analog input control enabled. Recommended for input frequencies >2MHz. See also HI_FREQ. |
| 12-10 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 9 | CLK3 | R/W | 0h | Select data rate for the data interface.<br>0 : Configuration for DATA_LANES = 0 or 2<br>1 : Configuration for DATA_LANES = 5 or 7 |
| 8 - 7 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 6-5 | RD_CLK | R/W | 0h | Data output clock control for data averaging. See Data Averaging for more details. |
| 4 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 3 - 2 | CLK4 | R/W | 0h | Clock configuration for ADS9227. See the *Data Interface* section for details. Not applicable for ADS9229 and ADS9228.<br>0 : 24-bit 2-lane mode<br>3 : all other modes |
| 1 - 0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.20 Register FBh (offset = FBh) [reset = 0h]

**Figure 8-51. Register FBh**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | NCO_SYSREF | XOR_MODE | CLK5 | MIXER_EN |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Figure 8-52. Register FBh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-4 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 3 | NCO_SYSREF | R/W | 0h | Set to 1b when applying periodic pulses on the SMPL_SYNC pin.<br>0: Synchronize the NCO with one pulse on the SMPL_SYNC pin.<br>1: Synchronize the NCO with the first pulse on the SMPL_SYNC pin when using periodic pulses. |
| 2 | XOR_MODE | R/W | 0h | Selects the bit with which the ADC output data is XORed when XOR output mode is enabled.<br>0 : PRBS bit is output after the ADC LSB. ADC output data is XORed with the PRBS bit.<br>1 : ADC output data is XORed with the LSB of the conversion result. |
| 1 | CLK5 | R/W | 0h | Clock configuration for the ADS9229 and ADS9228. See the *Data Interface* section for details. Not applicable for the ADS9227.<br>0 : 24-bit 2-lane SDR and DDR modes<br>1 : 24-bit 1-lane SDR and DDR modes |
| 0 | MIXER_EN | R/W | 0h | 0: Digital down converter disabled<br>1: Digital down converter enabled |

Copyright © 2025 Texas Instruments Incorporated

### 8.2.21 Register FCh (offset = FCh) [reset = 0h]

**Figure 8-53. Register FCh**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NCO_PHASE_COUNT | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_PHASE_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-54. Register FCh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | NCO_PHASE_COUNT[15:0] | R/W | 0h | Lower 15 bits of the NCO phase count. See the *Digital Down Converter* section. |

### 8.2.22 Register FDh (offset = FDh) [reset = 0h]

**Figure 8-55. Register FDh**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NCO_FREQUENCY | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_PHASE_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-56. Register FDh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | NCO_FREQUENCY[7:0] | R/W | 0h | Lower eight bits of the NCO phase count. See the *Digital Down Converter* section. |
| 7-0 | NCO_PHASE_COUNT[23:16] | R/W | 0h | Higher eight bits of the NCO phase count. See the *Digital Down Converter* section. |


Copyright © 2025 Texas Instruments Incorporated

### 8.2.23 Register FEh (offset = FEh) [reset = 0h]

**Figure 8-57. Register FEh**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NCO_FREQUENCY | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_FREQUENCY | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 8-58. Register FEh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | NCO_FREQUENCY | R/W | 0h | Higher 16 bits of the NCO phase count. See the *Digital Down Converter* section. |

## 8.3 Register Bank 2

**Figure 8-59. Register Bank 2 Map**

| ADD | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1Ch | RESERVED | | | | | | | | CLK6 | | RESERVED | | | | | |

**Table 8-3. Register Section/Block Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| W | W | Write |
| R/W | R/W | Read or write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 8.3.1 Register 1Ch (offset = 1Ch) [reset = 0h]

**Figure 8-60. Register 1Ch**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK6 | | RESERVED | | | | | |
| R/W-0h | | R/W-0h | | | | | |

**Figure 8-61. Register 1Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |
| 7-6 | CLK6 | R/W | 0h | Clock configuration for ADS9227. See the *Data Interface* section for details. Not applicable for the ADS9229 and ADS9228.<br>0 : 24-bit 2-lane mode<br>3 : all other modes |
| 5-0 | RESERVED | R/W | 0h | Reserved. Do not change from the default reset value. |


Copyright © 2025 Texas Instruments Incorporated

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The ADS922x features an integrated ADC driver, low-latency, high-speed, low AC and DC errors, and low temperature drift. These features make the ADS922x a high-performance signal-chain for applications where precision measurements with low-latency are required. The following section gives an example circuit and recommendations for using the ADS922x device family in a data acquisition (DAQ) system.

## 9.2 Typical Applications

### *9.2.1 Data Acquisition (DAQ) Circuit for ≤20kHz Input Signal Bandwidth*

Figure 9-1 shows a 2-channel signal chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS922x with the 2-channel, fully differential amplifier (FDA) THS4552.

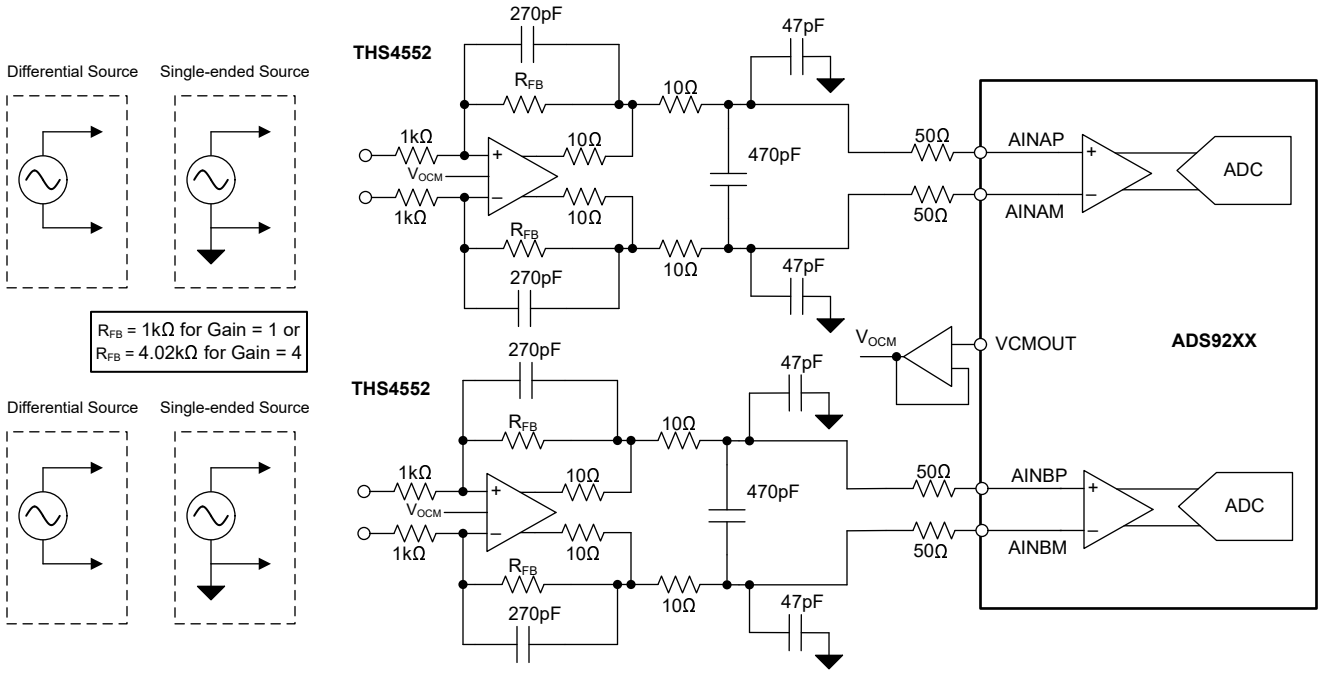



**Figure 9-1. Data Acquisition (DAQ) Circuit for ≤20kHz Input Signal Bandwidth**

#### 9.2.1.1 Design Requirements

Table 9-1 lists the parameters for this typical application.

**Table 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| SNR | ≥ 92dB |
| THD | ≤ –110dB |
| Input signal frequency | ≤ 20kHz |

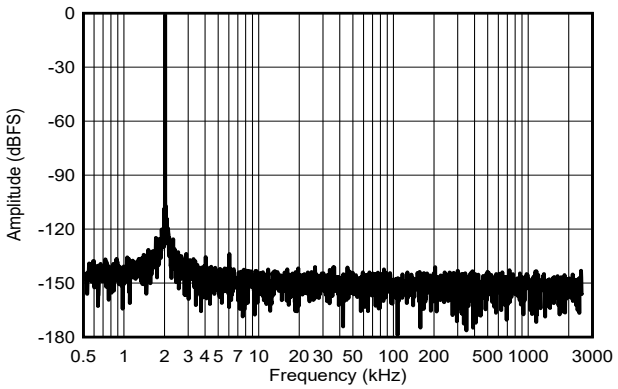
#### 9.2.1.2 Detailed Design Procedure

Use the procedure discussed in this section for any ADS922x application circuit.

- All ADS922x applications require the supply decoupling as provided in the *Power Supply Recommendations* section.
- Make sure the values provided in this section meet the maximum throughput and input signal frequency design requirements given. Use a lower bandwidth signal chain when lower noise performance is required.

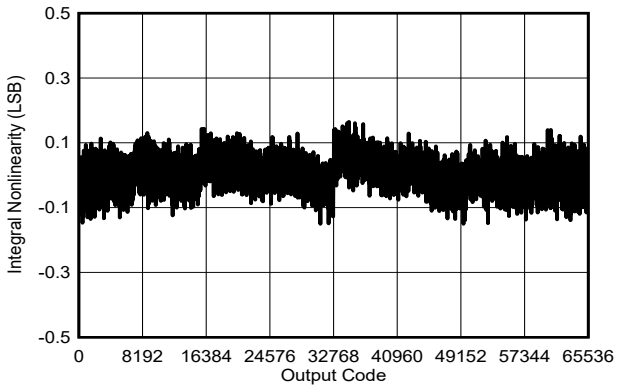
#### 9.2.1.3 Application Curves

The following figures show the SNR and INL performance for the circuit in Figure 9-1, respectively.




$f_{IN}$ = 2kHz, SNR = 93.9dBFS, THD = –122.5dB

**Figure 9-2. Typical FFT for $f_{IN}$ = 2kHz**




Typical INL = ±0.2LSB

**Figure 9-3. Typical INL**


Copyright © 2025 Texas Instruments Incorporated

### 9.2.2 Data Acquisition (DAQ) Circuit for ≤100kHz Input Signal Bandwidth

Figure 9-4 shows a 2-channel signal chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS922x with the 2-channel, fully differential amplifier (FDA) THS4552.

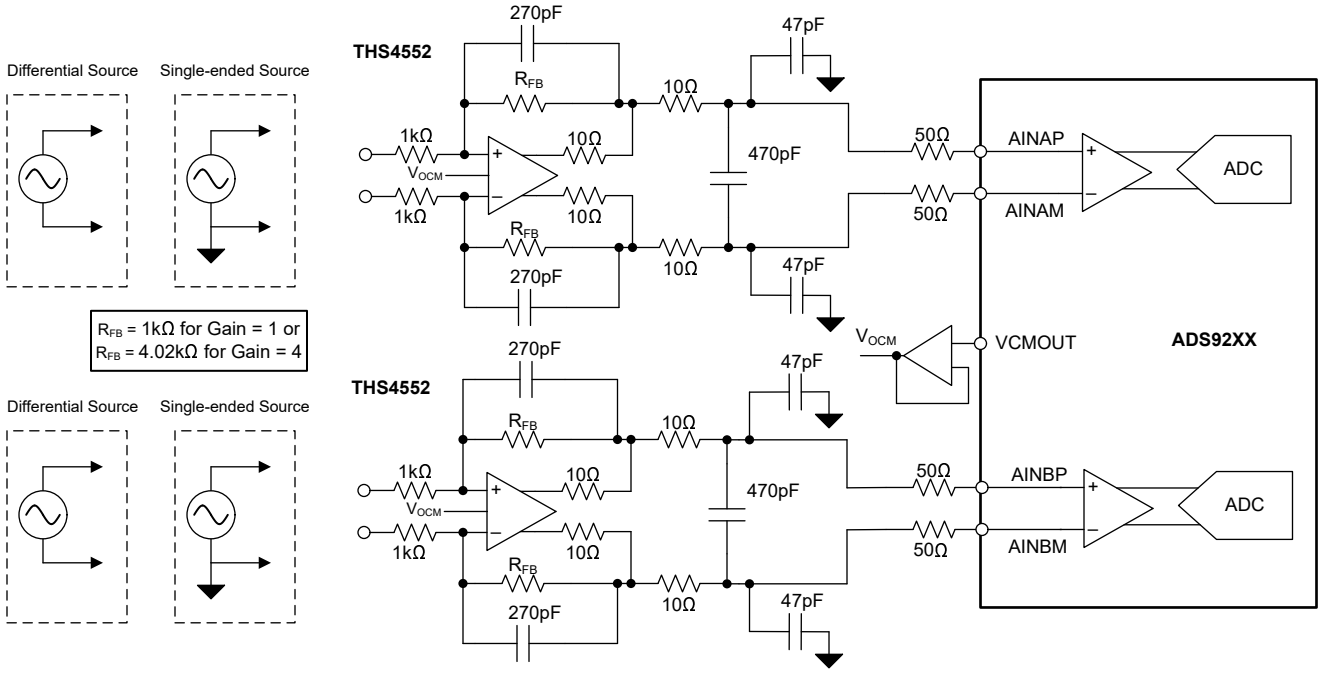



**Figure 9-4. Data Acquisition (DAQ) Circuit for ≤100kHz Input Signal Bandwidth**

#### 9.2.2.1 Design Requirements

Table 9-2 lists the parameters for this typical application.

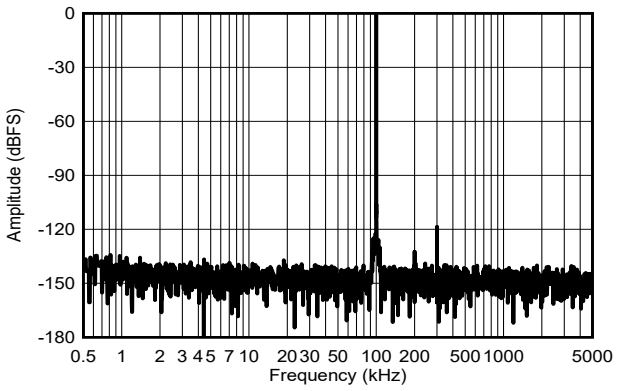
**Table 9-2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| SNR | ≥ 91dB |
| THD | ≤ –110dB |
| Input signal frequency | ≤ 100kHz |

Copyright © 2025 Texas Instruments Incorporated

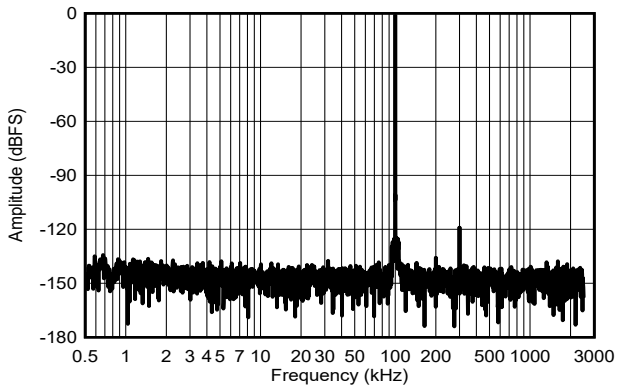
#### 9.2.2.2 Application Curves

The following figures show the FFT plots for the circuit in Figure 9-4.




$f_{IN}$ = 100kHz, SNR = 92dB, THD = –117dB

**Figure 9-5. Typical FFT at 10MSPS/Channel: ADS9228**




$f_{IN}$ = 100kHz, SNR = 92dB, THD = –117dB

**Figure 9-6. Typical FFT at 5MSPS/Channel: ADS9227**

### *9.2.3 Data Acquisition (DAQ) Circuit for ≤1MHz Input Signal Bandwidth*

Figure 9-7 shows a 2-channel solution with minimum external components. This signal-chain significantly reduces signal-chain size by driving the ADS9229 with the THS4541, which enables low-distortion performance with low power over wide signal bandwidth.

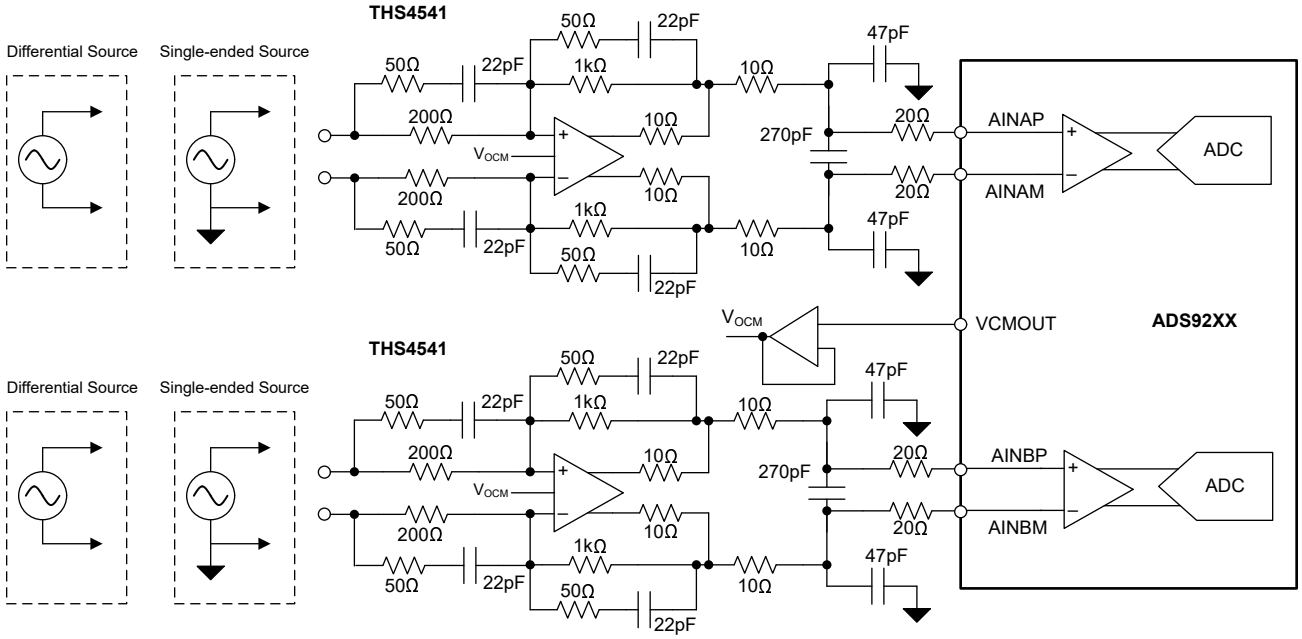



**Figure 9-7. Data Acquisition (DAQ) Circuit for ≤1MHz Input Signal Bandwidth**


Copyright © 2025 Texas Instruments Incorporated

#### 9.2.3.1 Design Requirements

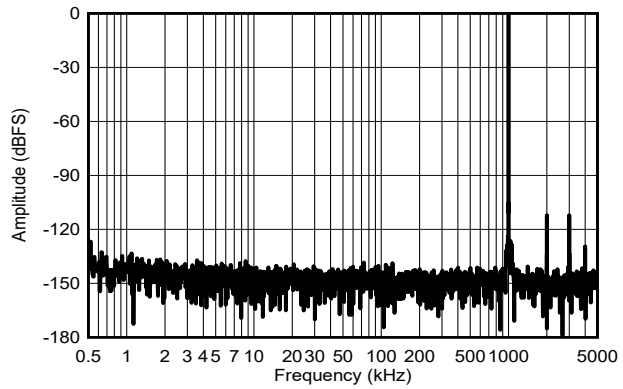
Table 9-3 lists the parameters for this typical application.

**Table 9-3. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| SNR | ≥ 80dB |
| THD | ≤ –100dB |
| Input signal frequency | ≤ 1MHz |

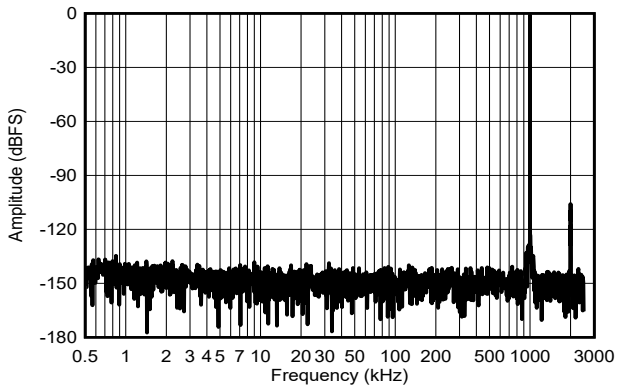
#### 9.2.3.2 Application Curves

The following figures show the FFT plots for the circuit in Figure 9-7.




$f_{IN}$ = 1MHz, SNR = 93.3dB, THD = –104dB

**Figure 9-8. Typical FFT at 10MSPS/Channel: ADS9228**




$f_{IN}$ = 1MHz, SNR = 90.5dB, THD = –104.2dB

**Figure 9-9. Typical FFT at 5MSPS/Channel: ADS9227**

Copyright © 2025 Texas Instruments Incorporated

## 9.3 Power Supply Recommendations

The ADS922x has three independent power supplies, AVDD_5V and VDD_1V8. The AVDD_5V supply provides power to the ADC driver. The VDD_1V8 provides power to the analog circuits and the digital interface. Set the AVDD_5 and VDD_1V8 supplies independently to voltages within the permissible range. Figure 9-10 shows how to decouple the power supplies.

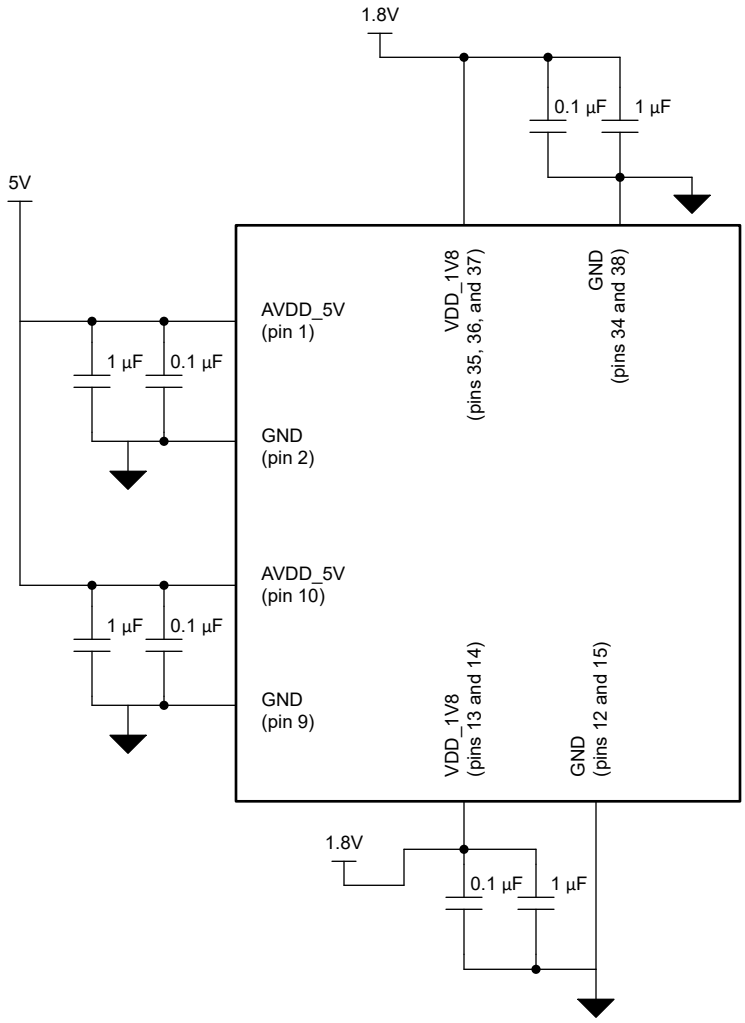



**Figure 9-10. Power-Supply Decoupling**


Copyright © 2025 Texas Instruments Incorporated

## 9.4 Layout

### 9.4.1 Layout Guidelines

Figure 9-11 shows a board layout example for the ADS922x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 0.1µF ceramic bypass capacitors in close proximity to the analog (AVDD_5V and VDD_1V8), and digital (VDD_1V8) power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors. Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

### 9.4.2 Layout Example

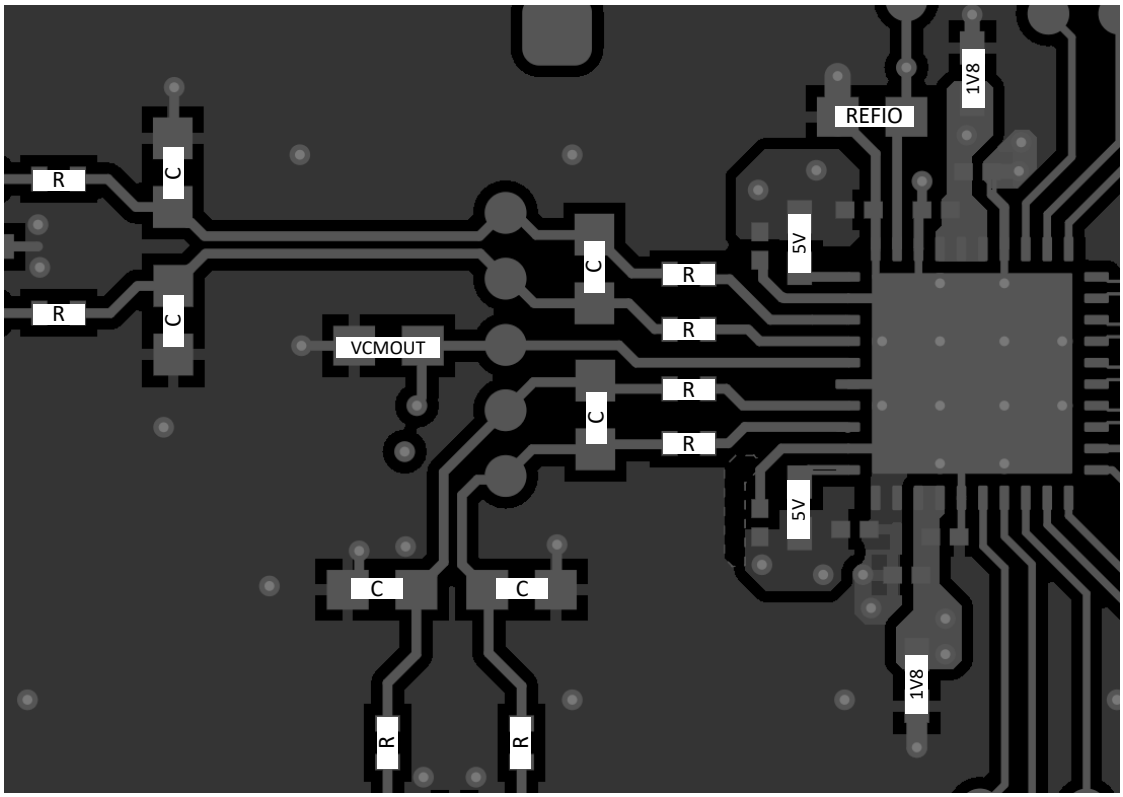



**Figure 9-11. Example Layout**

# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### *10.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *REF70 2 ppm/°C Maximum Drift, 0.23 $ppm_{p-p}$ 1/f Noise, Precision Voltage Reference*, data sheet
- Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier*, data sheet
- Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier*, data sheet

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |


Copyright © 2025 Texas Instruments Incorporated

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (August 2024) to Revision C (March 2025) | Page |
|---|---|
| • Changed ADS9229 from *Advance Information* to *Production Data*, added ADS9228 to document | 1 |
| • Changed *Device Block Diagram* figure | 1 |
| • Added *Device Comparison Table* | 3 |
| • Added *Sampling Edge to Corresponding Data MSB Output Timing* diagram | 12 |
| • Changed *Typical Characteristics: All Devices* section | 15 |
| • Changed *Typical Characteristics: ADS9229* section | 17 |
| • Changed condition statement for *Typical Characteristics: ADS9228* and SNR value in *Typical FFT for $f_{IN}$ = 1MHz* condition statement | 18 |
| • Changed condition statement of *Typical Characteristics: ADS9227* section and SNR value of *Typical FFT for $f_{IN}$ = 1MHz* condition statement | 19 |
| • Changed power consumption value from *187mW/ch* to *230mW/ch* in *Overview* section | 20 |
| • Changed *Transfer Characteristics* table | 21 |
| • Changed *Data Averaging* section | 23 |
| • Added OSR_RD (0xC5[6:5]) register row to *Decimation Settings for the DDC* table | 24 |
| • Changed *Register Map Settings for Output Data Interface for the ADS9229 and ADS9228* table and changed *Data Interface* subsections | 26 |
| • Changed *Test Patterns for Data Interface* section | 29 |
| • Changed *IOVDD* to *VDD_1V8* and *Single-Ended Sampling Clock* figure in *ADC Sampling Clock Input* | 30 |
| • Changed *Reset* section | 31 |
| • Changed *Power-Down Options* section | 31 |
| • Changed *Initialization Sequence* section | 31 |
| • Changed 0Dh, 33h, C5h registers, added 10h, 34h registers, deleted F4h, F6h registers | 39 |
| • Changed description of bit setting 1 for XOR_EN (bit 3) in register 12 of register bank 1 | 39 |
| • Changed *Register Bank 2* | 54 |
| • Changed *Application Curves* section in *Data Acquisition (DAQ) Circuit for ≤20kHz Input Signal Bandwidth* application | 56 |
| • Changed *Typical FFT at 10MSPS/Channel: ADS9228* figure in *Application Curves* section | 58 |
| • Changed SNR value from90.6dB to 93.3dB in *Typical FFT at 10MSPS/Channel: ADS9228* condition statement | 59 |
| • Changed *Power Supply Recommendations* section | 60 |
| • Changed *Example Layout* figure | 61 |

| Changes from Revision A (June 2024) to Revision B (August 2024) | Page |
|---|---|
| • Changed ADS9229 from *Preview* to *Advance Information* | 1 |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2025 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS9227RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS9227 |
| ADS9227RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS9227 |
| ADS9228RHAR | Active | Production | VQFN (RHA) \| 40 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS9228 |
| ADS9228RHAR.A | Active | Production | VQFN (RHA) \| 40 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | See ADS9228RHAR | ADS9228 |
| ADS9229RHAR | Active | Production | VQFN (RHA) \| 40 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS9229 |
| ADS9229RHAR.A | Active | Production | VQFN (RHA) \| 40 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | See ADS9229RHAR | ADS9229 |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

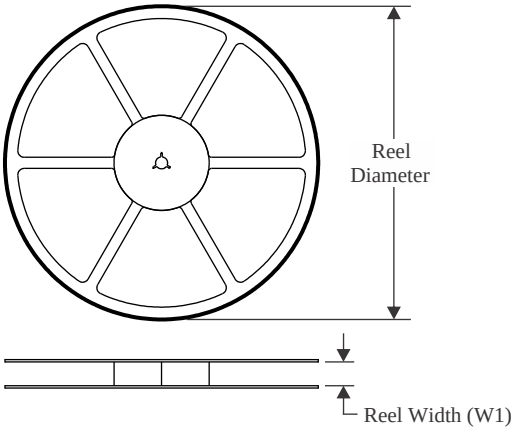
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

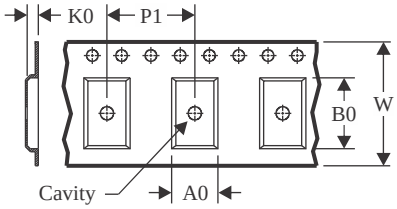
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

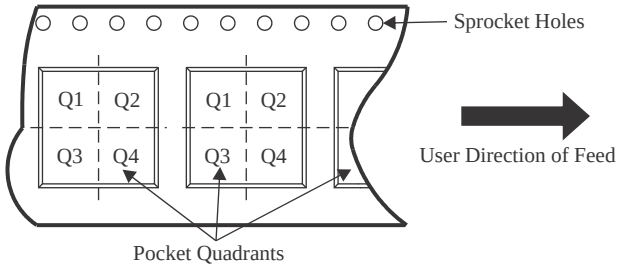



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

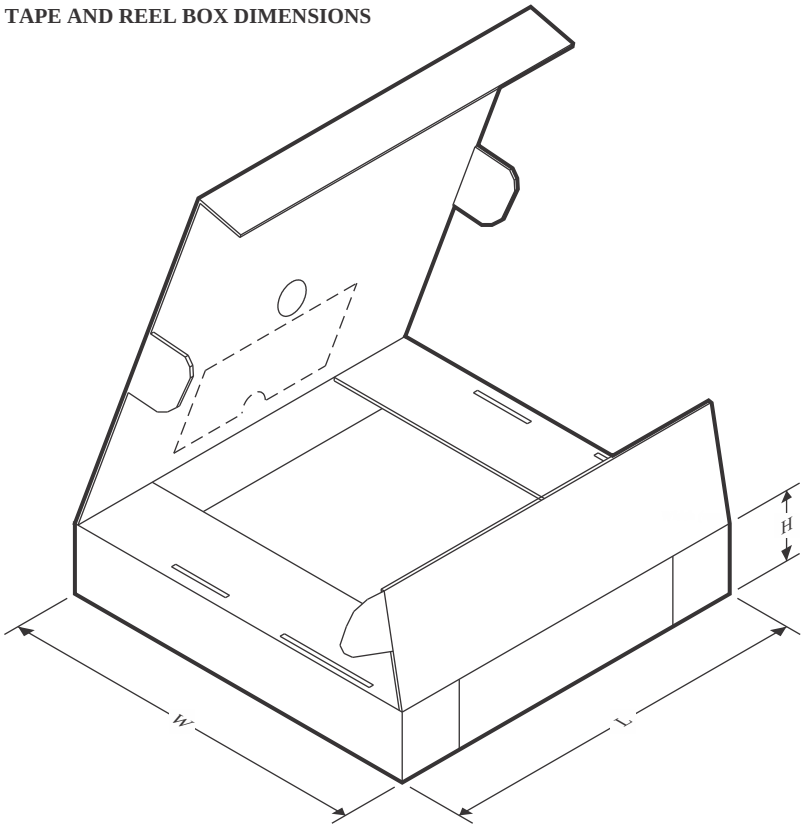
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS9227RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| ADS9228RHAR | VQFN | RHA | 40 | 4000 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| ADS9229RHAR | VQFN | RHA | 40 | 4000 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS9227RHAR | VQFN | RHA | 40 | 2500 | 360.0 | 360.0 | 36.0 |
| ADS9228RHAR | VQFN | RHA | 40 | 4000 | 360.0 | 360.0 | 36.0 |
| ADS9229RHAR | VQFN | RHA | 40 | 4000 | 360.0 | 360.0 | 36.0 |

# GENERIC PACKAGE VIEW

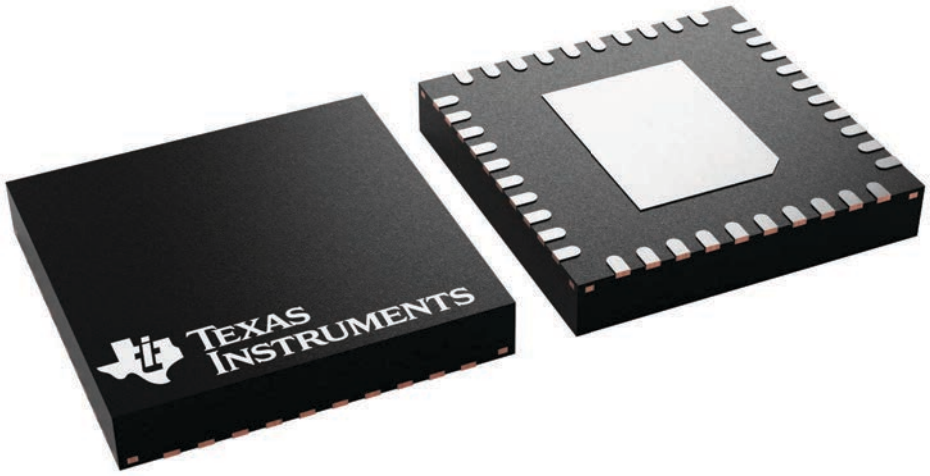
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



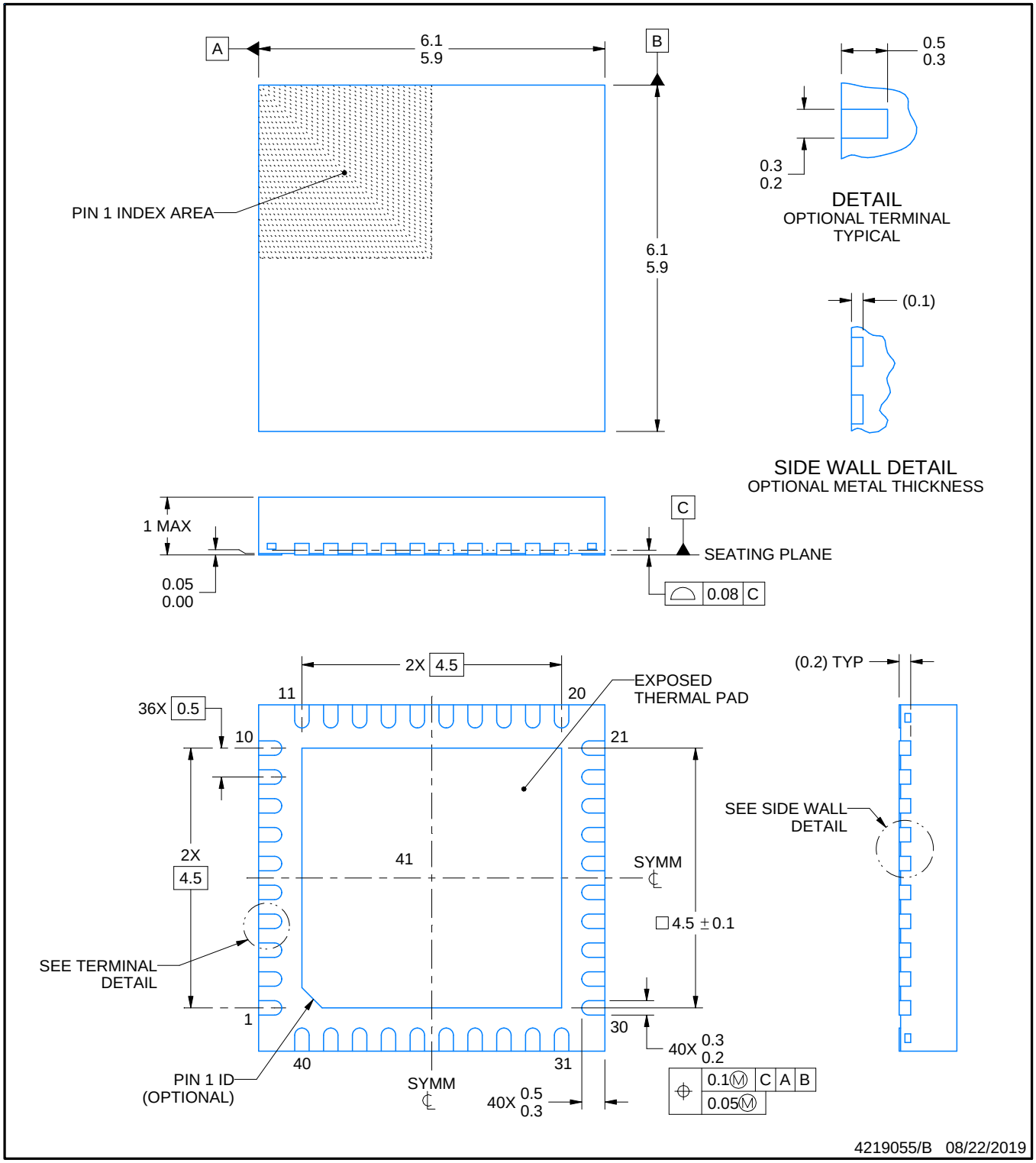

4225870/A

# PACKAGE OUTLINE

## RHA0040H

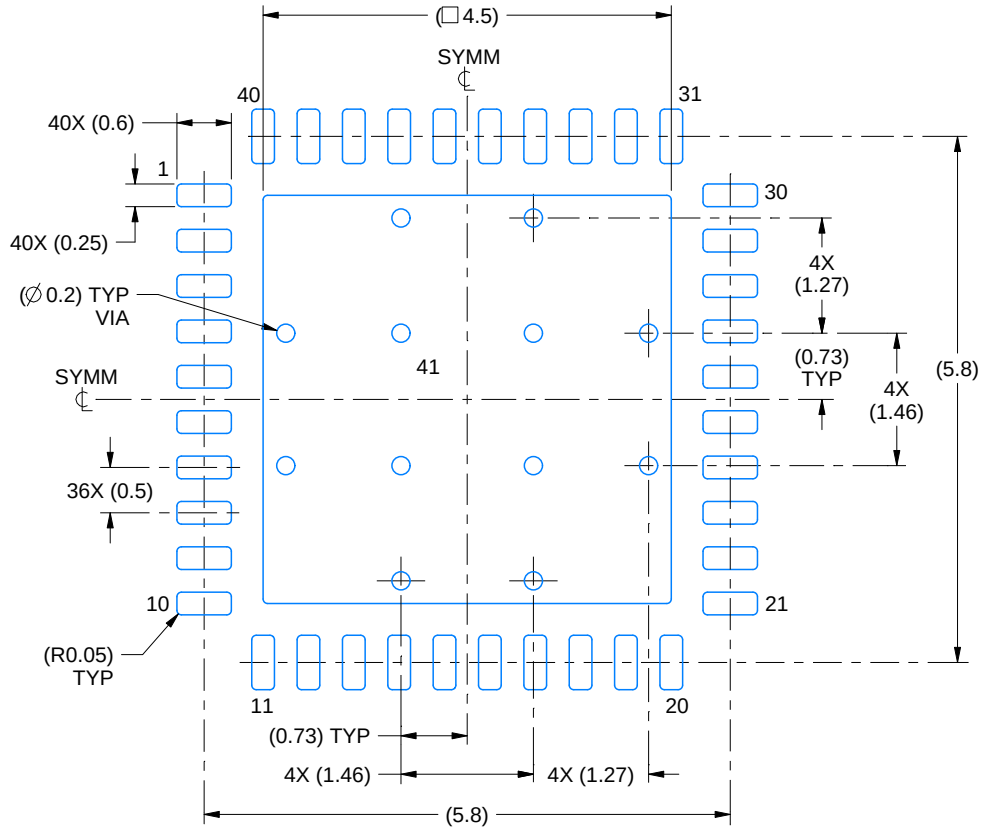
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

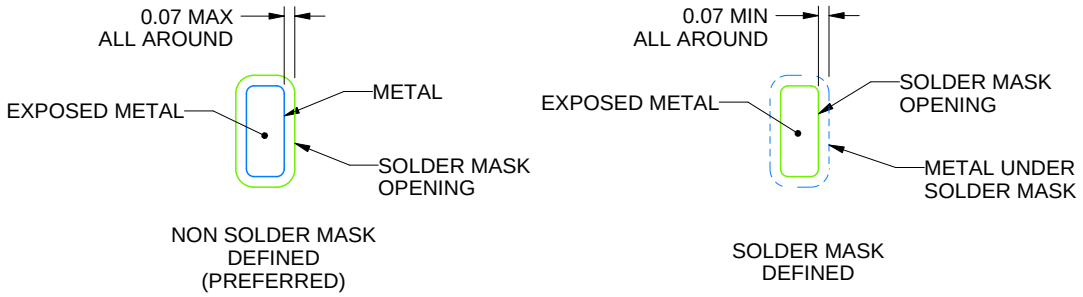



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

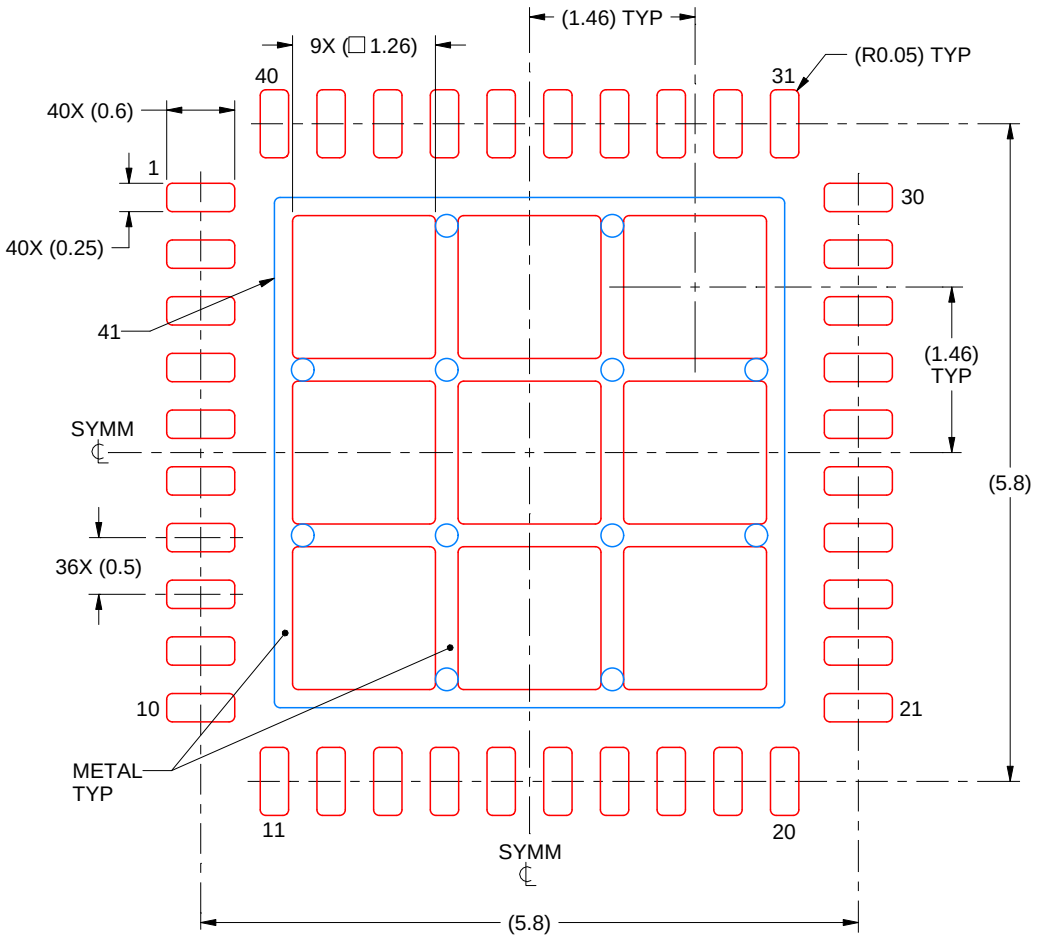



SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025