AFE5832LP 32-Channel Ultrasound AFE With 18.5-mW/Channel Power, 4-nV/√Hz, 12-Bit, 40-MSPS or 10-Bit, 50-MSPS Output and Passive CW Mixer

1 Features

- 32-Channel AFE for Ultrasound Applications:
  - LNA, Attenuator, LPF, ADC, and CW Mixer
  - Digital Time Gain Compensation (DTGC)
  - Total Gain Range: 0 dB to 48 dB
- Low-Noise Amplifier (LNA) With Programmable Gain:
  - Low Current Noise of 1pA/rtHz
  - Gain: 21 dB, 18 dB, and 15 dB
  - Linear Input Range: up to 700 mV_{PP}
- Programmable Attenuator (ATTEN):
  - Attenuation Range (Steps of 0.125 dB): 0 to 36 dB
  - Digital TGC Engine
- Programmable Gain Amplifier (PGA):
  - Gain: 21 dB, 24 dB, and 27 dB
- Third-Order, Linear-Phase, Low-Pass Filter (LPF):
  - Cut-off Frequency From 10 MHz to 25 MHz
- 16 ADCs Converting at 12-Bit, 80 MSPS or 10-Bit, 100 MSPS:
  - Each ADC Converts Two Sets of Inputs at Half Rate
  - 12-Bit Mode: 72-dBFS SNR
  - 10-Bit Mode: 61-dBFS SNR
- TGC Mode Power :
  - Lowest Power of 18.5 mW/Ch in Low Power Mode, 4 nV/rtHz, 10-Bit, 20 MSPS, LVDS (2x rate)
  - 27.8 mW/Ch at 3 nV/√Hz in Low Noise Mode at 12-Bit, 40 MSPS
  - 24.4 mW/Ch at 4 nV/√Hz in Low Power Mode at 12-Bit, 40 MSPS
- Excellent Device-to-Device Gain Matching:
  - ±0.5 dB (Typical)
- Harmonic Distortion: –55 dBc level
- Fast and Consistent Overload Recovery
- Continuous Wave (CW) Path With:
  - Low Close-In Phase Noise of –148 dBc/Hz at 1-kHz Frequency Offset off 5-MHz Carrier
  - Power Consumption With No Signal: 10 mW/Ch
  - Phase Resolution: λ/16
  - 12-dB Suppression on Third and Fifth Harmonics
- LVDS Interface with a Speed Up to 1-Gbps
- Small Package: 15-mm × 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment
- In-Probe Electronics

3 Description

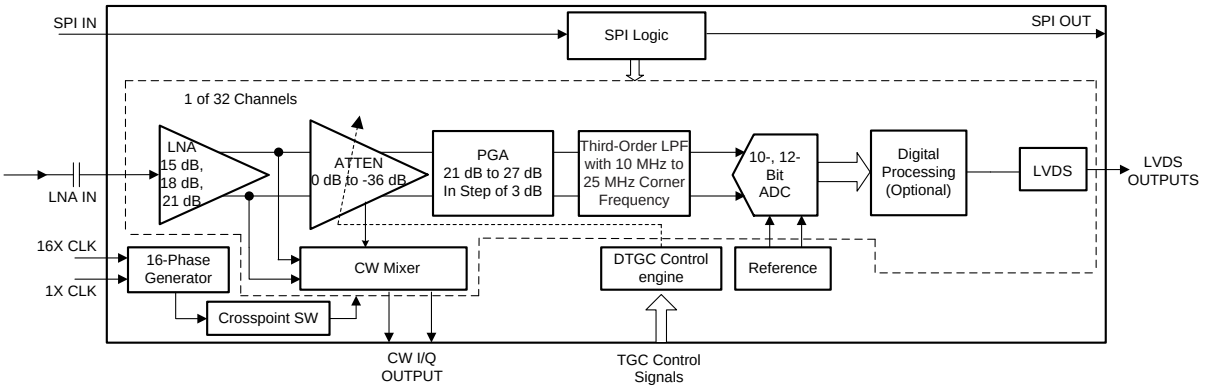
The AFE5832LP is a highly integrated, analog front-end (AFE) solution specifically designed for portable ultrasound systems where high performance, low power, and small size are required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE5832LP	nFBGA (289)	15.00 mm × 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2018	*	Initial release

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5 Description (continued)

The device is realized through a multichip module (MCM) with two dies: 1 VCA die and 1 ADC die. The VCA die has 32 channels that interface with the 16 channels of the ADC die. Each ADC channel alternately converts an odd and an even VCA channel.

Each channel in the VCA die can be configured in either of two modes: time-gain-compensation (TGC) mode or continuous wave (CW) mode. In the TGC mode, each channel includes a low-noise amplifier (LNA), a programmable attenuator (ATTEN), a programmable gain amplifier and a third-order, low-pass filter (LPF). The LNA gain is programmable to 21 dB, 18 dB, or 15 dB. The ATTEN supports an attenuation range of 0 dB to 36 dB, with digital control for the attenuation. The PGA provides gain options from 21 dB to 27 dB in steps of 3 dB. The LPF cutoff frequency can be set between 10 MHz and 25 MHz to support ultrasound applications with different frequencies. In the CW mode, the output of the LNA goes to a low-power passive mixer with 16 selectable phase delays. Different phase delays can be applied to each analog input signal to perform an on-chip beamforming operation. A harmonic filter in the CW mixer suppresses the third and fifth harmonic to enhance the sensitivity of the CW Doppler measurement.

The 16 channels of the ADC die can be configured to operate with a resolution of 12 bits or 10 bits. The ADC resolution can be traded off with conversion rate and can operate at maximum speeds of 80 MSPS and 100 MSPS at 12-bit and 10-bit resolution, respectively. Because each ADC alternately converts two VCA channels, the resulting maximum sample rate of each of the 32 channels of the AFE is 40 MSPS and 50 MSPS in the 12-bit and 10-bit modes, respectively. The ADC is designed to scale its power with sampling rate. The output interface of the ADC comes out through a low-voltage differential signaling (LVDS), which can easily interface with low-cost field-programmable gate arrays (FPGAs).

A very low-power AFE solution makes it suitable for system with strict battery-life requirement.

The AFE is available in a 15 mm × 15 mm 289-pin NFBGA package and is pin-compatible with the AFE5832 family.

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6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation see the following:

- *AFE5818 16-Channel, Ultrasound, Analog Front-End with 140-mW/Channel Power, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer*
- *ADS8413 16-BIT, 2-MSPS, LVDS SERIAL INTERFACE, SAR ANALOG-TO-DIGITAL CONVERTER*
- *ADS8472 16-BIT, 1-MSPS, PSEUDO-BIPOLAR, FULLY DIFFERENTIAL INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE, REFERENCE*
- *CDCE72010 Ten Output High Performance Clock Synchronizer, Jitter Cleaner, and Clock Distributor*
- *CDCM7005 3.3-V High Performance Clock Synchronizer and Jitter Cleaner*
- *ISO724x High-Speed, Quad-Channel Digital Isolators*
- *LMK0480x Low-Noise Clock Jitter Cleaner with Dual Loop PLLs*
- *OPA1632 High-Performance, Fully-Differential Audio Operational Amplifier*
- *OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier*
- *SN74AUP1T04 LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE INVERTER GATE*
- *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*
- *MicroStar BGA Packaging Reference Guide*

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

E2E is a trademark of Texas Instruments.
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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE5832LPZAV	Active	Production	NFBGA (ZAV) | 289	126 | JEDEC TRAY (5+1)	Yes	Call TI | Snagcu	Level-3-260C-168 HR	0 to 85	AFE5832LP
AFE5832LPZAV.A	Active	Production	NFBGA (ZAV) | 289	126 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	0 to 85	AFE5832LP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

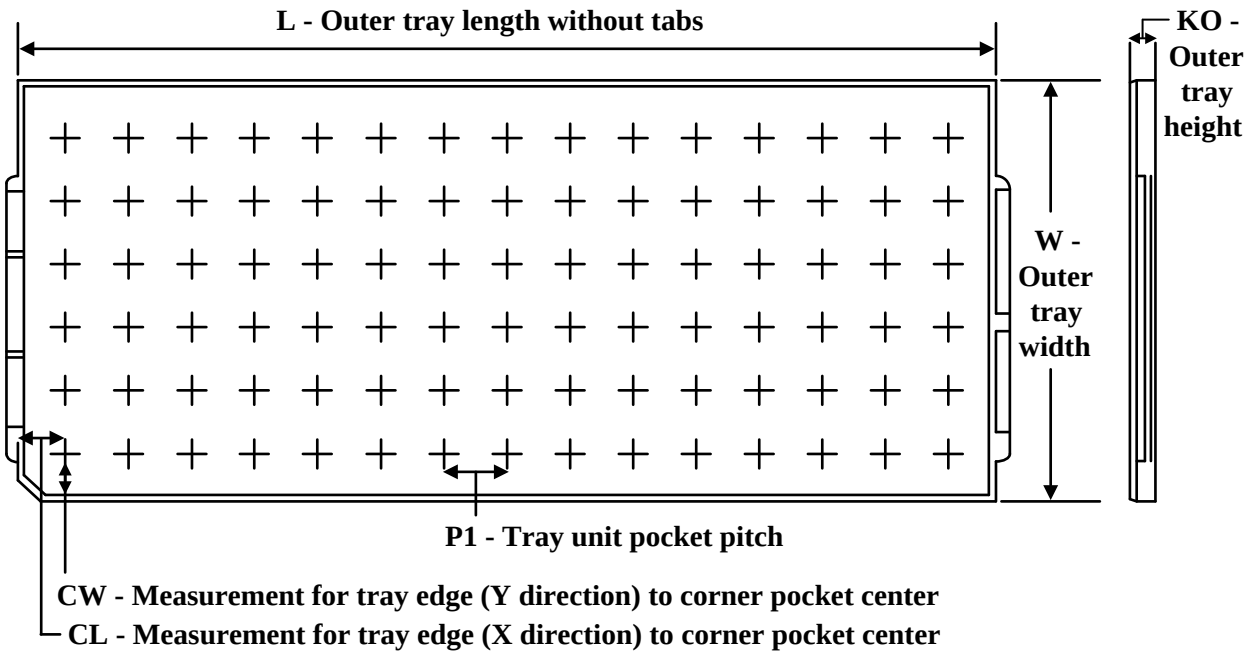
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY

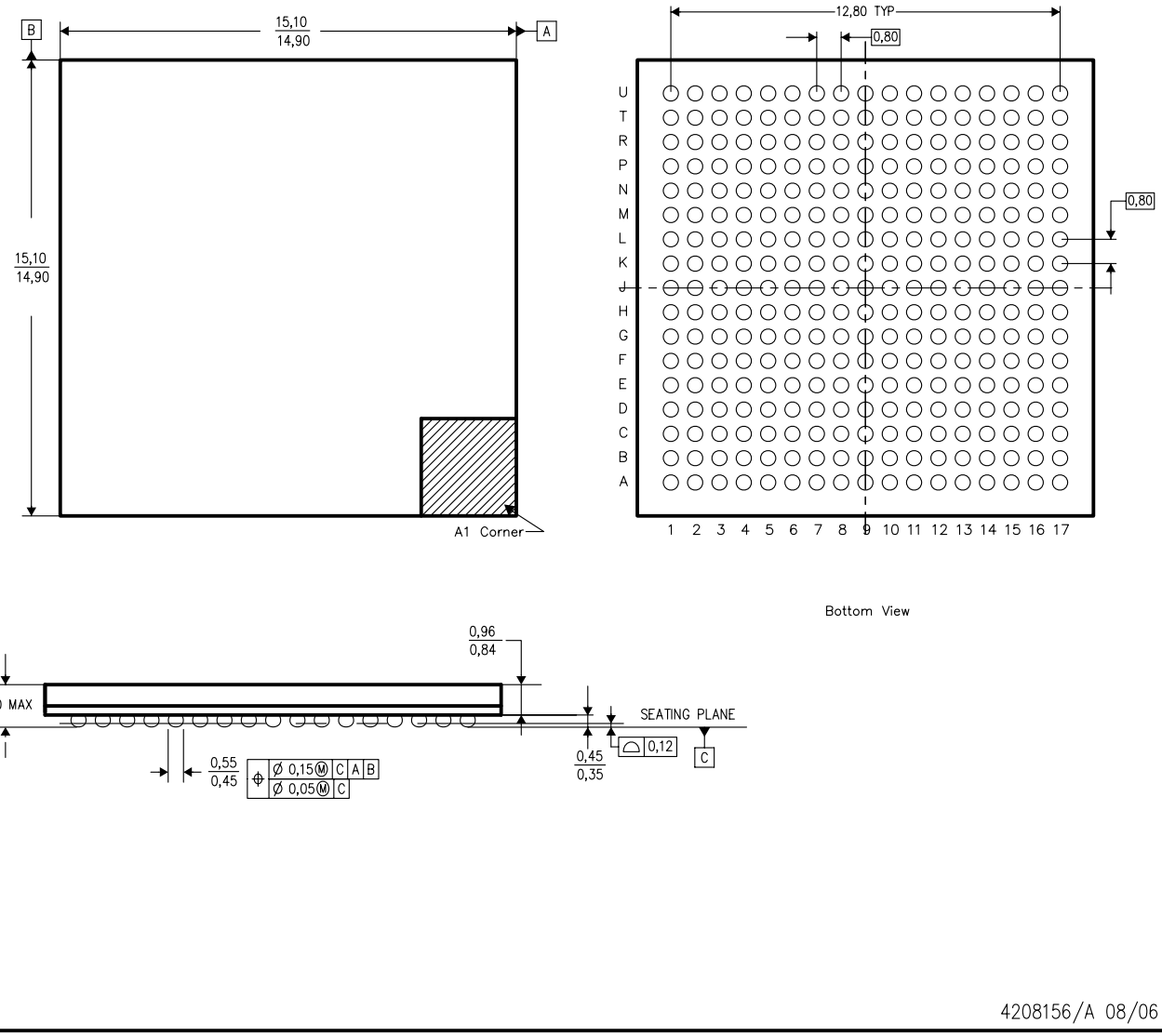


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE5832LPZAV	ZAV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35
AFE5832LPZAV.A	ZAV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

ZAV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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