AFE7903-EP/SEP/SP: 2T2R, 5MHz to 7.4GHz, 400MHz IBW, RF-Sampling AFE with 12GSPS DACs and 3GSPS ADCs

1 Features

- Request full data sheet
- Radiation hardness assured AFE7903-SP:
  – Single-event latch up (SEL): 70 MeV-cm^2/mg
  – RLAT Total ionizing dose (TID): 100 krad(Si)
- Radiation tolerant AFE7903-SEP:
  – Single-event latch up (SEL): 43 MeV-cm^2/mg
  – RLAT Total ionizing dose (TID): 30 krad(Si)
- Dual RF sampling 12GSPS transmit DACs
- Dual RF sampling 3GSPS receive ADCs
- Maximum signal bandwidth per TX or RX: 400MHz
- RF frequency range: 5MHz - 7.4GHz
- Digital step attenuators (DSA):
  – TX: 40dB range, 0.125dB steps
  – RX: 25dB range, 0.5dB steps
- Single or dual-band DUC/DDCs for TX and RX
  – 16x NCOs per TX/RX
- Optional Internal PLL or VCO for DAC or ADC clocks
- External clock at DAC or ADC sample rate
- SYSREF Alignment Detector
- SerDes data interface:
  – JESD204B and JESD204C compatible
  – 8 SerDes transceivers up to 29.5Gbps
  – Subclass 1 multi-device synchronization
- Supports aerospace and defense applications
  – Controlled baseline
  – One fabrication, assembly, and test site
  – Product traceability
  – Extended product life cycle
  – Radiation lot acceptance Test (RLAT) (AFE7903-SEP/SP only)
  – Meets ASTM E595 out-gassing specification
  – Production burn-in (AFE7903-SP only)
- This device contains non-encapsulated chip-caps with tin (Sn) finish of >97% purity. See reliability report for more information

2 Applications

- Satellite communications payload downlink
- Satellite telemetry payload downlink
- RADAR
- Seeker Front End
- Defense Radio
- Tactical Communications Infrastructure

3 Description

The AFE7903-x is a high performance, wide bandwidth multi-channel transceiver, integrating two RF sampling TX chains and two RF sampling RX chains. With operation up to 7.4GHz, this device enables direct RF sampling in the HF, VHF, UHF, L, S and C-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

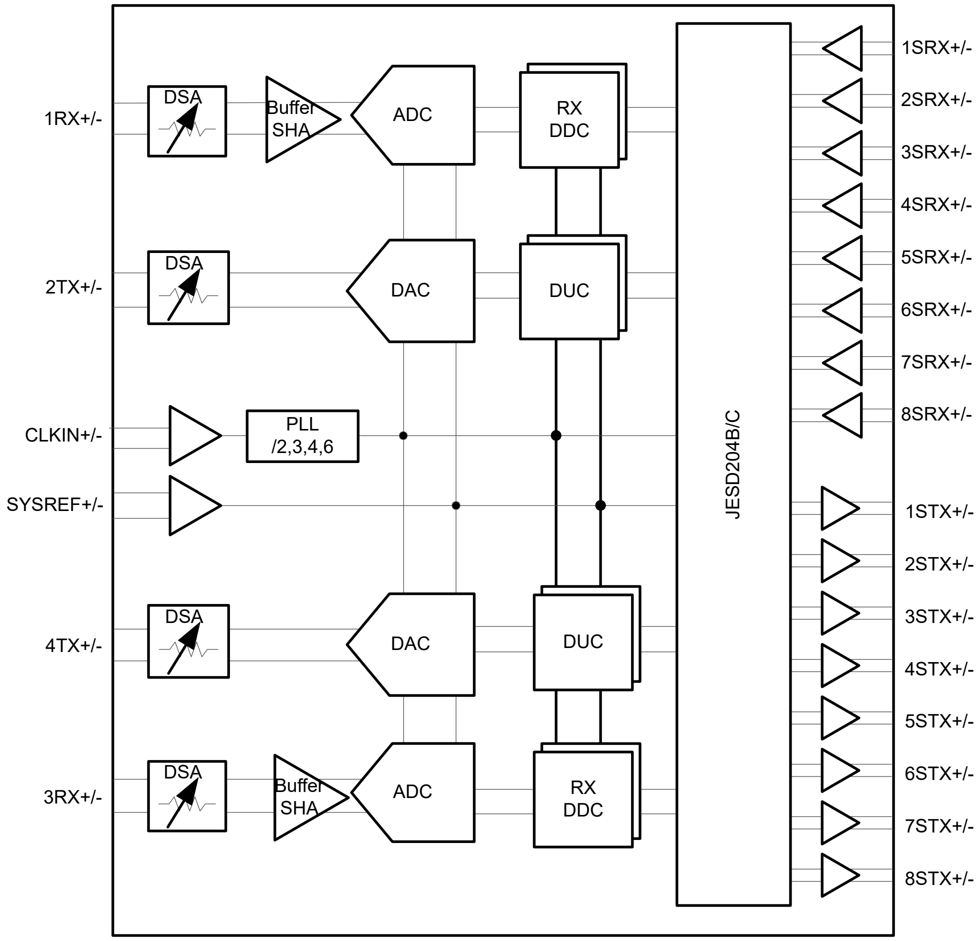
The TX signal paths support interpolation and digital up conversion options that deliver up to 400MHz of signal bandwidth. The output of the DUCs drives a 12GSPS DAC with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40dB range and 1dB analog and 0.125dB digital steps.

Each RX chain includes a 25dB range DSA (Digital Step Attenuator), followed by a 3GSPS ADC. Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 400MHz for two RX.

Package Information

PART NUMBER	GRADE	PACKAGE(1) (2)
AFE7903-SP(3)	Space Grade, Radiation-hardness-assured (RHA)	17mm × 17mm, plastic substrate, FC-BGA, 400 SnPb balls, 0.8mm pitch
AFE7903-SEP	Space Enhanced Product, Radiation-tolerant	
AFE7903-EP(3)	Enhanced Product	

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product Preview



Functional Block Diagram

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	–0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–45		85	°C
T_J	Operating Junction Temperature			105	°C

4.4 Thermal Information

THERMAL METRIC		FC-BGA	UNIT
		400 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	15.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.5	°C/W

4.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC_{RES}	DAC resolution			14		bits
f_{RFout}	RF output frequency range	f_{DAC} = 12 GSPS, 1st Nyquist	5		6000	MHz
		f_{DAC} = 9 GSPS, 1st Nyquist	5		4500	
		f_{DAC} = 9 GSPS, 2nd Nyquist	4500		7400	
		f_{DAC} = 6 GSPS, 1st Nyquist	5		3000	
		f_{DAC} = 6 GSPS, 2nd Nyquist	3000		6000	
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 10 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 30 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 400 MHz, f_{DAC} = 6GSPS, -0.1dBFS		5.6		dBm
		f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f_{out} = 3500 MHz, -0.5dBFS		2.9		dBm
		fout = 4900 MHz, -0.5dBFS		-0.6		dBm
		f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R_{TERM}	Output termination resistor	Default setting		100		Ω
ATT_{range}	DSA Attenuation range			40		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (1)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration		±0.2		
ATT_{step}	DSA Gain Steps Phase accuracy, any 8dB range(1)	f_{out} = 30MHz		±1		deg
		f_{out} = 400MHz		±1		deg
		f_{out} = 850MHz		±1		deg
		f_{out} = 1800MHz		±1		deg
		f_{out} =2600MHz		±1		deg
		f_{out} = 3500MHz		±1		
		f_{out} = 4900MHz		±1		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	f_{DAC} =6 GSPS, f_{out} = 5MHz ±1MHz, -7dBFS each tone		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -7dBFS each tone		-47		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -7dBFS each tone		-51		dBc
		f_{out} = 850MHz ±10MHz, -7dBFS each tone		-61		dBc
		f_{out} = 1800MHz ±10MHz, -7dBFS each tone		-62		dBc
		f_{out} = 2600MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 3500MHz ±10MHz, -7dBFS each tone		-63		dBc
		f_{out} = 4900MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 5MHz ±1MHz, -13dBFS each tone		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -13dBFS each tone		-71		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -13dBFS each tone		-72		dBc
		f_{out} = 850MHz ±10MHz, -13dBFS each tone		-73		dBc
		f_{out} = 1800MHz ±10MHz, -13dBFS each tone		-75		dBc
		f_{out} = 2600MHz ±10MHz, -13dBFS each tone		-79		dBc
		f_{out} = 3500MHz ±10MHz, -13dBFS each tone		-77		dBc
		f_{out} = 4900MHz ±10MHz, -13dBFS each tone		-77		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 30 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		45		dBc
		f_{out} = 400 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		48		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		62		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		56		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		39		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		42		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		60		dBc

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_S/2$ - f_{OUT}	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-47		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-43		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-43		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-75		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-73		dBc
		f_{out} = 400 MHz		-46		dBc
		f_{out} = 850 MHz		-65		dBc
		f_{out} = 1800 MHz		-68		dBc
		f_{out} = 2600 MHz		-47		dBc
		f_{out} = 3500 MHz		-59		dBc
		f_{out}= 4900 MHz		-48		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-74		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-67		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-58		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-69		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-59		dBc
HD3	3rd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-46		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-49		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-49		dBc
		f_{out} = 850 MHz		-56		dBc
		f_{out} = 1800 MHz		-58		dBc
		f_{out} = 2600 MHz		-60		dBc
		f_{out} = 3500 MHz		-63		dBc
		f_{out}= 4900 MHz		-66		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-82		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-88		dBc

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-58		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-60		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-61		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-50		dBc
		f_{out} = 850 MHz		-85		dBc
		f_{out} = 1800 MHz		-90		dBc
		f_{out} = 2600 MHz		-84		dBc
		f_{out} = 3500 MHz		-86		dBc
		f_{out}= 4900 MHz		-87		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-94		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-93		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-85		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-89		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-88		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-89		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{DAC} =6 GSPS, f_{out} = 400 MHz		87		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		84		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		78		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		80		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		81		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		74		dBc
$f_S/4$	Fixed Spur	f_{DAC} = 5898.24MSPS, $f_{OUT}=f_{DAC}/4$-50MHz		-95		dBFS
		f_{DAC} = 8847.36MSPS, $f_{OUT}=f_{DAC}/4$-50MHz		-88		dBFS
		f_{DAC} = 11796.48MSPS, $f_{OUT}=f_{DAC}/4$-50MHz		-76		dBFS
$f_S/2$	Fixed Spur	f_{DAC} = 5898.24MSPS, $f_{OUT}=f_{DAC}/2$-50MHz		-52		dBFS
		f_{DAC} = 8847.36MSPS, $f_{OUT}=f_{DAC}/2$-50MHz		-45		dBFS
		f_{DAC} = 11796.48 MSPS, $f_{OUT}=f_{DAC}/2$-50MHz		-49		dBFS

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_S/4$	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-82		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-75		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-49		dBFS
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-70		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-62		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-61		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-50		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-72		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-60		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-69		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-64		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-59		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-53		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-38		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.16		%
		F_{out} =1.8425 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.21		%
		F_{out} =2.6 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.24		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.27		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.38		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 5 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-148		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-143		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-129		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 30 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-154		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-142		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-132		dBFS/Hz

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 100 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-158		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-136		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 400 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-160		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-153		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.8		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.7		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-148.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-137.9		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-157.9		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-151.3		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.8		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-158.3		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151.6		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144.9		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-134.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-158.2		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-150.9		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-144.4		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-133.4		dBFS/Hz

4.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-154.6		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-147.0		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-140.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-129.9		dBFS/Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-12		dB
Isolation	Far Channel: 2TXOUT to 4TXOUT	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(2)		-104		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(2)		-100		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(2)		-105		dB
		f_{out} = 400 MH, f_{DAC} = 6000MSPS, straight mode(3)		-97		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-91		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83.2		dB
PN_{TXADD}	Additive Phase Noise External Clock Mode (4)	f_{out} = 3.7GHz, f_{OFFSET} = 100Hz		-97		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1kHz		-106		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10kHz		-117		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 100kHz		-128		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1MHz		-138		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10MHz		-144		dBc/Hz

(1) After DSA calibration procedure
(2) measured with 1µH DC feed inductor
(3) measured with 0.39µH DC feed inductor
(4) Input clock phase noise subtracted.

4.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		5		7400	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 5 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-0.4		dBm
		f_{IN} = 30 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-2.2		dBm
		f_{IN} = 410 MHz, DSA=0dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 12		-2.5		dBm
		f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
$P_{FS\_CW,MAX}$	MAX Full scale input power - reliability limited, at device pins	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		19.7		dBm
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		17.8		dBm
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		17.6		dBm
		f_{IN} = 830 MHz		16.7		dBm
		f_{IN} = 1760 MHz		17.0		dBm
		f_{IN} = 2610 MHz		18		dBm
		f_{IN} = 3610 MHz		18.5		dBm
		f_{IN} = 4910 MHz		19.3		dBm
R_{TERM}	Input reference impedance			100.0		Ω
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		1.8		deg
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

4.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density [3] (small signal = -30dBFS)	f_{IN} = 5 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-147.1		dBFS/Hz
		f_{IN} = 30 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-150.7		dBFS/Hz
		f_{IN} = 410 MHz, DSA = 3dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-155.4		dBFS/Hz
		f_{IN} = 830 MHz, DSA = 3dB		-156.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 3dB		-156.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 3dB		-155.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48, 3<=Atten<=22		-147.8		dBFS/Hz
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24, 3<=Atten<=22		-151.5		dBFS/Hz
		f_{IN} = 410 MHz, 3<=Atten<=22, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-156.6		dBFS/Hz
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		29.4		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		24.5		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		19.3		dB
		f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB

4.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure[4] DSA Atten=4dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		30.6		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		25.1		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		20.1		dB
		f_{IN} = 830 MHz		20.0		dB
		f_{IN} = 1760 MHz		20.6		dB
		f_{IN} = 2610 MHz		21.9		dB
		f_{IN} = 3610 MHz		23.5		dB
		f_{IN} = 4910 MHz		22.3		dB
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		45.9		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		40.2		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		35.0		dB
		f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
IMD3	3^{rd} order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 30±1 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-82		dBc
		f_{IN} = 400MHz and 405MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-75		dBc
		f_{IN} = 840 MHz		-82		dBc
		f_{IN} = 1770 MHz		-84		dBc
		f_{IN} = 2610 MHz		-74		dBc
		f_{IN} = 3610 MHz		-77		dBc
		f_{IN} = 4920 MHz		-76		dBc

4.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		100		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		94		dBFS
		f_{IN} = 830 MHz		88		dBFS
		f_{IN} = 1760 MHz		81		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		79		dBFS
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(2)	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-84		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-90		dBFS
		f_{IN} = 830 MHz		-86		dBFS
		f_{IN} = 1760 MHz		-90		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-87		dBFS
		f_{IN} = 4910 MHz		-84		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-96		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-94		dBFS
		f_{IN} = 830 MHz		-80		dBFS
		f_{IN} = 1760 MHz		-85		dBFS
		f_{IN} = 2610 MHz		-86		dBFS
		f_{IN} = 3610 MHz		-78		dBFS
		f_{IN} = 4910 MHz		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-94		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-94		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-94		dBFS
		f_{IN} = 830 MHz		-88		dBFS
		f_{IN} = 1760 MHz		-81		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-82		dBFS

4.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		101		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		95		dBFS
		f_{IN} = 830 MHz		89		dBFS
		f_{IN} = 1760 MHz		89		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		87		dBFS
		f_{IN} = 4910 MHz		90		dBFS
HD2	2nd Harmonic Distortion(2) A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-104		dBFS
		f_{IN} = 830 MHz, with board trim		-79		dBFS
		f_{IN} = 1760 MHz, with board trim		-102		dBFS
		f_{IN} = 2610 MHz, with board trim		-100		dBFS
		f_{IN} = 3610 MHz, with board trim		-101		dBFS
		f_{IN} = 4910 MHz, with board trim		-99		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-103		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-84		dBFS
		f_{IN} = 381 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 830 MHz		-95		dBFS
		f_{IN} = 1760 MHz		-95		dBFS
		f_{IN} = 2610 MHz		-98		dBFS
		f_{IN} = 3610 MHz		-97		dBFS
		f_{IN} = 4910 MHz		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-95		dBFS
		f_{IN} = 830 MHz		-89		dBFS
		f_{IN} = 1760 MHz		-89		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90		dBFS

4.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX-RX Isolation	2TXOUT to 1RXIN 4TXOUT to 3RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-105		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-101		dB
		f_{IN} = 400 MHz		-99		dB
		f_{IN} = 830 MHz		-86		dB
		f_{IN} = 1760 MHz		-87		dB
		f_{IN} = 2610 MHz		-84		dB
		f_{IN} = 3610 MHz		-82		dB
		f_{IN} = 4910 MHz		-82		dB

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
(2) After HD2 trim on specific printed circuit board.
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB

4.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f_{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
DIV_{RXADC}				1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error(1)	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff

4.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

4.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode			400		mV
Z_{SRdiff}	SerDes Internal Differential Termination(1)			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	
		Quarter rate mode	4.75		8.125	
		1/8th	2.375		4.062	
		1/16th	1.1875		2.031	
	Insertion Loss Tolerance(2)	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Input Voltage		VDD1P8GPIO–0.2			V
V_{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff(3)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff(3)
Z_T	Input termination	differential		100		Ω

4.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff[3]
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

4.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1a: 2T2R - TDD, 50%/50% duty cycle TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		260		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			297		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			70		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			89		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			288		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			536		mA
P_{diss}	Power Dissipation			2166		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1b: 2T2R - TX active, RX in standby, TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		205		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			282		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			71		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			21		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			365		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			499		mA
P_{diss}	Power Dissipation			2014		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1c: 2T2R - RX active, TX in standby TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		315		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			313		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			70		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			211		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			573		mA
P_{diss}	Power Dissipation			2318		mW

4.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 2T2R - FDD TX: 125MSPS input, 24x Int, f_{DAC} = 3GSPS RX: f_{ADC} = 1.5GSPS, 12x Dec, 125MSPS output f_{OUT} = 400 MHz, f_{IN} = 500 MHz Serdes: 8b/10b, 10Gbps TX/RX LMFS: 1-4-8-1		458		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			335		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			71		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			158		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			386		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			77		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			728		mA
P_{diss}	Power Dissipation			2974		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3a: 2T2R - TDD, 50%/50% duty cycle TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		307		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			321		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			397		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1108		mA
P_{diss}	Power Dissipation			3047		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3b: 2T2R - TX active, RX in standby TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		266		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			293		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			26		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			545		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1061		mA
P_{diss}	Power Dissipation			2899		mW

4.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3c: 2T2R - RX active, TX in standby TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		349		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			350		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			287		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			248		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1155		mA
P_{diss}	Power Dissipation			3195		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 2T2R - FDD TX: 500MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500MSPS output f_{OUT}= 3.5GHz, f_{IN}= 3.7 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		550		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			371		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			288		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			567		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1568		mA
P_{diss}	Power Dissipation			4354		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5a: 2T2R - TDD, 50%/50% duty cycle TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		307		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			312		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			370		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1051		mA
P_{diss}	Power Dissipation			2948		mW

4.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5b: 2T2R - TX active, RX in Standby TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		265		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			284		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			26		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			507		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			969		mA
P_{diss}	Power Dissipation			2749		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5c: 2T2R - RX active, TX in standby TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		348		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			341		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			287		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			234		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1133		mA
P_{diss}	Power Dissipation			3146		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6: 2T2R FDD TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-8-16-1		550		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			362		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			289		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			530		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1518		mA
P_{diss}	Power Dissipation			4253		mW

4.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.		16		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			174		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			33		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			37		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			155		mA
P_{diss}	Power Dissipation			596		mW

4.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(\overline{SDEN})}$	Setup Time, $\overline{SDEN}$ to Rising Edge of SCLK		15		ns
$t_{h(\overline{SDEN})}$	Hold Time, $\overline{SDEN}$ after last Rising Edge of SCLK [(1)]		5 + t_{SCLK}		ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(SCLK)\_W}$	Minimum SCLK period: registers write		25		ns
$t_{(SCLK)\_R}$	Minimum SCLK period: registers read		50		ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) $\overline{SDEN}$ need to be held one more extra clock cycle with the last SCLK edge

4.11 Switching Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

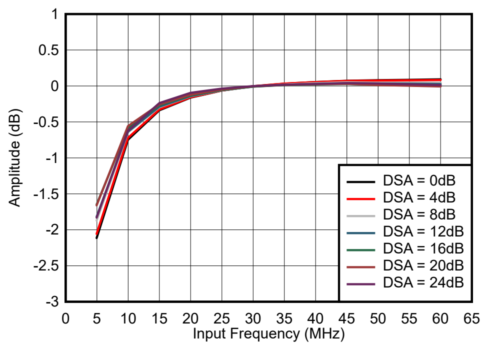
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t_{JESDTX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles(1)
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
t_{JESDRX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles(1)
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
	SerDes Transmitter Analog Delay			3.6		ns

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

4.12 Typical Characteristics

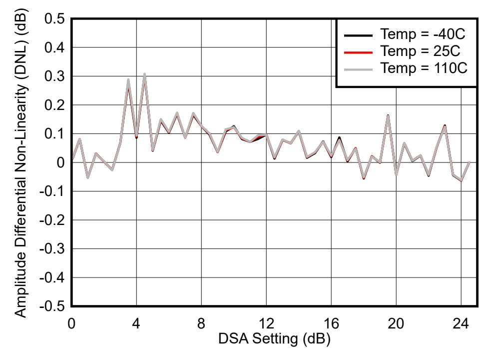
4.12.1 RX Typical Characteristics 30MHz and 400MHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



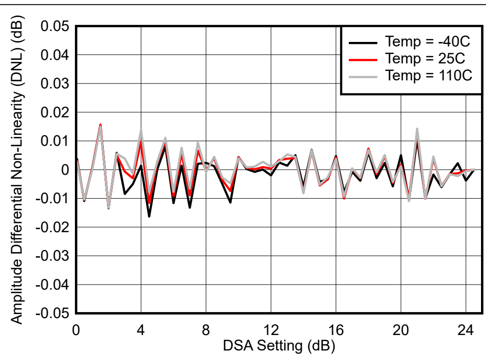
Normalized to 30MHz

Figure 4-1. RX In-Band Gain Flatness, f_{IN} = 30MHz



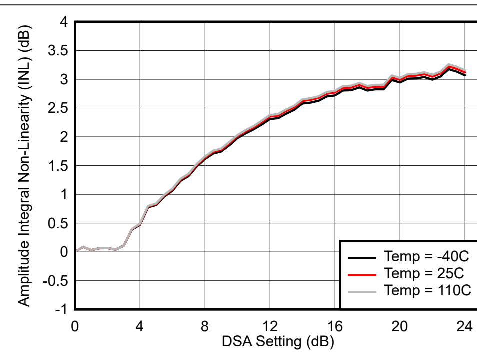
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 4-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 4-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30MHz

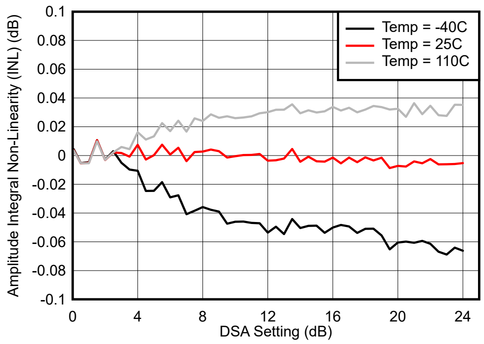


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30MHz

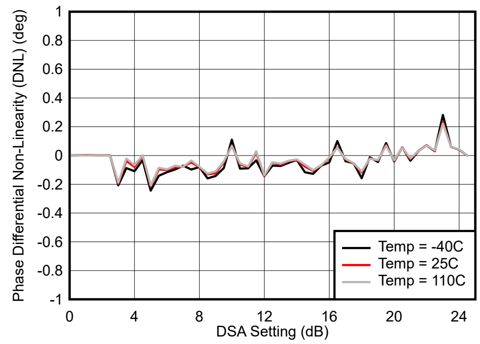
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



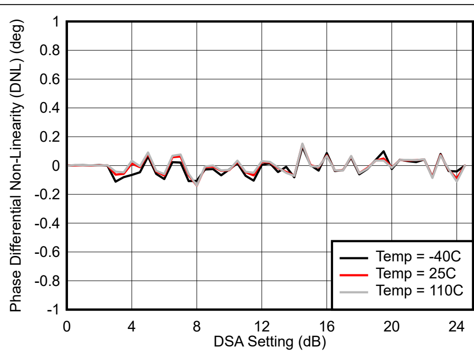
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30MHz



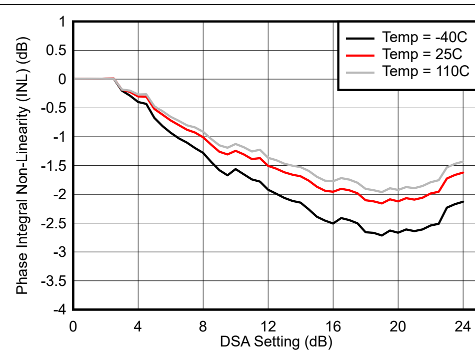
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 4-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 4-7. RX Calibrated Differential Phase Error vs DSA Setting at 30MHz

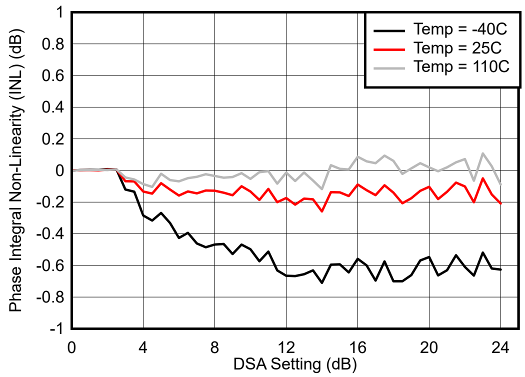


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30MHz

4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

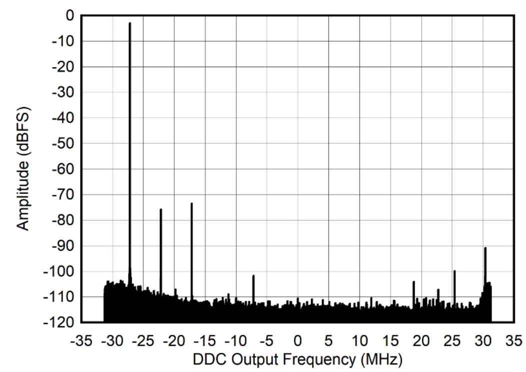
Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



With 0.8GHz matching

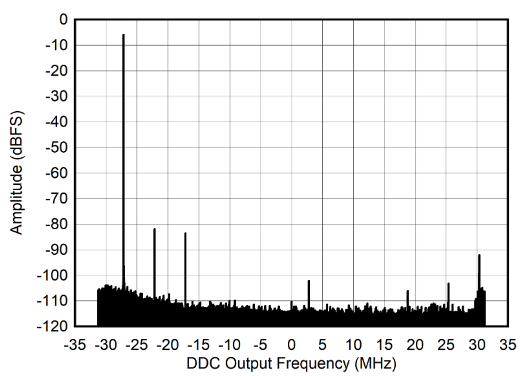
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30MHz



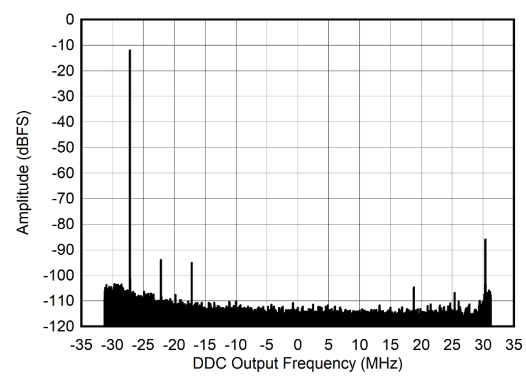
A_{IN} = -3dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-10. RX Output FFT at 5MHz



A_{IN} = -6dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz , Decimate by 24x

Figure 4-11. RX Output FFT at 5MHz

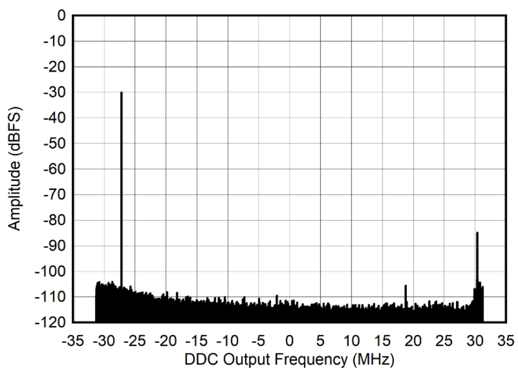


A_{IN} = -12dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-12. RX Output FFT at 5MHz

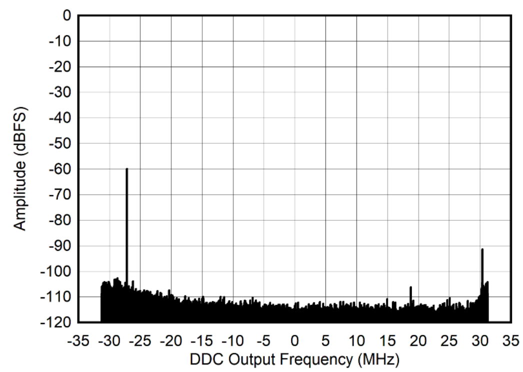
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



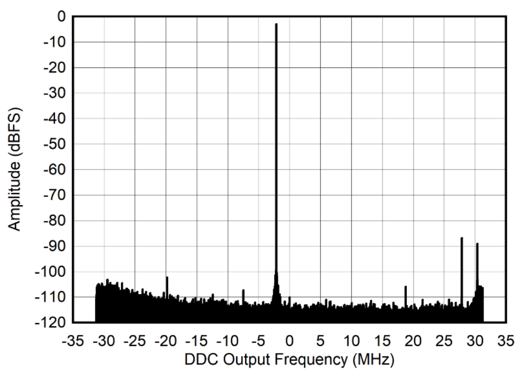
A_{IN} = -30dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-13. RX Output FFT at 5MHz



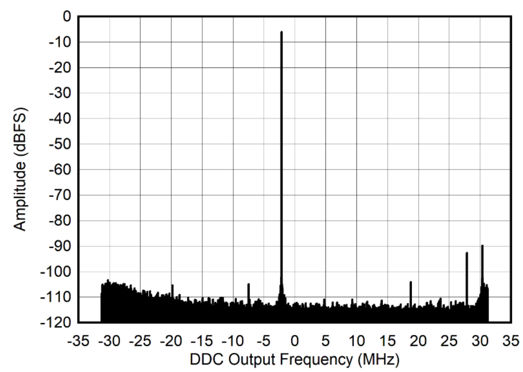
A_{IN} = -60dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-14. RX Output FFT at 5MHz



A_{IN} = -3dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-15. RX Output FFT at 30MHz

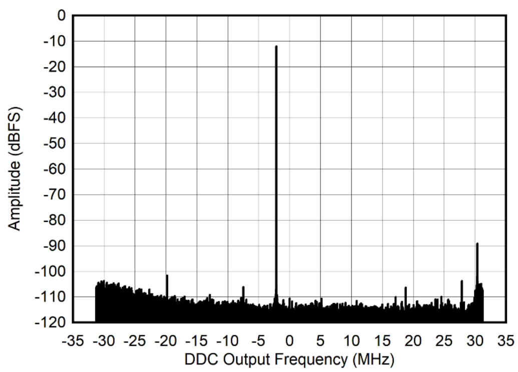


A_{IN} = -6dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-16. RX Output FFT at 30MHz

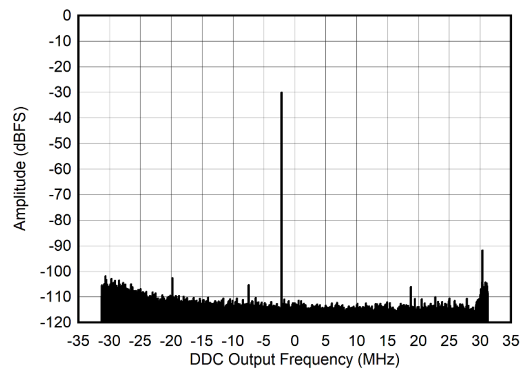
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



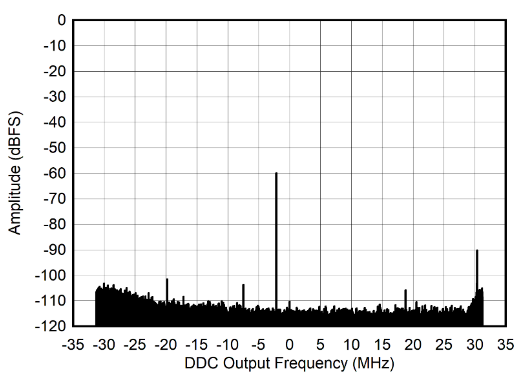
A_{IN} = -12dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-17. RX Output FFT at 30MHz



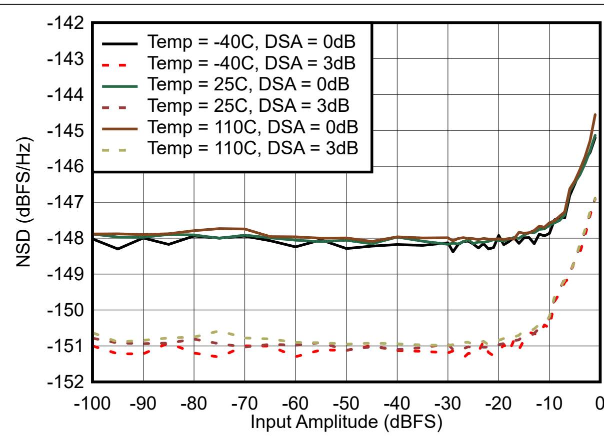
A_{IN} = -30dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-18. RX Output FFT at 30MHz



A_{IN} = -60 dBFS, f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-19. RX Output FFT at 30MHz

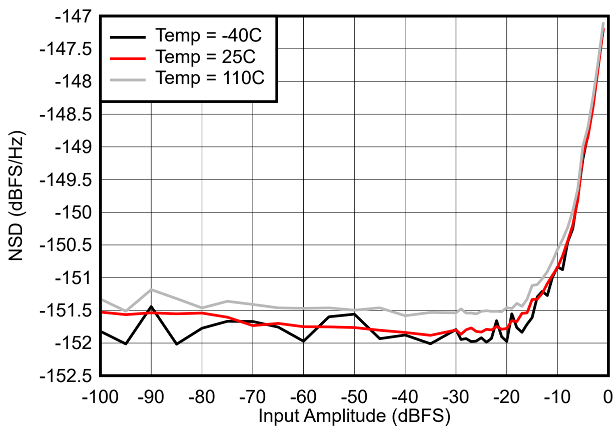


f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-20. NSD vs Input Amplitude at 30MHz with DSA = 0 and 3dB

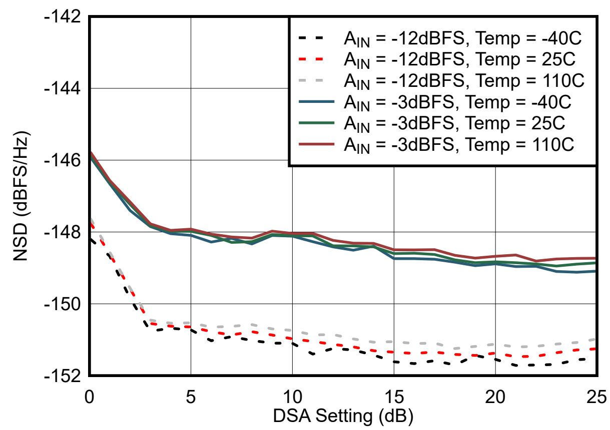
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



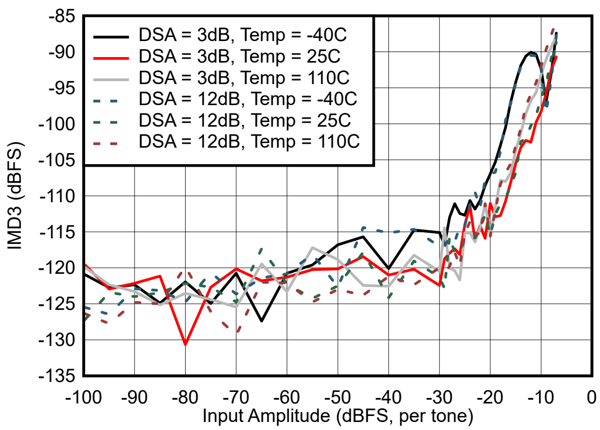
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-21. NSD vs Input Amplitude at 30MHz with DSA = 12



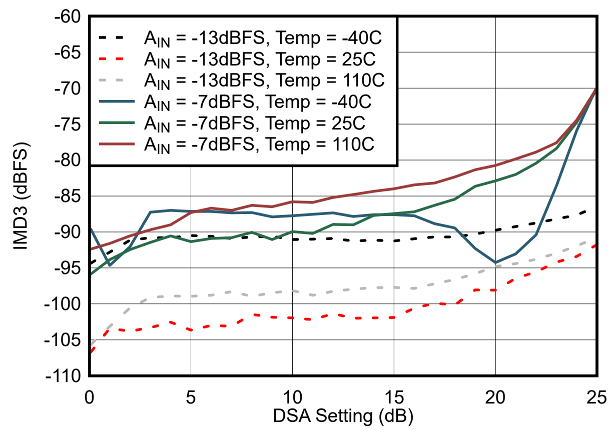
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-22. NSD vs DSA Attenuation at 30MHz



f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-23. IMD3 vs Input Amplitude at 30MHz

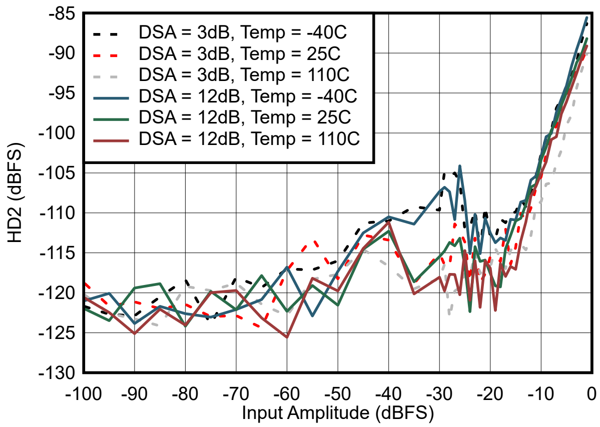


f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-24. IMD3 vs DSA Setting at 30MHz

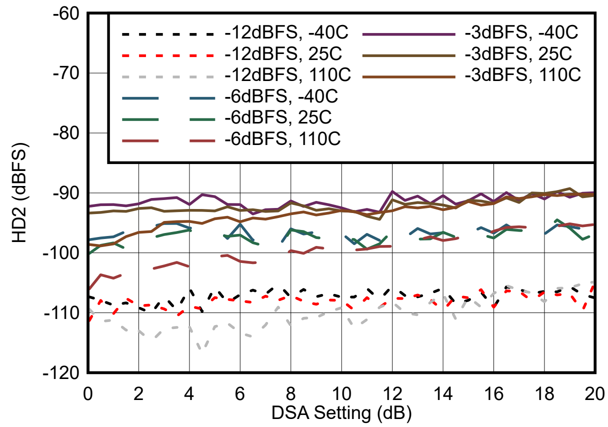
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



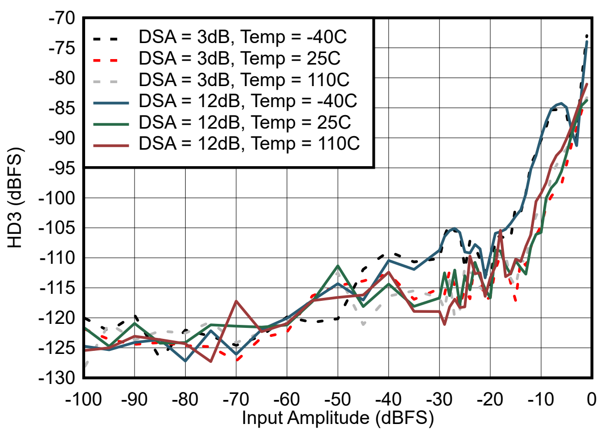
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-25. HD2 vs Input Amplitude at 30MHz



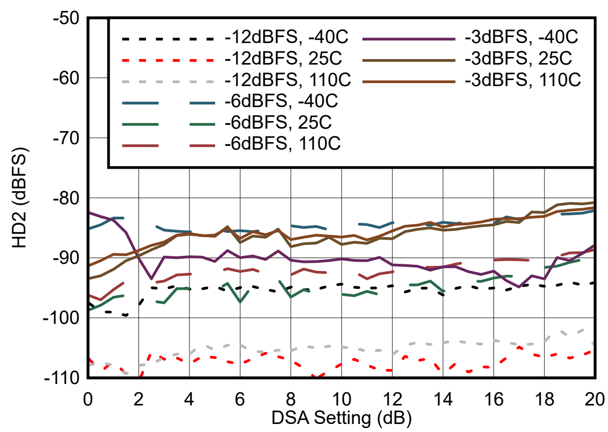
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz , Decimate by 24x

Figure 4-26. HD2 vs DSA Setting at 30MHz



f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-27. HD3 vs Input Amplitude at 30MHz

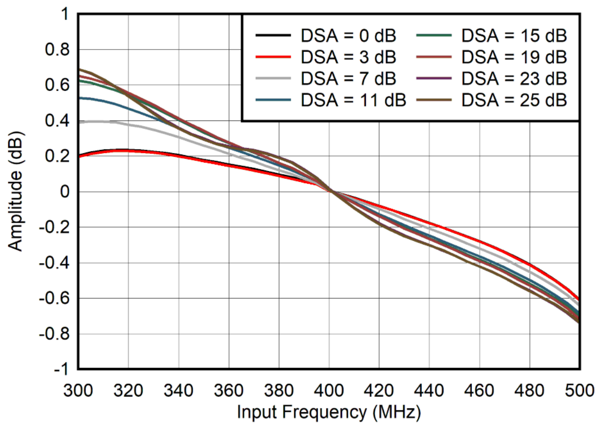


f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

Figure 4-28. HD3 vs DSA Setting at 30MHz

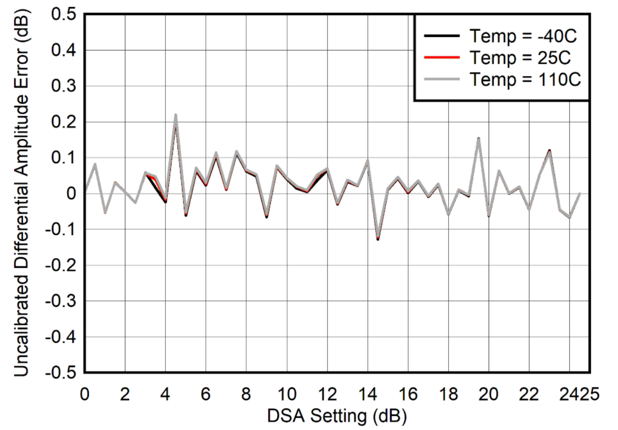
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



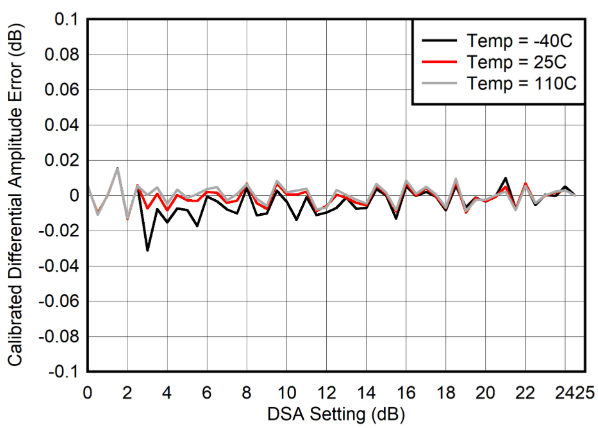
Normalized to 400MHz

Figure 4-29. RX In-Band Gain Flatness, f_{IN} = 400MHz



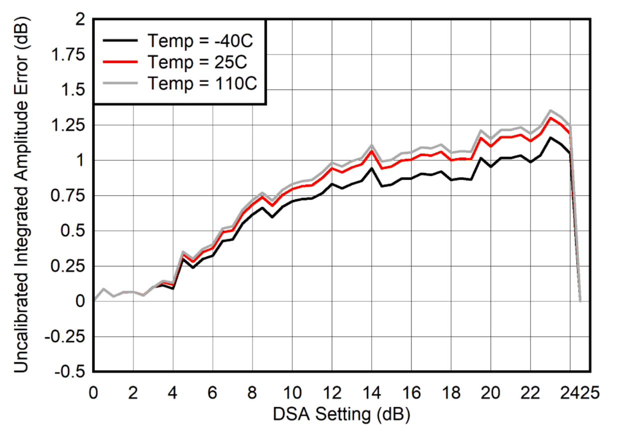
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 4-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 4-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400MHz

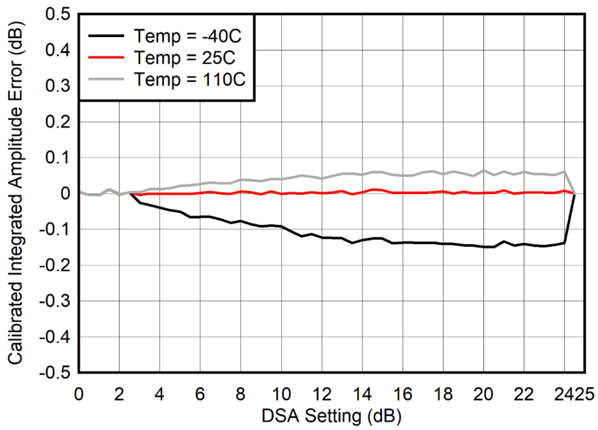


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400MHz

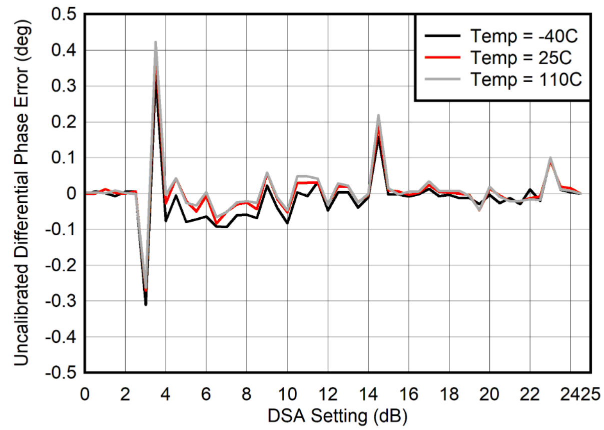
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



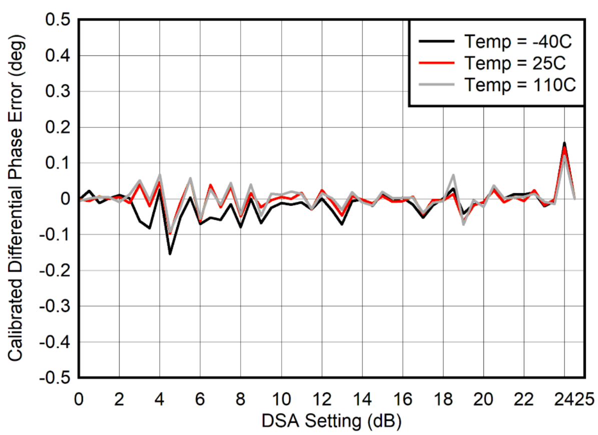
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400MHz



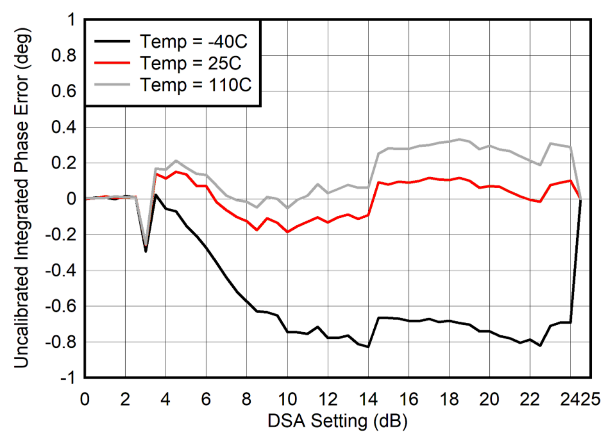
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 4-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 4-35. RX Calibrated Differential Phase Error vs DSA Setting at 400MHz

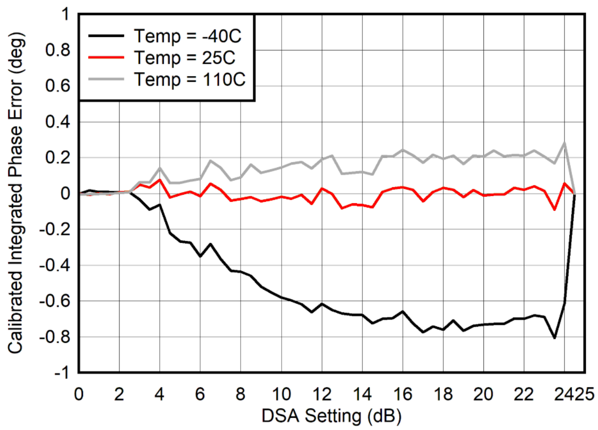


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400MHz

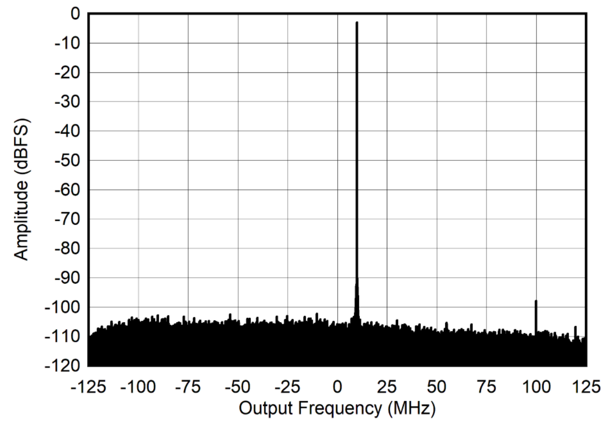
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



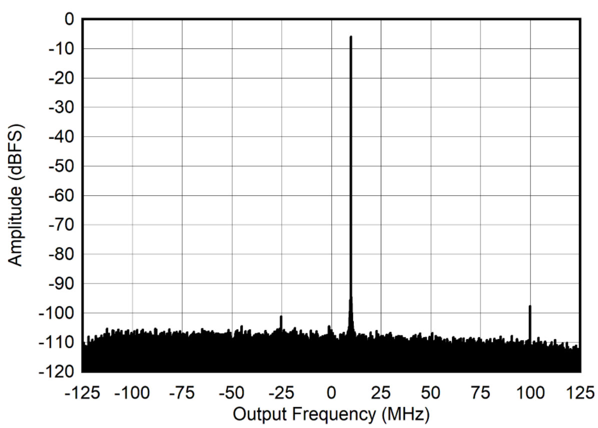
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400MHz



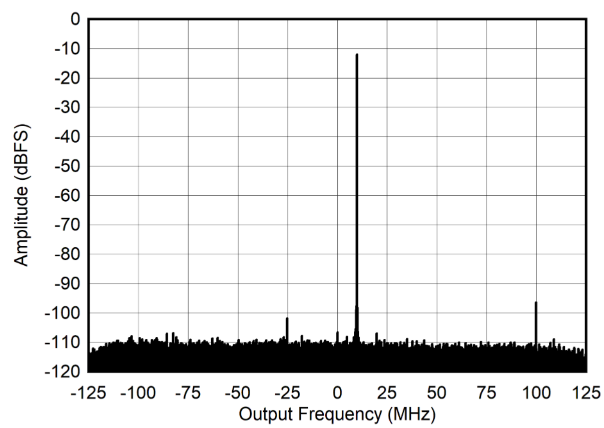
f_{NCO} = 400MHz

Figure 4-38. RX Output FFT at 405MHz and -3dBFS



f_{NCO} = 400MHz

Figure 4-39. RX Output FFT at 405MHz and -6dBFS

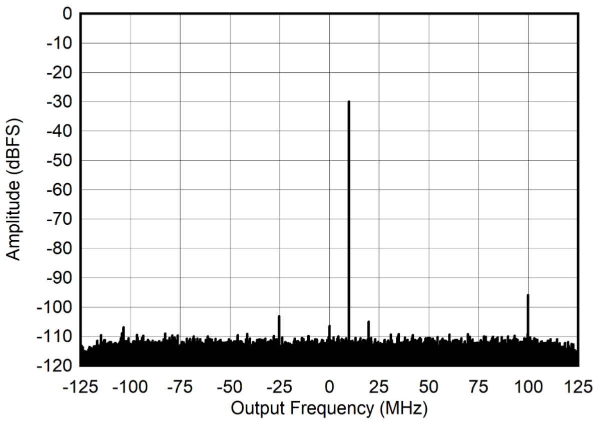


f_{NCO} = 400MHz

Figure 4-40. RX Output FFT at 405MHz and -12dBFS

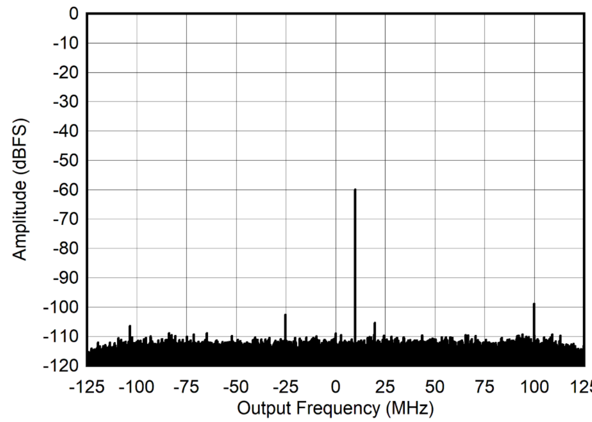
4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.



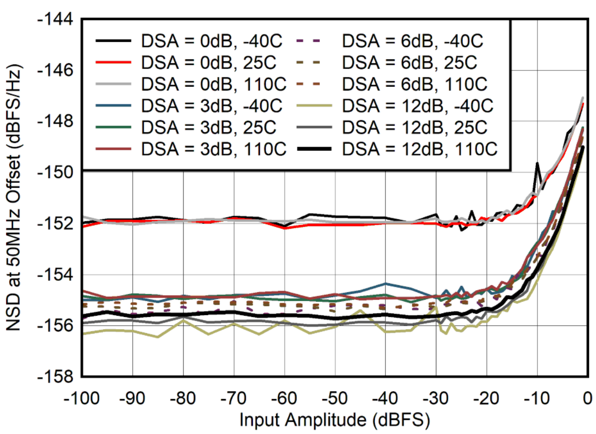
f_{NCO} = 400MHz

Figure 4-41. RX Output FFT at 405MHz and -30dBFS



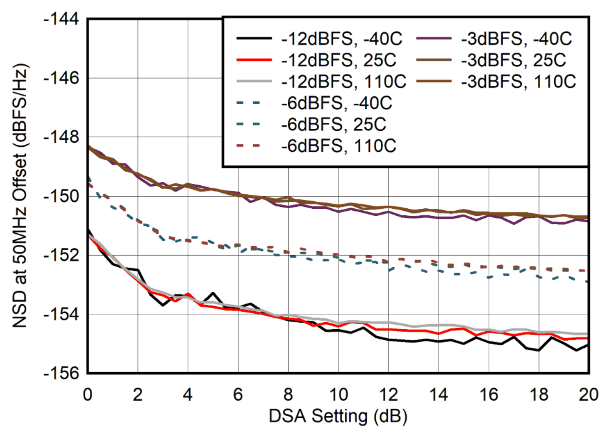
f_{NCO} = 400MHz

Figure 4-42. RX Output FFT at 405MHz and -60dBFS



f_{OFFSET} = 50MHz

Figure 4-43. NSD vs Input Amplitude at 400MHz



f_{OFFSET} = 50MHz

Figure 4-44. NSD vs DSA Setting at 400MHz

4.12.1 RX Typical Characteristics 30MHz and 400MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 62.5MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB. Default conditions at 400MHz: ADC Sampling Rate = 1500MSPS, output sample rate = 125MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500MHz, A_{IN} = –3dBFS, DSA setting = 3dB.

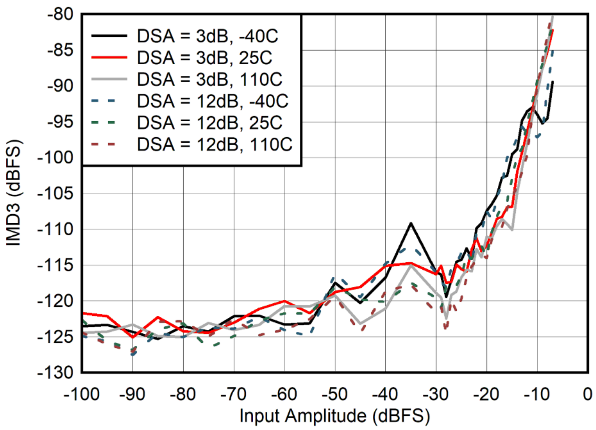


Figure 4-45. IMD3 vs Input Amplitude at 400MHz

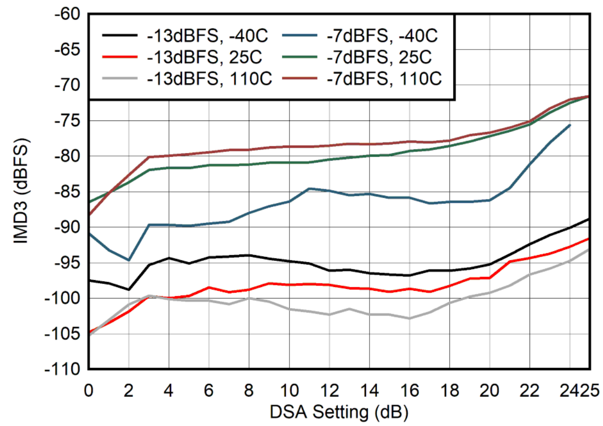


Figure 4-46. IMD3 vs DSA Setting at 400MHz

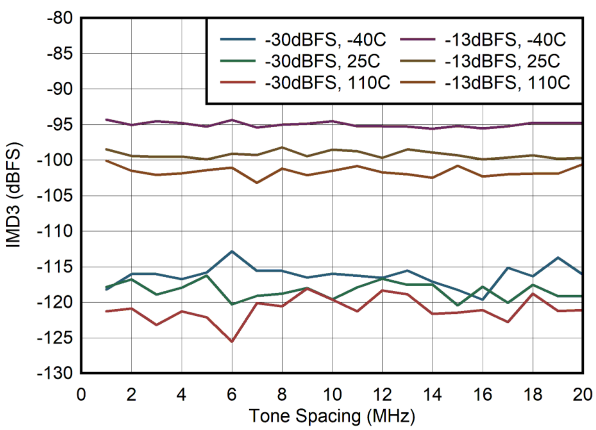


Figure 4-47. IMD3 vs Tone Spacing at 400MHz

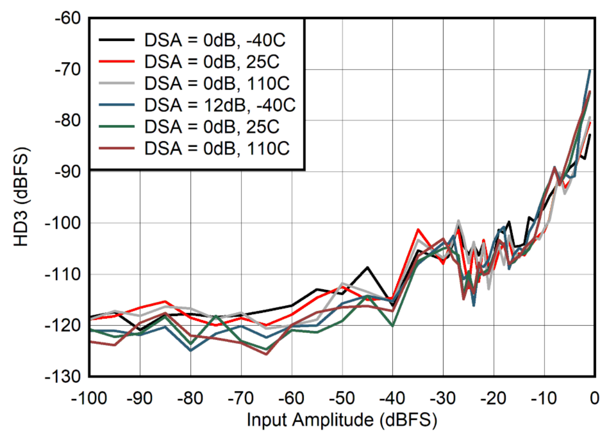


Figure 4-48. HD3 vs Input Amplitude at 400MHz

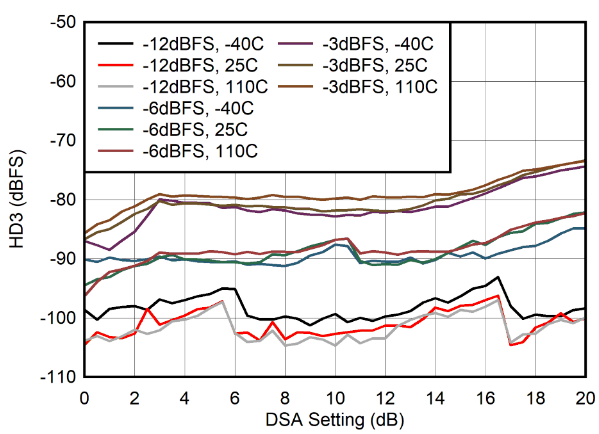
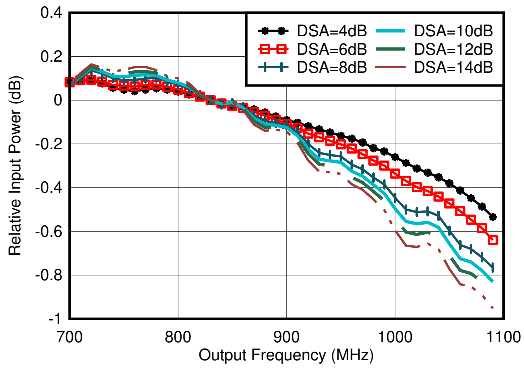


Figure 4-49. HD3 vs DSA Setting at 400MHz

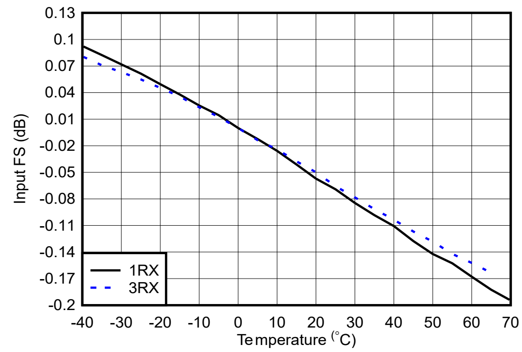
4.12.2 RX Typical Characteristics at 800MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



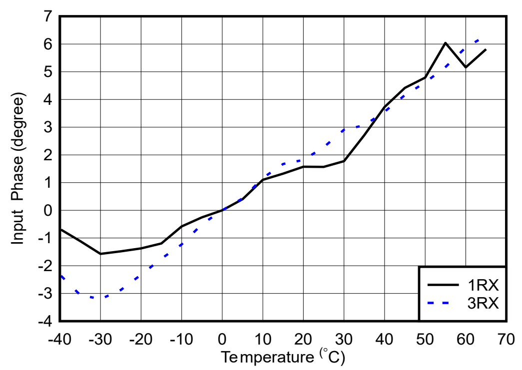
With 0.8GHz matching, normalized to 830MHz

Figure 4-50. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830MHz



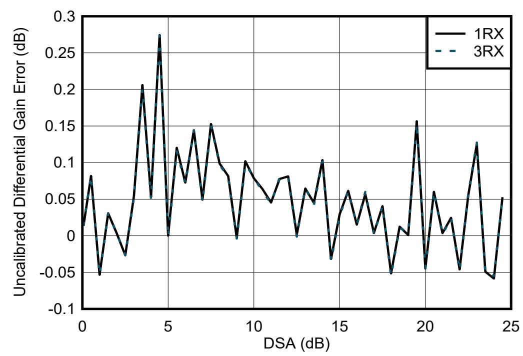
With 0.8GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-51. RX Input Fullscale vs Temperature and Channel at 800MHz



With 0.8GHz matching, normalized to phase at 25°C

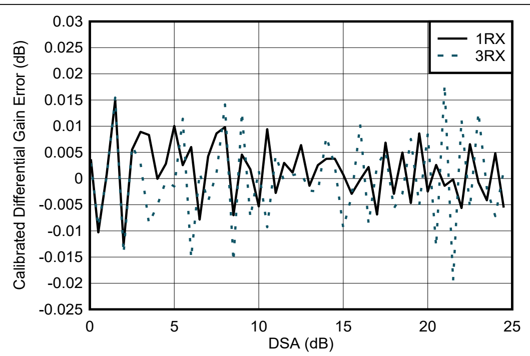
Figure 4-52. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8GHz



With 0.8GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

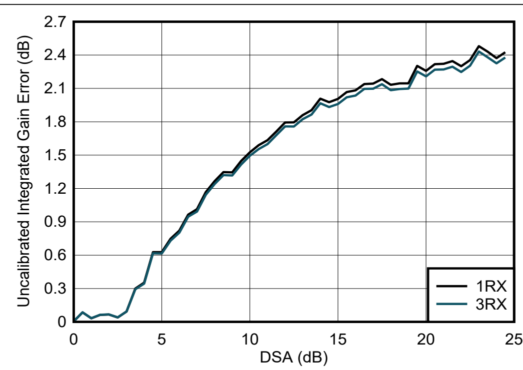
Figure 4-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8GHz



With 0.8GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 4-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8GHz



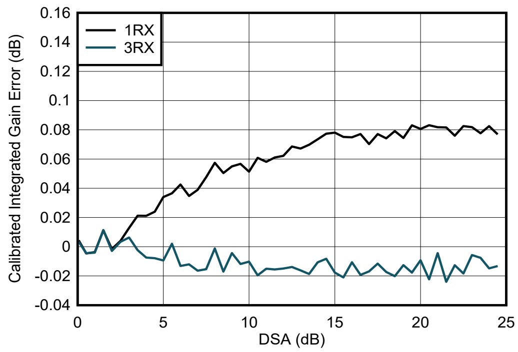
With 0.8GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8GHz

4.12.2 RX Typical Characteristics at 800MHz (continued)

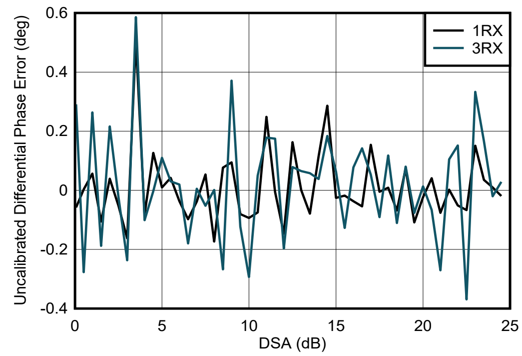
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 0.8GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

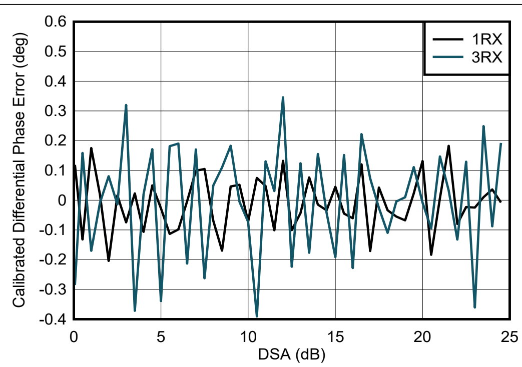
Figure 4-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6GHz



With 0.8GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

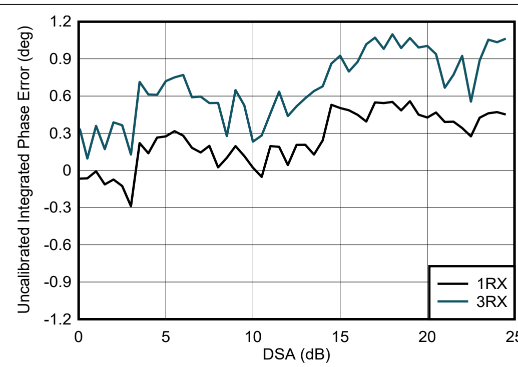
Figure 4-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8GHz



With 0.8GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 4-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8GHz



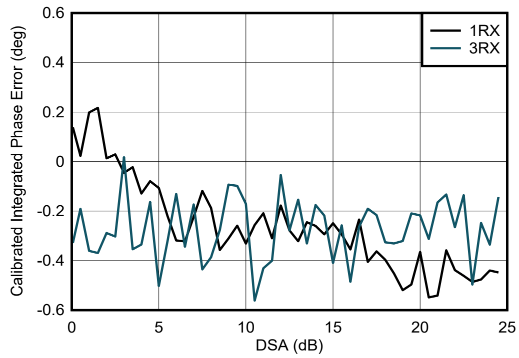
With 0.8GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8GHz

4.12.2 RX Typical Characteristics at 800MHz (continued)

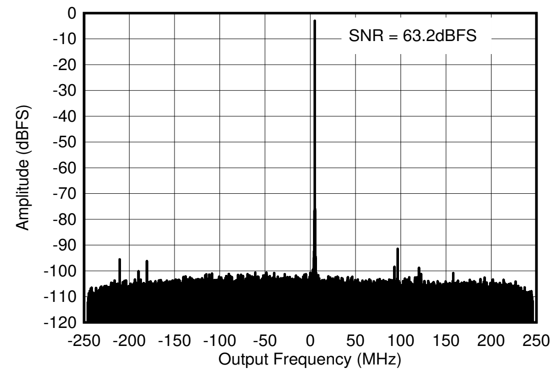
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 0.8GHz matching

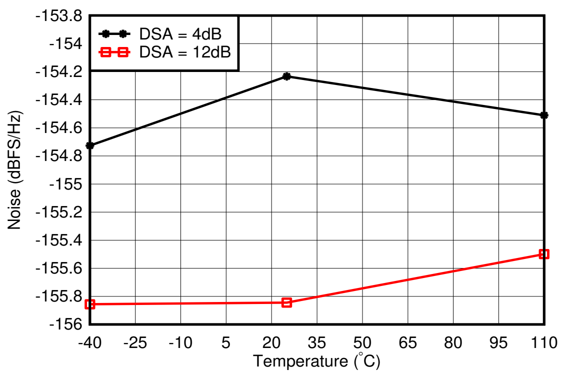
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8GHz



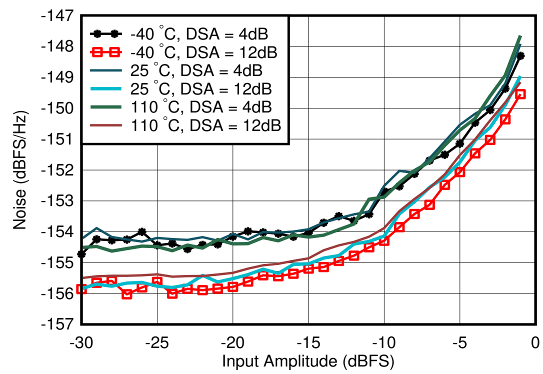
With 0.8GHz matching, f_{IN} = 840MHz, A_{IN}= –3dBFS

Figure 4-61. RX Output FFT at 0.8GHz



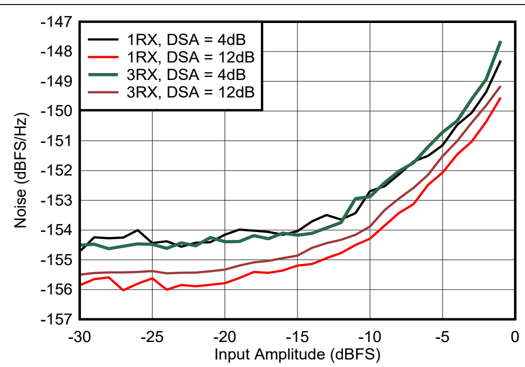
With 0.8GHz matching, 12.5MHz offset from tone

Figure 4-62. RX Noise Spectral Density vs Temperature at 0.8GHz



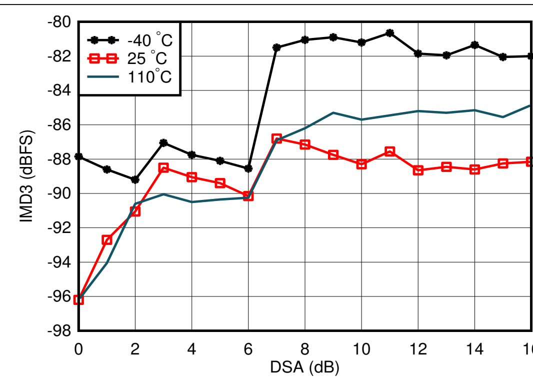
With 0.8GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

Figure 4-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8GHz



With 0.8GHz matching, 12.5MHz offset from tone

Figure 4-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8GHz

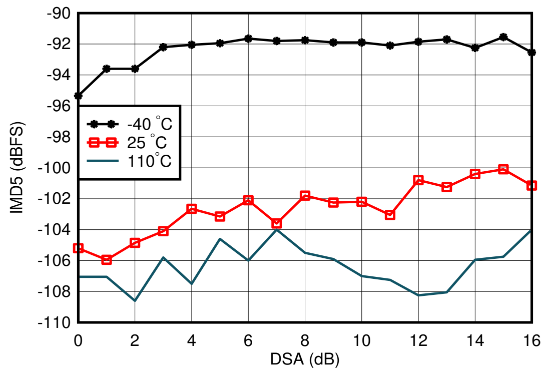


With 0.8GHz matching, each tone –7dBFS, tone spacing = 20MHz

Figure 4-65. RX IMD3 vs DSA Setting and Temperature at 0.8GHz

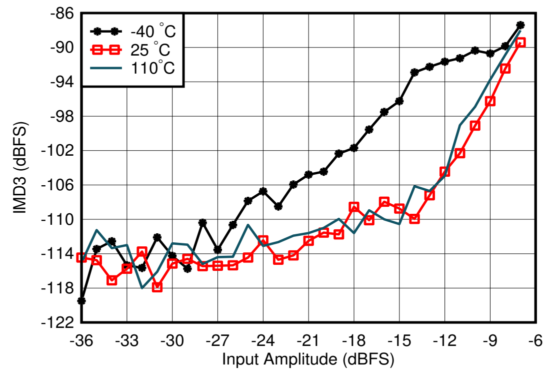
4.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



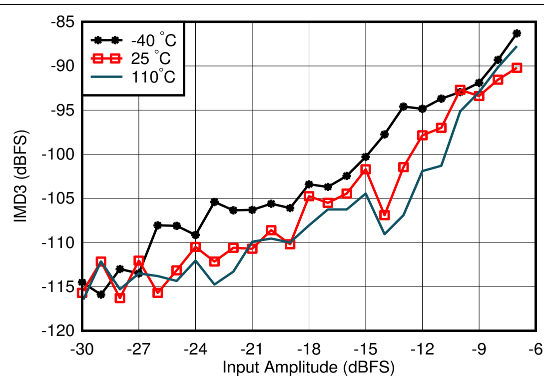
With 0.8GHz matching, each tone –7dBFS, tone spacing = 20MHz

Figure 4-66. RX IMD5 vs DSA Setting and Temperature at 0.8GHz



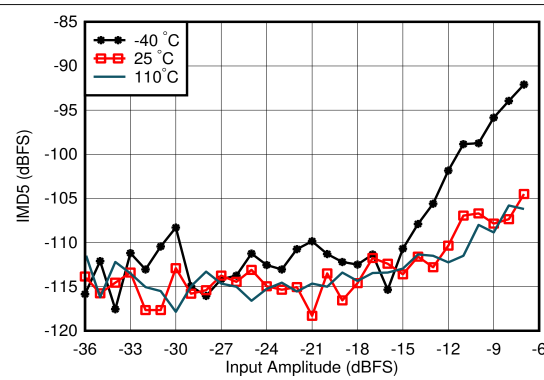
With 0.8GHz matching, tone spacing = 20MHz, DSA = 4dB

Figure 4-67. RX IMD3 vs Input Level and Temperature at 0.8GHz



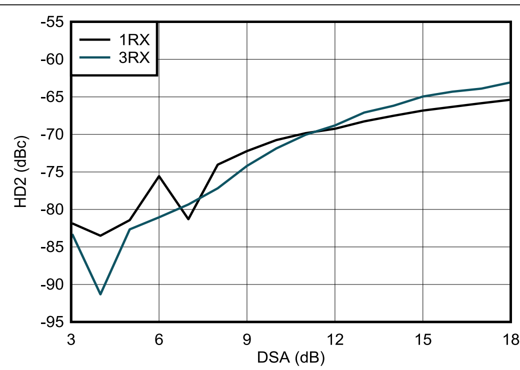
With 0.8GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-68. RX IMD3 vs Input Level and Temperature at 0.8GHz



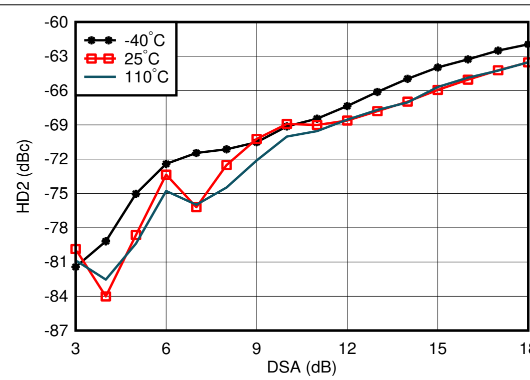
With 0.8GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-69. RX IMD5 vs Input Level and Temperature at 0.8GHz



With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-70. RX HD2 vs DSA Setting and Channel at 0.8GHz

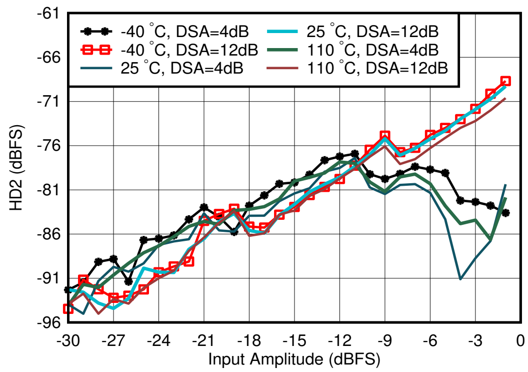


With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-71. RX HD2 vs DSA Setting and Temperature at 0.8GHz

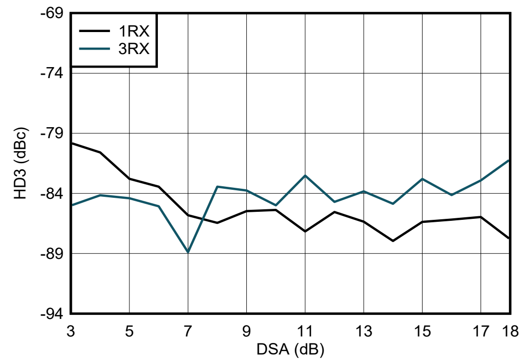
4.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



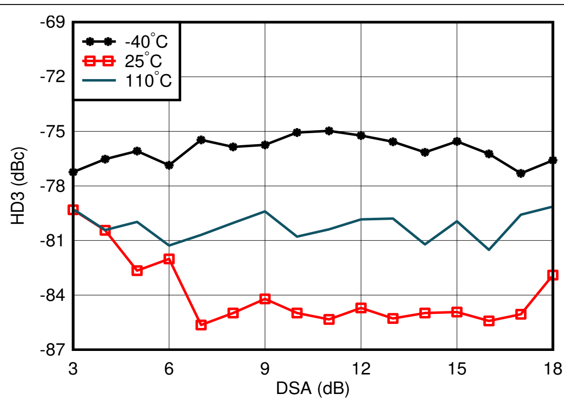
With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-72. RX HD2 vs Input Level and Temperature at 0.8GHz



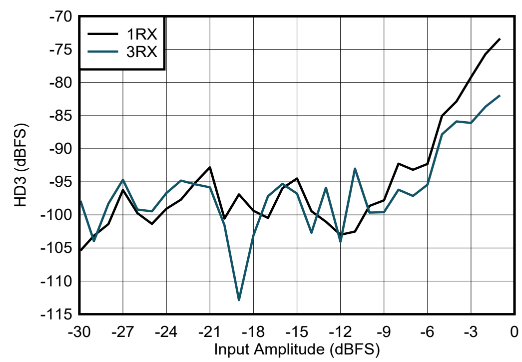
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-73. RX HD3 vs DSA Setting and Channel at 0.8GHz



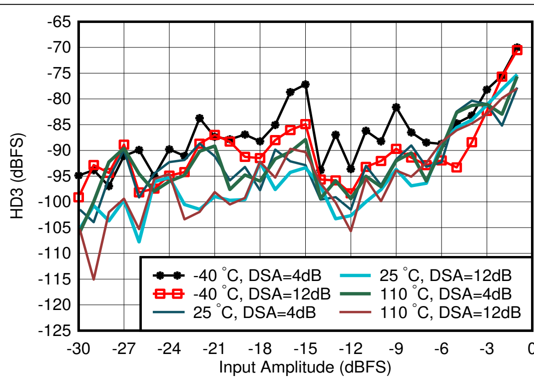
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-74. RX HD3 vs DSA Setting and Temperature at 0.8GHz



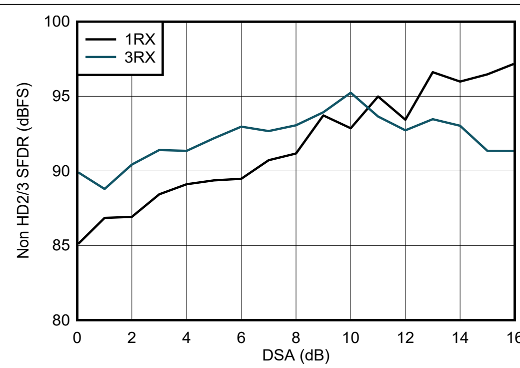
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-75. RX HD3 vs Input Level and Channel at 0.8GHz



With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-76. RX HD3 vs Input Level and Temperature at 0.8GHz

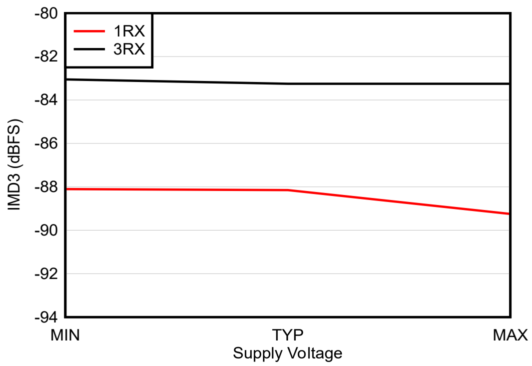


With 0.8GHz matching

Figure 4-77. RX Non-HD2/3 vs DSA Setting at 0.8GHz

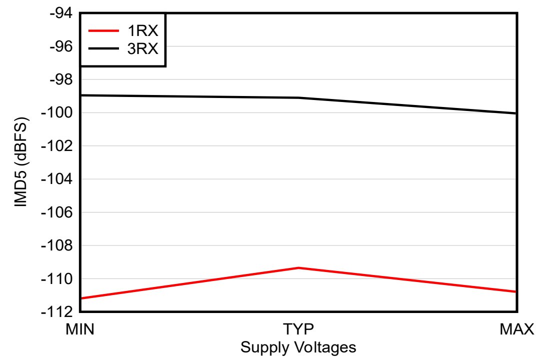
4.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



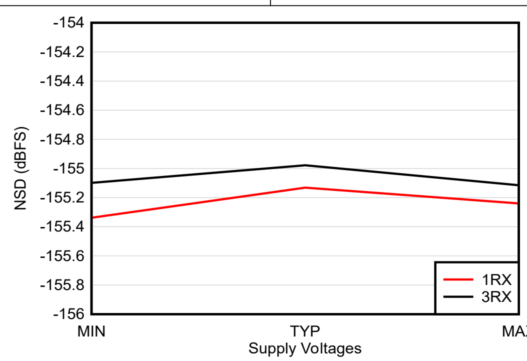
With 0.8GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-78. RX IMD3 vs Supply and Channel at 0.8GHz



With 0.8GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-79. RX IMD5 vs Supply and Channel at 0.8GHz

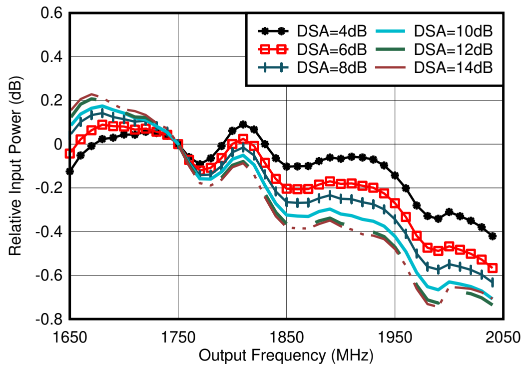


With 0.8GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-80. RX Noise Spectral Density vs Supply and Channel at 0.8GHz

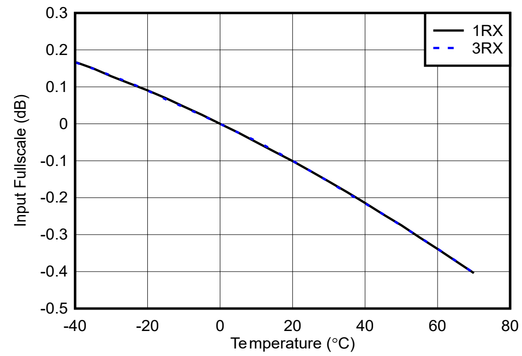
4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



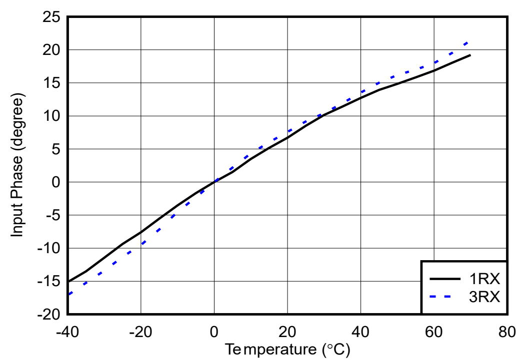
With 1.8GHz matching, normalized to 1.75GHz

Figure 4-81. RX In-Band Gain Flatness, f_{IN} = 1750MHz



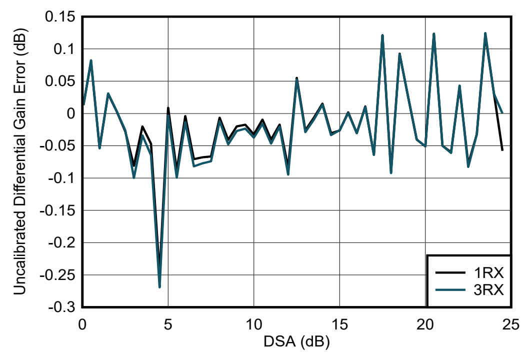
With 1.8GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-82. RX Input Fullscale vs Temperature and Channel at 1.75GHz



With 1.8GHz matching, normalized to phase at 25°C

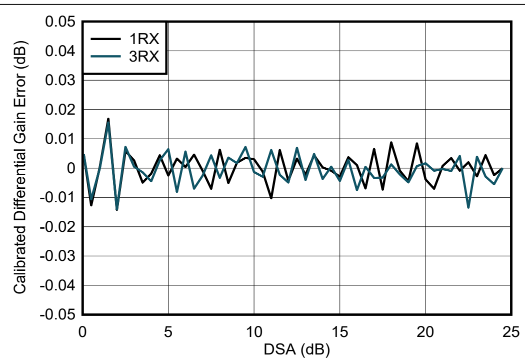
Figure 4-83. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75GHz



With 1.8GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

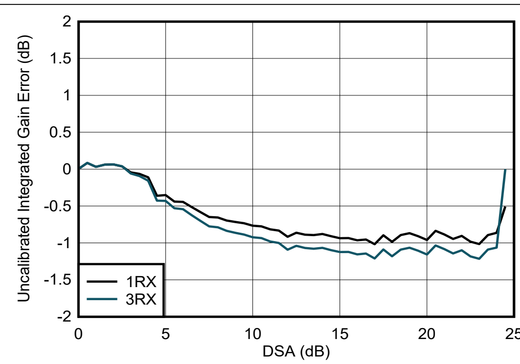
Figure 4-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75GHz



With 1.8GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

Figure 4-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75GHz



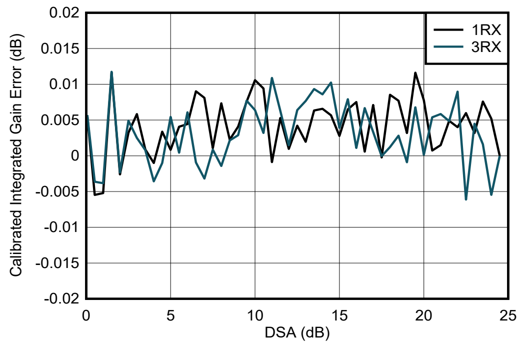
With 1.8GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

Figure 4-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75GHz

4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

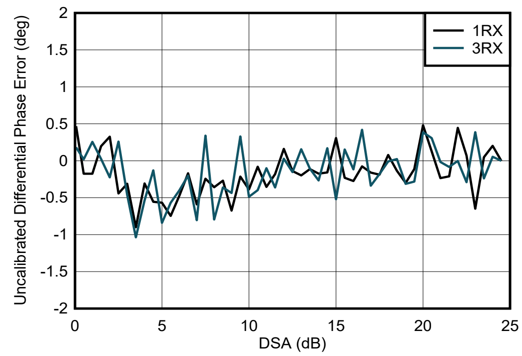
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 1.8GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

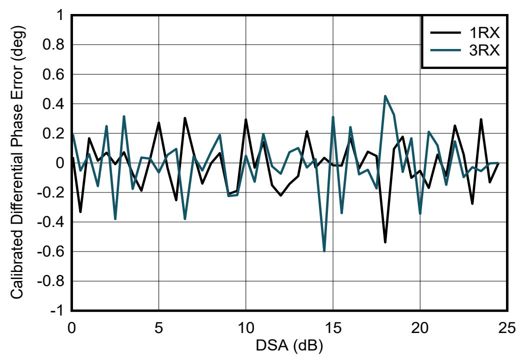
Figure 4-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75GHz



With 1.8GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

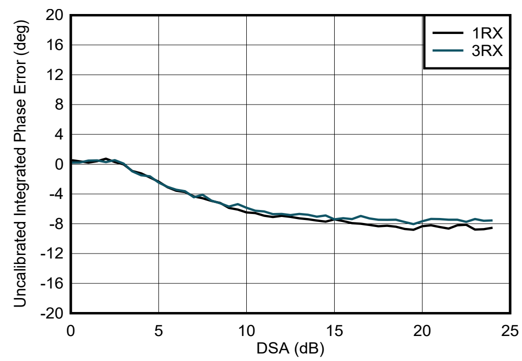
Figure 4-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75GHz



With 1.8GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

Figure 4-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75GHz



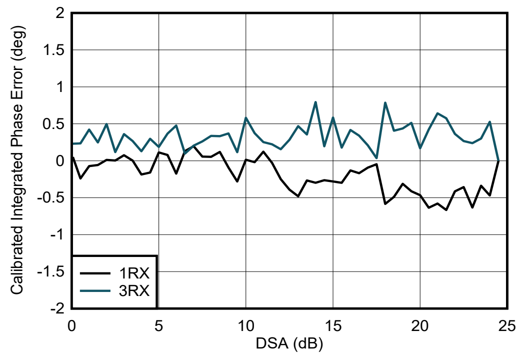
With 1.8GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75GHz

4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

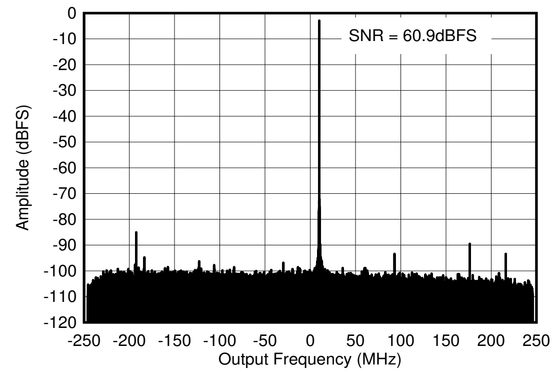
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 1.8GHz matching

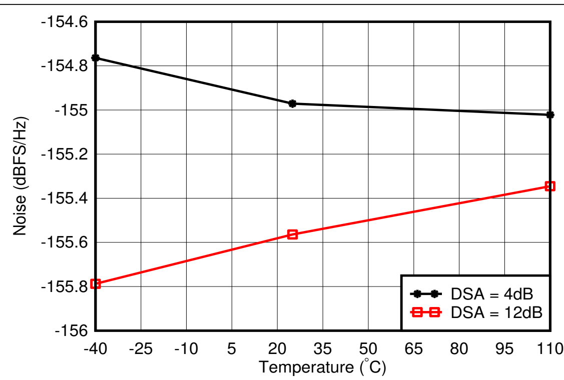
Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

Figure 4-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75GHz



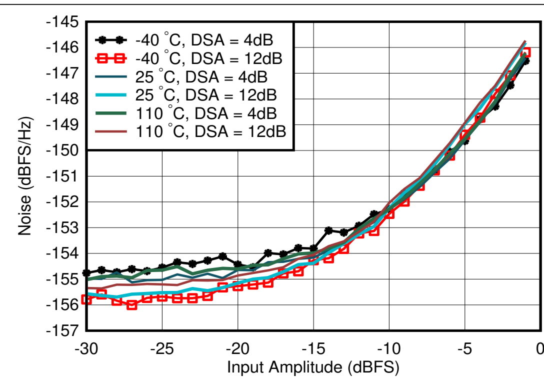
With 1.8GHz matching, f_{IN} = 2610MHz, A_{IN}= –3dBFS

Figure 4-92. RX Output FFT at 1.75GHz



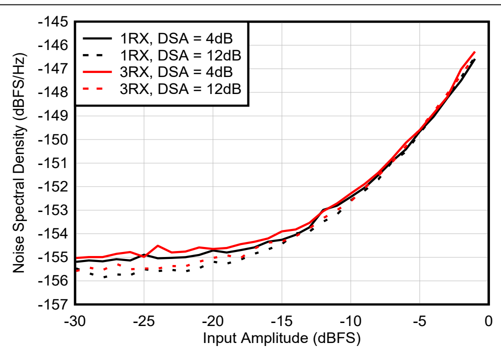
With 1.8GHz matching, 12.5MHz offset from tone

Figure 4-93. RX Noise Spectral Density vs Temperature at 1.75GHz



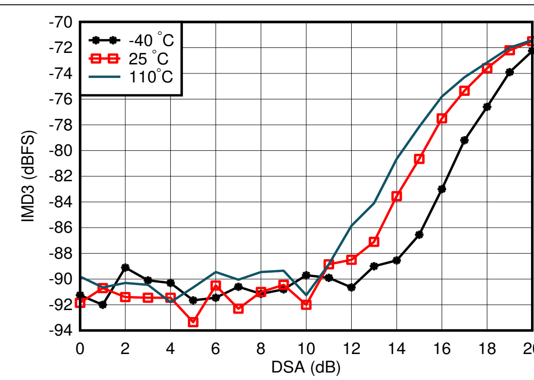
With 1.8GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

Figure 4-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75GHz



With 1.8GHz matching, 12.5MHz offset from tone

Figure 4-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75GHz

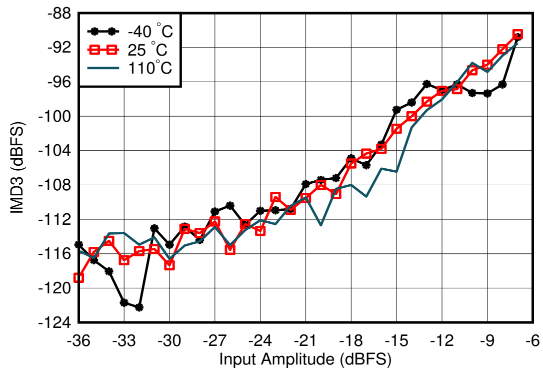


With 1.8GHz matching, each tone –7dBFS, tone spacing = 20MHz

Figure 4-96. RX IMD3 vs DSA Setting and Temperature at 1.75GHz

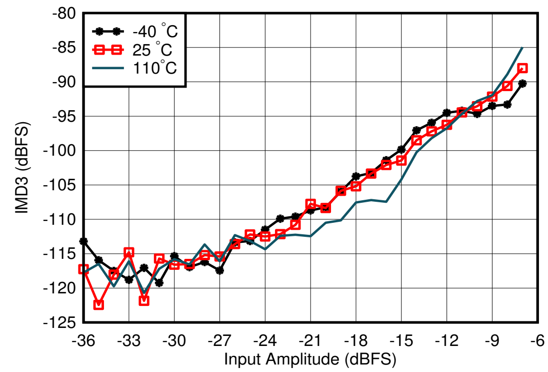
4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



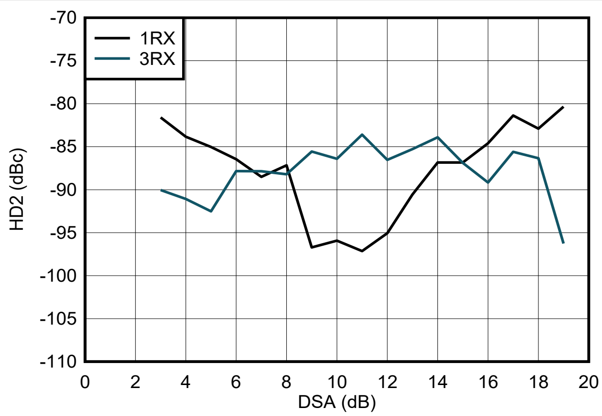
With 1.8GHz matching, tone spacing = 20MHz, DSA = 4dB

Figure 4-97. RX IMD3 vs Input Level and Temperature at 1.75GHz



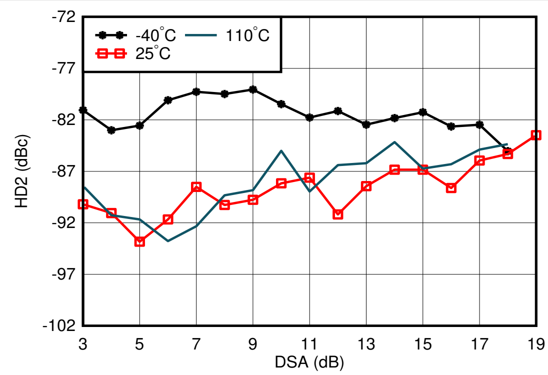
With 1.8GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-98. RX IMD3 vs Input Level and Temperature at 1.75GHz



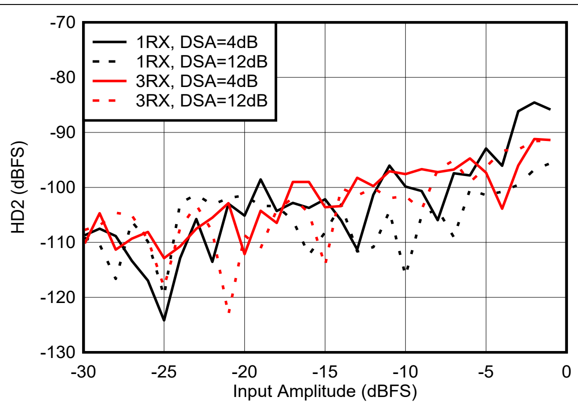
With 1.8GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-99. RX HD2 vs DSA Setting and Channel at 1.9GHz



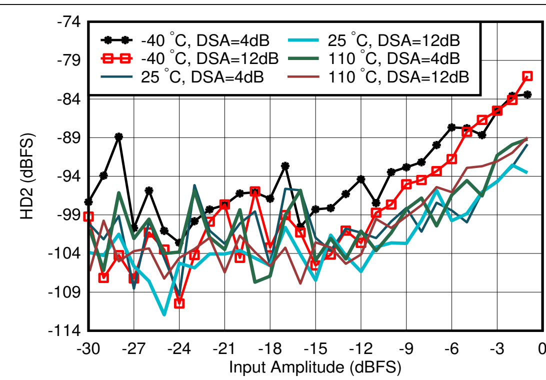
With 1.8GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-100. RX HD2 vs DSA Setting and Temperature at 1.9GHz



With 1.8GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-101. RX HD2 vs Input Amplitude and Channel at 1.9GHz

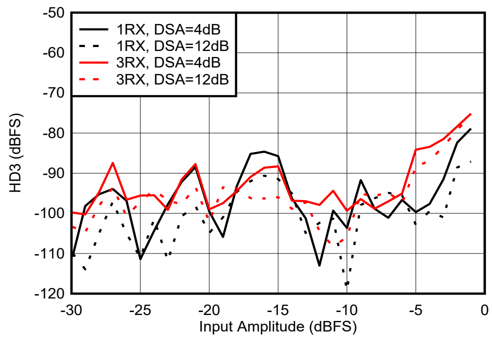


With 1.8GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-102. RX HD2 vs Input Amplitude and Temperature at 1.9GHz

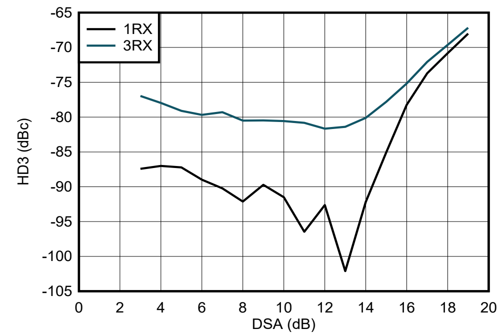
4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



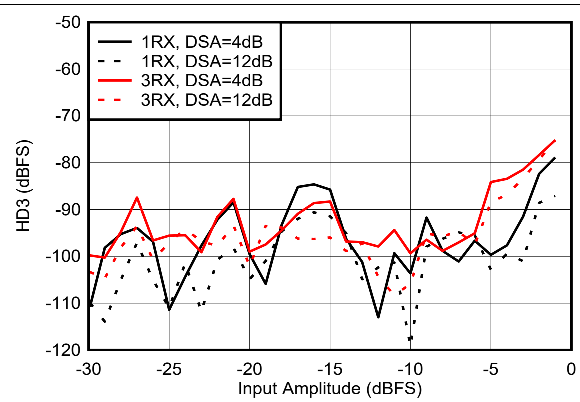
With 1.8GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-103. RX HD3 vs DSA Setting and Channel at 1.9GHz



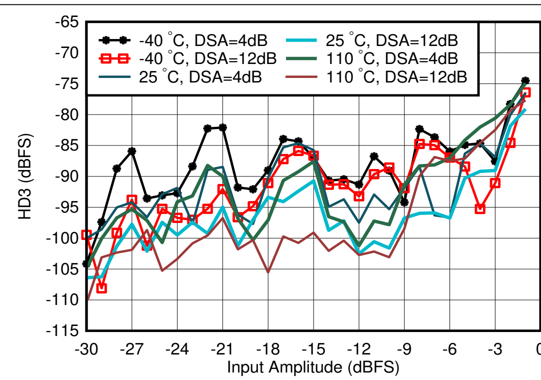
With 1.8GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-104. RX HD3 vs DSA Setting and Temperature at 1.9GHz



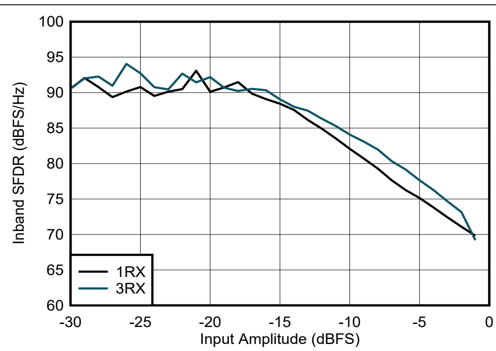
With 1.8GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-105. RX HD3 vs Input Level and Channel at 1.9GHz



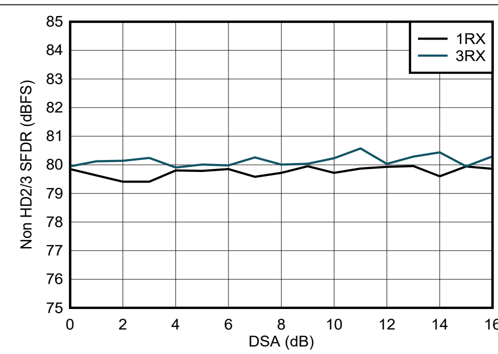
With 1.8GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 4-106. RX HD3 vs Input Level and Temperature at 1.9GHz



With 1.8GHz matching, decimated by 3

Figure 4-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75GHz

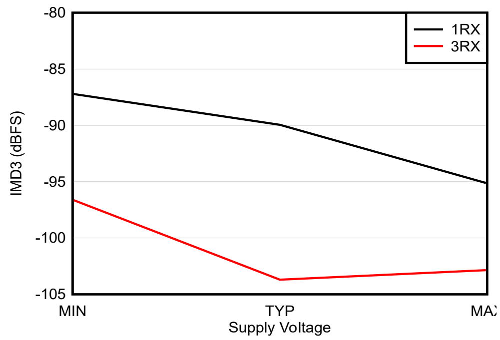


With 1.8GHz matching

Figure 4-108. RX Non-HD2/3 vs DSA Setting at 1.75GHz

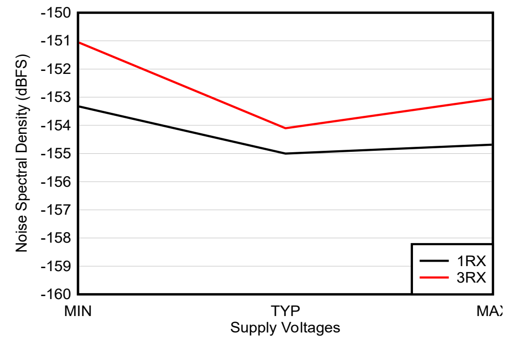
4.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 1.8GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-109. RX IMD3 vs Supply and Channel at 1.75GHz

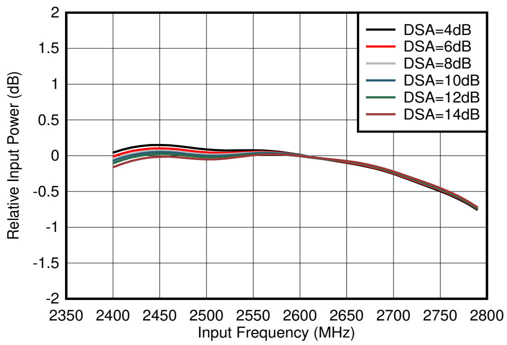


With 1.8GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-110. RX Noise Spectral Density vs Supply and Channel at 1.75GHz

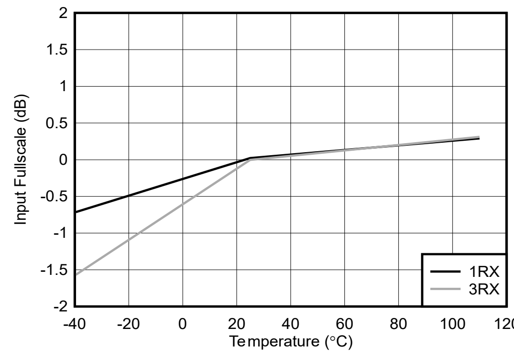
4.12.4 RX Typical Characteristics 2.6GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



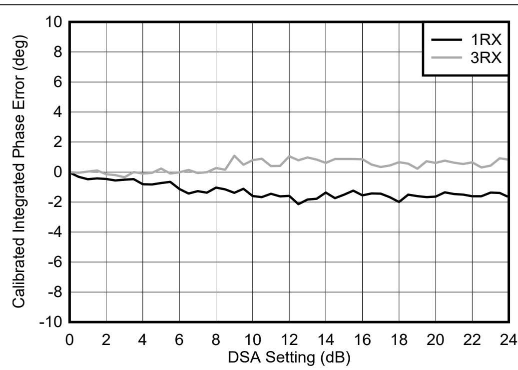
With matching, normalized to power at 2.6GHz for each DSA setting

Figure 4-111. RX Inband Gain Flatness, f_{IN} = 2600MHz



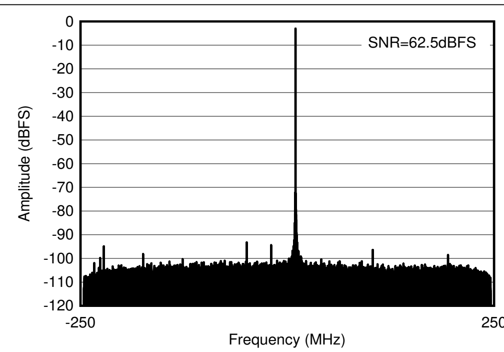
With 2.6GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-112. RX Input Fullscale vs Temperature and Channel at 2.6GHz



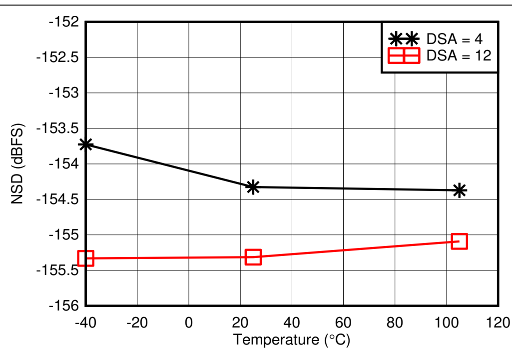
With 2.6GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6GHz



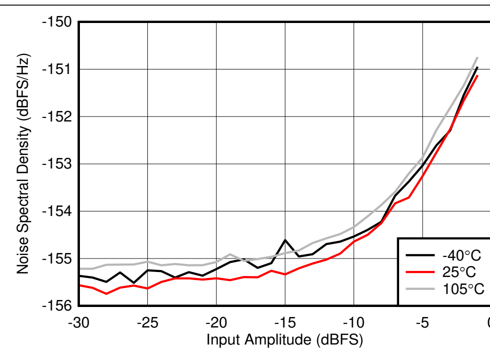
With 2.6GHz matching, f_{IN} = 2610MHz, A_{IN}= –3dBFS

Figure 4-114. RX Output FFT at 2.6GHz



With 2.6GHz matching, 12.5MHz offset from tone

Figure 4-115. RX Noise Spectral Density vs Temperature at 2.6GHz

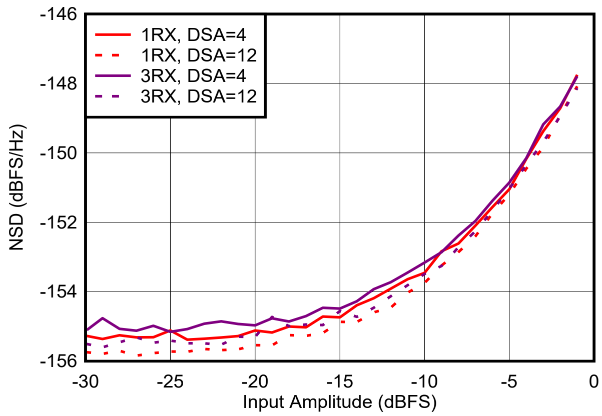


With 2.6GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

Figure 4-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6GHz

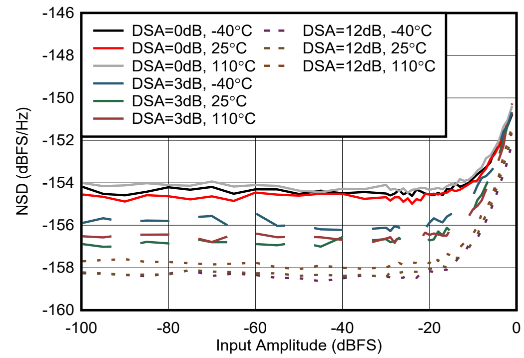
4.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



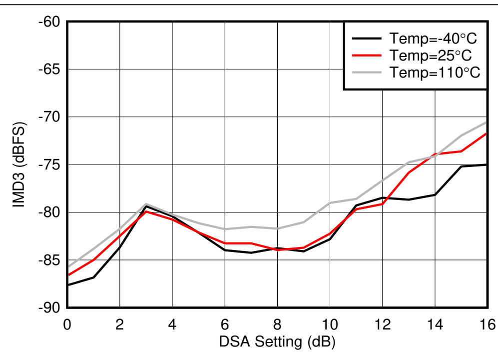
With 2.6GHz matching, 12.5MHz offset from tone

Figure 4-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6GHz



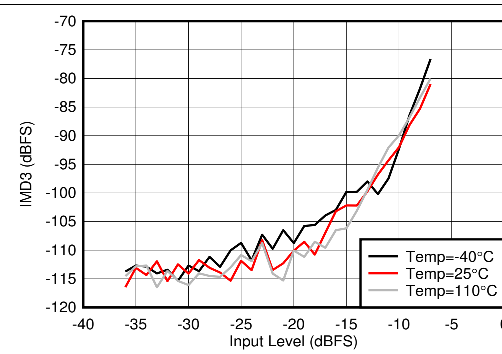
50MHz offset from tone, external clock mode

Figure 4-118. RX Noise Spectral Density vs Input Amplitude at 2.61GHz (Ext. Clock)



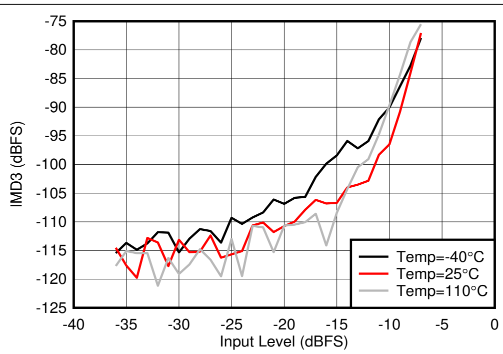
With 2.6GHz matching, each tone –7 dBFS, tone spacing = 20MHz

Figure 4-119. RX IMD3 vs DSA Setting and Temperature at 2.6GHz



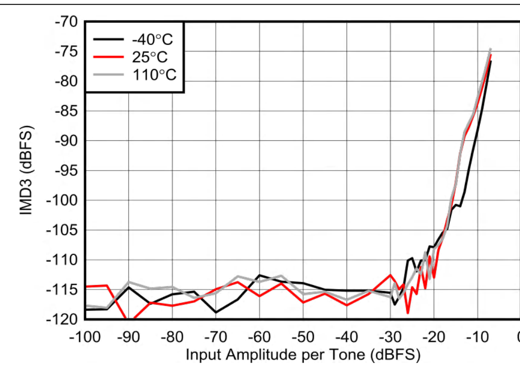
With 2.6GHz matching, tone spacing = 20MHz, DSA = 4dB

Figure 4-120. RX IMD3 vs Input Level and Temperature at 2.6GHz



With 2.6GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-121. RX IMD3 vs Input Level and Temperature at 2.6GHz

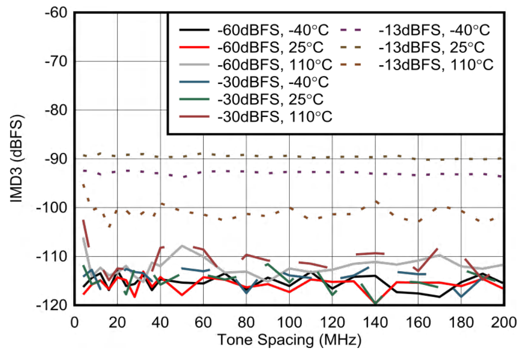


Tone spacing = 50MHz, External clock mode

Figure 4-122. RX IMD3 vs Input Level at 2.6GHz (Ext. Clock)

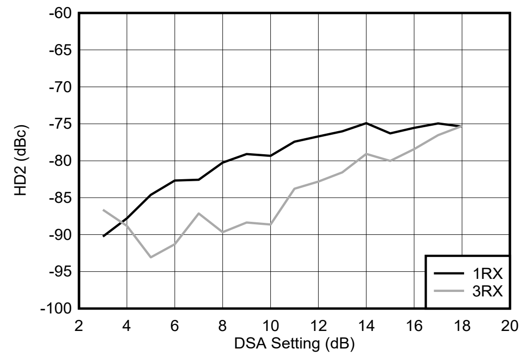
4.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



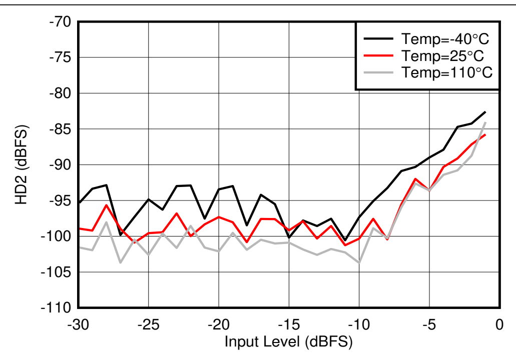
External clock mode

Figure 4-123. RX IMD3 vs Tone Spacing at 2.6GHz (Ext. Clock)



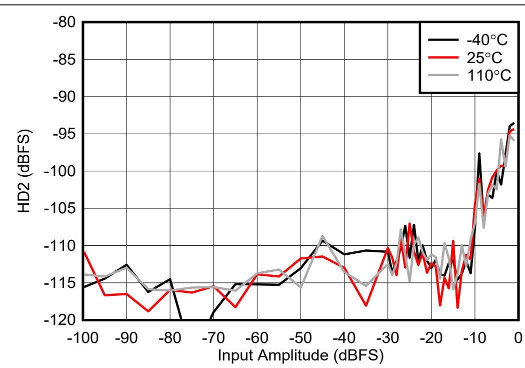
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-124. RX HD2 vs DSA Setting and Channel at 2.6GHz



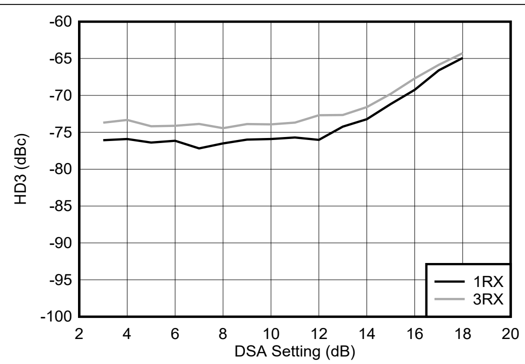
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-125. RX HD2 vs Input Level and Temperature at 2.6GHz



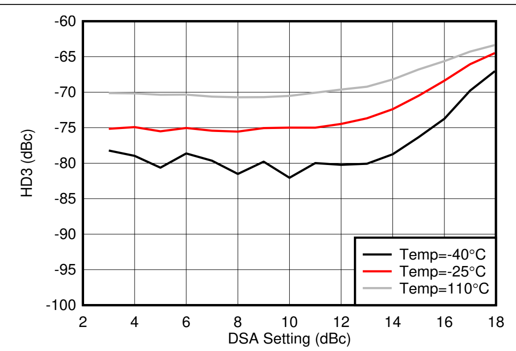
External clock mode

Figure 4-126. RX HD2 vs Input Level and Temperature at 2.6GHz



With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-127. RX HD3 vs DSA Setting and Channel at 2.6GHz

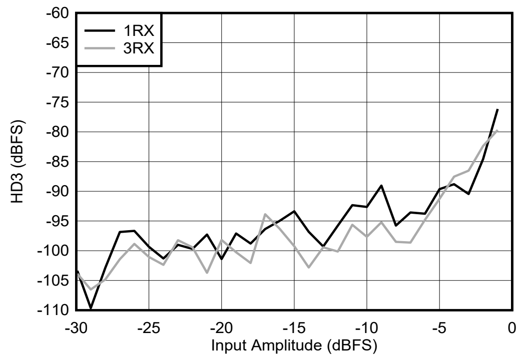


With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-128. RX HD3 vs DSA Setting and Temperature at 2.6GHz

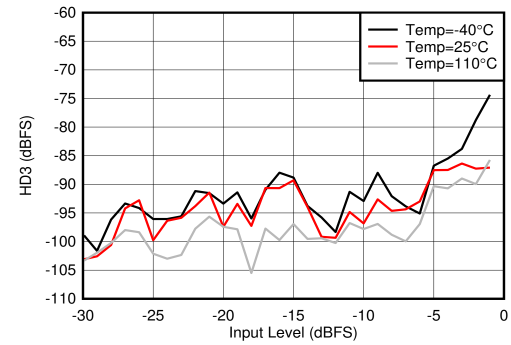
4.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



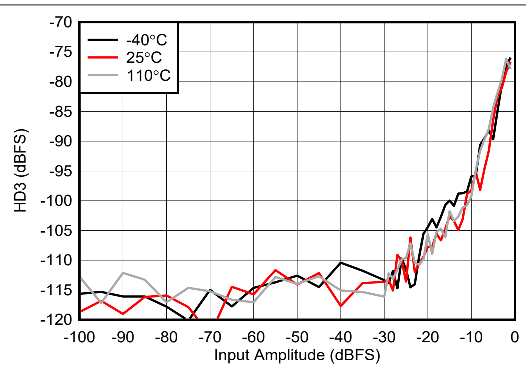
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-129. RX HD3 vs Input Level and Channel at 2.6GHz



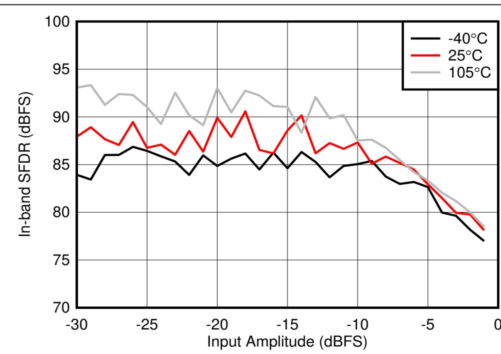
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-130. RX HD3 vs Input Level and Temperature at 2.6GHz



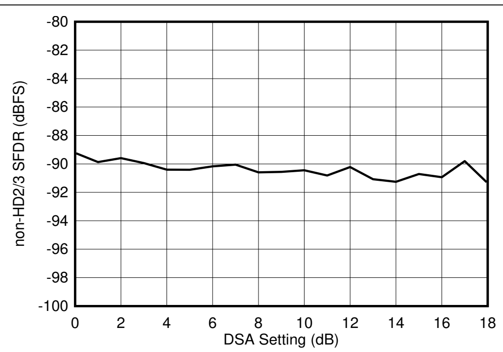
External clock mode

Figure 4-131. RX HD3 vs Input Level and Temperature at 2.6GHz



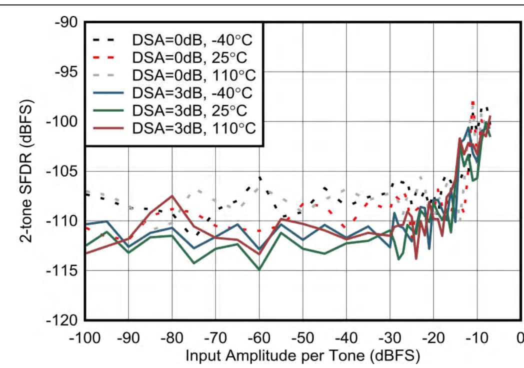
With 2.6GHz matching, decimate by 4

Figure 4-132. RX In-Band SFDR (±300MHz) vs Input Amplitude and Temperature at 2.6GHz



With 2.6GHz matching

Figure 4-133. RX Non-HD2/3 vs DSA Setting at 2.6GHz

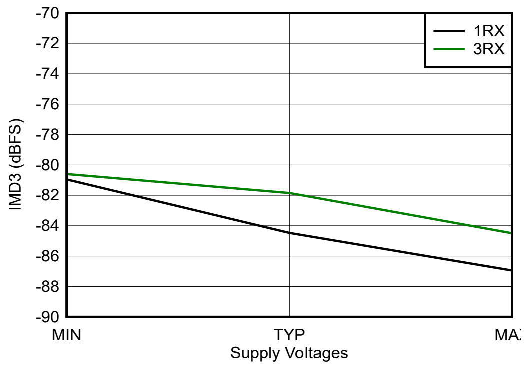


External clock mode, 50MHz tone spacing, excluding 3rd order distortion

Figure 4-134. RX 2-Tone SFDR vs Input Amplitude at 2.6GHz

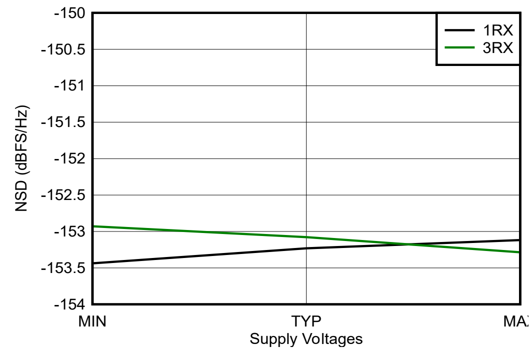
4.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 2.6GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-135. RX IMD3 vs Supply and Channel at 2.6GHz

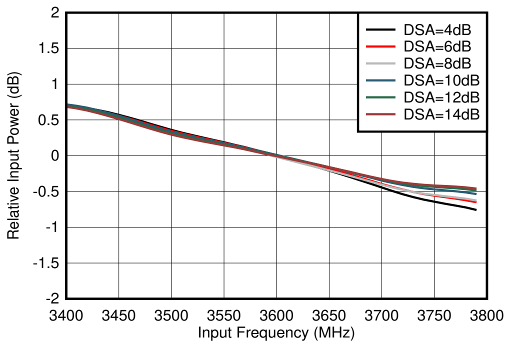


With 2.6GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-136. RX Noise Spectral Density vs Supply and Channel at 2.6GHz

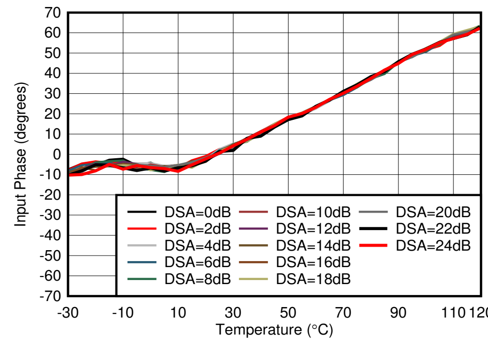
4.12.5 RX Typical Characteristics 3.5GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



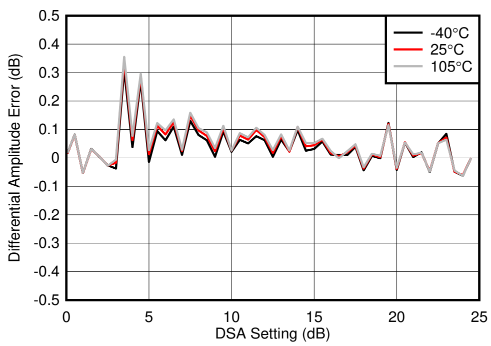
With 3.6GHz matching, normalized to 3.6GHz

Figure 4-137. RX In-Band Gain Flatness, f_{IN} = 3600MHz



With 3.6GHz matching, normalized to phase at 25°C

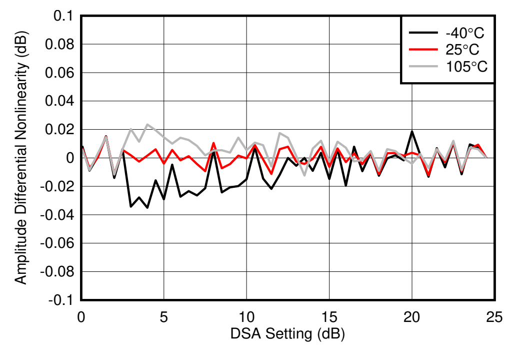
Figure 4-138. RX Input Phase vs Temperature at 3.6GHz



With 3.6GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

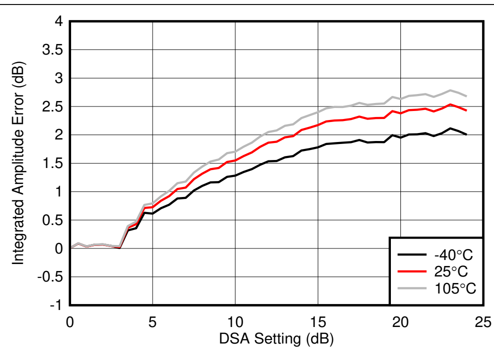
Figure 4-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6GHz



With 3.6GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

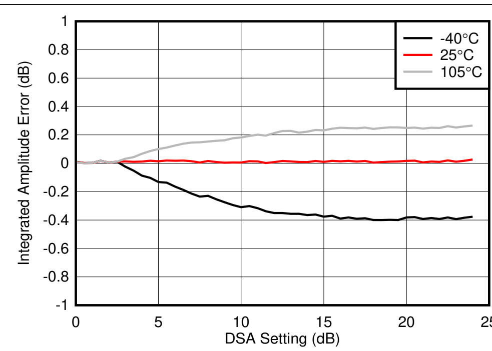
Figure 4-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6GHz



With 3.6GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6GHz



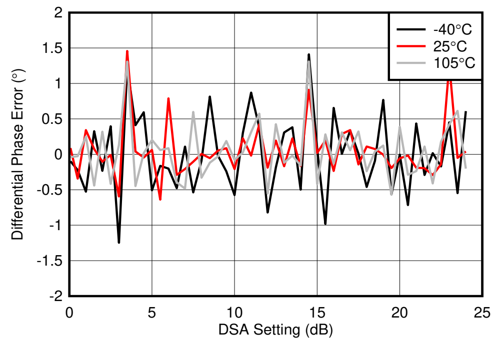
With 3.6GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 4-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6GHz

4.12.5 RX Typical Characteristics 3.5GHz (continued)

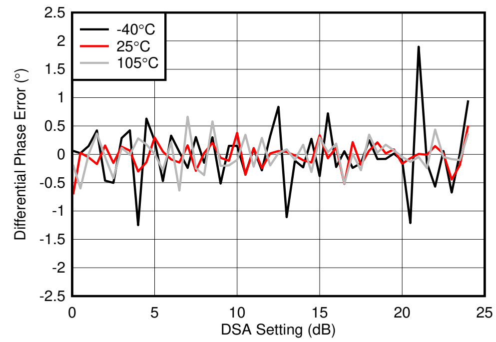
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 3.6GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

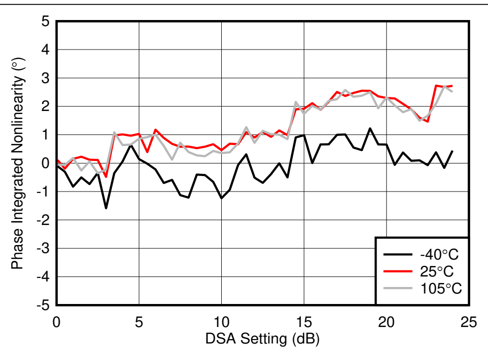
Figure 4-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6GHz



With 3.6GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

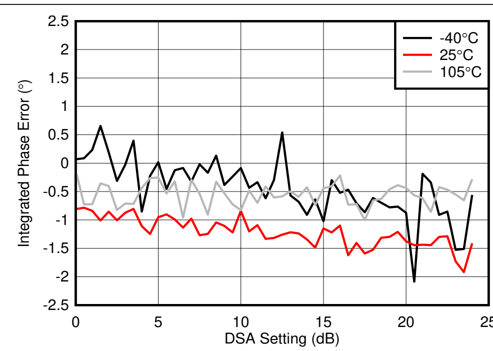
Figure 4-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6GHz



With 3.6GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

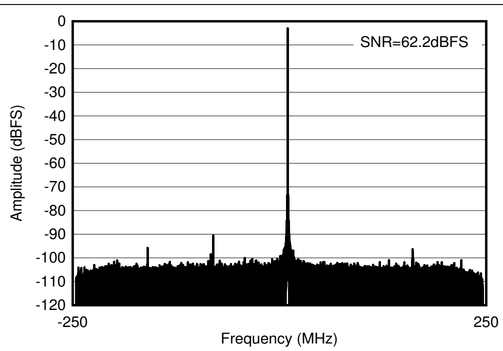
Figure 4-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6GHz



With 3.6GHz matching

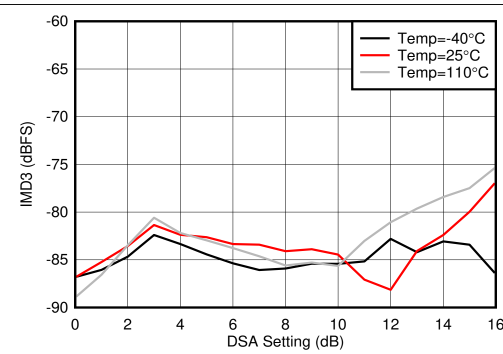
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6GHz



With 3.6GHz matching , f_{IN} = 3610MHz, A_{IN} = –3dBFS

Figure 4-147. RX Output FFT at 3.6GHz

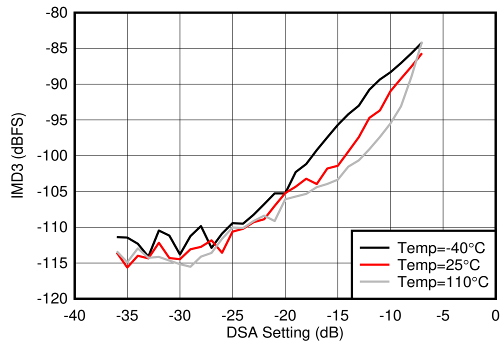


With 3.5GHz matching, each tone at –7dBFS, 20MHz tone spacing

Figure 4-148. RX IMD3 vs DSA Setting and Temperature at 3.6GHz

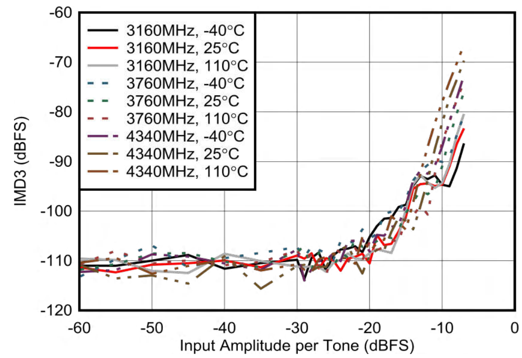
4.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



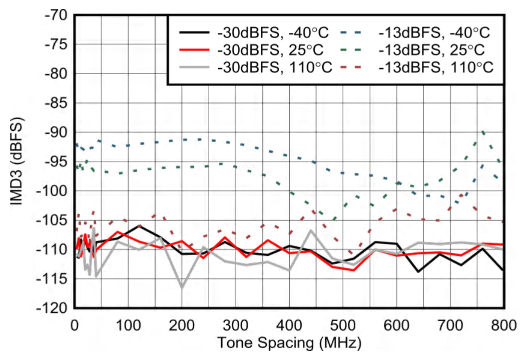
With 3.5GHz matching, 20MHz tone spacing

Figure 4-149. RX IMD3 vs Input Level and Temperature at 3.6GHz



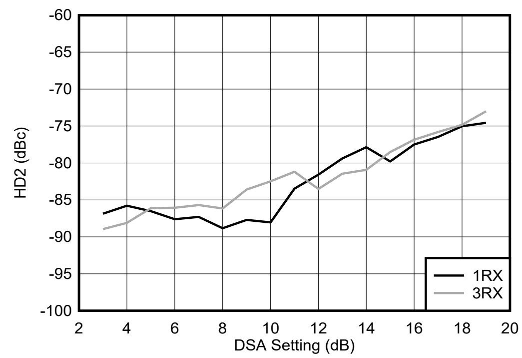
External clock mode, 20MHz tone spacing, 2x Decimation

Figure 4-150. RX IMD3 vs Input Level



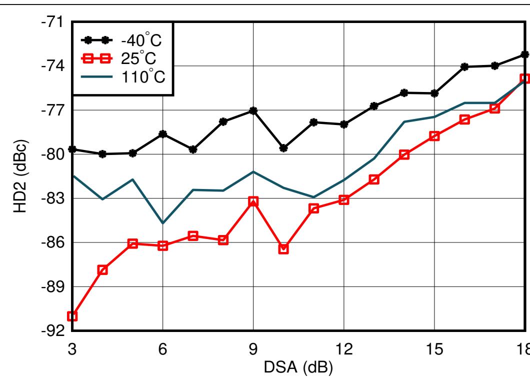
External clock mode, 2x Decimation

Figure 4-151. RX IMD3 vs Tone Spacing at 3.76GHz



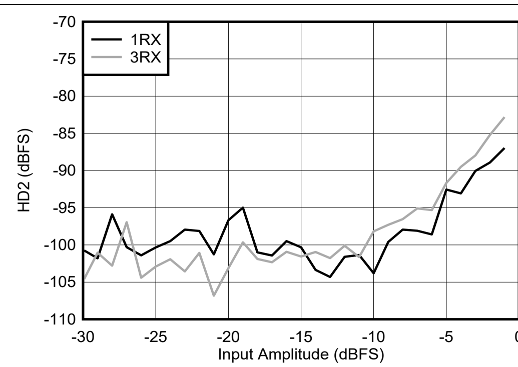
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-152. RX HD2 vs DSA Setting and Channel at 3.6GHz



With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-153. RX HD2 vs DSA Setting and Temperature at 3.6GHz

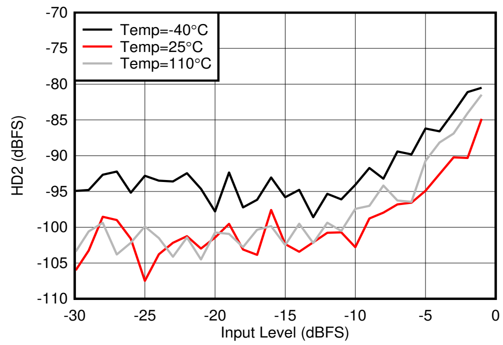


With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-154. RX HD2 vs Input Level and Channel at 3.6GHz

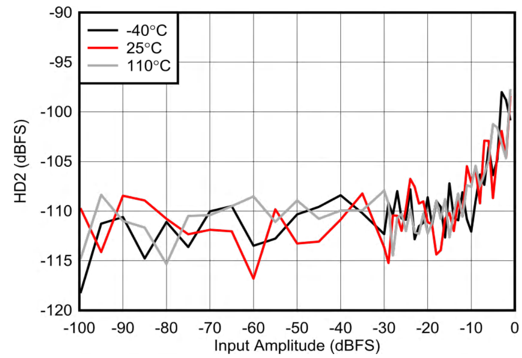
4.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



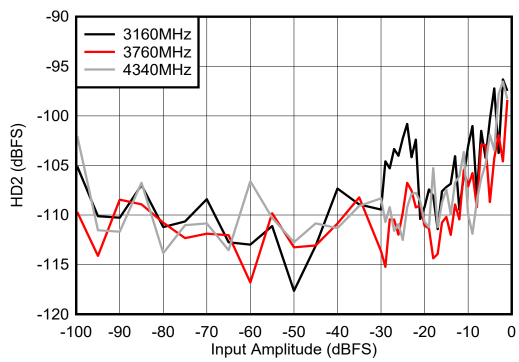
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-155. RX HD2 vs Input Level and Temperature at 3.6GHz



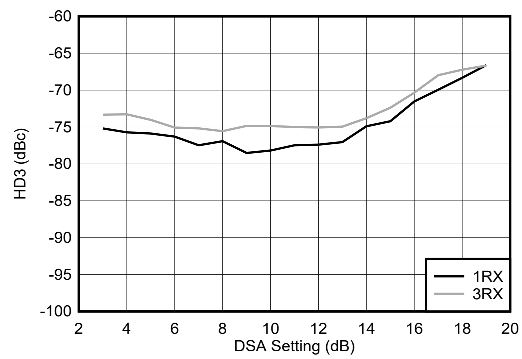
External clock mode, 2x Decimation

Figure 4-156. RX HD2 vs Input Level at 3.76GHz



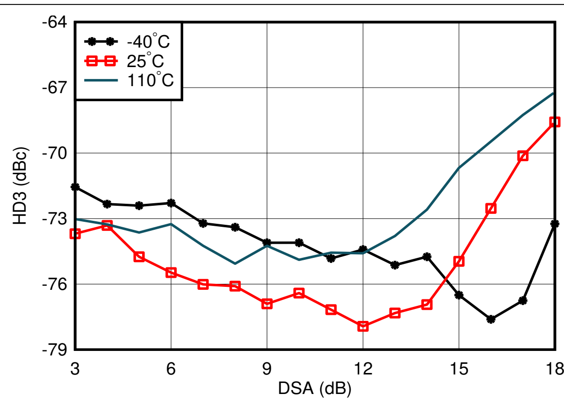
External clock mode, 25°C, 2x Decimation

Figure 4-157. RX HD2 vs Input Level



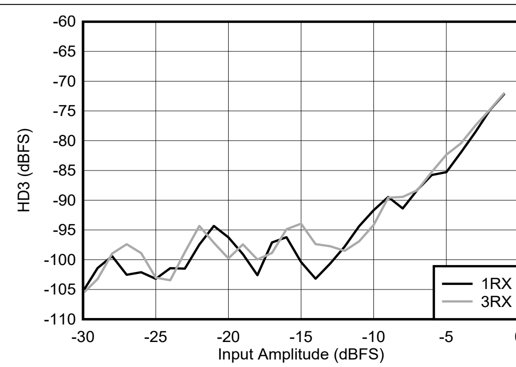
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-158. RX HD3 vs DSA Setting and Channel at 3.6GHz



With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-159. RX HD3 vs DSA Setting and Temperature at 3.6GHz

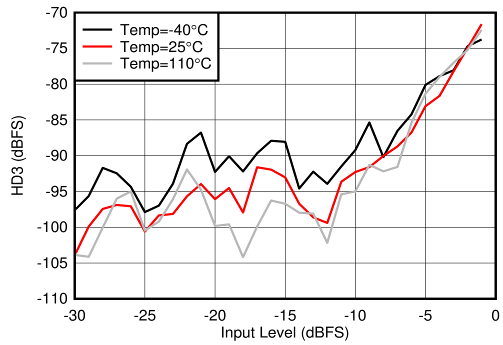


With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-160. RX HD3 vs Input Level and Channel at 3.6GHz

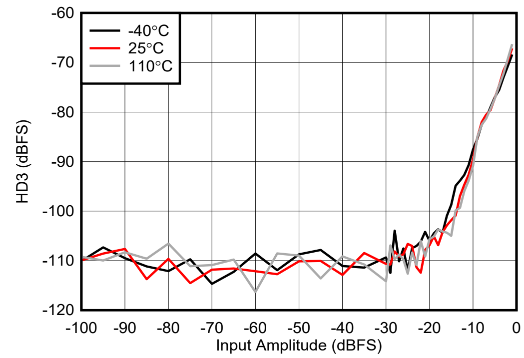
4.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



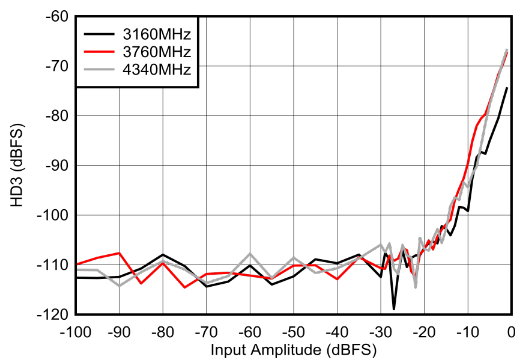
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-161. RX HD3 vs Input Level and Temperature at 3.6GHz



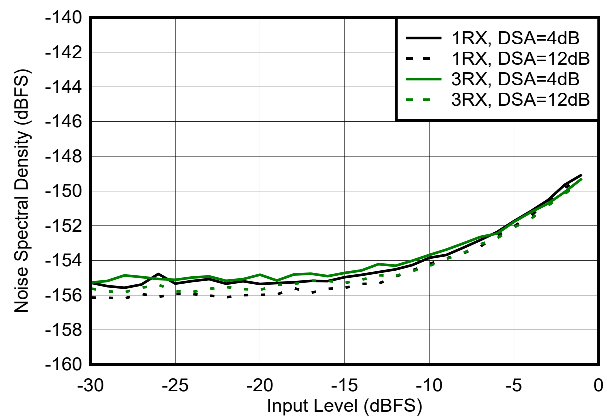
External clock mode, 2x Decimation

Figure 4-162. RX HD3 vs Input Level at 3.76GHz



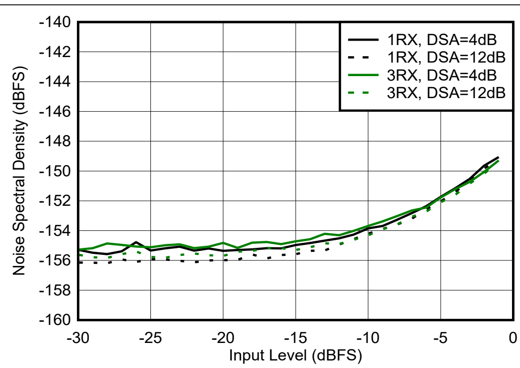
External clock mode, 25°C, 2x Decimation

Figure 4-163. RX HD3 vs Input Level



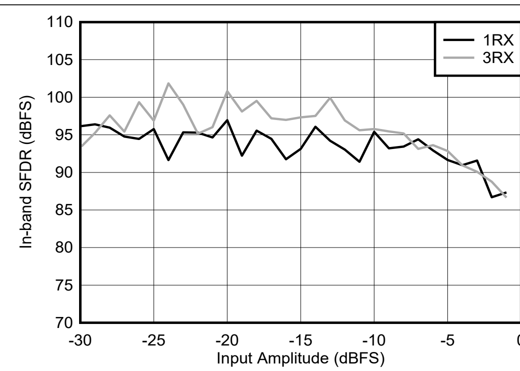
With 3.5GHz matching, 12.5MHz offset from tone

Figure 4-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6GHz



External clock mode, 25°C, 2x Decimation

Figure 4-165. RX Noise Spectral Density vs Input Level at 3.76GHz

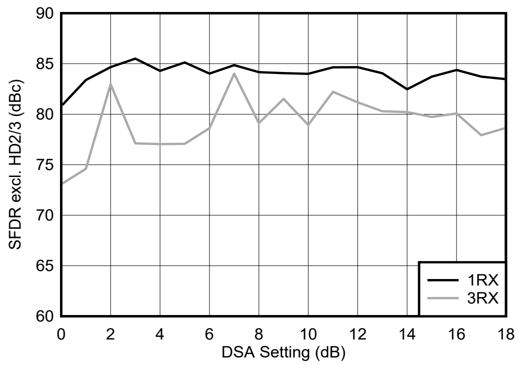


With 3.5GHz matching

Figure 4-166. RX In-Band SFDR (±200MHz) vs Input Level and Channel at 3.6GHz

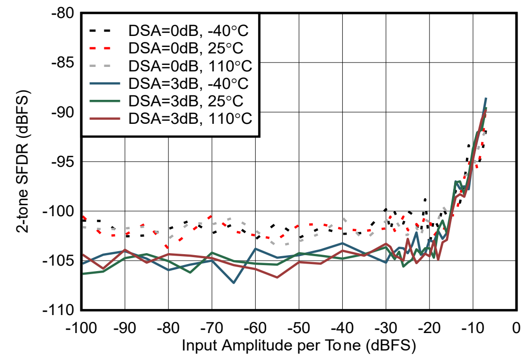
4.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



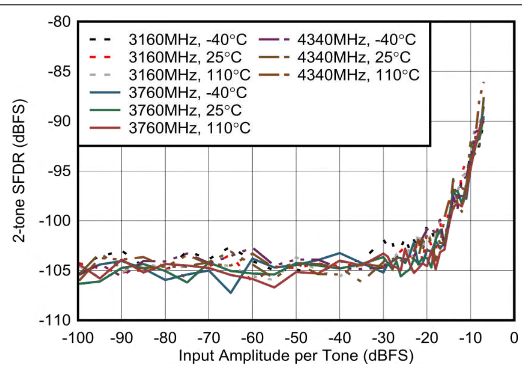
With 3.5GHz matching

Figure 4-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6GHz



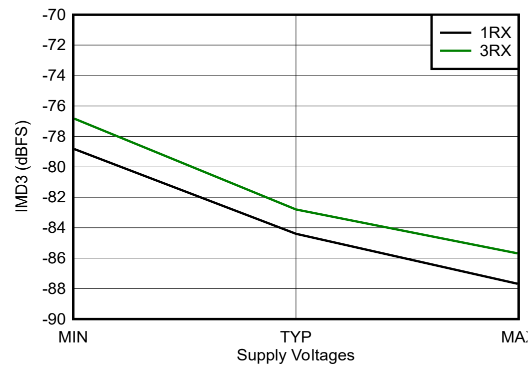
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 4-168. RX 2-Tone SFDR vs Input Amplitude and DSA Setting at 3.7GHz



External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 4-169. RX 2-Tone SFDR vs Input Amplitude and Frequency at 3.7GHz

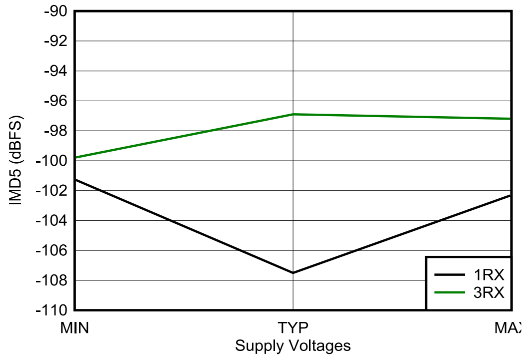


With 3.6GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-170. RX IMD3 vs Supply Voltage and Channel at 3.6GHz

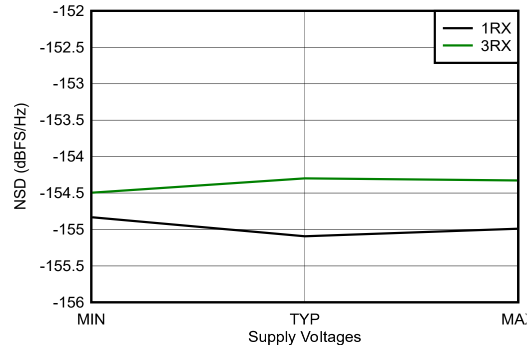
4.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 3.6GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-171. RX IMD5 vs Supply Voltage and Channel at 3.6GHz

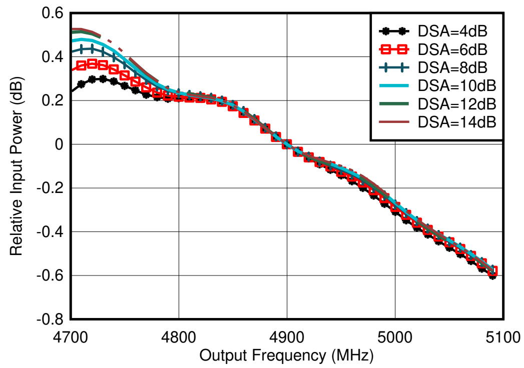


With 3.6GHz matching, tone at –20dBFS, 12.5MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6GHz

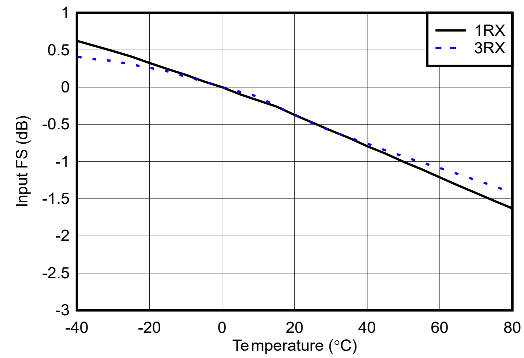
4.12.6 RX Typical Characteristics 4.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



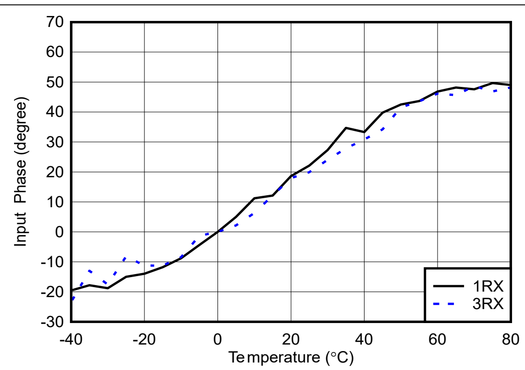
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 4-173. RX Inband Gain Flatness, f_{IN} = 4900MHz



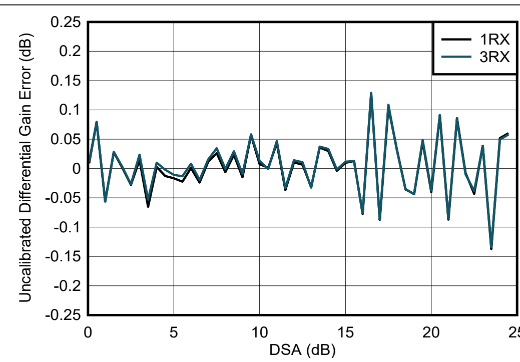
With 4.9GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-174. RX Input Fullscale vs Temperature and Channel at 4.9GHz



With 4.9GHz matching, normalized to phase at 25°C

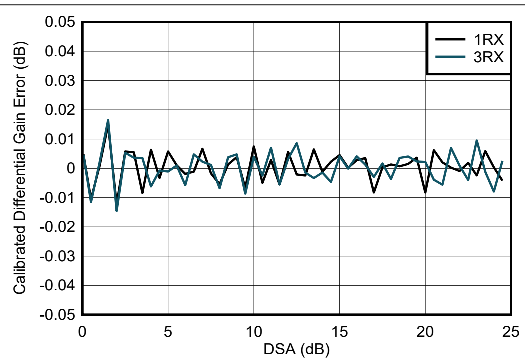
Figure 4-175. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9GHz



With 4.9GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

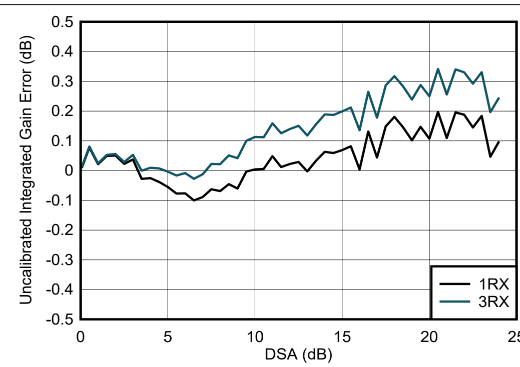
Figure 4-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9GHz



With 4.9GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

Figure 4-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9GHz



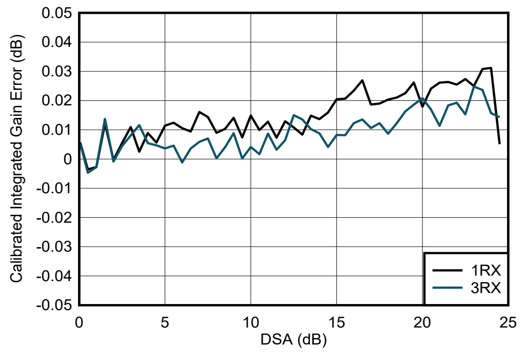
With 4.9GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

Figure 4-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9GHz

4.12.6 RX Typical Characteristics 4.9GHz (continued)

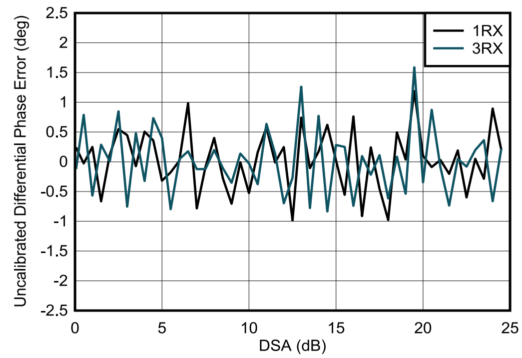
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



With 4.9GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

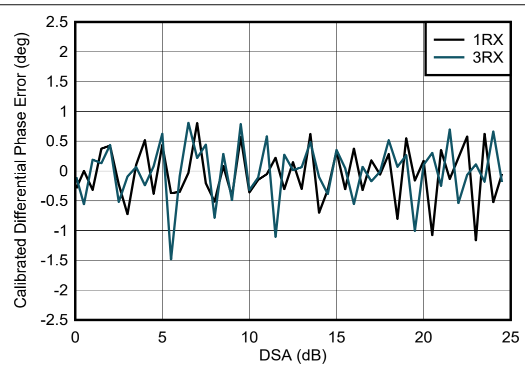
Figure 4-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9GHz



With 4.9GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

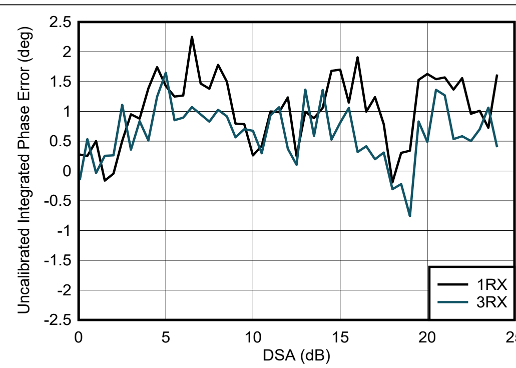
Figure 4-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9GHz



With 4.9GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

Figure 4-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9GHz



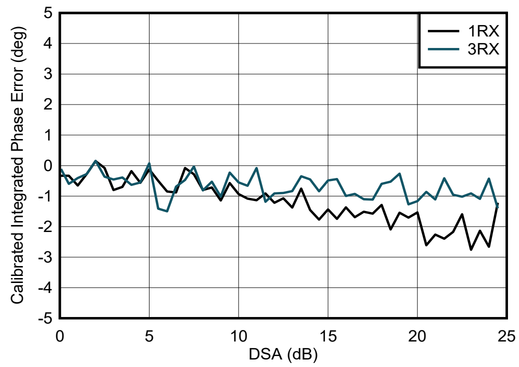
With 4.9GHz matching

Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

Figure 4-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9GHz

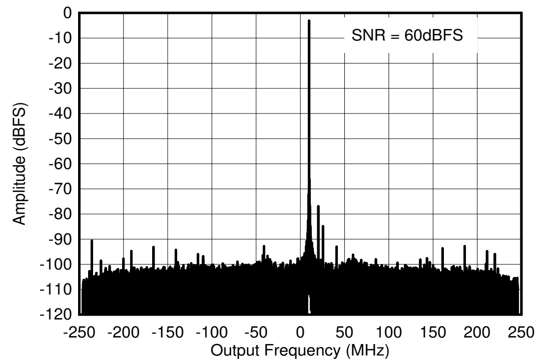
4.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



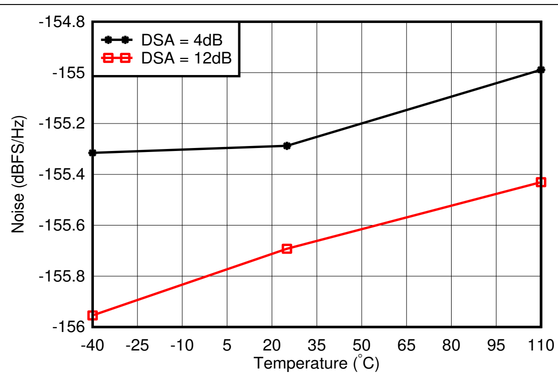
With 4.9GHz matching
Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

Figure 4-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9GHz



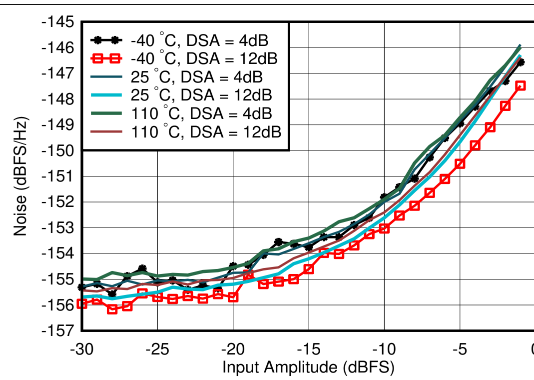
With 4.9GHz matching, f_{IN} = 4910MHz, A_{IN}= –3dBFS

Figure 4-184. RX Output FFT at 4.9GHz



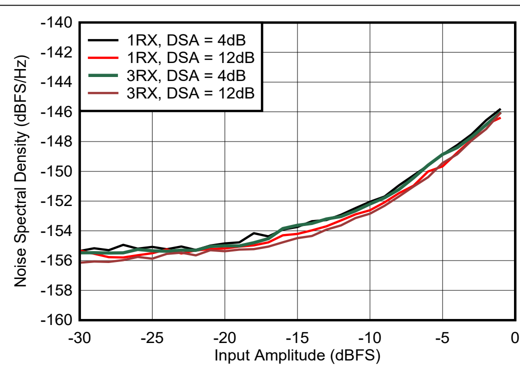
With 4.9GHz matching, 12.5MHz offset from tone

Figure 4-185. RX Noise Spectral Density vs Temperature at 4.9GHz



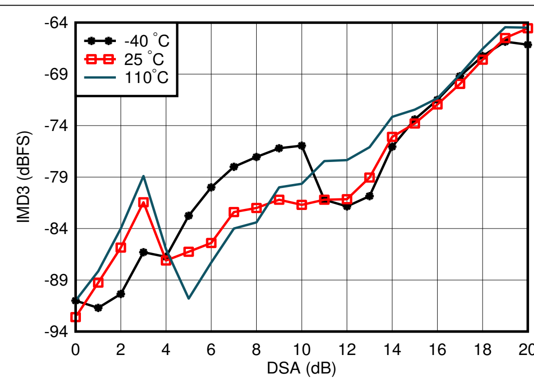
With 4.9GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

Figure 4-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9GHz



With 4.9GHz matching, 12.5MHz offset from tone

Figure 4-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9GHz

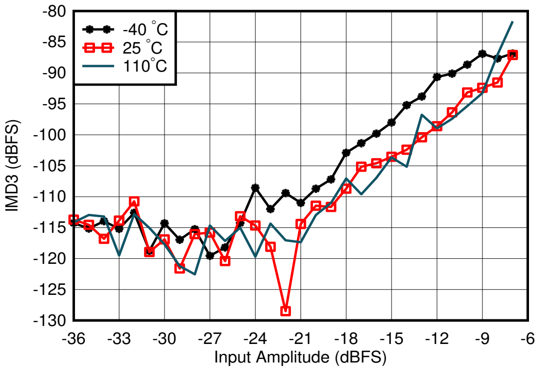


With 4.9GHz matching, each tone –7dBFS, tone spacing = 20MHz

Figure 4-188. RX IMD3 vs DSA Setting and Temperature at 4.9GHz

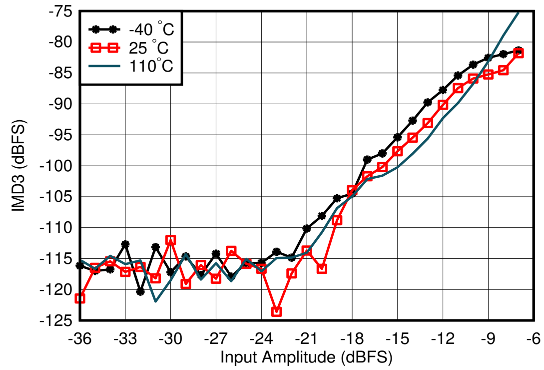
4.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



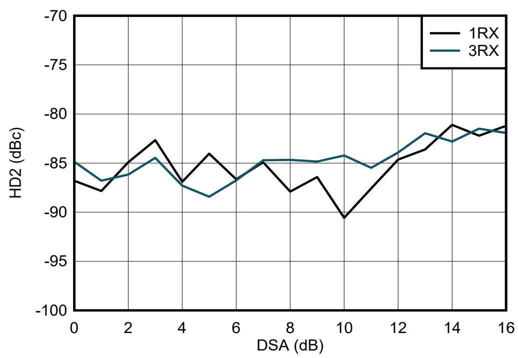
With 4.9GHz matching, tone spacing = 20MHz, DSA = 4dB

Figure 4-189. RX IMD3 vs Input Level and Temperature at 4.9GHz



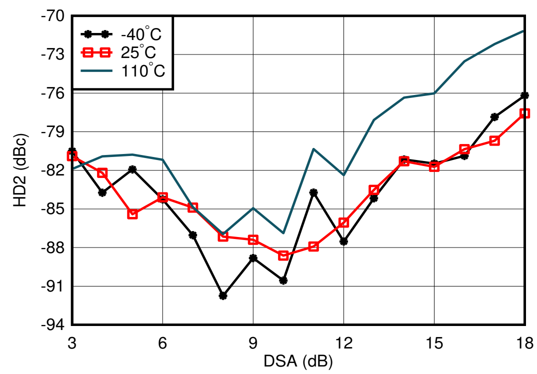
With 4.9GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-190. RX IMD3 vs Input Level and Temperature at 4.9GHz



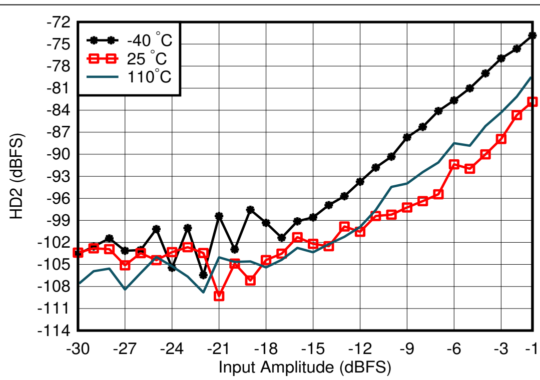
With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-191. RX HD2 vs DSA Setting and Channel at 4.9GHz



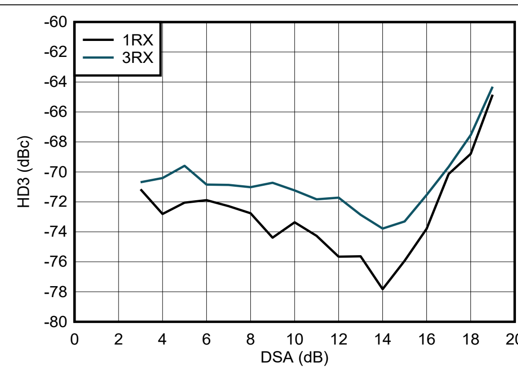
With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-192. RX HD2 vs DSA and Temperature at 4.9GHz



With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-193. RX HD2 vs Input Level and Temperature at 4.9GHz

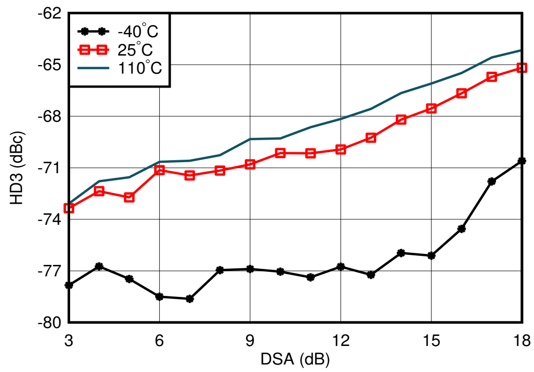


With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-194. RX HD3 vs DSA Setting and Channel at 4.9GHz

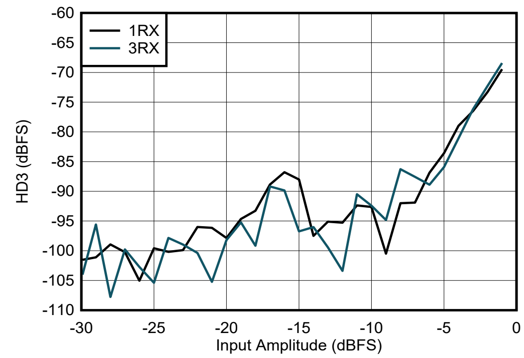
4.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.



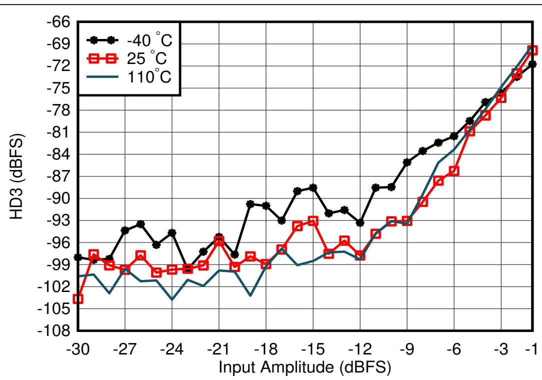
With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-195. RX HD3 vs DSA Setting and Temperature at 4.9GHz



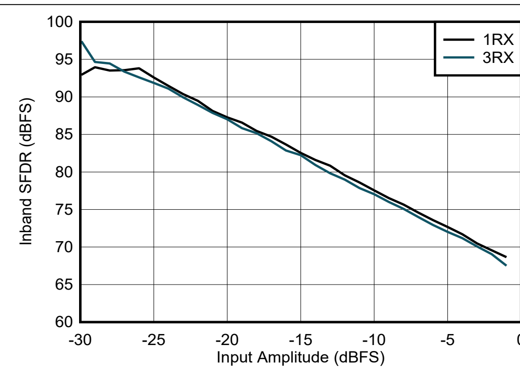
With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-196. RX HD3 vs Input Level and Channel at 4.9GHz



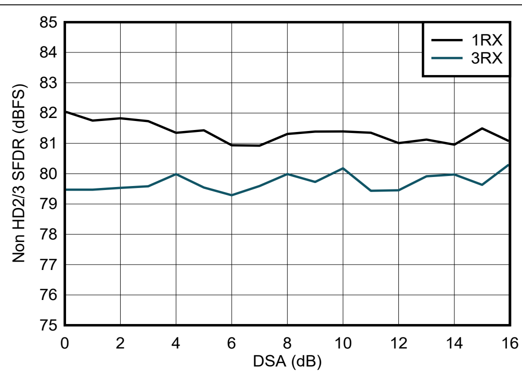
With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-197. RX HD3 vs Input Level and Temperature at 4.9GHz



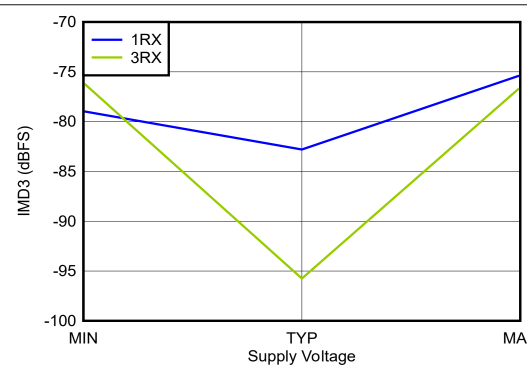
With 4.9GHz matching, decimate by 3

Figure 4-198. RX In-Band SFDR (±400MHz) vs Input Amplitude and Channel at 4.9GHz



With 4.9GHz matching

Figure 4-199. RX Non-HD2/3 vs DSA Setting at 4.9GHz

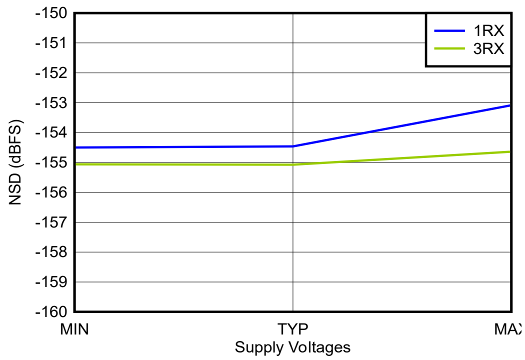


With 4.9GHz matching, –7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-200. RX IMD3 vs Supply and Channel at 4.9GHz

4.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3dBFS, DSA setting = 4dB.

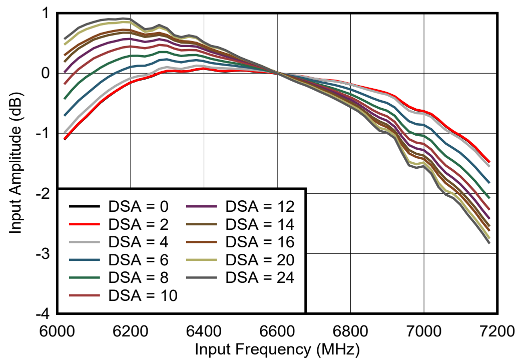


With 4.9GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-201. RX Noise Spectral Density vs Supply and Channel at 4.9GHz

4.12.7 RX Typical Characteristics 6.8GHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500MSPS (decimate by 6x), External clock mode , A_{IN} = –3dBFS, DSA setting = 3dB.



Normalized to 6.6GHz

Figure 4-202. RX In-Band Gain Flatness

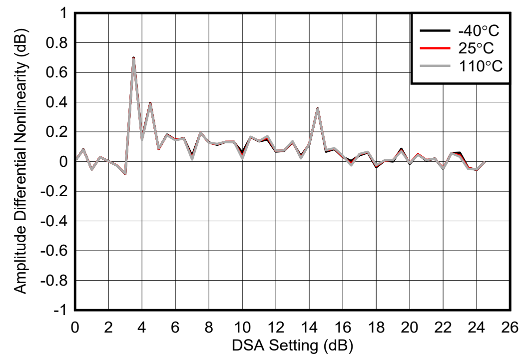
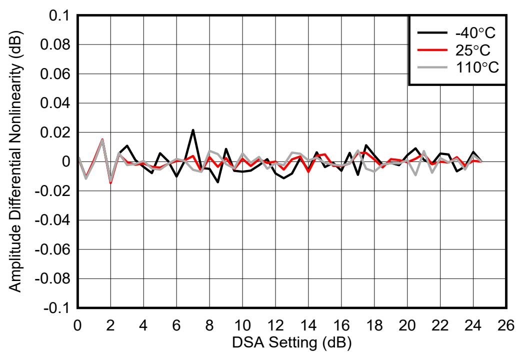


Figure 4-203. RX Uncalibrated Differential Amplitude Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

Figure 4-204. RX Calibrated Differential Amplitude Error at 6.851GHz

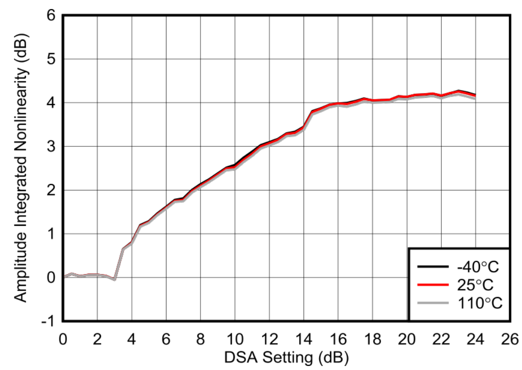
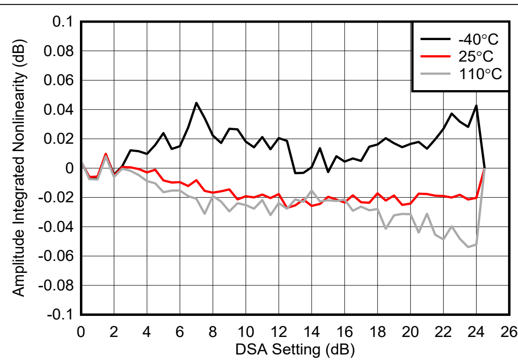


Figure 4-205. RX Uncalibrated Integrated Amplitude Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

Figure 4-206. RX Calibrated Integrated Amplitude Error at 6.851GHz

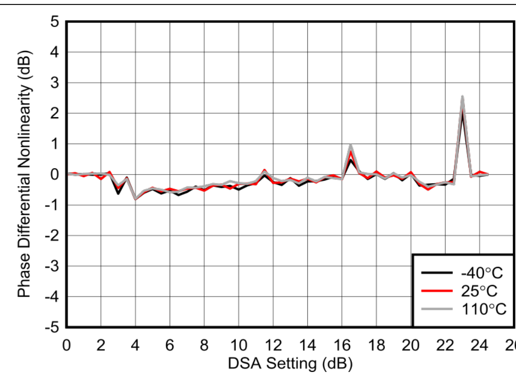
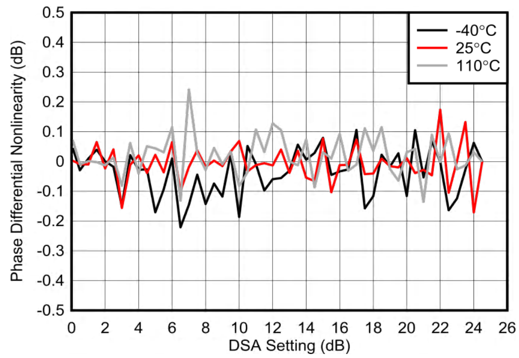


Figure 4-207. RX Uncalibrated Differential Phase Error at 6.851GHz

4.12.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500MSPS (decimate by 6x), External clock mode , A_{IN} = –3dBFS, DSA setting = 3dB.



Calibrated at 25°C, held at -40 and 110°C

Figure 4-208. RX Calibrated Differential Phase Error at 6.851GHz

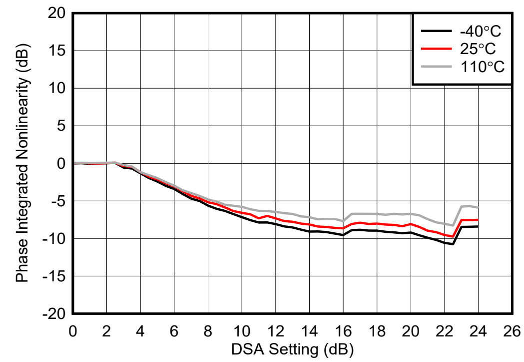
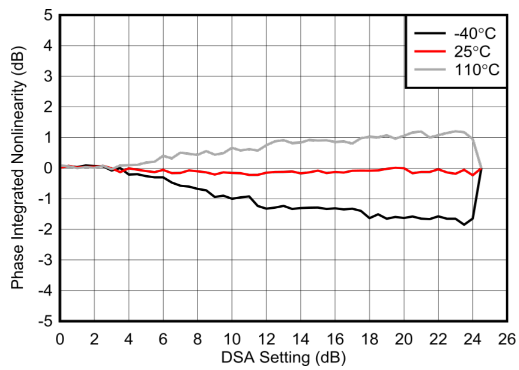
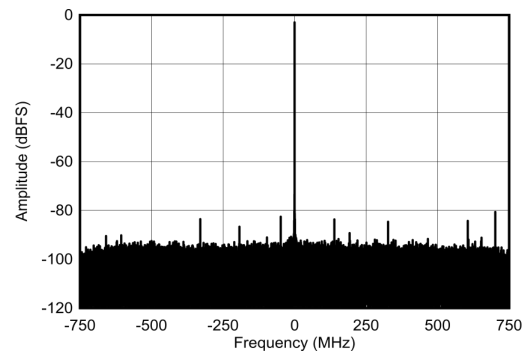


Figure 4-209. RX Uncalibrated Integrated Phase Error at 6.851GHz



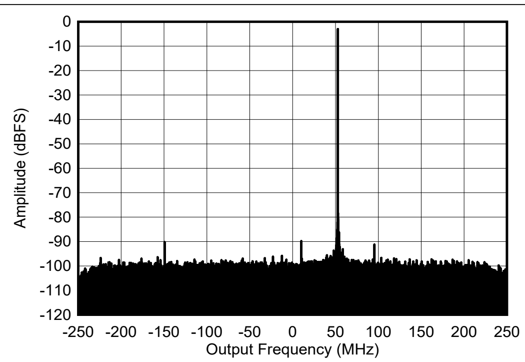
Calibrated at 25°C, held at -40 and 110°C

Figure 4-210. RX Calibrated Integrated Phase Error at 6.851GHz



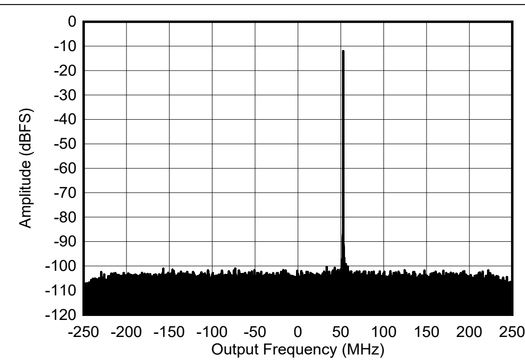
F_{IN} = 6.851GHz, F_{NCO} = 6.85GHz

Figure 4-211. RX Output FFT at 6.851GHz and -3 dBFS



F_{IN} = 6.851GHz, F_{NCO} = 6.85GHz

Figure 4-212. RX Output FFT at 6.851GHz and -6dBFS



F_{IN} = 6.851GHz, F_{NCO} = 6.85GHz

Figure 4-213. RX Output FFT at 6.851GHz and -12 dBFS

4.12.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500MSPS (decimate by 6x), External clock mode , A_{IN} = –3dBFS, DSA setting = 3dB.

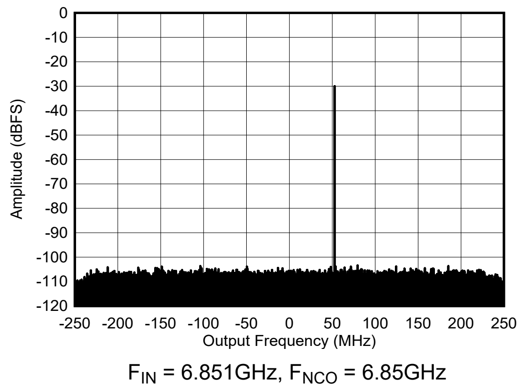


Figure 4-214. RX Output FFT at 6.851GHz and -30 dBFS

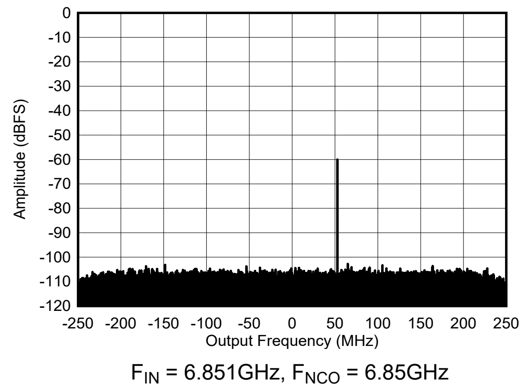


Figure 4-215. RX Output FFT at 6.851GHz and -60 dBFS

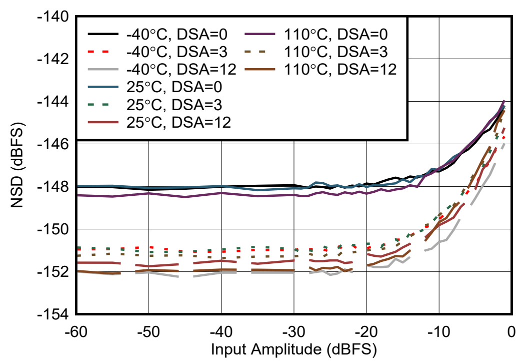


Figure 4-216. RX NSD vs Input Amplitude at 6.851GHz

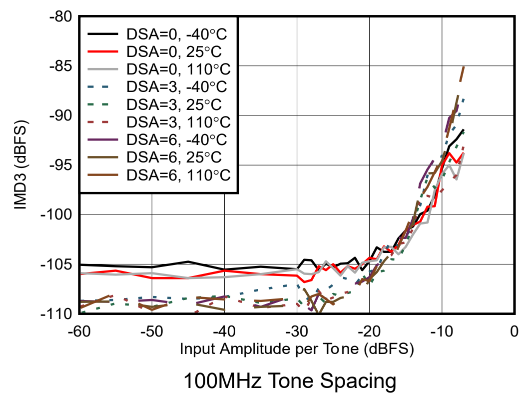


Figure 4-217. RX IMD3 vs Input Amplitude at 6.851GHz

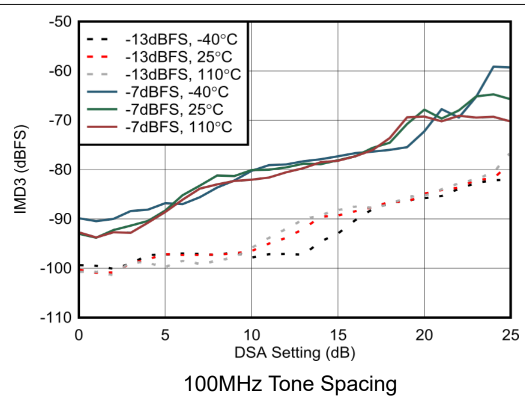


Figure 4-218. RX IMD3 vs DSA Setting at 6.851GHz

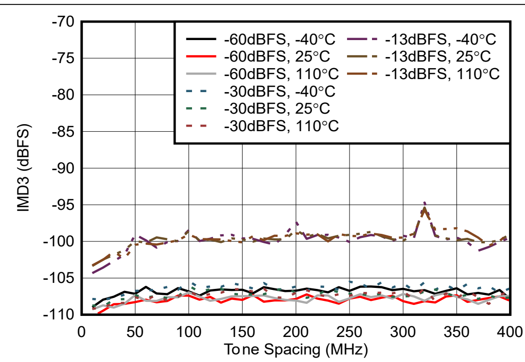


Figure 4-219. RX IMD3 vs Tone Spacing at 6.851GHz

4.12.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 500MSPS (decimate by 6x), External clock mode , A_{IN} = –3dBFS, DSA setting = 3dB.

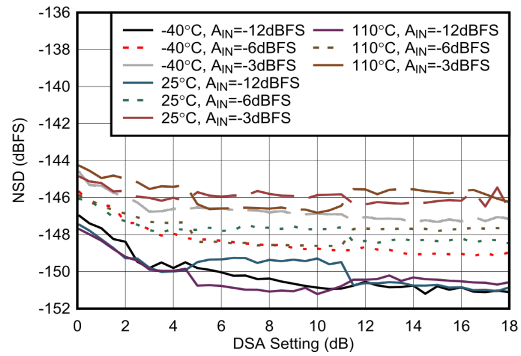
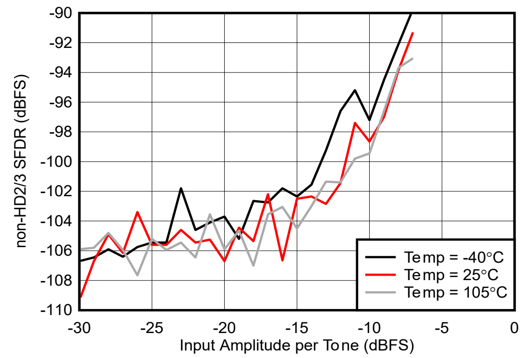


Figure 4-220. RX NSD vs DSA Setting at 6.851GHz



50MHz tone spacing, excluding 3rd order distortion

Figure 4-221. RX 2-tone SFDR vs Input Amplitude at 6.85GHz

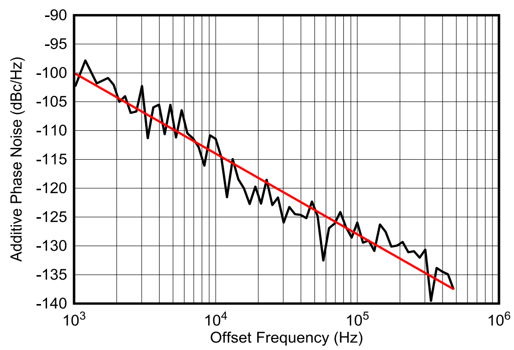
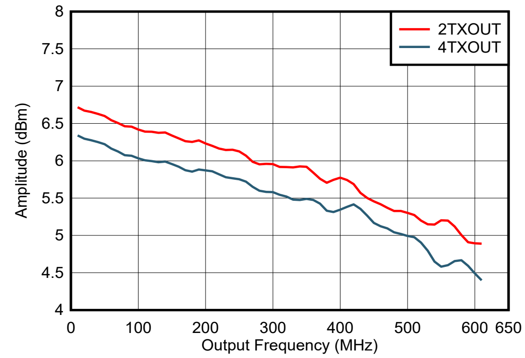


Figure 4-222. RX Additive Phase Noise at 6.85GHz

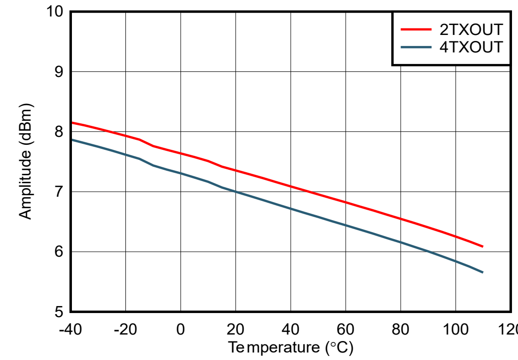
4.12.8 TX Typical Characteristics at 30MHz and 600MHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



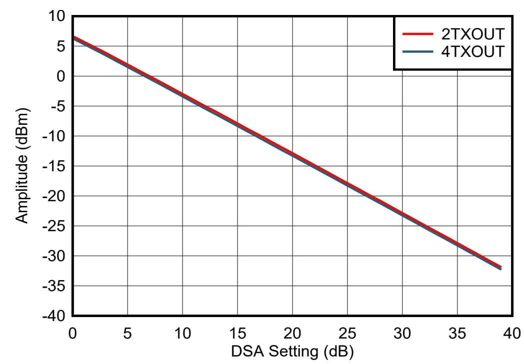
including PCB and cable losses

Figure 4-223. TX Output Fullscale vs Output Frequency: 5MHz - 600MHz



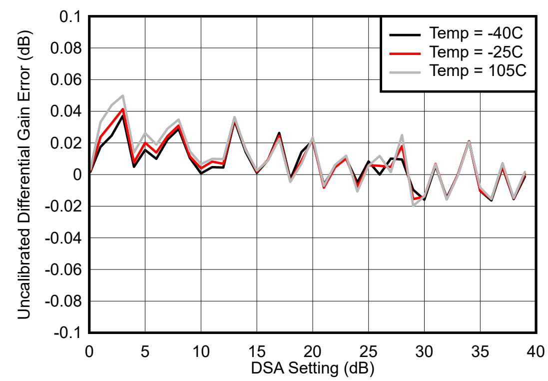
including PCB and cable losses

Figure 4-224. TX Output Fullscale vs Temperature at 30MHz



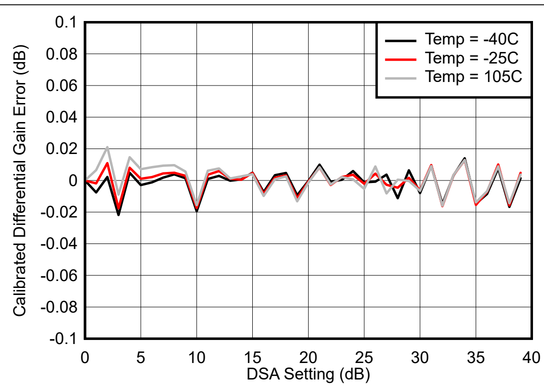
including PCB and cable losses

Figure 4-225. TX Output Fullscale vs DSA Setting at 30MHz



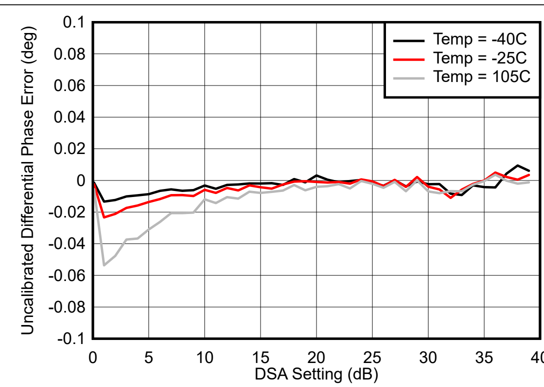
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-226. Uncalibrated TX Differential Gain Error (DNL) at 30MHz



Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-227. Calibrated TX Differential Gain Error (DNL) at 30MHz

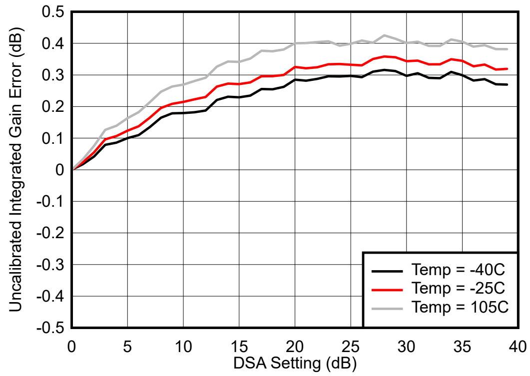


Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-228. Calibrated TX Differential Gain Error (DNL) at 30MHz

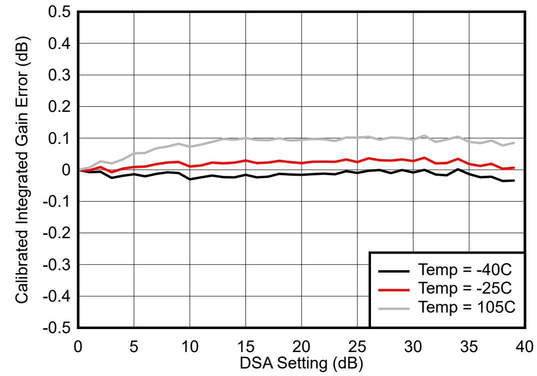
4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



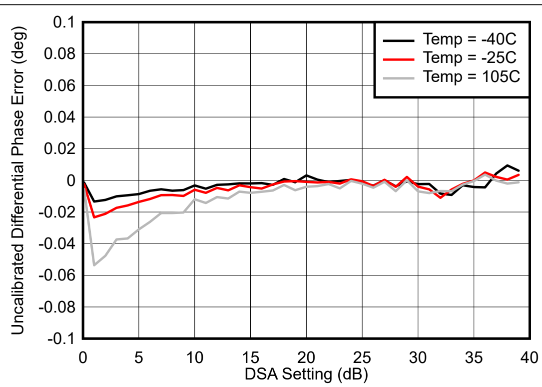
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 4-229. Uncalibrated TX Integrated Gain Error (INL) at 30MHz



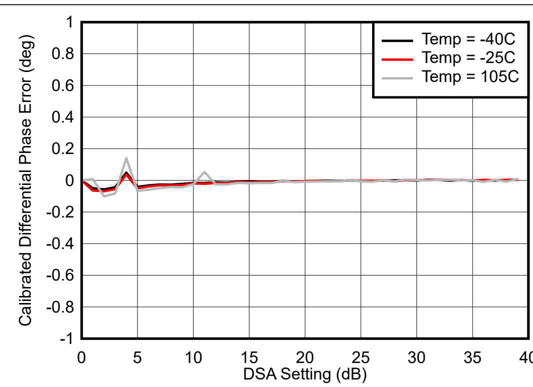
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 4-230. Calibrated TX Integrated Gain Error (INL) at 30MHz



Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-231. Uncalibrated TX Differential Phase Error (DNL) at 30MHz

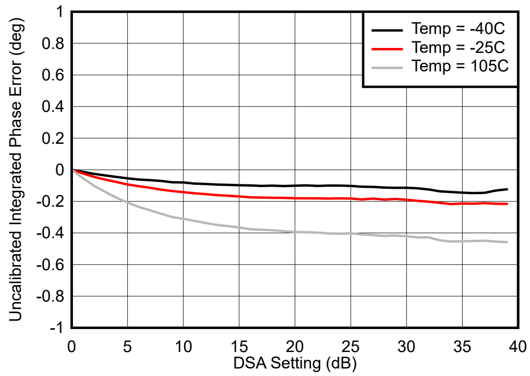


Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-232. Calibrated TX Differential Phase Error (DNL) at 30MHz

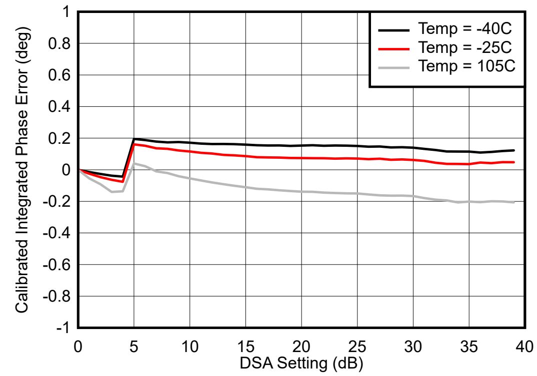
4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 4-233. Uncalibrated TX Integrated Phase Error (INL) at 30MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 4-234. Calibrated TX Integrated Phase Error (INL) at 30MHz

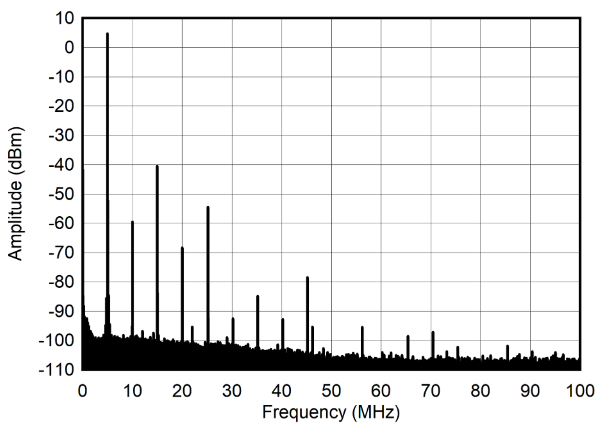


Figure 4-235. Single Tone Spectrum at 5MHz and -1dBFS (0 - 100MHz)

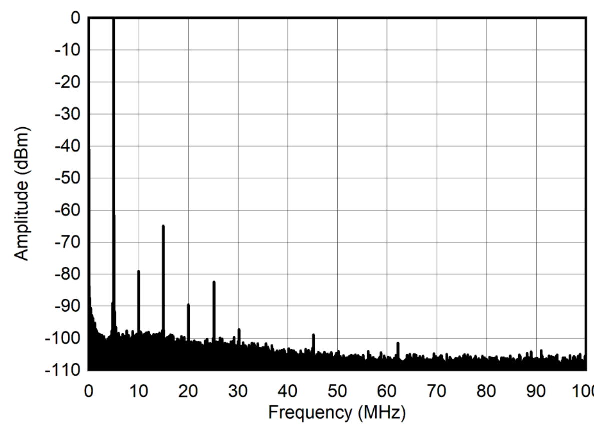


Figure 4-236. Single Tone Spectrum at 5MHz and -6d BFS (0 - 100MHz)

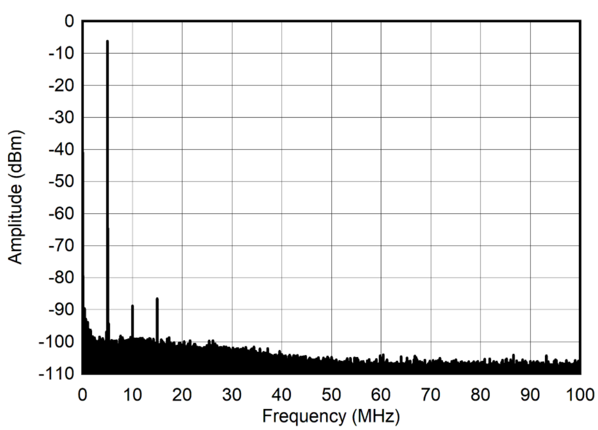


Figure 4-237. Single Tone Spectrum at 5MHz and -12dBFS (0 - 100MHz)

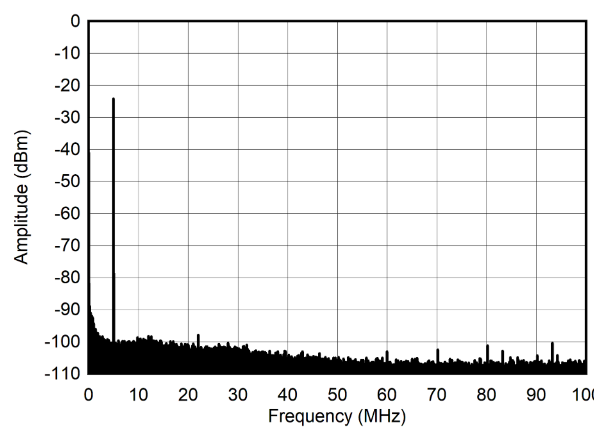


Figure 4-238. Single Tone Spectrum at 5MHz and -30dBFS (0 - 100MHz)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

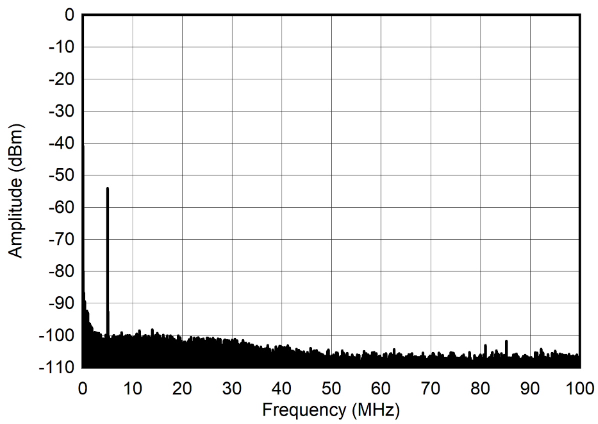


Figure 4-239. Single Tone Spectrum at 5MHz and -60dBFS (0 - 100MHz)

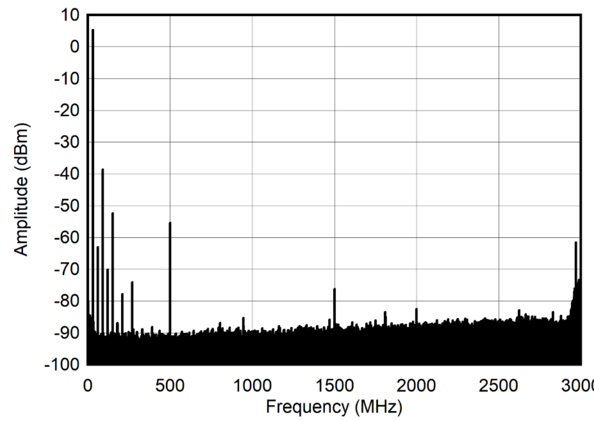


Figure 4-240. Single Tone Spectrum at 30MHz and -1dBFS (Nyquist)

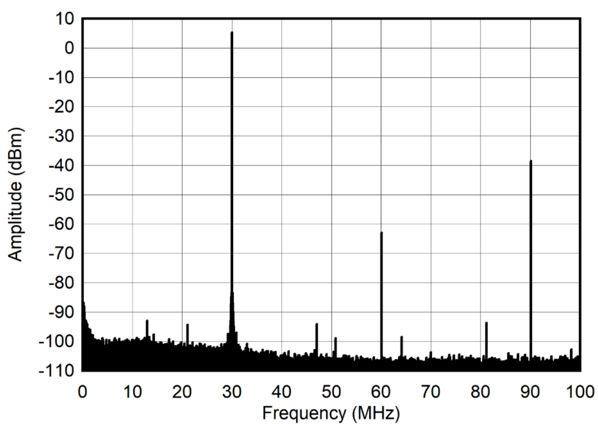


Figure 4-241. Single Tone Spectrum at 30MHz and -1dBFS (0 - 100MHz)

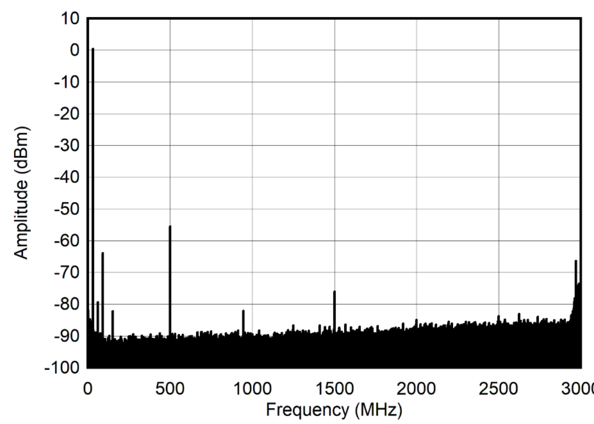


Figure 4-242. Single Tone Spectrum at 30MHz and -6dBFS (Nyquist)

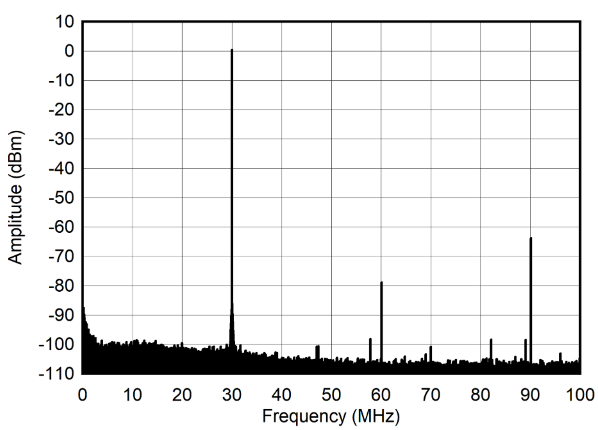


Figure 4-243. Single Tone Spectrum at 30MHz and -6dBFS (0 - 100MHz)

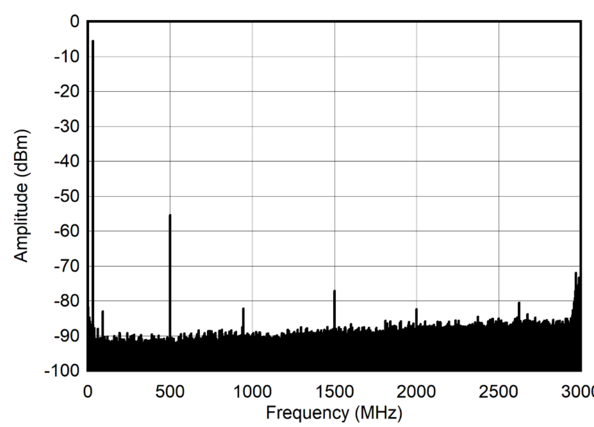


Figure 4-244. Single Tone Spectrum at 30MHz and -12dBFS (Nyquist)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

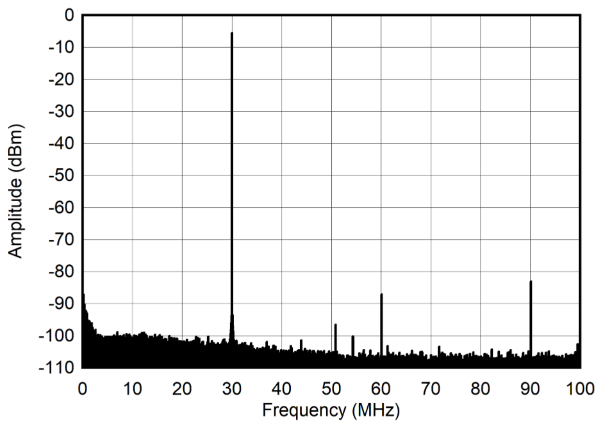


Figure 4-245. Single Tone Spectrum at 30MHz and -12dBFS (0 - 100MHz)

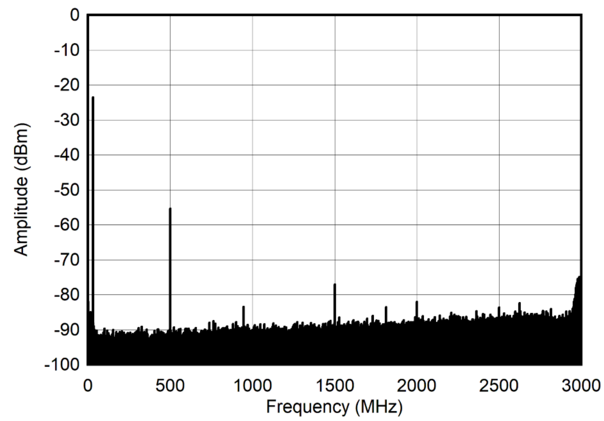


Figure 4-246. Single Tone Spectrum at 30MHz and -30dBFS (Nyquist)

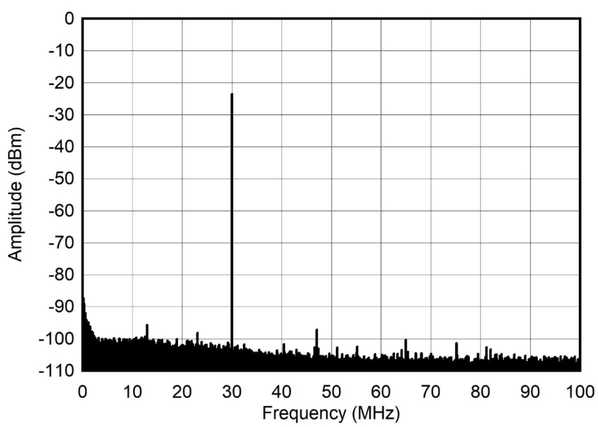


Figure 4-247. Single Tone Spectrum at 30MHz and -30dBFS (0 - 100MHz)

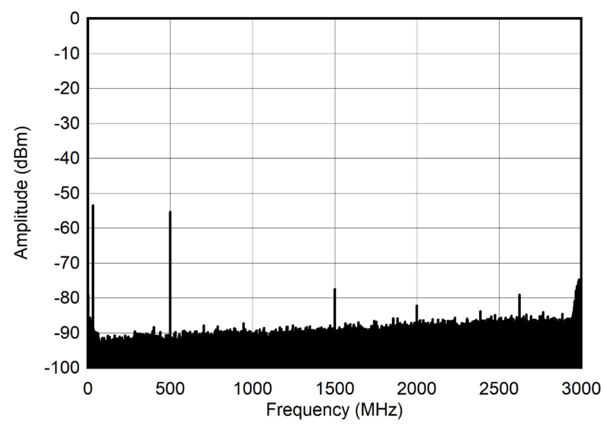


Figure 4-248. Single Tone Spectrum at 30MHz and -60dBFS (Nyquist)

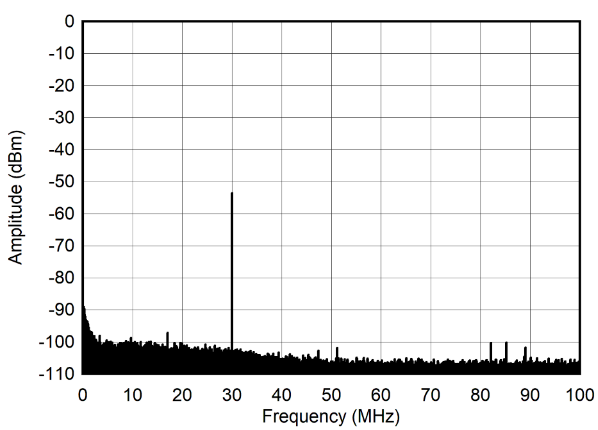


Figure 4-249. Single Tone Spectrum at 30MHz and -60dBFS (0 - 100MHz)

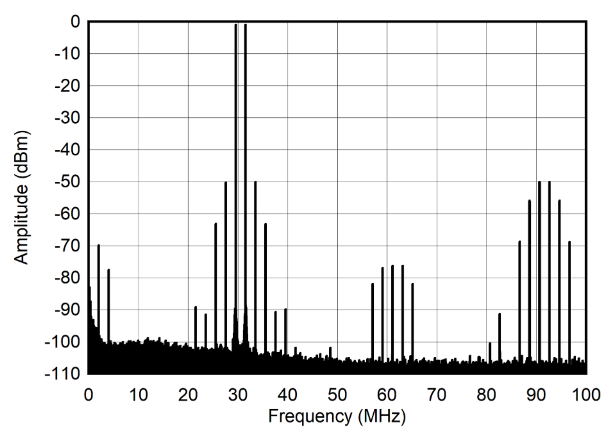


Figure 4-250. Dual Tone Spectrum at 30MHz and -7dBFS (0 - 100MHz)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

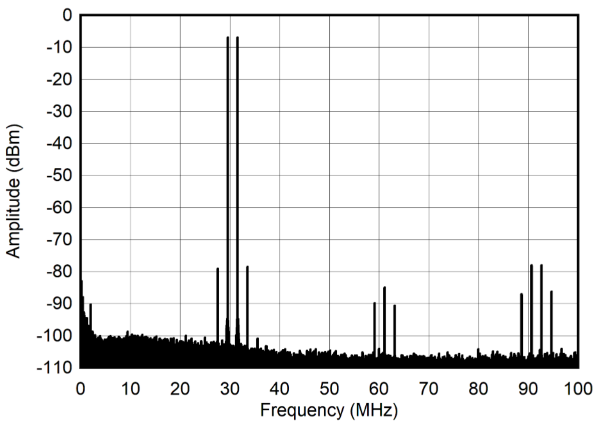


Figure 4-251. Dual Tone Spectrum at 30MHz and -13dBFS (0 - 100MHz)

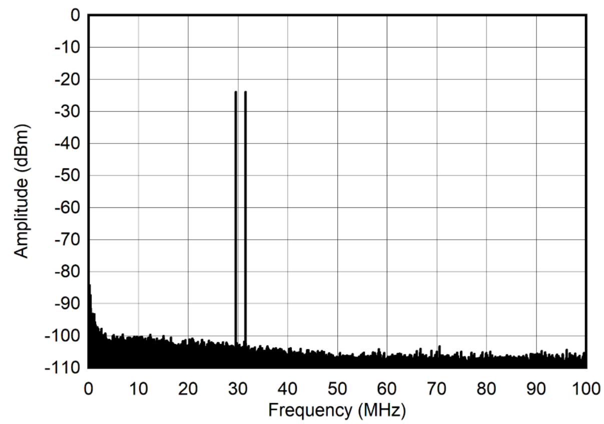


Figure 4-252. Dual Tone Spectrum at 30MHz and -30dBFS (0 - 100MHz)

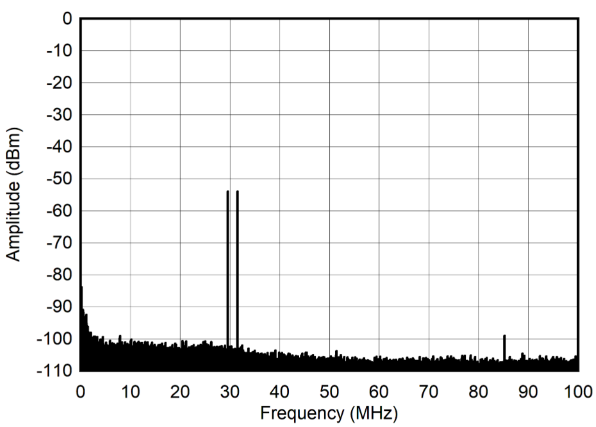
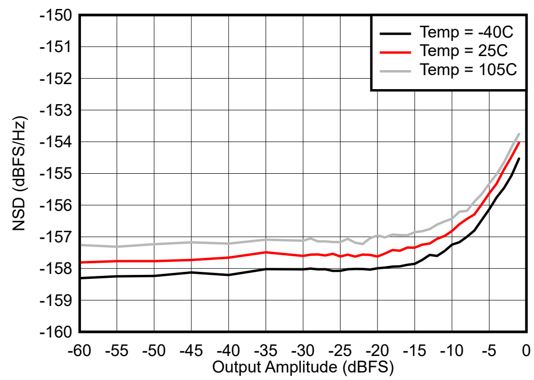
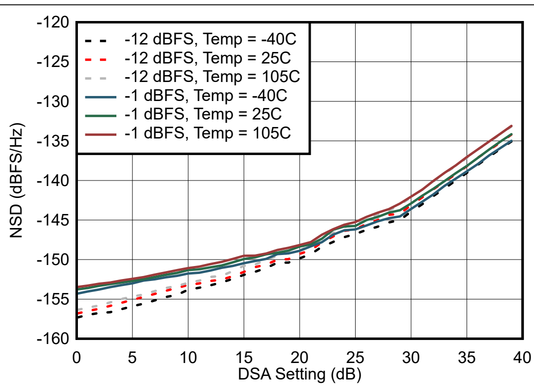


Figure 4-253. Dual Tone Spectrum at 30MHz and -60d BFS (0 - 100MHz)



measured at +50MHz offset

Figure 4-254. Noise Spectral Density vs Digital Amplitude at 30MHz



measured at +50MHz offset

Figure 4-255. Noise Spectral Density vs DSA Setting at 30MHz

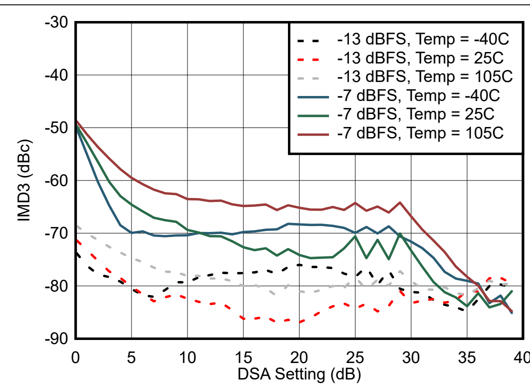


Figure 4-256. IMD3 vs DSA Setting at 30MHz

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

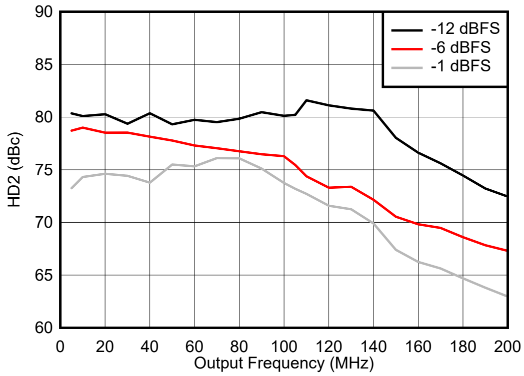


Figure 4-257. HD2 vs Frequency 0 - 200MHz

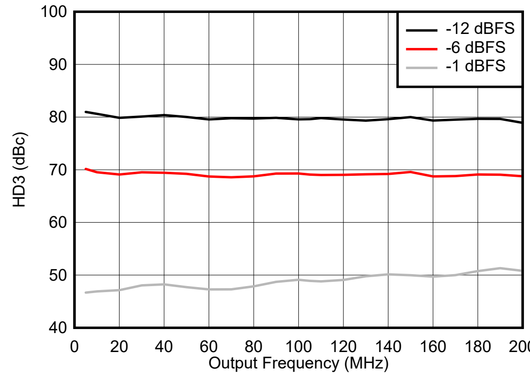
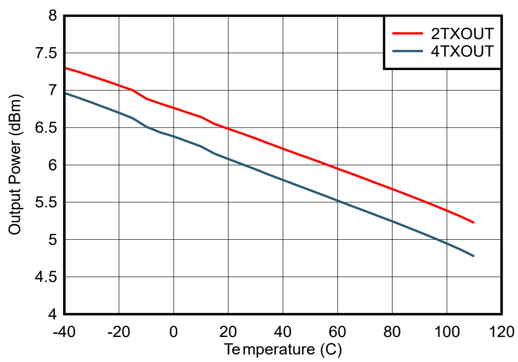
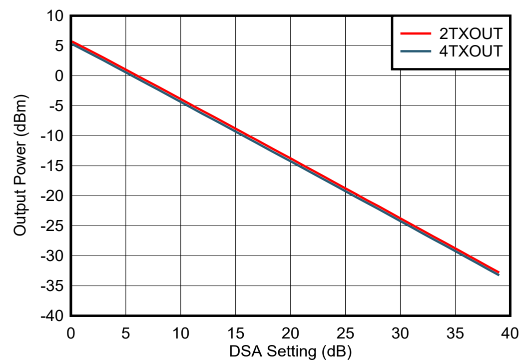


Figure 4-258. HD3 vs Frequency 0 - 200MHz



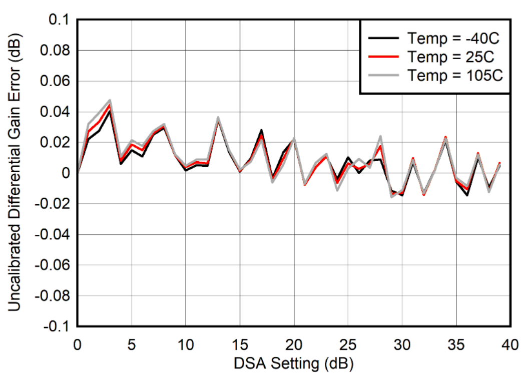
including PCB and cable losses

Figure 4-259. TX Output Fullscale vs Temperature at 400MHz



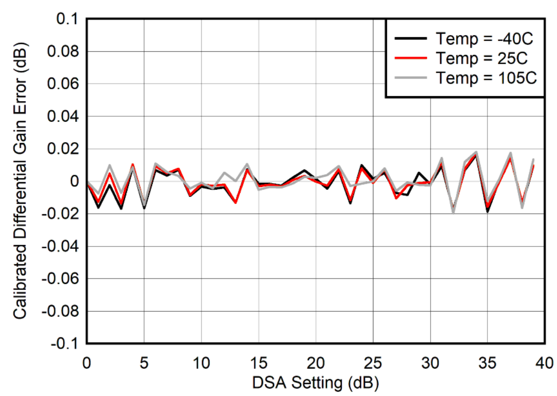
including PCB and cable losses

Figure 4-260. TX Output Fullscale vs DSA Setting at 400MHz



Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-261. Uncalibrated TX Differential Gain Error (DNL) at 400MHz

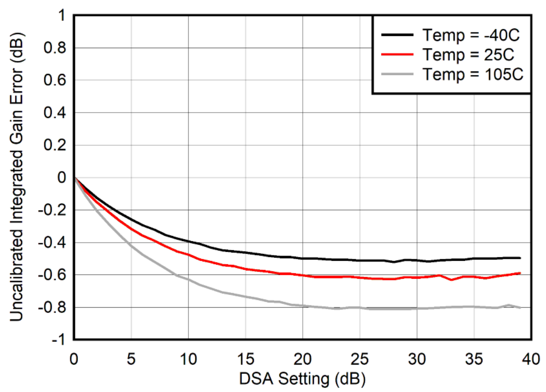


Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-262. Calibrated TX Differential Gain Error (DNL) at 400MHz

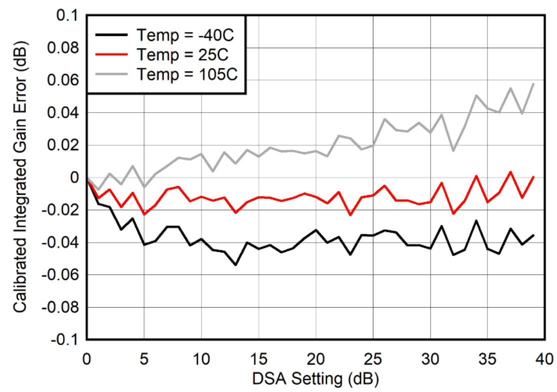
4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



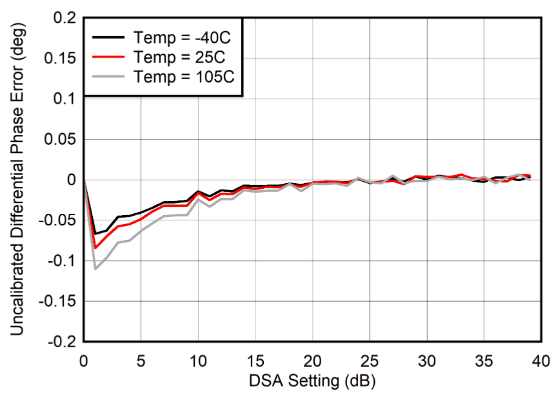
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 4-263. Uncalibrated TX Integrated Gain Error (INL) at 400MHz



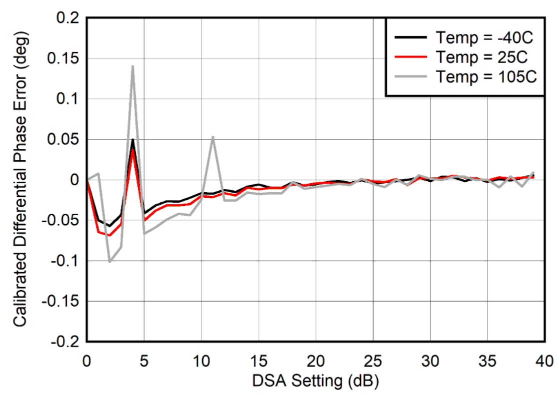
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

Figure 4-264. Calibrated TX Integrated Gain Error (INL) at 400MHz



Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-265. Uncalibrated TX Differential Phase Error (DNL) at 400MHz

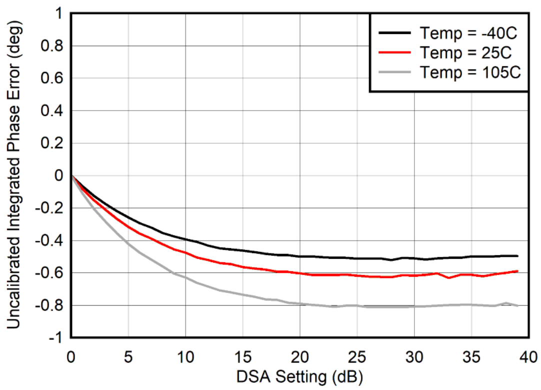


Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-266. Calibrated TX Differential Phase Error (DNL) at 400MHz

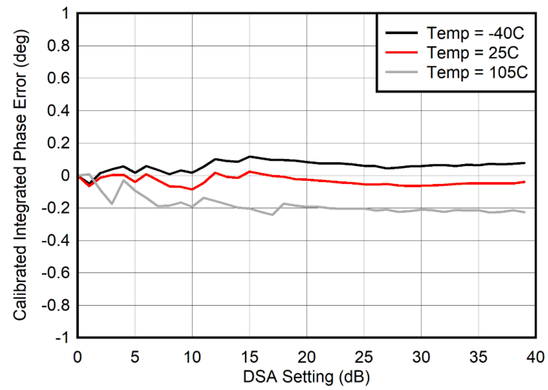
4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 4-267. Uncalibrated TX Integrated Phase Error (INL) at 400MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

Figure 4-268. Calibrated TX Integrated Phase Error (INL) at 400MHz

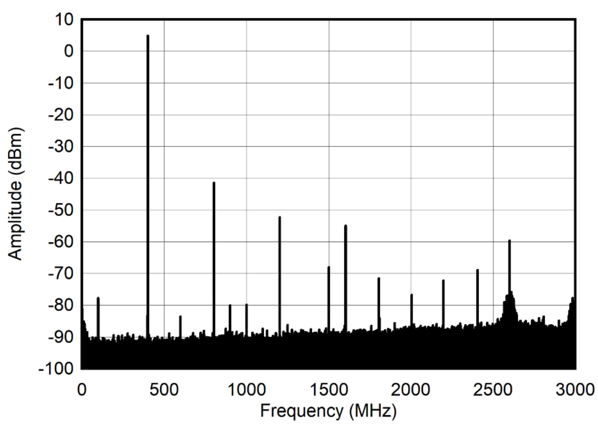


Figure 4-269. Single Tone Spectrum at 400MHz and -1dBFS (Nyquist)

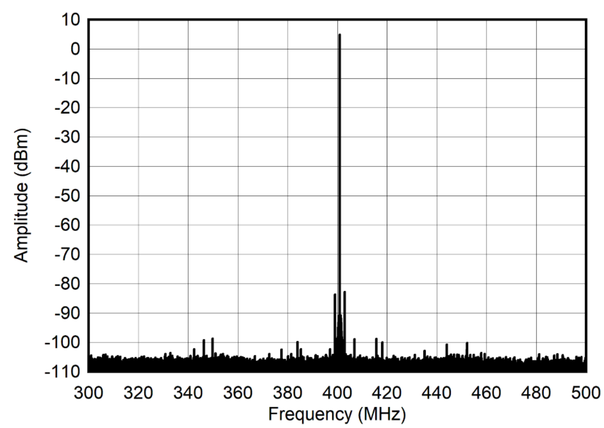


Figure 4-270. Single Tone Spectrum at 400MHz and -1dBFS (±100MHz)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

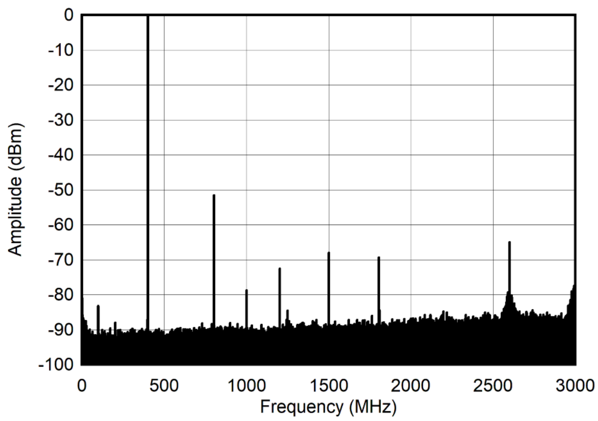


Figure 4-271. Single Tone Spectrum at 400MHz and -6dBFS (Nyquist)

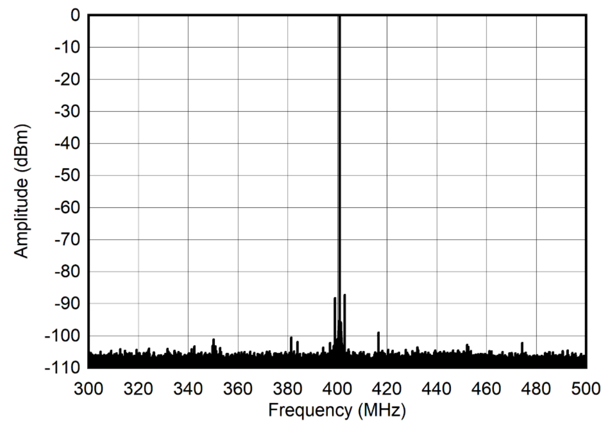


Figure 4-272. Single Tone Spectrum at 400MHz and -6dBFS (±100MHz)

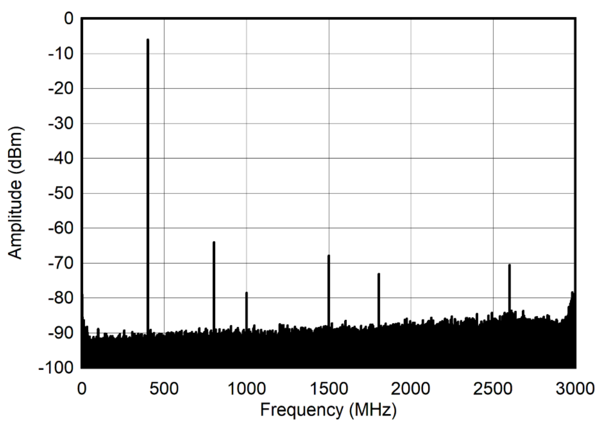


Figure 4-273. Single Tone Spectrum at 400MHz and -12dBFS (Nyquist)

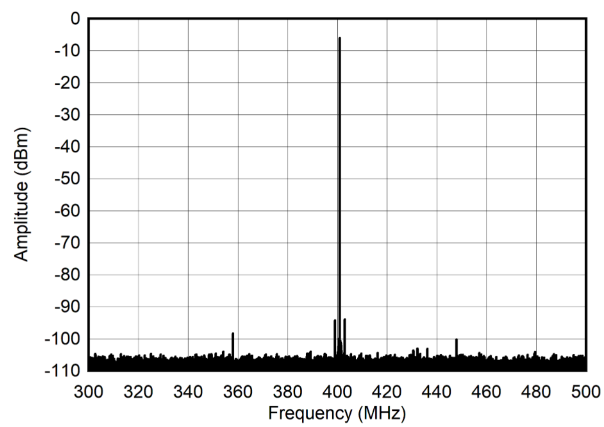


Figure 4-274. Single Tone Spectrum at 400MHz and -12dBFS (±100MHz)

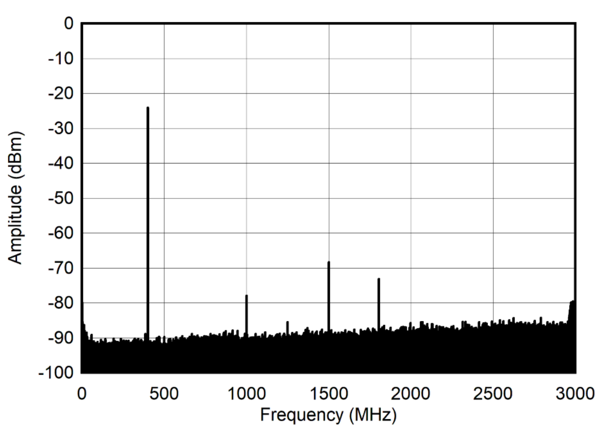


Figure 4-275. Single Tone Spectrum at 400MHz and -30dBFS (Nyquist)

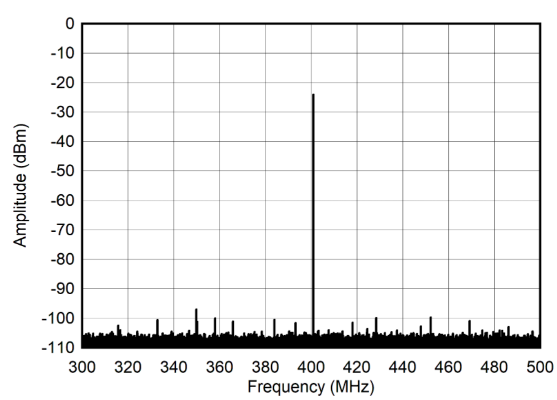


Figure 4-276. Single Tone Spectrum at 400MHz and -30dBFS (±100MHz)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1^{st} Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

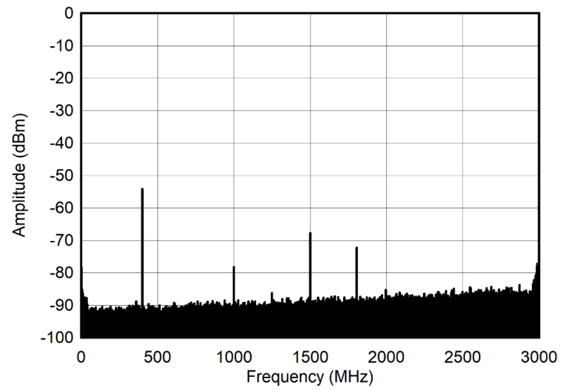


Figure 4-277. Single Tone Spectrum at 400MHz and -60dBFS (Nyquist)

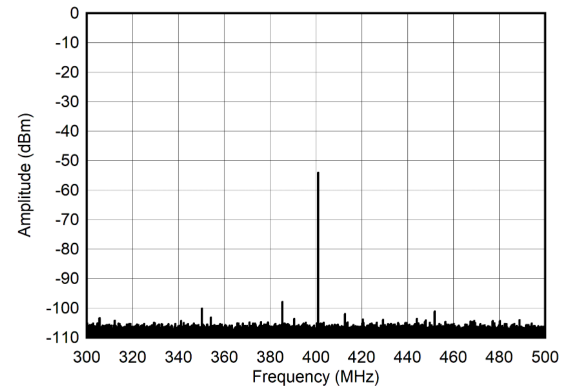
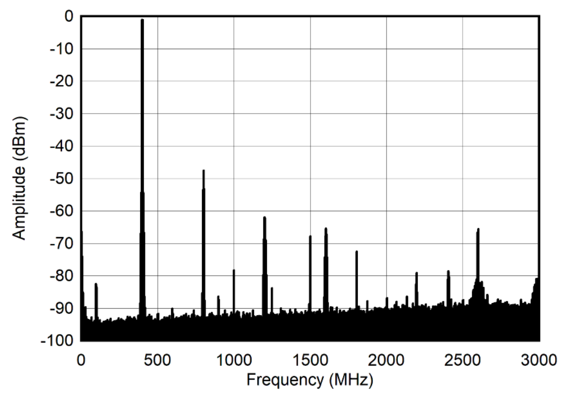
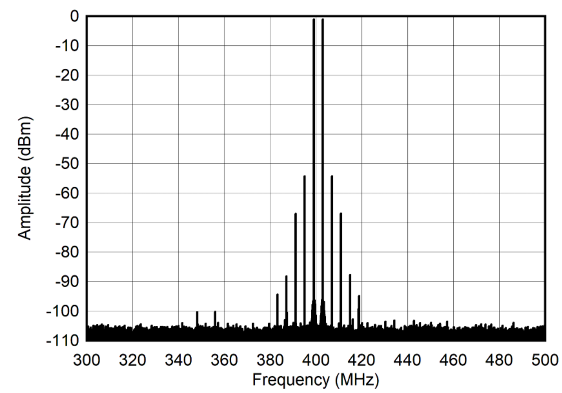


Figure 4-278. Single Tone Spectrum at 400MHz and -60dBFS (±100MHz)



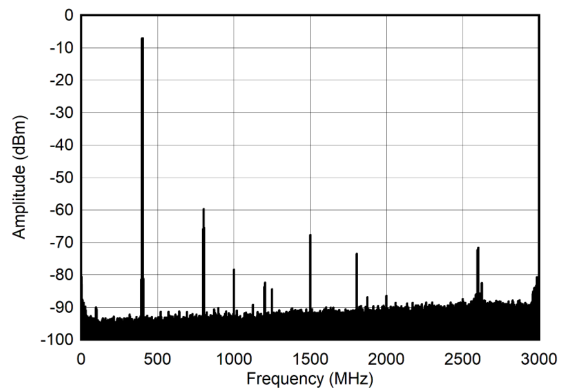
Tone Spacing = 4MHz

Figure 4-279. Dual Tone Spectrum at 400MHz and -7dBFS (Nyquist)



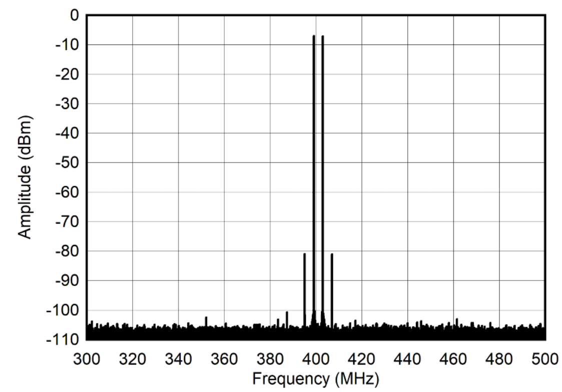
Tone Spacing = 4MHz

Figure 4-280. Dual Tone Spectrum at 400MHz and -7dBFS (±100MHz)



Tone Spacing = 4MHz

Figure 4-281. Dual Tone Spectrum at 400MHz and -13dBFS (Nyquist)



Tone Spacing = 4MHz

Figure 4-282. Dual Tone Spectrum at 400MHz and -13dBFS (±100MHz)

4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated

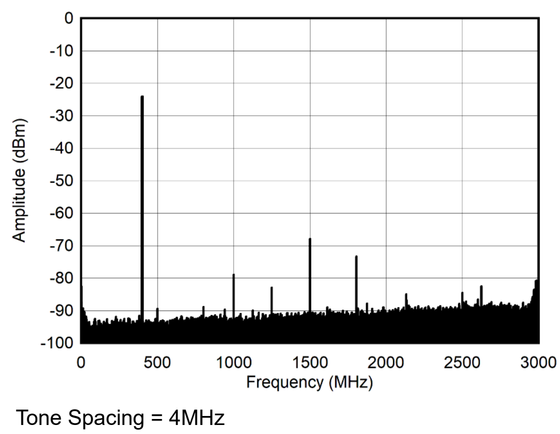


Figure 4-283. Dual Tone Spectrum at 400MHz and -30dBFS (Nyquist)

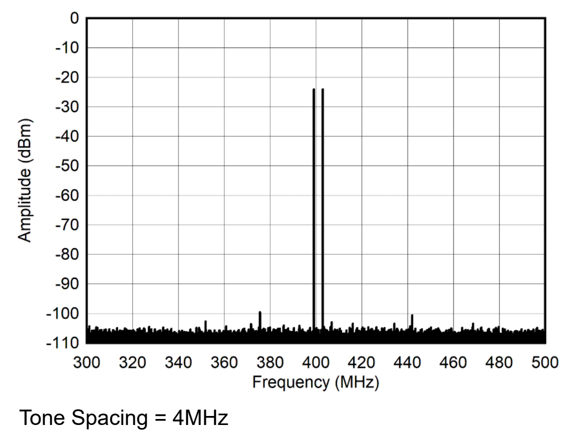


Figure 4-284. Dual Tone Spectrum at 400MHz and -30dBFS (±100MHz)

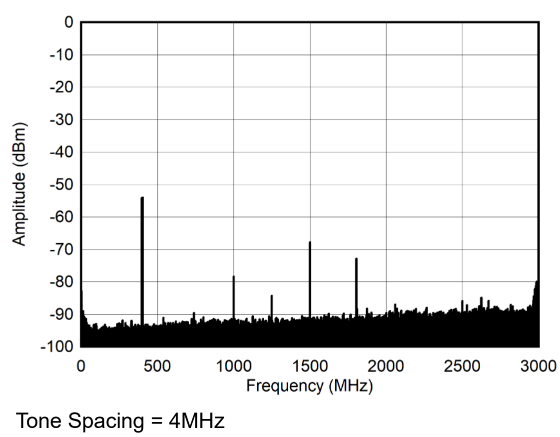


Figure 4-285. Dual Tone Spectrum at 400MHz and -60dBFS (Nyquist)

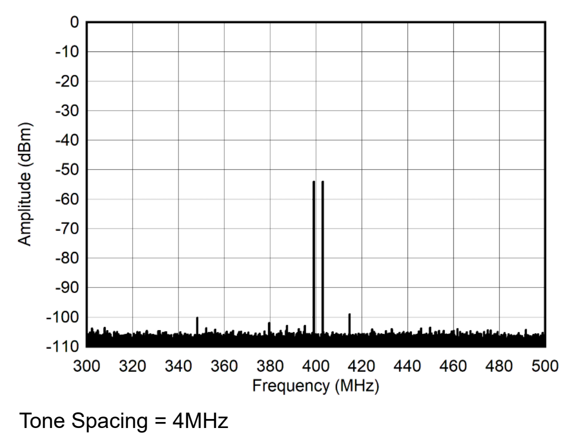
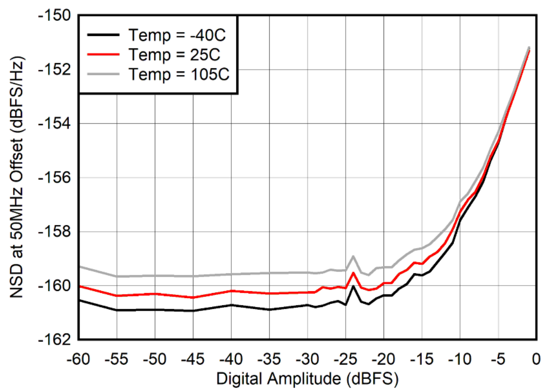


Figure 4-286. Dual Tone Spectrum at 400MHz and -60dBFS (±100MHz)

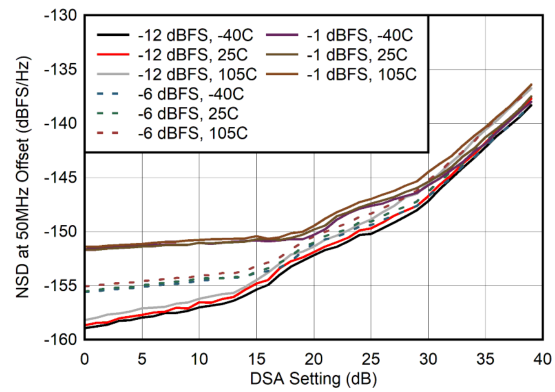
4.12.8 TX Typical Characteristics at 30MHz and 600MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125MSPS, f_{DAC} = 6000MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500MHz. Additional default conditions for all plots, A_{OUT} = –1dBFS, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



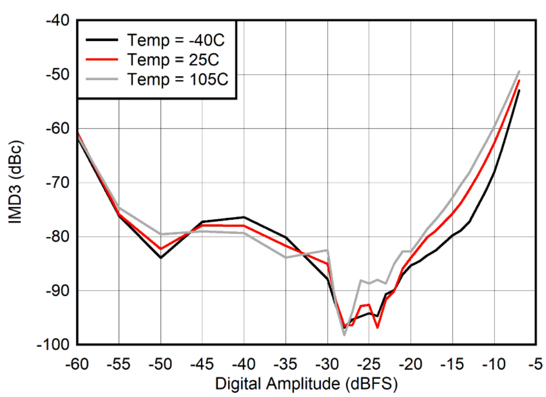
measured at 50MHz offset

Figure 4-287. Noise Spectral Density vs Digital Amplitude at 400MHz



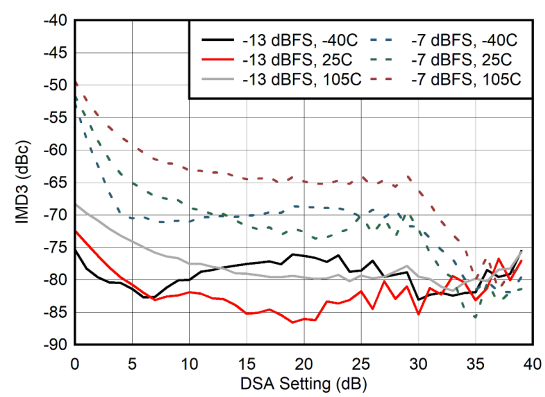
measured at 50MHz offset

Figure 4-288. Noise Spectral Density vs DSA Setting at 400MHz



Tone Spacing = 4MHz

Figure 4-289. IMD3 vs Digital Amplitude at 400MHz



Tone Spacing = 4MHz

Figure 4-290. IMD3 vs DSA Setting at 400MHz

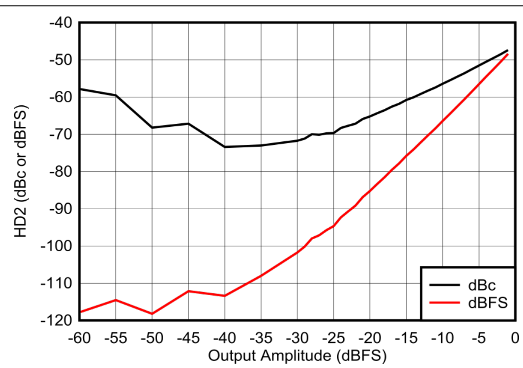


Figure 4-291. HD2 vs Amplitude at 400MHz

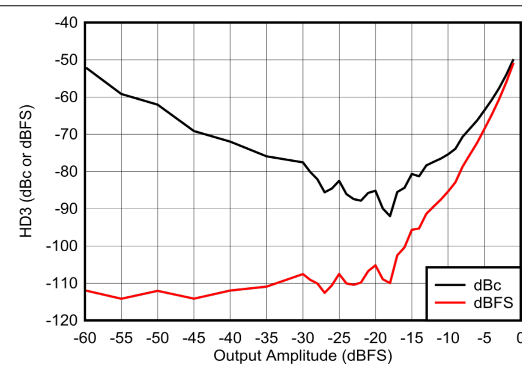
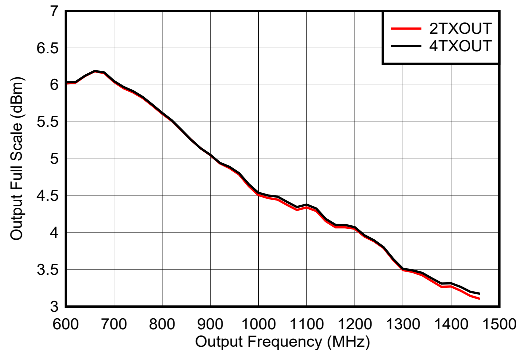


Figure 4-292. HD3 vs Amplitude at 400MHz

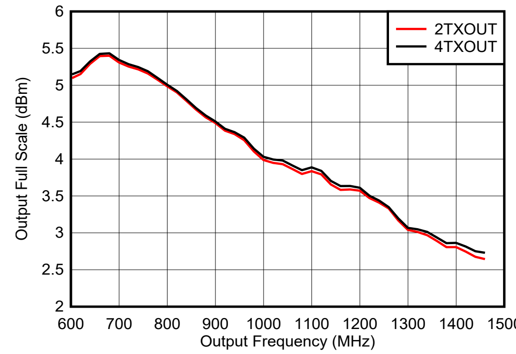
4.12.9 TX Typical Characteristics at 800MHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



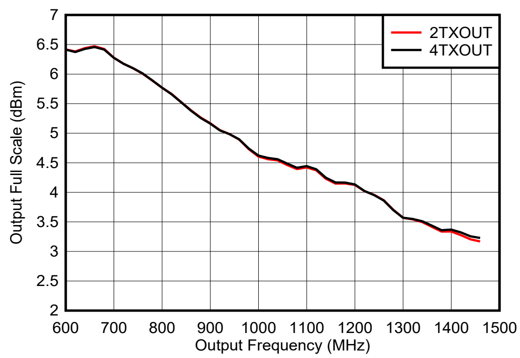
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-293. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode



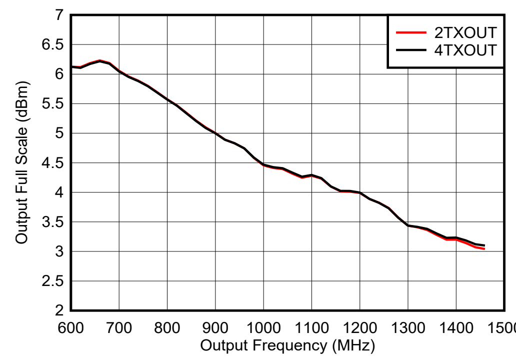
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-294. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode



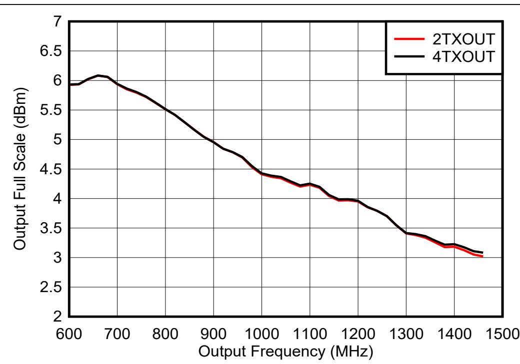
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-295. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode



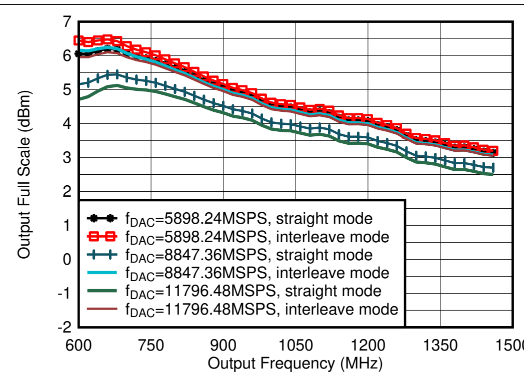
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-296. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode



Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-297. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS, Interleave Mode

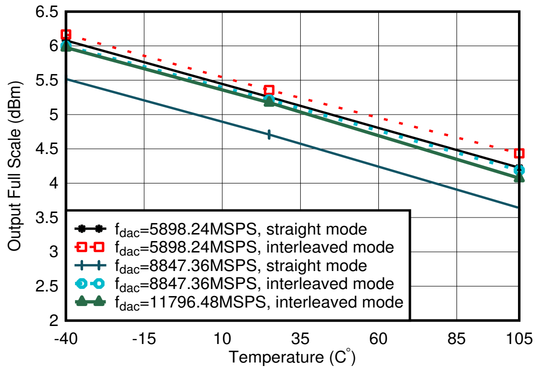


including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-298. TX Output Fullscale vs Output Frequency

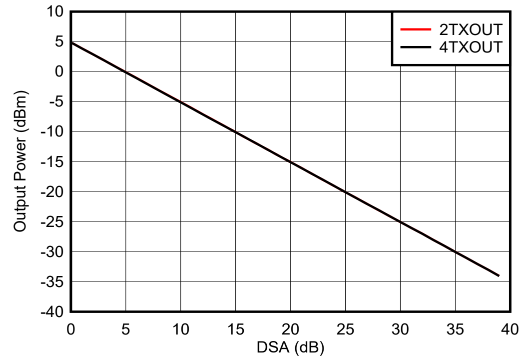
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



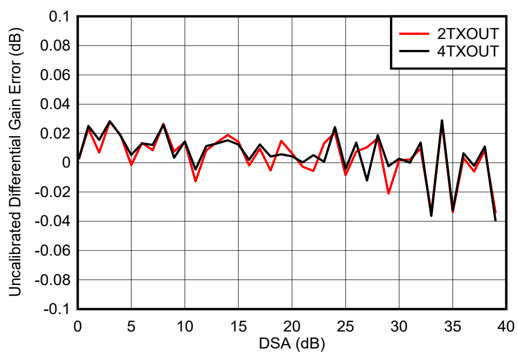
including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 0.8GHz matching

Figure 4-299. TX Output Fullscale vs Temperature



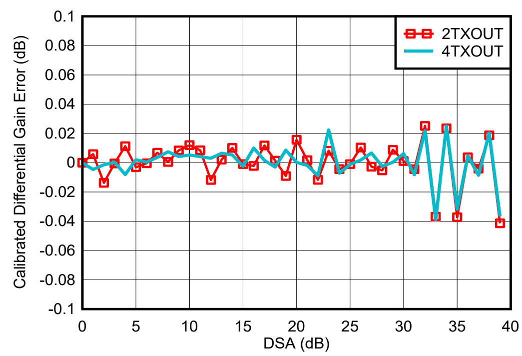
f_{DAC} = 11796.48MSPS, interleave mode, A_{out} = -0.5dBFS, matching 0.8GHz

Figure 4-300. TX Output Power vs DSA Setting and Channel at 0.85GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-301. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85GHz

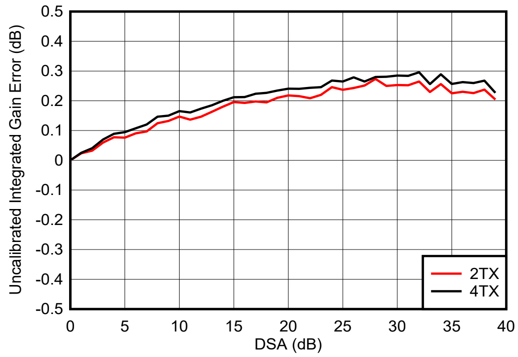


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-302. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85GHz

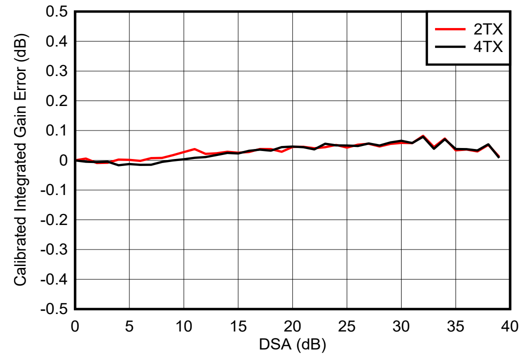
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



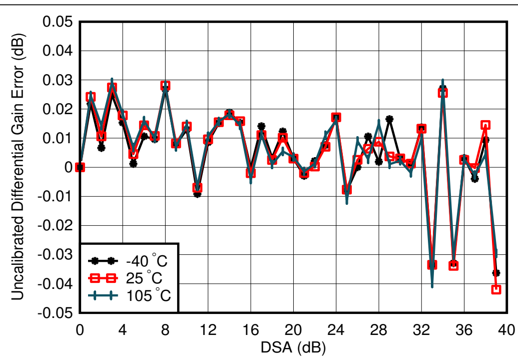
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

Figure 4-303. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85GHz



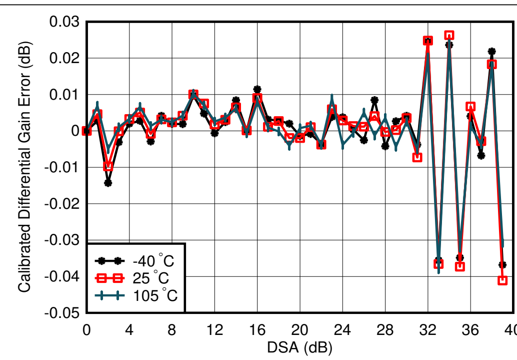
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 4-304. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-305. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85GHz

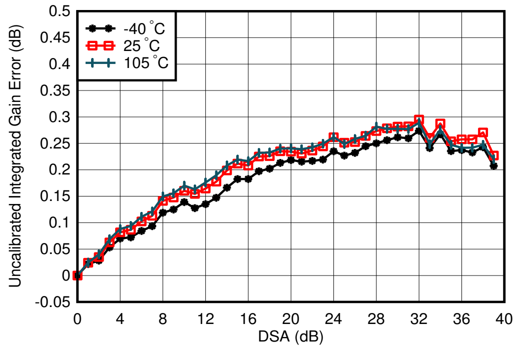


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-306. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85GHz

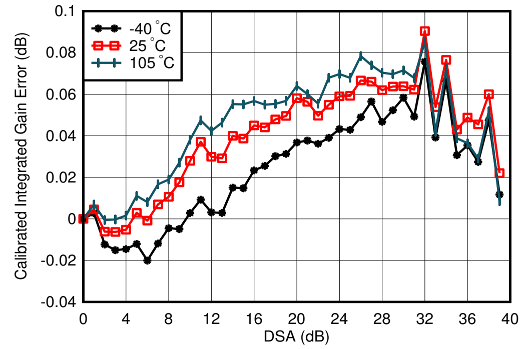
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



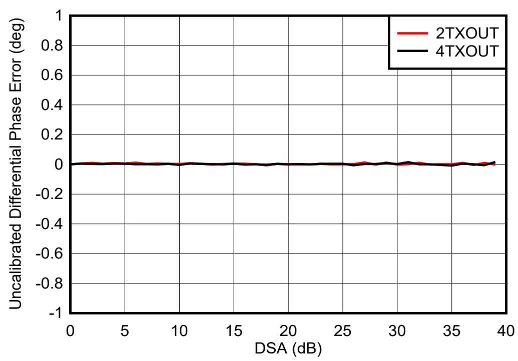
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 4-307. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85GHz



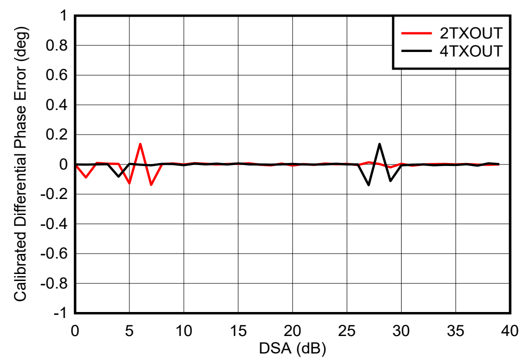
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 4-308. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-309. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85GHz

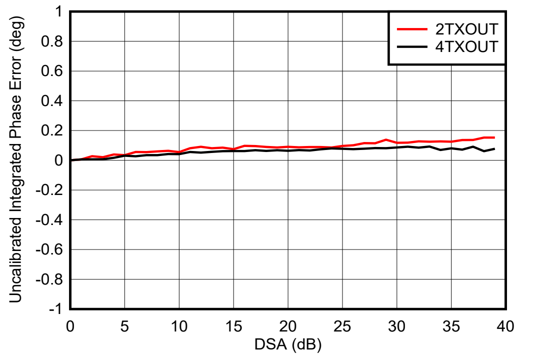


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 4-310. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85GHz

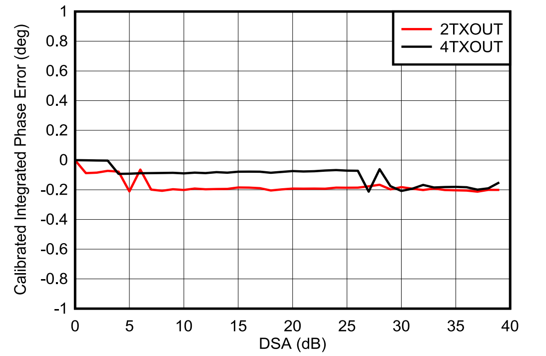
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



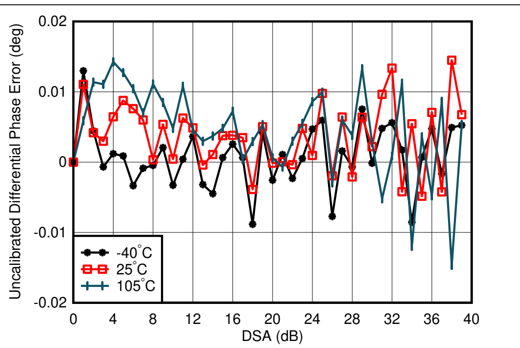
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 4-311. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85GHz



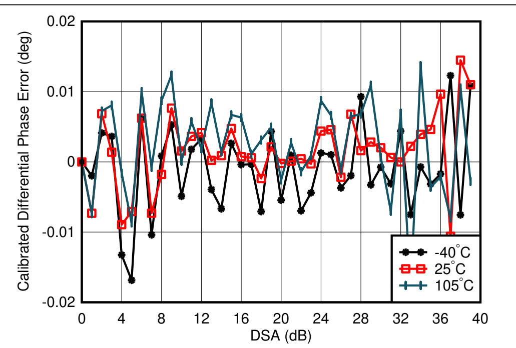
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 4-312. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 4-313. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85GHz

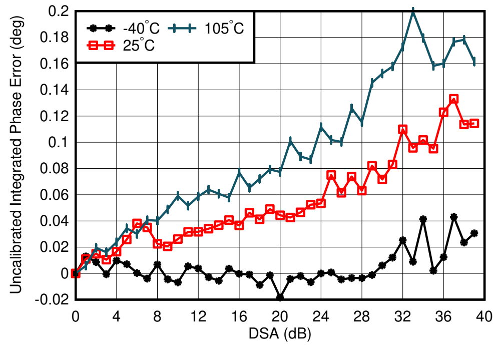


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 4-314. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85GHz

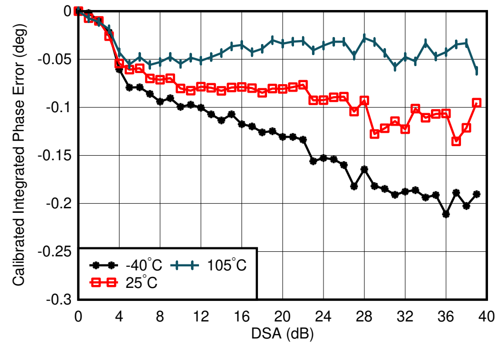
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



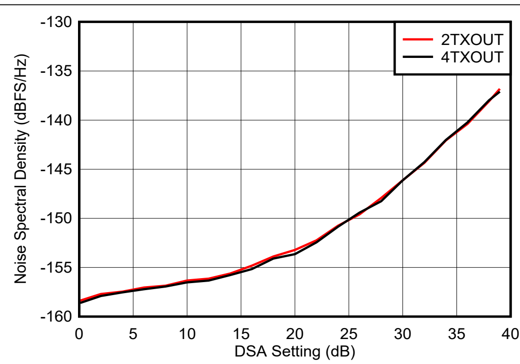
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 4-315. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85GHz



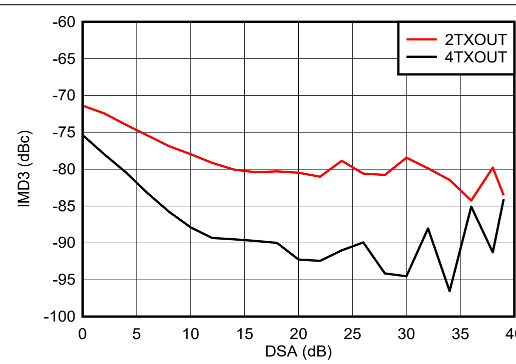
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 4-316. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85GHz



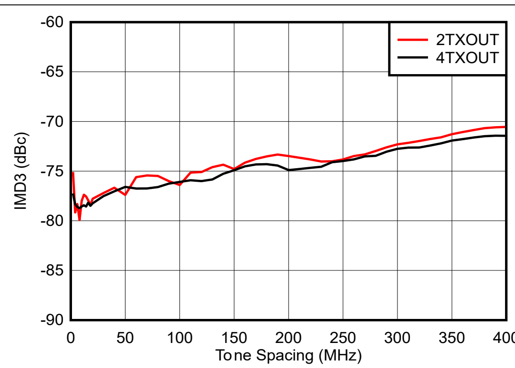
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8GHz, P_{OUT} = –13dBFS

Figure 4-317. TX Output Noise vs Channel and Attenuation at 0.85GHz



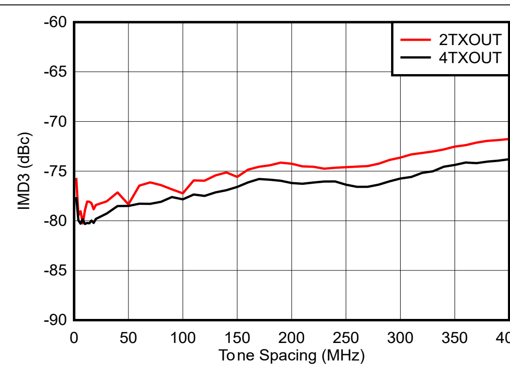
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone

Figure 4-318. TX IMD3 vs DSA Setting at 0.85GHz



f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone

Figure 4-319. TX IMD3 vs Tone Spacing and Channel at 0.85GHz

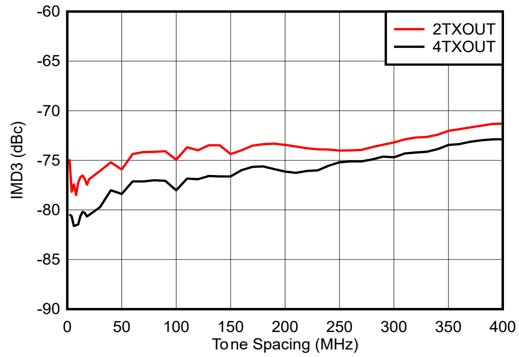


f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone

Figure 4-320. TX IMD3 vs Tone Spacing and Channel at 0.85GHz

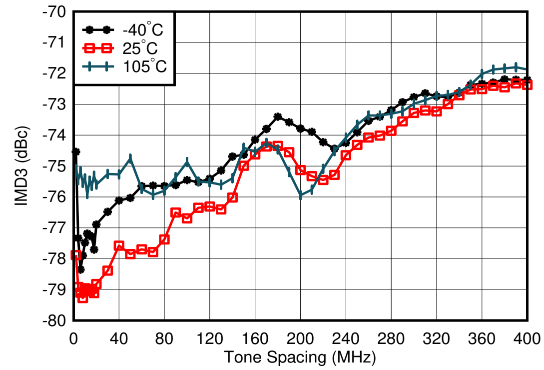
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



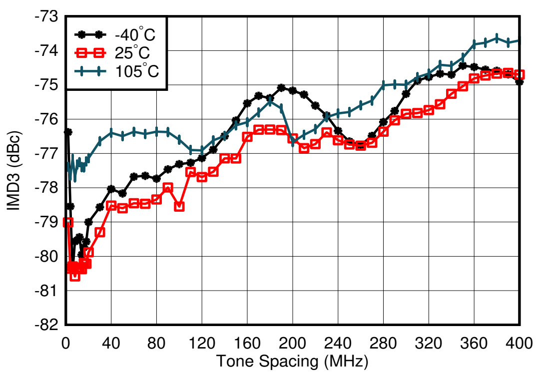
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone

Figure 4-321. TX IMD3 vs Tone Spacing and Channel at 0.85GHz



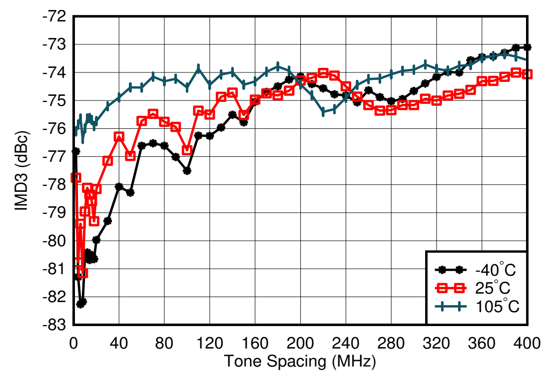
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} =0.85GHz, matching at 0.8GHz, –13dBFS each tone, worst channel

Figure 4-322. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz



f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone, worst channel

Figure 4-323. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz

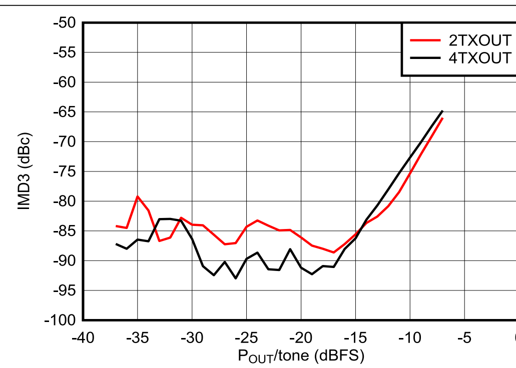


f_{DAC} = 11796.48MSPS, straight mode, f_{CENTER} = 0.85GHz, matching at 0.8GHz, –13dBFS each tone, worst channel

Figure 4-324. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz

f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85GHz, $f_{SPACING}$ = 20MHz, matching at 0.8GHz

Figure 4-325. TX IMD3 vs Digital Level at 0.85GHz

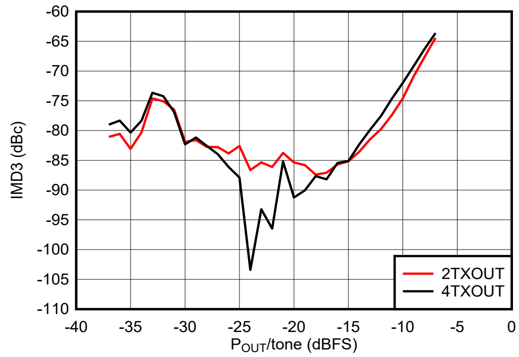


f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85GHz, $f_{SPACING}$ = 20MHz, matching at 0.8GHz

Figure 4-326. TX IMD3 vs Digital Level at 0.85GHz

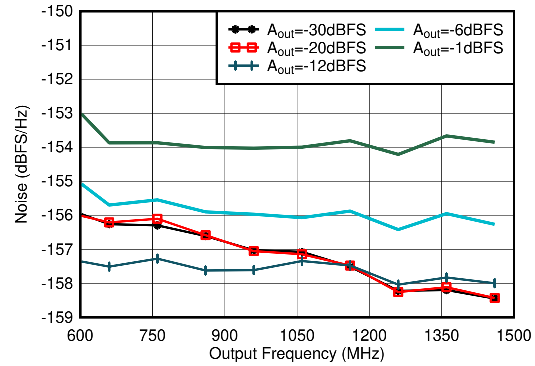
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



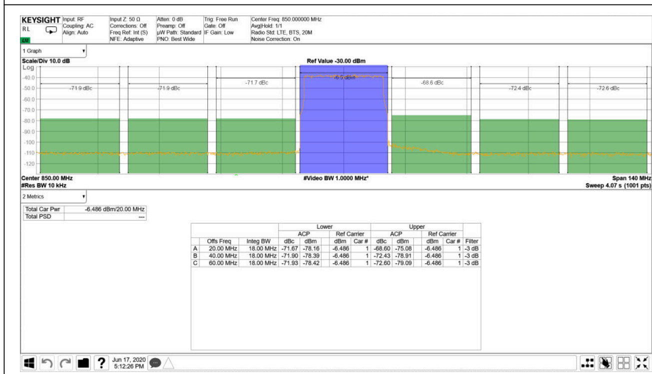
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85GHz, $f_{SPACING}$ = 20MHz, matching at 0.8GHz

Figure 4-327. TX IMD3 vs Digital Level at 0.85GHz



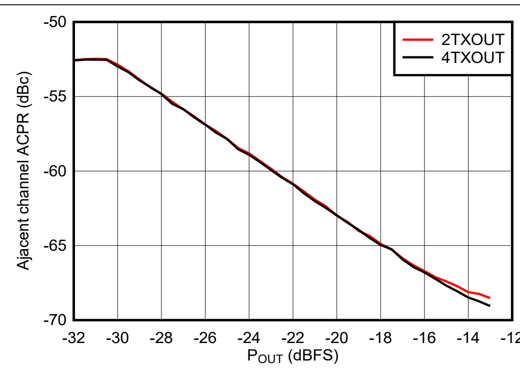
Matching at 0.8GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40MHz offset, DSA = 0dB

Figure 4-328. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85GHz



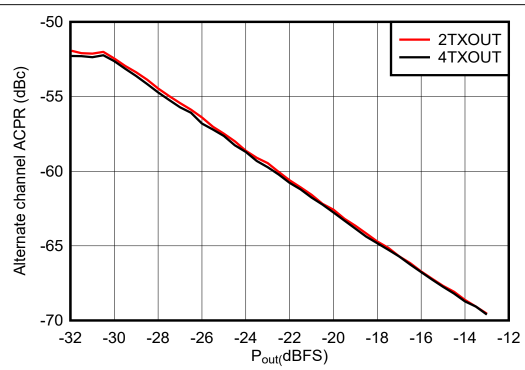
TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-329. TX 20MHz LTE Output Spectrum at 0.85GHz



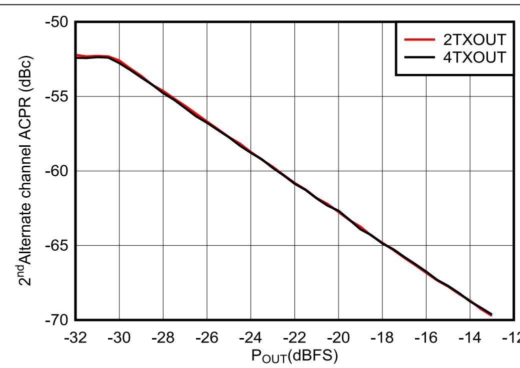
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-330. TX 20MHz LTE ACPR vs Digital Level at 0.85GHz



Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-331. TX 20MHz LTE alt-ACPR vs Digital Level at 0.85GHz

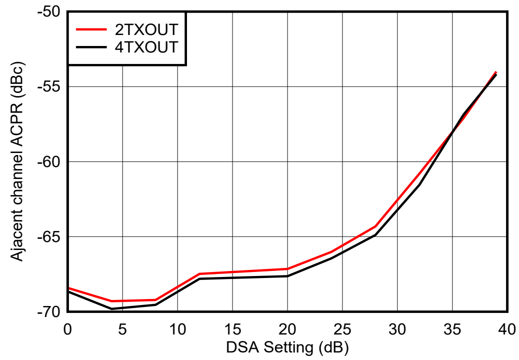


Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-332. TX 20MHz LTE alt2-ACPR vs Digital Level at 0.85GHz

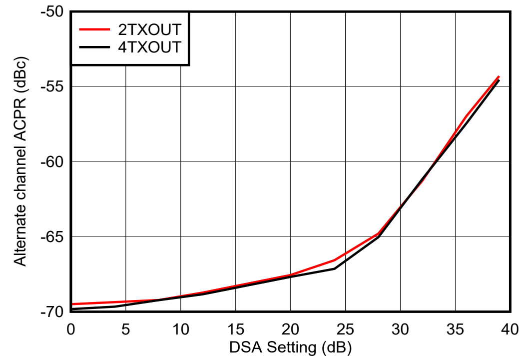
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



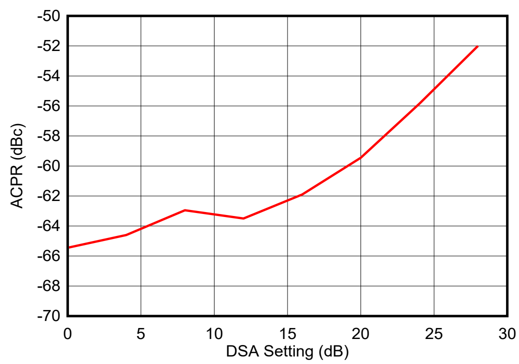
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-333. TX 20MHz LTE ACPR vs DSA at 0.85GHz



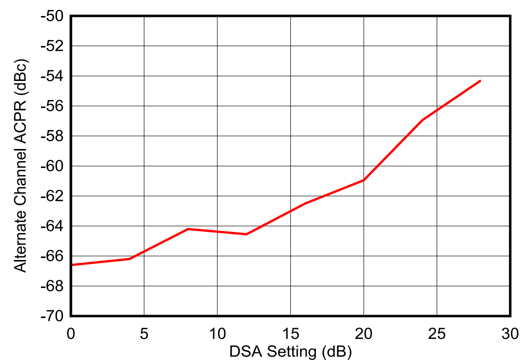
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-334. TX 20MHz LTE alt-ACPR vs DSA at 0.85GHz



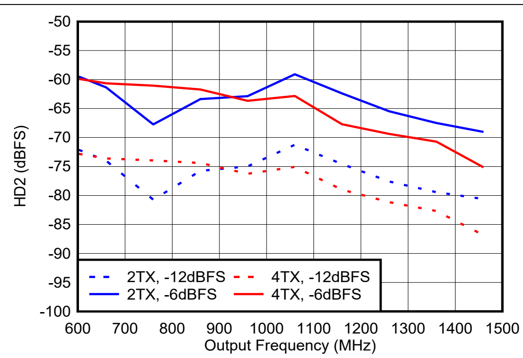
Matching at 0.8GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-335. TX 100MHz NR ACPR vs DSA at 0.85GHz



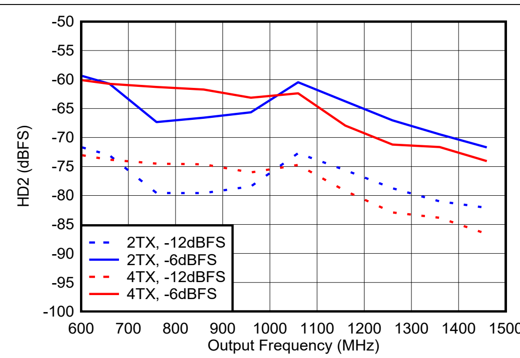
Matching at 0.8GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-336. TX 100MHz NR alt-ACPR vs DSA at 0.85GHz



Matching at 0.8GHz, f_{DAC} = 5898.24GSPS, straight mode

Figure 4-337. TX HD2 vs Digital Amplitude and Output Frequency at 0.85GHz

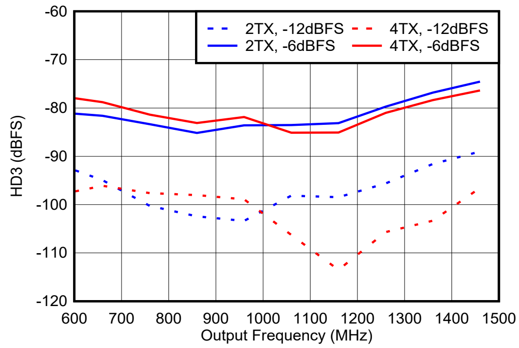


Matching at 0.8GHz, f_{DAC} = 8847.36GSPS, straight mode

Figure 4-338. TX HD2 vs Digital Amplitude and Output Frequency at 0.85GHz

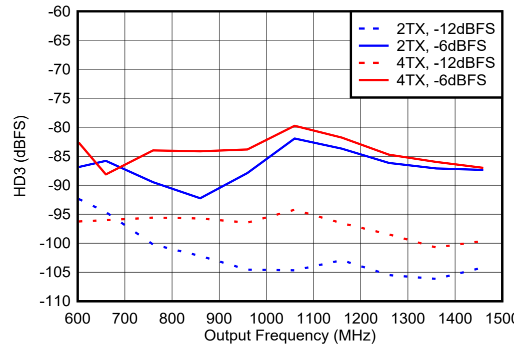
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



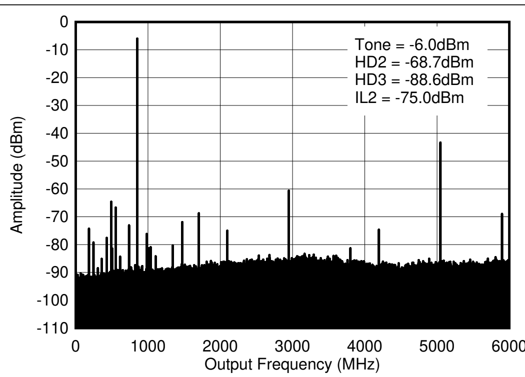
Matching at 0.8GHz, f_{DAC} = 5898.24MSPS, straight mode, normalized to output power at harmonic frequency

Figure 4-339. TX HD3 vs Digital Amplitude and Output Frequency at 0.85GHz



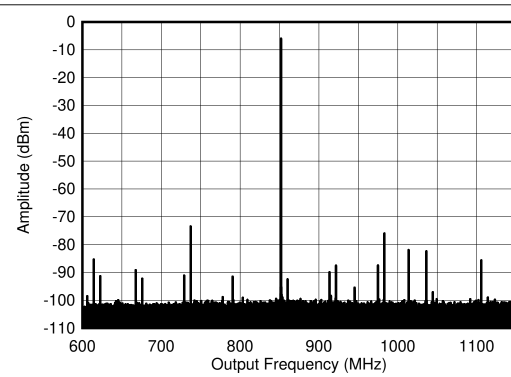
Matching at 0.8GHz, f_{DAC} = 8847.36MSPS, straight mode, normalized to output power at harmonic frequency

Figure 4-340. TX HD3 vs Digital Amplitude and Output Frequency at 0.85GHz



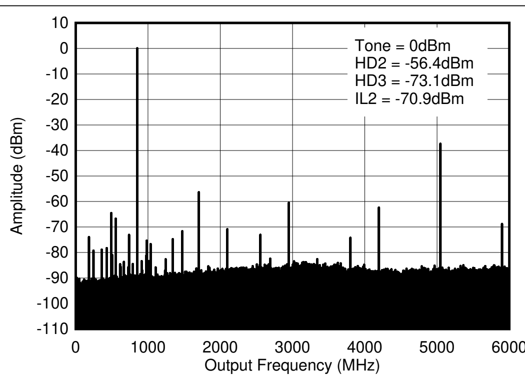
f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 4-341. TX Single Tone (–12dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})



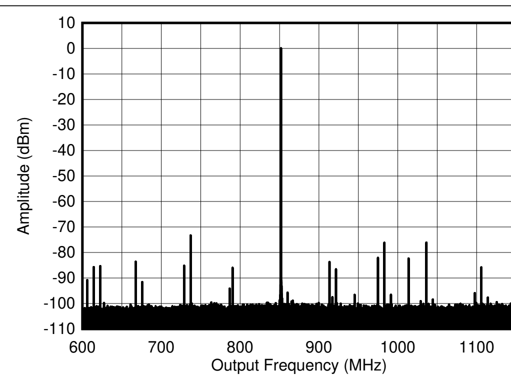
f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-342. TX Single Tone (–12dBFS) Output Spectrum at 0.85GHz (±300MHz)



f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 4-343. TX Single Tone (–6dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})

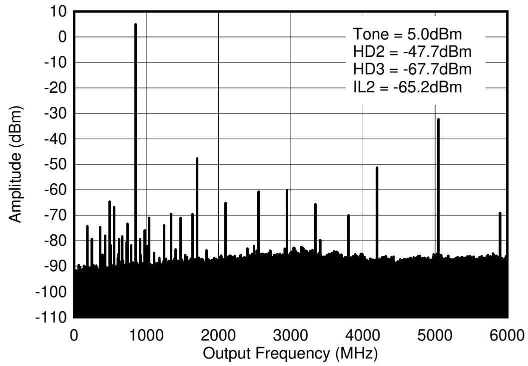


f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-344. TX Single Tone (–6dBFS) Output Spectrum at 0.85GHz (±300MHz)

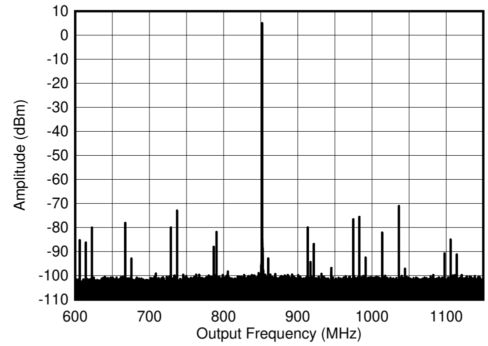
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



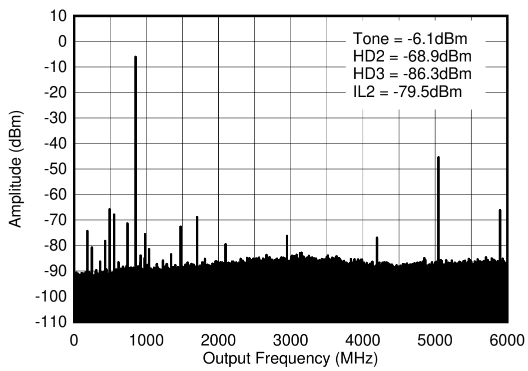
f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-345. TX Single Tone (–1dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})



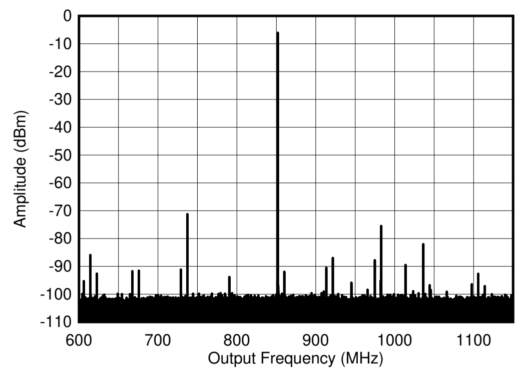
f_{DAC} = 5898.24MSPS, interleave mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-346. TX Single Tone (–1dBFS) Output Spectrum at 0.85GHz (±300MHz)



f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-347. TX Single Tone (–12dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})

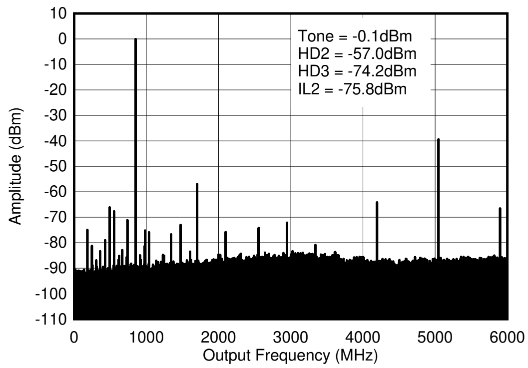


f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-348. TX Single Tone (–12dBFS) Output Spectrum at 0.85GHz (±300MHz)

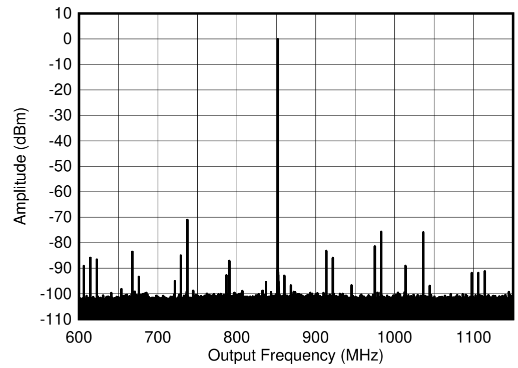
4.12.9 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



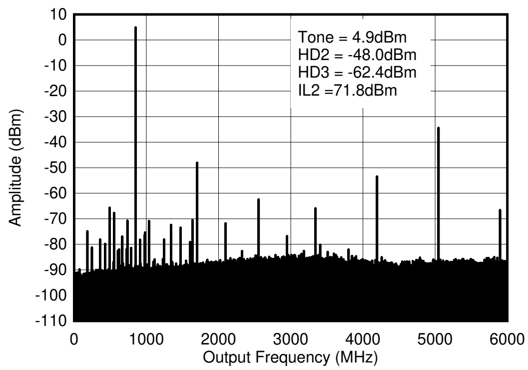
f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-349. TX Single Tone (–6dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})



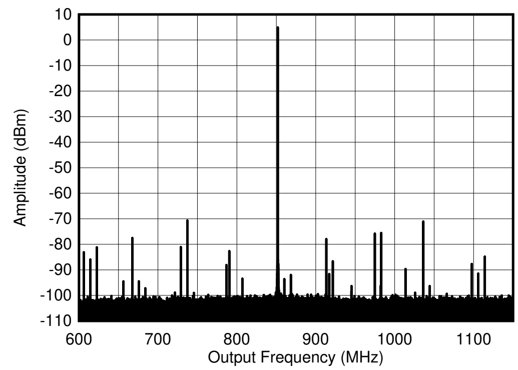
f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-350. TX Single Tone (–6dBFS) Output Spectrum at 0.85GHz (±300MHz)



f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-351. TX Single Tone (–1dBFS) Output Spectrum at 0.85GHz (0-f_{DAC})

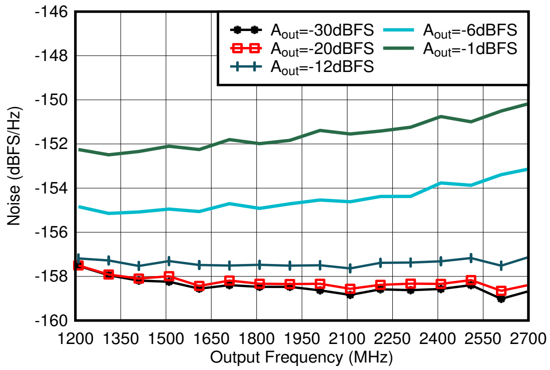


f_{DAC} = 5898.24MSPS, straight mode, 0.8GHz matching, includes PCB and cable losses

Figure 4-352. TX Single Tone (–1dBFS) Output Spectrum at 0.85GHz (±300MHz)

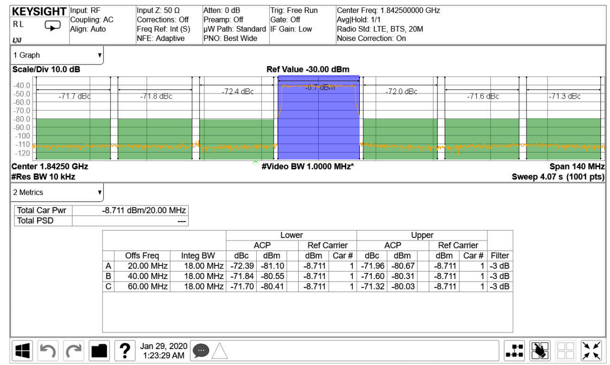
4.12.10 TX Typical Characteristics at 1.8GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



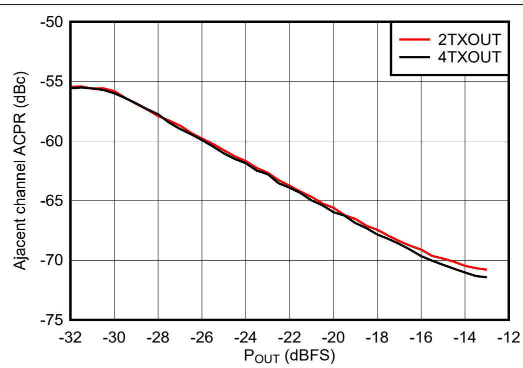
Matching at 1.8GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40MHz offset

Figure 4-353. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8GHz



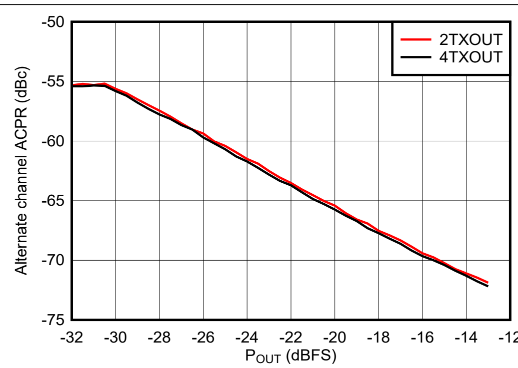
TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-354. TX 20MHz LTE Output Spectrum at 1.8425GHz



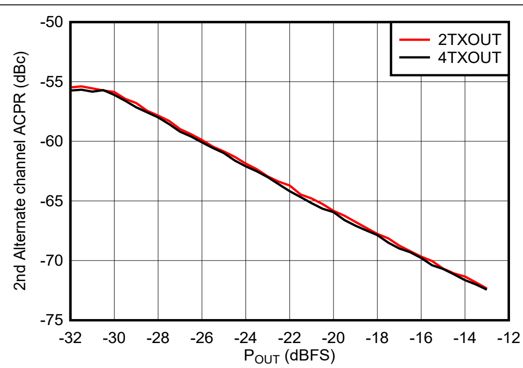
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-355. TX 20MHz LTE ACPR vs Digital Level at 1.8425GHz



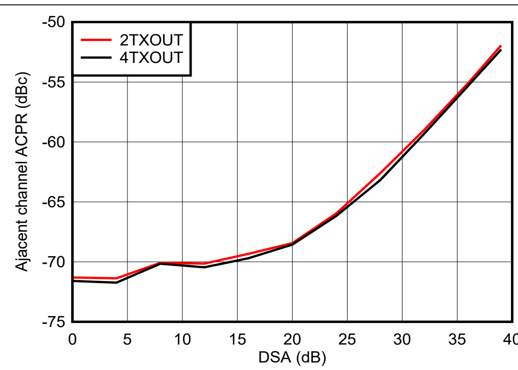
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-356. TX 20MHz LTE alt-ACPR vs Digital Level at 1.8425GHz



Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-357. TX 20MHz LTE alt2-ACPR vs Digital Level at 1.8425GHz

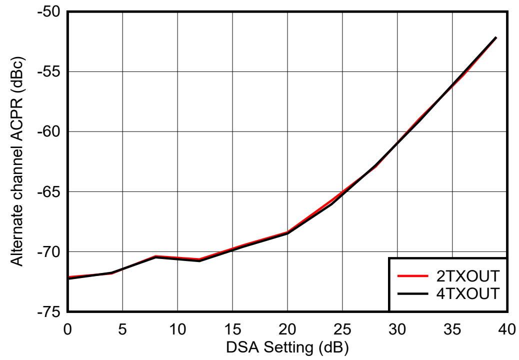


Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-358. TX 20MHz LTE ACPR vs DSA at 1.8GHz

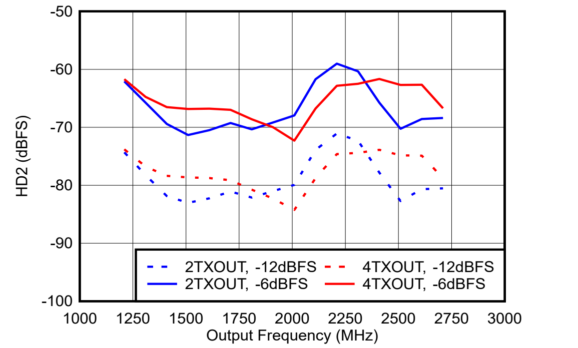
4.12.10 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



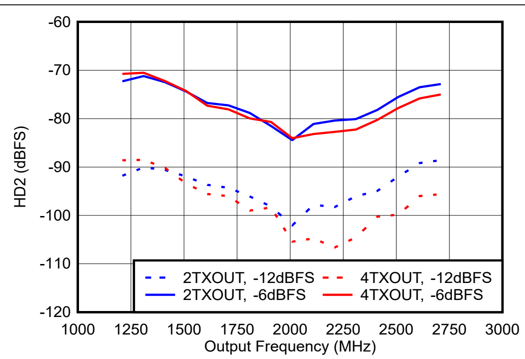
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-359. TX 20MHz LTE alt-ACPR vs DSA at 1.8GHz



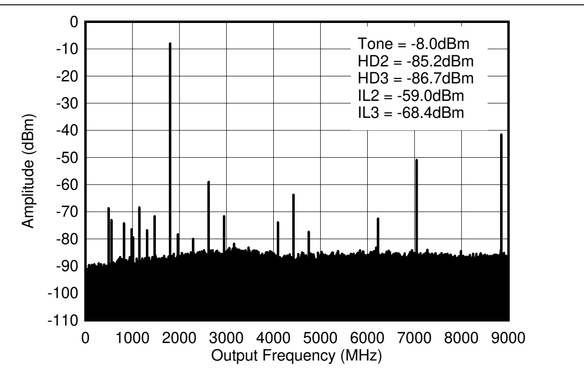
Matching at 1.8GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-360. TX HD2 vs Digital Amplitude and Output Frequency at 1.8GHz



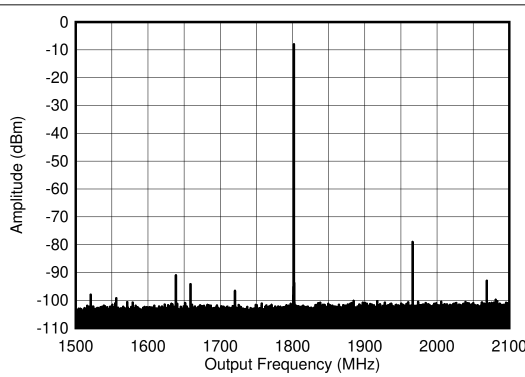
Matching at 1.8GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-361. TX HD3 vs Digital Amplitude and Output Frequency at 1.8GHz



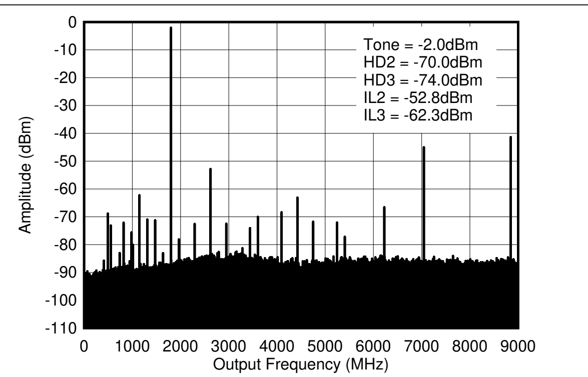
f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 4-362. TX Single Tone (–12dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})



f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-363. TX Single Tone (–12dBFS) Output Spectrum at 1.8GHz (±300MHz)

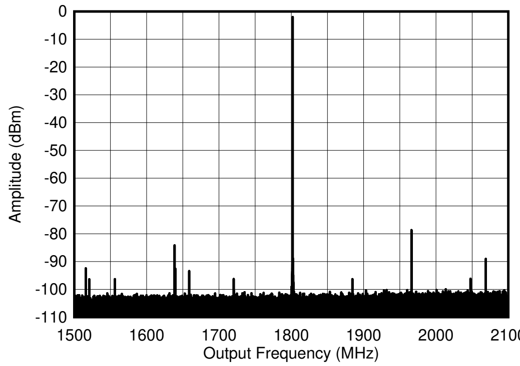


f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 4-364. TX Single Tone (–6dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})

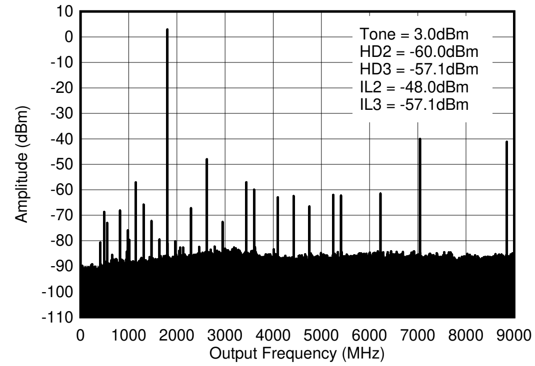
4.12.10 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



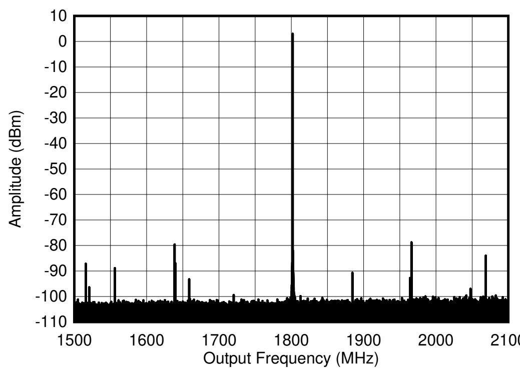
f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-365. TX Single Tone (–6dBFS) Output Spectrum at 1.8GHz (±300MHz)



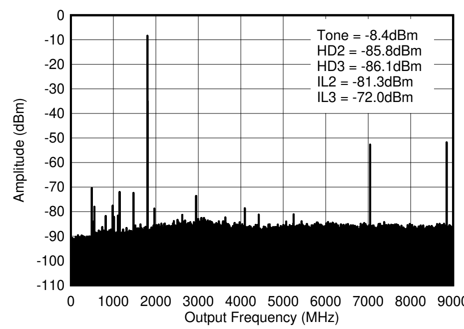
f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-366. TX Single Tone (–1dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})



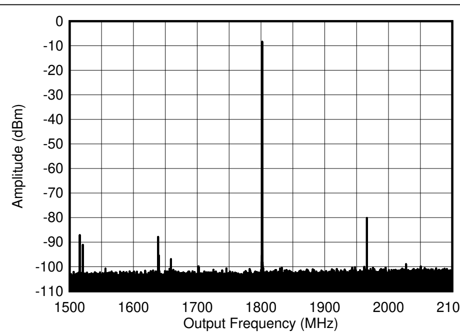
f_{DAC} = 8847.36MSPS, interleave mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-367. TX Single Tone (–1dBFS) Output Spectrum at 1.8GHz (±300MHz)



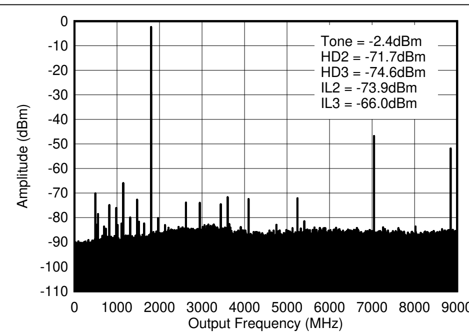
f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-368. TX Single Tone (–12dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})



f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-369. TX Single Tone (–12dBFS) Output Spectrum at 1.8GHz (±300MHz)

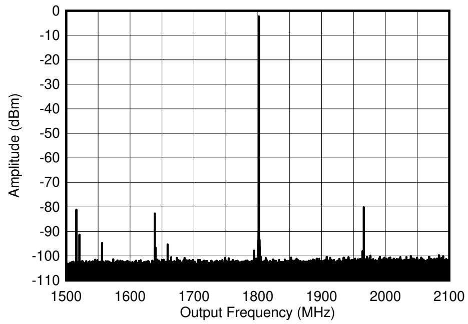


f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-370. TX Single Tone (–6dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})

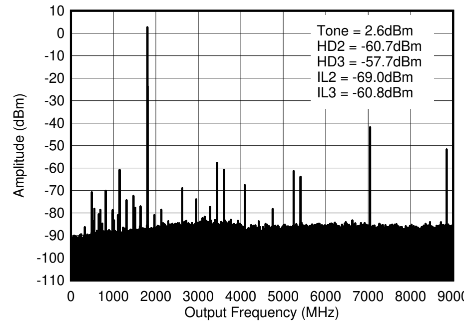
4.12.10 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



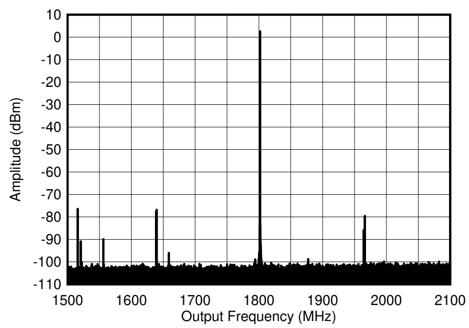
f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-371. TX Single Tone (–6dBFS) Output Spectrum at 1.8GHz (±300MHz)



f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-372. TX Single Tone (–1dBFS) Output Spectrum at 1.8GHz (0-f_{DAC})

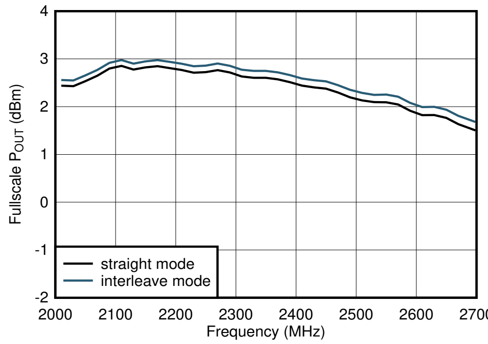


f_{DAC} = 8847.36MSPS, straight mode, 1.8GHz matching, includes PCB and cable losses

Figure 4-373. TX Single Tone (–1dBFS) Output Spectrum at 1.8GHz (±300MHz)

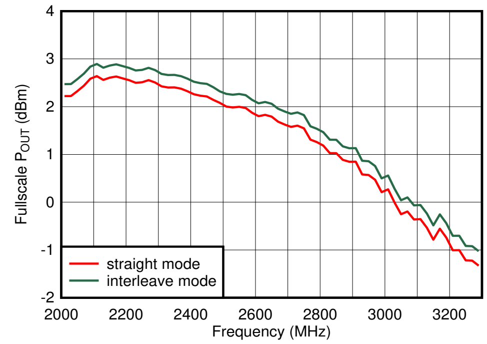
4.12.11 TX Typical Characteristics at 2.6GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



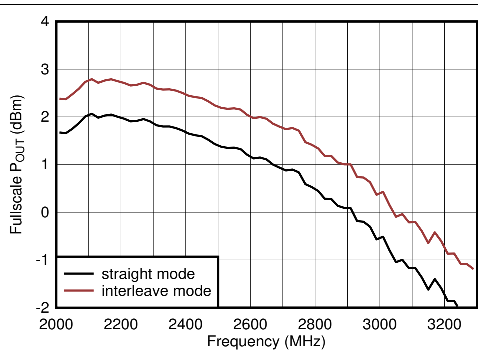
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6GHz matching

Figure 4-374. TX Full Scale vs RF Frequency at 5898.24MSPS



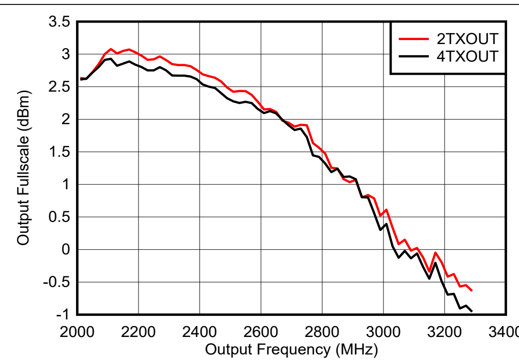
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6GHz matching

Figure 4-375. TX Full Scale vs RF Frequency at 8847.36MSPS



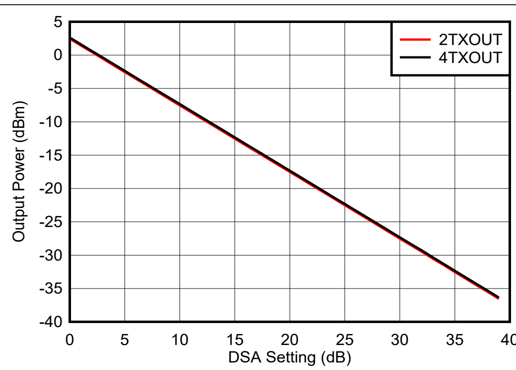
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6GHz matching

Figure 4-376. TX Full Scale vs RF Frequency at 11796.48MSPS



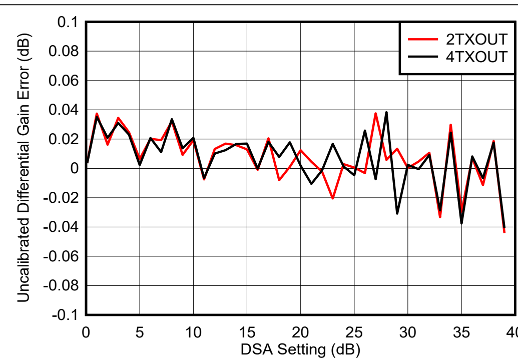
f_{DAC} = 8847.36MSPS, interleave mode, including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6GHz matching

Figure 4-377. TX Output Fullscale vs Output Frequency and Channel



f_{DAC} = 8847.36MSPS, A_{out} = -0.5dBFS, matching 2.6GHz

Figure 4-378. TX Output Power vs DSA Setting and Channel at 2.6GHz

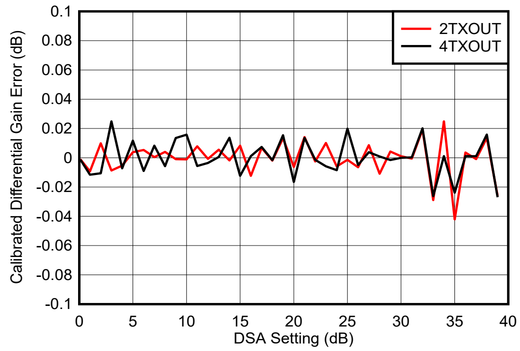


f_{DAC} =8847.36MSPS, straight mode, matching at 2.6GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-379. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6GHz

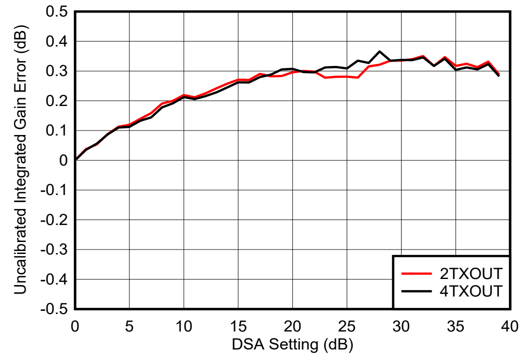
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



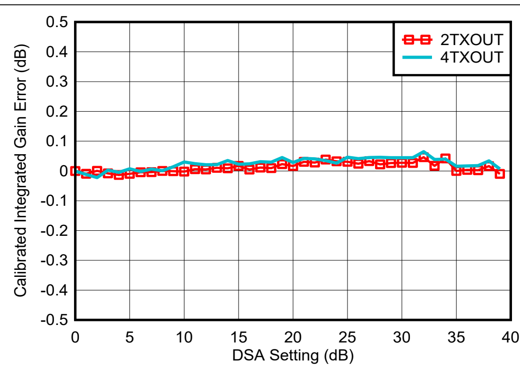
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-380. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6GHz



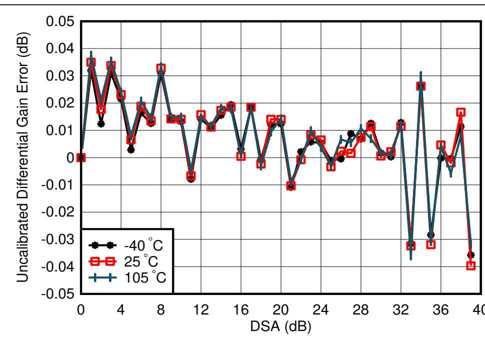
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-381. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-382. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6GHz

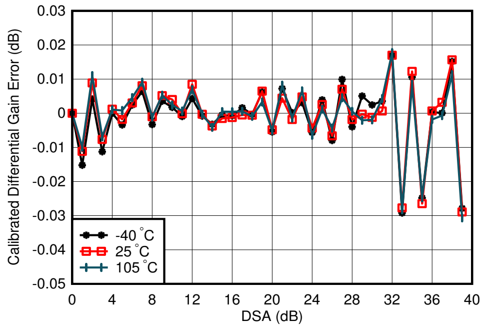


f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-383. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6GHz

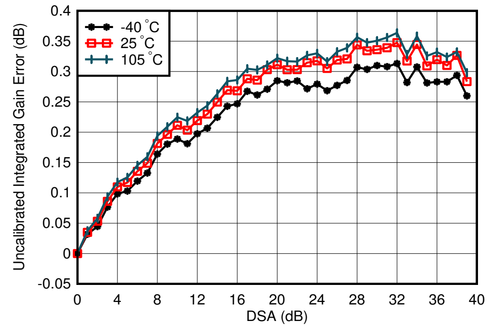
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



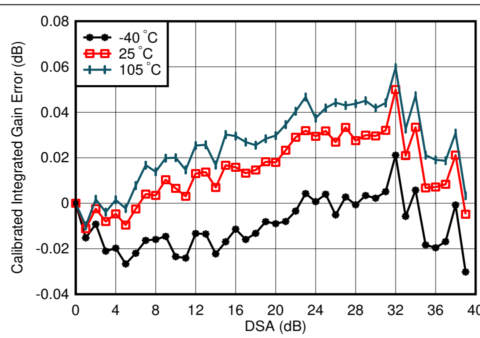
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-384. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6GHz



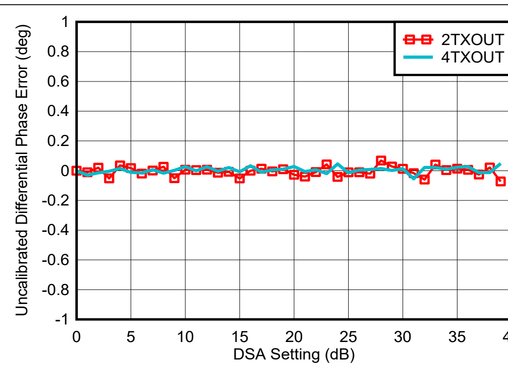
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-385. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-386. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6GHz

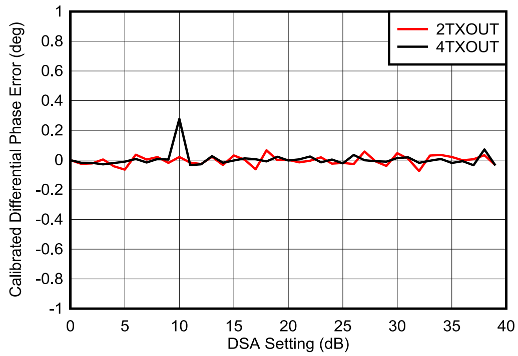


f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-387. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6GHz

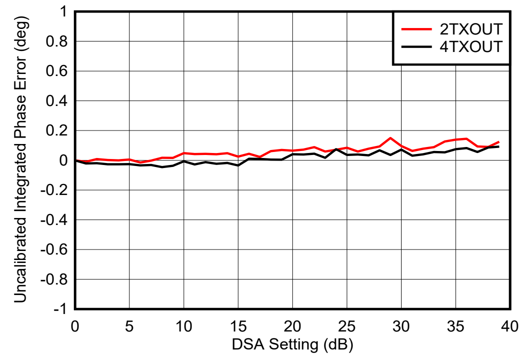
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



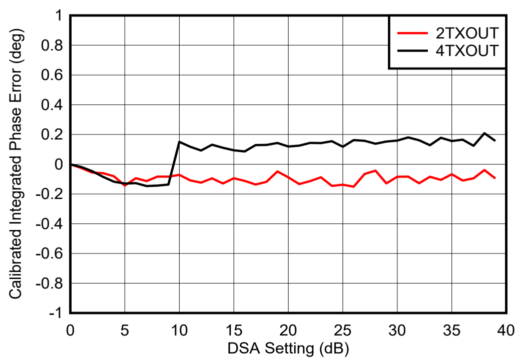
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 4-388. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6GHz



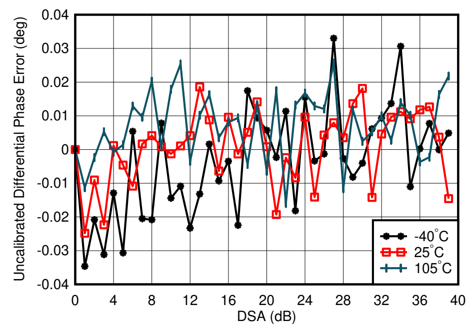
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-389. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-390. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6GHz

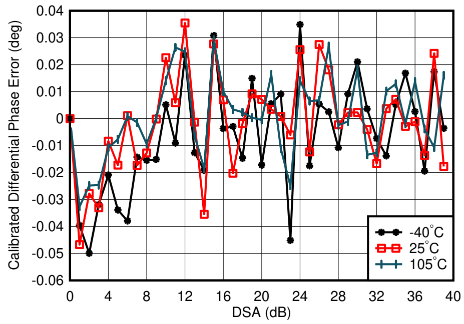


f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-391. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6GHz

4.12.11 TX Typical Characteristics at 2.6GHz (continued)

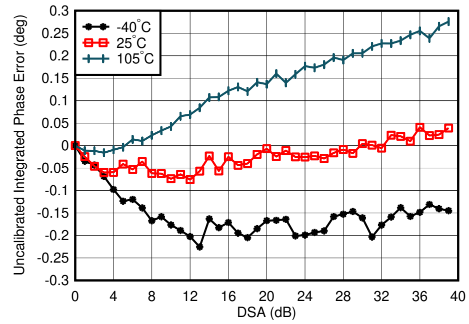
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

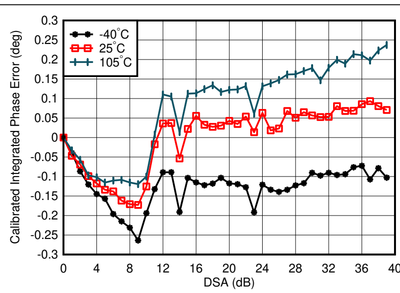
Figure 4-392. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the medium variation over DSA setting at 25°C

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

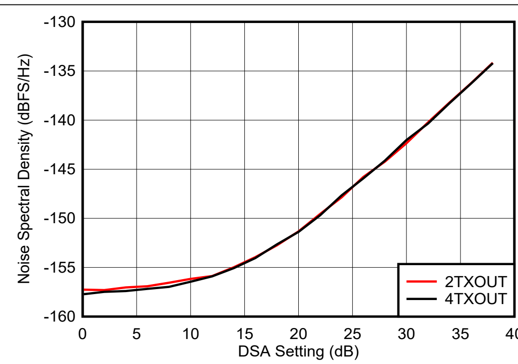
Figure 4-393. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C

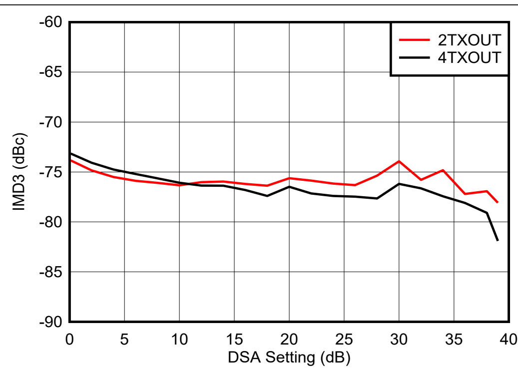
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-394. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6GHz



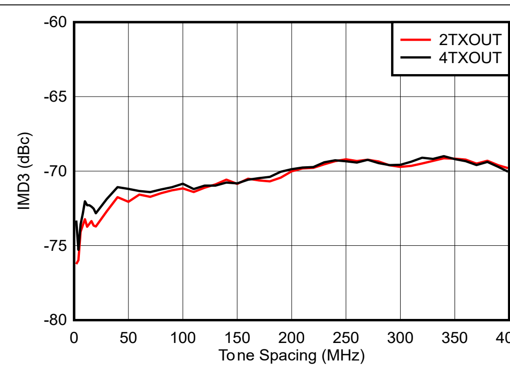
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6GHz, P_{OUT} = –13dBFS

Figure 4-395. TX Output Noise vs Channel and Attenuation at 2.6GHz



f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6GHz, matching at 2.6GHz, –13dBFS each tone

Figure 4-396. TX IMD3 vs DSA Setting at 2.6GHz

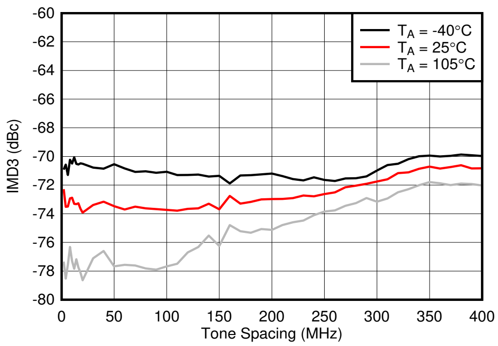


f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6GHz, matching at 2.6GHz, –13dBFS each tone

Figure 4-397. TX IMD3 vs Tone Spacing and Channel at 2.6GHz

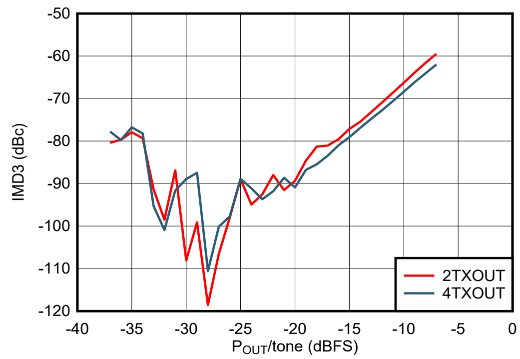
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



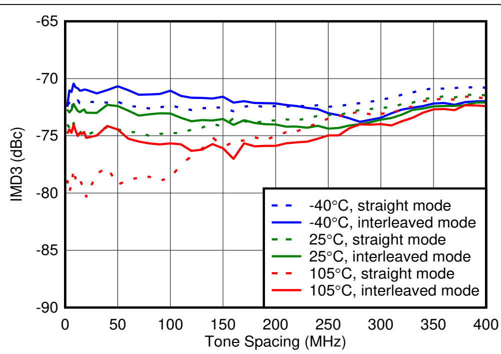
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6GHz, matching at 2.6GHz, –13dBFS each tone, worst channel, dither = 1.

Figure 4-398. TX IMD3 vs Tone Spacing and Temperature at 2.6GHz



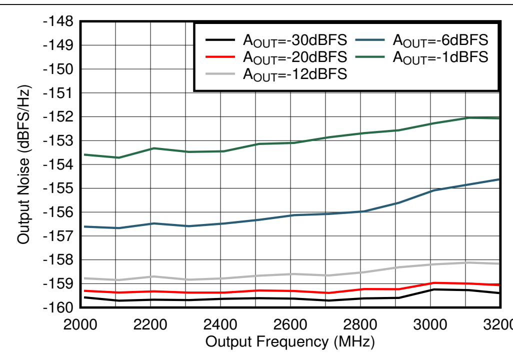
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6GHz, $f_{SPACING}$ = 20MHz, dither = 1, matching at 2.6GHz

Figure 4-399. TX IMD3 vs Digital Level at 2.6GHz



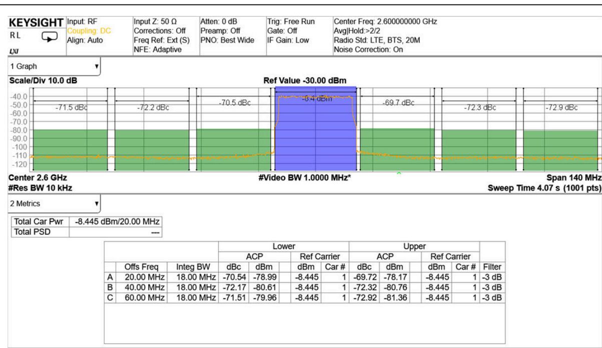
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6GHz, matching at 2.6GHz, –13dBFS each tone

Figure 4-400. TX IMD3 vs Tone Spacing and Temperature



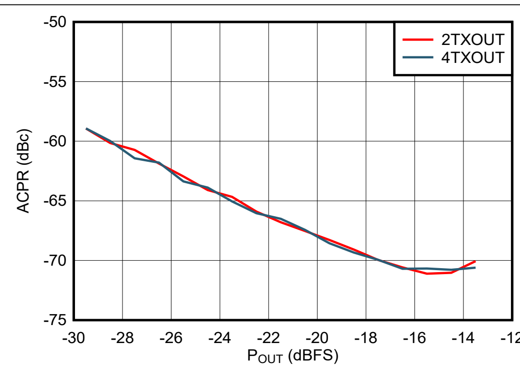
Matching at 2.6GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40MHz offset

Figure 4-401. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6GHz



TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-402. TX 20MHz LTE Output Spectrum at 2.6GHz (Band 41)

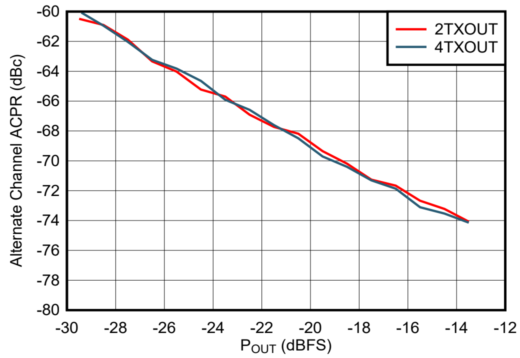


Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-403. TX 20MHz LTE ACPR vs Digital Level at 2.6GHz

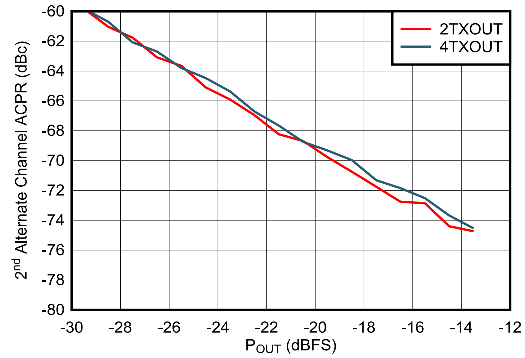
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



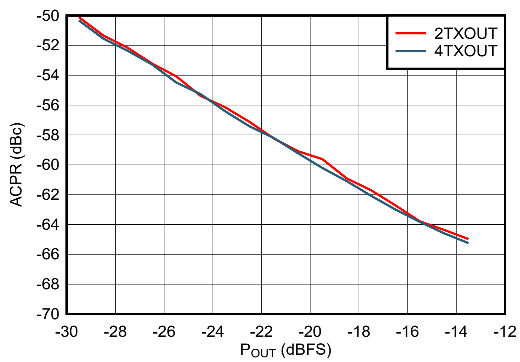
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-404. TX 20MHz LTE alt-ACPR vs Digital Level at 2.6GHz



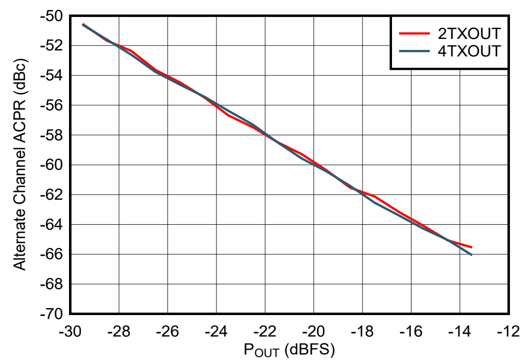
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-405. TX 20MHz LTE alt2-ACPR vs Digital Level at 2.6GHz



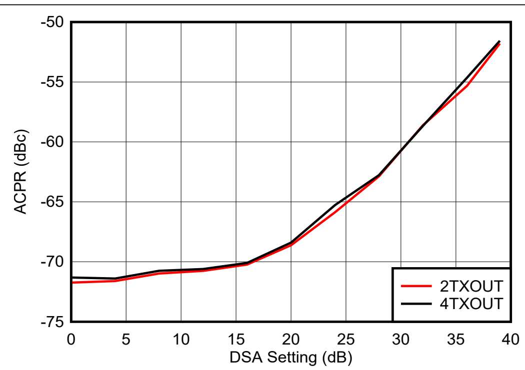
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-406. TX 100MHz NR ACPR vs Digital Level at 2.6GHz



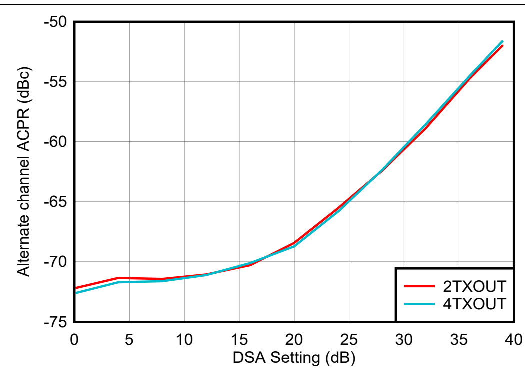
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-407. TX 100MHz NR alt-ACPR vs Digital Level at 2.6GHz



Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-408. TX 20MHz LTE ACPR vs DSA at 2.6GHz

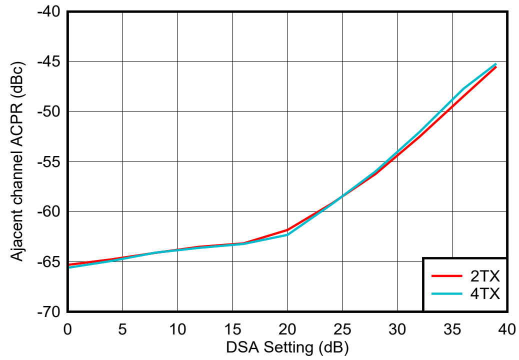


Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-409. TX 20MHz LTE alt-ACPR vs DSA at 2.6GHz

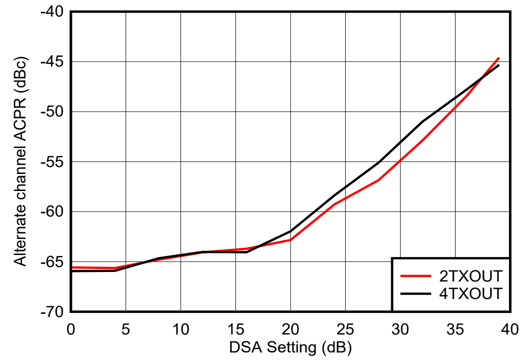
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



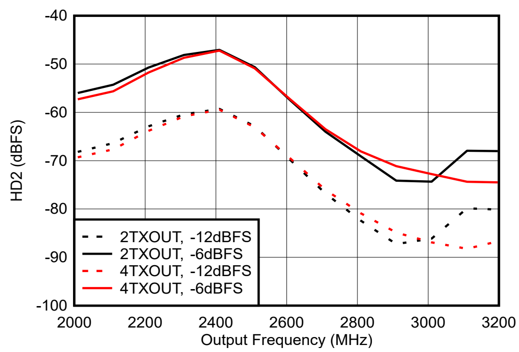
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-410. TX 100MHz NR ACPR vs DSA at 2.6GHz



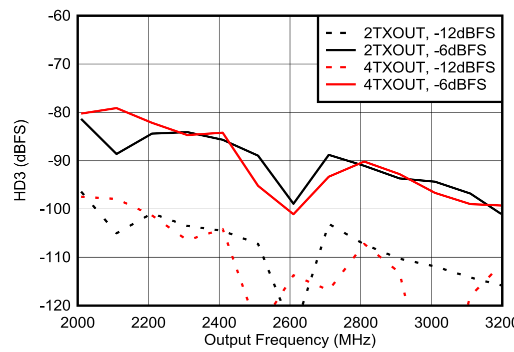
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-411. TX 100MHz NR alt-ACPR vs DSA at 2.6GHz



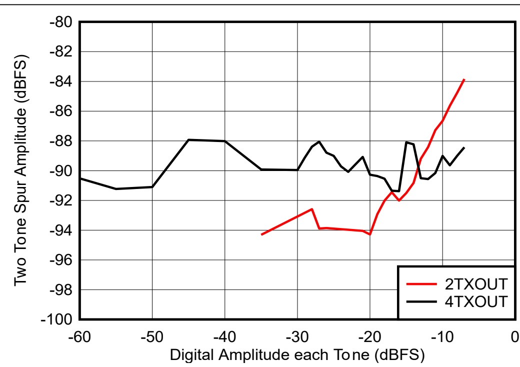
Matching at 2.6GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-412. TX HD2 vs Digital Amplitude and Output Frequency at 2.6GHz



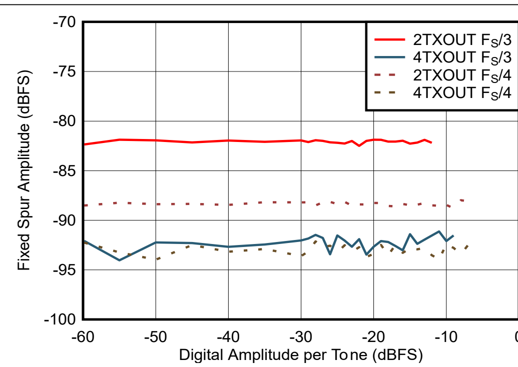
Matching at 2.6GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-413. TX HD3 vs Digital Amplitude and Output Frequency at 2.6GHz



Inband = 2600MHz ± 600MHz, f_{DAC} = 12GSPS, not including F_S/3 and F_S/4, external clock mode, non-interleave mode

Figure 4-414. Two Tone Inband SFDR vs Digital Amplitude at 2.6GHz

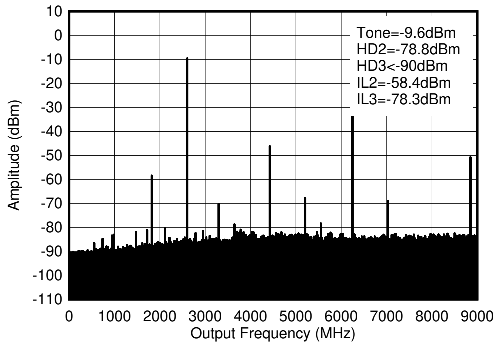


Inband = 2600MHz ± 600MHz, f_{DAC} = 12 GSPS, external clock mode, non-interleave mode

Figure 4-415. Two Tone Inband Fixed Spurs vs Digital Amplitude at 2.6GHz

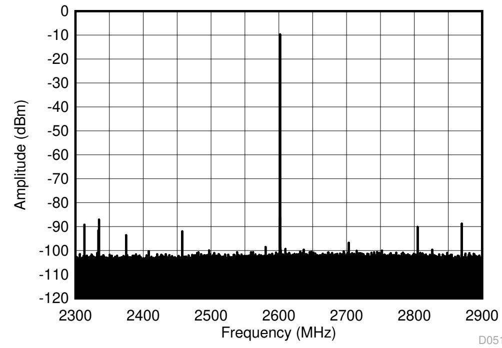
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



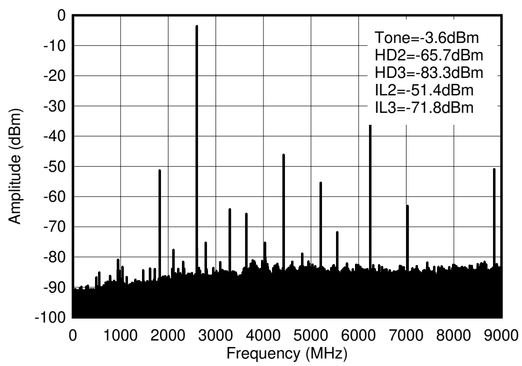
f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-416. TX Single Tone (–12dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})



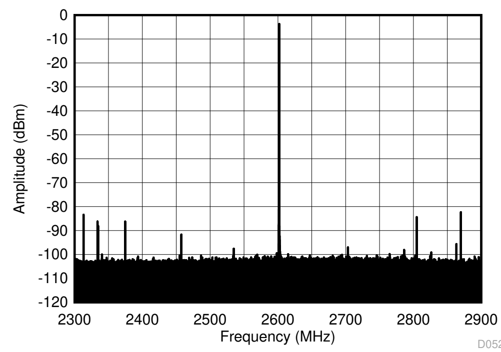
f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-417. TX Single Tone (–12dBFS) Output Spectrum at 2.6GHz (±300MHz)



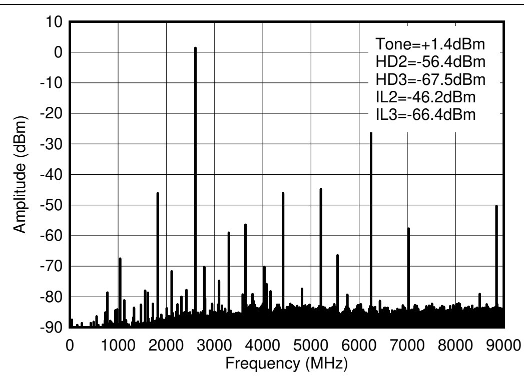
f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-418. TX Single Tone (–6dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})



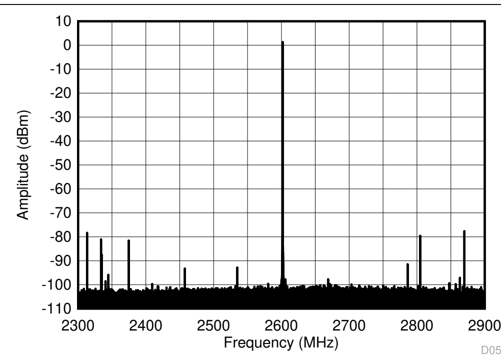
f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-419. TX Single Tone (–6dBFS) Output Spectrum at 2.6GHz (±300MHz)



f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-420. TX Single Tone (–1dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})

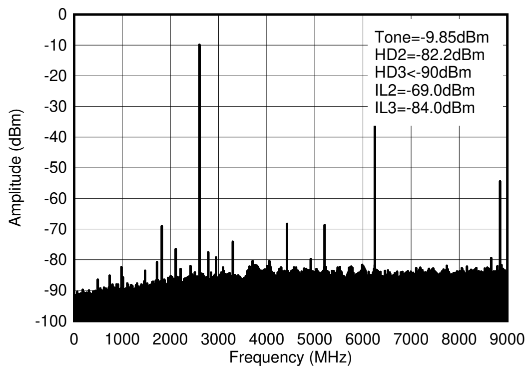


f_{DAC} = 8847.36MSPS, interleave mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-421. TX Single Tone (–1dBFS) Output Spectrum at 2.6GHz (±300MHz)

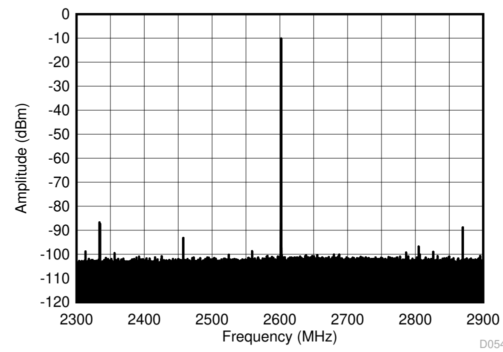
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



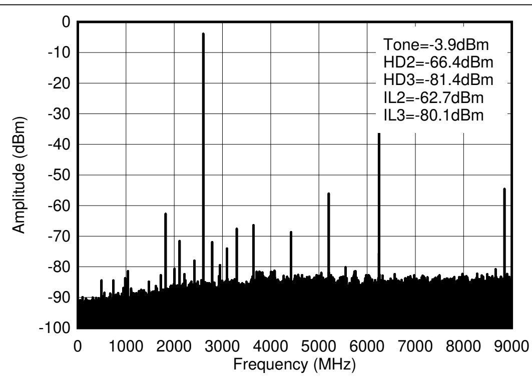
f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-422. TX Single Tone (–12dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})



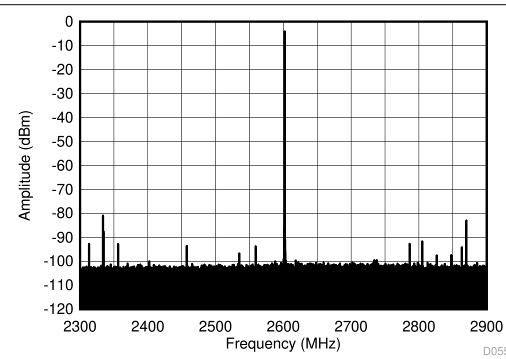
f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-423. TX Single Tone (–12dBFS) Output Spectrum at 2.6GHz (±300MHz)



f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-424. TX Single Tone (–6dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})

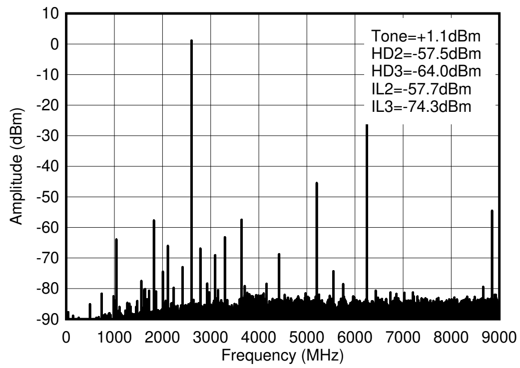


f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-425. TX Single Tone (–6dBFS) Output Spectrum at 2.6GHz (±300MHz)

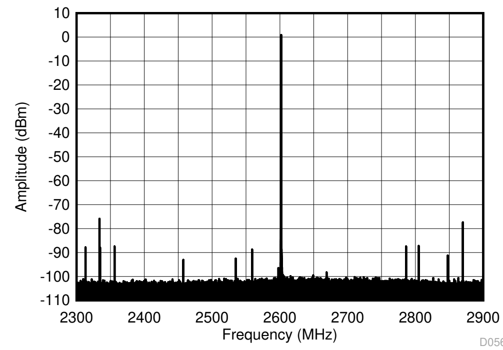
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



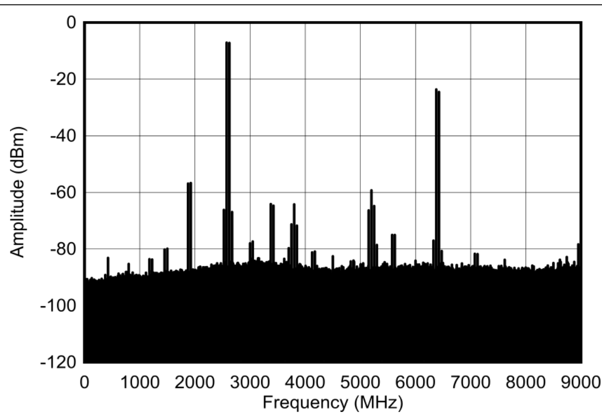
f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

Figure 4-426. TX Single Tone (–1dBFS) Output Spectrum at 2.6GHz (0-f_{DAC})



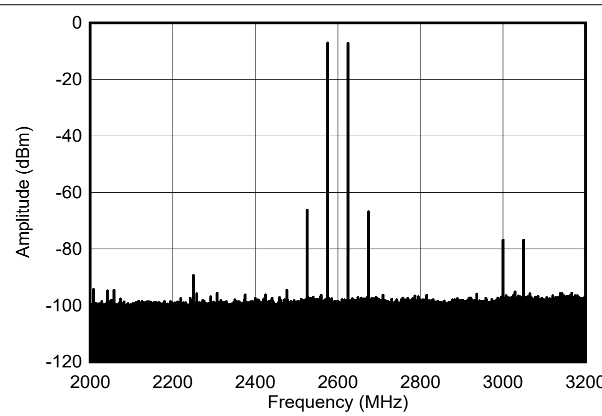
f_{DAC} = 8847.36MSPS, straight mode, 2.6GHz matching, includes PCB and cable losses

Figure 4-427. TX Single Tone (–1dBFS) Output Spectrum at 2.6GHz (±300MHz)



f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-428. TX Dual Tone Output Spectrum at 2.6GHz, -7dBFS each (0 - $_{DAC}$)

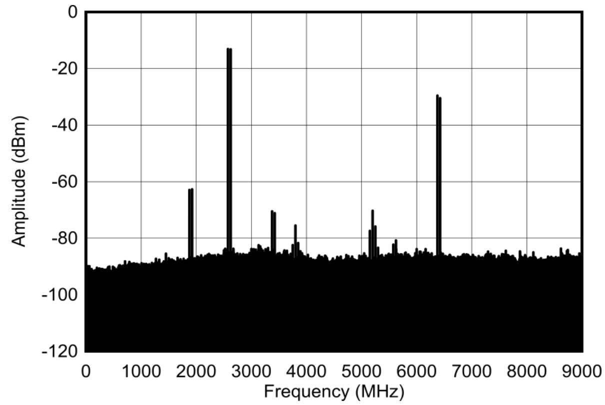


f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-429. TX Dual Tone Output Spectrum at 2.6GHz, -7dBFS each (±600MHz)

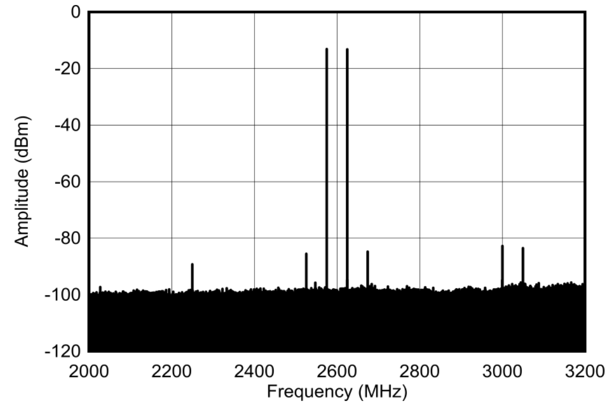
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



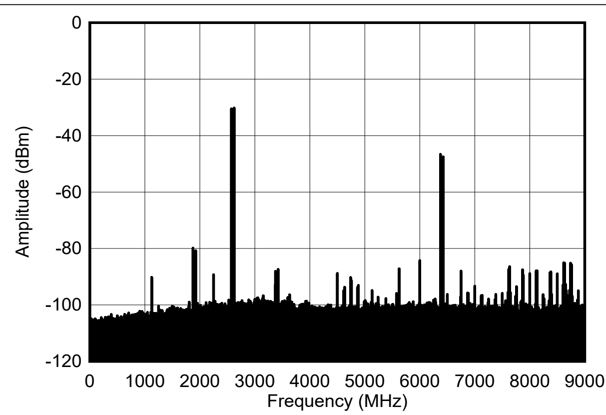
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-430. TX Dual Tone Output Spectrum at 2.6GHz, -13dBFS each (0 - $_{DAC}$)



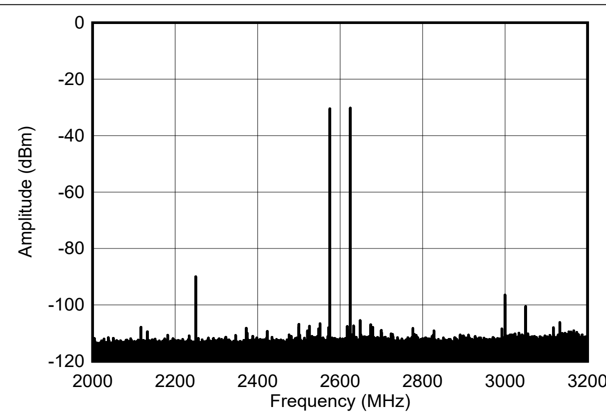
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-431. TX Dual Tone Output Spectrum at 2.6GHz, -13dBFS each (±600MHz)



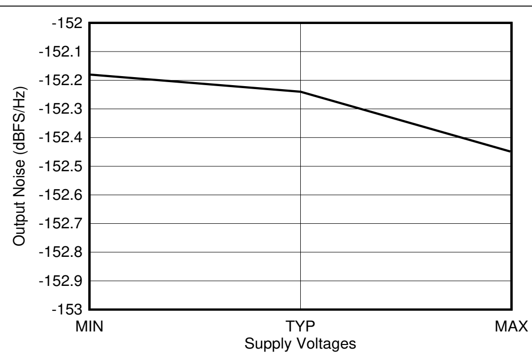
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-432. TX Dual Tone Output Spectrum at 2.6GHz, -30dBFS each (0 - $_{DAC}$)



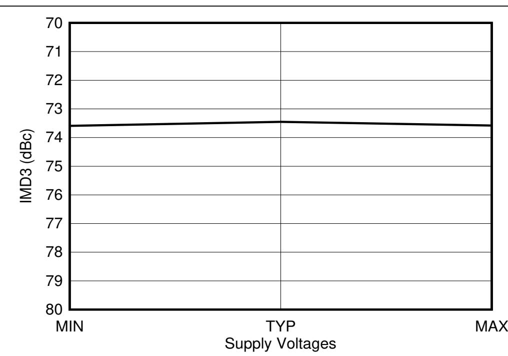
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

Figure 4-433. TX Dual Tone Output Spectrum at 2.6GHz, -30dBFS each (±600MHz)



f_{DAC} = 11796.48MSPS, interleave mode, 2.6GHz matching. 40-MHz offset from tone. Output Power = –1dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 4-434. TX Output Noise vs Supply Voltage at 2.6GHz

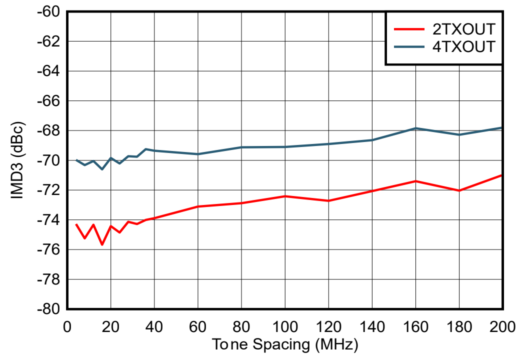


f_{DAC} = 11796.48MSPS, interleave mode, 2.6GHz matching. 40-MHz offset from tone. Output Power = –13dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 4-435. TX IMD3 vs Supply Voltage at 2.6GHz

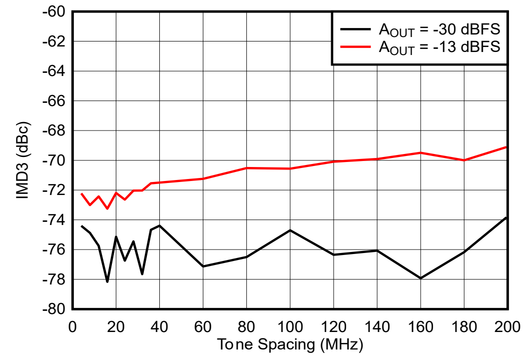
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



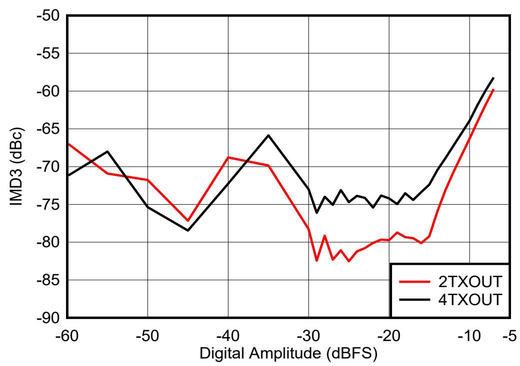
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

Figure 4-436. IMD3 vs Tone Spacing and Channel at 2.6GHz



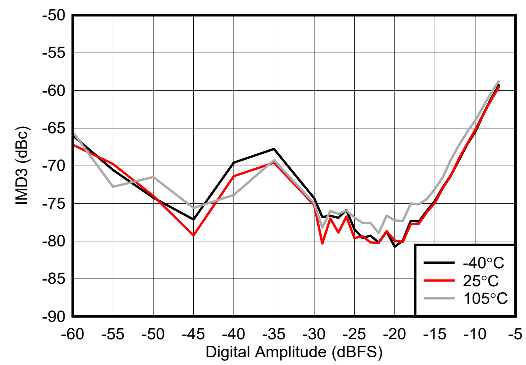
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

Figure 4-437. IMD3 vs Tone Spacing and Amplitude at 2.6GHz



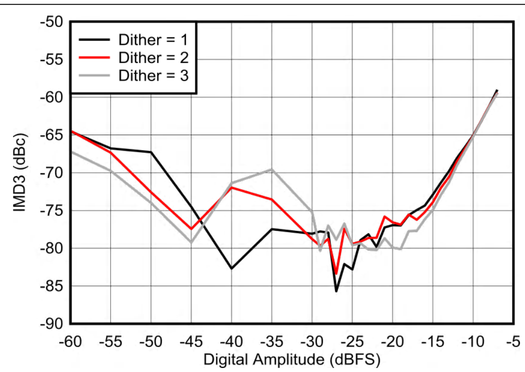
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

Figure 4-438. IMD3 vs Digital Amplitude and Channel at 2.6GHz



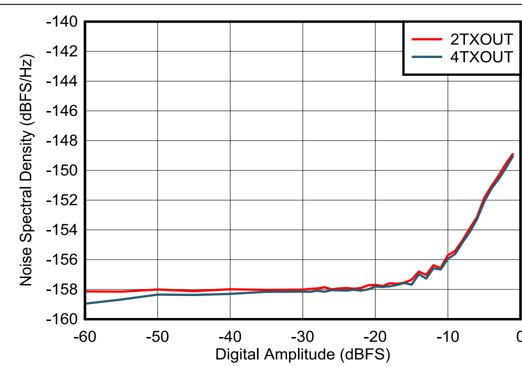
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

Figure 4-439. IMD3 vs Digital Amplitude and Temperature at 2.6GHz



f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

Figure 4-440. IMD3 vs Digital Amplitude and Dither at 2.6GHz

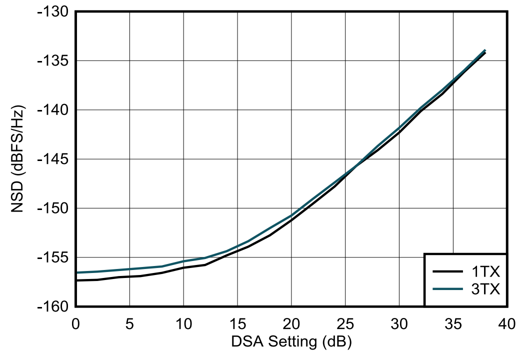


f_{DAC} = 9000MSPS, non-interleave mode, external clock mode, 50MHz offset

Figure 4-441. NSD vs Digital Amplitude and Channel at 2.6GHz

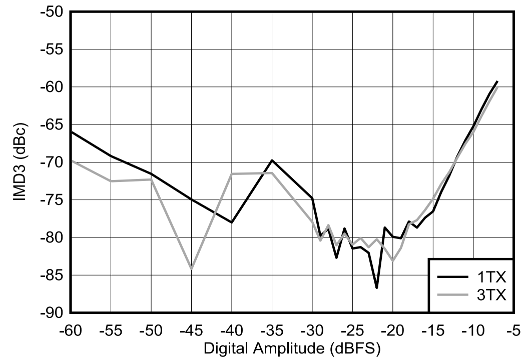
4.12.11 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



f_{DAC} = 9000MSPS, non-interleave mode, external clock mode, 50MHz offset

Figure 4-442. NSD vs Digital Amplitude and Temperature at 2.6GHz

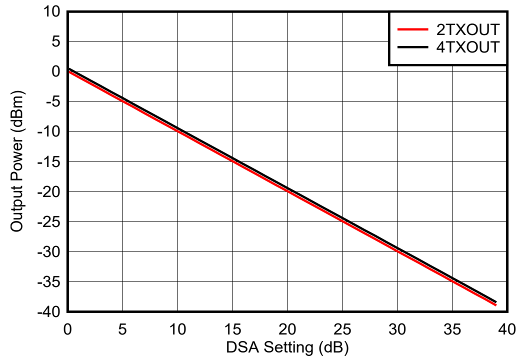


f_{DAC} = f_{CLK} = 9000MSPS, non-interleave mode

Figure 4-443. External Clock Additive Phase Noise at 2.6GHz

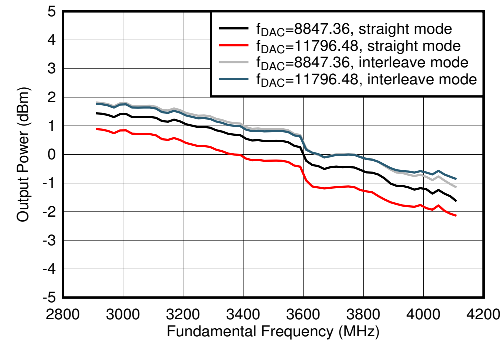
4.12.12 TX Typical Characteristics at 3.5GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



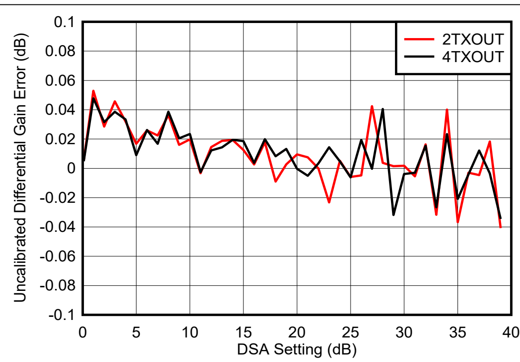
A_{out} = -0.5dBFS, 3.5GHz Matching, included PCB and cable losses

Figure 4-444. TX Output Power vs DSA Setting at 3.5GHz



A_{out} = -0.5dBFS, 3.5GHz Matching, included PCB and cable losses

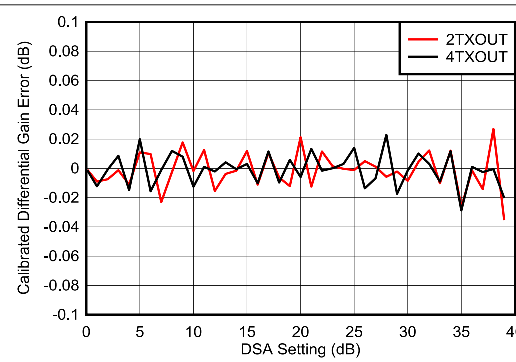
Figure 4-445. TX Output Power vs Frequency



3.5GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

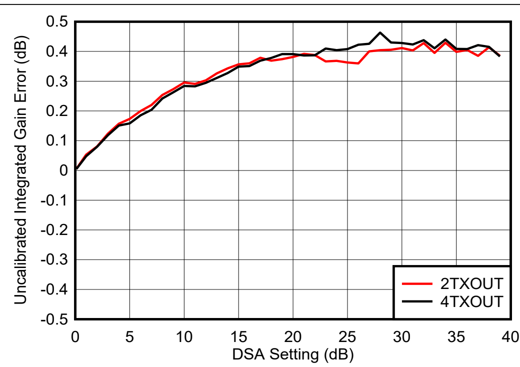
Figure 4-446. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5GHz



3.5GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

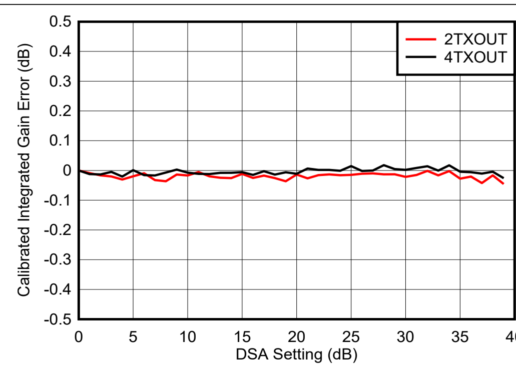
Figure 4-447. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5GHz



3.5GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-448. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5GHz



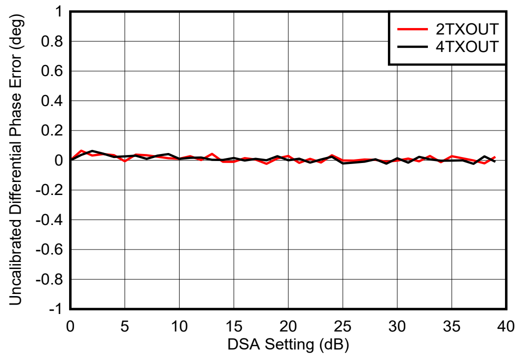
3.5GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-449. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5GHz

4.12.12 TX Typical Characteristics at 3.5GHz (continued)

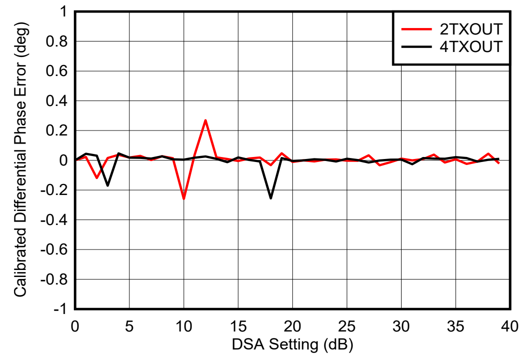
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



3.5GHz Matching, included PCB and cable losses

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

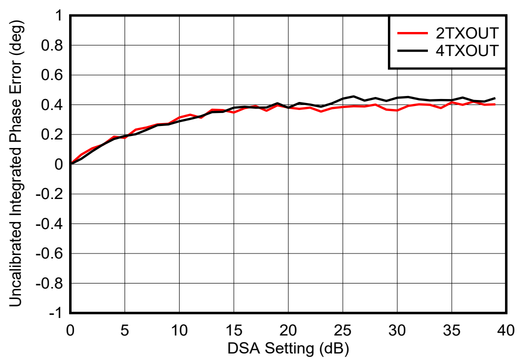
Figure 4-450. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5GHz



3.5GHz Matching, included PCB and cable losses

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting). Phase DNL spike may occur at any DSA setting.

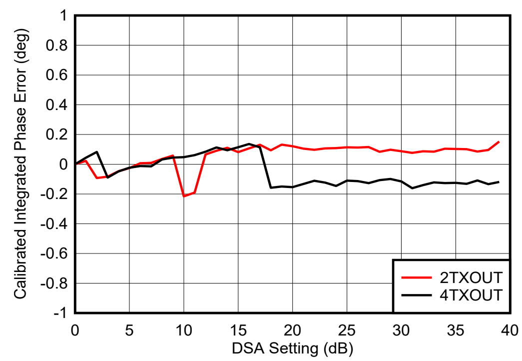
Figure 4-451. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5GHz



3.5GHz Matching, included PCB and cable losses

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-452. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5GHz



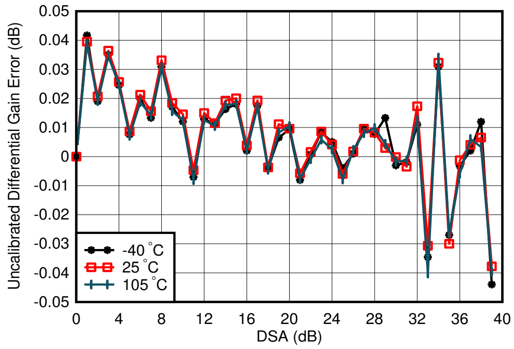
3.5GHz Matching, included PCB and cable losses

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-453. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5GHz

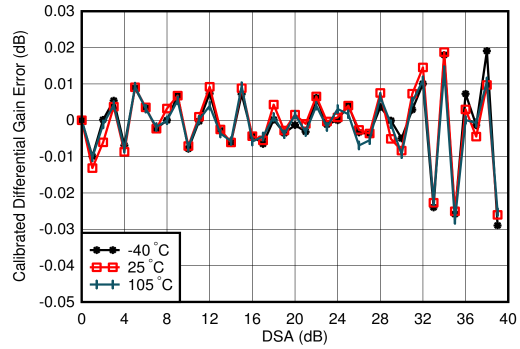
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



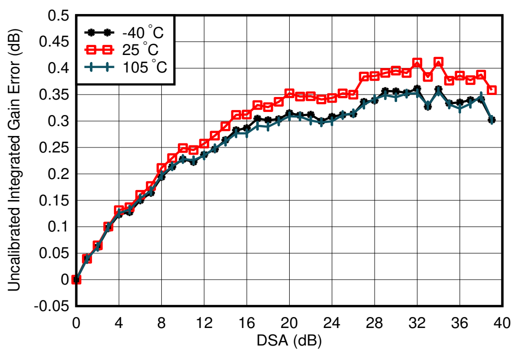
3.5GHz Matching, 1TX
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-454. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5GHz



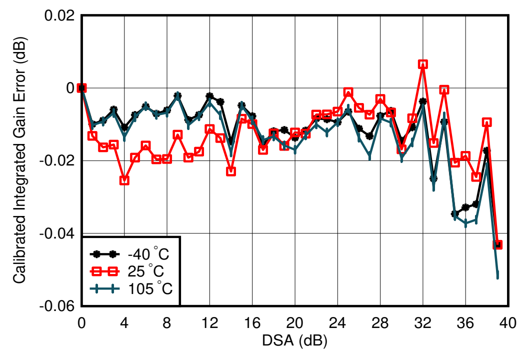
3.5GHz Matching, 1TX, Calibrated at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-455. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5GHz



3.5GHz Matching, 1TX
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-456. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5GHz

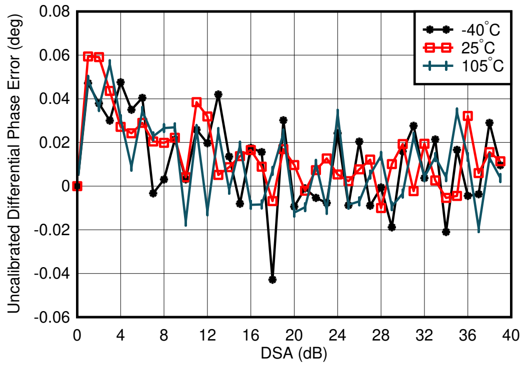


3.5GHz Matching, 1TX, Calibrated at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-457. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5GHz

4.12.12 TX Typical Characteristics at 3.5GHz (continued)

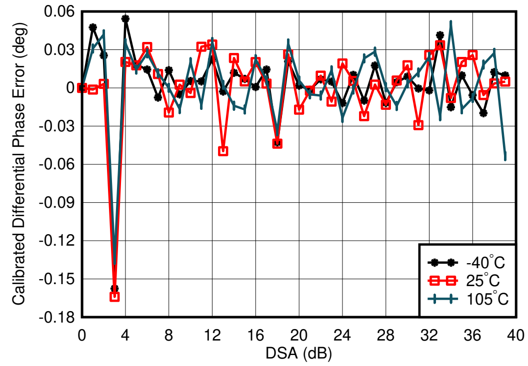
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



3.5GHz Matching, 1TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

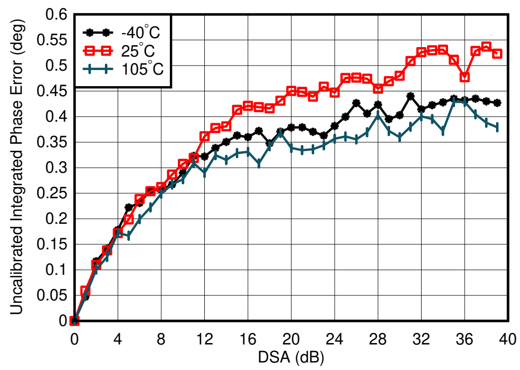
Figure 4-458. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5GHz



3.5GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

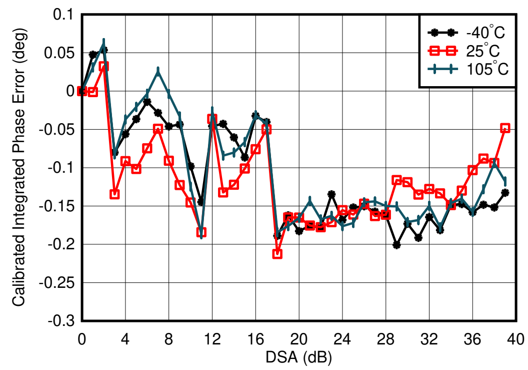
Figure 4-459. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5GHz



3.5GHz Matching, 1TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

Figure 4-460. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5GHz



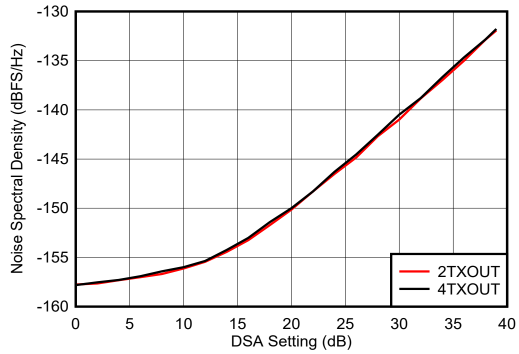
3.5GHz Matching, 1TX, Calibrated at 25°C

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-461. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5GHz

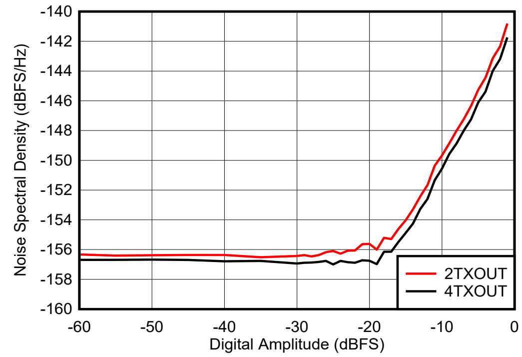
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



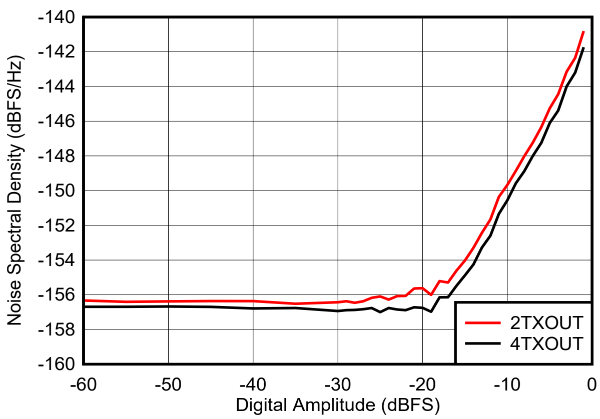
f_{DAC} = 11796.48MSPS, interleave mode, matching at 3.5GHz, A_{out} = –13dBFS.

Figure 4-462. TX NSD vs DSA Setting at 3.5GHz



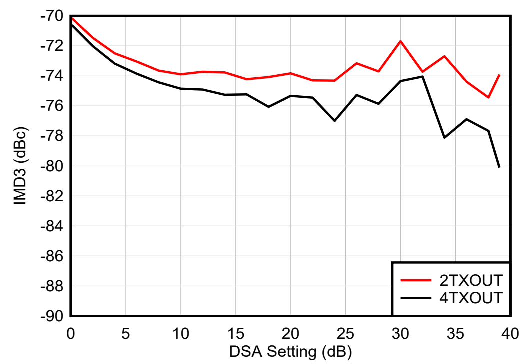
f_{DAC} = 12MSPS, external clock mode, non-interleave mode

Figure 4-463. TX NSD vs Digital Amplitude and Temperature at 3.75GHz



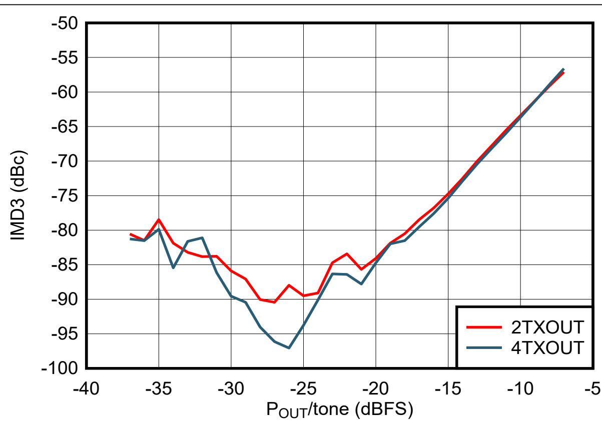
f_{DAC} = 12MSPS, external clock mode, non-interleave mode

Figure 4-464. TX NSD vs Digital Amplitude and Channel at 3.75GHz



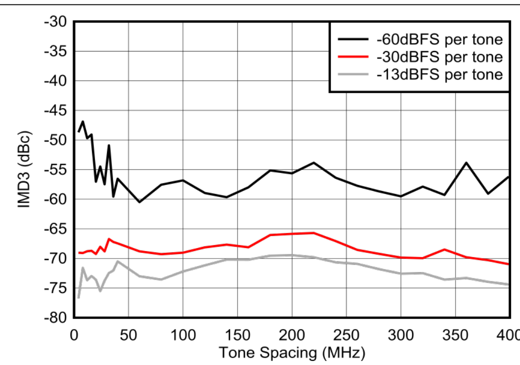
20MHz tone spacing, 3.5GHz Matching, –13dBFS each tone, included PCB and cable losses

Figure 4-465. TX IMD3 vs DSA Setting at 3.5GHz



20MHz tone spacing, 3.5GHz Matching

Figure 4-466. TX IMD3 vs Digital Amplitude and Channel at 3.5GHz

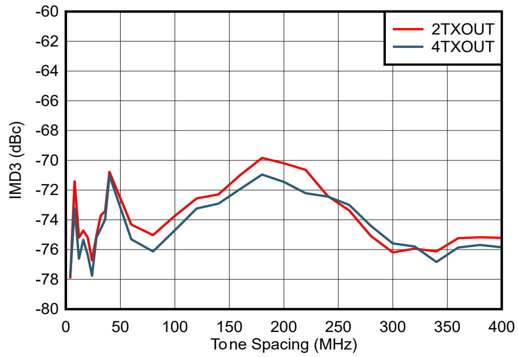


50MHz tone spacing, external clock mode, non-interleave mode

Figure 4-467. TX IMD3 vs Tone Spacing and Amplitude at 3.75GHz

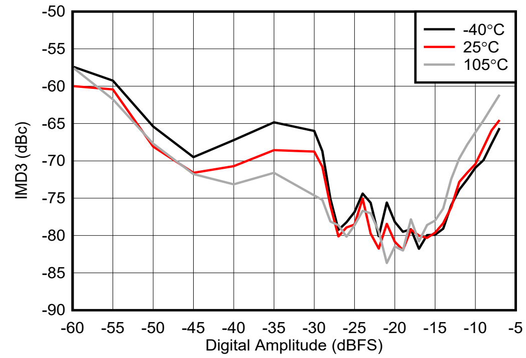
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



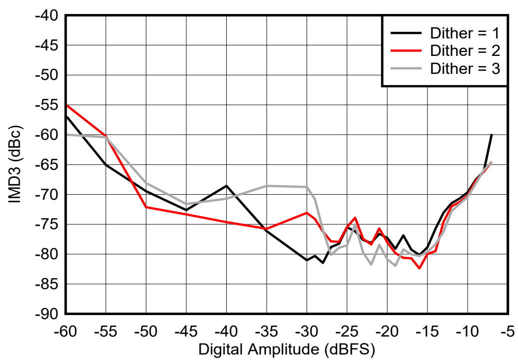
50MHz tone spacing, external clock mode, non-interleave mode

Figure 4-468. TX IMD3 vs Tone Spacing and Channel at 3.75GHz



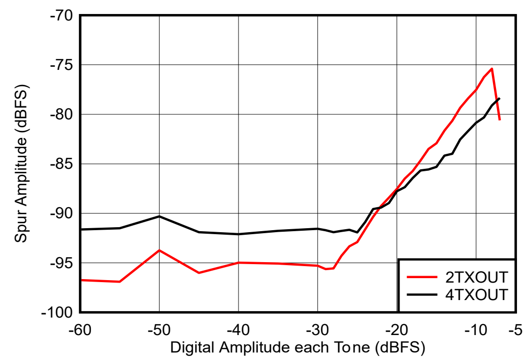
50MHz tone spacing, external clock mode, non-interleave mode

Figure 4-469. TX IMD3 vs Digital Amplitude and Temperature at 3.75GHz



50MHz tone spacing, external clock mode, non-interleave mode

Figure 4-470. TX IMD3 vs Digital Amplitude and Dither at 3.75GHz

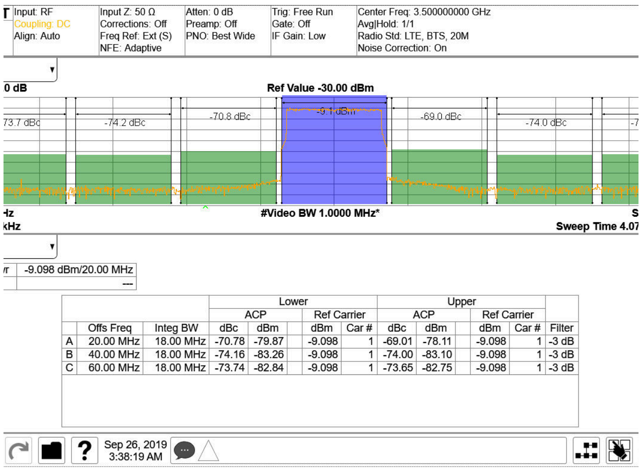


Inband = 3.75GHz ± 600MHz, f_{DAC} = 9GSPS, external clock mode, non-interleave mode.

Figure 4-471. Two Tone Inband SFDR vs Digital Amplitude at 3.75GHz

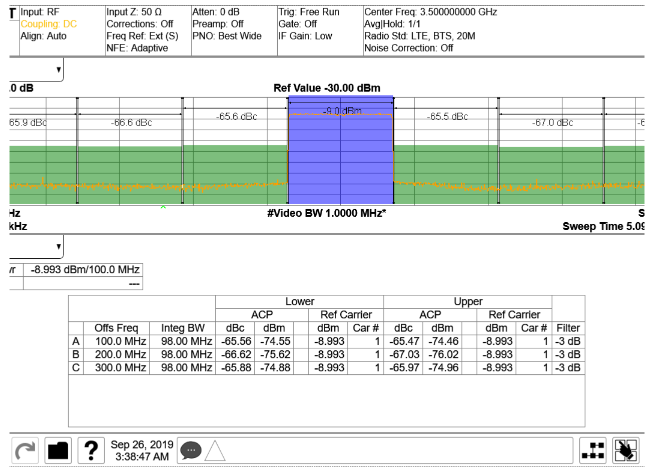
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



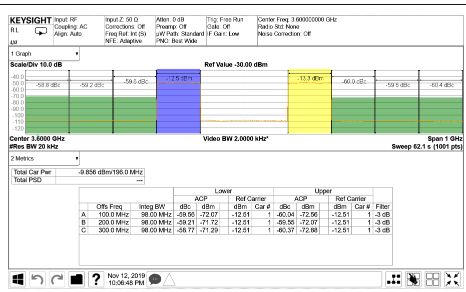
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

Figure 4-472. TX 20MHz LTE Output Spectrum at 3.5GHz (Band 42)



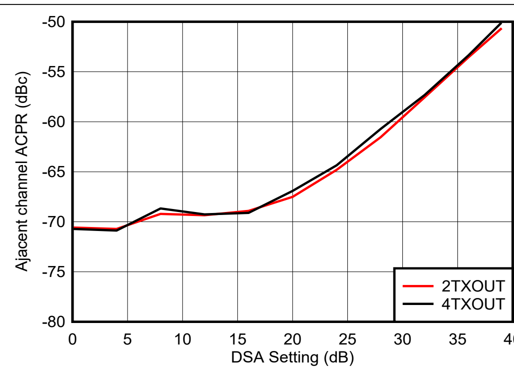
3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-473. TX 100MHz NR Output Spectrum at 3.5GHz (Band 42)



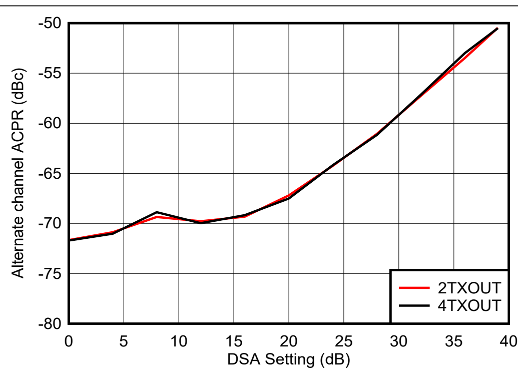
3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-474. TX 2 carrier 100MHz NR Output Spectrum at 3.45GHz and 3.75GHz



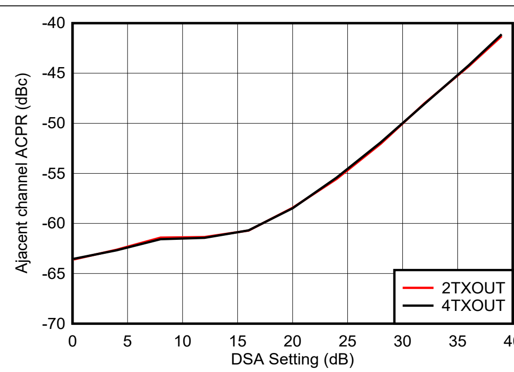
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

Figure 4-475. TX 20MHz LTE ACPR vs DSA Setting at 3.5GHz



3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

Figure 4-476. TX 20MHz LTE alt-ACPR vs DSA Setting at 3.5GHz

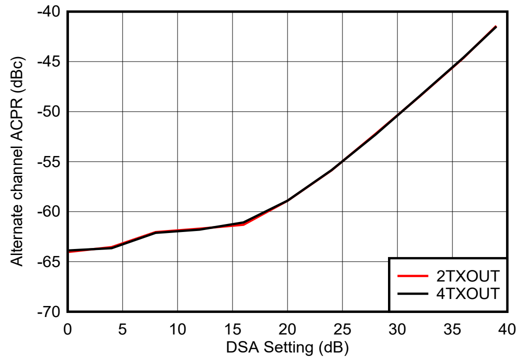


3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-477. TX 100MHz NR ACPR vs DSA Setting at 3.5GHz

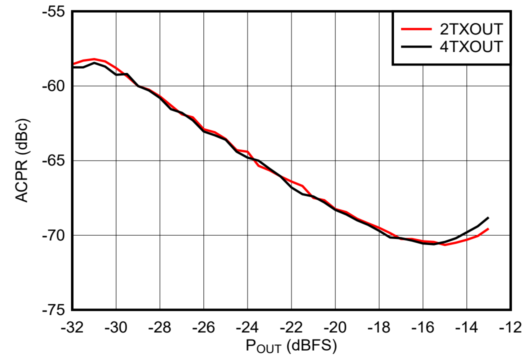
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



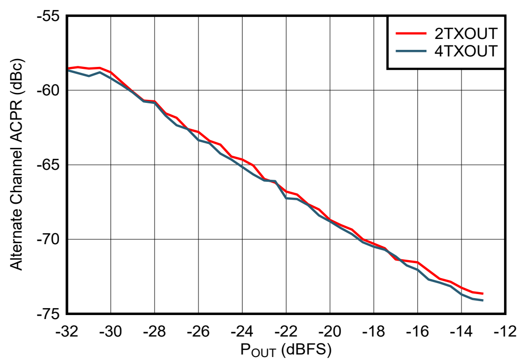
3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-478. TX 100MHz NR alt-ACPR vs DSA Setting at 3.5GHz



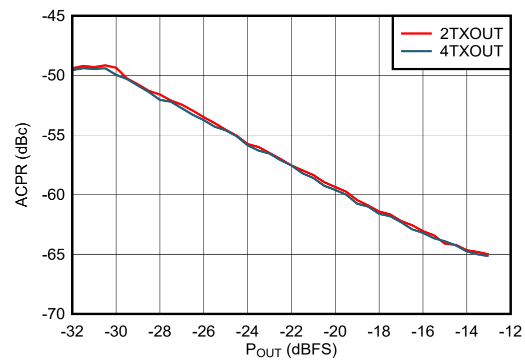
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

Figure 4-479. TX 20MHz LTE ACPR vs Digital Level at 3.5GHz



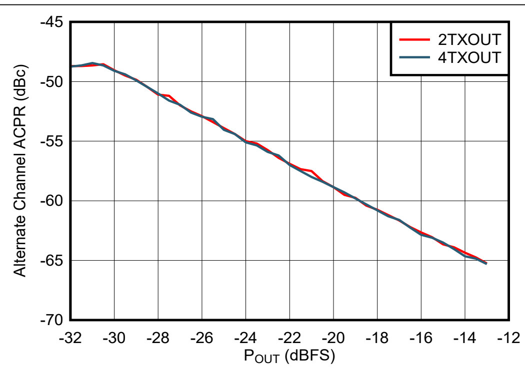
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

Figure 4-480. TX 20MHz LTE alt-ACPR vs Digital Level at 3.5GHz



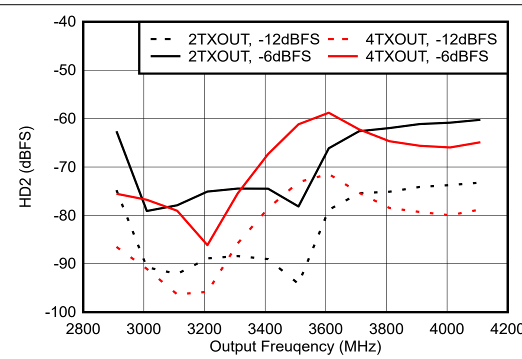
3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-481. TX 100MHz NR ACPR vs Digital Level at 3.5GHz



3.5GHz Matching, single carrier 100MHz BW NR TM1.1

Figure 4-482. TX 100MHz NR alt-ACPR vs Digital Level at 3.5GHz

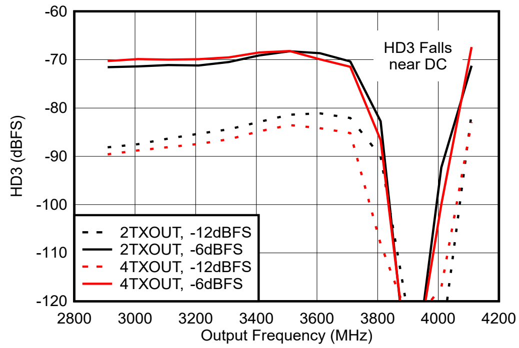


Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-483. TX Single Tone HD2 vs Frequency and Digital Level at 3.5GHz

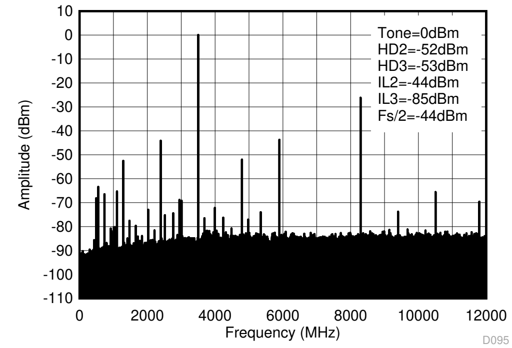
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



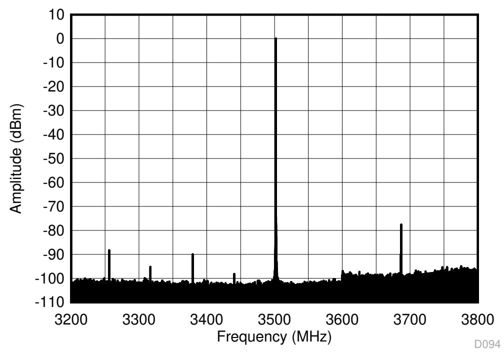
Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 4-484. TX Single Tone HD3 vs Frequency and Digital Level at 3.5GHz



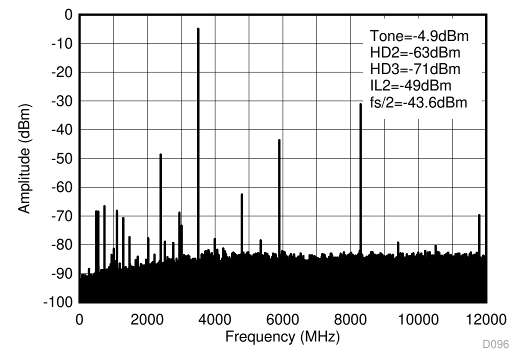
Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-485. TX Single Tone (–1dBFS) Output Spectrum at 3.5GHz (0 - f_{DAC})



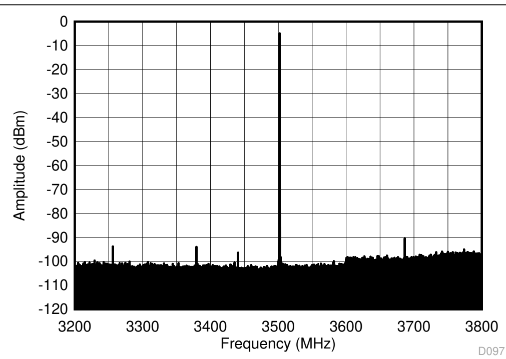
Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-486. TX Single Tone (–1dBFS) Output Spectrum at 3.5GHz (±300MHz)



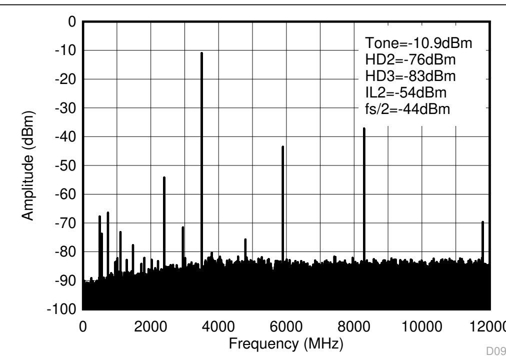
Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-487. TX Single Tone (–6dBFS) Output Spectrum at 3.5GHz (0 - f_{DAC})



Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-488. TX Single Tone (–6dBFS) Output Spectrum at 3.5GHz (±300MHz)

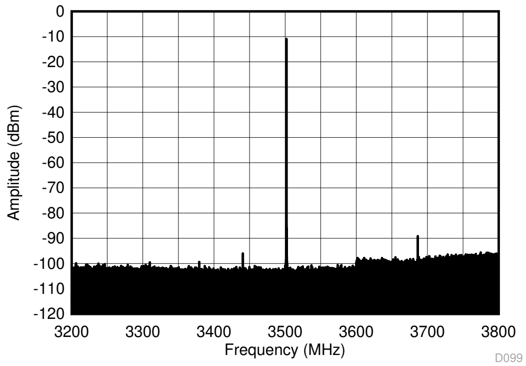


Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-489. TX Single Tone (–12dBFS) Output Spectrum at 3.5GHz (0 - f_{DAC})

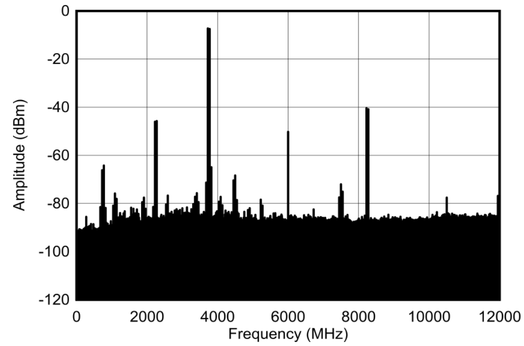
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



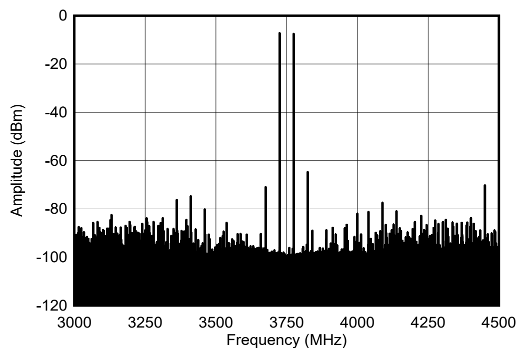
Matching at 3.5GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 4-490. TX Single Tone (–12dBFS) Output Spectrum at 3.5GHz (±300MHz)



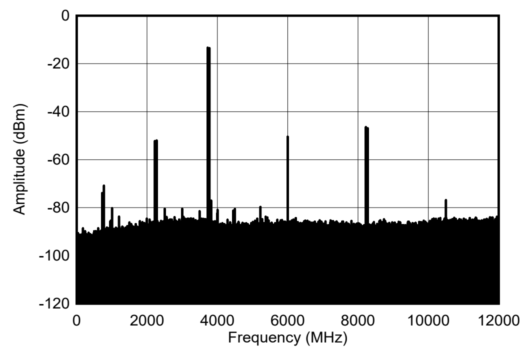
Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-491. TX Dual Tone Output Spectrum at 3.75GHz, -7dBFS each (0 - f_{DAC})



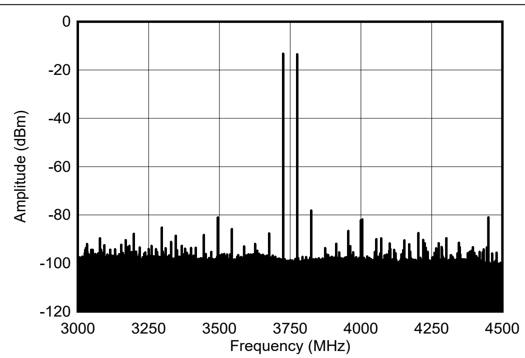
Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-492. TX Dual Tone Output Spectrum at 3.75GHz, -7dBFS each (±600MHz)



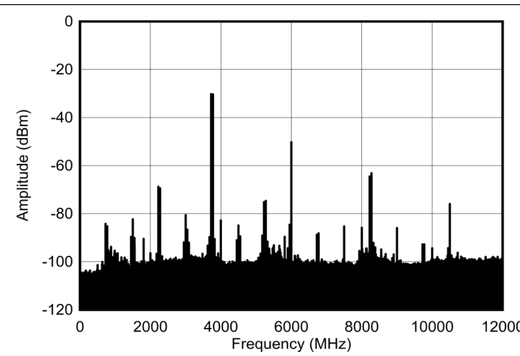
Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-493. TX Dual Tone Output Spectrum at 3.75GHz, -13dBFS each (0 - f_{DAC})



Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-494. TX Dual Tone Output Spectrum at 3.75GHz, -13dBFS each (±600MHz)

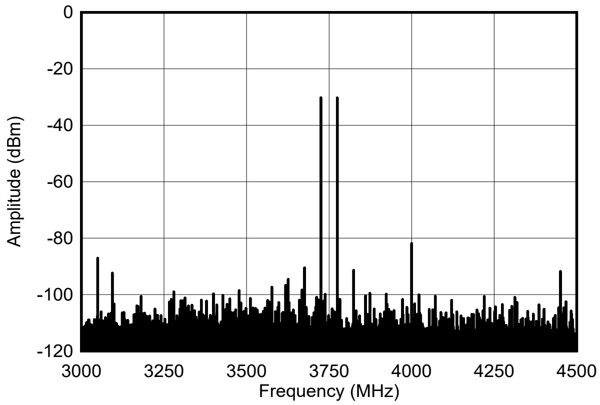


Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-495. TX Dual Tone Output Spectrum at 3.75GHz, -30dBFS each (0 - f_{DAC})

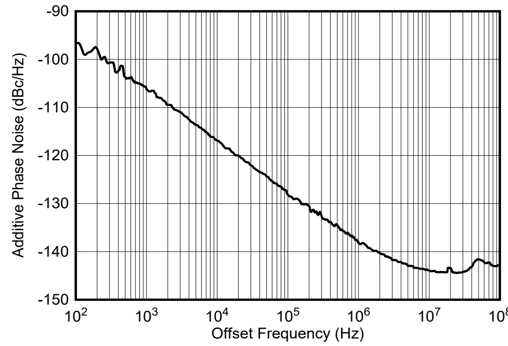
4.12.12 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



Matching at 3.5GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

Figure 4-496. TX Dual Tone Output Spectrum at 3.75GHz, -30dBFS each (±600MHz)

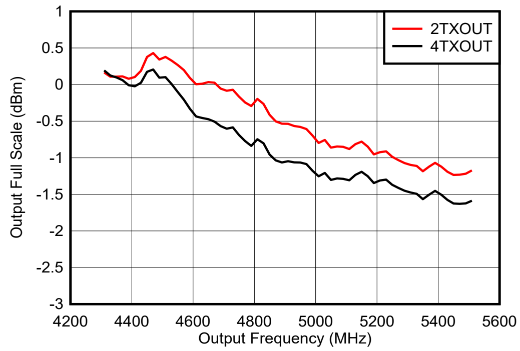


f_{DAC} = f_{CLK} = 12GSPS, non-interleave mode.

Figure 4-497. External Clock Additive Phase Noise at 3.7GHz

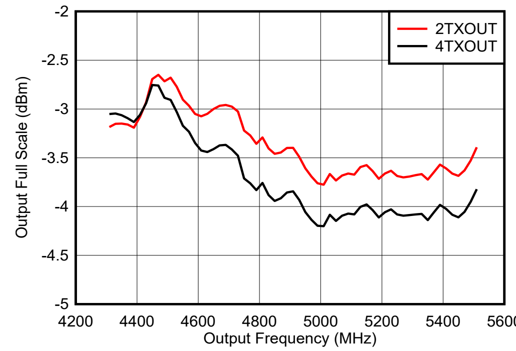
4.12.13 TX Typical Characteristics at 4.9GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



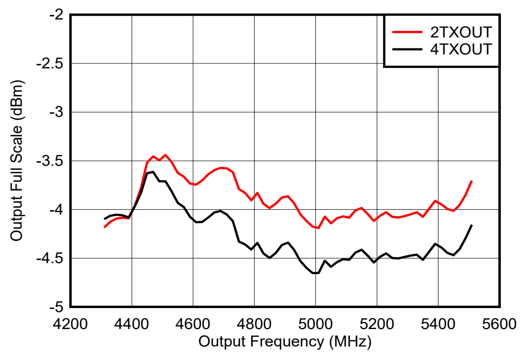
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9GHz matching

Figure 4-498. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS



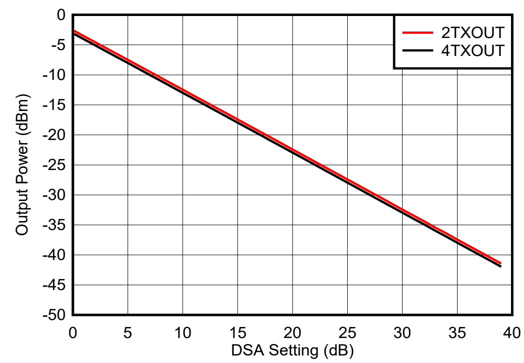
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9GHz matching

Figure 4-499. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Mixed Mode, 2nd Nyquist Zone



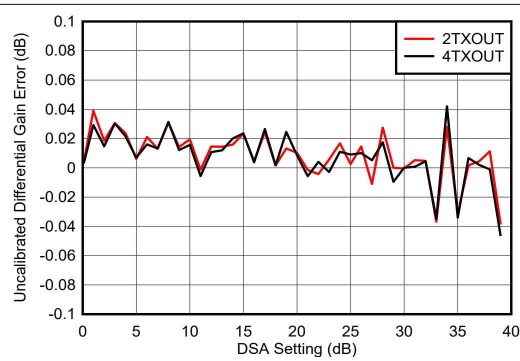
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9GHz matching

Figure 4-500. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Mixed Mode, 2nd Nyquist Zone



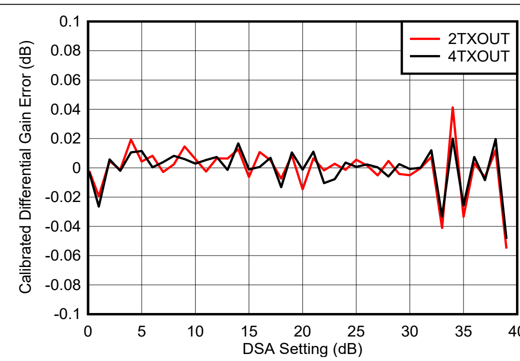
f_{DAC} = 11796.48MSPS, A_{out} = -0.5dBFS, matching 4.9GHz

Figure 4-501. TX Output Power vs DSA Setting and Channel at 4.9GHz



f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-502. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9GHz

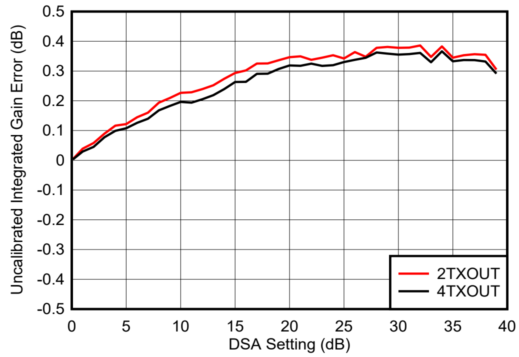


f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-503. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9GHz

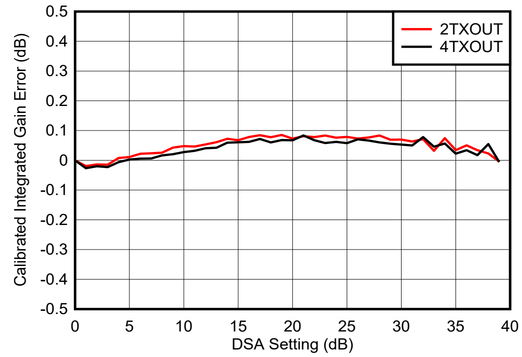
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



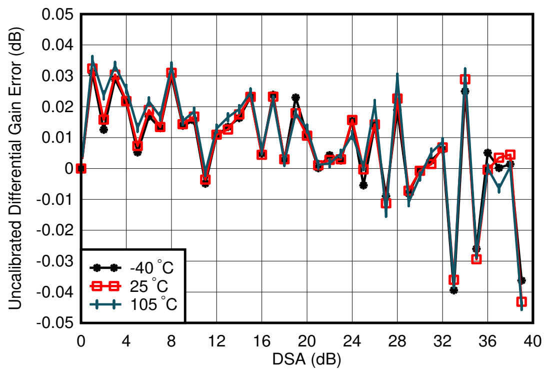
f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-504. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9GHz



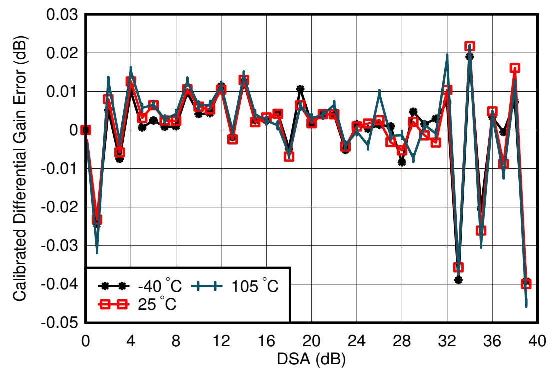
f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-505. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-506. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9GHz

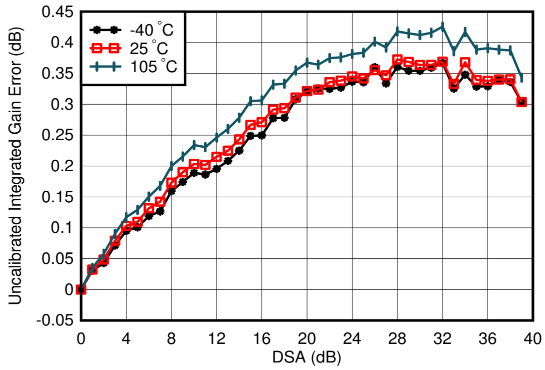


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 4-507. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9GHz

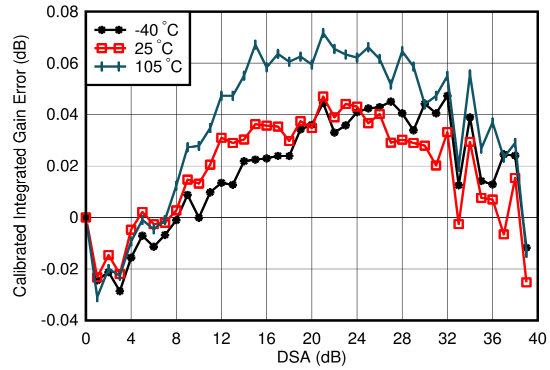
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



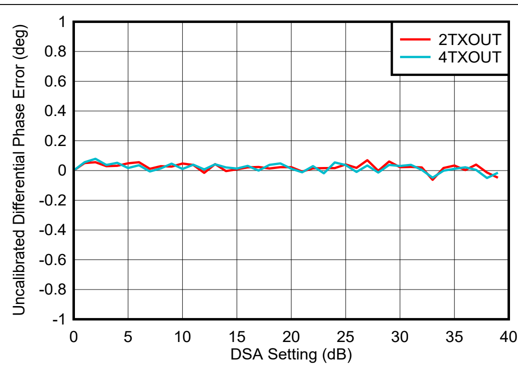
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-508. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9GHz



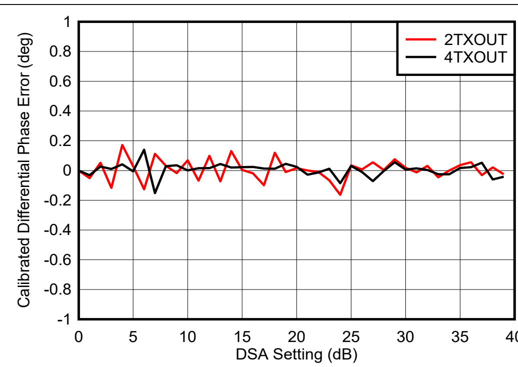
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 4-509. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-510. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9GHz

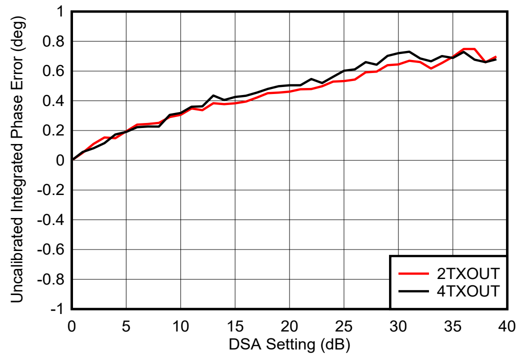


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 4-511. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9GHz

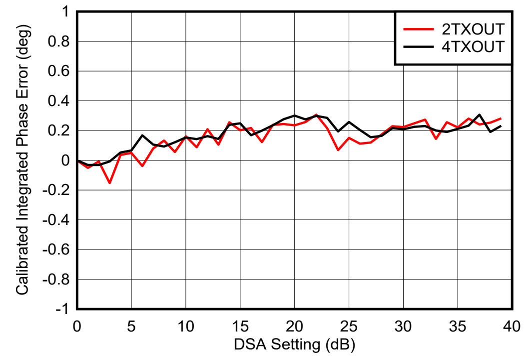
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



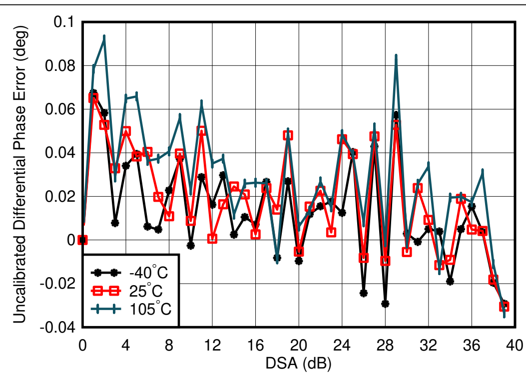
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-512. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9GHz



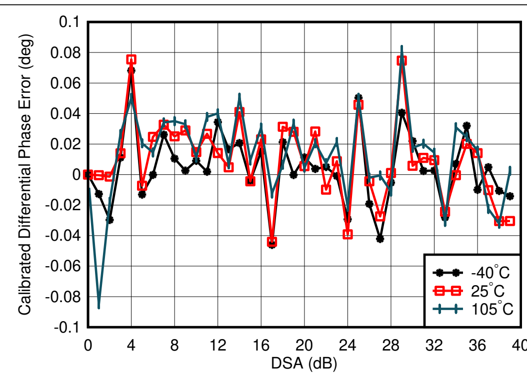
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-513. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-514. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9GHz

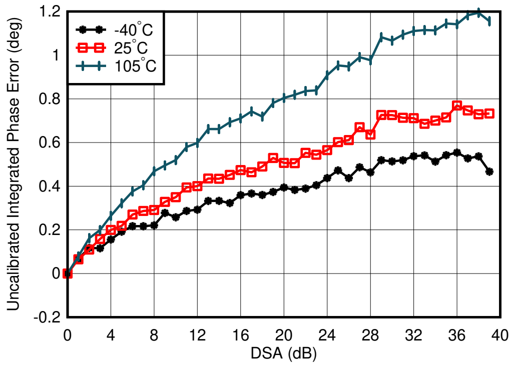


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 4-515. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9GHz

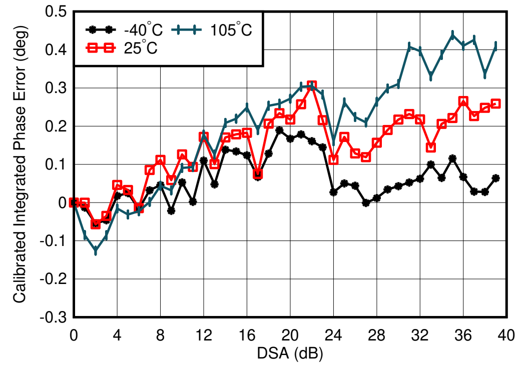
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



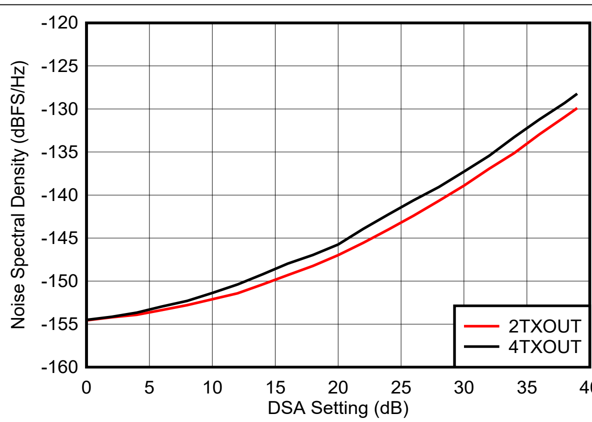
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-516. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9GHz



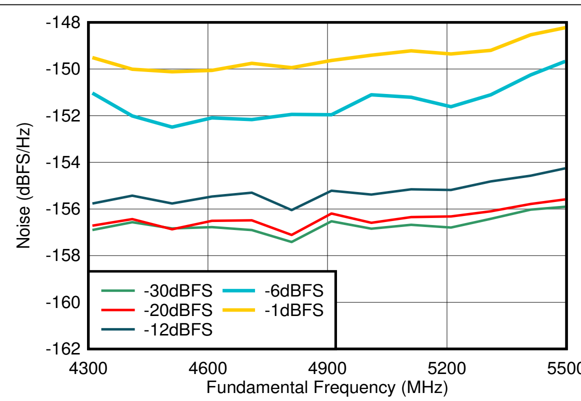
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-517. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz, P_{OUT} = –13dBFS

Figure 4-518. TX Output Noise vs DSA Setting and Channel at 4.9GHz

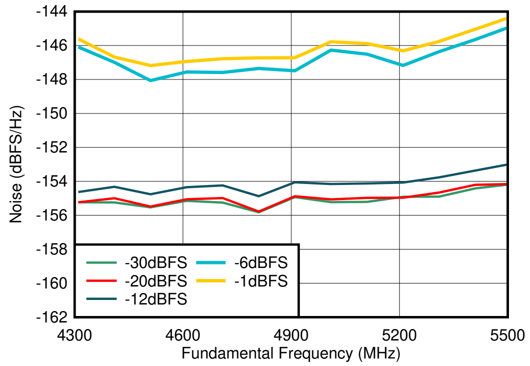


f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz, A_{out} = –13dBFS.

Figure 4-519. TX NSD vs Output Frequency and Digital Amplitude at 4.9GHz (DSA = 0dB)

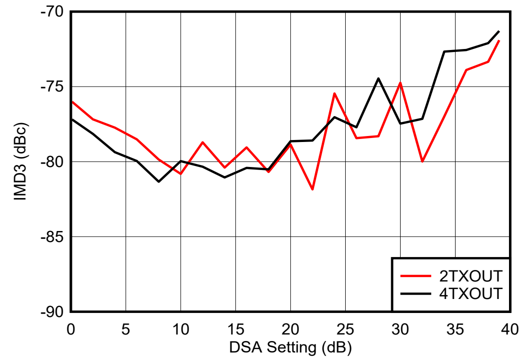
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



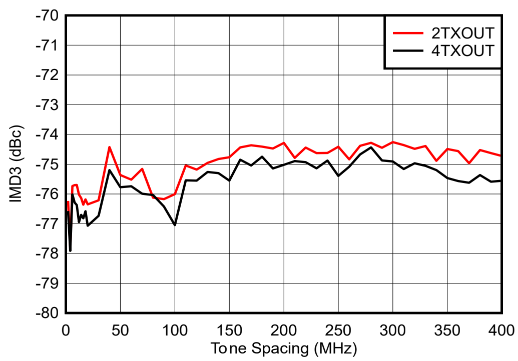
f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9GHz, A_{out} = –13dBFS.

Figure 4-520. TX NSD vs Output Frequency and Digital Amplitude at 4.9GHz (DSA = 6dB)



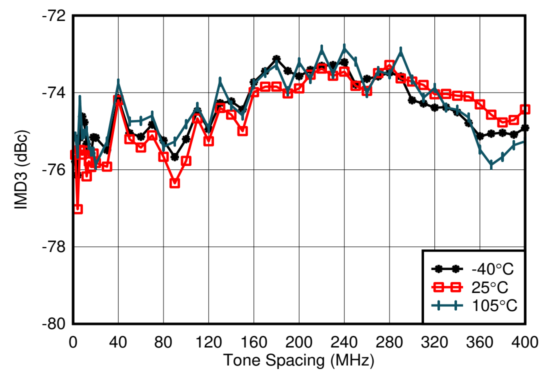
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz, f_{CENTER} = 4.9GHz, -13dBFS each tone

Figure 4-521. TX IMD3 vs DSA Setting at 4.9GHz



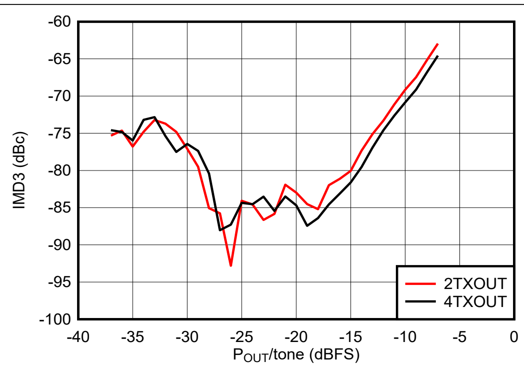
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz, f_{CENTER} = 4.9GHz, –13dBFS each tone

Figure 4-522. TX IMD3 vs Tone Spacing and Channel at 4.9GHz



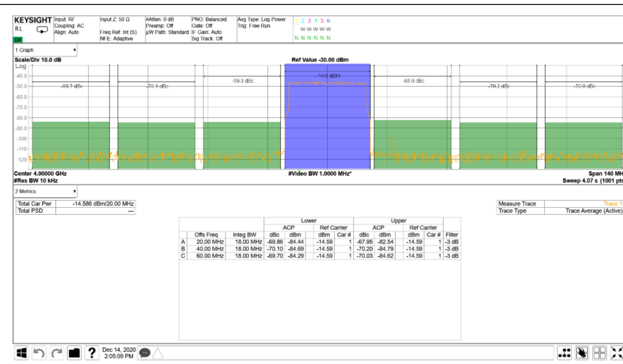
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz, f_{CENTER} = 4.9GHz, –13dBFS each tone, worst channel

Figure 4-523. TX IMD3 vs Tone Spacing and Temperature at 4.9GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9GHz, f_{CENTER} = 4.9GHz, $f_{SPACING}$ = 20MHz

Figure 4-524. TX IMD3 vs Digital Level at 4.9GHz

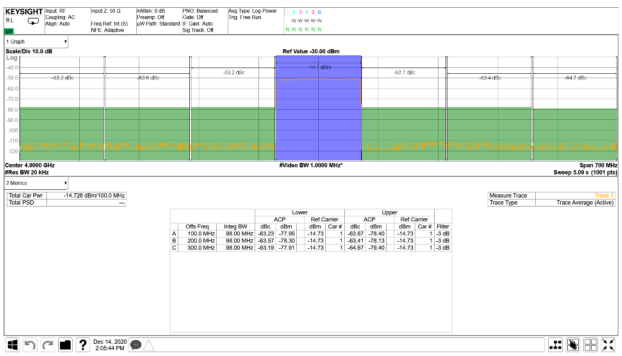


TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-525. TX 20MHz LTE Output Spectrum at 4.9GHz

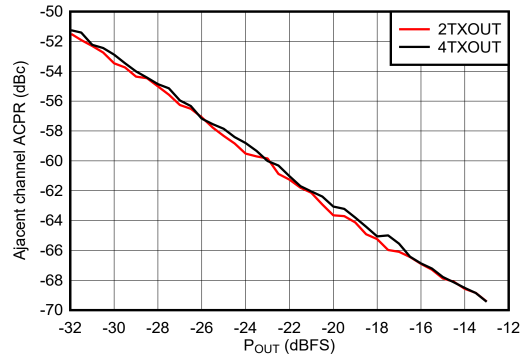
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



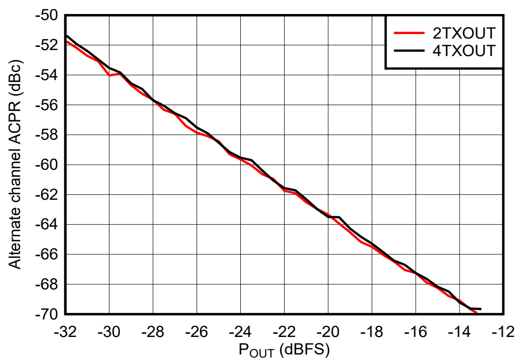
TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-526. TX 100MHz NR Output Spectrum at 4.9GHz



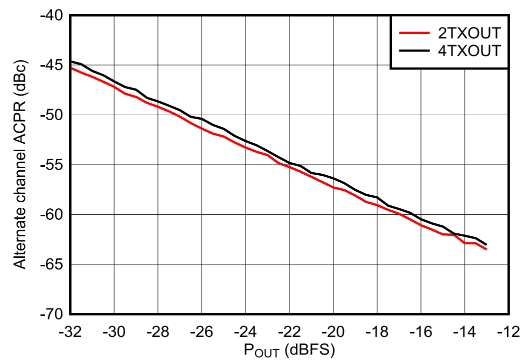
Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-527. TX 20MHz LTE ACPR vs Digital Level at 4.9GHz



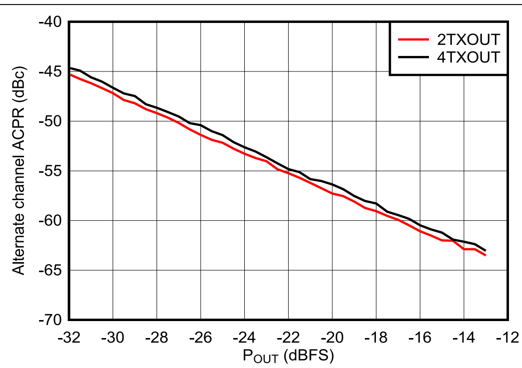
Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-528. TX 20MHz LTE alt-ACPR vs Digital Level at 4.9GHz



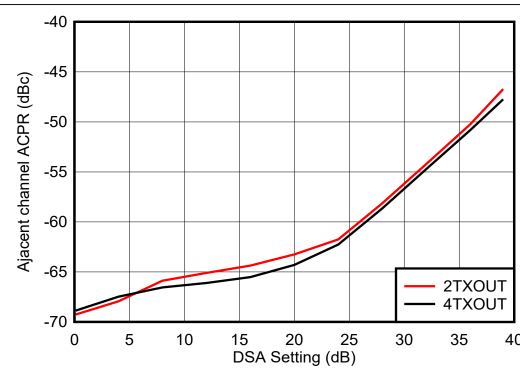
Matching at 4.9GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-529. TX 100MHz NR ACPR vs Digital Level at 4.9GHz



Matching at 4.9GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-530. TX 100MHz NR alt-ACPR vs Digital Level at 4.9GHz

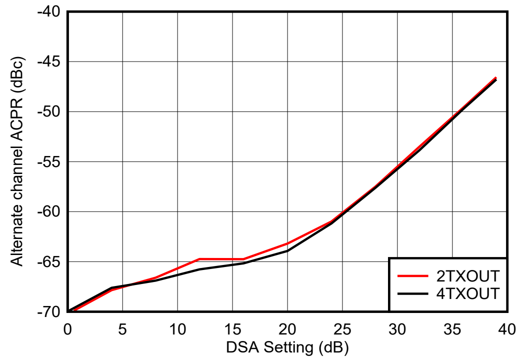


Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-531. TX 20MHz LTE ACPR vs DSA at 4.9GHz

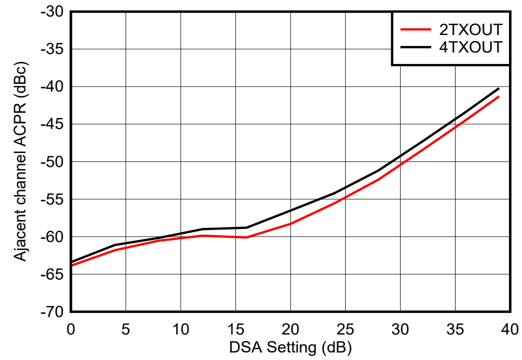
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



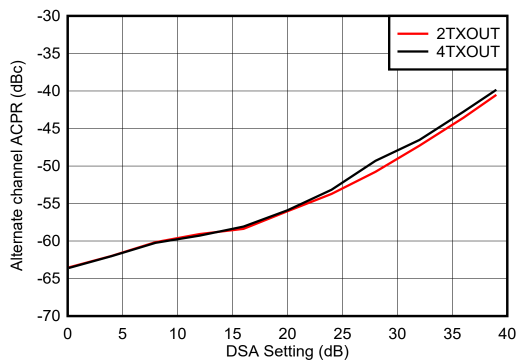
Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-532. TX 20MHz LTE alt-ACPR vs DSA at 4.9GHz



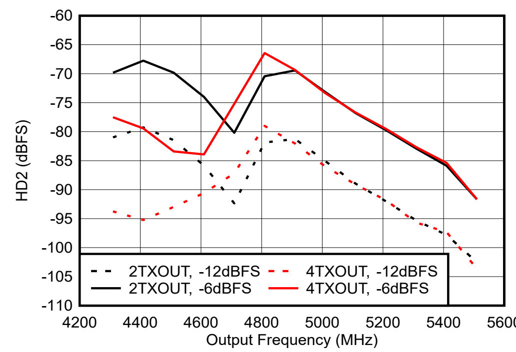
Matching at 4.9GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-533. TX 100MHz NR ACPR vs DSA at 4.9GHz



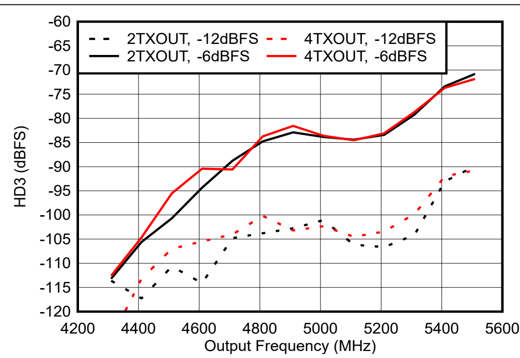
Matching at 4.9GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-534. TX 100MHz NR alt-ACPR vs DSA at 4.9GHz



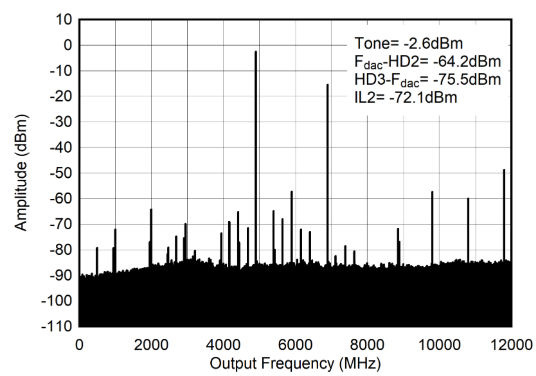
Matching at 4.9GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-535. TX HD2 vs Digital Amplitude and Output Frequency at 4.9GHz



Matching at 4.9GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 4-536. TX HD3 vs Digital Amplitude and Output Frequency at 4.9GHz

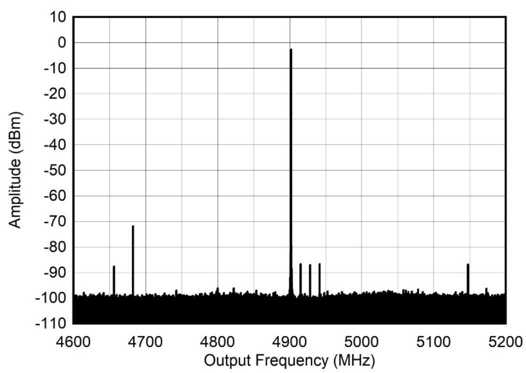


f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-537. TX Single Tone (–1dBFS) Output Spectrum at 4.9GHz (0-f_{DAC})

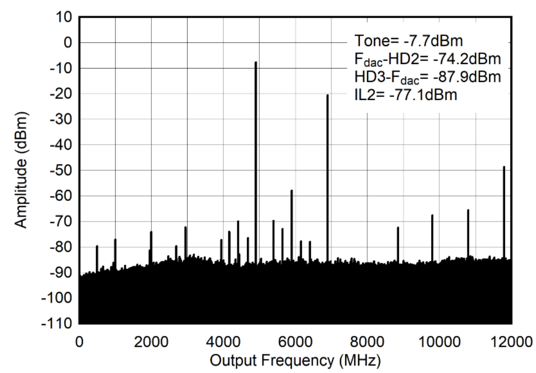
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



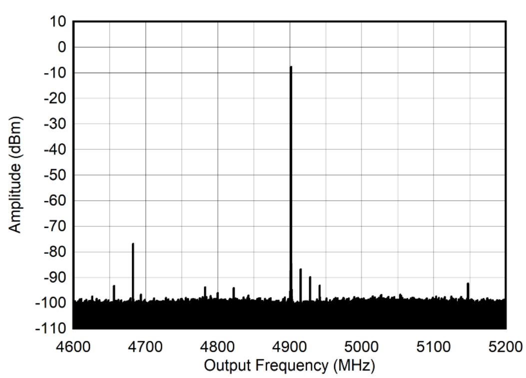
f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses

Figure 4-538. TX Single Tone (–1dBFS) Output Spectrum at 4.9GHz (±300MHz)



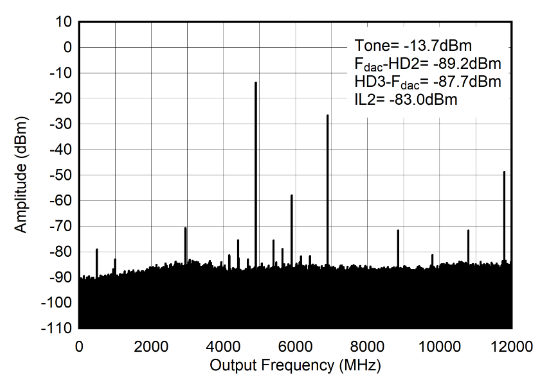
f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-539. TX Single Tone (–6dBFS) Output Spectrum at 4.9GHz (0-f_{DAC})



f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses

Figure 4-540. TX Single Tone (–6dBFS) Output Spectrum at 4.9GHz (±300MHz)

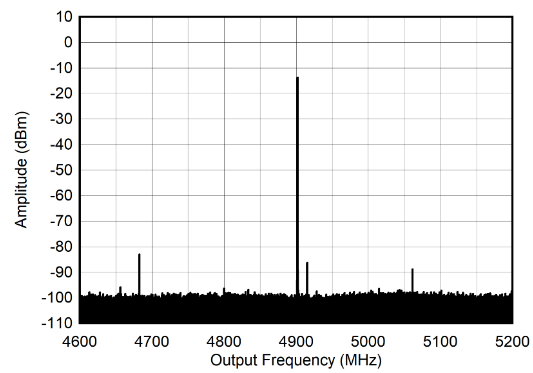


f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

Figure 4-541. TX Single Tone (–12dBFS) Output Spectrum at 4.9GHz (0-f_{DAC})

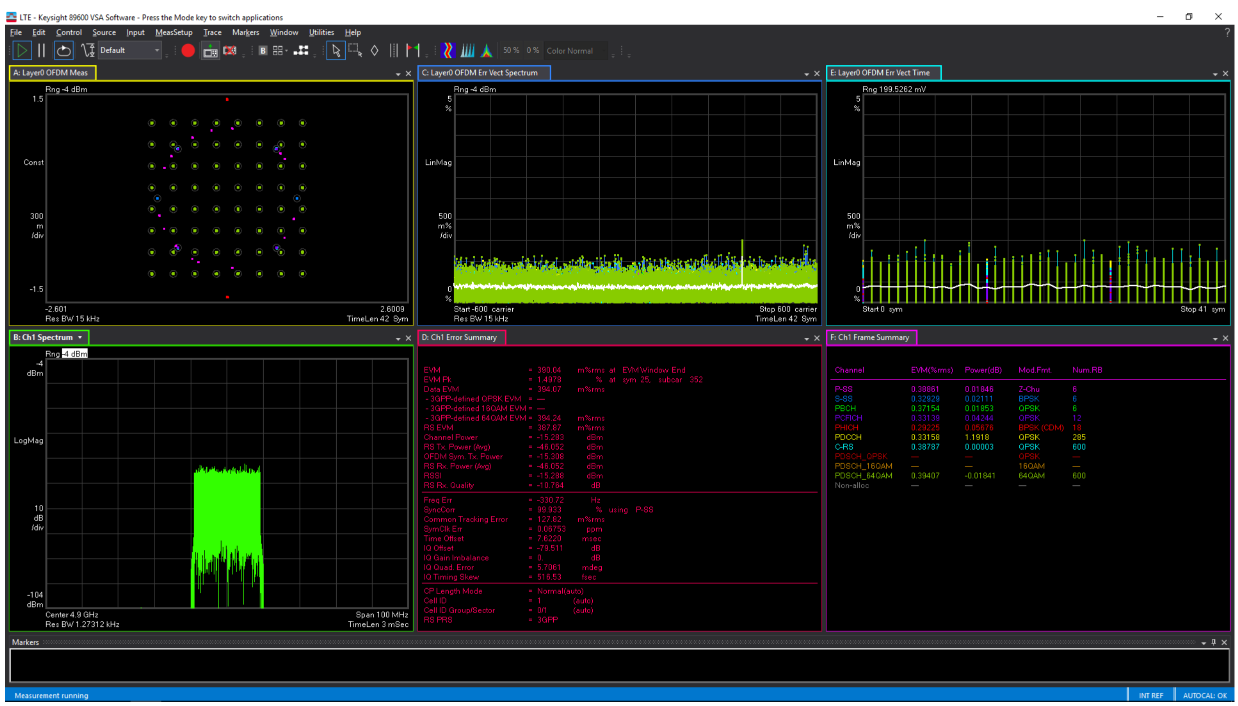
4.12.13 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated



f_{DAC} = 11796.48MSPS, interleave mode, 4.9GHz matching, includes PCB and cable losses

Figure 4-542. TX Single Tone (–12dBFS) Output Spectrum at 4.9GHz (±300MHz)

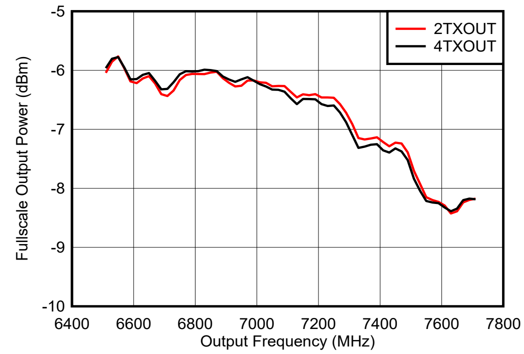


TM1.1, P_{OUT_RMS} = –13dBFS

Figure 4-543. TX 20MHz LTE Error Vector Magnitude at 4.9GHz

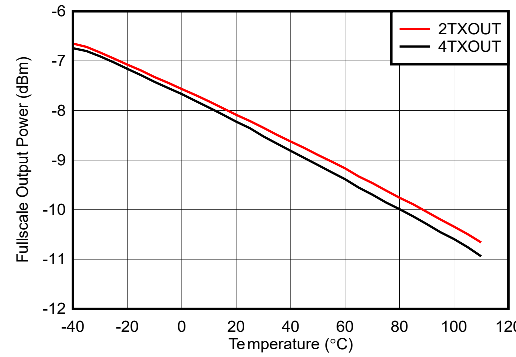
4.12.14 TX Typical Characteristics at 7.1GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2^{nd} Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



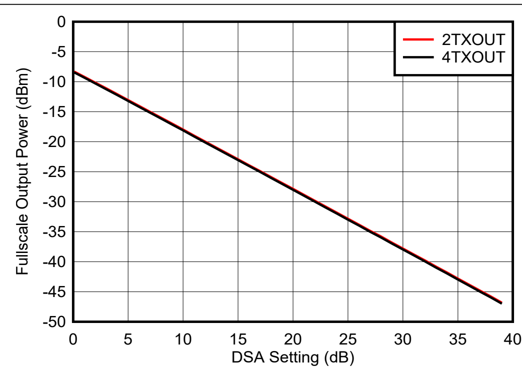
Excluding PCB and cable losses

Figure 4-544. TX Full Scale vs RF Frequency and Channel



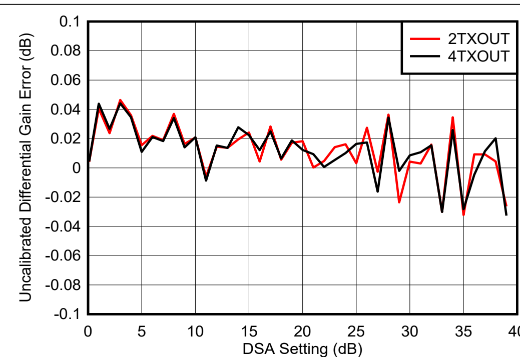
Excluding PCB and cable losses

Figure 4-545. TX Full Scale vs Temperature and Channel at 7.1GHz



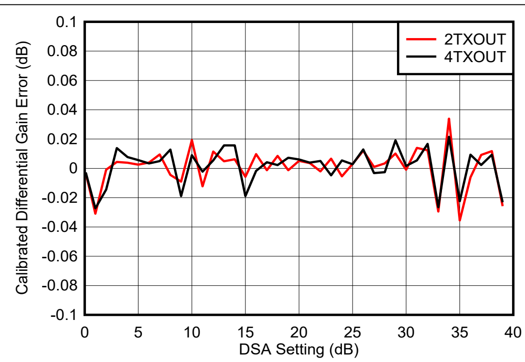
Excluding PCB and cable losses

Figure 4-546. TX Full Scale vs DSA Setting and Channel at 7.1GHz



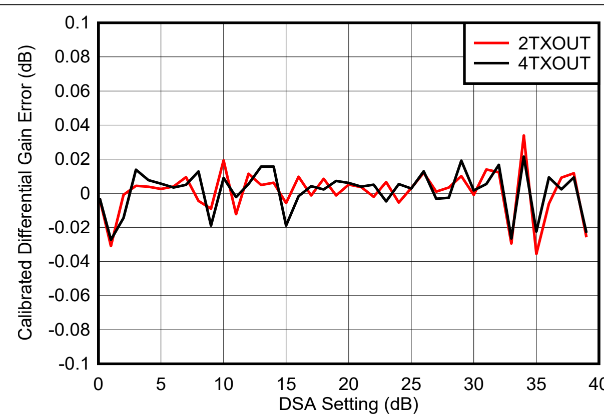
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 4-547. Uncalibrated Differential Gain Error vs Channel at 7.1GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 4-548. Uncalibrated Differential Gain Error vs Temperature at 7.1GHz

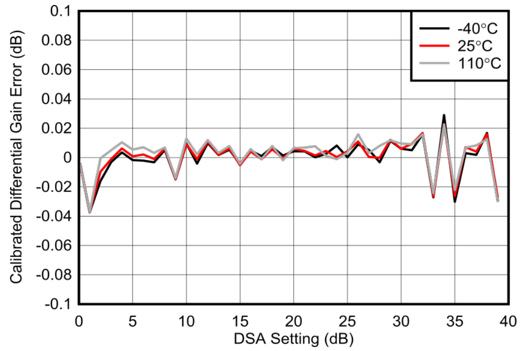


Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 4-549. Calibrated Differential Gain Error vs Channel at 7.1GHz

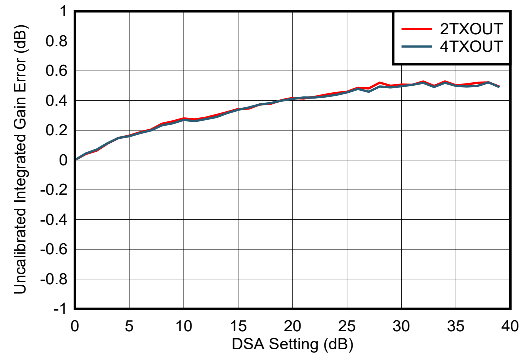
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



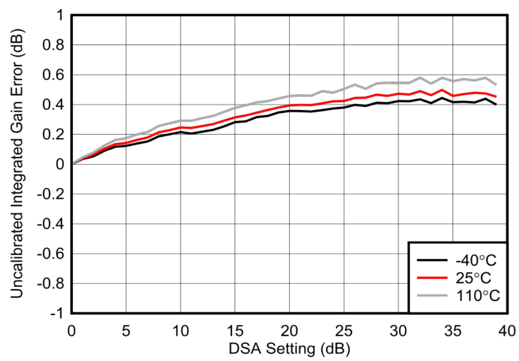
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 4-550. Calibrated Differential Gain Error vs Temperature at 7.1GHz



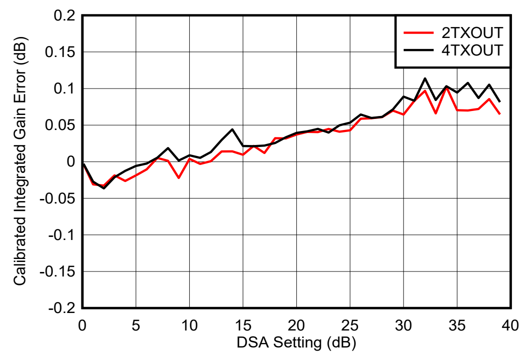
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 4-551. Uncalibrated Integrated Gain Error vs Channel at 7.1GHz



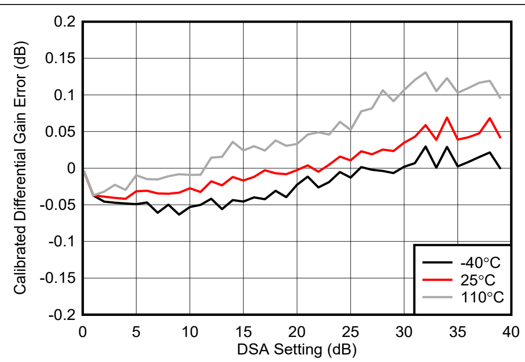
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 4-552. Uncalibrated Integrated Gain Error vs Temperature at 7.1GHz



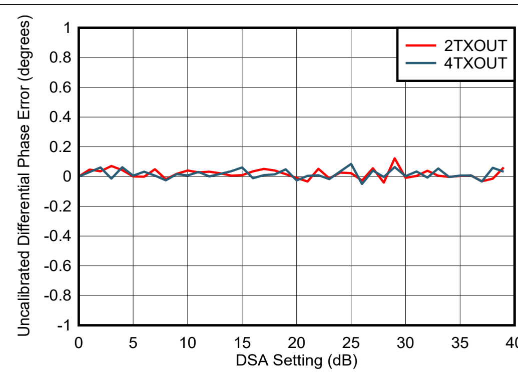
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 4-553. Calibrated Integrated Gain Error vs Channel at 7.1GHz



Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

Figure 4-554. Calibrated Integrated Gain Error vs Temperature at 7.1GHz

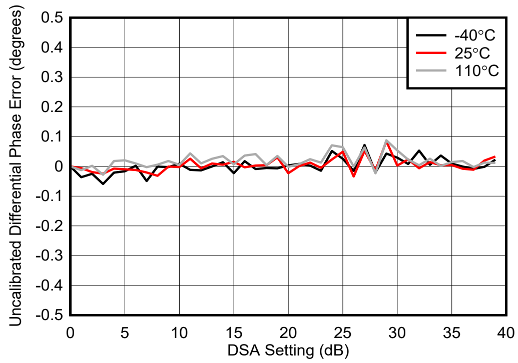


Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 4-555. Uncalibrated Differential Phase Error vs Channel at 7.1GHz

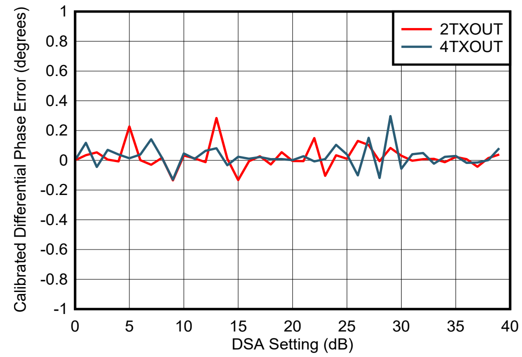
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



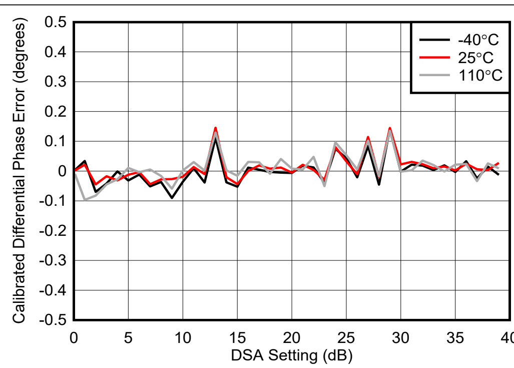
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 4-556. Uncalibrated Differential Phase Error vs Temperature at 7.1GHz



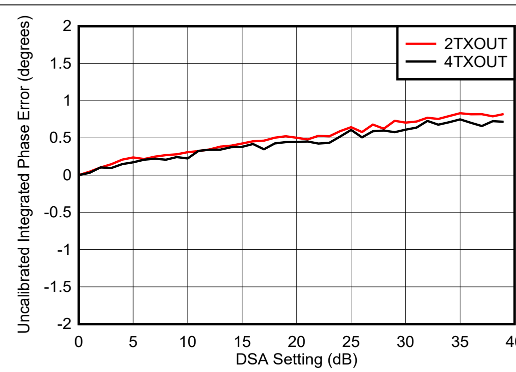
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 4-557. Calibrated Differential Phase Error vs Channel at 7.1GHz



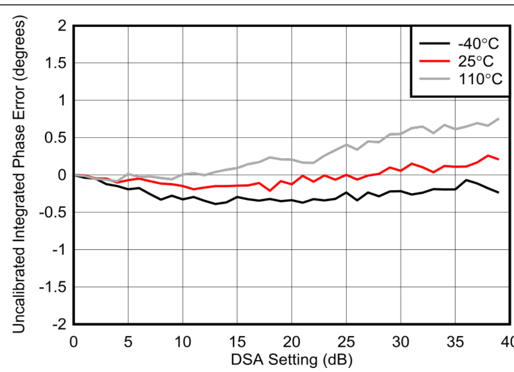
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

Figure 4-558. Calibrated Differential Phase Error vs Temperature at 7.1GHz



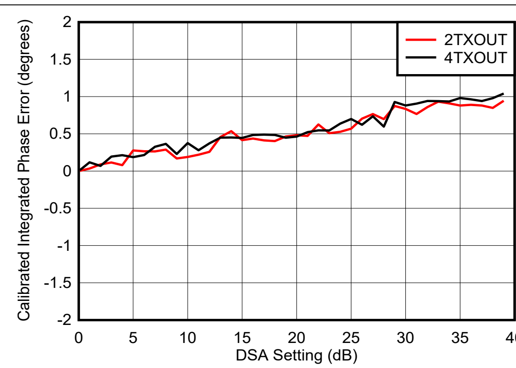
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-559. Uncalibrated Integrated Phase Error vs Channel at 7.1GHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-560. Uncalibrated Integrated Phase Error vs Temperature at 7.1GHz

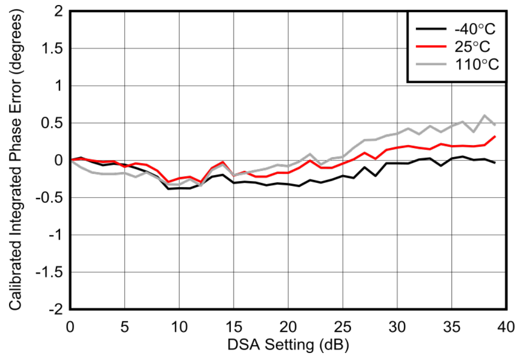


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-561. Calibrated Integrated Phase Error vs Channel at 7.1GHz

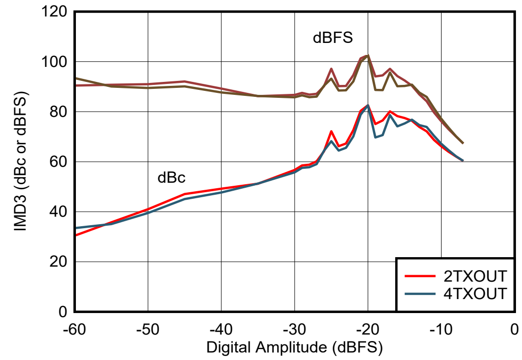
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



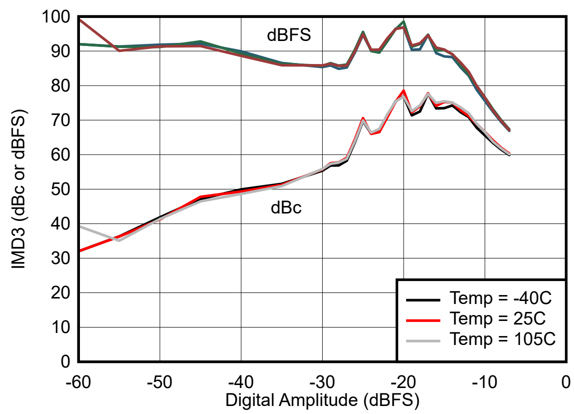
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 4-562. Calibrated Integrated Phase Error vs Temperature at 7.1GHz



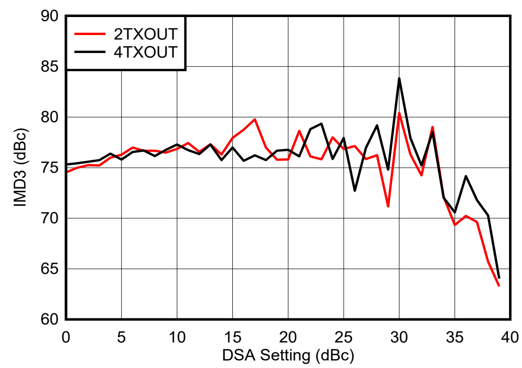
Tone spacing = 50MHz

Figure 4-563. IMD3 vs Digital Amplitude and Channel at 7.1GHz



Tone spacing = 50MHz

Figure 4-564. IMD3 vs Digital Amplitude and Temperature at 7.1GHz

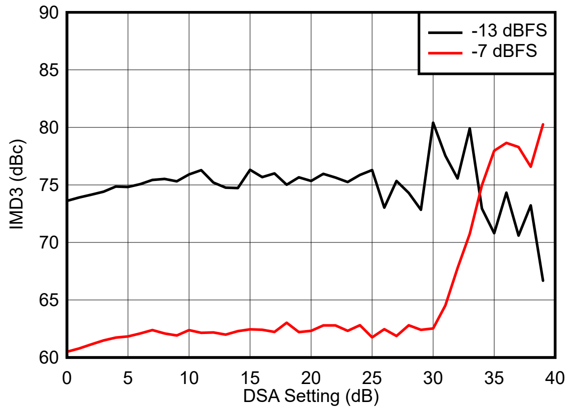


Tone spacing = 50MHz

Figure 4-565. IMD3 vs DSA Setting and Channel at 7.1GHz

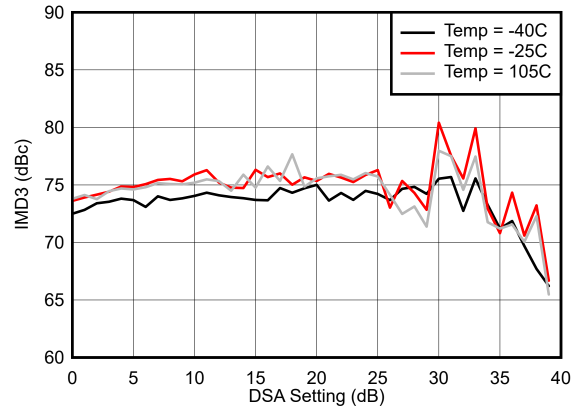
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



Tone spacing = 50MHz

Figure 4-566. IMD3 vs DSA Setting and Digital Amplitude at 7.1GHz



Tone spacing = 50MHz

Figure 4-567. IMD3 vs DSA Setting and Temperature at 7.1GHz

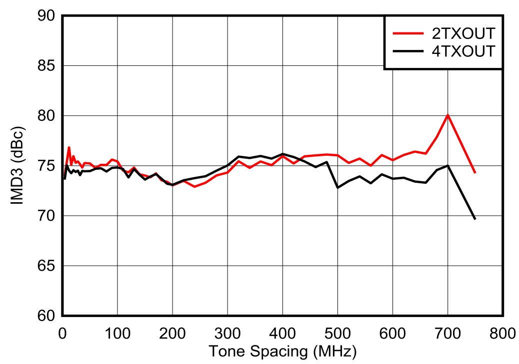


Figure 4-568. IMD3 vs Tone Spacing and Channel at 7.1GHz

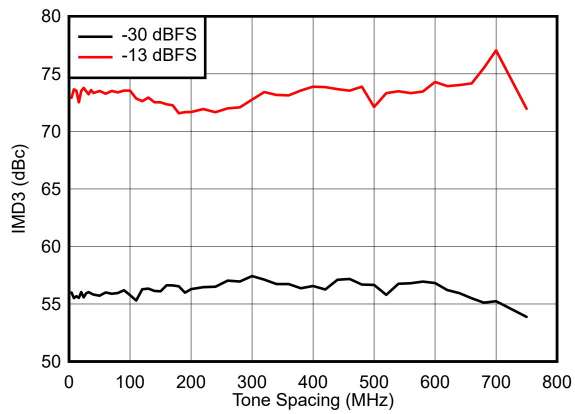


Figure 4-569. IMD3 vs Tone Spacing and Digital Amplitude at 7.1GHz

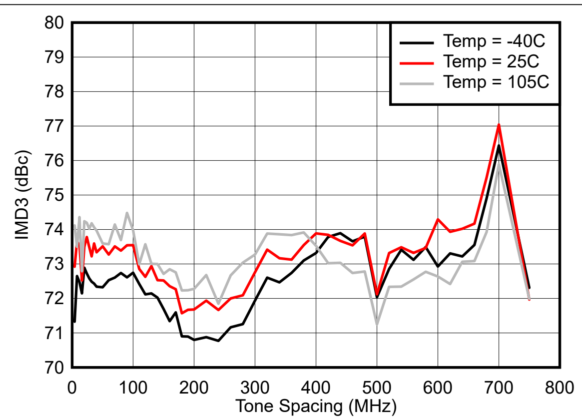
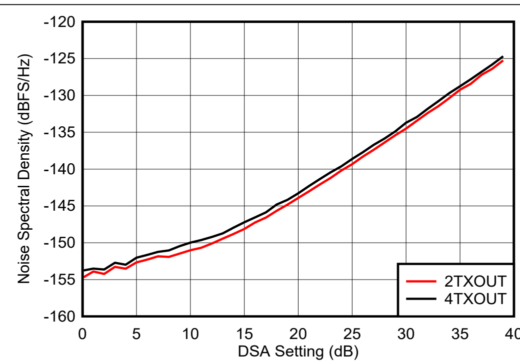


Figure 4-570. IMD3 vs Tone Spacing and Temperature at 7.1GHz

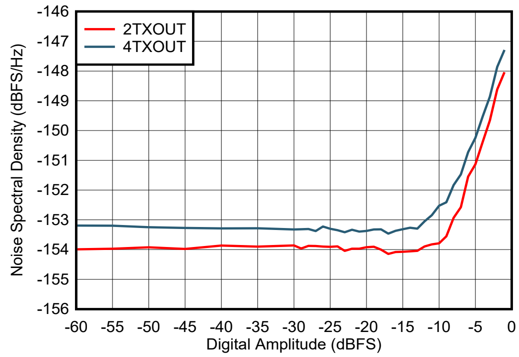


Tone at -12dBFS, 50MHz offset from tone

Figure 4-571. NSD vs DSA Setting and Channel at 7.1GHz

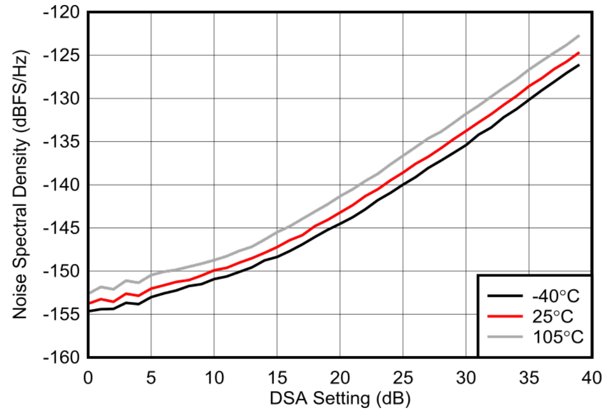
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



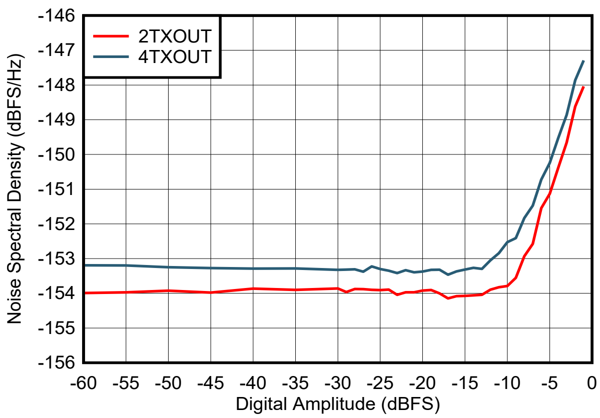
50MHz offset from tone

Figure 4-572. NSD vs DSA Setting and Amplitude at 7.1GHz



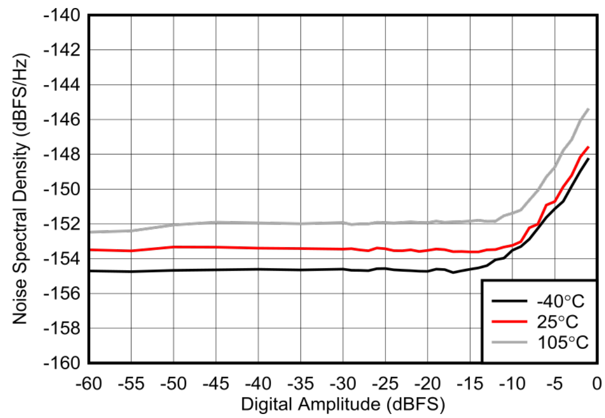
Tone at -12dBFS, 50MHz offset from tone

Figure 4-573. NSD vs DSA Setting and Temperature at 7.1GHz



50MHz offset from tone

Figure 4-574. NSD vs Digital Amplitude and Channel at 7.1GHz

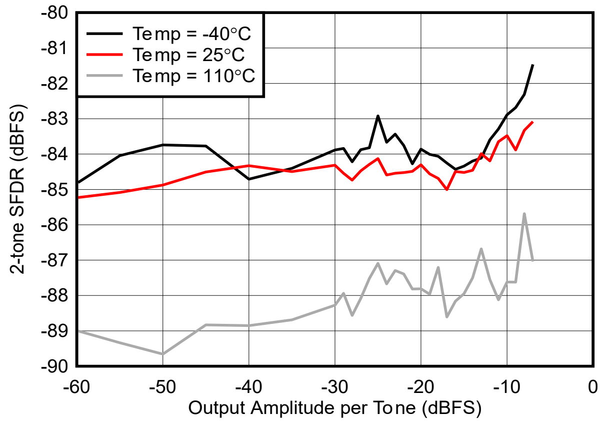


50MHz offset from tone

Figure 4-575. NSD vs Digital Amplitude and Temperature at 7.1GHz

4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



50MHz tone spacing, inband = 7100MHz ± 200MHz, excluding IMD3 components separately

Figure 4-576. Two Tone Inband SFDR vs Output Amplitude at 7.1GHz

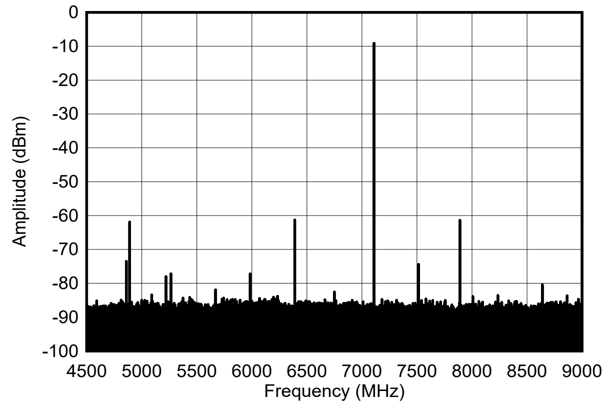


Figure 4-577. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Nyquist)

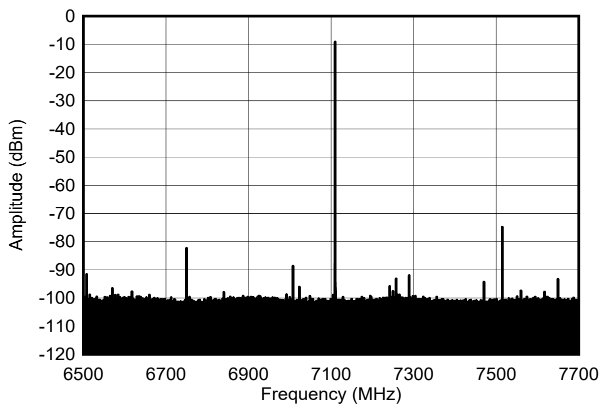


Figure 4-578. Single Tone Output Spectrum at 7.1GHz, -1dBFS (narrow span)

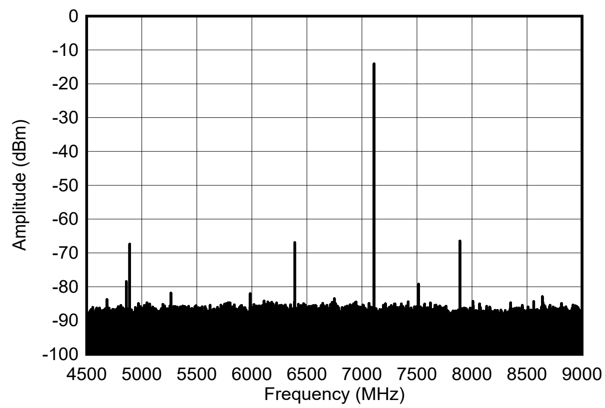


Figure 4-579. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Nyquist)

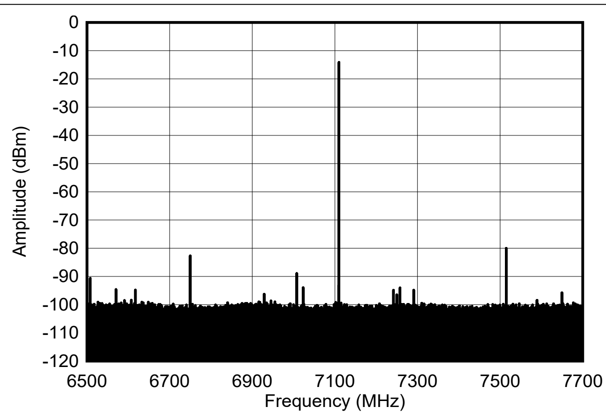


Figure 4-580. Single Tone Output Spectrum at 7.1GHz, -6dBFS (narrow span)

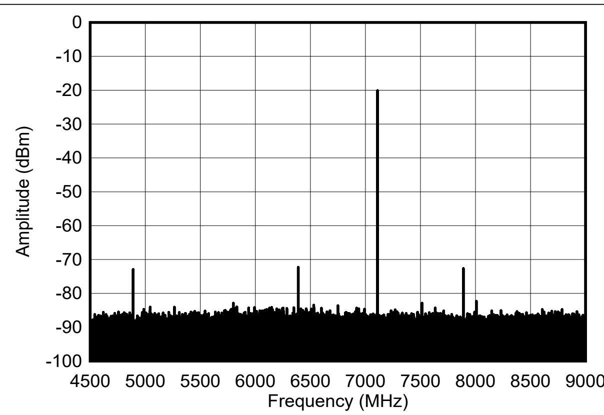


Figure 4-581. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Nyquist)

4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2[nd] Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.

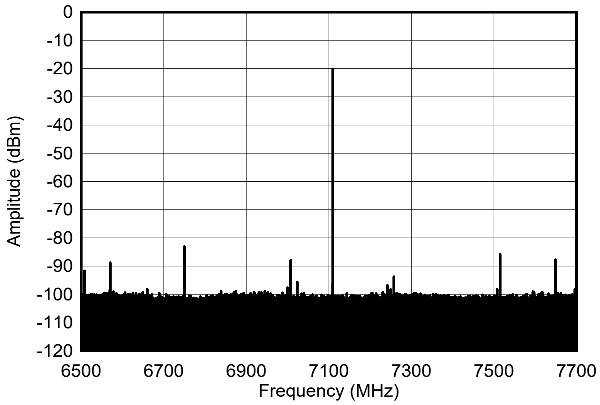
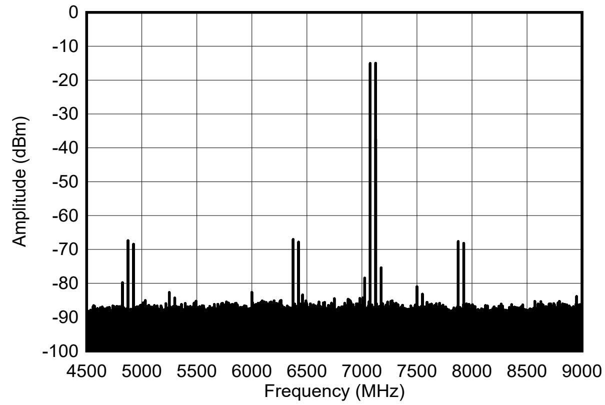
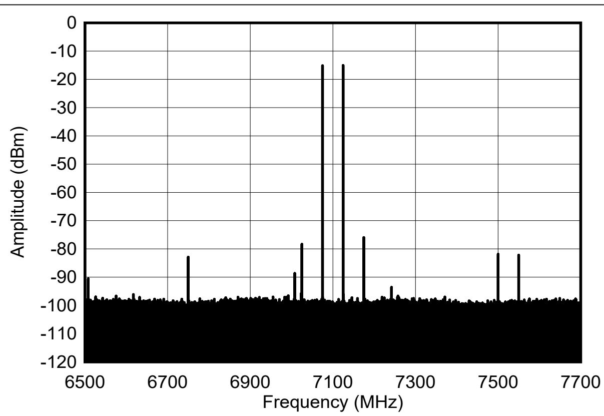


Figure 4-582. Single Tone Output Spectrum at 7.1GHz, -12dBFS (narrow span)



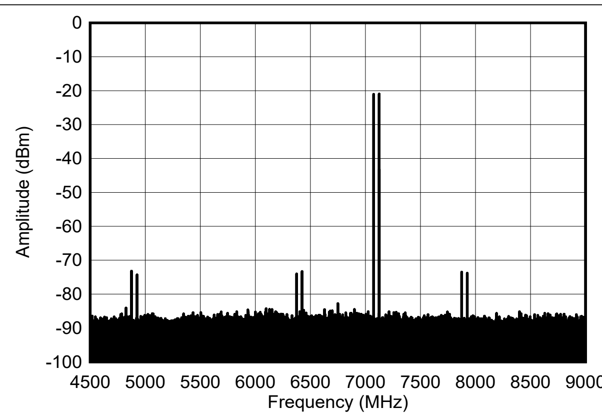
50MHz Tone Spacing

Figure 4-583. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Nyquist)



50MHz Tone Spacing

Figure 4-584. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (narrow band)

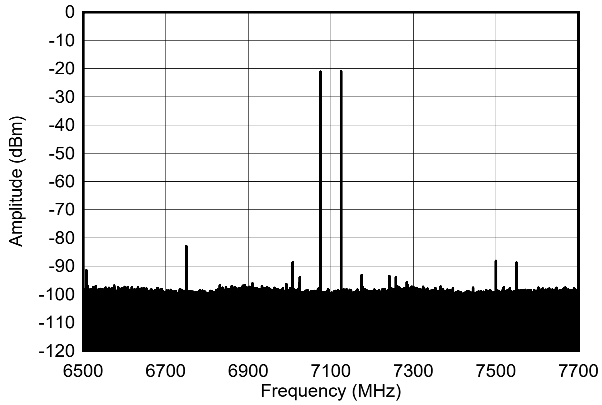


50MHz Tone Spacing

Figure 4-585. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Nyquist)

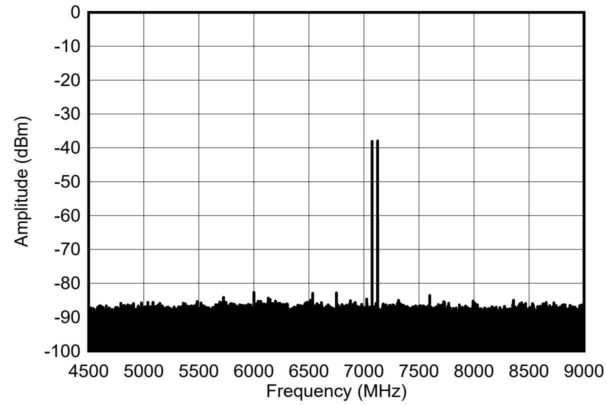
4.12.14 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 7.1GHz matching.



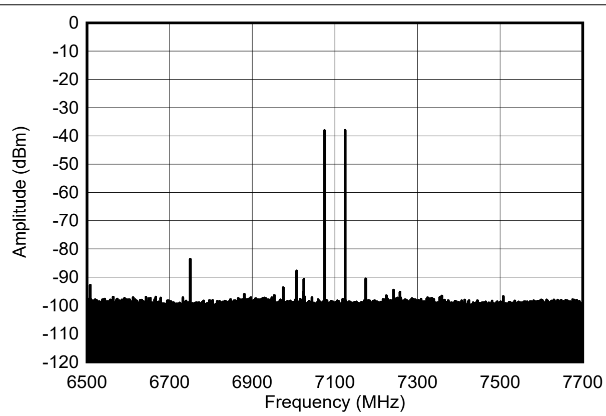
50MHz Tone Spacing

Figure 4-586. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (narrow span)



50MHz Tone Spacing

Figure 4-587. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Nyquist)



50MHz Tone Spacing

Figure 4-588. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (narrow span)

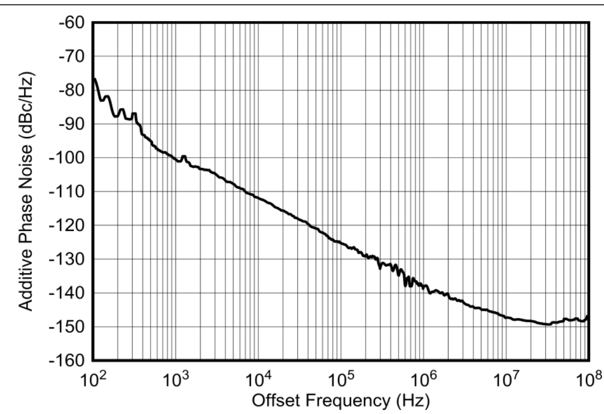
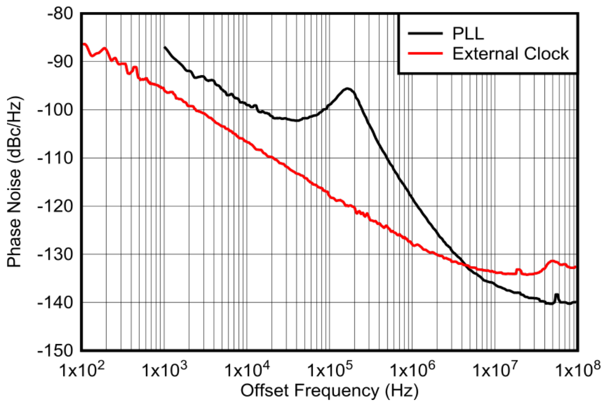


Figure 4-589. External Clock Additive Phase Noise at 7.1GHz

4.12.15 PLL and Clock Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



measured at TX output, normalized to 12GHz by 20*log10(12GHz/F_{OUT})

Figure 4-590. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz

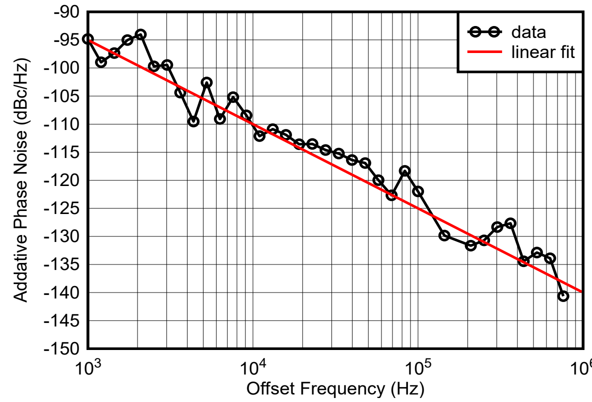
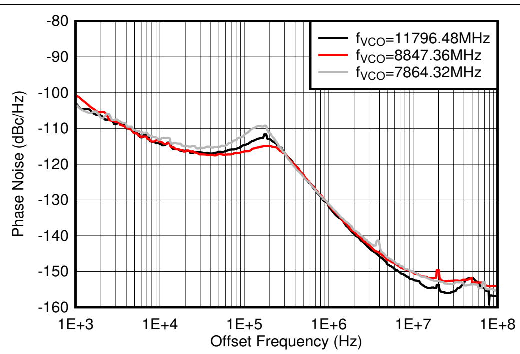
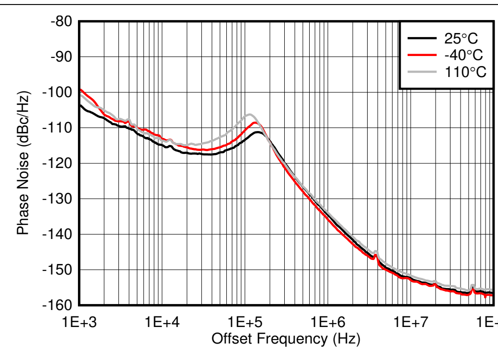


Figure 4-591. RX Addative Phase Noise at 9.61GHz



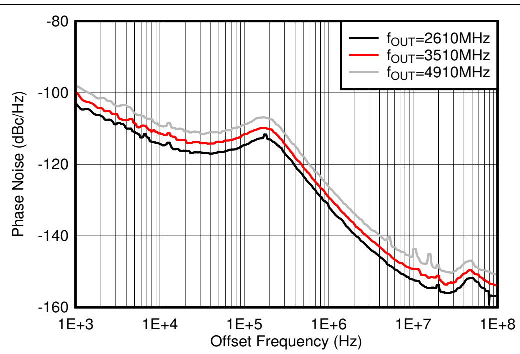
PLL enabled, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-592. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610MHz



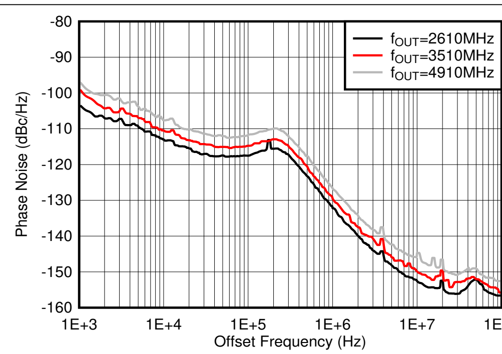
PLL enabled, f_{VCO} = 11796.48MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-593. Phase Noise for 12GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910MHz



PLL enabled, f_{VCO} = 11796.48MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-594. Phase Noise for 12GHz VCO vs Offset Frequency and f_{OUT} at 25°C

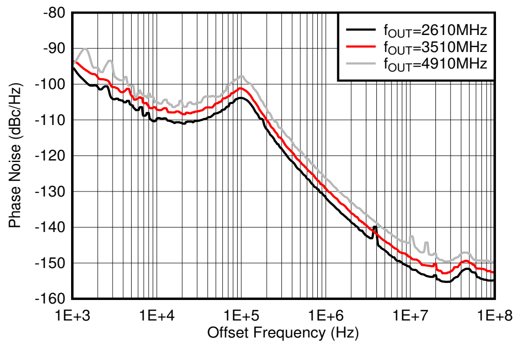


PLL enabled, f_{VCO} = 11796.48MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-595. Phase Noise for 12GHz VCO vs Offset Frequency and f_{OUT} at –40°C

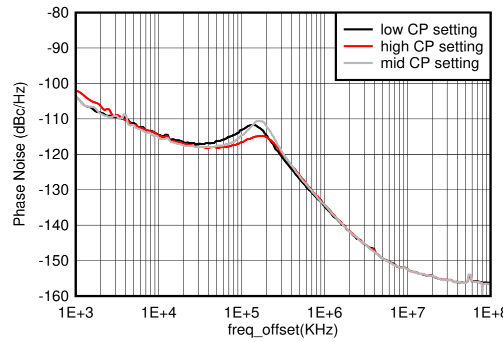
4.12.15 PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



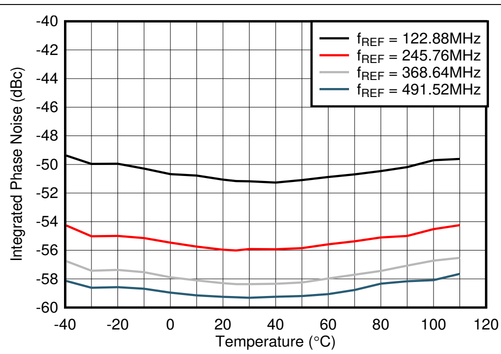
PLL enabled, f_{VCO} = 11796.48MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-596. Phase Noise for 12GHz VCO vs Offset Frequency and f_{OUT} at 110°C



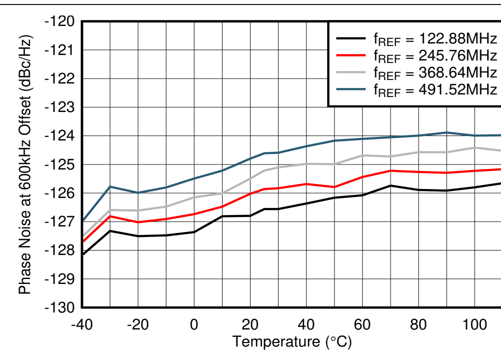
PLL enabled, f_{VCO} = 11796.48MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-597. Phase Noise for 12GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6GHz



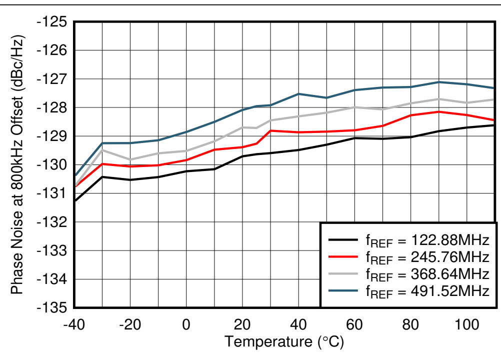
PLL enabled, f_{VCO} = 11796.48MHz, 1kHz to 100MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 4-598. Integrated Phase Noise for 12GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



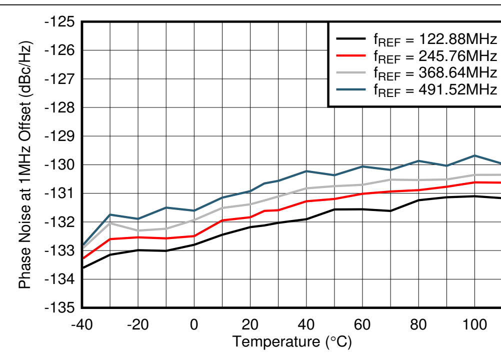
PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-599. Phase Noise for 12GHz VCO at 600kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-600. Phase Noise for 12GHz VCO at 800kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz

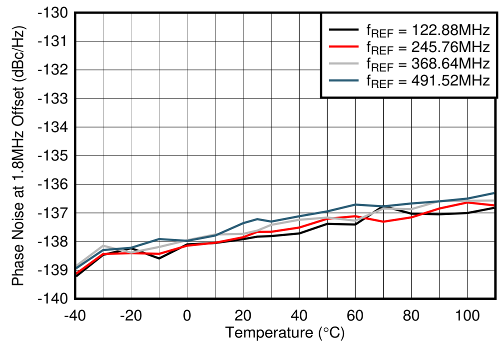


PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-601. Phase Noise for 12GHz VCO at 1MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz

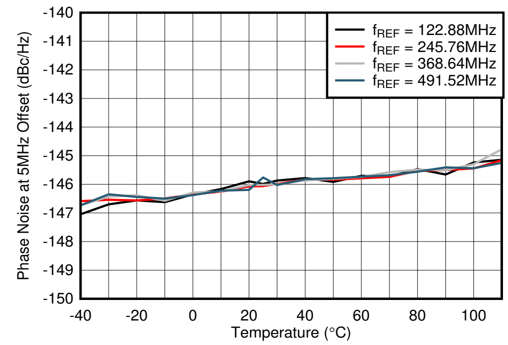
4.12.15 PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



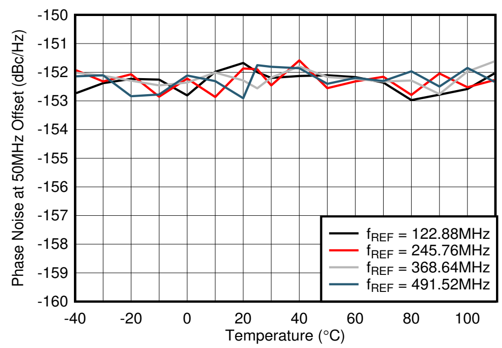
PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-602. Phase Noise for 12GHz VCO at 1.8MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



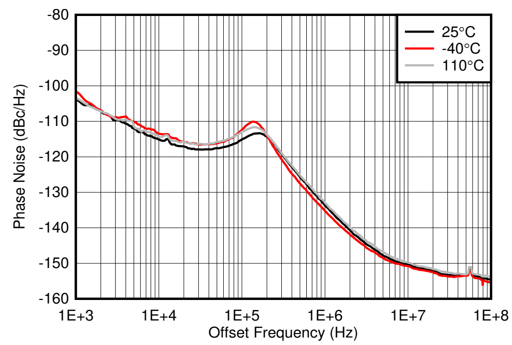
PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-603. Phase Noise for 12GHz VCO at 5MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



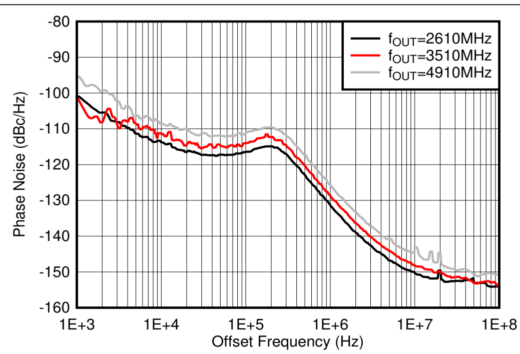
PLL enabled, f_{VCO} = 11796.48MHz, measured at 2TXOUT

Figure 4-604. Phase Noise for 12GHz VCO at 50MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



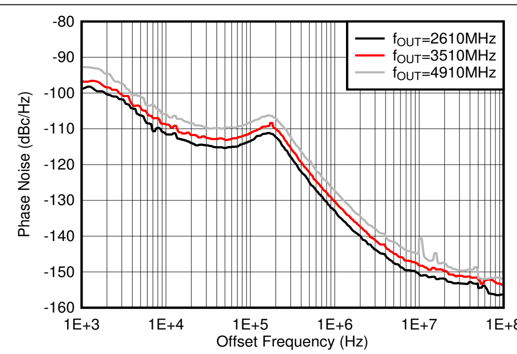
PLL enabled, f_{VCO} = 9830.4MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-605. Phase Noise for 10GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910MHz



PLL enabled, f_{VCO} = 9830.4MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-606. Phase Noise for 10GHz VCO vs Offset Frequency and f_{OUT} at 25°C

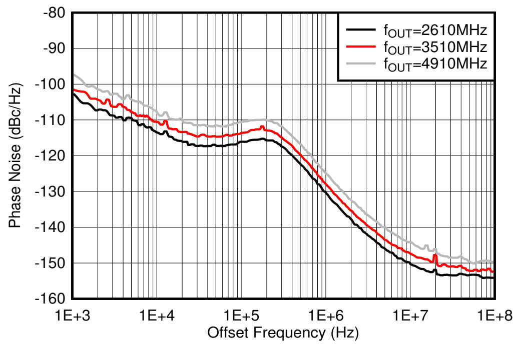


PLL enabled, f_{VCO} = 9830.4MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-607. Phase Noise for 10GHz VCO vs Offset Frequency and f_{OUT} at –40°C

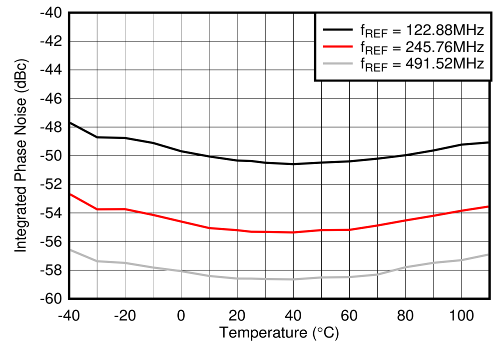
4.12.15 PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



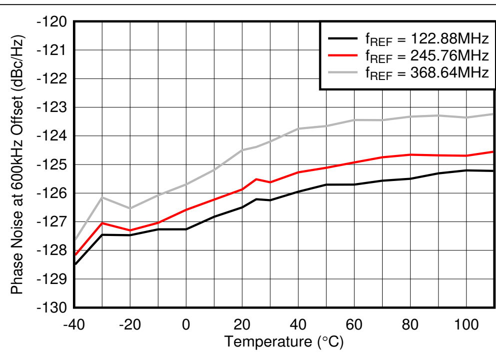
PLL enabled, f_{VCO} = 9830.4MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-608. Phase Noise for 10GHz VCO vs Offset Frequency and f_{OUT} at 110°C



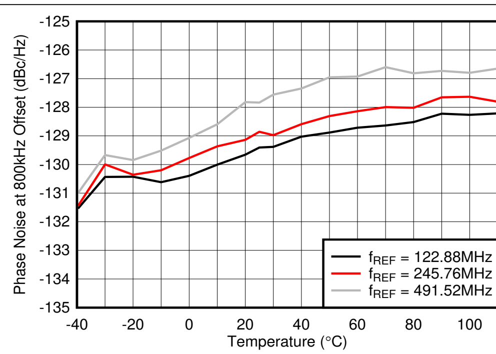
PLL enabled, f_{VCO} = 9830.4MHz, 1kHz to 100MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 4-609. Integrated Phase Noise for 10GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



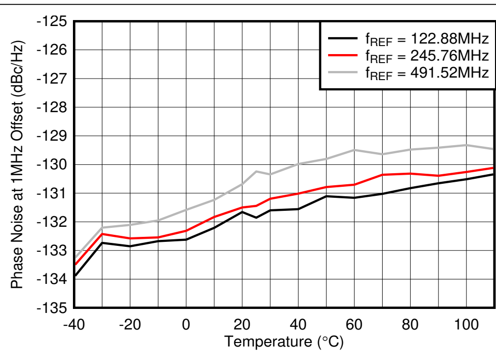
PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-610. Phase Noise for 10GHz VCO at 600kHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



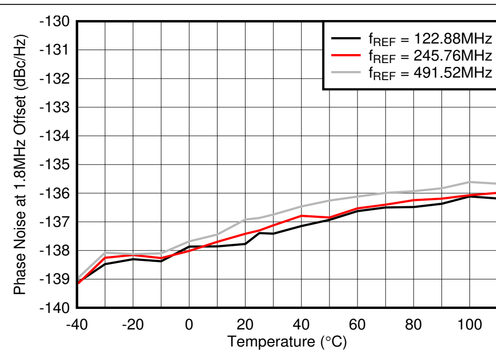
PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-611. Phase Noise for 10GHz VCO at 800kHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-612. Phase Noise for 10GHz VCO at 1MHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz

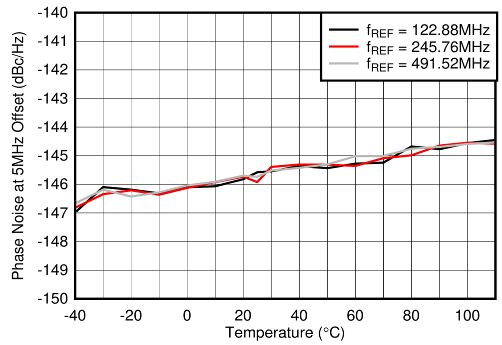


PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-613. Phase Noise for 10GHz VCO at 1.8MHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz

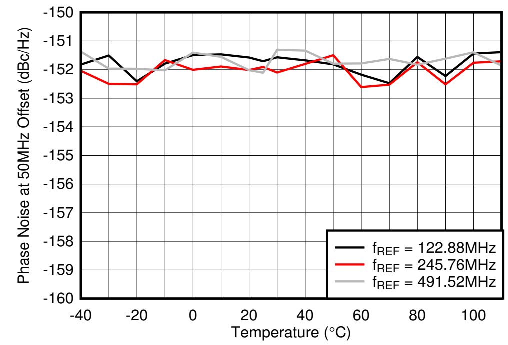
4.12.15 PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



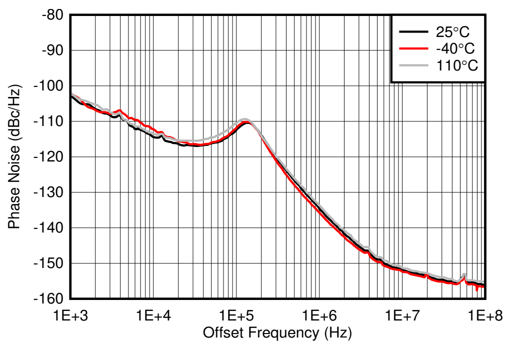
PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-614. Phase Noise for 10GHz VCO at 5MHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



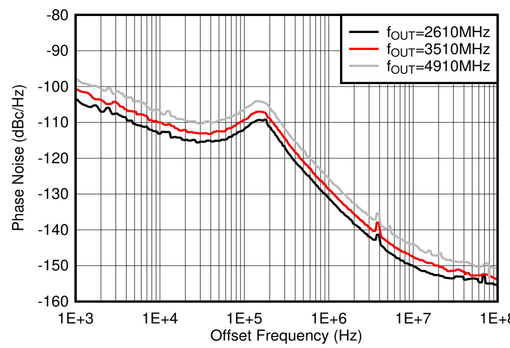
PLL enabled, f_{VCO} = 9830.4MHz, measured at 2TXOUT

Figure 4-615. Phase Noise for 10GHz VCO at 50MHz vs Temperature and f_{REF} at f_{OUT} = 2.6GHz



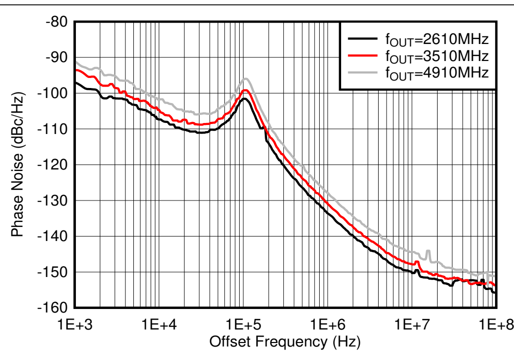
PLL enabled, f_{VCO} = 8847.36MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-616. Phase Noise for 9GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910MHz



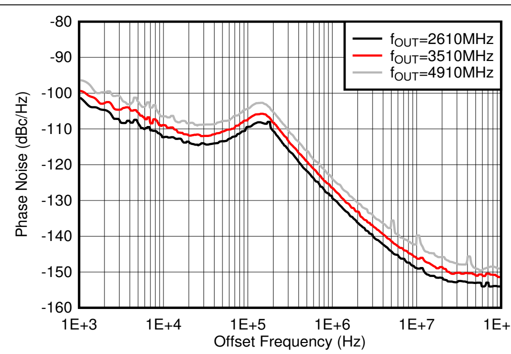
PLL enabled, f_{VCO} = 8847.36MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-617. Phase Noise for 9GHz VCO vs Offset Frequency and f_{OUT} at 25°C



PLL enabled, f_{VCO} = 8847.36MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-618. Phase Noise for 9GHz VCO vs Offset Frequency and f_{OUT} at –40°C

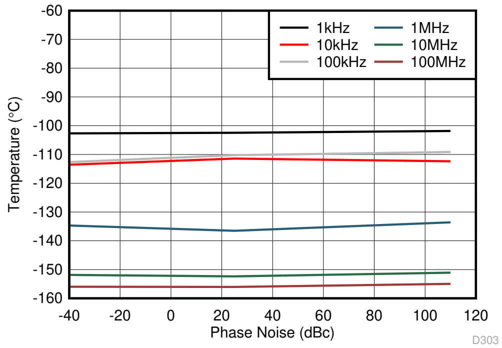


PLL enabled, f_{VCO} = 8847.36MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-619. Phase Noise for 9GHz VCO vs Offset Frequency and f_{OUT} at 110°C

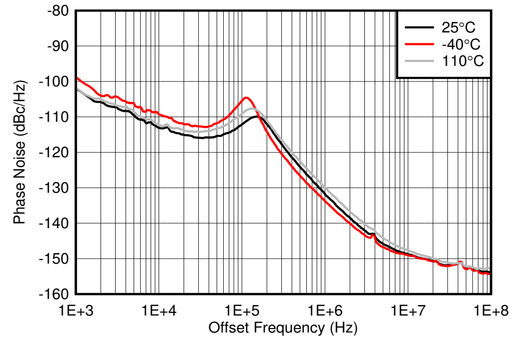
4.12.15 PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52MHz, Phase noise measured at TX output



PLL enabled, f_{VCO} = 8847.36MHz, f_{REF} = 491.52MSPS, minimum LPF BW, measured at 2TXOUT

Figure 4-620. Phase Noise for 9GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6GHz



PLL enabled, f_{VCO} = 7864.32MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 4-621. Phase Noise for 8GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910MHz

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7903ALKSEPM	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	Call TI	Call TI	-40 to 85	AFE7903NSP SNPB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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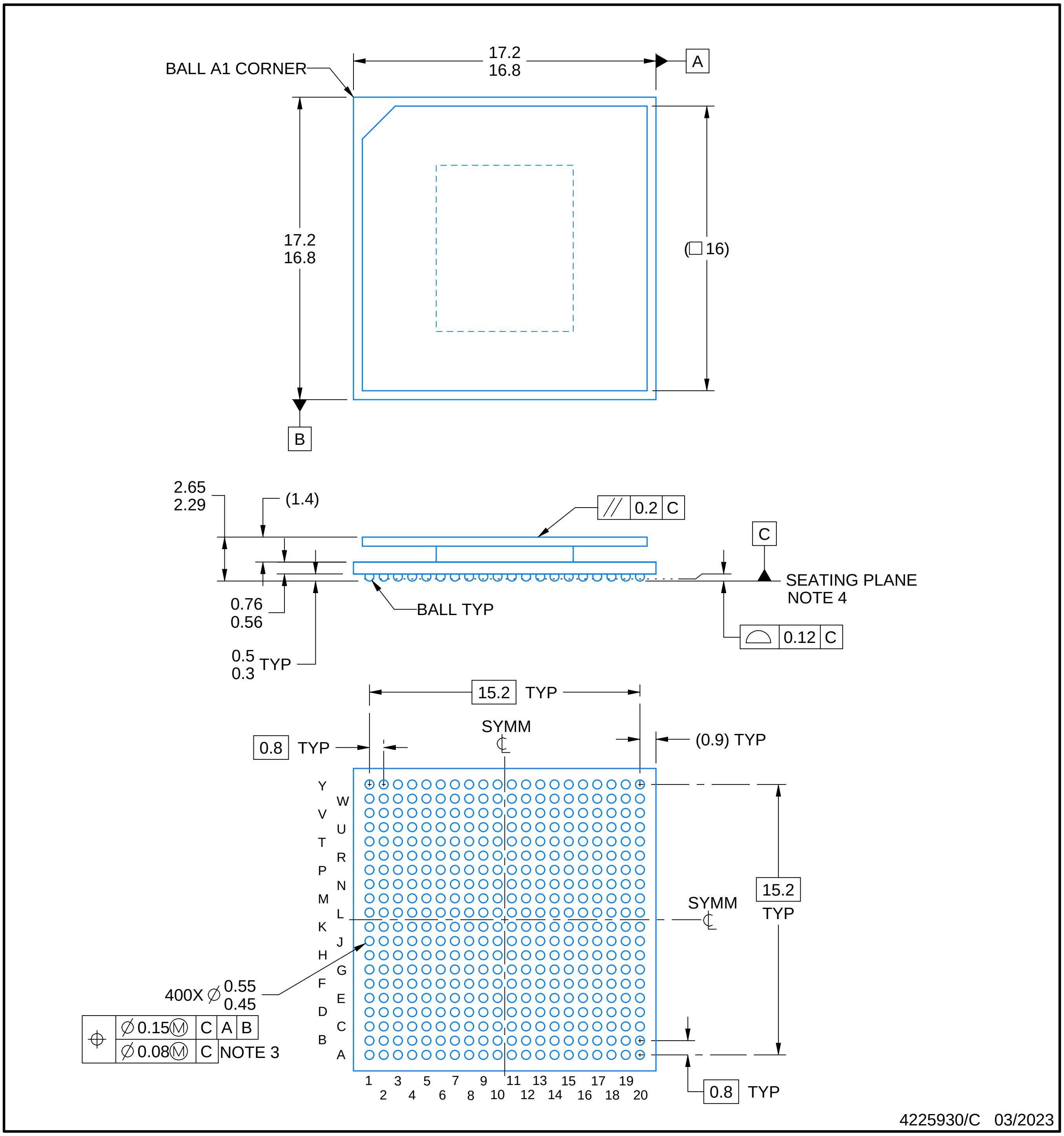
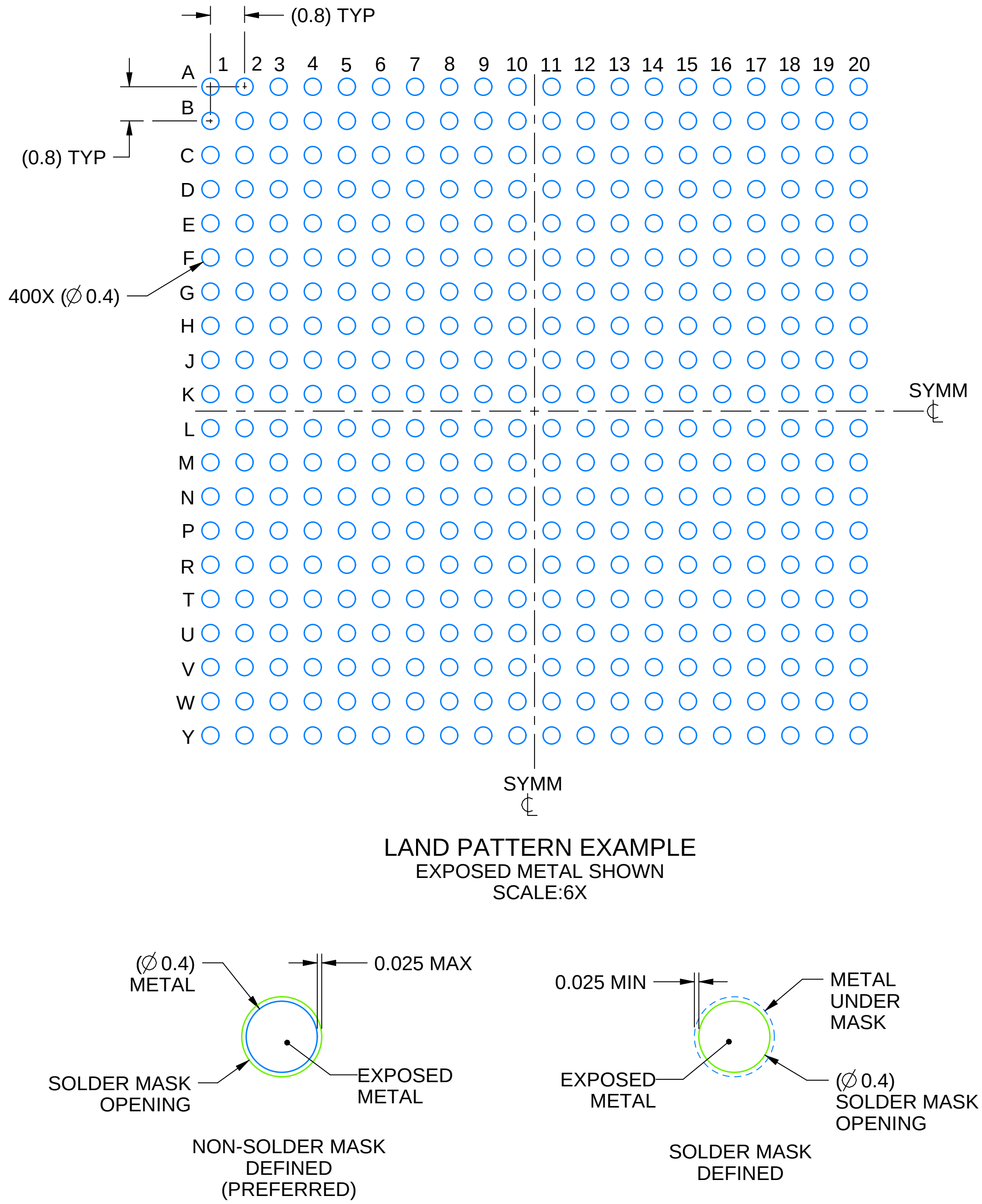


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



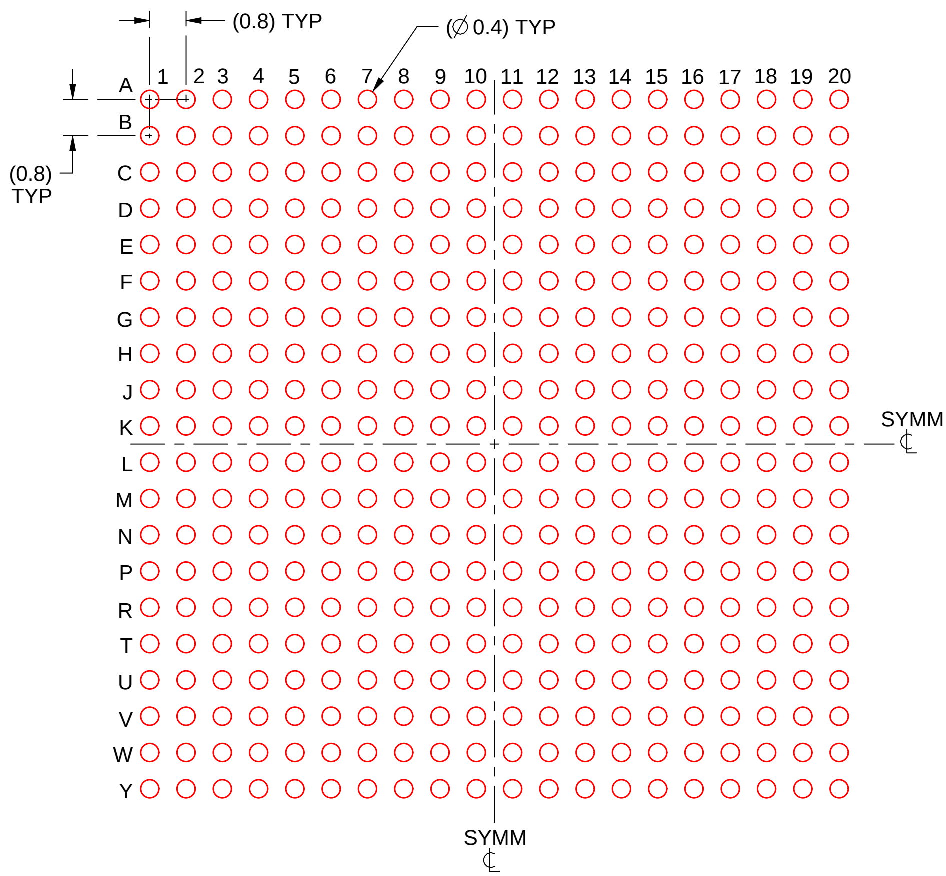
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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