AM13E230x Microcontrollers

1 Features

- **Device Cores**
  - Arm® Cortex®-M33 32-bit CPU up to 250MHz
    - Floating Point Unit (FPU), Custom Datapath Extension (CDE), Memory Protection Unit (MPU) and Micro Trace Buffer (MTB)
    - DSP Extension and 32-bit Trigonometric Math Unit (TMU) accelerates trigonometric calculations
    - 250MHz with *400*DMIPS and *1080* CoreMark® (4.32 CoreMark®/MHz)
    - 200MHz with *325* DMIPS and *870* CoreMark® (4.36 CoreMark®/MHz)
  - 1x TinyEngine™ Neural-Network Processing Unit (NPU) optimized for time-series Edge AI enablement
- **Memories**
  - Up to 512kB (2 banks of up to 256kB, 2kB sectors) of non-volatile flash memory
    - 144-bit word with Error Correction Code
    - Bank swap for dual-image firmware
  - Up to 128kB of 0-wait state SRAM
    - Hardware parity and 1kB instruction cache
    - 32KB RAM (SRAM0) retained in low power modes
  - External Peripheral Interface (EPI) supporting SDRAM, ASRAM, or ASIC/FPGA external interfaces
- **High-Performance Analog Peripherals**
  - 3x SAR Analog-to-digital Converters (ADCs)
    - 7.81MSPS with 12-bit resolution
    - Each ADC supports up to 32 single ended input channels
    - Configurable 1.65V or 2.5V internal shared voltage reference (VREF)
    - Support for external voltage reference (VREF)
    - Hardware oversampling and undersampling modes, with accumulation, averaging and outlier rejection
  - 4x Analog Comparator Sub-systems (CMPSS)
    - 2x Comparators with Window Functionality
    - 2x 10-bit effective DAC and 2x digital filters
    - CMPSS[2:3] support buffered DACL_OUT to pin
  - 3x Programmable Gain Amplifiers (PGA)
    - Unity Gain Support
    - Inverting and non-inverting gain mode support
    - Gain options: 1, 2/-1, 4/-3, 8/-7, 16/-15, 32/-31, 64/-63
    - 4:1 input mux supporting up to 12 channels
    - Programmable output filtering
  - Programmable analog connections between ADC, PGAs, CMPSS and DAC
- **Optimized Low-Power Modes**
  - RUN: 225µA/MHz (CoreMark)
  - STANDBY: 196uA with CPU execution resume and 32kB SRAM retention
  - SHUTDOWN: <5µA with IO wake-up capability
- **Flexible System Peripherals**
  - 12-channel Direct Memory Access (DMA) controller
  - Nested Vectored Interrupt Controller (NVIC)
  - Up to 107 GPIO with Input/Output XBAR connectivity
  - 8 GPIOs with Shutdown Wakeup Capability
  - 1x Windowed Watchdog Timer (WWDT)
    - Independent 32kHz clock with programmable divider
    - 25-bit counter with configurable timer periods
  - 2x general-purpose timers
    - TIMG4 (16-bit), TIMG12 (32-bit)
    - Pre-scaler, Compare/Capture, Shadow
    - Up to 2x channels each
- **Real-time Control Peripherals**
  - 5x Multi-channel pulse-width modulator (MCPWM) modules
    - 6 PWM channels per module with 16-bit time base
    - 4 Start Of Conversion (SOCs) per module enable precise ADC sampling for single shunt or three shunt current sensing mode
    - Support dead-band, trip event and time base synchronization
  - 2x Enhanced Capture (eCAP) modules
    - 32-bit timer for speed, elapsed time, period and duty cycle measurements
    - 1x alternative PWM channel per module
  - 3x Enhanced Quadrature Encoder Pulse (eQEP)
    - Supports linear or rotary incremental encoder interface
    - Edge capture unit for optimized speed measurement at low speed
  - Device Crossbars (INPUTXBAR, OUTPUTXBAR, PWMXBAR)
    - Flexibility to route signals from GPIO to other modules

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    - For example, the INPUTXBAR is used to route signals from a GPIO to other modules such as ADC, CMPSS, MCPWM, eCAP, eQEP, and external interrupts
- **Enhanced Serial Communication Interfaces**
  - Two configurable serial interfaces supporting UART (LIN) or I^2C (SMBus/PMBus)
  - Four configurable serial interfaces supporting UART, I^2C, or SPI
  - One Modular Controller Area Network (MCAN) with Flexible Data-rate (CAN FD)
- **Clock System**
  - Internal 4MHz/32MHz oscillator (SYSOSC)
  - Internal 32kHz oscillator (LFOSC)
  - System Phase-locked loop (SYSPLL) up to 250MHz
  - External 4MHz to 25MHz crystal oscillator (XTAL)
  - External 4MHz to 48MHz clock input (HFCLK)
- **OS Support**
  - FreeRTOS, Zephyr, Baremetal
- **Safety**
  - Enabling IEC61508 SIL-2 and SIL-3 systems
- **Security and Encryption**
  - Secure Boot/FWU/Debug/JTAG Lock
  - Secure Key Storage and Management
  - Privileged/Non-Privileged resource partitioning
  - Flash Write/Erase/Hide Protections
  - Device Life cycle Management
  - AES Encryption with 128- or 256-bit Key
  - Unique Identification Number (UID)
- **Internal Diagnostic Modules**
  - Cyclic Redundancy Checker (CRC-16, CRC-32)
  - Integrated Temperature Sensor
  - Integrated BOR/POR Supply Monitors
- **Development Support**
  - JTAG (4-pin) and Serial Wire Debug (SWD) (2-pin)
  - Micro Trace Buffer (MTB)
  - Embedded Trace Macrocell (ETM) (TRACE_DATA[0:3])
    - Supports Serial Trace and Parallel Trace
- **Package Options**
  - 128-pin PDT Thin Quad Flat Package (TQFP) (0.4mm pitch)
  - 100-pin PZ Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 80-pin PN Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 64-pin PM Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 48-pin PT Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 48-pin RGZ Very Thin Quad Flatpack No-Lead (VQFN) (0.5mm pitch)
- **Operating Characteristics**
  - Supply voltage: 3.3V
  - Ambient Temperature Range(T_A): –40°C up to 125°C

2 Applications

- Dual Motor Drive + PFC (Power Factor Correction)
- Multiple Motor Control
- 3-Phase Motor
- Industrial Drive
- Fan/Pump Drive
- Power Tools
- HVAC
- Air conditional outdoor unit
- Robotic lawn mower
- Washer & dryer
- Refrigerator & freezer
- AC inverter & VF drives
- Servo & stepper drives
- Field transmitter & sensor
- Humanoid robot motor drive
- Robot safety module
- Collaborative robot servo drive
- HVAC controller
- HVAC motor control
- HVAC valve and actuator control
- Elevator main control panel
- Elevator & escalator motor controll
- Cordless power tool
- Appliances
- Industrial Automation
- Robotics
- Medical & Healthcare
- Building Automation
- Test & Measurement

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3 Description

AM13E230x microcontrollers (MCUs) are part of the AM13x highly integrated, low-cost 32-bit MCU family based on the Arm® Cortex®-M33 32-bit CPU operating at up to 250MHz or 200MHz frequency. These real-time control optimized MCUs offer high-performance analog, control, and digital peripheral integration, support ambient temperature ranges from -40°C to 125°C, and operate with a 3.3V supply voltage.

The AM13E230x MCUs provide up to 512KB of embedded flash program memory (2 banks of up to 256KB) with built-in error correction code (ECC) and up to 128KB SRAM with hardware parity. Smaller memory configuration variants are offered.

The processing system incorporates Custom Datapath Extension (CDE) support, a Memory Protection Unit (MPU), Micro Trace Buffer (MTB), a 32-bit Trigonometric Math Unit (TMU), and a TinyEngine™ Neural-network Processing Unit (NPU).

AM13E230x MCUs are enabled with robust, high-performance analog peripherals. Three 12-bit ADCs with a maximum sampling rate of 7.81MSPS, four high speed comparator subsystems with built-in 10-bit reference DACs, and three programmable gain amplifiers with 4:1 mux provide true real-time signal chain performance.

These MCUs also offer real-time control and timing peripherals such as a 12-channel DMA controller, multi-channel PWM generation, generic timers, specialty timers for capture and encoder interface, and a flexible X-BAR system for connecting GPIO and control peripherals.

An independent oscillator and windowed watchdog timer are included as well as multiple internal and external clocking options. Multiple operational power modes are offered for flexibility in controlling power consumption vs. wake-up time.

Data integrity and encryption features (AES, secure boot) provide security across the AM13E230x domains. A Cyclic Redundancy Checker (CRC) module provides internal diagnostics to the AM13E230x MCUs.

Enhanced communication interfaces are supported through one MCAN and up to 6 UNICOMM peripherals to support a combination of UART/LIN, I2C/SMBUS, and SPI. For connecting to external devices or memory, the high-speed External Peripheral Interface (EPI) can connect to SDRAM or asynchronous RAM devices such as FPGA or ASIC.

Package options include 48-pin QFN as well as 48/64/80/100/128-pin QFP. All packages support 250 MHz operation across an ambient temperature range of -40°C to 125°C. Additional packages supporting 200 MHz operation within the same temperature range are also available. For detailed Orderable Part Numbers (OPNs), please refer to the Mechanical, Packaging, and Orderable Information section.

Package Information

PART NUMBER (1)	PACKAGE (2)	PACKAGE SIZE (3)	BODY SIZE (NOM)	PITCH
AM13E23019	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm	0.5mm
	RGZ (VQFN, 48)	7mm × 7mm	7mm × 7mm	0.5mm
AM13E23018	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm	0.5mm
	RGZ (VQFN, 48)	7mm × 7mm	7mm × 7mm	0.5mm

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Package Information (continued)

PART NUMBER (1)	PACKAGE (2)	PACKAGE SIZE (3)	BODY SIZE (NOM)	PITCH
AM13E23017	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm	0.5mm
	RGZ (VQFN, 48)	7mm × 7mm	7mm × 7mm	0.5mm

1. For orderable part number see the Mechanical, Packaging, and Orderable Information section.
2. For more information, see the Mechanical, Packaging, and Orderable Information section.
3. The package size (length × width) is a nominal value and includes pins, where applicable.

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3.1 Functional Block Diagram

Figure 3-1 shows the AM13E230x functional block diagram.

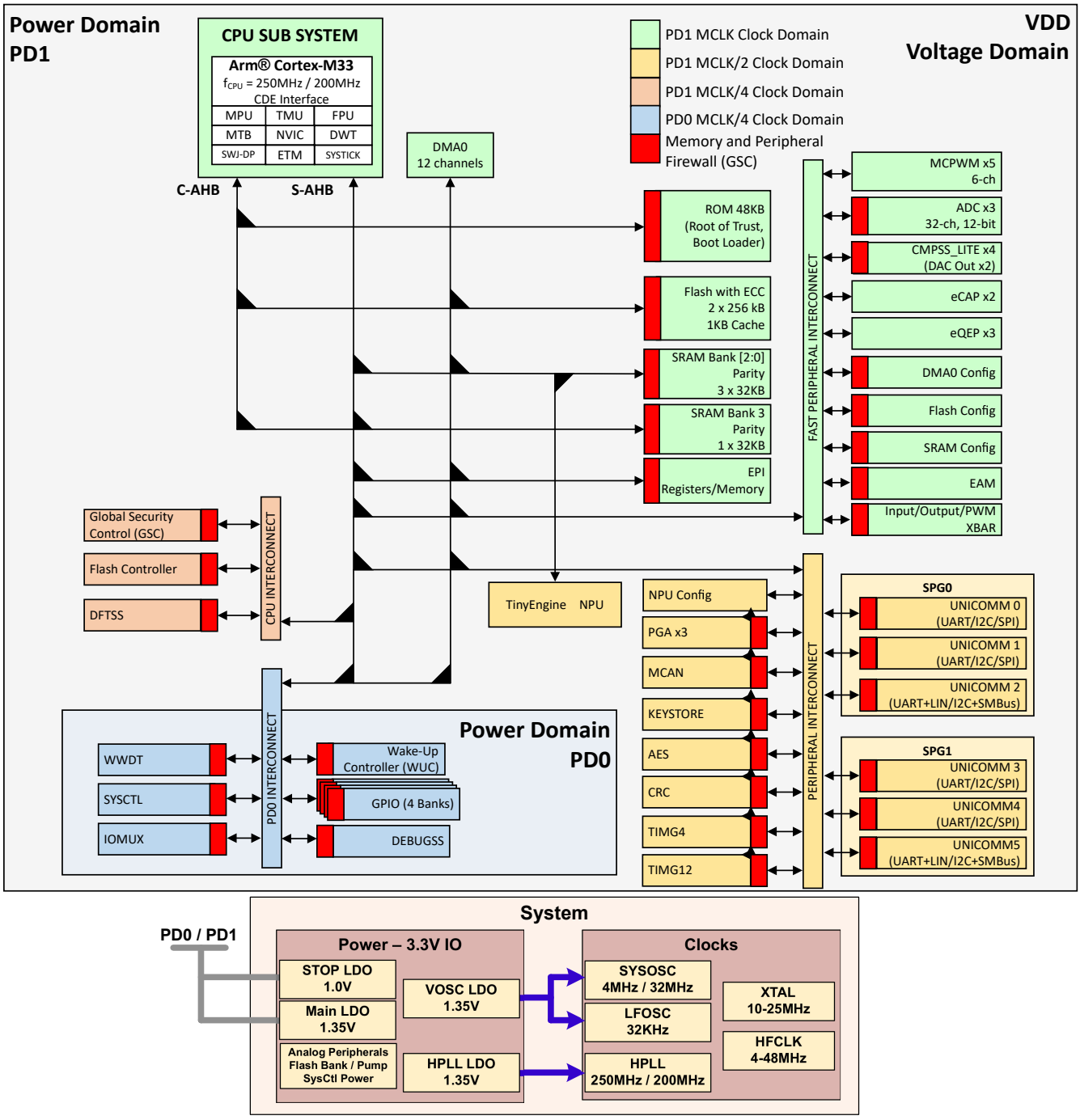


Figure 3-1. AM13E230x Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the AM13E230x microcontrollers.

Table 4-1. Device Comparison

Feature		AM13E23019	AM13E23018	AM13E23017
PROCESSOR AND ACCELERATORS				
Arm® Cortex®-M33	CPU Core Frequency	250MHz / 200MHz		
	Custom Datapath Extension (CDE)	Yes		
	Memory Protection Unit (MPU)	Yes		
	Micro Trace Buffer (MTB)	Yes		
	Trigonometric Math Unit (TMU)	Yes		
TinyEngine™ Neural-network Processing Unit (NPU)		Yes		
MEMORY				
Flash - with Error Correction Code (ECC)		512KB	256KB	128KB
SRAM - with HW Parity		128KB	128KB	64KB
Security Features		JTAGLOCK, Secure Boot		
Cyclic Redundancy Check (CRC)		CRC-16/CRC-32		
SYSTEM				
Direct Memory Access (DMA) Controller		1x 12-Channel		
16-bit General-Purpose Timer (TIMG4)		1		
32-bit General-Purpose Timer (TIMG12)		1		
Windowed Watchdog Timer (WWDT)		1		
Internal 4MHz/32MHz Oscillator (SYSOSC)		1		
Phase-Locked Loop up to 200MHz / 250MHz (SYSPLL)		1		
Internal 32kHz Oscillator (LFOSC)		1		
Crystal Oscillator (HFXT)/External Clock (HFCLK) input		1		
Internal 3.3V to 1.35V LDO		Yes		
General Purpose Input/Output (GPIO)		Up to 107 (package-dependent)		
ANALOG PERIPHERALS				
Analog to Digital Converter (ADC)	ADCs	3		
	Bits	12-bit ADC		
	ADC channels	Up to 32 channels		
Temperature Sensor		1		
Programmable Gain Amplifier (PGA) with Analog Input Mux		3		
Comparator Subsystem (CMPSS)	CMPSS (each includes 2x 11-bit DAC + 2x digital filters)	4		
	DACL Buffered Output	2		
CONTROL PERIPHERALS				
Motor-control Pulse Width Modulation (MCPWM)		5 (6-ch)		
Enhanced Capture Module (eCAP)		2		
Enhanced Quadrature Encoder Pulse Module (eQEP)		3		

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Table 4-1. Device Comparison (continued)

Feature			AM13E23019	AM13E23018	AM13E23017
COMMUNICATION PERIPHERALS					
UNICOMM	SPGSS0	UART	Up to 3 (2 UART, 1 UART+LIN)		
		I^2C	Up to 3 (2 I^2C, 1 I^2C+SMBUS)		
		SPI	Up to 2		
	SPGSS1	UART	Up to 3 (2 UART, 1 UART+LIN)		
		I^2C	Up to 3 (2 I^2C, 1 I^2C+SMBUS)		
		SPI	Up to 2		
Modular Controller Area Network (MCAN)			1x (CAN/CAN-FD)		
HIGH SPEED PERIPHERALS					
External Peripheral Interface (EPI)			1		
PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS					
Junction temperature (T_J)			–40°C to 140°C		
Ambient Temperature (T_A)			–40°C to 125°C		

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5 Terminal Configuration and Functions

5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers. The HTML version of this document provides additional information when hovering your cursor over a ball. For full pin configuration and functions for each package option, refer to *Pin Attributes* and *Signal Descriptions* sections.

Device Package Options

Package	Type	Size	Pitch	Pin Layout	Analog IO	Digital IO	Pin Count (Total)
LQFP128	PDT (TQFP)	14x14mm^2	0.4mm	32x32	44	107	128-pin
LQFP100_G	PZ (LQFP)	14x14mm^2	0.5mm	25x25	44	86	100-pin
LQFP100_H	PZ (LQFP)	14x14mm^2	0.5mm	25x25	43	85	100-pin
LQFP80	PN (LQFP)	12x12mm^2	0.5mm	20x20	39	66	80-pin
LQFP64_G	PM (LQFP)	10x10mm^2	0.5mm	16x16	27	52	64-pin
LQFP64_H	PM (LQFP)	10x10mm^2	0.5mm	16x16	26	52	64-pin
LQFP48	PT (LQFP)	9x9mm^2	0.5mm	12x12	21	38	48-pin
QFN48	RGZ (VQFN)	7x7mm^2	0.5mm	12x12	22	42	48-pin (PWRPAD)

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5.2 AM13E230x Pin Diagrams

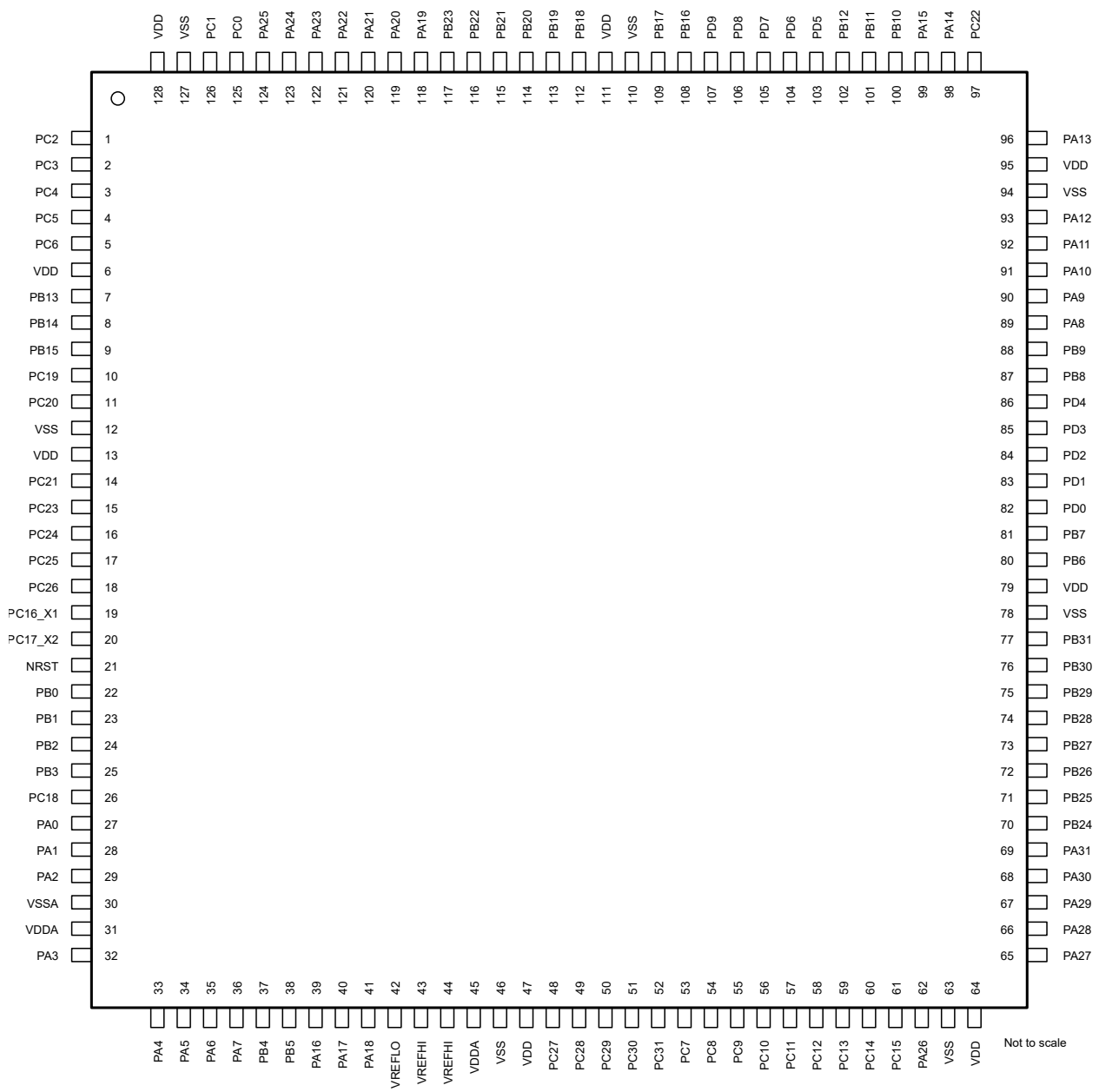


Figure 5-1. LQFP128 (PDT) Package

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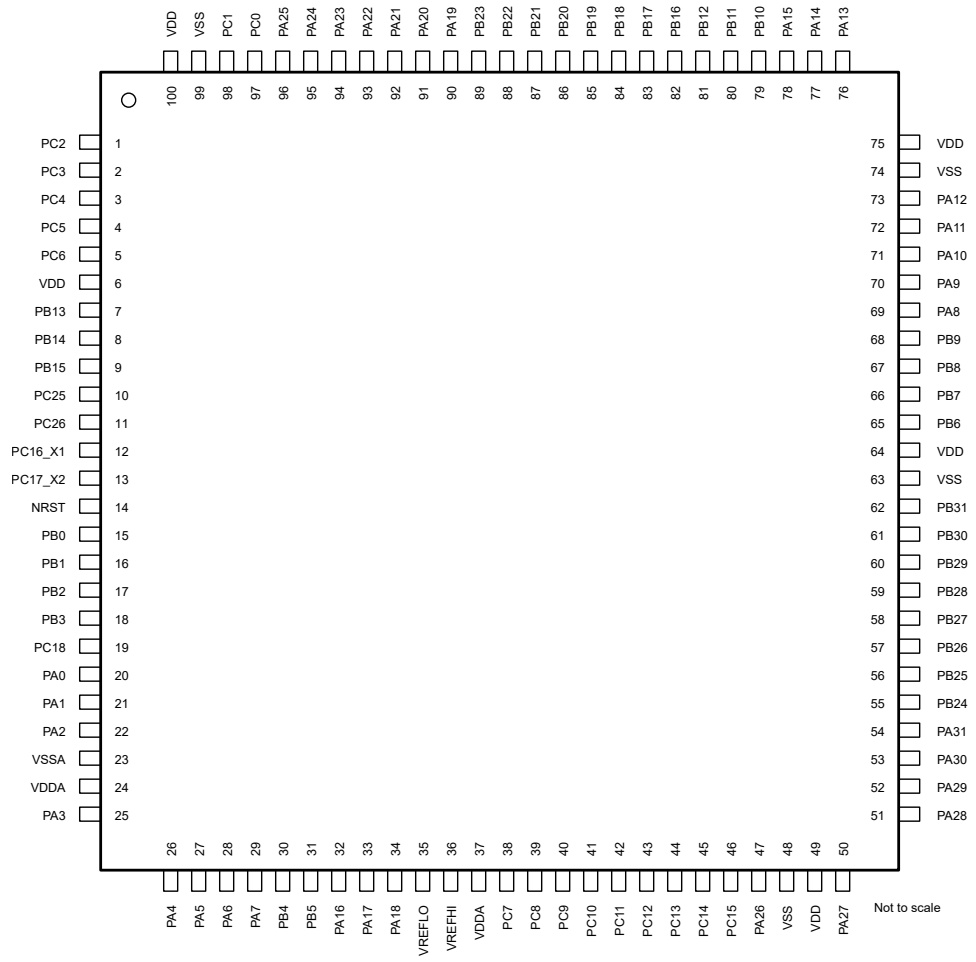


Figure 5-2. LQFP100_G (PZ) Package

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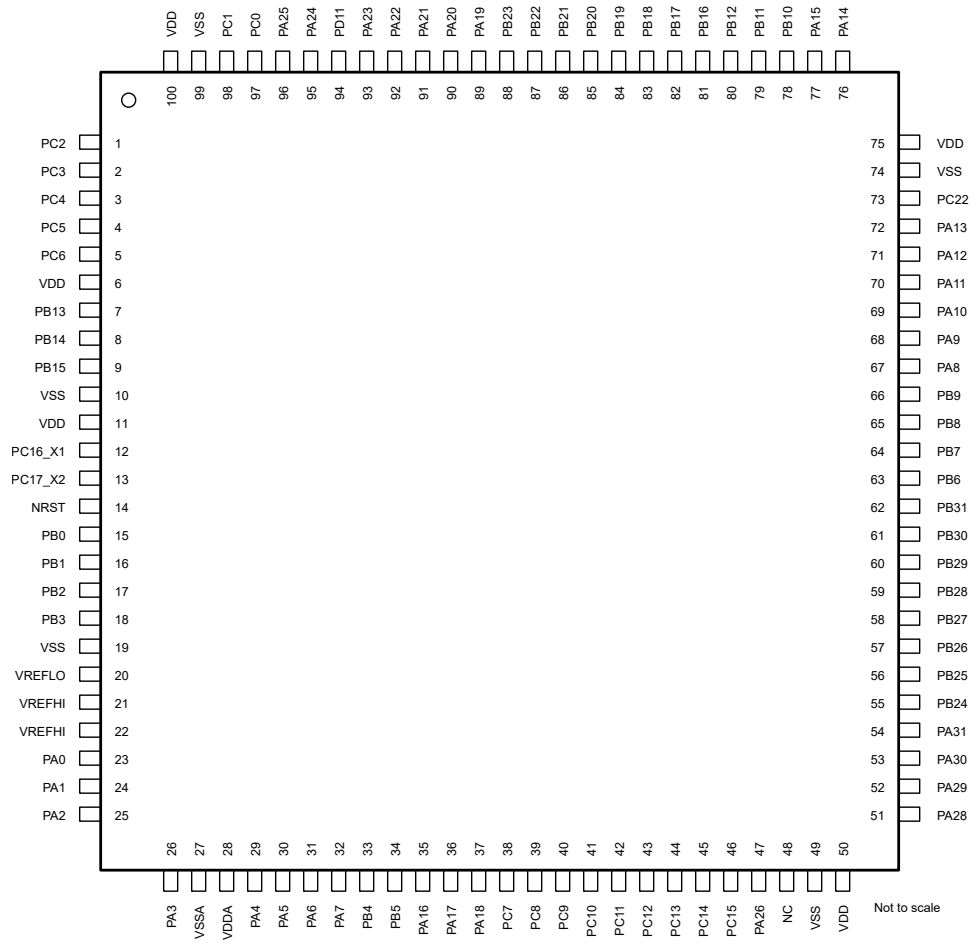


Figure 5-3. LQFP100_H (PZ) Package

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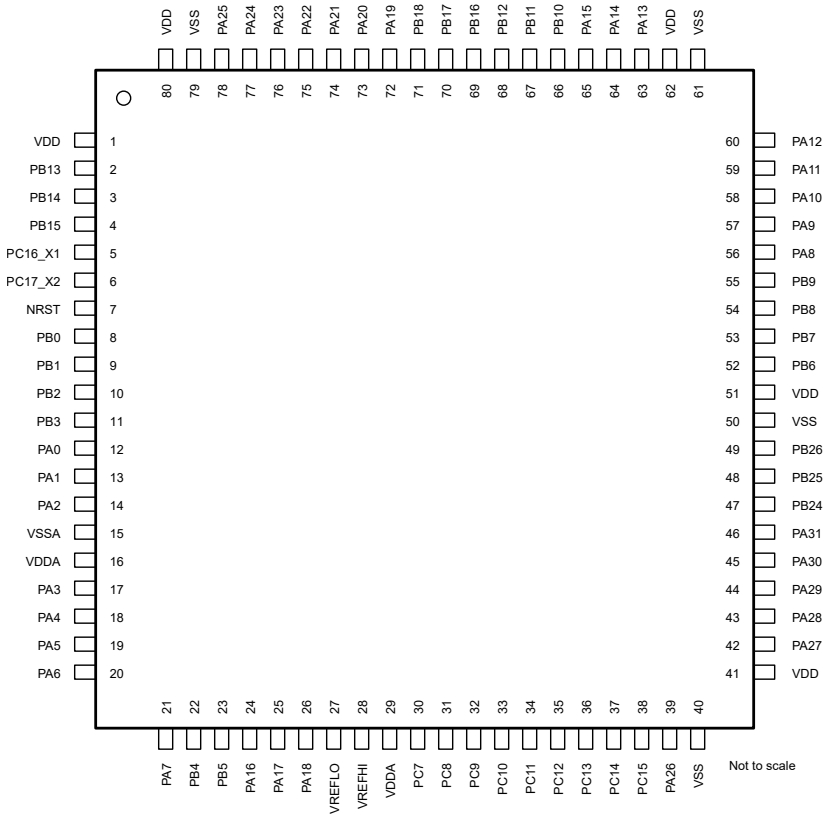


Figure 5-4. LQFP80 (PN) Package

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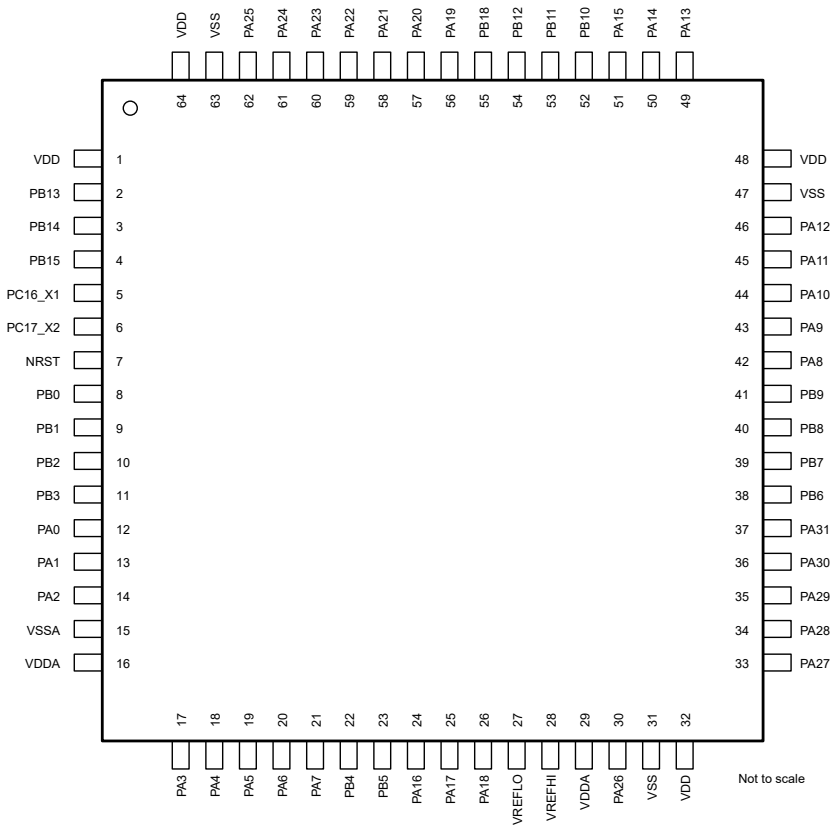


Figure 5-5. LQFP64_G (PM) Package

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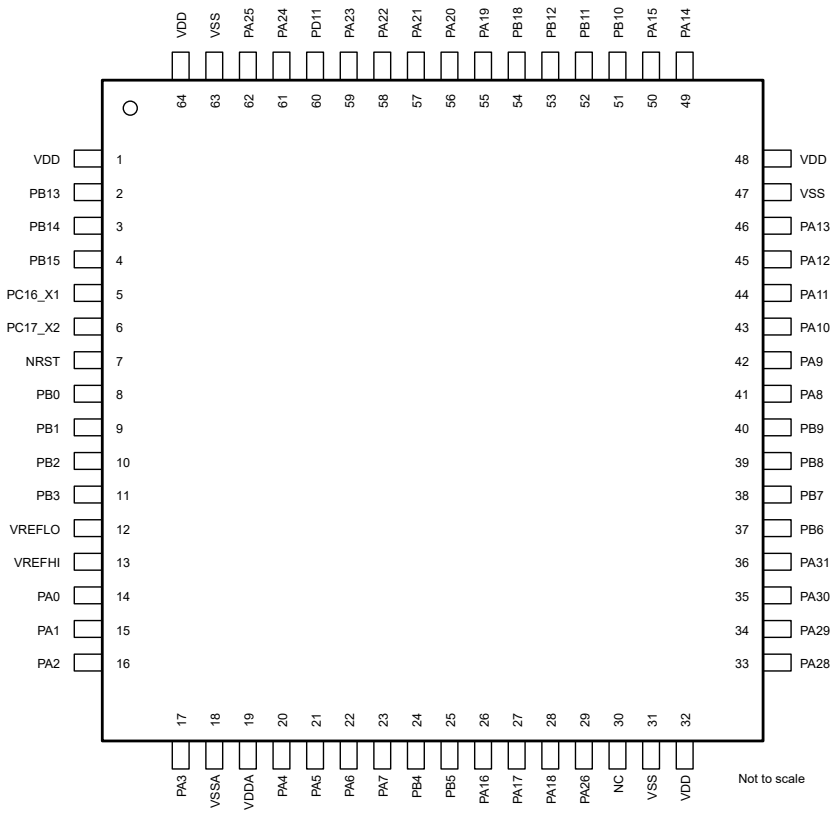


Figure 5-6. LQFP64_H (PM) Package

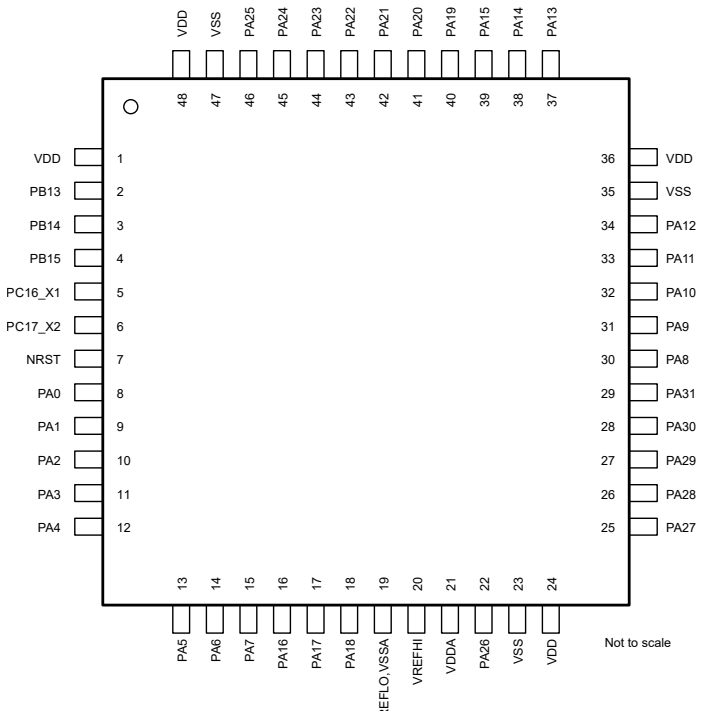


Figure 5-7. LQFP48 (PT) Package

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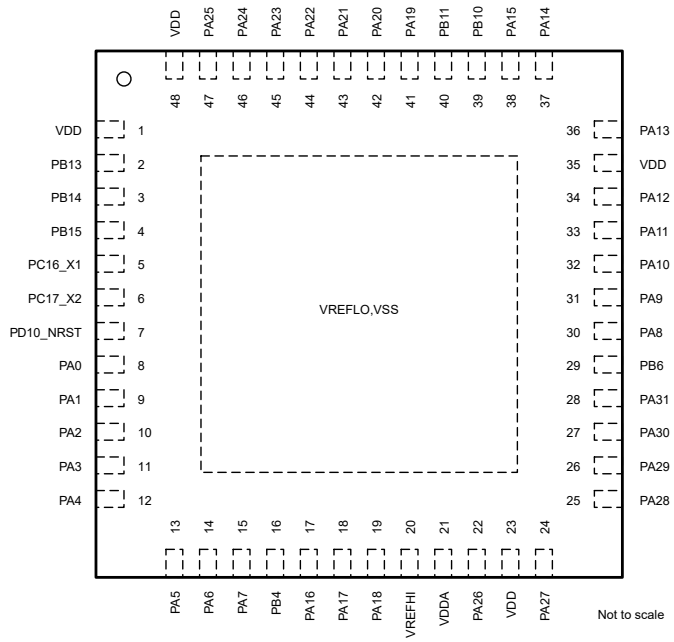


Figure 5-8. QFN48 (RGZ) Package

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5.3 Pin Attributes

The following table describes the function available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 5-1. Digital IO Features by IO Type

IO TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SD (standard drive IO)	Y		Y	Y	
SDL (standard drive IO) with low leakage	Y		Y	Y	
SDW (standard drive IO) with wakeup	Y		Y	Y	Y
HS (High speed IO)	Y	Y	Y	Y	

5.3.1 Pin Attributes Header List

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - An empty box or "-" means Not Applicable.

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Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
6. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
7. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
		48			30			NC		NC	0	NC
21	14	14	7	7	7	7	7	NRST IOMUX_PD10_NRST 0x400C_C1A8		NRST	0	RST
27	20	23	12	12	14	8	8	PA0 IOMUX_PA0 0x400C_C000	SDW	ANALOG_AIN6	A	A
										A0_1	AMUX0	A
										Disconnected	0	NA
										GPIO00	1	IO
										A1_1	AMUX1	A
										CMP0_HN0	AMUX2	A
										MCPWM4_1A	2	O
										MCPWM3_1A	3	O
										CMP2_HP0_LP0	AMUX3	A
										TIMG12_0_CCP0	4	IO
										TIMG4_0_CCP0	5	IO
										UC5_RX_SCL	6	IO
										UC4_TX_SDA_PICO	7	O
										UC1_CTS_CS0	8	IO
										UC1_TX_SDA_PICO	9	O
										MCPWM4_2A	10	O
										UC2_RX_SCL	11	IO
										UC0_CTS_CS0	13	IO
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
28	21	24	13	13	15	9	9	PA1 IOMUX_PA1 0x400C_C004	SDL	*Disconnected*	0	NA
										A0_2	AMUX0	A
										ANALOG_AIN7	A	A
										A1_2	AMUX1	A
										GPIO01	1	IO
										MCPWM4_1B	2	O
										CMP0_HP1_LP1	AMUX2	A
										PGA0_P1	AMUX3	A
										MCPWM3_2A	3	O
										PGA1_M0	AMUX4	A
										TIMG12_0_CCP1	4	IO
										TIMG4_0_CCP1	5	IO
										PGA2_P2	AMUX5	A
										UC5_TX_SDA	6	O
										UC4_RX_SCL_SCLK	7	IO
										UC1_RTS_POCI	8	O
										UC1_RX_SCL_SCLK	9	IO
										MCPWM3_1B	10	O
										UC2_TX_SDA	11	O
										MCPWM4_2B	12	O
										UC0_RTS_POCI	13	O
										OUTPUTXBAR4	16	O
29	22	25	14	14	16	10	10	PA2 IOMUX_PA2 0x400C_C008	SDW	A0_3	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN8	A	A
										A2_25	AMUX1	A
										GPIO02	1	IO
										MCPWM4_2A	2	O
										CMP1_HN0	AMUX2	A
										PGA0_OUT	AMUX3	A
										MCPWM3_1B	3	O
										MCPWM3_3A	4	O
										MCPWM4_3A	5	O
										MCPWM4_2B	6	O
										UC1_TX_SDA_PICO	8	O
										MCPWM3_1A	10	O
										UC0_TX_SDA_PICO	13	O
										OUTPUTXBAR5	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
32	25	26	17	17	17	11	11	PA3 IOMUX_PA3 0x400C_C00C	SDL	A0_4	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN9	A	A
										A2_21	AMUX1	A
										GPIO03	1	IO
										SYSCTL_HFCLKIN	2	A
										CMP1_HP0_LP0	AMUX2	A
										PGA0_M0	AMUX3	A
										MCPWM3_2B	3	O
										PGA0_P2	AMUX4	A
										TIMG4_0_CCP0	4	IO
										TIMG12_0_CCP0	5	IO
										PGA2_M0	AMUX5	A
										MCPWM3_3B	6	O
										MCPWM4_2B	7	O
										UC1_RX_SCL_SCLK	8	IO
										MCPWM3_2A	10	O
										UC0_RX_SCL_SCLK	13	IO
										OUTPUTXBAR6	16	O
33	26	29	18	18	20	12	12	PA4 IOMUX_PA4 0x400C_C010	SDL	ANALOG_AIN10	A	A
										A1_17	AMUX0	A
										Disconnected	0	NA
										GPIO04	1	IO
										A2_18	AMUX1	A
										CMP2_DACL	AMUX2	A
										SYSCTL_XCLKOUT	2	O
										MCPWM4_3B	3	O
										CMP0_HN1	AMUX3	A
										TIMG4_0_CCP1	4	IO
										INTERNAL_TESTANA0	AMUX4	Internal/A
										TIMG12_0_CCP1	5	IO
										UC0_RTS_POCI	6	O
										UC2_RTS	7	O
										UC3_RTS_POCI	9	O
										UC5_RTS	11	O
										OUTPUTXBAR6	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
34	27	30	19	19	21	13	13	PA5 IOMUX_PA5 0x400C_C014	SDL	A1_13	AMUX0	A
										ANALOG_AIN11	A	A
										Disconnected	0	NA
										A2_19	AMUX1	A
										GPIO05	1	IO
										MCPWM4_1A	2	O
										CMP1_HN1	AMUX2	A
										PGA1_M1	AMUX3	A
										MCPWM2_1B	3	O
										INTERNAL_TESTANA1	AMUX4	Internal/A
										MCPWM3_1B	4	O
										UC0_RX_SCL_SCLK	6	IO
										UC3_RX_SCL_SCLK	9	IO
										OUTPUTXBAR7	16	O
35	28	31	20	20	22	14	14	PA6 IOMUX_PA6 0x400C_C018	SDL	ANALOG_AIN12	A	A
										A0_17	AMUX0	A
										Disconnected	0	NA
										GPIO06	1	IO
										A1_3	AMUX1	A
										A2_26	AMUX2	A
										MCPWM3_1A	2	O
										MCPWM3_3A	3	O
										CMP3_DACL	AMUX3	A
										MCPWM4_2A	4	O
										PGA1_OUT	AMUX4	A
										ADCCAL_ADCINCAL0	AMUX5	A
										UC0_CTS_CS0	6	IO
										UC3_CTS_CS0	9	IO
										UC3_RTS_POCI	11	O
										UC0_RTS_POCI	13	O
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
36	29	32	21	21	23	15	15	PA7 IOMUX_PA7 0x400C_C01C	SDL	A1_4	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN13	A	A
										A2_22	AMUX1	A
										GPIO07	1	IO
										MCPWM3_3A	2	O
										CMP1_HP1_LP1	AMUX2	A
										PGA0_P3	AMUX3	A
										MCPWM3_3B	3	O
										PGA1_P1	AMUX4	A
										MCPWM4_1A	4	O
										MCPWM1_1B	5	O
										UC0_TX_SDA_PICO	6	O
										MCPWM0_1B	7	O
										MCPWM4_1B	8	O
										UC3_TX_SDA_PICO	9	O
										MCPWM4_3A	10	O
										MCPWM4_2B	11	O
										OUTPUTXBAR1	16	O
89	69	67	56	42	41	30	30	PA8 IOMUX_PA8 0x400C_C020	SDL	*Disconnected*	0	NA
										ANALOG_AIN42	A	A
										A1_18	AMUX0	A
										GPIO08	1	IO
										UC0_RX_SCL_SCLK	3	IO
										UC1_TX_SDA_PICO	5	O
										MCPWM4_1A	6	O
										MCPWM0_1A	7	O
										UC3_RX_SCL_SCLK	9	IO
										UC4_TX_SDA_PICO	10	O
										MCAN0_TX	12	O
										MCPWM3_1A	14	O
										MCPWM4_2A	15	O
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
90	70	68	57	43	42	31	31	PA9 IOMUX_PA9 0x400C_C024	SDL	*Disconnected*	0	NA
										A1_19	AMUX0	A
										ANALOG_AIN43	A	A
										GPIO09	1	IO
										UC1_RX_SCL_SCLK	5	IO
										UC4_RX_SCL_SCLK	6	IO
										MCPWM0_2A	7	O
										UC0_TX_SDA_PICO	8	O
										UC5_RTS	9	O
										UC4_TX_SDA_PICO	10	O
										MCPWM4_2A	11	O
										UC2_RTS	12	O
										MCPWM3_3A	13	O
										MCPWM3_1B	14	O
										MCPWM4_2B	15	O
										OUTPUTXBAR4	16	O
91	71	69	58	44	43	32	32	PA10 IOMUX_PA10 0x400C_C028	SDL	*Disconnected*	0	NA
										GPIO10	1	IO
										MCPWM4_3A	4	O
										UC4_TX_SDA_PICO	5	O
										UC1_TX_SDA_PICO	6	O
										MCPWM0_3A	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC5_RX_SCL	9	IO
										UC4_RX_SCL_SCLK	10	IO
										MCPWM4_2B	11	O
										UC2_RX_SCL	12	IO
										MCPWM3_3B	13	O
										MCPWM3_2A	14	O
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
92	72	70	59	45	44	33	33	PA11 IOMUX_PA11 0x400C_C02C	SDL	*Disconnected*	0	NA
										GPIO11	1	IO
										MCPWM4_2A	2	O
										UC3_CTS_CS0	3	IO
										UC2_TX_SDA	4	O
										UC4_CTS_CS0	5	IO
										UC1_CTS_CS0	6	IO
										MCPWM0_1B	7	O
										UC0_CTS_CS0	8	IO
										UC5_TX_SDA	9	O
										MCAN0_RX	10	I
										MCPWM2_2A	11	O
										MCPWM0_1A	12	O
										MCPWM4_1B	13	O
										MCPWM3_2B	14	O
										MCPWM4_1A	15	O
										OUTPUTXBAR5	16	O
93	73	71	60	46	45	34	34	PA12 IOMUX_PA12 0x400C_C030	HS	*Disconnected*	0	NA
										GPIO12	1	IO
										MCPWM3_1A	2	O
										MCPWM4_2A	3	O
										MCPWM3_2B	6	O
										MCPWM0_2B	7	O
										UC0_RTS_POCI	8	O
										UC3_RTS_POCI	9	O
										MCAN0_TX	10	O
										MCPWM2_2B	11	O
										MCPWM0_1B	12	O
										MCPWM4_2B	13	O
										MCPWM3_3B	14	O
										MCPWM4_1B	15	O
										OUTPUTXBAR6	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
96	76	72	63	49	46	37	36	PA13 IOMUX_PA13 0x400C_C034	SDL	*Disconnected*	0	NA
										GPIO13	1	IO
										DEBUG_TMS_SWDIO	2	IO
										MCPWM3_1B	3	O
										MCPWM4_2B	4	O
										UC0_RX_SCL_SCLK	5	IO
										UC3_RX_SCL_SCLK	6	IO
										UC0_CTS_CS0	8	IO
										SYSCTL_FCC_IN	9	I
										UC3_CTS_CS0	10	IO
										MCPWM2_3A	11	O
										MCPWM3_3A	12	O
										MCPWM4_3A	13	O
										OUTPUTXBAR7	16	O
98	77	76	64	50	49	38	37	PA14 IOMUX_PA14 0x400C_C038	SDL	*Disconnected*	0	NA
										GPIO14	1	IO
										DEBUG_JTCK_SWCLK	2	IO
										UC0_TX_SDA_PICO	5	O
										MCPWM1_2A	6	O
										MCPWM3_3A	7	O
										UC1_TX_SDA_PICO	8	O
										UC2_CTS	9	O
										UC5_CTS	10	O
										OUTPUTXBAR8	16	O
99	78	77	65	51	50	39	38	PA15 IOMUX_PA15 0x400C_C03C	HS	*Disconnected*	0	NA
										GPIO15	1	IO
										DEBUG_JTDI	2	I
										MCPWM3_1A	3	O
										MCPWM1_1A	4	O
										UC0_RX_SCL_SCLK	5	IO
										UC0_RTS_POCI	6	O
										UC3_RTS_POCI	7	O
										UC1_RX_SCL_SCLK	8	IO
										UC2_RTS	9	O
										UC5_RTS	10	O
										MCPWM4_2A	11	O
										MCAN0_RX	12	I
										OUTPUTXBAR1	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
39	32	35	24	24	26	16	17	PA16 IOMUX_PA16 0x400C_C040	SDL	ANALOG_AIN16	A	A
										Disconnected	0	NA
										A0_15	AMUX0	A
										GPIO16	1	IO
										A2_12	AMUX1	A
										CMP3_HP1_LP1	AMUX2	A
										MCPWM4_1A	3	O
										PGA1_P2	AMUX3	A
										MCPWM4_3B	4	O
										PGA2_P3	AMUX4	A
										MCPWM1_2B	5	O
										MCPWM4_2B	6	O
										MCPWM0_2B	7	O
										MCPWM3_3B	8	O
										SYSCTL_FCC_IN	9	I
										OUTPUTXBAR1	16	O
40	33	36	25	25	27	17	18	PA17 IOMUX_PA17 0x400C_C044	SDL	ANALOG_AIN17	A	A
										A0_12	AMUX0	A
										Disconnected	0	NA
										GPIO17	1	IO
										A2_1	AMUX1	A
										CMP0_HP0_LP0	AMUX2	A
										MCPWM4_1B	3	O
										PGA1_M3	AMUX3	A
										MCPWM2_1B	4	O
										PGA2_OUT	AMUX4	A
										MCPWM1_3B	5	O
										MCPWM4_3B	6	O
										MCPWM0_3B	7	O
										MCPWM3_1B	8	O
										UC3_RTS_POCI	11	O
										UC0_RTS_POCI	13	O
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
41	34	37	26	26	28	18	19	PA18 IOMUX_PA18 0x400C_C048	SDL	A1_12	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN18	A	A
										CMP3_HN0_LN0	AMUX1	A
										GPIO18	1	IO
										PGA2_M1	AMUX2	A
										MCPWM3_1A	3	O
										MCPWM2_1A	4	O
										MCPWM4_2A	5	O
										OUTPUTXBAR3	16	O
118	90	89	72	56	55	40	41	PA19 IOMUX_PA19 0x400C_C04C	HS	*Disconnected*	0	NA
										GPIO19	1	IO
										DEBUG_JTDO_SWO	2	O
										MCPWM4_1B	3	O
										MCPWM4_2B	4	O
										MCPWM1_1B	5	O
										UC0_RX_SCL_SCLK	6	IO
										UC3_RX_SCL_SCLK	7	IO
										UC1_TX_SDA_PICO	8	O
										UC3_TX_SDA_PICO	9	O
										MCAN0_RX	12	I
										OUTPUTXBAR2	16	O
119	91	90	73	57	56	41	42	PA20 IOMUX_PA20 0x400C_C050	SDL	*Disconnected*	0	NA
										GPIO20	1	IO
										MCPWM4_2A	2	O
										MCPWM3_1A	3	O
										MCPWM4_3A	4	O
										MCPWM1_2B	5	O
										UC0_CTS_CS0	6	IO
										UC3_CTS_CS0	7	IO
										UC1_RX_SCL_SCLK	8	IO
										UC3_RTS_POCI	9	O
										UC4_RX_SCL_SCLK	10	IO
										UC0_RTS_POCI	11	O
										MCAN0_TX	12	O
										MCPWM4_3B	13	O
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
120	92	91	74	58	57	42	43	PA21 IOMUX_PA21 0x400C_C054	SDL	*Disconnected*	0	NA
										GPIO21	1	IO
										MCPWM4_3B	3	O
										MCPWM1_3B	4	O
										MCPWM4_1B	5	O
										UC0_TX_SDA_PICO	6	O
										UC3_TX_SDA_PICO	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC3_RX_SCL_SCLK	9	IO
										MCAN0_RX	10	I
										MCPWM3_3A	11	O
										MCPWM4_3A	12	O
										UC0_CTS_CS0	14	IO
										UC3_CTS_CS0	15	IO
										OUTPUTXBAR4	16	O
121	93	92	75	59	58	43	44	PA22 IOMUX_PA22 0x400C_C058	SDL	*Disconnected*	0	NA
										GPIO22	1	IO
										MCPWM3_1B	2	O
										MCPWM2_2A	3	O
										UC2_TX_SDA	4	O
										MCPWM4_2B	5	O
										MCPWM1_1A	6	O
										UC5_TX_SDA	7	O
										UC0_TX_SDA_PICO	8	O
										UC3_TX_SDA_PICO	9	O
										MCAN0_TX	10	O
										MCPWM3_3B	11	O
										MCPWM4_3B	12	O
										EPI0_S30	13	IO
										MCPWM4_2A	14	O
										MCPWM3_2A	15	O
										OUTPUTXBAR5	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
122	94	93	76	60	59	44	45	PA23 IOMUX_PA23 0x400C_C05C	SDL	*Disconnected*	0	NA
										GPIO23	1	IO
										MCPWM3_3B	2	O
										MCPWM2_2B	3	O
										UC2_RX_SCL	4	IO
										UC0_TX_SDA_PICO	5	O
										MCPWM4_3B	6	O
										UC5_RX_SCL	7	IO
										UC0_RX_SCL_SCLK	8	IO
										UC3_RX_SCL_SCLK	9	IO
										UC3_TX_SDA_PICO	10	O
										MCPWM4_1B	11	O
										MCPWM3_2B	12	O
										MCPWM4_2B	13	O
										UC4_CTS_CS0	14	IO
										UC1_CTS_CS0	15	IO
										OUTPUTXBAR6	16	O
123	95	95	77	61	61	45	46	PA24 IOMUX_PA24 0x400C_C060	SDL	*Disconnected*	0	NA
										GPIO24	1	IO
										MCPWM3_1A	2	O
										MCPWM2_3A	3	O
										MCPWM4_2A	4	O
										UC0_RX_SCL_SCLK	5	IO
										UC3_RX_SCL_SCLK	6	IO
										MCPWM3_3A	7	O
										UC0_TX_SDA_PICO	8	O
										UC3_TX_SDA_PICO	9	O
										MCAN0_RX	10	I
										MCPWM1_2A	11	O
										MCPWM4_3A	12	O
										OUTPUTXBAR7	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
124	96	96	78	62	62	46	47	PA25 IOMUX_PA25 0x400C_C064	SDL	*Disconnected*	0	NA
										GPIO25	1	IO
										MCPWM3_3A	2	O
										MCPWM2_3B	3	O
										MCPWM4_3A	4	O
										UC0_TX_SDA_PICO	5	O
										UC3_TX_SDA_PICO	6	O
										MCPWM3_3B	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC3_RX_SCL_SCLK	9	IO
										MCAN0_TX	10	O
										MCPWM1_3A	11	O
										MCPWM4_3B	12	O
										MCPWM0_3B	13	O
										MCPWM4_1A	14	O
										OUTPUTXBAR7	16	O
62	47	47	39	30	29	22	22	PA26 IOMUX_PA26 0x400C_C068	SDL	*Disconnected*	0	NA
										A2_17	AMUX0	A
										ANALOG_AIN28	A	A
										CMP0_LN1	AMUX1	A
										GPIO26	1	IO
										MCPWM4_2A	2	O
										PGA2_M2	AMUX2	A
										PGA0_M2	AMUX3	A
										TIMG4_0_CCP0	3	IO
										TIMG12_0_CCP0	4	IO
										MCPWM3_3A	5	O
										MCPWM4_3A	6	O
										UC0_RX_SCL_SCLK	8	IO
										UC0_TX_SDA_PICO	9	O
										UC3_TX_SDA_PICO	10	O
										UC3_RX_SCL_SCLK	11	IO
										EPI0_S33	13	IO
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
65	50		42	33		25	24	PA27 IOMUX_PA27 0x400C_C06C	SDL	*Disconnected*	0	NA
										A0_14	AMUX0	A
										ANALOG_AIN29	A	A
										A1_14	AMUX1	A
										GPIO27	1	IO
										MCPWM4_2B	2	O
										CMP1_HP2_LP2	AMUX2	A
										PGA0_P4	AMUX3	A
										TIMG4_0_CCP1	3	IO
										PGA2_P0	AMUX4	A
										TIMG12_0_CCP1	4	IO
										MCPWM3_3B	5	O
										SYSCTL_XCLKOUT	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC0_TX_SDA_PICO	9	O
										UC3_TX_SDA_PICO	10	O
										UC3_RX_SCL_SCLK	11	IO
										OUTPUTXBAR3	16	O
66	51	51	43	34	33	26	25	PA28 IOMUX_PA28 0x400C_C070	SDL	ANALOG_AIN30	A	A
										A0_11	AMUX0	A
										Disconnected	0	NA
										GPIO28	1	IO
										A2_30	AMUX1	A
										CMP2_LN1	AMUX2	A
										TIMG12_0_CCP0	2	IO
										TIMG4_0_CCP0	3	IO
										PGA1_P3	AMUX3	A
										MCAN0_RX	4	I
										PGA0_P7	AMUX4	A
										UC1_RTS_POCI	6	O
										UC0_CTS_CS0	8	IO
										UC0_RTS_POCI	9	O
										UC4_RTS_POCI	10	O
										UC3_CTS_CS0	11	IO
										EPI0_S34	13	IO
										MCPWM3_3A	14	O
										MCPWM4_1A	15	O
										OUTPUTXBAR4	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
67	52	52	44	35	34	27	26	PA29 IOMUX_PA29 0x400C_C074	SDL	ANALOG_AIN31	A	A
										A2_5	AMUX0	A
										Disconnected	0	NA
										GPIO29	1	IO
										CMP0_HP2_LP2	AMUX1	A
										PGA0_P5	AMUX2	A
										TIMG12_0_CCP1	2	IO
										TIMG4_0_CCP1	3	IO
										PGA1_P4	AMUX3	A
										MCAN0_TX	4	O
										PGA2_P4	AMUX4	A
										MCPWM4_1B	6	O
										MCPWM0_1B	7	O
										SYSCTL_FCC_IN	8	I
										UC0_CTS_CS0	9	IO
										UC3_CTS_CS0	11	IO
										EPI0_S35	13	IO
										MCPWM3_3B	14	O
										MCPWM4_3B	15	O
										OUTPUTXBAR5	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
68	53	53	45	36	35	28	27	PA30 IOMUX_PA30 0x400C_C078	SDL	ANALOG_AIN32	A	A
										A0_5	AMUX0	A
										Disconnected	0	NA
										GPIO30	1	IO
										A2_27	AMUX1	A
										CMP2_HP3_LP3	AMUX2	A
										MCPWM3_1A	2	O
										MCPWM4_2A	3	O
										PGA1_P5	AMUX3	A
										MCPWM3_3B	4	O
										PGA2_P5	AMUX4	A
										MCPWM4_2B	5	O
										UC1_TX_SDA_PICO	6	O
										MCPWM0_2B	7	O
										UC0_RTS_POCI	8	O
										UC4_RTS_POCI	10	O
										UC4_TX_SDA_PICO	11	O
										MCPWM4_1A	14	O
										OUTPUTXBAR6	16	O
69	54	54	46	37	36	29	28	PA31 IOMUX_PA31 0x400C_C07C	SDL	ANALOG_AIN33	A	A
										A1_15	AMUX0	A
										Disconnected	0	NA
										GPIO31	1	IO
										A2_28	AMUX1	A
										CMP1_LN1	AMUX2	A
										MCPWM3_2A	2	O
										MCPWM3_1B	3	O
										PGA2_M3	AMUX3	A
										MCPWM4_3B	4	O
										MCPWM0_3B	5	O
										UC1_CTS_CS0	6	IO
										MCPWM4_2B	7	O
										UC4_CTS_CS0	11	IO
										MCPWM4_1B	14	O
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
22	15	15	8	8	8			PB0 IOMUX_PB0 0x400C_C080	SDL	ANALOG_AIN2	A	A
										Disconnected	0	NA
										A0_6	AMUX0	A
										A1_6	AMUX1	A
										GPIO32	1	IO
										CMP2_HN1	AMUX2	A
										MCPWM0_1A	3	O
										MCPWM4_1A	4	O
										UC0_RX_SCL_SCLK	9	IO
										UC3_RX_SCL_SCLK	11	IO
										OUTPUTXBAR5	16	O
23	16	16	9	9	9			PB1 IOMUX_PB1 0x400C_C084	SDW	A0_7	AMUX0	A
										ANALOG_AIN3	A	A
										Disconnected	0	NA
										GPIO33	1	IO
										A1_7	AMUX1	A
										CMP2_HP1_LP1	AMUX2	A
										MCPWM0_2A	3	O
										MCPWM4_2A	4	O
										MCPWM3_3A	5	O
										UC0_TX_SDA_PICO	9	O
										UC3_TX_SDA_PICO	11	O
										OUTPUTXBAR6	16	O
24	17	17	10	10	10			PB2 IOMUX_PB2 0x400C_C088	SDL	A0_8	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN4	A	A
										GPIO34	1	IO
										A1_8	AMUX1	A
										MCPWM0_3A	3	O
										MCPWM4_3A	4	O
										MCPWM4_2A	6	O
										MCPWM2_2A	7	O
										MCPWM3_2A	8	O
										OUTPUTXBAR7	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
25	18	18	11	11	11			PB3 IOMUX_PB3 0x400C_C08C	SDL	*Disconnected*	0	NA
										ANALOG_AIN5	A	A
										A0_9	AMUX0	A
										GPIO35	1	IO
										A1_9	AMUX1	A
										PGA2_P1	AMUX2	A
										MCPWM0_1A	3	O
										PGA0_P0	AMUX3	A
										MCPWM4_1A	4	O
										PGA1_P0	AMUX4	A
										OUTPUTXBAR8	16	O
37	30	33	22	22	24		16	PB4 IOMUX_PB4 0x400C_C090	SDL	A1_5	AMUX0	A
										ANALOG_AIN14	A	A
										Disconnected	0	NA
										A2_23	AMUX1	A
										GPIO36	1	IO
										UC1_RX_SCL_SCLK	5	IO
										UC0_TX_SDA_PICO	8	O
										UC3_TX_SDA_PICO	9	O
										MCAN0_RX	10	I
										UC4_RX_SCL_SCLK	11	IO
										OUTPUTXBAR2	16	O
38	31	34	23	23	25			PB5 IOMUX_PB5 0x400C_C094	SDW	*Disconnected*	0	NA
										ANALOG_AIN15	A	A
										A1_11	AMUX0	A
										A2_24	AMUX1	A
										GPIO37	1	IO
										PGA0_M1	AMUX2	A
										PGA1_M2	AMUX3	A
										MCPWM4_1B	6	O
										MCPWM0_1B	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC3_RX_SCL_SCLK	9	IO
										MCAN0_TX	10	O
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
80	65	63	52	38	37		29	PB6 IOMUX_PB6 0x400C_C098	SDL	*Disconnected*	0	NA
										GPIO38	1	IO
										MCPWM3_3A	3	O
										MCPWM1_1A	5	O
										MCPWM4_2A	6	O
										UC5_RX_SCL	8	IO
										UC2_RX_SCL	9	IO
										MCPWM4_3B	14	O
										OUTPUTXBAR3	16	O
81	66	64	53	39	38			PB7 IOMUX_PB7 0x400C_C09C	SDL	*Disconnected*	0	NA
										GPIO39	1	IO
										MCPWM3_3B	3	O
										MCPWM4_3A	4	O
										MCPWM1_2A	5	O
										UC5_TX_SDA	8	O
										UC2_TX_SDA	9	O
										OUTPUTXBAR4	16	O
87	67	65	54	40	39			PB8 IOMUX_PB8 0x400C_C0A0	SDL	*Disconnected*	0	NA
										GPIO40	1	IO
										TRACE_DATA1	2	O
										MCPWM3_1A	3	O
										MCPWM4_2A	4	O
										MCPWM1_3A	5	O
										UC2_CTS	6	O
										MCPWM2_3A	7	O
										MCPWM3_3A	8	O
										UC0_RX_SCL_SCLK	9	IO
										UC3_RX_SCL_SCLK	10	IO
										UC5_RTS	11	O
										MCPWM4_3A	13	O
										MCPWM4_3B	14	O
										MCPWM3_3B	15	O
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
88	68	66	55	41	40			PB9 IOMUX_PB9 0x400C_C0A4	SDL	*Disconnected*	0	NA
										GPIO41	1	IO
										MCPWM3_1B	3	O
										MCPWM4_2B	4	O
										MCPWM1_1A	5	O
										UC2_RTS	6	O
										MCPWM4_2A	7	O
										MCPWM3_3B	8	O
										UC0_TX_SDA_PICO	9	O
										UC3_TX_SDA_PICO	10	O
										UC5_CTS	11	O
										OUTPUTXBAR3	16	O
100	79	78	66	52	51		39	PB10 IOMUX_PB10 0x400C_C0A8	SDL	*Disconnected*	0	NA
										GPIO42	1	IO
										UC5_TX_SDA	4	O
										MCPWM1_1B	5	O
										UC2_TX_SDA	6	O
										UC3_RX_SCL_SCLK	7	IO
										UC0_TX_SDA_PICO	8	O
										UC0_RX_SCL_SCLK	9	IO
										UC3_TX_SDA_PICO	10	O
										MCPWM3_2B	11	O
										OUTPUTXBAR2	16	O
101	80	79	67	53	52		40	PB11 IOMUX_PB11 0x400C_C0AC	SDL	*Disconnected*	0	NA
										GPIO43	1	IO
										TRACE_CLK	2	IO
										UC5_RX_SCL	4	IO
										MCPWM1_2B	5	O
										UC2_RX_SCL	6	IO
										UC3_CTS_CS0	7	IO
										UC0_RX_SCL_SCLK	8	IO
										UC0_TX_SDA_PICO	9	O
										UC0_CTS_CS0	10	IO
										UC3_RX_SCL_SCLK	11	IO
										UC3_TX_SDA_PICO	13	O
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
102	81	80	68	54	53			PB12 IOMUX_PB12 0x400C_C0B0	SDL	*Disconnected*	0	NA
										GPIO44	1	IO
										TRACE_DATA3	2	O
										MCPWM3_1B	3	O
										MCPWM4_2B	4	O
										MCPWM1_3B	5	O
										UC3_TX_SDA_PICO	6	O
										UC3_RX_SCL_SCLK	7	IO
										UC0_RX_SCL_SCLK	8	IO
										MCPWM4_1B	9	O
										UC0_TX_SDA_PICO	11	O
										EPI0_S27	13	IO
										OUTPUTXBAR4	16	O
7	7	7	2	2	2	2	2	PB13 IOMUX_PB13 0x400C_C0B4	SDW	*Disconnected*	0	NA
										GPIO45	1	IO
										SYSCTL_XCLKOUT	2	O
										MCPWM0_1B	5	O
										MCPWM3_1B	6	O
										MCPWM1_1B	7	O
										SYSCTL_FCC_IN	8	I
										MCPWM4_2B	9	O
										OUTPUTXBAR6	16	O
8	8	8	3	3	3	3	3	PB14 IOMUX_PB14 0x400C_C0B8	SDL	*Disconnected*	0	NA
										GPIO46	1	IO
										SYSCTL_XCLKOUT	2	O
										UC0_TX_SDA_PICO	8	O
										MCAN0_RX	10	I
										UC3_TX_SDA_PICO	11	O
										OUTPUTXBAR1	16	O
9	9	9	4	4	4	4	4	PB15 IOMUX_PB15 0x400C_C0BC	SDL	*Disconnected*	0	NA
										GPIO47	1	IO
										UC0_RX_SCL_SCLK	8	IO
										MCAN0_TX	10	O
										UC3_RX_SCL_SCLK	11	IO
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
108	82	81	69					PB16 IOMUX_PB16 0x400C_C0C0	SDL	*Disconnected*	0	NA
										GPIO48	1	IO
										UC5_TX_SDA	4	O
										MCPWM1_1B	7	O
										MCPWM3_2B	8	O
										MCAN0_TX	10	O
										UC2_TX_SDA	11	O
										EPI0_S2	13	IO
										OUTPUTXBAR2	16	O
109	83	82	70					PB17 IOMUX_PB17 0x400C_C0C4	SDL	*Disconnected*	0	NA
										GPIO49	1	IO
										UC5_RX_SCL	4	IO
										MCPWM1_1A	5	O
										MCPWM3_2A	6	O
										MCAN0_RX	10	I
										UC2_RX_SCL	11	IO
										EPI0_S3	13	IO
										OUTPUTXBAR3	16	O
112	84	83	71	55	54			PB18 IOMUX_PB18 0x400C_C0C8	HS	*Disconnected*	0	NA
										GPIO50	1	IO
										TRACE_DATA2	2	O
										UC5_CTS	4	O
										UC3_RX_SCL_SCLK	6	IO
										UC3_TX_SDA_PICO	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC0_TX_SDA_PICO	9	O
										UC2_CTS	11	O
										EPI0_S31	13	IO
										OUTPUTXBAR4	16	O
113	85	84						PB19 IOMUX_PB19 0x400C_C0CC	SDW	*Disconnected*	0	NA
										GPIO51	1	IO
										MCPWM4_1A	3	O
										UC5_RTS	4	O
										UC1_CTS_CS0	8	IO
										UC4_CTS_CS0	10	IO
										UC2_RTS	11	O
										EPI0_S28	13	IO
										OUTPUTXBAR5	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
114	86	85						PB20 IOMUX_PB20 0x400C_C0D0	SDL	*Disconnected*	0	NA
										GPIO52	1	IO
										MCPWM4_1B	3	O
										UC1_RTS_POCI	8	O
										UC4_RTS_POCI	10	O
										EPI0_S29	13	IO
										OUTPUTXBAR6	16	O
115	87	86						PB21 IOMUX_PB21 0x400C_C0D4	SDL	*Disconnected*	0	NA
										GPIO53	1	IO
										UC1_TX_SDA_PICO	8	O
										UC4_TX_SDA_PICO	10	O
										EPI0_S32	13	IO
										OUTPUTXBAR7	16	O
116	88	87						PB22 IOMUX_PB22 0x400C_C0D8	SDL	*Disconnected*	0	NA
										GPIO54	1	IO
										MCPWM4_2B	3	O
										MCPWM3_3B	4	O
										MCPWM4_3B	5	O
										UC1_RX_SCL_SCLK	8	IO
										UC4_RX_SCL_SCLK	10	IO
										EPI0_S26	13	IO
										OUTPUTXBAR8	16	O
117	89	88						PB23 IOMUX_PB23 0x400C_C0DC	SDL	*Disconnected*	0	NA
										GPIO55	1	IO
										MCPWM4_2A	3	O
										MCPWM3_3A	4	O
										MCPWM4_3A	5	O
										OUTPUTXBAR1	16	O
70	55	55	47					PB24 IOMUX_PB24 0x400C_C0E0	SDL	ANALOG_AIN34	A	A
										Disconnected	0	NA
										A0_21	AMUX0	A
										A1_21	AMUX1	A
										GPIO56	1	IO
										PGA0_M3	AMUX2	A
										UC5_RX_SCL	9	IO
										UC2_RX_SCL	11	IO
										EPI0_S13	13	IO
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
71	56	56	48					PB25 IOMUX_PB25 0x400C_C0E4	SDL	ANALOG_AIN35	A	A
										Disconnected	0	NA
										A0_22	AMUX0	A
										A1_22	AMUX1	A
										GPIO57	1	IO
										PGA1_P6	AMUX2	A
										PGA2_P7	AMUX3	A
										UC5_TX_SDA	9	O
										UC2_TX_SDA	11	O
										EPI0_S14	13	IO
										OUTPUTXBAR4	16	O
72	57	57	49					PB26 IOMUX_PB26 0x400C_C0E8	SDL	ANALOG_AIN36	A	A
										Disconnected	0	NA
										A0_26	AMUX0	A
										GPIO58	1	IO
										A1_26	AMUX1	A
										A2_7	AMUX2	A
										TIMG4_0_CCP0	2	IO
										CMP1_LN0	AMUX3	A
										EPI0_S15	13	IO
										OUTPUTXBAR5	16	O
73	58	58						PB27 IOMUX_PB27 0x400C_C0EC	SDL	ANALOG_AIN37	A	A
										Disconnected	0	NA
										A0_27	AMUX0	A
										GPIO59	1	IO
										A1_27	AMUX1	A
										A2_8	AMUX2	A
										TIMG4_0_CCP1	2	IO
										CMP1_HP3_LP3	AMUX3	A
										PGA0_P6	AMUX4	A
										PGA1_P8	AMUX5	A
										PGA2_P8	AMUX6	A
										UC0_CTS_CS0	8	IO
										UC5_CTS	9	O
										UC2_CTS	10	O
										UC3_CTS_CS0	11	IO
										EPI0_S16	13	IO
										OUTPUTXBAR6	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
74	59	59						PB28 IOMUX_PB28 0x400C_C0F0	SDL	ANALOG_AIN38	A	A
										Disconnected	0	NA
										A0_28	AMUX0	A
										GPIO60	1	IO
										A1_28	AMUX1	A
										A2_9	AMUX2	A
										TIMG4_0_CCP0	2	IO
										MCPWM2_2A	3	O
										CMP0_HP3_LP3	AMUX3	A
										MCPWM3_2A	4	O
										PGA2_P6	AMUX4	A
										PGA0_P8	AMUX5	A
										MCPWM4_2A	5	O
										UC0_RTS_POCI	8	O
										UC5_RTS	9	O
										UC2_RTS	10	O
										UC3_RTS_POCI	11	O
										EPI0_S17	13	IO
										OUTPUTXBAR7	16	O
75	60	60						PB29 IOMUX_PB29 0x400C_C0F4	SDL	ANALOG_AIN39	A	A
										A0_29	AMUX0	A
										Disconnected	0	NA
										GPIO61	1	IO
										A1_29	AMUX1	A
										A2_10	AMUX2	A
										TIMG4_0_CCP1	2	IO
										MCPWM2_2B	3	O
										CMP0_LN0	AMUX3	A
										MCPWM3_2B	4	O
										MCPWM4_2B	5	O
										UC5_RX_SCL	6	IO
										UC5_TX_SDA	8	O
										UC2_RX_SCL	10	IO
										UC2_TX_SDA	11	O
										EPI0_S18	13	IO
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
76	61	61						PB30 IOMUX_PB30 0x400C_C0F8	SDL	A0_30	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN40	A	A
										A1_30	AMUX1	A
										GPIO62	1	IO
										TIMG4_0_CCP0	2	IO
										A2_11	AMUX2	A
										CMP2_HP2_LP2	AMUX3	A
										MCPWM2_3A	3	O
										PGA1_P7	AMUX4	A
										MCPWM3_3A	4	O
										MCPWM4_3A	5	O
										UC5_TX_SDA	6	O
										UC5_RX_SCL	8	IO
										UC2_TX_SDA	10	O
										UC2_RX_SCL	11	IO
										EPI0_S0	13	IO
										OUTPUTXBAR1	16	O
77	62	62						PB31 IOMUX_PB31 0x400C_C0FC	SDL	A2_29	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN41	A	A
										GPIO63	1	IO
										CMP2_LN0	AMUX1	A
										TIMG4_0_CCP1	2	IO
										MCPWM2_3B	3	O
										MCPWM3_3B	4	O
										MCPWM4_3B	5	O
										UC1_RTS_POCI	7	O
										UC4_RTS_POCI	11	O
										EPI0_S1	13	IO
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
125	97	97						PC0 IOMUX_PC0 0x400C_C100	SDL	*Disconnected*	0	NA
										GPIO64	1	IO
										MCPWM3_1B	3	O
										MCPWM2_1B	4	O
										MCPWM3_1A	5	O
										MCPWM4_2A	6	O
										UC0_TX_SDA_PICO	8	O
										UC3_TX_SDA_PICO	9	O
										EPI0_S24	13	IO
										OUTPUTXBAR1	16	O
126	98	98						PC1 IOMUX_PC1 0x400C_C104	SDL	*Disconnected*	0	NA
										GPIO65	1	IO
										TRACE_DATA0	2	O
										MCPWM4_1A	4	O
										MCPWM3_3A	5	O
										MCPWM3_1A	6	O
										MCPWM2_1A	7	O
										UC0_RX_SCL_SCLK	8	IO
										UC3_RX_SCL_SCLK	9	IO
										EPI0_S25	13	IO
										OUTPUTXBAR2	16	O
1	1	1						PC2 IOMUX_PC2 0x400C_C108	SDL	*Disconnected*	0	NA
										GPIO66	1	IO
										TRACE_CLK	2	IO
										MCPWM4_3A	3	O
										UC5_RX_SCL	5	IO
										UC3_RX_SCL_SCLK	6	IO
										MCPWM2_1A	7	O
										SYSCTL_FCC_IN	8	I
										MCPWM3_1A	9	O
										UC2_RX_SCL	10	IO
										UC0_RX_SCL_SCLK	11	IO
										EPI0_S23	13	IO
										OUTPUTXBAR1	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
2	2	2						PC3 IOMUX_PC3 0x400C_C10C	SDL	*Disconnected*	0	NA
										GPIO67	1	IO
										TRACE_DATA0	2	O
										MCPWM4_3B	3	O
										MCPWM4_2A	4	O
										UC5_TX_SDA	5	O
										UC3_RTS_POCI	6	O
										MCPWM2_2A	7	O
										MCPWM3_2A	8	O
										UC2_TX_SDA	10	O
										UC0_RTS_POCI	11	O
										EPI0_S19	13	IO
										OUTPUTXBAR2	16	O
3	3	3						PC4 IOMUX_PC4 0x400C_C110	SDL	*Disconnected*	0	NA
										GPIO68	1	IO
										TRACE_DATA1	2	O
										MCPWM4_1A	3	O
										UC3_RTS_POCI	6	O
										MCPWM2_1B	7	O
										MCPWM3_1B	8	O
										UC0_RTS_POCI	11	O
										EPI0_S20	13	IO
										OUTPUTXBAR3	16	O
4	4	4						PC5 IOMUX_PC5 0x400C_C114	SDL	*Disconnected*	0	NA
										GPIO69	1	IO
										TRACE_DATA2	2	O
										MCPWM4_1B	3	O
										MCPWM4_2B	4	O
										UC3_CTS_CS0	6	IO
										MCPWM2_2B	7	O
										MCPWM3_2B	8	O
										UC0_CTS_CS0	11	IO
										EPI0_S21	13	IO
										OUTPUTXBAR4	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
5	5	5						PC6 IOMUX_PC6 0x400C_C118	SDW	*Disconnected*	0	NA
										GPIO70	1	IO
										TRACE_DATA3	2	O
										MCPWM3_3B	4	O
										UC3_TX_SDA_PICO	6	O
										MCPWM2_3B	7	O
										UC0_TX_SDA_PICO	11	O
										EPI0_S22	13	IO
										OUTPUTXBAR5	16	O
53	38	38	30					PC7 IOMUX_PC7 0x400C_C11C	SDL	A2_4	AMUX0	A
										ANALOG_AIN19	A	A
										Disconnected	0	NA
										CMP3_HP0_LP0	AMUX1	A
										GPIO71	1	IO
										UC0_RTS_POCI	7	O
										UC5_RX_SCL	8	IO
										UC2_RX_SCL	11	IO
										EPI0_S4	13	IO
										OUTPUTXBAR1	16	O
54	39	39	31					PC8 IOMUX_PC8 0x400C_C120	SDL	A0_23	AMUX0	A
										ANALOG_AIN20	A	A
										Disconnected	0	NA
										GPIO72	1	IO
										A1_23	AMUX1	A
										MCPWM3_2A	2	O
										A2_6	AMUX2	A
										CMP3_HN1_LN1	AMUX3	A
										MCPWM0_1B	3	O
										MCPWM4_1B	4	O
										MCPWM0_2B	7	O
										UC5_TX_SDA	8	O
										UC2_TX_SDA	11	O
										EPI0_S5	13	IO
										OUTPUTXBAR2	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
55	40	40	32					PC9 IOMUX_PC9 0x400C_C124	SDL	A2_2	AMUX0	A
										ANALOG_AIN21	A	A
										Disconnected	0	NA
										GPIO73	1	IO
										CMP3_HP2_LP2	AMUX1	A
										MCPWM3_2B	2	O
										MCPWM0_1A	3	O
										MCPWM4_1A	4	O
										MCPWM0_3B	7	O
										EPI0_S6	13	IO
										OUTPUTXBAR3	16	O
56	41	41	33					PC10 IOMUX_PC10 0x400C_C128	SDL	A0_16	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN22	A	A
										GPIO74	1	IO
										A1_16	AMUX1	A
										A2_14	AMUX2	A
										MCPWM0_2B	3	O
										MCPWM4_2B	4	O
										MCPWM3_3B	5	O
										MCPWM0_1B	7	O
										EPI0_S7	13	IO
										OUTPUTXBAR4	16	O
57	42	42	34					PC11 IOMUX_PC11 0x400C_C12C	SDL	ANALOG_AIN23	A	A
										Disconnected	0	NA
										A0_24	AMUX0	A
										A1_24	AMUX1	A
										GPIO75	1	IO
										A2_15	AMUX2	A
										MCPWM0_2A	3	O
										MCPWM4_2A	4	O
										MCPWM3_3A	5	O
										UC3_RTS_POCI	6	O
										UC0_RTS_POCI	11	O
										EPI0_S8	13	IO
										OUTPUTXBAR5	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
58	43	43	35					PC12 IOMUX_PC12 0x400C_C130	SDL	*Disconnected*	0	NA
										ANALOG_AIN24	A	A
										A0_25	AMUX0	A
										A1_25	AMUX1	A
										GPIO76	1	IO
										A2_16	AMUX2	A
										MCPWM0_3B	3	O
										MCPWM4_3B	4	O
										UC3_RX_SCL_SCLK	6	IO
										UC0_RX_SCL_SCLK	11	IO
										EPI0_S9	13	IO
										OUTPUTXBAR6	16	O
59	44	44	36					PC13 IOMUX_PC13 0x400C_C134	SDL	*Disconnected*	0	NA
										ANALOG_AIN25	A	A
										A2_3	AMUX0	A
										GPIO77	1	IO
										MCPWM0_3A	3	O
										MCPWM4_3A	4	O
										UC3_CTS_CS0	6	IO
										UC0_CTS_CS0	11	IO
										EPI0_S26	12	IO
										EPI0_S10	13	IO
										OUTPUTXBAR7	16	O
60	45	45	37					PC14 IOMUX_PC14 0x400C_C138	SDL	A0_18	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN26	A	A
										GPIO78	1	IO
										MCPWM0_1A	3	O
										MCPWM4_1A	4	O
										MCPWM4_1B	5	O
										UC3_TX_SDA_PICO	6	O
										MCPWM0_1B	7	O
										UC0_TX_SDA_PICO	11	O
										EPI0_S11	13	IO
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
61	46	46	38					PC15 IOMUX_PC15 0x400C_C13C	SDL	*Disconnected*	0	NA
										ANALOG_AIN27	A	A
										A0_19	AMUX0	A
										GPIO79	1	IO
										CMP3_HP3_LP3	AMUX1	A
										MCPWM4_1A	5	O
										MCPWM0_1A	7	O
										UC0_TX_SDA_PICO	8	O
										UC0_RX_SCL_SCLK	9	IO
										UC3_RX_SCL_SCLK	10	IO
										UC3_TX_SDA_PICO	11	O
										EPI0_S12	13	IO
										OUTPUTXBAR1	16	O
26	19							PC18 IOMUX_PC18 0x400C_C148	SDL	*Disconnected*	0	NA
										GPIO82	1	IO
										MCPWM2_3A	3	O
										MCPWM3_3A	4	O
										MCPWM4_3A	5	O
										EPI0_S2	13	IO
										OUTPUTXBAR7	16	O
10								PC19 IOMUX_PC19 0x400C_C14C	SDL	*Disconnected*	0	NA
										GPIO83	1	IO
										MCPWM2_1A	3	O
										MCPWM3_1A	4	O
										UC0_RX_SCL_SCLK	5	IO
										UC5_RX_SCL	6	IO
										UC4_TX_SDA_PICO	7	O
										UC5_CTS	8	O
										SYSCTL_FCC_IN	9	I
										UC1_TX_SDA_PICO	11	O
										EPI0_S3	13	IO
										OUTPUTXBAR3	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
19	12	12	5	5	5	5	5	PC16_X1 IOMUX_PC16_X1 0x400C_C140	SDL	A0_10	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN0	A	A
										SYSCTL_HFCLKIN	AMUX1	A
										GPIO80	1	IO
										UC2_TX_SDA	2	O
										SYSCTL_X1	AMUX2	A
										MCPWM3_2B	4	O
										UC1_TX_SDA_PICO	5	O
										UC1_RTS_POCI	6	O
										MCPWM0_3B	7	O
										UC4_RTS_POCI	8	O
										MCPWM4_3B	9	O
										OUTPUTXBAR2	16	O
20	13	13	6	6	6	6	6	PC17_X2 IOMUX_PC17_X2 0x400C_C144	SDL	A1_10	AMUX0	A
										Disconnected	0	NA
										ANALOG_AIN1	A	A
										GPIO81	1	IO
										CMP2_HN0	AMUX1	A
										UC2_RX_SCL	2	IO
										SYSCTL_X2	AMUX2	A
										UC1_RX_SCL_SCLK	6	IO
										OUTPUTXBAR3	16	O
11								PC20 IOMUX_PC20 0x400C_C150	SDL	*Disconnected*	0	NA
										GPIO84	1	IO
										MCPWM3_1B	3	O
										MCPWM2_1B	4	O
										UC0_TX_SDA_PICO	5	O
										UC5_TX_SDA	6	O
										UC4_RX_SCL_SCLK	7	IO
										UC5_RTS	8	O
										UC1_RX_SCL_SCLK	11	IO
										EPI0_S4	13	IO
										OUTPUTXBAR4	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
14								PC21 IOMUX_PC21 0x400C_C154	SDL	*Disconnected*	0	NA
										GPIO85	1	IO
										MCPWM2_2B	3	O
										MCPWM3_2B	4	O
										MCPWM4_2B	6	O
										EPI0_S5	13	IO
										OUTPUTXBAR5	16	O
97		73						PC22 IOMUX_PC22 0x400C_C158	SDL	*Disconnected*	0	NA
										GPIO86	1	IO
										MCPWM3_3B	3	O
										MCPWM2_3B	4	O
										UC1_RX_SCL_SCLK	5	IO
										UC4_RX_SCL_SCLK	6	IO
										MCPWM3_1A	7	O
										UC0_RTS_POCI	8	O
										MCPWM4_2A	9	O
										UC3_RTS_POCI	10	O
										MCPWM4_3B	11	O
										OUTPUTXBAR2	16	O
15								PC23 IOMUX_PC23 0x400C_C15C	SDL	*Disconnected*	0	NA
										GPIO87	1	IO
										UC5_RX_SCL	2	IO
										MCPWM2_2A	3	O
										MCPWM3_2A	4	O
										UC4_RTS_POCI	5	O
										MCPWM4_2A	6	O
										MCPWM3_1B	7	O
										UC1_RTS_POCI	10	O
										UC2_RX_SCL	11	IO
										EPI0_S1	13	IO
										OUTPUTXBAR6	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
16								PC24 IOMUX_PC24 0x400C_C160	SDL	*Disconnected*	0	NA
										GPIO88	1	IO
										UC5_TX_SDA	2	O
										MCPWM3_1B	4	O
										UC4_CTS_CS0	5	IO
										MCPWM3_2A	7	O
										UC1_CTS_CS0	10	IO
										UC2_TX_SDA	11	O
										EPI0_S24	13	IO
										OUTPUTXBAR7	16	O
17	10							PC25 IOMUX_PC25 0x400C_C164	SDL	*Disconnected*	0	NA
										GPIO89	1	IO
										UC5_CTS	2	O
										UC2_TX_SDA	3	O
										MCPWM3_1A	4	O
										UC4_TX_SDA_PICO	5	O
										UC1_RX_SCL_SCLK	6	IO
										MCPWM3_2B	7	O
										UC5_RX_SCL	8	IO
										MCPWM4_2A	9	O
										UC2_CTS	11	O
										EPI0_S25	13	IO
										OUTPUTXBAR8	16	O
18	11							PC26 IOMUX_PC26 0x400C_C168	SDL	*Disconnected*	0	NA
										GPIO90	1	IO
										UC5_RTS	2	O
										UC2_RX_SCL	3	IO
										MCPWM3_2A	4	O
										UC4_RX_SCL_SCLK	5	IO
										UC1_RX_SCL_SCLK	6	IO
										SYSCTL_XCLKOUT	7	O
										UC5_TX_SDA	8	O
										UC2_RTS	11	O
										EPI0_S0	13	IO
										OUTPUTXBAR1	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
48								PC27 IOMUX_PC27 0x400C_C16C	SDL	*Disconnected*	0	NA
										GPIO91	1	IO
										EPI0_S33	13	IO
										OUTPUTXBAR4	16	O
49								PC28 IOMUX_PC28 0x400C_C170	SDL	*Disconnected*	0	NA
										GPIO92	1	IO
										MCPWM2_1A	3	O
										MCPWM3_1A	4	O
										EPI0_S6	13	IO
										OUTPUTXBAR5	16	O
50								PC29 IOMUX_PC29 0x400C_C174	SDL	*Disconnected*	0	NA
										GPIO93	1	IO
										MCPWM2_2A	3	O
										MCPWM3_2A	4	O
										MCPWM4_2A	5	O
										UC0_CTS_CS0	7	IO
										EPI0_S7	13	IO
										OUTPUTXBAR6	16	O
51								PC30 IOMUX_PC30 0x400C_C178	SDL	*Disconnected*	0	NA
										GPIO94	1	IO
										MCPWM2_3A	3	O
										MCPWM3_3A	4	O
										UC2_RX_SCL	5	IO
										MCPWM4_3A	6	O
										UC0_RX_SCL_SCLK	7	IO
										UC5_RX_SCL	8	IO
										EPI0_S8	13	IO
										OUTPUTXBAR7	16	O
52								PC31 IOMUX_PC31 0x400C_C17C	SDL	*Disconnected*	0	NA
										GPIO95	1	IO
										MCPWM2_1A	3	O
										MCPWM3_1A	4	O
										UC2_TX_SDA	5	O
										UC0_TX_SDA_PICO	7	O
										UC5_TX_SDA	8	O
										EPI0_S9	13	IO
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
82								PD0 IOMUX_PD0 0x400C_C180	SDL	*Disconnected*	0	NA
										GPIO96	1	IO
										MCPWM2_1B	3	O
										MCPWM3_1B	4	O
										UC2_RTS	5	O
										UC5_RTS	8	O
										MCPWM4_2A	14	O
										MCPWM3_1A	15	O
										OUTPUTXBAR5	16	O
83								PD1 IOMUX_PD1 0x400C_C184	SDL	*Disconnected*	0	NA
										GPIO97	1	IO
										MCPWM2_2B	3	O
										MCPWM3_2B	4	O
										UC2_CTS	5	O
										UC5_CTS	8	O
										MCPWM4_2B	14	O
										MCPWM3_1B	15	O
										OUTPUTXBAR6	16	O
84								PD2 IOMUX_PD2 0x400C_C188	SDL	*Disconnected*	0	NA
										GPIO98	1	IO
										MCPWM2_3B	3	O
										MCPWM3_3B	4	O
										MCPWM4_3B	5	O
										UC0_RX_SCL_SCLK	6	IO
										UC3_RX_SCL_SCLK	11	IO
										MCPWM3_2A	15	O
										OUTPUTXBAR7	16	O
85								PD3 IOMUX_PD3 0x400C_C18C	SDL	*Disconnected*	0	NA
										GPIO99	1	IO
										UC2_RX_SCL	5	IO
										UC0_CTS_CS0	6	IO
										MCPWM2_1B	7	O
										MCPWM3_1B	8	O
										UC3_CTS_CS0	10	IO
										UC5_RX_SCL	11	IO
										MCPWM3_2B	15	O
										OUTPUTXBAR8	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
86								PD4 IOMUX_PD4 0x400C_C190	SDL	*Disconnected*	0	NA
										GPIO100	1	IO
										UC2_TX_SDA	5	O
										UC0_TX_SDA_PICO	6	O
										UC3_TX_SDA_PICO	10	O
										UC5_TX_SDA	11	O
										MCPWM4_1A	13	O
										MCPWM4_3A	14	O
										MCPWM3_3A	15	O
										OUTPUTXBAR1	16	O
103								PD5 IOMUX_PD5 0x400C_C194	SDL	*Disconnected*	0	NA
										GPIO101	1	IO
										UC0_RTS_POCI	6	O
										UC1_CTS_CS0	8	IO
										UC0_CTS_CS0	9	IO
										OUTPUTXBAR5	16	O
104								PD6 IOMUX_PD6 0x400C_C198	SDL	*Disconnected*	0	NA
										GPIO102	1	IO
										UC1_RTS_POCI	8	O
										UC0_RTS_POCI	9	O
										OUTPUTXBAR6	16	O
105								PD7 IOMUX_PD7 0x400C_C19C	SDL	*Disconnected*	0	NA
										GPIO103	1	IO
										UC0_RX_SCL_SCLK	5	IO
										UC1_TX_SDA_PICO	8	O
										UC0_TX_SDA_PICO	9	O
										UC3_RX_SCL_SCLK	11	IO
										EPI0_S35	13	IO
										OUTPUTXBAR7	16	O

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Table 5-2. Pin Attributes (LQFP128, LQFP100_G, LQFP100_H, LQFP80, LQFP64_G, LQFP64_H, LQFP48, QFN48 Packages) (continued)

LQFP128	LQFP100_G	LQFP100_H	LQFP80	LQFP64_G	LQFP64_H	LQFP48	QFN48	BALL NAME/ IOMUX REGISTER/ IOMUX ADDRESS	IO TYPE	SIGNAL NAME	MODE	TYPE
106								PD8 IOMUX_PD8 0x400C_C1A0	SDL	*Disconnected*	0	NA
										GPIO104	1	IO
										UC0_TX_SDA_PICO	5	O
										UC1_RX_SCL_SCLK	8	IO
										UC0_RX_SCL_SCLK	9	IO
										UC3_TX_SDA_PICO	11	O
										EPI0_S34	13	IO
										MCPWM4_2A	14	O
										MCPWM3_1A	15	O
										OUTPUTXBAR8	16	O
107								PD9 IOMUX_PD9 0x400C_C1A4	SDL	*Disconnected*	0	NA
										GPIO105	1	IO
										UC2_RX_SCL	7	IO
										UC0_TX_SDA_PICO	8	O
										UC5_RX_SCL	9	IO
										UC3_TX_SDA_PICO	10	O
										EPI0_S27	13	IO
										MCPWM4_2B	14	O
										MCPWM3_1B	15	O
										OUTPUTXBAR1	16	O
		94			60			PD11 IOMUX_PD11 0x400C_C1AC	SDL	*Disconnected*	0	NA
										GPIO107	1	IO
										OUTPUTXBAR8	16	O
111, 128, 13, 47, 6, 64, 79, 95	100, 49, 6, 64, 75	100, 11, 50, 6, 75	1, 41, 51, 62, 80	1, 32, 48, 64	1, 32, 48, 64	1, 24, 36, 48	1, 23, 35, 48	VDD		VDD	0	PWR
31, 45	24, 37	28	16, 29	16, 29	19	21	21	VDDA		VDDA	0	APWR
43, 44	36	21, 22	28	28	13	20	20	VREFHI		VREFHI	0	AREF
42	35	20	27	27	12	19	PAD	VREFLO		VREFLO	0	AREF
110, 12, 127, 46, 63, 78, 94	48, 63, 74, 99	10, 19, 49, 74, 99	40, 50, 61, 79	31, 47, 63	31, 47, 63	23, 35, 47	PAD	VSS		VSS	0	GND
30	23	27	15	15	18	19	PAD	VSSA None None		VSSA	0	AGND

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5.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the *AM13E230x Microcontrollers Technical Reference Manual*..

2. **SIGNAL TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   -
   -
   -
   - A = Analog
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

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Table 5-3. ADC0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
A0_1	ADC0 Input 1	A	27	20	23	12	12	14	8	8
A0_2	ADC0 Input 2	A	28	21	24	13	13	15	9	9
A0_3	ADC0 Input 3	A	29	22	25	14	14	16	10	10
A0_4	ADC0 Input 4	A	32	25	26	17	17	17	11	11
A0_5	ADC0 Input 5	A	68	53	53	45	36	35	28	27
A0_6	ADC0 Input 6	A	22	15	15	8	8	8		
A0_7	ADC0 Input 7	A	23	16	16	9	9	9		
A0_8	ADC0 Input 8	A	24	17	17	10	10	10		
A0_9	ADC0 Input 9	A	25	18	18	11	11	11		
A0_10	ADC0 Input 10	A	19	12	12	5	5	5	5	5
A0_11	ADC0 Input 11	A	66	51	51	43	34	33	26	25
A0_12	ADC0 Input 12	A	40	33	36	25	25	27	17	18
A0_14	ADC0 Input 14	A	65	50		42	33		25	24
A0_15	ADC0 Input 15	A	39	32	35	24	24	26	16	17
A0_16	ADC0 Input 16	A	56	41	41	33				
A0_17	ADC0 Input 17	A	35	28	31	20	20	22	14	14
A0_18	ADC0 Input 18	A	60	45	45	37				
A0_19	ADC0 Input 19	A	61	46	46	38				
A0_21	ADC0 Input 21	A	70	55	55	47				
A0_22	ADC0 Input 22	A	71	56	56	48				
A0_23	ADC0 Input 23	A	54	39	39	31				
A0_24	ADC0 Input 24	A	57	42	42	34				
A0_25	ADC0 Input 25	A	58	43	43	35				
A0_26	ADC0 Input 26	A	72	57	57	49				
A0_27	ADC0 Input 27	A	73	58	58					
A0_28	ADC0 Input 28	A	74	59	59					
A0_29	ADC0 Input 29	A	75	60	60					
A0_30	ADC0 Input 30	A	76	61	61					

Table 5-4. ADC1 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
A1_1	ADC1 Input 1	A	27	20	23	12	12	14	8	8
A1_2	ADC1 Input 2	A	28	21	24	13	13	15	9	9
A1_3	ADC1 Input 3	A	35	28	31	20	20	22	14	14

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Table 5-4. ADC1 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
A1_4	ADC1 Input 4	A	36	29	32	21	21	23	15	15
A1_5	ADC1 Input 5	A	37	30	33	22	22	24		16
A1_6	ADC1 Input 6	A	22	15	15	8	8	8		
A1_7	ADC1 Input 7	A	23	16	16	9	9	9		
A1_8	ADC1 Input 8	A	24	17	17	10	10	10		
A1_9	ADC1 Input 9	A	25	18	18	11	11	11		
A1_10	ADC1 Input 10	A	20	13	13	6	6	6	6	6
A1_11	ADC1 Input 11	A	38	31	34	23	23	25		
A1_12	ADC1 Input 12	A	41	34	37	26	26	28	18	19
A1_13	ADC1 Input 13	A	34	27	30	19	19	21	13	13
A1_14	ADC1 Input 14	A	65	50		42	33		25	24
A1_15	ADC1 Input 15	A	69	54	54	46	37	36	29	28
A1_16	ADC1 Input 16	A	56	41	41	33				
A1_17	ADC1 Input 17	A	33	26	29	18	18	20	12	12
A1_18	ADC1 Input 18	A	89	69	67	56	42	41	30	30
A1_19	ADC1 Input 19	A	90	70	68	57	43	42	31	31
A1_21	ADC1 Input 21	A	70	55	55	47				
A1_22	ADC1 Input 22	A	71	56	56	48				
A1_23	ADC1 Input 23	A	54	39	39	31				
A1_24	ADC1 Input 24	A	57	42	42	34				
A1_25	ADC1 Input 25	A	58	43	43	35				
A1_26	ADC1 Input 26	A	72	57	57	49				
A1_27	ADC1 Input 27	A	73	58	58					
A1_28	ADC1 Input 28	A	74	59	59					
A1_29	ADC1 Input 29	A	75	60	60					
A1_30	ADC1 Input 30	A	76	61	61					

Table 5-5. ADC2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
A2_1	ADC2 Input 1	A	40	33	36	25	25	27	17	18
A2_2	ADC2 Input 2	A	55	40	40	32				
A2_3	ADC2 Input 3	A	59	44	44	36				
A2_4	ADC2 Input 4	A	53	38	38	30				
A2_5	ADC2 Input 5	A	67	52	52	44	35	34	27	26

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Table 5-5. ADC2 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
A2_6	ADC2 Input 6	A	54	39	39	31				
A2_7	ADC2 Input 7	A	72	57	57	49				
A2_8	ADC2 Input 8	A	73	58	58					
A2_9	ADC2 Input 9	A	74	59	59					
A2_10	ADC2 Input 10	A	75	60	60					
A2_11	ADC2 Input 11	A	76	61	61					
A2_12	ADC2 Input 12	A	39	32	35	24	24	26	16	17
A2_14	ADC2 Input 14	A	56	41	41	33				
A2_15	ADC2 Input 15	A	57	42	42	34				
A2_16	ADC2 Input 16	A	58	43	43	35				
A2_17	ADC2 Input 17	A	62	47	47	39	30	29	22	22
A2_18	ADC2 Input 18	A	33	26	29	18	18	20	12	12
A2_19	ADC2 Input 19	A	34	27	30	19	19	21	13	13
A2_21	ADC2 Input 21	A	32	25	26	17	17	17	11	11
A2_22	ADC2 Input 22	A	36	29	32	21	21	23	15	15
A2_23	ADC2 Input 23	A	37	30	33	22	22	24		16
A2_24	ADC2 Input 24	A	38	31	34	23	23	25		
A2_25	ADC2 Input 25	A	29	22	25	14	14	16	10	10
A2_26	ADC2 Input 26	A	35	28	31	20	20	22	14	14
A2_27	ADC2 Input 27	A	68	53	53	45	36	35	28	27
A2_28	ADC2 Input 28	A	69	54	54	46	37	36	29	28
A2_29	ADC2 Input 29	A	77	62	62					
A2_30	ADC2 Input 30	A	66	51	51	43	34	33	26	25

Table 5-6. ADCCAL Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ADCCAL_ADCINCAL0	ADC Calibration Input 0	A	35	28	31	20	20	22	14	14

Table 5-7. ANALOG Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ANALOG_AIN0	A0_10 HFCLKIN X1	A	19	12	12	5	5	5	5	5

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Table 5-7. ANALOG Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ANALOG_AIN1	A1_10 CMP2_HN0 X2	A	20	13	13	6	6	6	6	6
ANALOG_AIN2	A0_6 A1_6 CMP2_HN1	A	22	15	15	8	8	8		
ANALOG_AIN3	A0_7 A1_7 CMP2_HP1_LP1	A	23	16	16	9	9	9		
ANALOG_AIN4	A0_8 A1_8	A	24	17	17	10	10	10		
ANALOG_AIN5	A0_9 A1_9 PGA2_P1 PGA0_P0 PGA1_P0	A	25	18	18	11	11	11		
ANALOG_AIN6	A0_1 A1_1 CMP0_HN0 CMP2_HP0_LP0	A	27	20	23	12	12	14	8	8
ANALOG_AIN7	A0_2 A1_2 CMP0_HP1_LP1 PGA0_P1 PGA1_M0 PGA2_P2	A	28	21	24	13	13	15	9	9
ANALOG_AIN8	A0_3 A2_25 CMP1_HN0 PGA0_OUT	A	29	22	25	14	14	16	10	10
ANALOG_AIN9	A0_4 A2_21 CMP1_HP0_LP0 PGA0_M0 PGA0_P2 PGA2_M0	A	32	25	26	17	17	17	11	11
ANALOG_AIN10	A1_17 A2_18 CMP2_DACL CMP0_HN1 TESTANA0	A	33	26	29	18	18	20	12	12
ANALOG_AIN11	A1_13 A2_19 CMP1_HN1 PGA1_M1 TESTANA1	A	34	27	30	19	19	21	13	13

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Table 5-7. ANALOG Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ANALOG_AIN12	A0_17 A1_3 A2_26 CMP3_DACL PGA1_OUT ADCINCAL0	A	35	28	31	20	20	22	14	14
ANALOG_AIN13	A1_4 A2_22 CMP1_HP1_LP1 PGA0_P3 PGA1_P1	A	36	29	32	21	21	23	15	15
ANALOG_AIN14	A1_5 A2_23	A	37	30	33	22	22	24		16
ANALOG_AIN15	A1_11 A2_24 PGA0_M1 PGA1_M2	A	38	31	34	23	23	25		
ANALOG_AIN16	A0_15 A2_12 CMP3_HP1_LP1 PGA1_P2 PGA2_P3	A	39	32	35	24	24	26	16	17
ANALOG_AIN17	A0_12 A2_1 CMP0_HP0_LP0 PGA1_M3 PGA2_OUT	A	40	33	36	25	25	27	17	18
ANALOG_AIN18	A1_12 CMP3_HN0_LN0 PGA2_M1	A	41	34	37	26	26	28	18	19
ANALOG_AIN19	A2_4 CMP3_HP0_LP0	A	53	38	38	30				
ANALOG_AIN20	A0_23 A1_23 A2_6 CMP3_HN1_LN1	A	54	39	39	31				
ANALOG_AIN21	A2_2 CMP3_HP2_LP2	A	55	40	40	32				
ANALOG_AIN22	A0_16 A1_16 A2_14	A	56	41	41	33				
ANALOG_AIN23	A0_24 A1_24 A2_15	A	57	42	42	34				

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Table 5-7. ANALOG Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ANALOG_AIN24	A0_25 A1_25 A2_16	A	58	43	43	35				
ANALOG_AIN25	A2_3	A	59	44	44	36				
ANALOG_AIN26	A0_18	A	60	45	45	37				
ANALOG_AIN27	A0_19 CMP3_HP3_LP3	A	61	46	46	38				
ANALOG_AIN28	A2_17 CMP0_LN1 PGA2_M2 PGA0_M2	A	62	47	47	39	30	29	22	22
ANALOG_AIN29	A0_14 A1_14 CMP1_HP2_LP2 PGA0_P4 PGA2_P0	A	65	50		42	33		25	24
ANALOG_AIN30	A0_11 A2_30 CMP2_LN1 PGA1_P3 PGA0_P7	A	66	51	51	43	34	33	26	25
ANALOG_AIN31	A2_5 CMP0_HP2_LP2 PGA0_P5 PGA1_P4 PGA2_P4	A	67	52	52	44	35	34	27	26
ANALOG_AIN32	A0_5 A2_27 CMP2_HP3_LP3 PGA1_P5 PGA2_P5	A	68	53	53	45	36	35	28	27
ANALOG_AIN33	A1_15 A2_28 CMP1_LN1 PGA2_M3	A	69	54	54	46	37	36	29	28
ANALOG_AIN34	A0_21 A1_21 PGA0_M3	A	70	55	55	47				
ANALOG_AIN35	A0_22 A1_22 PGA1_P6 PGA2_P7	A	71	56	56	48				
ANALOG_AIN36	A0_26 A1_26 A2_7 CMP1_LN0	A	72	57	57	49				

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Table 5-7. ANALOG Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
ANALOG_AIN37	A0_27 A1_27 A2_8 CMP1_HP3_LP3 PGA0_P6 PGA1_P8 PGA2_P8	A	73	58	58					
ANALOG_AIN38	A0_28 A1_28 A2_9 CMP0_HP3_LP3 PGA2_P6 PGA0_P8	A	74	59	59					
ANALOG_AIN39	A0_29 A1_29 A2_10 CMP0_LN0	A	75	60	60					
ANALOG_AIN40	A0_30 A1_30 A2_11 CMP2_HP2_LP2 PGA1_P7	A	76	61	61					
ANALOG_AIN41	A2_29 CMP2_LN0	A	77	62	62					
ANALOG_AIN42	A1_18	A	89	69	67	56	42	41	30	30
ANALOG_AIN43	A1_19	A	90	70	68	57	43	42	31	31

Table 5-8. CMP0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
CMP0_HN0	CMPSS0 High Comparator Negative Input 0	A	27	20	23	12	12	14	8	8
CMP0_HN1	CMPSS0 High Comparator Negative Input 1	A	33	26	29	18	18	20	12	12
CMP0_HP0_LP0	CMPSS0 High/Low Comparator Positive Input 0	A	40	33	36	25	25	27	17	18
CMP0_HP1_LP1	CMPSS0 High/Low Comparator Positive Input 1	A	28	21	24	13	13	15	9	9
CMP0_HP2_LP2	CMPSS0 High/Low Comparator Positive Input 2	A	67	52	52	44	35	34	27	26
CMP0_HP3_LP3	CMPSS0 High/Low Comparator Positive Input 3	A	74	59	59					
CMP0_LN0	CMPSS0 Low Comparator Negative Input 0	A	75	60	60					

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Table 5-8. CMP0 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
CMP0_LN1	CMPSS0 Low Comparator Negative Input 1	A	62	47	47	39	30	29	22	22

Table 5-9. CMP1 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
CMP1_HN0	CMPSS1 High Comparator Negative Input 0	A	29	22	25	14	14	16	10	10
CMP1_HN1	CMPSS1 High Comparator Negative Input 1	A	34	27	30	19	19	21	13	13
CMP1_HP0_LP0	CMPSS1 High/Low Comparator Positive Input 0	A	32	25	26	17	17	17	11	11
CMP1_HP1_LP1	CMPSS1 High/Low Comparator Positive Input 1	A	36	29	32	21	21	23	15	15
CMP1_HP2_LP2	CMPSS1 High/Low Comparator Positive Input 2	A	65	50		42	33		25	24
CMP1_HP3_LP3	CMPSS1 High/Low Comparator Positive Input 3	A	73	58	58					
CMP1_LN0	CMPSS1 Low Comparator Negative Input 0	A	72	57	57	49				
CMP1_LN1	CMPSS1 Low Comparator Negative Input 1	A	69	54	54	46	37	36	29	28

Table 5-10. CMP2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
CMP2_DACL	CMPSS2 Buffered DACL Out	A	33	26	29	18	18	20	12	12
CMP2_HN0	CMPSS2 High Comparator Negative Input 0	A	20	13	13	6	6	6	6	6
CMP2_HN1	CMPSS2 High Comparator Negative Input 1	A	22	15	15	8	8	8		
CMP2_HP0_LP0	CMPSS2 High/Low Comparator Positive Input 0	A	27	20	23	12	12	14	8	8
CMP2_HP1_LP1	CMPSS2 High/Low Comparator Positive Input 1	A	23	16	16	9	9	9		
CMP2_HP2_LP2	CMPSS2 High/Low Comparator Positive Input 2	A	76	61	61					
CMP2_HP3_LP3	CMPSS2 High/Low Comparator Positive Input 3	A	68	53	53	45	36	35	28	27

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Table 5-10. CMP2 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
CMP2_LN0	CMPSS2 Low Comparator Negative Input 0	A	77	62	62					
CMP2_LN1	CMPSS2 Low Comparator Negative Input 1	A	66	51	51	43	34	33	26	25

Table 5-11. CMP3 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP48 PIN
CMP3_DACL	CMPSS3 Buffered DACL Out	A	14
CMP3_HN0_LN0	CMPSS3 High/Low Comparator Negative Input 0	A	18
CMP3_HN1_LN1	CMPSS3 High/Low Comparator Negative Input 1	A	
CMP3_HP0_LP0	CMPSS3 High/Low Comparator Positive Input 0	A	
CMP3_HP1_LP1	CMPSS3 High/Low Comparator Positive Input 1	A	16
CMP3_HP2_LP2	CMPSS3 High/Low Comparator Positive Input 2	A	
CMP3_HP3_LP3	CMPSS3 High/Low Comparator Positive Input 3	A	

Table 5-12. DEBUG Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
DEBUG_JTCK_SWCLK	JTAG Test Clock/Serial Wire Debug Clock	IO	98	77	76	64	50	49	38	37
DEBUG_JTDI	JTAG Test Data In	I	99	78	77	65	51	50	39	38
DEBUG_JTDO_SWO	JTAG Test Data Out/Serial Wire Debug Out	O	118	90	89	72	56	55	40	41
DEBUG_TMS_SWDIO	JTAG Test Mode Select/Serial Wire Debug In-Out	IO	96	76	72	63	49	46	37	36

Table 5-13. EPI0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
EPI0_S0	External Peripheral Interface Signal 0	IO	18, 76	11, 61	61					
EPI0_S1	External Peripheral Interface Signal 1	IO	15, 77	62	62					
EPI0_S2	External Peripheral Interface Signal 2	IO	108, 26	19, 82	81	69				
EPI0_S3	External Peripheral Interface Signal 3	IO	10, 109	83	82	70				
EPI0_S4	External Peripheral Interface Signal 4	IO	11, 53	38	38	30				
EPI0_S5	External Peripheral Interface Signal 5	IO	14, 54	39	39	31				
EPI0_S6	External Peripheral Interface Signal 6	IO	49, 55	40	40	32				

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Table 5-13. EPI0 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
EPI0_S7	External Peripheral Interface Signal 7	IO	50, 56	41	41	33				
EPI0_S8	External Peripheral Interface Signal 8	IO	51, 57	42	42	34				
EPI0_S9	External Peripheral Interface Signal 9	IO	52, 58	43	43	35				
EPI0_S10	External Peripheral Interface Signal 10	IO	59	44	44	36				
EPI0_S11	External Peripheral Interface Signal 11	IO	60	45	45	37				
EPI0_S12	External Peripheral Interface Signal 12	IO	61	46	46	38				
EPI0_S13	External Peripheral Interface Signal 13	IO	70	55	55	47				
EPI0_S14	External Peripheral Interface Signal 14	IO	71	56	56	48				
EPI0_S15	External Peripheral Interface Signal 15	IO	72	57	57	49				
EPI0_S16	External Peripheral Interface Signal 16	IO	73	58	58					
EPI0_S17	External Peripheral Interface Signal 17	IO	74	59	59					
EPI0_S18	External Peripheral Interface Signal 18	IO	75	60	60					
EPI0_S19	External Peripheral Interface Signal 19	IO	2	2	2					
EPI0_S20	External Peripheral Interface Signal 20	IO	3	3	3					
EPI0_S21	External Peripheral Interface Signal 21	IO	4	4	4					
EPI0_S22	External Peripheral Interface Signal 22	IO	5	5	5					
EPI0_S23	External Peripheral Interface Signal 23	IO	1	1	1					
EPI0_S24	External Peripheral Interface Signal 24	IO	125, 16	97	97					
EPI0_S25	External Peripheral Interface Signal 25	IO	126, 17	10, 98	98					
EPI0_S26	External Peripheral Interface Signal 26 (Chip Select 0)	IO	116, 59	44, 88	44, 87	36				
EPI0_S27	External Peripheral Interface Signal 27 (Chip Select 1)	IO	102, 107	81	80	68	54	53		
EPI0_S28	External Peripheral Interface Signal 28 (Read/Output Enable)	IO	113	85	84					
EPI0_S29	External Peripheral Interface Signal 29 (Write Enable)	IO	114	86	85					
EPI0_S30	External Peripheral Interface Signal 30 (Address Latch Enable)	IO	121	93	92	75	59	58	43	44
EPI0_S31	External Peripheral Interface Signal 31 (Clock)	IO	112	84	83	71	55	54		
EPI0_S32	External Peripheral Interface Signal 32 (Input Ready/nWAIT)	IO	115	87	86					
EPI0_S33	External Peripheral Interface Signal 33 (Chip Select 3)	IO	48, 62	47	47	39	30	29	22	22
EPI0_S34	External Peripheral Interface Signal 34 (Chip Select 2)	IO	106, 66	51	51	43	34	33	26	25

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Table 5-13. EPI0 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
EPI0_S35	External Peripheral Interface Signal 35 (Configure Register Enable)	IO	105, 67	52	52	44	35	34	27	26

Table 5-14. GPIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
GPIO00	General Purpose Input/Output 0 (Wakeup0)	IO	27	20	23	12	12	14	8	8
GPIO01	General Purpose Input/Output 1	IO	28	21	24	13	13	15	9	9
GPIO02	General Purpose Input/Output 2 (Wakeup3)	IO	29	22	25	14	14	16	10	10
GPIO03	General Purpose Input/Output 3	IO	32	25	26	17	17	17	11	11
GPIO04	General Purpose Input/Output 4	IO	33	26	29	18	18	20	12	12
GPIO05	General Purpose Input/Output 5	IO	34	27	30	19	19	21	13	13
GPIO06	General Purpose Input/Output 6	IO	35	28	31	20	20	22	14	14
GPIO07	General Purpose Input/Output 7	IO	36	29	32	21	21	23	15	15
GPIO08	General Purpose Input/Output 8	IO	89	69	67	56	42	41	30	30
GPIO09	General Purpose Input/Output 9	IO	90	70	68	57	43	42	31	31
GPIO10	General Purpose Input/Output 10	IO	91	71	69	58	44	43	32	32
GPIO11	General Purpose Input/Output 11	IO	92	72	70	59	45	44	33	33
GPIO12	General Purpose Input/Output 12	IO	93	73	71	60	46	45	34	34
GPIO13	General Purpose Input/Output 13	IO	96	76	72	63	49	46	37	36
GPIO14	General Purpose Input/Output 14	IO	98	77	76	64	50	49	38	37
GPIO15	General Purpose Input/Output 15	IO	99	78	77	65	51	50	39	38
GPIO16	General Purpose Input/Output 16	IO	39	32	35	24	24	26	16	17
GPIO17	General Purpose Input/Output 17	IO	40	33	36	25	25	27	17	18
GPIO18	General Purpose Input/Output 18	IO	41	34	37	26	26	28	18	19
GPIO19	General Purpose Input/Output 19	IO	118	90	89	72	56	55	40	41
GPIO100	General Purpose Input/Output 100	IO	86							
GPIO101	General Purpose Input/Output 101	IO	103							
GPIO102	General Purpose Input/Output 102	IO	104							
GPIO103	General Purpose Input/Output 103	IO	105							
GPIO104	General Purpose Input/Output 104	IO	106							
GPIO105	General Purpose Input/Output 105	IO	107							
GPIO107	General Purpose Input/Output 107	IO			94			60		
GPIO20	General Purpose Input/Output 20	IO	119	91	90	73	57	56	41	42

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Table 5-14. GPIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
GPIO21	General Purpose Input/Output 21	IO	120	92	91	74	58	57	42	43
GPIO22	General Purpose Input/Output 22	IO	121	93	92	75	59	58	43	44
GPIO23	General Purpose Input/Output 23	IO	122	94	93	76	60	59	44	45
GPIO24	General Purpose Input/Output 24	IO	123	95	95	77	61	61	45	46
GPIO25	General Purpose Input/Output 25	IO	124	96	96	78	62	62	46	47
GPIO26	General Purpose Input/Output 26	IO	62	47	47	39	30	29	22	22
GPIO27	General Purpose Input/Output 27	IO	65	50		42	33		25	24
GPIO28	General Purpose Input/Output 28	IO	66	51	51	43	34	33	26	25
GPIO29	General Purpose Input/Output 29	IO	67	52	52	44	35	34	27	26
GPIO30	General Purpose Input/Output 30	IO	68	53	53	45	36	35	28	27
GPIO31	General Purpose Input/Output 31	IO	69	54	54	46	37	36	29	28
GPIO32	General Purpose Input/Output 32	IO	22	15	15	8	8	8		
GPIO33	General Purpose Input/Output 33 (Wakeup5)	IO	23	16	16	9	9	9		
GPIO34	General Purpose Input/Output 34	IO	24	17	17	10	10	10		
GPIO35	General Purpose Input/Output 35	IO	25	18	18	11	11	11		
GPIO36	General Purpose Input/Output 36	IO	37	30	33	22	22	24		16
GPIO37	General Purpose Input/Output 37 (Wakeup4)	IO	38	31	34	23	23	25		
GPIO38	General Purpose Input/Output 38	IO	80	65	63	52	38	37		29
GPIO39	General Purpose Input/Output 39	IO	81	66	64	53	39	38		
GPIO40	General Purpose Input/Output 40	IO	87	67	65	54	40	39		
GPIO41	General Purpose Input/Output 41	IO	88	68	66	55	41	40		
GPIO42	General Purpose Input/Output 42	IO	100	79	78	66	52	51		39
GPIO43	General Purpose Input/Output 43	IO	101	80	79	67	53	52		40
GPIO44	General Purpose Input/Output 44	IO	102	81	80	68	54	53		
GPIO45	General Purpose Input/Output 45 (Wakeup1)	IO	7	7	7	2	2	2	2	2
GPIO46	General Purpose Input/Output 46	IO	8	8	8	3	3	3	3	3
GPIO47	General Purpose Input/Output 47	IO	9	9	9	4	4	4	4	4
GPIO48	General Purpose Input/Output 48	IO	108	82	81	69				
GPIO49	General Purpose Input/Output 49	IO	109	83	82	70				
GPIO50	General Purpose Input/Output 50 (Wakeup6)	IO	112	84	83	71	55	54		
GPIO51	General Purpose Input/Output 51 (Wakeup7)	IO	113	85	84					

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Table 5-14. GPIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
GPIO52	General Purpose Input/Output 52	IO	114	86	85					
GPIO53	General Purpose Input/Output 53	IO	115	87	86					
GPIO54	General Purpose Input/Output 54	IO	116	88	87					
GPIO55	General Purpose Input/Output 55	IO	117	89	88					
GPIO56	General Purpose Input/Output 56	IO	70	55	55	47				
GPIO57	General Purpose Input/Output 57	IO	71	56	56	48				
GPIO58	General Purpose Input/Output 58	IO	72	57	57	49				
GPIO59	General Purpose Input/Output 59	IO	73	58	58					
GPIO60	General Purpose Input/Output 60	IO	74	59	59					
GPIO61	General Purpose Input/Output 61	IO	75	60	60					
GPIO62	General Purpose Input/Output 62	IO	76	61	61					
GPIO63	General Purpose Input/Output 63	IO	77	62	62					
GPIO64	General Purpose Input/Output 64	IO	125	97	97					
GPIO65	General Purpose Input/Output 65	IO	126	98	98					
GPIO66	General Purpose Input/Output 66	IO	1	1	1					
GPIO67	General Purpose Input/Output 67	IO	2	2	2					
GPIO68	General Purpose Input/Output 68	IO	3	3	3					
GPIO69	General Purpose Input/Output 69	IO	4	4	4					
GPIO70	General Purpose Input/Output 70 (Wakeup2)	IO	5	5	5					
GPIO71	General Purpose Input/Output 71	IO	53	38	38	30				
GPIO72	General Purpose Input/Output 72	IO	54	39	39	31				
GPIO73	General Purpose Input/Output 73	IO	55	40	40	32				
GPIO74	General Purpose Input/Output 74	IO	56	41	41	33				
GPIO75	General Purpose Input/Output 75	IO	57	42	42	34				
GPIO76	General Purpose Input/Output 76	IO	58	43	43	35				
GPIO77	General Purpose Input/Output 77	IO	59	44	44	36				
GPIO78	General Purpose Input/Output 78	IO	60	45	45	37				
GPIO79	General Purpose Input/Output 79	IO	61	46	46	38				
GPIO80	General Purpose Input/Output 80	IO	19	12	12	5	5	5	5	5
GPIO81	General Purpose Input/Output 81	IO	20	13	13	6	6	6	6	6
GPIO82	General Purpose Input/Output 82	IO	26	19						
GPIO83	General Purpose Input/Output 83	IO	10							
GPIO84	General Purpose Input/Output 84	IO	11							
GPIO85	General Purpose Input/Output 85	IO	14							

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Table 5-14. GPIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
GPIO86	General Purpose Input/Output 86	IO	97		73					
GPIO87	General Purpose Input/Output 87	IO	15							
GPIO88	General Purpose Input/Output 88	IO	16							
GPIO89	General Purpose Input/Output 89	IO	17	10						
GPIO90	General Purpose Input/Output 90	IO	18	11						
GPIO91	General Purpose Input/Output 91	IO	48							
GPIO92	General Purpose Input/Output 92	IO	49							
GPIO93	General Purpose Input/Output 93	IO	50							
GPIO94	General Purpose Input/Output 94	IO	51							
GPIO95	General Purpose Input/Output 95	IO	52							
GPIO96	General Purpose Input/Output 96	IO	82							
GPIO97	General Purpose Input/Output 97	IO	83							
GPIO98	General Purpose Input/Output 98	IO	84							
GPIO99	General Purpose Input/Output 99	IO	85							

Table 5-15. GROUND Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
VSS	Digital Ground	GND	110, 12, 127, 46, 63, 78, 94	48, 63, 74, 99	10, 19, 49, 74, 99	40, 50, 61, 79	31, 47, 63	31, 47, 63	23, 35, 47	PAD
VSSA	Analog Ground	AGND	30	23	27	15	15	18	19	PAD

Table 5-16. MCAN0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCAN0_RX	CAN Receive (RX) Signal	I	109, 118, 120, 123, 37, 66, 8, 92, 99	30, 51, 72, 78, 8, 83, 90, 92, 95	33, 51, 70, 77, 8, 82, 89, 91, 95	22, 3, 43, 59, 65, 70, 72, 74, 77	22, 3, 34, 45, 51, 56, 58, 61	24, 3, 33, 44, 50, 55, 57, 61	26, 3, 33, 39, 40, 42, 45	16, 25, 3, 33, 38, 41, 43, 46
MCAN0_TX	CAN Transmit (TX) Signal	O	108, 119, 121, 124, 38, 67, 89, 9, 93	31, 52, 69, 73, 82, 9, 91, 93, 96	34, 52, 67, 71, 81, 9, 90, 92, 96	23, 4, 44, 56, 60, 69, 73, 75, 78	23, 35, 4, 42, 46, 57, 59, 62	25, 34, 4, 41, 45, 56, 58, 62	27, 30, 34, 4, 41, 43, 46	26, 30, 34, 4, 42, 44, 47

Table 5-17. MCPWM0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM0_1A	MCPWM0 Output 1A	O	22, 25, 55, 60, 61, 89, 92	15, 18, 40, 45, 46, 69, 72	15, 18, 40, 45, 46, 67, 70	11, 32, 37, 38, 56, 59, 8	11, 42, 45, 8	11, 41, 44, 8	30, 33	30, 33

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Table 5-17. MCPWM0 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM0_1B	MCPWM0 Output 1B	O	36, 38, 54, 56, 60, 67, 7, 92, 93	29, 31, 39, 41, 45, 52, 7, 72, 73	32, 34, 39, 41, 45, 52, 7, 70, 71	2, 21, 23, 31, 33, 37, 44, 59, 60	2, 21, 23, 35, 45, 46	2, 23, 25, 34, 44, 45	15, 2, 27, 33, 34	15, 2, 26, 33, 34
MCPWM0_2A	MCPWM0 Output 2A	O	23, 57, 90	16, 42, 70	16, 42, 68	34, 57, 9	43, 9	42, 9	31	31
MCPWM0_2B	MCPWM0 Output 2B	O	39, 54, 56, 68, 93	32, 39, 41, 53, 73	35, 39, 41, 53, 71	24, 31, 33, 45, 60	24, 36, 46	26, 35, 45	16, 28, 34	17, 27, 34
MCPWM0_3A	MCPWM0 Output 3A	O	24, 59, 91	17, 44, 71	17, 44, 69	10, 36, 58	10, 44	10, 43	32	32
MCPWM0_3B	MCPWM0 Output 3B	O	124, 19, 40, 55, 58, 69	12, 33, 40, 43, 54, 96	12, 36, 40, 43, 54, 96	25, 32, 35, 46, 5, 78	25, 37, 5, 62	27, 36, 5, 62	17, 29, 46, 5	18, 28, 47, 5

Table 5-18. MCPWM1 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM1_1A	MCPWM1 Output 1A	O	109, 121, 80, 88, 99	65, 68, 78, 83, 93	63, 66, 77, 82, 92	52, 55, 65, 70, 75	38, 41, 51, 59	37, 40, 50, 58	39, 43	29, 38, 44
MCPWM1_1B	MCPWM1 Output 1B	O	100, 108, 118, 36, 7	29, 7, 79, 82, 90	32, 7, 78, 81, 89	2, 21, 66, 69, 72	2, 21, 52, 56	2, 23, 51, 55	15, 2, 40	15, 2, 39, 41
MCPWM1_2A	MCPWM1 Output 2A	O	123, 81, 98	66, 77, 95	64, 76, 95	53, 64, 77	39, 50, 61	38, 49, 61	38, 45	37, 46
MCPWM1_2B	MCPWM1 Output 2B	O	101, 119, 39	32, 80, 91	35, 79, 90	24, 67, 73	24, 53, 57	26, 52, 56	16, 41	17, 40, 42
MCPWM1_3A	MCPWM1 Output 3A	O	124, 87	67, 96	65, 96	54, 78	40, 62	39, 62	46	47
MCPWM1_3B	MCPWM1 Output 3B	O	102, 120, 40	33, 81, 92	36, 80, 91	25, 68, 74	25, 54, 58	27, 53, 57	17, 42	18, 43

Table 5-19. MCPWM2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM2_1A	MCPWM2 Output 1A	O	1, 10, 126, 41, 49, 52	1, 34, 98	1, 37, 98	26	26	28	18	19
MCPWM2_1B	MCPWM2 Output 1B	O	11, 125, 3, 34, 40, 82, 85	27, 3, 33, 97	3, 30, 36, 97	19, 25	19, 25	21, 27	13, 17	13, 18
MCPWM2_2A	MCPWM2 Output 2A	O	121, 15, 2, 24, 50, 74, 92	17, 2, 59, 72, 93	17, 2, 59, 70, 92	10, 59, 75	10, 45, 59	10, 44, 58	33, 43	33, 44
MCPWM2_2B	MCPWM2 Output 2B	O	122, 14, 4, 75, 83, 93	4, 60, 73, 94	4, 60, 71, 93	60, 76	46, 60	45, 59	34, 44	34, 45
MCPWM2_3A	MCPWM2 Output 3A	O	123, 26, 51, 76, 87, 96	19, 61, 67, 76, 95	61, 65, 72, 95	54, 63, 77	40, 49, 61	39, 46, 61	37, 45	36, 46
MCPWM2_3B	MCPWM2 Output 3B	O	124, 5, 77, 84, 97	5, 62, 96	5, 62, 73, 96	78	62	62	46	47

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Table 5-20. MCPWM3 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM3_1A	MCPWM3 Output 1A	O	1, 10, 106, 119, 123, 125, 126, 17, 27, 29, 35, 41, 49, 52, 68, 82, 87, 89, 93, 97, 99	1, 10, 20, 22, 28, 34, 53, 67, 69, 73, 78, 91, 95, 97, 98	1, 23, 25, 31, 37, 53, 65, 67, 71, 73, 77, 90, 95, 97, 98	12, 14, 20, 26, 45, 54, 56, 60, 65, 73, 77	12, 14, 20, 26, 36, 40, 42, 46, 51, 57, 61	14, 16, 22, 28, 35, 39, 41, 45, 50, 56, 61	10, 14, 18, 28, 30, 34, 39, 41, 45, 8	10, 14, 19, 27, 30, 34, 38, 42, 46, 8
MCPWM3_1B	MCPWM3 Output 1B	O	102, 107, 11, 121, 125, 15, 16, 28, 29, 3, 34, 40, 69, 7, 82, 83, 85, 88, 90, 96	21, 22, 27, 3, 33, 54, 68, 7, 70, 76, 81, 93, 97	24, 25, 3, 30, 36, 54, 66, 68, 7, 72, 80, 92, 97	13, 14, 19, 2, 25, 46, 55, 57, 63, 68, 75	13, 14, 19, 2, 25, 37, 41, 43, 49, 54, 59	15, 16, 2, 21, 27, 36, 40, 42, 46, 53, 58	10, 13, 17, 2, 29, 31, 37, 43, 9	10, 13, 18, 2, 28, 31, 36, 44, 9
MCPWM3_2A	MCPWM3 Output 2A	O	109, 121, 15, 16, 18, 2, 24, 28, 32, 50, 54, 69, 74, 84, 91	11, 17, 2, 21, 25, 39, 54, 59, 71, 83, 93	17, 2, 24, 26, 39, 54, 59, 69, 82, 92	10, 13, 17, 31, 46, 58, 70, 75	10, 13, 17, 37, 44, 59	10, 15, 17, 36, 43, 58	11, 29, 32, 43, 9	11, 28, 32, 44, 9
MCPWM3_2B	MCPWM3 Output 2B	O	100, 108, 122, 14, 17, 19, 32, 4, 55, 75, 83, 85, 92, 93	10, 12, 25, 4, 40, 60, 72, 73, 79, 82, 94	12, 26, 4, 40, 60, 70, 71, 78, 81, 93	17, 32, 5, 59, 60, 66, 69, 76	17, 45, 46, 5, 52, 60	17, 44, 45, 5, 51, 59	11, 33, 34, 44, 5	11, 33, 34, 39, 45, 5
MCPWM3_3A	MCPWM3 Output 3A	O	117, 120, 123, 124, 126, 23, 26, 29, 35, 36, 51, 57, 62, 66, 76, 80, 86, 87, 90, 96, 98	16, 19, 22, 28, 29, 42, 47, 51, 61, 65, 67, 70, 76, 77, 89, 92, 95, 96, 98	16, 25, 31, 32, 42, 47, 51, 61, 63, 65, 68, 72, 76, 88, 91, 95, 96, 98	14, 20, 21, 34, 39, 43, 52, 54, 57, 63, 64, 74, 77, 78, 9	14, 20, 21, 30, 34, 38, 40, 43, 49, 50, 58, 61, 62, 9	16, 22, 23, 29, 33, 37, 39, 42, 46, 49, 57, 61, 62, 9	10, 14, 15, 22, 26, 31, 37, 38, 42, 45, 46	10, 14, 15, 22, 25, 29, 31, 36, 37, 43, 46, 47
MCPWM3_3B	MCPWM3 Output 3A	O	116, 121, 122, 124, 32, 36, 39, 5, 56, 65, 67, 68, 77, 81, 84, 87, 88, 91, 93, 97	25, 29, 32, 41, 5, 50, 52, 53, 62, 66, 67, 68, 71, 73, 88, 93, 94, 96	26, 32, 35, 41, 5, 52, 53, 62, 64, 65, 66, 69, 71, 73, 87, 92, 93, 96	17, 21, 24, 33, 42, 44, 45, 53, 54, 55, 58, 60, 75, 76, 78	17, 21, 24, 33, 35, 36, 39, 40, 41, 44, 46, 59, 60, 62	17, 23, 26, 34, 35, 38, 39, 40, 43, 45, 58, 59, 62	11, 15, 16, 25, 27, 28, 32, 34, 43, 44, 46	11, 15, 17, 24, 26, 27, 32, 34, 44, 45, 47

Table 5-21. MCPWM4 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM4_1A	MCPWM4 Output 1A	O	113, 124, 126, 22, 25, 27, 3, 34, 36, 39, 55, 60, 61, 66, 68, 86, 89, 92	15, 18, 20, 27, 29, 3, 32, 40, 45, 46, 51, 53, 69, 72, 85, 96, 98	15, 18, 23, 3, 30, 32, 35, 40, 45, 46, 51, 53, 67, 70, 84, 96, 98	11, 12, 19, 21, 24, 32, 37, 38, 43, 45, 56, 59, 78, 8	11, 12, 19, 21, 24, 34, 36, 42, 45, 62, 8	11, 14, 21, 23, 26, 33, 35, 41, 44, 62, 8	13, 15, 16, 26, 28, 30, 33, 46, 8	13, 15, 17, 25, 27, 30, 33, 47, 8
MCPWM4_1B	MCPWM4 Output 1B	O	102, 114, 118, 120, 122, 28, 36, 38, 4, 40, 54, 60, 67, 69, 92, 93	21, 29, 31, 33, 39, 4, 45, 52, 54, 72, 73, 81, 86, 90, 92, 94	24, 32, 34, 36, 39, 4, 45, 52, 54, 70, 71, 80, 85, 89, 91, 93	13, 21, 23, 25, 31, 37, 44, 46, 59, 60, 68, 72, 74, 76	13, 21, 23, 25, 35, 37, 45, 46, 54, 56, 58, 60	15, 23, 25, 27, 34, 36, 44, 45, 53, 55, 57, 59	15, 17, 27, 29, 33, 34, 40, 42, 44, 9	15, 18, 26, 28, 33, 34, 41, 43, 45, 9

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Table 5-21. MCPWM4 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
MCPWM4_2A	MCPWM4 Output 2A	O	106, 117, 119, 121, 123, 125, 15, 17, 2, 23, 24, 27, 29, 35, 41, 50, 57, 62, 68, 74, 80, 82, 87, 88, 89, 90, 92, 93, 97, 99	10, 16, 17, 2, 20, 22, 28, 34, 42, 47, 53, 59, 65, 67, 68, 69, 70, 72, 73, 78, 89, 91, 93, 95, 97	16, 17, 2, 23, 25, 31, 37, 42, 47, 53, 59, 63, 65, 66, 67, 68, 70, 71, 73, 77, 88, 90, 92, 95, 97	10, 12, 14, 20, 26, 34, 39, 45, 52, 54, 55, 56, 57, 59, 60, 65, 73, 75, 77, 9	10, 12, 14, 20, 26, 30, 36, 38, 40, 41, 42, 43, 45, 46, 51, 57, 59, 61, 9	10, 14, 16, 22, 28, 29, 35, 37, 39, 40, 41, 42, 44, 45, 50, 56, 58, 61, 9	10, 14, 18, 22, 28, 30, 31, 33, 34, 39, 41, 43, 45, 8	10, 14, 19, 22, 27, 29, 30, 31, 33, 34, 38, 42, 44, 46, 8
MCPWM4_2B	MCPWM4 Output 2B	O	102, 107, 116, 118, 121, 122, 14, 28, 29, 32, 36, 39, 4, 56, 65, 68, 69, 7, 75, 83, 88, 90, 91, 93, 96	21, 22, 25, 29, 32, 4, 41, 50, 53, 54, 60, 68, 7, 70, 71, 73, 76, 81, 88, 90, 93, 94	24, 25, 26, 32, 35, 4, 41, 53, 54, 60, 66, 68, 69, 7, 71, 72, 80, 87, 89, 92, 93	13, 14, 17, 2, 21, 24, 33, 42, 45, 46, 55, 57, 58, 60, 63, 68, 72, 75, 76	13, 14, 17, 2, 21, 24, 33, 36, 37, 41, 43, 44, 46, 49, 54, 56, 59, 60	15, 16, 17, 2, 23, 26, 35, 36, 40, 42, 43, 45, 46, 53, 55, 58, 59	10, 11, 15, 16, 2, 25, 28, 29, 31, 32, 34, 37, 40, 43, 44, 9	10, 11, 15, 17, 2, 24, 27, 28, 31, 32, 34, 36, 41, 44, 45, 9
MCPWM4_3A	MCPWM4 Output 3A	O	1, 117, 119, 120, 123, 124, 24, 26, 29, 36, 51, 59, 62, 76, 81, 86, 87, 91, 96	1, 17, 19, 22, 29, 44, 47, 61, 66, 67, 71, 76, 89, 91, 92, 95, 96	1, 17, 25, 32, 44, 47, 61, 64, 65, 69, 72, 88, 90, 91, 95, 96	10, 14, 21, 36, 39, 53, 54, 58, 63, 73, 74, 77, 78	10, 14, 21, 30, 39, 40, 44, 49, 57, 58, 61, 62	10, 16, 23, 29, 38, 39, 43, 46, 56, 57, 61, 62	10, 15, 22, 32, 37, 41, 42, 45, 46	10, 15, 22, 32, 36, 42, 43, 46, 47
MCPWM4_3B	MCPWM4 Output 3B	O	116, 119, 120, 121, 122, 124, 19, 2, 33, 39, 40, 58, 67, 69, 77, 80, 84, 87, 97	12, 2, 26, 32, 33, 43, 52, 54, 62, 65, 67, 88, 91, 92, 93, 94, 96	12, 2, 29, 35, 36, 43, 52, 54, 62, 63, 65, 73, 87, 90, 91, 92, 93, 96	18, 24, 25, 35, 44, 46, 5, 52, 54, 73, 74, 75, 76, 78	18, 24, 25, 35, 37, 38, 40, 5, 57, 58, 59, 60, 62	20, 26, 27, 34, 36, 37, 39, 5, 56, 57, 58, 59, 62	12, 16, 17, 27, 29, 41, 42, 43, 44, 46, 5	12, 17, 18, 26, 28, 29, 42, 43, 44, 45, 47, 5

Table 5-22. NC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
NC	No Connect	NC			48			30		

Table 5-23. OUTPUTXBAR Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
OUTPUTXBAR1	Output X-BAR Output (Group 1)	O	1, 107, 117, 125, 18, 36, 39, 53, 61, 76, 8, 86, 99	1, 11, 29, 32, 38, 46, 61, 78, 8, 89, 97	1, 32, 35, 38, 46, 61, 77, 8, 88, 97	21, 24, 3, 30, 38, 65	21, 24, 3, 51	23, 26, 3, 50	15, 16, 3, 39	15, 17, 3, 38
OUTPUTXBAR2	Output X-BAR Output (Group 2)	O	100, 108, 118, 126, 19, 2, 37, 40, 54, 62, 69, 77, 87, 9, 97	12, 2, 30, 33, 39, 47, 54, 62, 67, 79, 82, 9, 90, 98	12, 2, 33, 36, 39, 47, 54, 62, 65, 73, 78, 81, 89, 9, 98	22, 25, 31, 39, 4, 46, 5, 54, 66, 69, 72	22, 25, 30, 37, 4, 40, 5, 52, 56	24, 27, 29, 36, 39, 4, 5, 51, 55	17, 22, 29, 4, 40, 5	16, 18, 22, 28, 39, 4, 41, 5

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Table 5-23. OUTPUTXBAR Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
OUTPUTXBAR3	Output X-BAR Output (Group 3)	O	10, 101, 109, 119, 20, 3, 38, 41, 55, 65, 70, 80, 88, 89	13, 3, 31, 34, 40, 50, 55, 65, 68, 69, 80, 83, 91	13, 3, 34, 37, 40, 55, 63, 66, 67, 79, 82, 90	23, 26, 32, 42, 47, 52, 55, 56, 6, 67, 70, 73	23, 26, 33, 38, 41, 42, 53, 57, 6	25, 28, 37, 40, 41, 52, 56, 6	18, 25, 30, 41, 6	19, 24, 29, 30, 40, 42, 6
OUTPUTXBAR4	Output X-BAR Output (Group 4)	O	102, 11, 112, 120, 28, 4, 48, 56, 66, 71, 81, 90	21, 4, 41, 51, 56, 66, 70, 81, 84, 92	24, 4, 41, 51, 56, 64, 68, 80, 83, 91	13, 33, 43, 48, 53, 57, 68, 71, 74	13, 34, 39, 43, 54, 55, 58	15, 33, 38, 42, 53, 54, 57	26, 31, 42, 9	25, 31, 43, 9
OUTPUTXBAR5	Output X-BAR Output (Group 5)	O	103, 113, 121, 14, 22, 29, 49, 5, 57, 67, 72, 82, 92	15, 22, 42, 5, 52, 57, 72, 85, 93	15, 25, 42, 5, 52, 57, 70, 84, 92	14, 34, 44, 49, 59, 75, 8	14, 35, 45, 59, 8	16, 34, 44, 58, 8	10, 27, 33, 43	10, 26, 33, 44
OUTPUTXBAR6	Output X-BAR Output (Group 6)	O	104, 114, 122, 15, 23, 32, 33, 50, 58, 68, 7, 73, 83, 93	16, 25, 26, 43, 53, 58, 7, 73, 86, 94	16, 26, 29, 43, 53, 58, 7, 71, 85, 93	17, 18, 2, 35, 45, 60, 76, 9	17, 18, 2, 36, 46, 60, 9	17, 2, 20, 35, 45, 59, 9	11, 12, 2, 28, 34, 44	11, 12, 2, 27, 34, 45
OUTPUTXBAR7	Output X-BAR Output (Group 7)	O	105, 115, 123, 124, 16, 24, 26, 34, 51, 59, 74, 84, 96	17, 19, 27, 44, 59, 76, 87, 95, 96	17, 30, 44, 59, 72, 86, 95, 96	10, 19, 36, 63, 77, 78	10, 19, 49, 61, 62	10, 21, 46, 61, 62	13, 37, 45, 46	13, 36, 46, 47
OUTPUTXBAR8	Output X-BAR Output (Group 8)	O	106, 116, 17, 25, 27, 35, 52, 60, 75, 85, 91, 98	10, 18, 20, 28, 45, 60, 71, 77, 88	18, 23, 31, 45, 60, 69, 76, 87, 94	11, 12, 20, 37, 58, 64	11, 12, 20, 44, 50	11, 14, 22, 43, 49, 60	14, 32, 38, 8	14, 32, 37, 8

Table 5-24. PGA0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
PGA0_OUT	PGA0 Output	A	29	22	25	14	14	16	10	10
PGA0_M0	PGA0 Negative (-) Input 0	A	32	25	26	17	17	17	11	11
PGA0_M1	PGA0 Negative (-) Input 1	A	38	31	34	23	23	25		
PGA0_M2	PGA0 Negative (-) Input 2	A	62	47	47	39	30	29	22	22
PGA0_M3	PGA0 Negative (-) Input 3	A	70	55	55	47				
PGA0_P0	PGA0 Positive (+) Input 0	A	25	18	18	11	11	11		
PGA0_P1	PGA0 Positive (+) Input 1	A	28	21	24	13	13	15	9	9
PGA0_P2	PGA0 Positive (+) Input 2	A	32	25	26	17	17	17	11	11
PGA0_P3	PGA0 Positive (+) Input 3	A	36	29	32	21	21	23	15	15
PGA0_P4	PGA0 Positive (+) Input 4	A	65	50		42	33		25	24
PGA0_P5	PGA0 Positive (+) Input 5	A	67	52	52	44	35	34	27	26
PGA0_P6	PGA0 Positive (+) Input 6	A	73	58	58					
PGA0_P7	PGA0 Positive (+) Input 7	A	66	51	51	43	34	33	26	25

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Table 5-24. PGA0 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
PGA0_P8	PGA0 Positive (+) Input 8	A	74	59	59					

Table 5-25. PGA1 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
PGA1_OUT	PGA1 Output	A	35	28	31	20	20	22	14	14
PGA1_M0	PGA1 Negative (-) Input 0	A	28	21	24	13	13	15	9	9
PGA1_M1	PGA1 Negative (-) Input 1	A	34	27	30	19	19	21	13	13
PGA1_M2	PGA1 Negative (-) Input 2	A	38	31	34	23	23	25		
PGA1_M3	PGA1 Negative (-) Input 3	A	40	33	36	25	25	27	17	18
PGA1_P0	PGA1 Positive (+) Input 0	A	25	18	18	11	11	11		
PGA1_P1	PGA1 Positive (+) Input 1	A	36	29	32	21	21	23	15	15
PGA1_P2	PGA1 Positive (+) Input 2	A	39	32	35	24	24	26	16	17
PGA1_P3	PGA1 Positive (+) Input 3	A	66	51	51	43	34	33	26	25
PGA1_P4	PGA1 Positive (+) Input 4	A	67	52	52	44	35	34	27	26
PGA1_P5	PGA1 Positive (+) Input 5	A	68	53	53	45	36	35	28	27
PGA1_P6	PGA1 Positive (+) Input 6	A	71	56	56	48				
PGA1_P7	PGA1 Positive (+) Input 7	A	76	61	61					
PGA1_P8	PGA1 Positive (+) Input 8	A	73	58	58					

Table 5-26. PGA2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
PGA2_OUT	PGA2 Output	A	40	33	36	25	25	27	17	18
PGA2_M0	PGA2 Negative (-) Input 0	A	32	25	26	17	17	17	11	11
PGA2_M1	PGA2 Negative (-) Input 1	A	41	34	37	26	26	28	18	19
PGA2_M2	PGA2 Negative (-) Input 2	A	62	47	47	39	30	29	22	22
PGA2_M3	PGA2 Negative (-) Input 3	A	69	54	54	46	37	36	29	28
PGA2_P0	PGA2 Positive (+) Input 0	A	65	50		42	33		25	24
PGA2_P1	PGA2 Positive (+) Input 1	A	25	18	18	11	11	11		
PGA2_P2	PGA2 Positive (+) Input 2	A	28	21	24	13	13	15	9	9
PGA2_P3	PGA2 Positive (+) Input 3	A	39	32	35	24	24	26	16	17
PGA2_P4	PGA2 Positive (+) Input 4	A	67	52	52	44	35	34	27	26
PGA2_P5	PGA2 Positive (+) Input 5	A	68	53	53	45	36	35	28	27
PGA2_P6	PGA2 Positive (+) Input 6	A	74	59	59					

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Table 5-26. PGA2 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
PGA2_P7	PGA2 Positive (+) Input 7	A	71	56	56	48				
PGA2_P8	PGA2 Positive (+) Input 8	A	73	58	58					

Table 5-27. POWER Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
VDD	3.3V Digital Power Pin	PWR	111, 128, 13, 47, 6, 64, 79, 95	100, 49, 6, 64, 75	100, 11, 50, 6, 75	1, 41, 51, 62, 80	1, 32, 48, 64	1, 32, 48, 64	1, 24, 36, 48	1, 23, 35, 48
VDDA	3.3V Analog Power Pin	APWR	31, 45	24, 37	28	16, 29	16, 29	19	21	21

Table 5-28. SYSCTL Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
NRST	Device Reset (NRST)	RST	21	14	14	7	7	7	7	7
SYSCTL_FCC_IN	Frequency Clock Counter (FCC) Input Signal	I	1, 10, 39, 67, 7, 96	1, 32, 52, 7, 76	1, 35, 52, 7, 72	2, 24, 44, 63	2, 24, 35, 49	2, 26, 34, 46	16, 2, 27, 37	17, 2, 26, 36
SYSCTL_HFCLKIN	External Clock Input	A	19, 32	12, 25	12, 26	17, 5	17, 5	17, 5	11, 5	11, 5
SYSCTL_X1	Crystal (XTAL) Input (X1) or Single-ended Clock Input	A	19	12	12	5	5	5	5	5
SYSCTL_X2	Crystal (XTAL) Output (X2)	A	20	13	13	6	6	6	6	6
SYSCTL_XCLKOUT	External Clock Output. This pin outputs an (optionally) divided-down version of a chosen clock signal from within the device.	O	18, 33, 65, 7, 8	11, 26, 50, 7, 8	29, 7, 8	18, 2, 3, 42	18, 2, 3, 33	2, 20, 3	12, 2, 25, 3	12, 2, 24, 3

Table 5-29. TIMER Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
TIMG12_0_CCP0	TIMG12_0 Capture/Compare0 Signal	IO	27, 32, 62, 66	20, 25, 47, 51	23, 26, 47, 51	12, 17, 39, 43	12, 17, 30, 34	14, 17, 29, 33	11, 22, 26, 8	11, 22, 25, 8
TIMG12_0_CCP1	TIMG12_0 Capture/Compare1 Signal	IO	28, 33, 65, 67	21, 26, 50, 52	24, 29, 52	13, 18, 42, 44	13, 18, 33, 35	15, 20, 34	12, 25, 27, 9	12, 24, 26, 9
TIMG4_0_CCP0	TIMG4_0 Capture/Compare0 Signal	IO	27, 32, 62, 66, 72, 74, 76	20, 25, 47, 51, 57, 59, 61	23, 26, 47, 51, 57, 59, 61	12, 17, 39, 43, 49	12, 17, 30, 34	14, 17, 29, 33	11, 22, 26, 8	11, 22, 25, 8
TIMG4_0_CCP1	TIMG4_0 Capture/Compare1 Signal	IO	28, 33, 65, 67, 73, 75, 77	21, 26, 50, 52, 58, 60, 62	24, 29, 52, 58, 60, 62	13, 18, 42, 44	13, 18, 33, 35	15, 20, 34	12, 25, 27, 9	12, 24, 26, 9

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Table 5-30. TRACE Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
TRACE_CLK	Trace Clock	IO	1, 101	1, 80	1, 79	67	53	52		40
TRACE_DATA0	Trace Data 0	O	126, 2	2, 98	2, 98					
TRACE_DATA1	Trace Data 1	O	3, 87	3, 67	3, 65	54	40	39		
TRACE_DATA2	Trace Data 2	O	112, 4	4, 84	4, 83	71	55	54		
TRACE_DATA3	Trace Data 3	O	102, 5	5, 81	5, 80	68	54	53		

Table 5-31. UC0 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC0_RTS_POCI	UNICOMM0 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	O	103, 104, 119, 2, 28, 3, 33, 35, 40, 53, 57, 66, 68, 74, 93, 97, 99	2, 21, 26, 28, 3, 33, 38, 42, 51, 53, 59, 73, 78, 91	2, 24, 29, 3, 31, 36, 38, 42, 51, 53, 59, 71, 73, 77, 90	13, 18, 20, 25, 30, 34, 43, 45, 60, 65, 73	13, 18, 20, 25, 34, 36, 46, 51, 57	15, 20, 22, 27, 33, 35, 45, 50, 56	12, 14, 17, 26, 28, 34, 39, 41, 9	12, 14, 18, 25, 27, 34, 38, 42, 9
UC0_RX_SCL_SCLK	UNICOMM0 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	IO	1, 10, 100, 101, 102, 105, 106, 112, 118, 120, 122, 123, 124, 126, 22, 32, 34, 38, 51, 58, 61, 62, 65, 84, 87, 89, 9, 91, 96, 99	1, 15, 25, 27, 31, 43, 46, 47, 50, 67, 69, 71, 76, 78, 79, 80, 81, 84, 9, 90, 92, 94, 95, 96, 98	1, 15, 26, 30, 34, 43, 46, 47, 65, 67, 69, 72, 77, 78, 79, 80, 83, 89, 9, 91, 93, 95, 96, 98	17, 19, 23, 35, 38, 39, 4, 42, 54, 56, 58, 63, 65, 66, 67, 68, 71, 72, 74, 76, 77, 78, 8	17, 19, 23, 30, 33, 4, 40, 42, 44, 49, 51, 52, 53, 54, 55, 56, 58, 60, 61, 62, 8	17, 21, 25, 29, 39, 4, 41, 43, 46, 50, 51, 52, 53, 54, 55, 57, 59, 61, 62, 8	11, 13, 22, 25, 30, 32, 37, 39, 4, 40, 42, 44, 45, 46	11, 13, 22, 24, 30, 32, 36, 38, 39, 4, 40, 41, 43, 45, 46, 47
UC0_TX_SDA_PICO	UNICOMM0 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	O	100, 101, 102, 105, 106, 107, 11, 112, 120, 121, 122, 123, 124, 125, 23, 29, 36, 37, 5, 52, 60, 61, 62, 65, 8, 86, 88, 90, 98	16, 22, 29, 30, 45, 46, 47, 5, 50, 68, 70, 77, 79, 8, 80, 81, 84, 92, 93, 94, 95, 96, 97	16, 25, 32, 33, 45, 46, 47, 5, 66, 68, 76, 78, 79, 8, 80, 83, 91, 92, 93, 95, 96, 97	14, 21, 22, 3, 37, 38, 39, 42, 55, 57, 64, 66, 67, 68, 71, 74, 75, 76, 77, 78, 9	14, 21, 22, 3, 30, 33, 41, 43, 50, 52, 53, 54, 55, 58, 59, 60, 61, 62, 9	16, 23, 24, 29, 3, 40, 42, 49, 51, 52, 53, 54, 57, 58, 59, 61, 62, 9	10, 15, 22, 25, 3, 31, 38, 42, 43, 44, 45, 46	10, 15, 16, 22, 24, 3, 31, 37, 39, 40, 43, 44, 45, 46, 47
UC0_CTS_CS0	UNICOMM0 CTS: UART Clear To Send CS0: SPI Chip Select 0	IO	101, 103, 119, 120, 27, 35, 4, 50, 59, 66, 67, 73, 85, 92, 96	20, 28, 4, 44, 51, 52, 58, 72, 76, 80, 91, 92	23, 31, 4, 44, 51, 52, 58, 70, 72, 79, 90, 91	12, 20, 36, 43, 44, 59, 63, 67, 73, 74	12, 20, 34, 35, 45, 49, 53, 57, 58	14, 22, 33, 34, 44, 46, 52, 56, 57	14, 26, 27, 33, 37, 41, 42, 8	14, 25, 26, 33, 36, 40, 42, 43, 8

Table 5-32. UC1 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC1_RTS_POCI	UNICOMM1 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	O	104, 114, 15, 19, 28, 66, 77	12, 21, 51, 62, 86	12, 24, 51, 62, 85	13, 43, 5	13, 34, 5	15, 33, 5	26, 5, 9	25, 5, 9

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Table 5-32. UC1 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC1_RX_SCL_SCLK	UNICOMM1 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	IO	106, 11, 116, 119, 17, 18, 20, 28, 32, 37, 90, 97, 99	10, 11, 13, 21, 25, 30, 70, 78, 88, 91	13, 24, 26, 33, 68, 73, 77, 87, 90	13, 17, 22, 57, 6, 65, 73	13, 17, 22, 43, 51, 57, 6	15, 17, 24, 42, 50, 56, 6	11, 31, 39, 41, 6, 9	11, 16, 31, 38, 42, 6, 9
UC1_TX_SDA_PICO	UNICOMM1 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	O	10, 105, 115, 118, 19, 27, 29, 68, 89, 91, 98	12, 20, 22, 53, 69, 71, 77, 87, 90	12, 23, 25, 53, 67, 69, 76, 86, 89	12, 14, 45, 5, 56, 58, 64, 72	12, 14, 36, 42, 44, 5, 50, 56	14, 16, 35, 41, 43, 49, 5, 55	10, 28, 30, 32, 38, 40, 5, 8	10, 27, 30, 32, 37, 41, 5, 8
UC1_CTS_CS0	UNICOMM1 CTS: UART Clear To Send CS0: SPI Chip Select 0	IO	103, 113, 122, 16, 27, 69, 92	20, 54, 72, 85, 94	23, 54, 70, 84, 93	12, 46, 59, 76	12, 37, 45, 60	14, 36, 44, 59	29, 33, 44, 8	28, 33, 45, 8

Table 5-33. UC2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC2_CTS	UNICOMM2 CTS: UART Clear To Send	O	112, 17, 73, 83, 87, 98	10, 58, 67, 77, 84	58, 65, 76, 83	54, 64, 71	40, 50, 55	39, 49, 54	38	37
UC2_RTS	UNICOMM2 RTS: UART Release To Send	O	113, 18, 33, 74, 82, 88, 90, 99	11, 26, 59, 68, 70, 78, 85	29, 59, 66, 68, 77, 84	18, 55, 57, 65	18, 41, 43, 51	20, 40, 42, 50	12, 31, 39	12, 31, 38
UC2_RX_SCL	UNICOMM2 RX: UART Receive SCL: I2C Clock	IO	1, 101, 107, 109, 122, 15, 18, 20, 27, 51, 53, 70, 75, 76, 80, 85, 91	1, 11, 13, 20, 38, 55, 60, 61, 65, 71, 80, 83, 94	1, 13, 23, 38, 55, 60, 61, 63, 69, 79, 82, 93	12, 30, 47, 52, 58, 6, 67, 70, 76	12, 38, 44, 53, 6, 60	14, 37, 43, 52, 59, 6	32, 44, 6, 8	29, 32, 40, 45, 6, 8
UC2_TX_SDA	UNICOMM2 TX: UART Transmit SDA: I2C Data	O	100, 108, 121, 16, 17, 19, 2, 28, 52, 54, 71, 75, 76, 81, 86, 92	10, 12, 2, 21, 39, 56, 60, 61, 66, 72, 79, 82, 93	12, 2, 24, 39, 56, 60, 61, 64, 70, 78, 81, 92	13, 31, 48, 5, 53, 59, 66, 69, 75	13, 39, 45, 5, 52, 59	15, 38, 44, 5, 51, 58	33, 43, 5, 9	33, 39, 44, 5, 9

Table 5-34. UC3 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC3_RTS_POCI	UNICOMM3 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	O	119, 2, 3, 33, 35, 40, 57, 74, 93, 97, 99	2, 26, 28, 3, 33, 42, 59, 73, 78, 91	2, 29, 3, 31, 36, 42, 59, 71, 73, 77, 90	18, 20, 25, 34, 60, 65, 73	18, 20, 25, 46, 51, 57	20, 22, 27, 45, 50, 56	12, 14, 17, 34, 39, 41	12, 14, 18, 34, 38, 42
UC3_RX_SCL_SCLK	UNICOMM3 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	IO	1, 100, 101, 102, 105, 112, 118, 120, 122, 123, 124, 126, 22, 34, 38, 58, 61, 62, 65, 84, 87, 89, 9, 96	1, 15, 27, 31, 43, 46, 47, 50, 67, 69, 76, 79, 80, 81, 84, 9, 90, 92, 94, 95, 96, 98	1, 15, 30, 34, 43, 46, 47, 65, 67, 72, 78, 79, 80, 83, 89, 9, 91, 93, 95, 96, 98	19, 23, 35, 38, 39, 4, 42, 54, 56, 63, 66, 67, 68, 71, 72, 74, 76, 77, 78, 8	19, 23, 30, 33, 4, 40, 42, 49, 52, 53, 54, 55, 56, 58, 60, 61, 62, 8	21, 25, 29, 39, 4, 41, 46, 51, 52, 53, 54, 55, 57, 59, 61, 62, 8	13, 22, 25, 30, 37, 4, 40, 42, 44, 45, 46	13, 22, 24, 30, 36, 39, 4, 40, 41, 43, 45, 46, 47

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Table 5-34. UC3 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC3_TX_SDA_PICO	UNICOMM3 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	O	100, 101, 102, 106, 107, 112, 118, 120, 121, 122, 123, 124, 125, 23, 36, 37, 5, 60, 61, 62, 65, 8, 86, 88	16, 29, 30, 45, 46, 47, 5, 50, 68, 79, 8, 80, 81, 84, 90, 92, 93, 94, 95, 96, 97	16, 32, 33, 45, 46, 47, 5, 66, 78, 79, 8, 80, 83, 89, 91, 92, 93, 95, 96, 97	21, 22, 3, 37, 38, 39, 42, 55, 66, 67, 68, 71, 72, 74, 75, 76, 77, 78, 9	21, 22, 3, 30, 33, 41, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 9	23, 24, 29, 3, 40, 51, 52, 53, 54, 55, 57, 58, 59, 61, 62, 9	15, 22, 25, 3, 40, 42, 43, 44, 45, 46	15, 16, 22, 24, 3, 39, 40, 41, 43, 44, 45, 46, 47
UC3_CTS_CS0	UNICOMM3 CTS: UART Clear To Send CS0: SPI Chip Select 0	IO	101, 119, 120, 35, 4, 59, 66, 67, 73, 85, 92, 96	28, 4, 44, 51, 52, 58, 72, 76, 80, 91, 92	31, 4, 44, 51, 52, 58, 70, 72, 79, 90, 91	20, 36, 43, 44, 59, 63, 67, 73, 74	20, 34, 35, 45, 49, 53, 57, 58	22, 33, 34, 44, 46, 52, 56, 57	14, 26, 27, 33, 37, 41, 42	14, 25, 26, 33, 36, 40, 42, 43

Table 5-35. UC4 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC4_RTS_POCI	UNICOMM4 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	O	114, 15, 19, 66, 68, 77	12, 51, 53, 62, 86	12, 51, 53, 62, 85	43, 45, 5	34, 36, 5	33, 35, 5	26, 28, 5	25, 27, 5
UC4_RX_SCL_SCLK	UNICOMM4 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	IO	11, 116, 119, 18, 28, 37, 90, 91, 97	11, 21, 30, 70, 71, 88, 91	24, 33, 68, 69, 73, 87, 90	13, 22, 57, 58, 73	13, 22, 43, 44, 57	15, 24, 42, 43, 56	31, 32, 41, 9	16, 31, 32, 42, 9
UC4_TX_SDA_PICO	UNICOMM4 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	O	10, 115, 17, 27, 68, 89, 90, 91	10, 20, 53, 69, 70, 71, 87	23, 53, 67, 68, 69, 86	12, 45, 56, 57, 58	12, 36, 42, 43, 44	14, 35, 41, 42, 43	28, 30, 31, 32, 8	27, 30, 31, 32, 8
UC4_CTS_CS0	UNICOMM4 CTS: UART Clear To Send CS0: SPI Chip Select 0	IO	113, 122, 16, 69, 92	54, 72, 85, 94	54, 70, 84, 93	46, 59, 76	37, 45, 60	36, 44, 59	29, 33, 44	28, 33, 45

Table 5-36. UC5 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC5_CTS	UNICOMM5 CTS: UART Clear To Send	O	10, 112, 17, 73, 83, 88, 98	10, 58, 68, 77, 84	58, 66, 76, 83	55, 64, 71	41, 50, 55	40, 49, 54	38	37
UC5_RTS	UNICOMM5 RTS: UART Release To Send	O	11, 113, 18, 33, 74, 82, 87, 90, 99	11, 26, 59, 67, 70, 78, 85	29, 59, 65, 68, 77, 84	18, 54, 57, 65	18, 40, 43, 51	20, 39, 42, 50	12, 31, 39	12, 31, 38
UC5_RX_SCL	UNICOMM5 RX: UART Receive SCL: I2C Clock	IO	1, 10, 101, 107, 109, 122, 15, 17, 27, 51, 53, 70, 75, 76, 80, 85, 91	1, 10, 20, 38, 55, 60, 61, 65, 71, 80, 83, 94	1, 23, 38, 55, 60, 61, 63, 69, 79, 82, 93	12, 30, 47, 52, 58, 67, 70, 76	12, 38, 44, 53, 60	14, 37, 43, 52, 59	32, 44, 8	29, 32, 40, 45, 8

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Table 5-36. UC5 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
UC5_TX_SDA	UNICOMM5 TX: UART Transmit SDA: I2C Data	O	100, 108, 11, 121, 16, 18, 2, 28, 52, 54, 71, 75, 76, 81, 86, 92	11, 2, 21, 39, 56, 60, 61, 66, 72, 79, 82, 93	2, 24, 39, 56, 60, 61, 64, 70, 78, 81, 92	13, 31, 48, 53, 59, 66, 69, 75	13, 39, 45, 52, 59	15, 38, 44, 51, 58	33, 43, 9	33, 39, 44, 9

Table 5-37. VREF Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	LQFP128 PIN	LQFP100 G PIN	LQFP100 H PIN	LQFP80 PIN	LQFP64 G PIN	LQFP64 H PIN	LQFP48 PIN	QFN48 PIN
VREFHI	Positive ADC Voltage Reference	AREF	43, 44	36	21, 22	28	28	13	20	20
VREFLO	Negative ADC Voltage Reference	AREF	42	35	20	27	27	12	19	PAD

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5.5 Pin Connectivity Requirements

Pin Number	Pin Name	Pin Connectivity Requirements
See DEBUG Signal Descriptions Table	DEBUG_JTCK_SWCLK DEBUG_JTDI DEBUG_JTDO_SWO	Each of these pins must be connected to the corresponding power supply through separate external pull resistors to ensure these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull–up may be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
See ADCCAL Signal Descriptions Table	ADCINCAL0	If all Ax_y inputs for all ADC instances (ADC[0:2]_AIN[0:31]) are not used, the ADCINCAL0 analog pin must be connected (shorted) directly to ground (VSS).
ADC PIN	A[0:2]_[0:31]	Any unused Ax_y input pin for any ADC instance (ADC[0:2]_AIN[0:31]) must be connected (shorted) directly to ground (VSS).
LVCMOS PIN	Any LVCMOS Voltage Buffer Pin	If an associated IOMUX pad configuration register exists for a given pin, it may remain unconnected. After NRST, the LVCMOS voltage buffer is configured to a default state compatible with an unconnected pin.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

Parameters		MIN	MAX	UNIT
Supply voltage	VDD with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage (3)	V_{IN} (3.3V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current - per pin (4) (5)	I_{IK} - V_{IN} < VSS/VSSA - V_{IN} > VDD/VDDA)	–20	20	mA
Input clamp current - total for all inputs (4) (5)	$I_{IKTOTAL}$ - V_{IN} < VSS/VSSA - V_{IN} > VDD/VDDA)	–20	20	mA
Current of SDIO pin(6)	I_{IO_SD}		4	mA
Current of HSIO pin(6)	I_{IO_HS}		6	mA
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Ambient temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature(7)	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Input clamp current must also be observed.
(4) Continuous clamp current per pin is ±2mA. Do not operate in this condition continuously as V_{DD}/V_{DDA} voltage may internally rise and impact other electrical specifications.
(5) Applying a V_{IN} greater than VDD/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current to flow to the respective supply rail. If this occurs, the current must be kept within the MIN/MAX listed to prevent permanent damage to the device.
(6) Refer to Digital IO Features by IO Type table in Pin Attributes section, SDIO includes SD, SDL and SDW IOs, HSIO includes HS IO.
(7) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

6.2 ESD Ratings – Commercial

				VALUE	UNIT
AM13E23019, AM13E23018, AM13E23017 in 128-pin PDT TQFP					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins except corner pins	±500	
			Corner pins on 128-pin PDT: 1, 32, 33, 64, 65, 96, 97, 128	±750	
AM13E23019, AM13E23018, AM13E23017 in 100-pin PZ LQFP					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins except corner pins	±500	
			Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100	±750	
AM13E23019, AM13E23018, AM13E23017 in 80-pin PN LQFP					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins except corner pins	±500	
			Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80	±750	
AM13E23019, AM13E23018, AM13E23017 in 64-pin PM LQFP					

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				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins except corner pins	±500	
			Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64	±750	
AM13E23019, AM13E23018, AM13E23017 in 48-pin PT LQFP					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins except corner pins	±500	
			Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48	±750	
AM13E23019, AM13E23018, AM13E23017 in 48-pin RGZ VQFN					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins except corner pins	±500	
			Corner pins on 48-pin RGZ: 1, 12, 13, 24, 25, 36, 37, 48	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Parameters		MIN	NOM	MAX	UNIT
Device supply voltage, VDD and VDDA	Internal BOR enabled[1]	3.1	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device ground, VSS			0		V
Analog ground, VSSA			0		V
V_{IN}	Digital input voltage [2]	VSS – 0.3		VDD + 0.3	V
	Analog input voltage [2]	VSSA – 0.3		VDDA + 0.3	V
Capacitor connected between VDD and VSS, C_{VDD}	Filter capacitor[3]		10		µF
Junction temperature, T_J	T Series	–40		140	°C
Free-Air temperature, T_A	T Series	–40		125	°C

(1) Internal BOR is enabled by default.
(2) Applying a VIN greater than VDD/VDDA or less than VSS/VSSA voltage will internally rise and could impact other electrical characteristics.
(3) Connect C_{VDD} between VDD and VSS as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}

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6.4 Supply Current Characteristics

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

6.4.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled (unless otherwise noted).

PARAMETER		TEST CONDITIONS			25°C		55°C		85°C		105°C		125°C		UNIT
		V_{DD}	V_{DDC}	MCLK	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode															
I_{DD} (Run) (1) (4)	MCLK=SYSPLL, CoreMark, execute from RAM (SRAM3) (2)	3.3V	1.35V	250MHz	56.8										mA
				200MHz	45.6										
				170MHz											
				135MHz											
			1.30V	180MHz	41.4										
			1.25V	170MHz	37.1										
			1.20V	160MHz	33.7										
				150MHz	32.0										
				135MHz	29.2										
				120MHz	26.4										
				100MHz	22.7										
				80MHz	19.0										
				50MHz	13.4										mA
	MCLK=SYSOSC, CoreMark, execute from RAM (SRAM3) (2)	3.3V	1.20V	32MHz	8.3										mA
I_{DD} (Run) (1) (4)	MCLK=SYSPLL, CoreMark, execute from flash (2)	3.3V	1.35V	250MHz	58.9										mA
				200MHz	47.6										
				170MHz											
				135MHz											
			1.30V	180MHz	42.7										
			1.25V	170MHz	38.0										
			1.20V	160MHz	34.7										
				150MHz	33.0										
				135MHz	30.1										
				120MHz	27.2										
				80MHz	19.5										
				50MHz	13.7										
	MCLK=SYSOSC, CoreMark, execute from flash	3.3V	1.20V	32MHz	11.8										

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VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled (unless otherwise noted).

PARAMETER		TEST CONDITIONS			25°C		55°C		85°C		105°C		125°C		UNIT
		V_{DD}	V_{DDC}	MCLK	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Run) with motor control (3) (4)	MCLK=SYSPLL, CoreMark, execute from flash (2)	3.3V	1.35V	250MHz											mA
				200MHz	57.9										
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz	46.5										
			1.20V	160MHz											
				150MHz	40.0										
				135MHz											
				120MHz	32.9										
				100MHz	28.2										
SLEEP Mode															
I_{DD} (Sleep)	MCLK=SYSPLL, SYSPLLREF=SYSOSC CPU is halted	3.3V	1.35V	250MHz											µA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	135MHz											
				100MHz											
				32MHz											µA
I_{DD} (Sleep)	MCLK=SYSOSC, PLL is disabled CPU is halted	3.3V	1.20V	32MHz											µA

(1) Current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency
(2) V_{DDC} (Core Voltage) can be set to the right value to reduce the current consumption based on the required running frequency (MCLK)
(3) Motor Control App - 3 PWMs running at 10KHz(All PWM out's are mapped to GPIOs), ADC conversion happening with PWM triggers, DMA initialized, 3 SPI instances initialized with waiting for data over GPIOs, CPU is executing continuously at while(1) from Flash with Cache enabled and 3ws access
(4) Guaranteed by characterization results, unless otherwise specified.

6.4.2 STOP/STANDBY Modes

VDD=3.3V. All inputs in VDD domain tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
I_{DD} (Stop)	SYSOSC=32MHz, USE4MHZSTOP=1, DISABLESTOP=0	4MHz			240								uA
STANDBY0 Mode													
I_{DD} (Standby 0)	GPIOA enabled, RAM retention, PD0 all clocked	32kHz			196								uA
STANDBY1 Mode													

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VDD=3.3V. All inputs in VDD domain tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Standby 1)	GPIOA enabled, RAM retention, PD0 all clock gated	OFF			196								uA

6.4.3 SHUTDOWN Mode

All inputs in VDD domain tied to 0V or VDD. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Shutdown)	Supply current in SHUTDOWN mode	3.3V			2.5								uA

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6.4.4 Reducing Current Consumption

The AM13E23x devices provide some methods to reduce the device current consumption:

- One of the three low-power modes—SLEEP, STOP or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups and pulldowns on pins that assume an output function.
- Each peripheral has an individual power enable bit (PWREN_MCPERIPH or PWREN_SYSPERIPH). Reduced current consumption may be achieved by disabling the power to any peripheral that is not used in a given application. The *Typical Current Reduction per Disabled Peripheral* table lists the typical current reduction that may be achieved by disabling the power using the PWREN_MCPERIPH or PWREN_SYSPERIPH register, see the *Power Management and Clock Unit (PMCU)* chapter of the *AM13E230x Microcontrollers Technical Reference Manual*.
- To realize the lowest VDDA current consumption in an LPM, see the *Analog-to-Digital Converter (ADC)* chapter of the *AM13E230x Microcontrollers Technical Reference Manual* to ensure each ADC module is powered down as well.

6.4.4.1 Typical Current Reduction per Disabled Peripheral

All I/O pins configured in Analog or Input mode. All peripherals clocked/powered off, with only a single peripheral active to measure its current consumption. Nominal ambient temperature (25°C) and supply voltage (3.3V).

PERIPHERAL	I_{DD} (Typ)	Unit
ADC(1) (2)		mA
XBAR(3)		mA
CMPSS (0~3)(3)		mA
CMPSS_DACL		mA
MCPWM (0~4)(3)		mA
eCAP (0~1)(3)	0.12	mA
eQEP (0~2)(3)	0.18	mA
EPI(3)		mA
PGA (0~2)(3)		mA
TINIE(3)		mA
TIMERG12		mA
TIMERG4		mA
UNICOMM (0~5)		mA
MCAN (CAN-FD)		mA
DMA		mA
FCC		mA
EAM		mA
CRC		mA
KEYSTORE		mA
AES		mA

(1) This current represents the current drawn by the digital portion of the each module.
(2) The ADC modules are powered down upon reset. Use ADCCTL1 to power down or up ADC.
(3) All peripherals are disabled upon reset. Use the PWREN_MCPERIPH or PWREN_SYSPERIPH register to individually disable or enable the power to peripherals. For peripherals with multiple instances, the current quoted is for a single module.

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6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDD * 0.8			V
			I_{OH} = –100µA	VDD – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins		VOH=VDDS-0.4V		66		Ω
R_{OL}	Low-level output impedance for all output pins		VOL=0.4V		60		Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDD = 3.3V V_{IN} = VDD		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled(1)	VDD = 3.3V V_{IN} = 0 V		160		µA
$R_{PULLDOWN}$	Weak pulldown resistance				40		kΩ
R_{PULLUP}	Weak pullup resistance				40		kΩ
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDD			0.1	µA
I_{LEAK}	Pin leakage	Analog pins	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	µA
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins(2)					
POR and BOR							
POR, BOR(3)							

(1) See Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section.
(3) See the *Power Management Module (PMM)* section.

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6.6 Digital IO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Electrical Characteristics							
V_{IH}	High level input voltage	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	0.7*VDD		VDD+0.3	V
		Reset pin	2.8 ≤ VDD ≤ 3.6	0.85*VDD		VDD+0.3	
V_{IL}	Low level input voltage	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	-0.3		0.3*VDD	
		Reset pin	2.8 ≤ VDD ≤ 3.6	-0.3		0.15*VDD	V
V_{HYS}	Hysteresis	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	0.1*VDD			
		Reset pin	2.8 ≤ VDD ≤ 3.6	0.3*VDD			
I_{lkg}	High-Z leakage current(1) (2)	SDIO	2.8 ≤ VDD ≤ 3.6			50	nA
		HSIO	2.8 ≤ VDD ≤ 3.6			200	nA
R_{PU}	Pull up resistance		VIN = VSS		40		kΩ
R_{PD}	Pull down resistance		VIN = VDD		40		kΩ
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, I_{IO}=–4mA	VDD-0.4			V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=–6mA	VDD-0.4			
			VDD≥2.7V, DRV=0, I_{IO}=–4mA	VDD-0.4			
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, I_{IO}=4mA			0.4	V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=6mA			0.4	
			VDD≥2.7V, DRV=0, I_{IO}=4mA			0.4	
Switching Characteristics							
f_{max}	Port output frequency	SDIO (3)	VDD ≥ 2.7V, C_L= 20pF			32	MHz
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L= 20pF			50	
			VDD ≥ 2.7V, DRV = 0, C_L= 20pF			32	
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, C_L = 20pF			3.5	ns
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L = 20pF			1.8	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			5.9	

(1) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) The sum of the $|I_{IO}|$ current sourced or sunk by the device must always respect the absolute maximum rating

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6.7 Thermal Information

This section provides the thermal resistance characteristics used on this device. For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

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6.8 System

6.8.1 Power Supply Sequencing

6.8.1.1 Power Supply Ramp

Figure 6-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

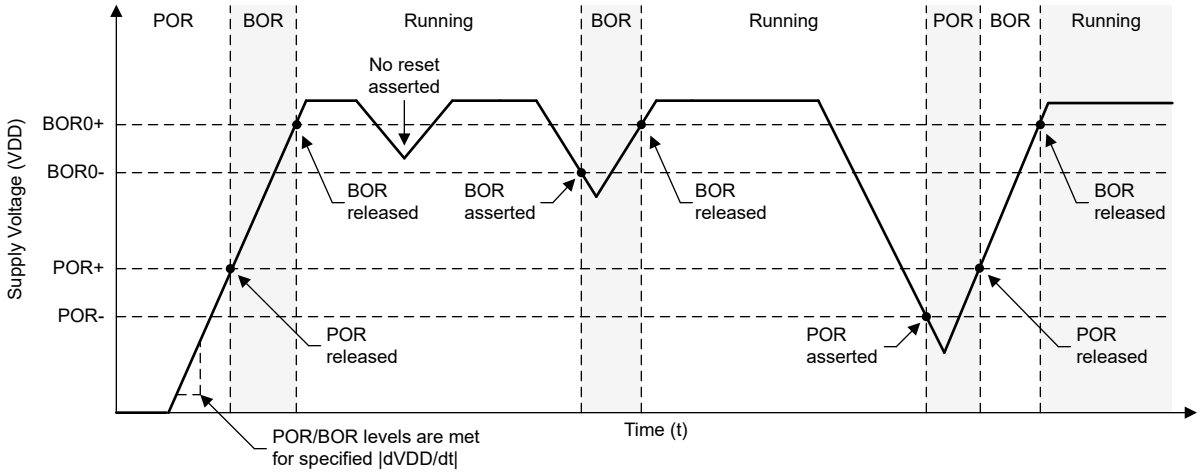


Figure 6-1. Power Cycle POR and BOR Conditions

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6.8.1.2 POR and BOR

The two voltage monitors (POR and BOR) have to release their respective outputs before the device begins operation (that is, NRST goes high). However, if either of the voltage monitors trips, NRST is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

The POR monitor supervises the VDD rail. During power up, this is the first monitor to release (that is, first to untrip) on VDD.

The BOR monitor also supervises the VDD rail. During power up, this is the second monitor to release (that is, second to untrip) on VDD. This monitor has a tighter tolerance compared to the POR.

Any drop in voltage below the recommended operating voltages will trip the BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The BOR can only be disabled after the device has fully booted up. If the BOR is disabled, the POR will reset the device for voltage drops.

6.8.1.2.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Power supply range		3.1	3.3	3.6	V
VDD	Power supply range	BOR bypass	2.8	3.3	3.6	V
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling (1)			0.01	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	0.95	1.30	1.59	V
V_{POR-}	Power-on reset voltage level	Falling	0.9	1.25	1.54	V
$V_{HYS, POR}$	POR hysteresis			50		mV
$V_{BOR+, COLD}$	Brown-out reset voltage (default level)	Cold start, rising	2.45	2.7	2.97	V
V_{BOR+}	Brown-out reset voltage (default level)	Rising (1)	2.8	2.885	2.97	V
V_{BOR-}	Brown-out reset voltage (default level)	Falling (1)	2.8	2.85	2.97	V
$V_{BOR, STBY}$	Brown-out reset voltage (default level)	STANDBY mode	2.73	2.84	2.97	V
$V_{HYS,BOR}$	Brown-out reset hysteresis			35		mV
$t_{PD:BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
$t_{PD:BOR}$	BOR propagation delay	STANDBY mode			100	us
C_{VDD} (2) (3)	VDD Capacitance Per Pin		0.1			uF
C_{VDDA} (2) (3)	VDDA Capacitance Per Pin		2.2			uF
$V_{BOR-VDD-GB}$ (4)	VDD Brown Out Reset Voltage Guardband			0.1		V
$I_{VREG(Run)-LOAD}$	Run Voltage Regulator Load Current				175	mA
$I_{VREG(Stop)-LOAD}$	Stop Voltage Regulator Load Current				5	mA

(1) Device operating in RUN, SLEEP, or STOP mode.
(2) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(3) It is recommended to tie the 3.3V rails (VDD, VDDA) together and supply them from a single source.
(4) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDD resets due to normal supply noise or load-transient events on the 3.3-V VDD system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDD during normal device operation. The value of $V_{BOR-VDD-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.

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6.8.1.3 Timing Characteristics

6.8.1.3.1 Timing Characteristics

over recommended operating conditions, VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE:SLEEP}$	Wakeup time from SLEEP to RUN (1)					µs
$t_{WAKE:STOP}$	Wakeup time from STOP to RUN (SYSOSC enabled) (1)			68		µs
$t_{WAKE:STBY}$	Wakeup time from STANDBY0 to RUN (1)			120		µs
	Wakeup time from STANDBY1 to RUN (1)			121		µs
$t_{WAKEUP:SHDN}$	Wakeup time from SHUTDOWN to RUN			1040		µs
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP				µs
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0				
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1				
Startup Timing						
$t_{START:RESET}$	Device cold startup time from reset/ power-up (2)					µs
NRST Timing						
$t_{RST:BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz				µs
		ULPCLK=32kHz				
$t_{RST:POR}$	Pulse length on NRST pin to generate POR					s

(1) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(2) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

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6.8.2 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim
- **LFXT/LFCKIN** : Low-frequency external crystal oscillator or digital clock input (32 kHz)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 250 MHz)

6.8.2.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=0 (BASE)		32		MHz
		SYSOSCCFG.FREQ=1		4		
f_{SYSOSC}	SYSOSC frequency accuracy with FCL enabled(1) (2)	-40℃ ≤ Ta ≤ 70℃	-1.0		1.0	%
		-40℃ ≤ Ta ≤ 90℃ (3) (4)	-1.0		1.0	%
		-40℃ ≤ Ta ≤ 105℃ (3) (4)	1.4		1	%
		-40℃ ≤ Ta ≤ 125 ℃ (3) (4)	-2.0		1	%
		-20℃ ≤ Ta ≤ 90℃ over 10 years(4)				%
		-40℃ ≤ Ta ≤ 105℃ over 10 years(4)				%
	SYSOSC raw frequency accuracy with FCL disabled, 32MHz(5)	SYSOSCCFG.FREQ=0, -40℃ ≤ T_a ≤ 105℃				%
	SYSOSC frequency accuracy with FCL disabled, 4MHz	SYSOSCCFG.FREQ=1, -40℃ ≤ T_a ≤ 105℃				%
$t_{settle, SYSOSC}$	Settling time to target accuracy(6)	SETUSEFCL=1				us
$f_{settle, SYSOSC}$	f_{SYSOSC} accuracy during t_{settle} (6)	SETUSEFCL=1	-11			%

(1) f_{SYSOSC} may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.
(2) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.
(3) Data is preliminary, derived from characterization and design, not verified through production testing.
(4) Power consumption is assumed to be 0.25W.
(5) SYSOSC accuracy is measured in the default power-up state, with MCLK = SYSOSC, the CPU executing a continuous while(1) loop, and the SYSPLL disabled.
(6) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.

6.8.2.2 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High Frequency External Crystal Oscillator (XTAL)						
f_{XTAL}	XTAL frequency	USEHSCLK=1, USEEXTHFCLK=0	4		48	MHz
DC_{XTAL}	XTAL duty cycle	USEHSCLK=1, USEEXTHFCLK=0		50		%
OA_{XTAL}	XTAL crystal oscillation allowance	4 to 48MHz range		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)	USEHSCLK=1, USEEXTHFCLK=0		1		pF
$t_{start, XTAL}$	XTAL start-up time (2)	32MHz crystal		0.5		ms
I_{HFXT}	XTAL current consumption	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		75		uA
		f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High Frequency Digital Clock Input (HFCLK_IN)						

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFIN}	HFCLK_IN frequency (3)	USEHSCLK=1, USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{X1}×C_{X2}/(C_{X1}+C_{X2})$, where C_{X1} and C_{X2} are the total capacitance at SYSCTL_X1 and SYSCTL_X2, respectively.
(2) The High Frequency External Crystal Oscillator (XTAL) startup time ($t_{start, XTAL}$) is measured from the time the XTAL is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the External Crystal Oscillator (XTAL) section of the AM13E230x Microcontrollers Technical Reference Manual
(3) The digital clock input (SYSCTL_HFCLKIN) accepts a logic level square wave clock.

6.8.2.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range		4		48	MHz
f_{VCO}	VCO output frequency	BIASRANGEFIX should be HIGH and by default this is recommended mode of operation.	160		800	MHz
f_{SYSPLL}	SYSPLL output frequency range (1)	SYSPLLCLK0, SYSPLLCLK1	5		400	MHz
		SYSPLLCLK2X	20		400	
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz; SYSPLLCLK2X	30		70	%
		$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, SYSPLLCLK0/1	45		55	%
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	$f_{SYSPLLREF}$=32MHz, fINTCLK = 8MHz		TBD		%
	SYSPLL RMS period jitter		-2.5		2.5	
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, PDIV=2; SYSPLL =400 MHz			1.35	mA
$t_{start, SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, PDIV=2; SYSPLL =200 MHz, ±1% accuracy			24.5	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.

6.8.2.4 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T_a ≤ 125 °C	–5		5	%
		-40 °C ≤ T_a ≤ 85 °C	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1.7		ms

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6.8.3 Flash Memory Characteristics

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 256-bit-wide prefetch reads, a pipeline buffer and code block cache. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has SECCFG sectors which are used for security configuration and flash management.

Table 6-1 lists the minimum required wait states for AM13E230 flash at different frequencies.

Table 6-1. Minimum Required AM13E230 Flash Wait States with Different Clock Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT][1])
200 < CPUCLK ≤ 250	4
150 < CPUCLK ≤ 200	3
100 < CPUCLK ≤ 150	2
0 < CPUCLK ≤ 100	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

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6.8.3.1 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		3.1		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
N_{WEC}	Write/Erase cycle endurance		20			k cycles
N_{WEC}	Write/Erase Cycles for entire device (limited by flash pump endurance)		20			k cycles
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	20			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 128)}$	Program time for flash word (1) (3)			40		µs
$t_{PROG\ (SEC,\ 128)}$	Program time for 2kB sector (2) (3)			5.1		ms
t_{ERASE} (4) (5)	2KB (sector) erase time	at < 25 erase/program cycles		15	55	ms
	64KB erase time			17	61	ms
	128KB erase time			18	66	ms
	256KB erase time			21	78	ms
t_{ERASE}	2KB (sector) erase time	at 1000 erase/program cycles		25	130	ms
	64KB erase time			28	143	ms
	128KB erase time			30	157	ms
	256KB erase time			35	183	ms
t_{ERASE}	2KB (sector) erase time	at 2000 erase/program cycles		30	221	ms
	64KB erase time			33	243	ms
	128KB erase time			36	265	ms
	256KB erase time			42	310	ms
t_{ERASE}	2KB (sector) erase time	at 20K erase/program cycles		120	1003	ms
	64KB erase time			132	1102	ms
	128KB erase time			145	1205	ms
	256KB erase time			169	1410	ms
F_{CLK}	Flash clock frequency				50	MHz

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.

(3) Flash word size is 128 data bits (16 bytes). On devices with ECC, the total flash word size is 144 bits (128 data bits plus 16 ECC bits).

(4) Erase time includes Erase verify by the CPU.

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(5) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

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6.8.4 RAM Specifications

The device includes a 128kB of SRAM across four banks fully protected by hardware parity. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code.

- SRAM0 (32kB) memory fully retained in low power modes of STOP and STANDBY operating mode.

The Table 6-2 describes the operational conditions for the multiple SRAM banks on the device.

Table 6-2. SRAM Bank Property

	SRAM0	SRAM1/2/3
0-Wait State Frequency	200MHz / 250MHz	200MHz / 250MHz
Safety	Parity	Parity
Security	GSC based	GSC based
RUN Mode State	ACTIVE	ACTIVE
SLEEP Mode State	ACTIVE	ACTIVE
STOP Mode State	RETAINED	OFF
STANDBY 0 Mode State	RETAINED	OFF
STANDBY 1 Mode State	RETAINED	OFF
SHUTDOWN Mode State	OFF	OFF

For more details, see the SRAM chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

6.8.5 ROM Specifications

Table 6-3. ROM Parameters

ROM Block	SIZE EACH	ECC/Parity	Secured	WAIT STATES	HOST ACCESS LIST
CPU Boot ROM	48KB	No	No	1 @ 200MHz / 250MHz	CPU1

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6.9 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device includes 3 Analog-to-Digital Converters(ADC), 1 Temperature Sensor, 3 Programmable Gain Amplifiers (PGA), and 4 Comparator Subsystems (CMPSS).

The analog subsystem has the following features:

- Flexible voltage references
  - The ADC is referenced to VREFHI and VREFLO pins.
    - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
    - The internal voltage reference range can be selected to be 0V to 2.5V
  - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
  - Low comparator DAC (COMPDACOUT) can optionally be brought out to a multiplexed ADC pin for external use (mutually exclusive with use of CMPSS compare functions and only available on some CMPSS instances)
  - Internal connection to VREFLO on ADC for offset self-calibration

6.9.1 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based.

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 32 channels
- 16 configurable SOCs controlled by sequencers (SEQ[0:3])
- 16 individually addressable result registers
- Sample cap reset feature for memory crosstalk mitigation
- Multiple trigger sources
  - Software immediate start
  - All MCPWMs: ADCSOC A or B
  - GPIO (external SOC)
  - GP Timers 0/1
  - ADCINT1/2
  - eCAP events in capture mode (CEVT1, CEVT2, CEVT3, and CEVT4) and APWM mode (period match, compare match, or both).
  - Global software trigger for multiple ADCs
- Four flexible interrupts
- Burst-mode triggering option
- Hardware oversampling mode up to 128x, with configurable trigger spread delay
- Hardware undersampling mode
- Trigger phase delay function

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- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and MCPWM trip capability
  - Configurable digital filter for high/low/zero-crossing compare
  - Trigger-to-sample delay capture
  - Absolute value calculation
  - 24-bit accumulation register for oversampling, with configurable binary shift
  - Minimum/maximum calculation for outlier rejection

6.9.1.1 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.9.1.1.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from MCLK)	200MHz MCLK	5		100	MHz
	250MHz MCLK	5		125	MHz
Sample rate(4) (5)	100MHz ADCCLK, SAMPCAPRESETSEL = 0			6.25	MSPS
	100MHz ADCCLK, SAMPCAPRESETSEL = 1			6.67	MSPS
	125MHz ADCCLK, SAMPCAPRESETSEL = 0			7.35	MSPS
	125MHz ADCCLK, SAMPCAPRESETSEL = 1			7.81	MSPS
Sample window duration (set by ACQPS and MCLK)(1)	With 50Ω or less R_s	40			ns
	Internal VREFLO Connection	40			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
VREFHI - VREFLO		2.4		VDDA	V
Conversion range	Internal Reference = 3.3V Range	0		3.3	V
	Internal Reference = 2.5V Range	0		2.5	
	External Reference	VREFLO		VREFHI	
Conversion range	Package = QFN48	0		VDDA(3)	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

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(3) On QFN48 package, VREFHI is internally tied to VDDA and VREFLO is internally tied to VSSA. Internal reference mode is not supported on QFN48 package.
(4) Non-integer ADC clock dividers are not supported: ADCCTL2.PRESCALE should only use even values
(5) Sample and hold cap reset feature must be enabled; SAMPCAPRESETSEL = 0

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6.9.1.1.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles(1)				11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5V range and 3.3V range.			5000	µs
VREFHI input current(2)			200		µA
Internal Reference Capacitor Value(3)		2.2			µF
External Reference Capacitor Value(3)		2.2			µF
DC Characteristics					
Gain Error	Internal reference		±45		LSB
	External reference		±5		
Offset Error			±2		LSB
Channel-to-Channel Gain Error(5)			2		LSB
Channel-to-Channel Offset Error(5)			2		LSB
ADC-to-ADC Gain Error(6)	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error(6)	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error			±1.0		LSB
INL Error			±2.0		LSB
ADC-to-ADC Isolation	VREFHI = 2.5V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1		67.08		dB
	VREFHI = 2.5V, fin = 100kHz, MCLK from SYSOSC		TBD		
THD(4)	VREFHI = 2.5V, fin = 100kHz		–77		dB
SFDR(4)	VREFHI = 2.5V, fin = 100kHz		82		dB
SINAD(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1		67.08		dB
	VREFHI = 2.5V, fin = 100kHz, MCLK from SYSOSC		62.3		
ENOB(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1, Single ADC		10.8		bits
PSRR	VDDA = 3.3V DC + 200mV DC up to Sine at 1kHz		60		dB
	VDDA = 3.3V DC + 200mV Sine at 900kHz		57		

(1) Using SAMPCAPRESET feature; SAMPCAPRESETSEL = 1 and SAMPCAPRESETDISABLE = 0 inside the corresponding ADCSOCxCTL register.
(2) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(3) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(4) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(5) Variation across all channels belonging to the same ADC module.
(6) Worst case variation compared to other ADC modules.

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6.9.1.1.3 ADC Input Model

The ADC input characteristics are given by Figure 6-2 and Section ADC Input Model.

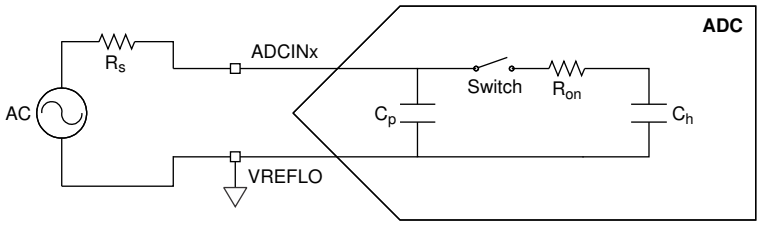


Figure 6-2. ADC Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the *Choosing an Acquisition Window Duration* section of the Analog-to-Digital Converter (ADC) chapter in the *AM13E230x Microcontrollers Technical Reference Manual* . For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Note.

ADC Input Model

over operating free-air temperature range (unless otherwise noted)

PARAMETER	Description	Reference Mode	TYP	UNIT
C_p	Parasitic input capacitance	All Modes		
R_{on}	Sampling switch resistance	External Reference, 2.5V Internal Reference	400	Ω
		3.3V Internal Reference	500	Ω
C_h	Sampling capacitance	External Reference, 2.5V Internal Reference	10	ρF
		3.3V Internal Reference	8	ρF
R_s	Nominal source impedance	All Modes	50	Ω

6.9.1.1.4 ADC Timing Requirements

		MIN	MAX	UNIT
$t_{su(ADCCHSEL-SOC)}$	ADCCHSEL valid before ADCSOC high	0.5		ns
$t_{su(ADCSOC)}$	ADCSOC low before ADCCLK high	1		ns
$t_{w(ADCCLK)}$	Width of ADCCLK	0.8		ns
$t_{w(ADCSOC)}$	Width of ADCSOC	0.6		ns

6.9.1.1.5 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(SYSCLK)}$		cycles

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6.9.2 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 8-bit DACs, and two digital filters. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin. The negative input can be driven by an external pin or by the programmable reference 10-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required.

Each CMPSS includes:

- Two analog comparators
- Two (10-bit effective DACs on CMPSS_LITE instances)
- Two digital filters, 65536 max filter clock prescale
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to synchronize output with MCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option for positive input of comparator to be driven by an external signal or by the PGA
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)

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6.9.2.1 CMPSS Electrical Data and Timing

6.9.2.1.1 CMPSS_LITE Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time	Bandgap Not Enabled			500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Via AIO/AGPIO, Input common mode = 5% to 95% of VDDA	–20		20	mV
Hysteresis[1]	Hysteresis[1]	0x	-6	0	6	mV
Hysteresis[1]		1x	1	10	19	mV
		2x	7	20	34	
		3x	14	30	51	
		4x	19	41	70	
		5x	25	52	88	
		6x	31	64	109	
		7x	37	77	131	
Response time (delay from CMPINx input change to output on MCPWM X-BAR or Output X-BAR)		Step response		21	40	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		
VDDA	Analog Supply		2.8	3.3	3.63	V
VDD	Core Supply		1.08	1.2	1.32	V
Tj	Temperature		–40	27	155	°C
Resolution				12		bits
Input Clock (SYSCLK) Frequency			1		100	MHz
Input Clock (SYSCLK) Pulse Width				TSYSCLK/2		
Conversion Range		VDAC	0		VDAC	V
Conversion Range		VDDA	0		VDDA	V
VDAC	VDAC Range		2.4	3.3	VDDA	V
DNL	Differential Non Linearity		–1		4	LSB
INL	Static Integral Non Linearity		–16		16	LSB
Ramp Linearity	Dynamic Ramp Error	20 DAC Input Steps per 60 MHz SYSCLK. Response Must be Monotonic.	–64		64	LSB
Full Scale Step Response Settling Time					1	µs
Comparator Trip Disturbance			–512	+/-120	512	LSB
Comparator Trip Disturbance Settling Time					200	ns
Gain	Gain Error		–2		2	% of FSR
Reference Input Impedence	Reference Input Impedance			8		kΩ
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
Ramp Response Time				26		ns
Slow Ramp Response Time				30		ns
Step Response Time		AIO			50	ns
Input Offsett Error	Input Offset Error	w/ Jitter Aggressor	–20	5	20	mV
Input Hysteresis from Ideal			–5	0	5	mV
CMRR	Common Mode Rejection Ratio		40			dB
IVDDA	Active Current (Analog Supply)	CMPSS			120	µA
IVDD	Active Current (Core Supply)	CMPSS			6	µA
IVDDA(leak)	Leakage Current (Analog Supply)	CMPSS				µA
IVDD(leak)	Leakage Current (Core Supply)	CMPSS				µA
IVDDA	Active Current (Analog Supply)	DAC		400		µA
IVDD	Active Current (Core Supply)	DAC		0		µA

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over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVDDA(leak)	Leakage Current (Analog Supply)	DAC				µA
IVDD(leak)	Leakage Current (Core Supply)	DAC				µA
dvt	Transient vt shift			5		mV

(1) Hysteresis is available for all comparator input source configurations.

6.9.2.1.2 CMPSS_LITE DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS_LITE DAC output range		0		VDDA	V
Static offset error(1)		–25		25	mV
Static gain error(1)		–0.5		0.5	% of FSR
Static DNL	Endpoint corrected	–5		5	LSB (12-bit)
Static INL	Endpoint corrected	–5		5	LSB (12-bit)
Static TUE (Total Unadjusted Error)				35	mV
Settling time	Settling to 1LSB after full-scale output change		1		µs
Resolution(2)			12		bits

(1) Includes comparator input referred errors.
(2) 9.5-bit effective resolution for monotonic response

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6.9.3 Programmable Gain Amplifier (PGA)

The Programmable Gain Amplifier (PGA) is used to amplify an input voltage for the purpose of increasing the effective resolution of the downstream ADC and CMPSS modules.

The integrated PGA helps to reduce cost and design effort for many control applications that traditionally require external, stand-alone amplifiers. On-chip integration ensures that the PGA is compatible with the downstream ADC and CMPSS modules. Software-selectable gain and filter settings make the PGA adaptable to various performance needs.

The PGA has the following features:

- Rail to rail input and output voltage within VDDA and VSSA range
- Programmable gain modes including unity gain and other values from 2X - 64X
- Standalone gain mode using off-chip passive components
- Post-gain filtering using on-chip resistors
- Differential input support
- Hardware assisted chopping for offset reduction
- Support for Kelvin ground connections using PGA_INM pins

The active component in the PGA is an embedded operational amplifier (op amp) that is configured as a non-inverting or inverting amplifier with internal feedback resistors. These internal feedback resistor values are paired to produce software selectable voltage gains.

Three PGA signals are available at the device pins:

- PGA_INP is the positive input to the PGA op-amp.
- PGA_INM is the negative input to the PGA op-amp. See the device data manual for more information.
- PGA_OUT supports op-amp output filtering with RC components. The filtered signal is available for sampling and monitoring by on-chip ADC and CMPSS modules.

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6.9.3.1 PGA Electrical Data and Timing

6.9.3.1.1 PGA Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDA		2.8	3.3	3.6	V
VDD		1.08	1.2	1.32	V
TEMP	T_J	–40	27	155	C
Clock Frequency		SYSCLK		150	MHz
Clock Duty Cycle		40	50	60	%
PGA Output Range(1)		VSSA+0.025		VDDA–0.025	V
PGA Input Range		–0.05		VDDA	V
Min ADC S+H	With Filter	75			ns
Min ADC S+H (No Filter, Level Shifting)		220			ns
Capacitive Load on PGA Out			40		pF

(1) This is the linear output range of the PGA. The PGA can output voltages outside this range, but the voltages will not be linear.

6.9.3.1.2 PGA Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
Min ADC S+H Settling within ±1 ADC LSB Accuracy (No Filter; All Gain Settings; Single ADC Driven) (5)	Gain = 1	125			ns
	Gain = 2/-1	146			
	Gain = 4/-3	125			
	Gain = 8/-7	154			
	Gain = 16/-15	227			
	Gain = 32/-31	322			
	Gain = 64/-63	420			
Gain Settings			1		
			2, 4, 8, 16, 32, 64		
			–1, –3, –7, –15, –31, –63		
Short Circuit Current (6)			41		mA
Full Scale Step Response (No Filter) Settling within 0.05% Accuracy(5)	G<64			420	ns
	G = 64/-63			500	ns
Settling Time: Gain Switching				10	µs
Slew Rate	Naked OPA Mode		12		V/µs
Slew Rate	Gain = 1		12		V/µs
	Gain = 2/-1		24		V/µs
	Gain = 4/-3		43		V/µs
	Gain = 8/-7		67		V/µs
	Gain = 16/-15		35		V/µs
	Gain = 32/-31		29		V/µs
	Gain = 64/-63		26		V/µs
Overload Recovery Time	Settling to 0.1%		.400		µs

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over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ia}	Gain = 1		256		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		7		kΩ
	Gain = 8/-7		8		kΩ
	Gain = 16/-15		8		kΩ
	Gain = 32/-31		8		kΩ
	Gain = 64/-63		4		kΩ
R_{ib}	Gain = 1		0		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		21		kΩ
	Gain = 8/-7		56		kΩ
	Gain = 16/-15		120		kΩ
	Gain = 32/-31		248		kΩ
	Gain = 64/-63		252		kΩ
Filter Resistor Targets	R_{FILT} = 800Ω		800		Ω
	R_{FILT} = 400Ω		400		Ω
	R_{FILT} = 200Ω		200		Ω
	R_{FILT} = 100Ω		100		Ω
	R_{FILT} = 50Ω		50	62	Ω
Active Current	VDDA Without Filter		1.3	1.7	mA
	VDDA With Filter		1.3	1.9	mA
	VDD Without Filter		10	200	uA
	VDD With Filter		10	200	uA
Leakage Current	VDDA		.02		µA
	VDD		.03		µA
Gain Bandwidth Product (Naked Op-Amp Mode)	Gain=1		7		MHz
Closed Loop -3bd BW	Gain=1		15		MHz
	Gain=2/-1		14		MHz
	Gain=4/-3		13.5		MHz
	Gain=8/-7		12		MHz
	Gain=16/-15		11		MHz
	Gain=32/-31		5.5		MHz
	Gain=64/-63		5.0		MHz
DC Characteristics					
Gain Error(1)	Gain = 1	–0.18		0.18	%
	Gain = 2, -1	–0.37		0.37	%
	Gain = 4, -3	–0.6		0.6	%
	Gain = 8, -7	–0.73		0.73	%
	Gain = 16, -15	–0.81		0.81	%
	Gain = 32, -31	–1.0		1.0	%
	Gain = 64, -63	–1.82		1.82	%
Offset Error (Untrimmed)	Input Referred	–8		8	mV
Offset Error(2)	Input Referred	–3.0	+/–1.0	3.0	mV
Offset Temp Coefficient	Input Referred	–7.0		7.0	µV/C

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over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Error - Chopped		–0.8		0.8	mV
Offset Temp Coefficient - Chopped			0.3		µV/C
Offset Trim Range	Min			–8	mV
	8			mV	
Long Term Offset Drift	Input Referred		3		mV
INL	With ADC	–3		3	12b LSB
DC Code Spread	G<64		2.5		12b LSB
	G = 64/-63		4		12b LSB
AC Characteristics					
Phase Margin Naked OPA	C_{load} = 40pF G=1		45		Deg
Aol (Open loop voltage gain) Naked OPA	R_L=7.5kΩ to GND 0.3V<V_O<VDDA-0.3V		94		dB
THD + Noise (THD+N) Naked OPA	f_{in}=1kHz G=1		82		dB
Bandwidth(3)	All Gain Modes		7		MHz
SNR 10kHz (With ADC)	Gain = 1		68		dB
	Gain = 2, -1		68		
	Gain = 4, -3		66		
	Gain = 8, -7		62		
	Gain = 16, -15		58		
	Gain = 32, -31		55		
	Gain = 64, -63		51		
THD(4)	DC		–78		dB
THD(Up to 100kHz) (4)	Gain = 1		–58		dB
	Gain = 2, -1		–70		
	Gain = 4, -3		–70		
	Gain = 8, -7		–70		
	Gain = 16, -15		–70		
	Gain = 32, -31		–58		
	Gain = 64, -63		–58		
CMRR	DC: V_{IN} <=1.5V		–86		dB
	DC: Full Input Range		–77		dB
	Up to 100kHz		–50		dB
PSRR(4)	DC		–75		dB
	Up to 10kHz		–60		dB
	Up to 100kHz		–40		dB
Noise PSD(4)	1kHz		200		nV/sqrt(Hz)
	10kHz		100		nV/sqrt(Hz)
Integrated Noise (Input Referred)(4)	3Hz to 30MHz		100		µV

(1) Includes ADC gain error.
(2) Includes ADC offset error.
(3) 3dB bandwidth.
(4) Performance of PGA alone.
(5) Step response time w filter = tS+H + 7.6*R_{filt}* C_{filt}

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(6) Assumes no filter circuit

6.9.4 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly (-2 mV/°C) with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

See the temperature sensor section of the *AM13E230x Microcontrollers Technical Reference Manual* for guidance on calculating the device temperature with the factory trim value.

6.9.4.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature, and provides a voltage output that changes linearly (-2 mV/°C) with device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software in MCU SDK. When sampling the temperature sensor, the ADC must meet the acquisition time in the *Temperature Sensor Characteristics* table."

See the temperature sensor section of the *AM13E230x Microcontrollers Technical Reference Manual*

for guidance on calculating the device temperature with the factory trim value.

6.9.4.2 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	Internal reference		±15		°C
T_{acc}	Temperature Accuracy	External reference		±15		°C
T_{TRIM}	Factory trim temperature	External reference	27	30	33	°C
T_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃, External reference	-2.1	-2	-1.9	mV/°C
dVout/dT	Temperature Sensitivity		3.3	3.8	4.3	mV/°C
t_{pu}	Power up time				500	µs
t_{SET}	Temperature sensor settling time				10	µs
t_{OS}	Voltage Output Settling Time				450	ns
PSR	Power Supply Rejection				40	dB
IDDA	Active Current (Analog Supply)			210	296	µA
IDD	Active Current (Core Supply)					µA
IDDA(leak)	Leakage Current (Analog Supply)			17	147	nA
IDD(leak)	Leakage Current (Core Supply)				400	nA

6.9.5 Internal Analog Connections

over operating free-air temperature range (unless otherwise noted)

Internal Signal	Connections
TEMPSENSOR	A0_13/A2_13
PGA0_OUT (Internal)	A0_31
PGA1_OUT (Internal)	A1_31
PGA2_OUT (Internal)	A2_31

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6.10 Control Peripherals

6.10.1 Multichannel Pulse Width Modulator (MCPWM)

The MCPWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The MCPWM module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the MCPWM module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-3 shows the MCPWM module.

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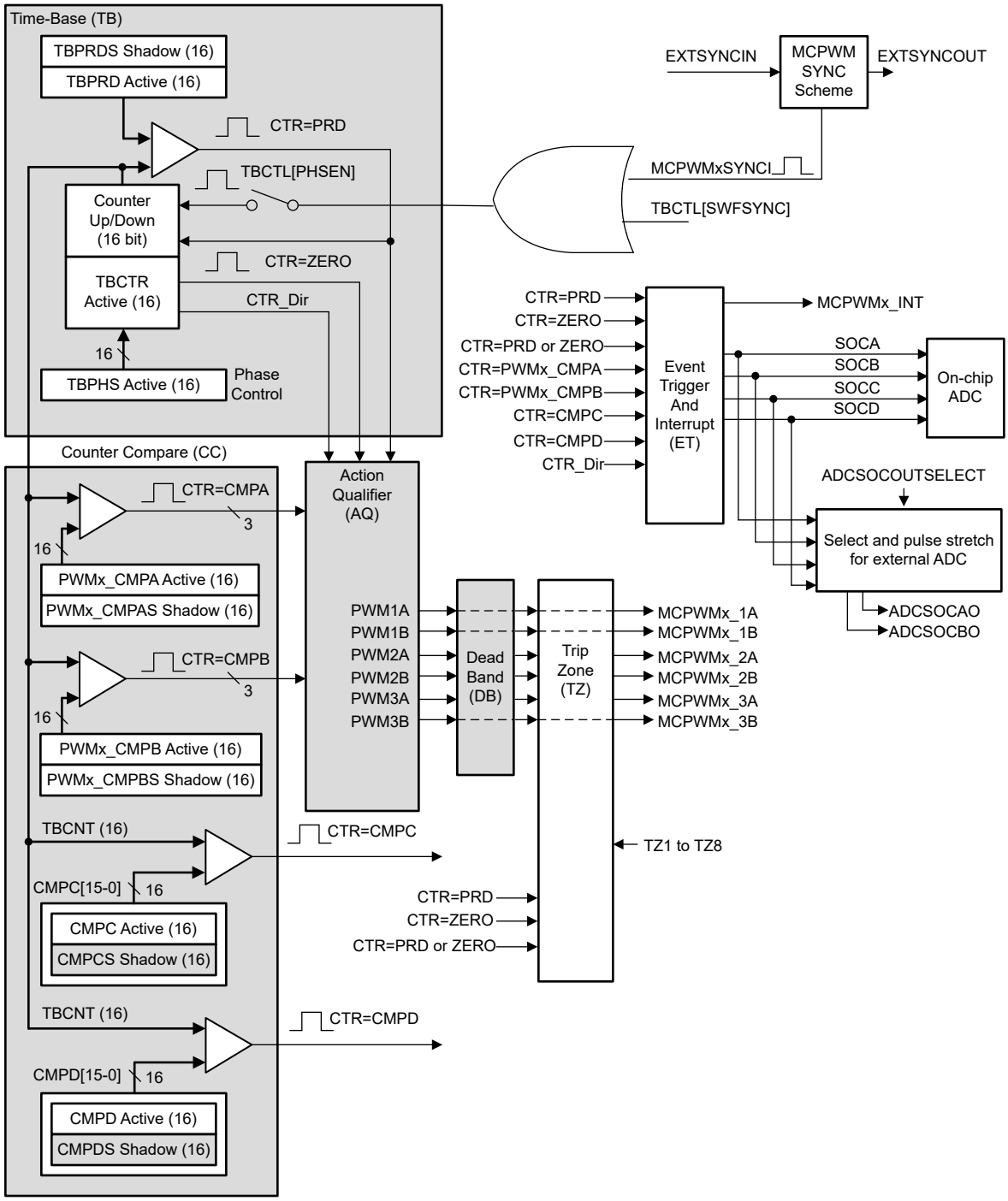


Figure 6-3. MCPWM Submodules and Critical Internal Signal Interconnects

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6.10.2 Control Peripherals Synchronization

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules. Figure 6-4 shows the synchronization scheme.

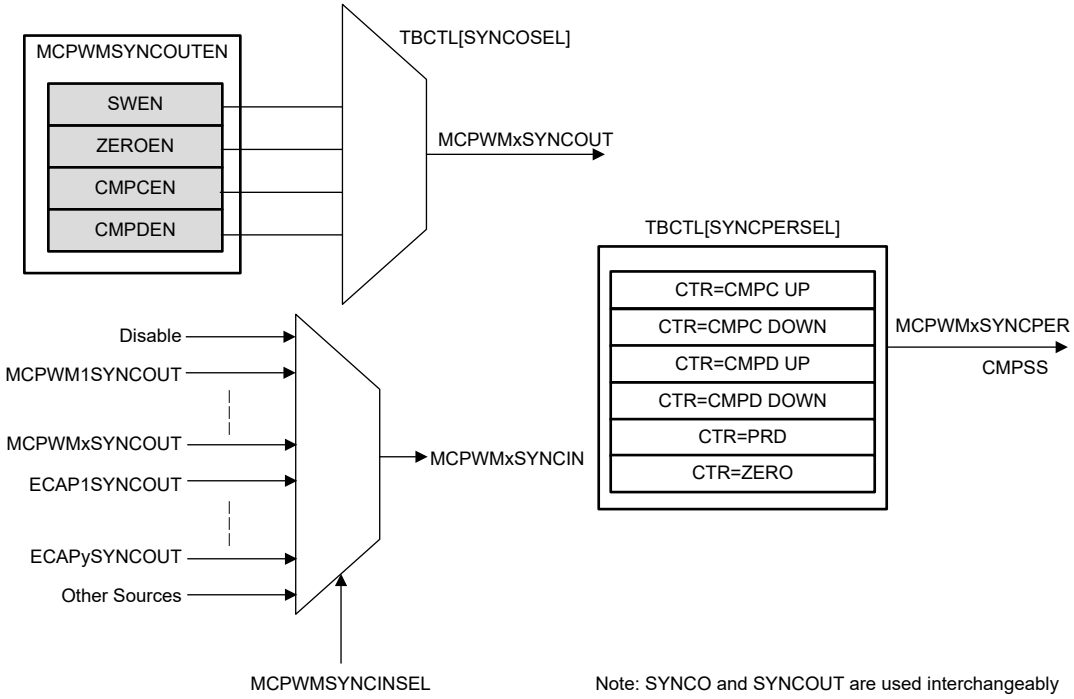


Figure 6-4. Synchronization Chain Architecture

6.10.3 MCPWM Electrical Data and Timing

6.10.3.1 MCPWM Timing Requirements

PARAMETER			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.10.3.2 MCPWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		30	ns
tskew	Skew of all MCPWM outputs (Shortest Path)(1)		5.1	ns
tskew	Skew of all MCPWM outputs (Longest Path)(1)		8.9	ns

(1) The MCPWMs have a similar configuration.

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6.10.4 Enhanced Capture eCAP

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this section include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCNTRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
  - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the *eCAP* section of the Enhanced Capture (eCAP) chapter in the TRM.
- EALLOW protection
  - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

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6.10.5 eCAP Block Diagram

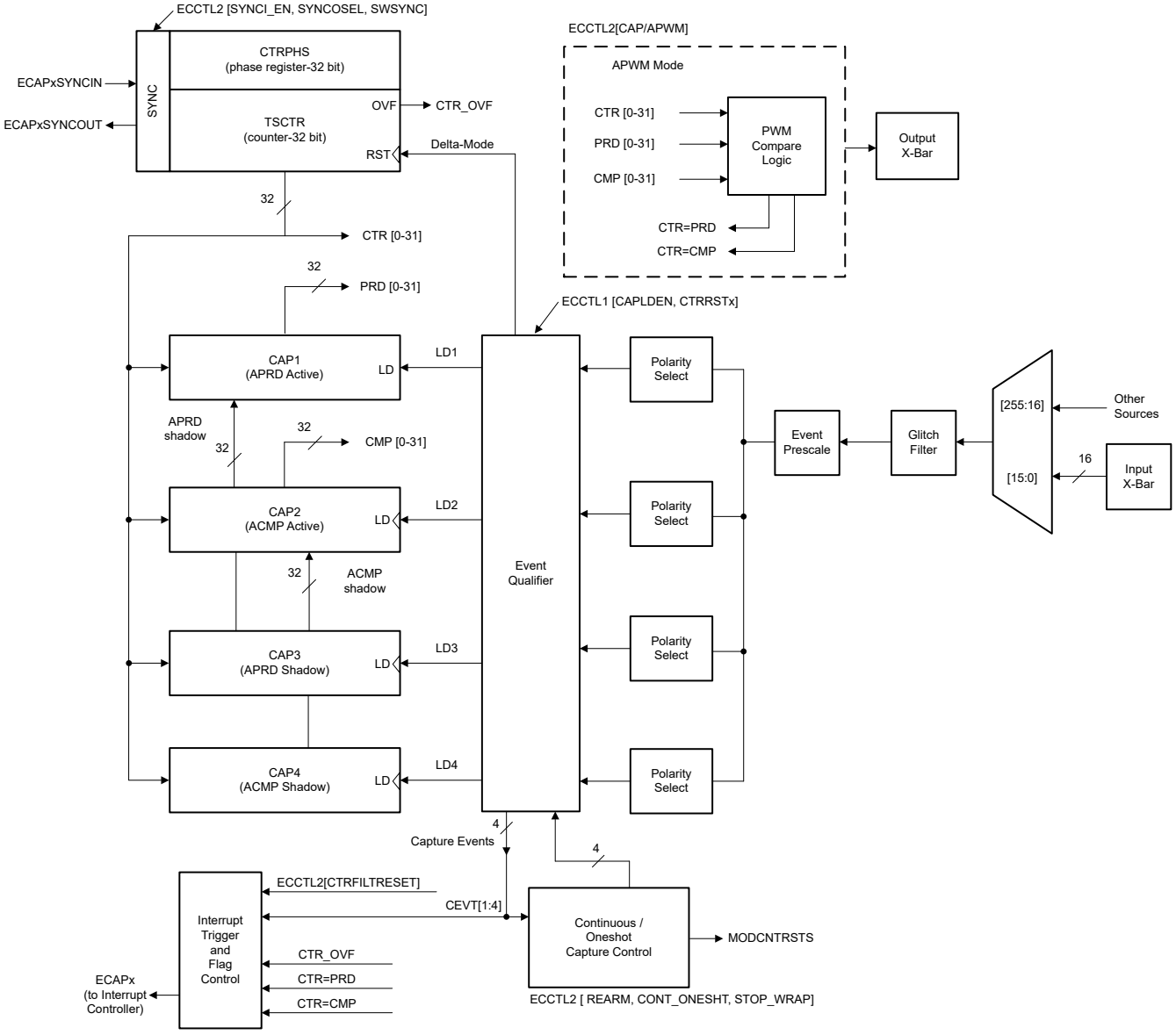


Figure 6-5. eCAP Block Diagram

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6.10.6 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from PWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in the diagram below.

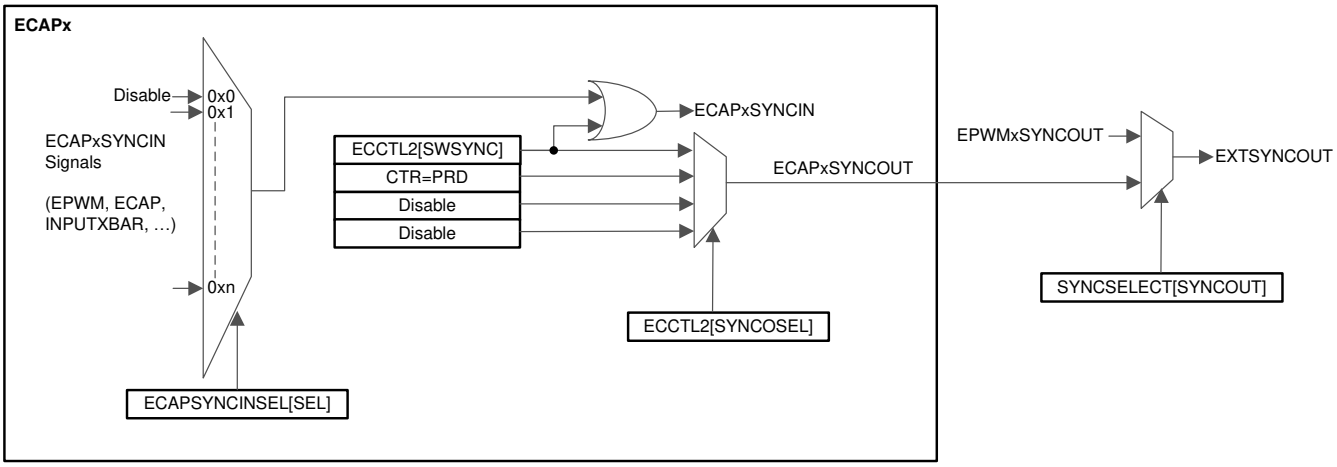


Figure 6-6. eCAP Synchronization Scheme

6.10.7 eCAP Electrical Data and Timing

6.10.7.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w_(IQSW)}$			

6.10.7.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

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6.10.8 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units:

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

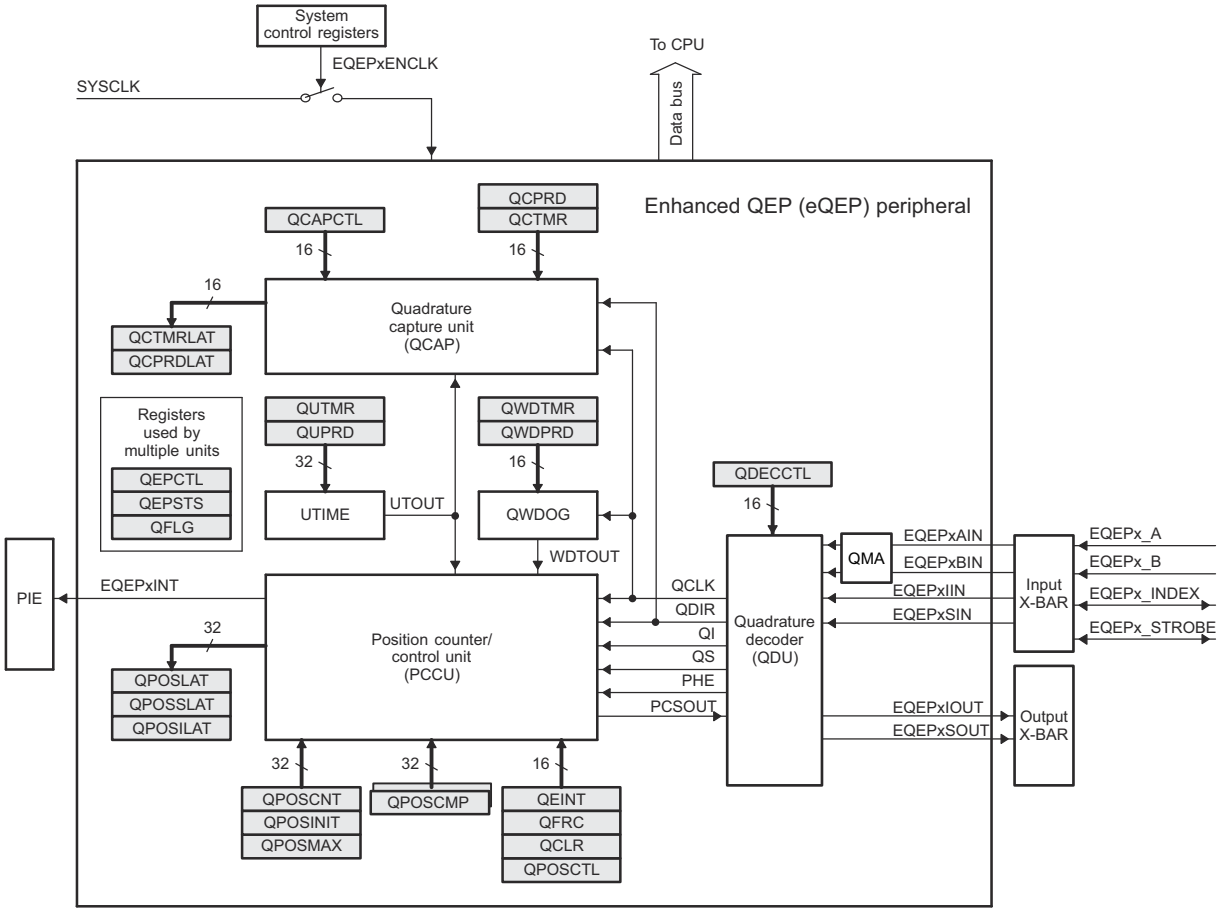


Figure 6-7. eQEP Block Diagram

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6.10.9 eQEP Electrical Data and Timing

6.10.9.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(QEPP)}$	QEP input period	Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.10.9.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

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6.11 Communication Peripherals

6.11.1 UNICOMM (UART/I²C/SPI)

UNICOMM is a highly flexible peripheral which can be configured to operate with a UART, SPI, I²C Controller or a I²C Target protocol at runtime. The user can select one of the serial interfaces during initialization. The peripheral uses shared 16-deep FIFOs in each UCx instance to maximize the device capability. A scalable peripheral group (SPG) combines one or more UNICOMM instances for special functions like inter-module internal loopback and I2C pairing. Table 6-4 describes the peripheral serial interfaces available on each UNICOMM instance and how these are grouped into SPG groupings on the device.

Table 6-4. UNICOMM (UCx) Serial Interface

SPG Instance	UNICOMM Instance	Supported Serial Protocols	Available Peripheral Types
SPG0 (PD1)	UC0	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC1	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC2	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target
SPG1 (PD1)	UC3	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC4	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC5	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target

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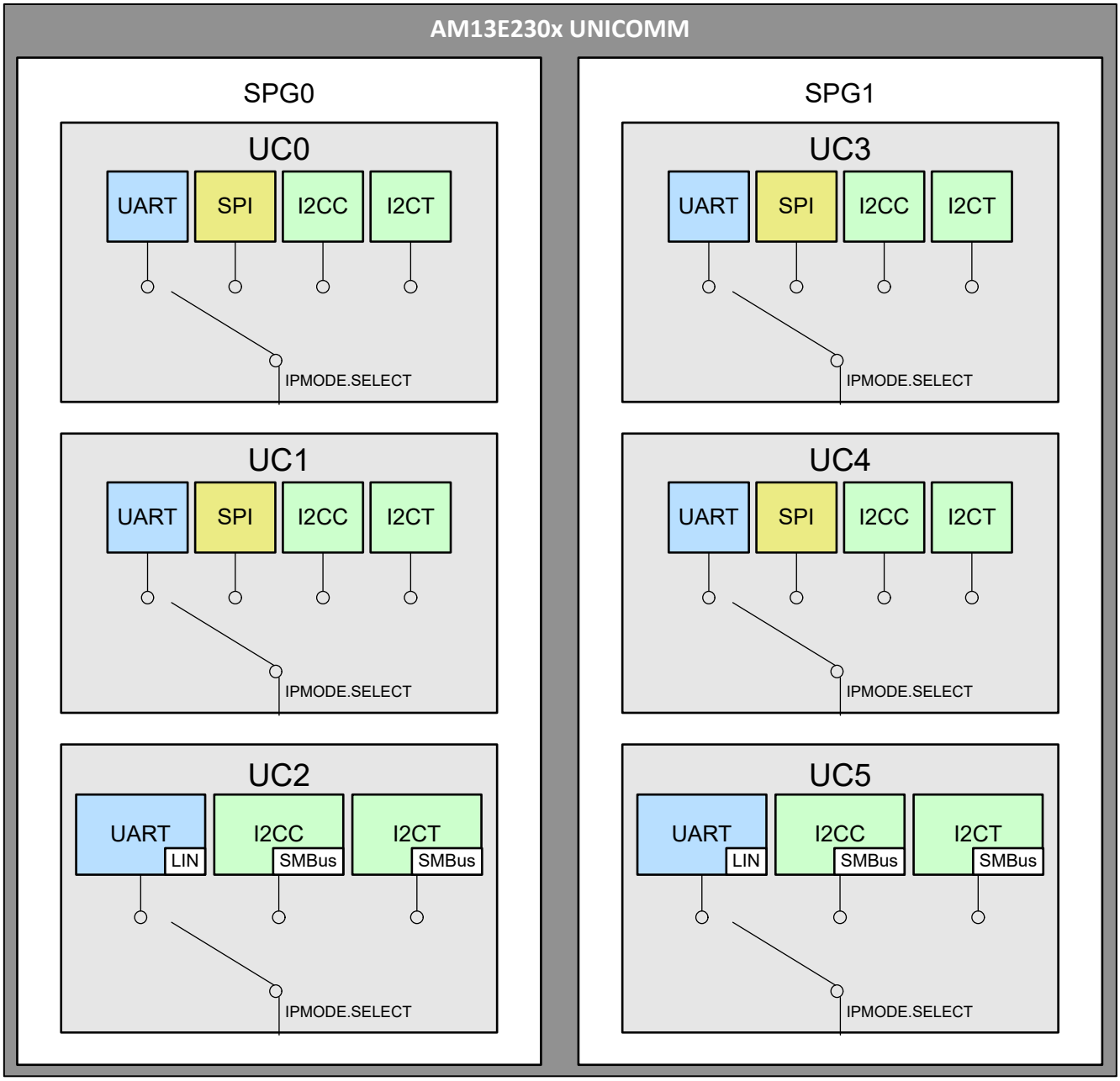


Figure 6-8. Unicomm Block Diagram

6.11.1.1 Universal Asychronous Receiver/Transmitter (UART)

The universal asychronous receiver/transmitter (UART) UNICOMM peripheral mode supports the following key features:

- Fully programmable serial interface:
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - LSB-first or MSB-first data transmit and receive
  - Line-break detection
  - Programmable baud-rate generation with oversampling by 16, 8 or 3

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- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support
- Local Interconnect Network (LIN) hardware support (Basic+ instances)
- Transmit to receive internal loopback mode operation
- Hardware Flow Control (CTS/RTS)
- RS485 Flow Control support
- Idle-line Multiprocessor Mode
- 9-Bit UART Mode
- ISO7816 Smartcard support (Basic instances)

See Table 6-5 for more detailed information on supported features for individual UCx instances.

Table 6-5. UART (UNICOMM) Features

Supported Features	Basic Instances: UC0.UART, UC1.UART, UC3.UART,UC4.UART	Basic+ Instances: UC2.UART, UC5.UART
Active in Stop and Standby Mode	Yes	Yes
Hardware Flow Control (CTS/RTS)	Yes	Yes
9-bit Mode	Yes	Yes
LIN Mode	No	Yes
ISO7816 Smart Card	Yes	No
DMA Access / Support	Yes	Yes
Internal Loopback Support	Yes	Yes
Idle-line Multiprocessor Mode	Yes	Yes
RS485 Flow Control Mode	Yes	Yes

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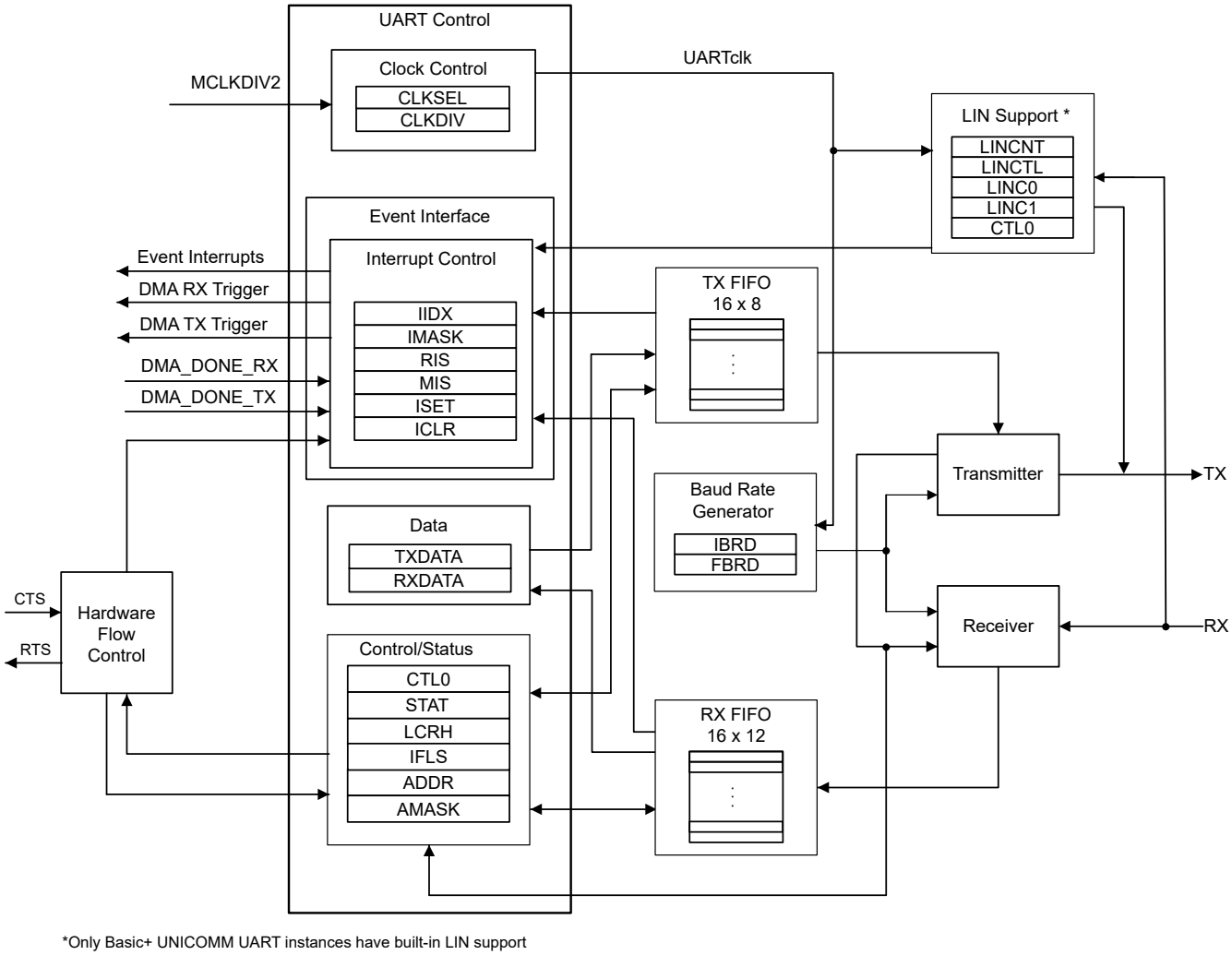


Figure 6-9. UART Functional Block Diagram

For more details, see the UART (UNICOMM) chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

6.11.1.1.1 UART Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			100	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			12.5	Mbps
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

6.11.1.2 Inter-Integrated Circuit (I2C)

The inter-intergrated circuit (I2C) UNICOMM peripheral modes (I2C Controller and I2C Target) support the following key features:

- 7-bit and 10-bit addressing modes

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- Dual Addressing Support
- Standard-mode (Sm) Support, with a bit rate up to 100 kbit/s
- Fast-mode (Fm) Support, with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) Support, with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support
- SMBus 3.0 Support
  - Packet Error Checking (PEC)
  - Timeout Detection
  - Enhanced Frame Acknowledgement: Manual or Automatic
  - Default Device/Host/Alert Response Address
  - Target Arbitration
- Analog and Digital Glitch Suppresion

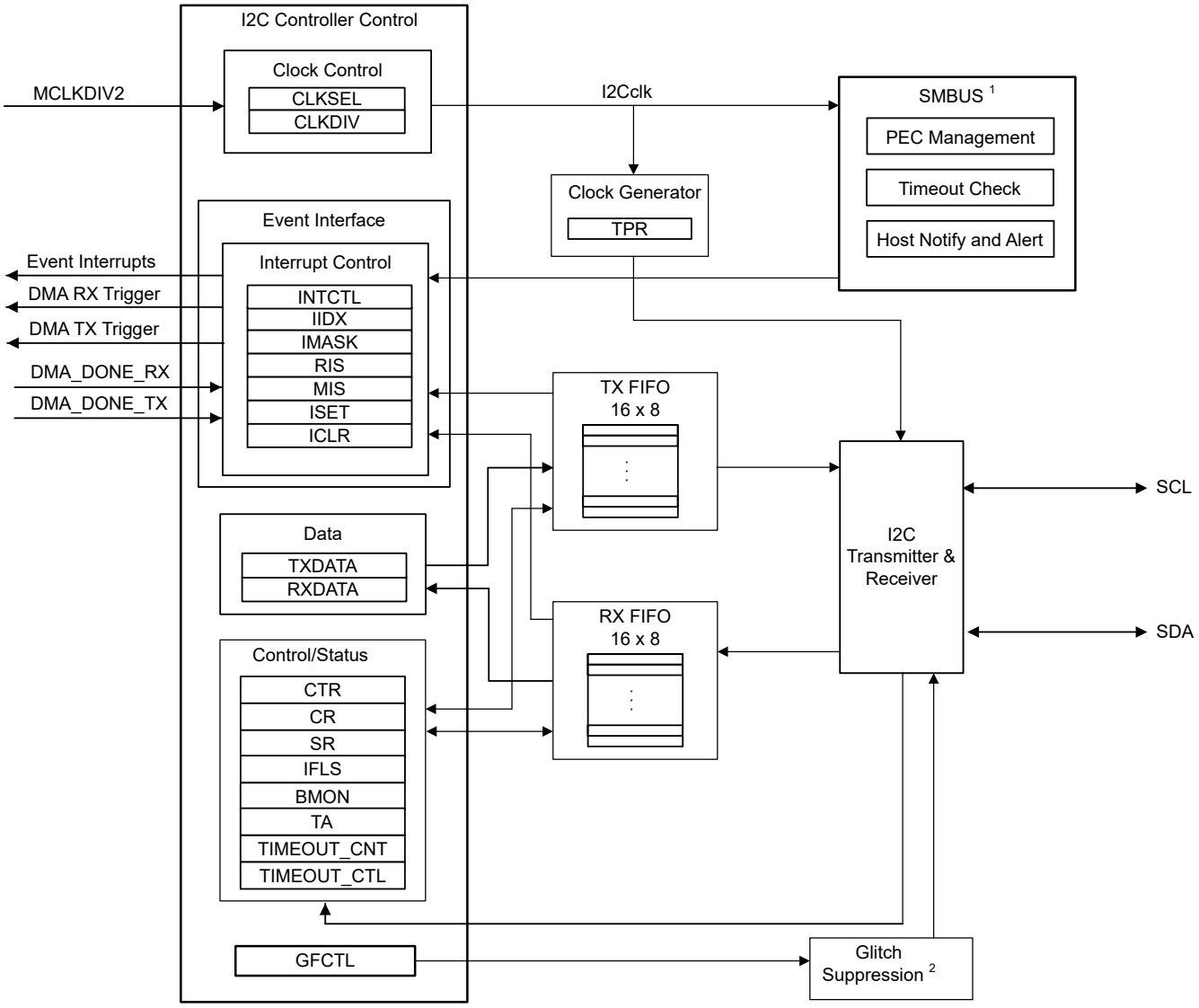
See Table 6-6 for more detailed information on supported features for individual UCx instances and I2C operating modes (I2C Controller and I2C Target).

Table 6-6. I2C Controller and Target (UNICOMM) Features

Supported Features	I2C Controllers		I2C Targets	
	Basic Instances: UC0.I2CC, UC1.I2CC, UC3.I2CC, UC4.I2CC	Advanced Instances: UC2.I2CC, UC5.I2CC	Basic Instances: UC0.I2CT, UC1.I2CT, UC3.I2CT, UC4.I2CT	Advanced Instances: UC2.I2CT, UC5.I2CT
Standard-mode (Sm) Support	Yes	Yes	Yes	Yes
Fast-mode (Fm) Support	Yes	Yes	Yes	Yes
Fast-mode Plus (Fm+) Support	Yes	Yes	Yes	Yes
Analog Glitch Filtering	No	Yes	No	Yes
Digital Glitch Filtering	Yes	No	Yes	No
Burst Mode	No	Yes	-	-
SMBus v3.0 Support	No	Yes		
Dual Addressing	-	-	No	Yes

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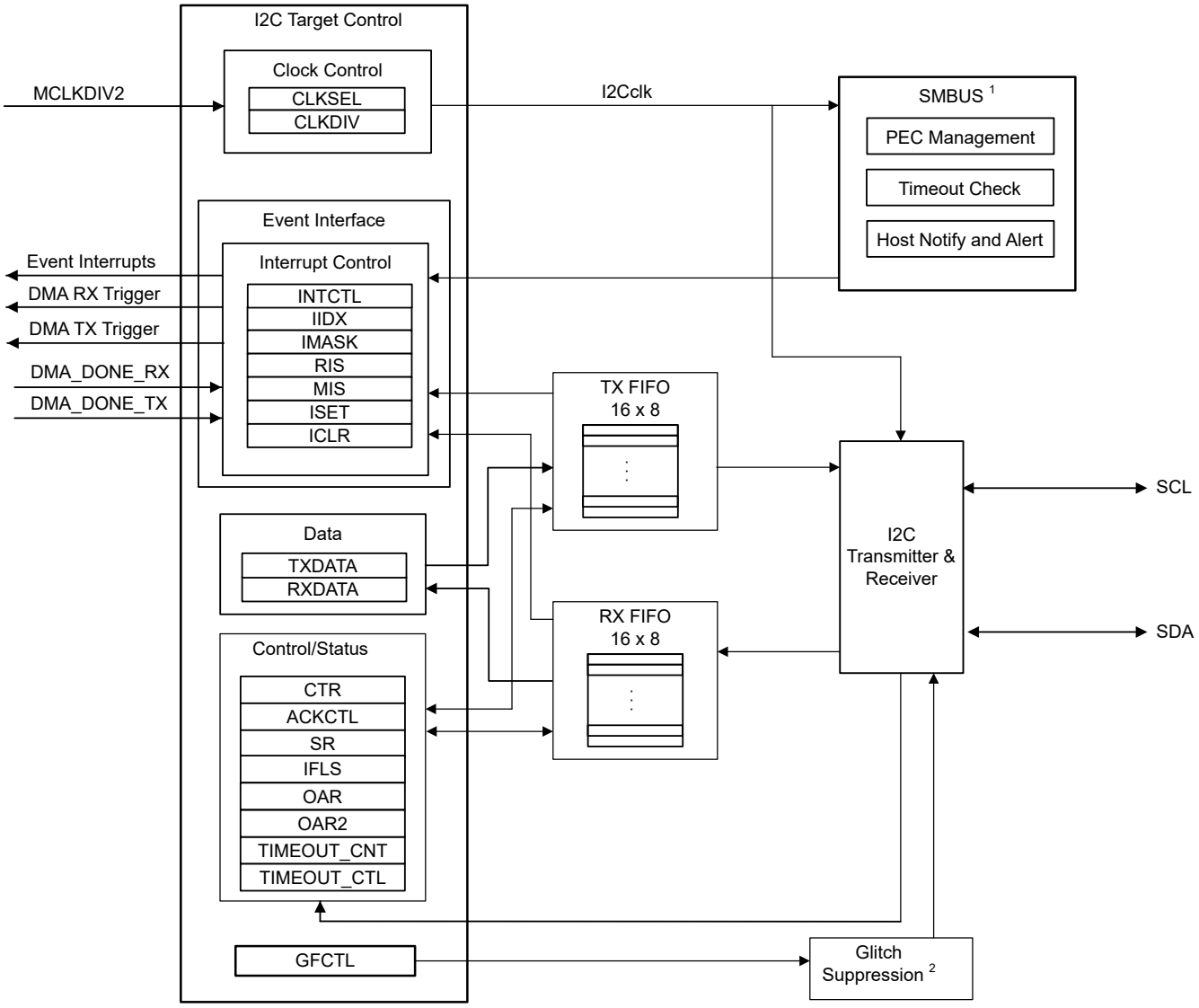
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[1] Only Advanced I2CC instances have built-in SMBUS support
[2] Basic I2CC instances have only digital glitch support and Advanced I2CC instances have only analog glitch support

Figure 6-10. I2C Controller (I2CC) Functional Block Diagram

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[1] Only Advanced I2CT instances have built-in SMBUS support
[2] Basic I2CT instances have only digital glitch support and Advanced I2CT instances have only analog glitch support

For more details, see the I2C (UNICOMM) chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

Figure 6-11. I2C Target (I2CT) Functional Block Diagram

6.11.1.2.1 I2C Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain1, , MCLK = 200MHz		100		100		100	MHz
		I2C in Power Domain1, , MCLK = 250MHz		125		125		125	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

6.11.1.2.2 I2C Filter Timings

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

6.11.1.2.3 I²C Timing Diagram

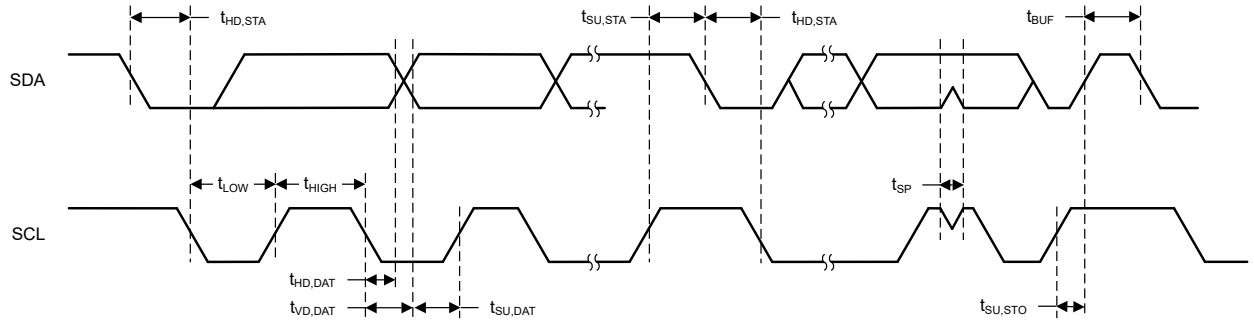


Figure 6-12. I2C Timing Diagram

6.11.1.3 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) UNICOMM peripheral mode supports the following key features:

- Supports up to 40 Mbits/s in both controller and peripheral mode [1]
- Controller or Peripheral Modes
- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support
- Single Parity for Transmit and Receive
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4-16 bits (controller mode) and 7-16 bits (peripheral mode)
- Texas Instruments Synchronous Serial and Motorola SPI Frame Format Support

[1] Only SPI signals on HSIO pins support data rates up to 40 Mbits/s; see the *Pin Diagrams* section for HSIO pins.

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All UCx instances with SPI peripheral mode available on this device (UC0.SPI, UC1.SPI, UC3.SPI, and UC4.SPI) support all of the above features.

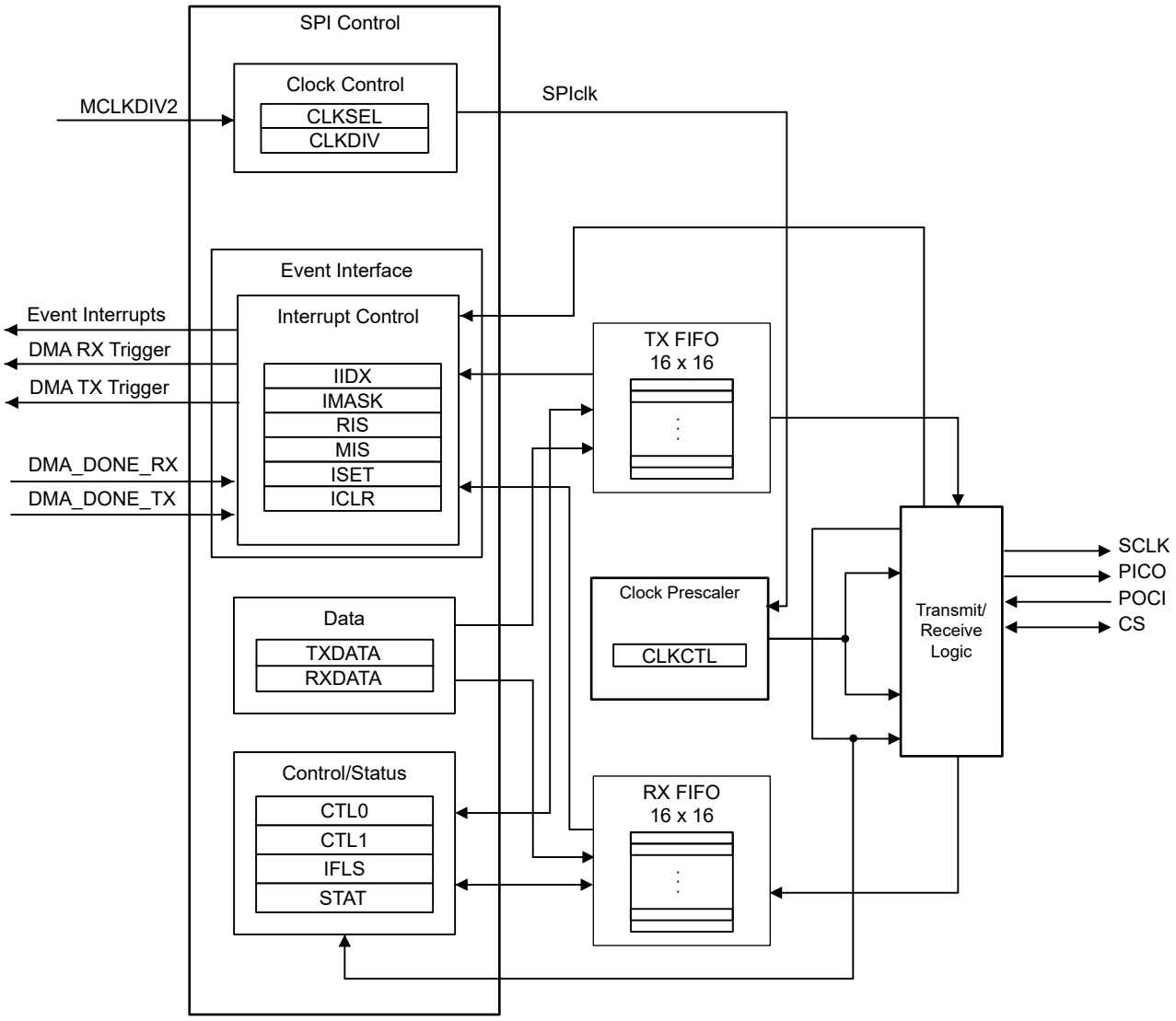


Figure 6-13. SPI Functional Block Diagram

For more details, see the SPI (UNICOMM) chapter of the *AM13E230x Microcontrollers Technical Reference Manual* s.

6.11.1.3.1 SPI Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	TYP	MAX	UNIT
SPI					
f_{SPI}	SPI clock frequency, MCLK = 200MHz			25	MHz
	SPI clock frequency, MCLK = 250MHz			31.25	MHz
DC_{SCK}	SCK Duty Cycle	40	50	60	%
Controller					
$t_{SCLK_H/L}$	SCLK High or Low time	(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock	1 SPI Clock - 3	1 SPI Clock		ns
		1/2 SPI Clock - 3	1/2 SPI Clock		ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	1 SPI Clock - 3	1 SPI Clock		ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out		1/2 SPI Clock	1/2 SPI Clock + 3	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance		1 SPI Clock	1 SPI Clock + 3	ns
$t_{SU.CI}$	POCI input data setup time (1)	1			ns
$t_{HD.CI}$	POCI input data hold time	20			ns
$t_{SU.CI}$	POCI input data setup time (1)	18			ns
$t_{HD.CI}$	POCI input data hold time	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)			3	ns
$t_{HD.CO}$	PICO output data hold time (3)	-3			ns
Peripheral					
$t_{CS.LEAD}$	CS lead-time, CS active to clock	19			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out			25	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance			39	ns
$t_{SU.PI}$	PICO input data setup time	7			ns
$t_{HD.PI}$	PICO input data hold time	0			ns
$t_{VALID.PO}$	POCI output data valid time(2)			19	ns
$t_{HD.PO}$	POCI output data hold time(3)	3			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

6.11.1.3.2 SPI Timing Diagram

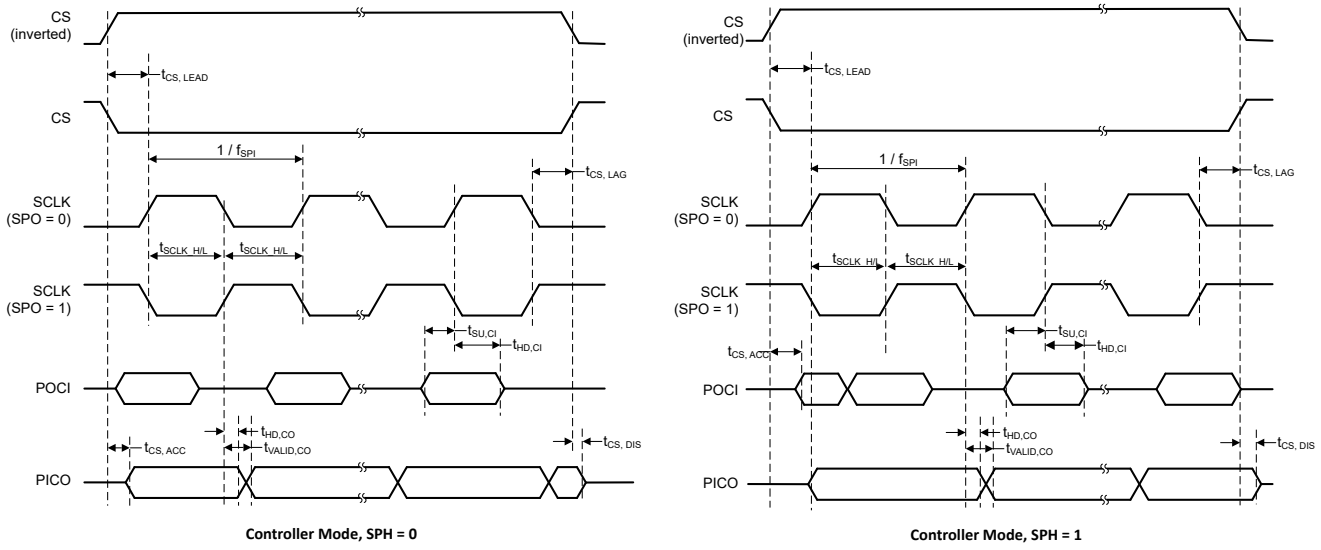


Figure 6-14. SPI Timing Diagram - Controller Mode

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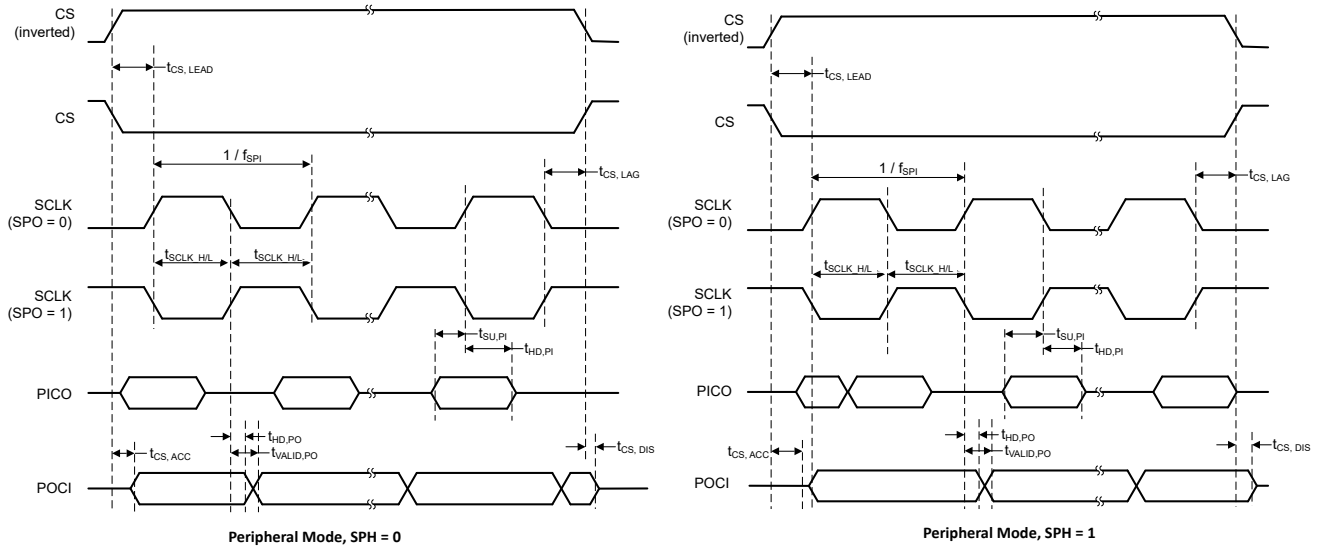


Figure 6-15. SPI Timing Diagram - Peripheral Mode

6.11.2 Modular Controller Area Network (MCAN)

The Modular Controller Area Network (MCAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 1-Mbps nominal bit rate, up to 8-Mbps data bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1KB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the Modular Controller Area Network (MCAN) chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

6.11.2.1 CAN Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CANCLK}	CAN input clock frequency	MCLK=250MHz			125	MHZ
		MCLK=200MHz			100	
f_{BAUD}	CAN Baud rate				8	Mbps

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6.12 External Peripheral Interface (EPI)

The external peripheral interface (EPI) is a high-speed parallel bus for external peripherals or memory. The module has several modes of operation to interface seamlessly to many types of external devices. The EPI is similar to a standard microprocessor address/data bus, except that it must typically be connected to just one type of external device. Enhanced capabilities include DMA support, clocking control and support for external FIFO buffers.

The EPI has the following features:

- 8/16/32-bit dedicated parallel bus for external peripherals and memory
- Memory interface supports contiguous memory access independent of data bus width, thus enabling code execution directly from SDRAM, SRAM and Flash memory
- Blocking and non-blocking reads
- Separates processor from timing details through use of an internal write FIFO
- Efficient transfers using Direct Memory Access (DMA) Controller
  - Separate channels for read and write
  - Read channel request asserted by programmable levels on the internal non-blocking read FIFO (NBRFIFO)
  - Write channel request asserted by empty on the internal write FIFO (WFIFO)

The EPI supports three primary functional modes: Synchronous Dynamic Random Access Memory (SDRAM) mode, Traditional Host-Bus mode, and General-Purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

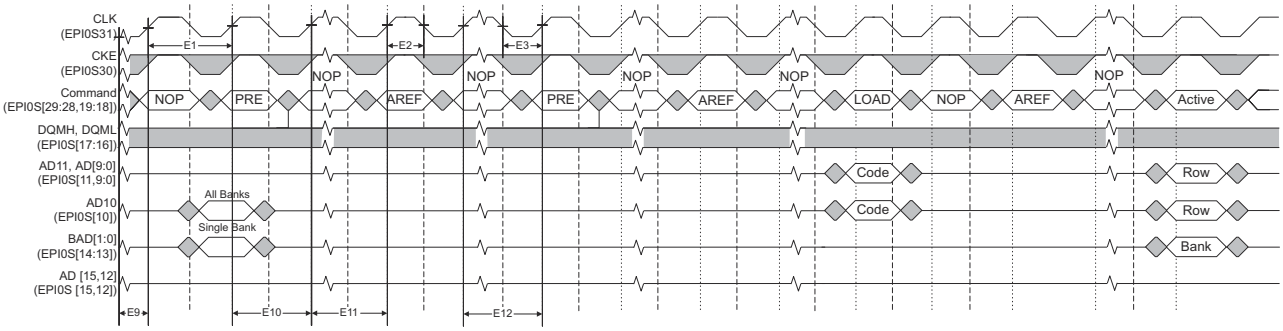
- Synchronous Dynamic Random Access Memory (SDRAM)
  - Supports x16 (single data rate) SDRAM at up to 50MHz
  - Supports low-cost SDRAMs up to 64 MB (512 megabits)
  - Includes automatic refresh and access to all banks/rows
  - Includes a Sleep/Standby mode to keep contents active with minimal power draw
  - Multiplexed address/data interface for reduced pin count
- Host-bus
  - Traditional x8 and x16 MCU bus interface capabilities
  - Similar device compatibility options as PIC, ATmega, 8051, and others
  - Access to SRAM, NOR Flash memory, and other devices, with up to 1 MB of addressing in non-multiplexed mode and 256 MB in multiplexed mode (512 MB in Host-Bus 16 mode with no byte selects)
  - Support of both muxed and de-muxed address and data
  - Access to a range of devices supporting the non-address FIFO x8 and x16 interface variant, with support for external FIFO (XFIFO) EMPTY and FULL signals
  - Speed controlled, with read and write data wait-state counters
  - Support for read/write burst mode to Host Bus
  - Multiple chip select modes including single, dual, and quad chip selects, with and without ALE
  - External iRDY signal provided for stall capability of reads and writes
  - Manual chip-enable (or use extra address pins)
- General Purpose
  - Wide parallel interfaces for fast communications with CPLDs and FPGAs
  - Data widths up to 32 bits
  - Data rates up to 125 MB/second
  - Optional "address" sizes from 4 bits to 20 bits
  - Optional clock output, read/write strobes, framing (with counter-based size), and clock-enable input
- General parallel GPIO
  - 1 to 32 bits, FIFOed with speed control
  - Useful for custom peripherals or for digital data acquisition and actuator controls

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6.12.1 EPI SDRAM Interface Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
NO.	PARAMETER		MIN	TYP	MAX	UNIT
E1	$t_{c(CK)}$	Cycle time, SDRAM clock	19	20	21	ns
E2	$t_{w(CKH)}$	Pulse duration, SDRAM clock high	9	10	11	ns
E3	$t_{w(CKL)}$	Pulse duration, SDRAM clock low	9	10	11	ns
E4	$t_{d(CK-OV)}$	Delay time, clock to output valid	–5		5	ns
E5	$t_{d(CK-OIV)}$	Delay time, clock to output invalid	–5		5	ns
E6	$t_{d(CK-OZ)}$	Delay time, clock to output high-impedance	–5		5	ns
E7	$t_{su(AD-CK)}$	Setup time, input before clock	12			ns
E8	$t_{h(CK-AD)}$	Hold time, input after clock	0			ns
E9	t_{PU}	Power-up time	100			µs
E10	t_{pc}	Precharge time, all banks	20			ns
E11	t_{rf}	Autorefresh	66			ns
E12	t_{MRD}	Program mode register	40			ns

6.12.2 EPI SDRAM Timing Diagram



A. If $\overline{CS}$ is high at clock high time, all applied commands are NOP.
B. The Mode register may be loaded before the autorefresh cycles if desired.
C. JEDEC and PC100 specify three clocks.
D. Outputs are ensured High-Z after command is issued.

Figure 6-16. SDRAM Initialization and Load Mode Register Timing

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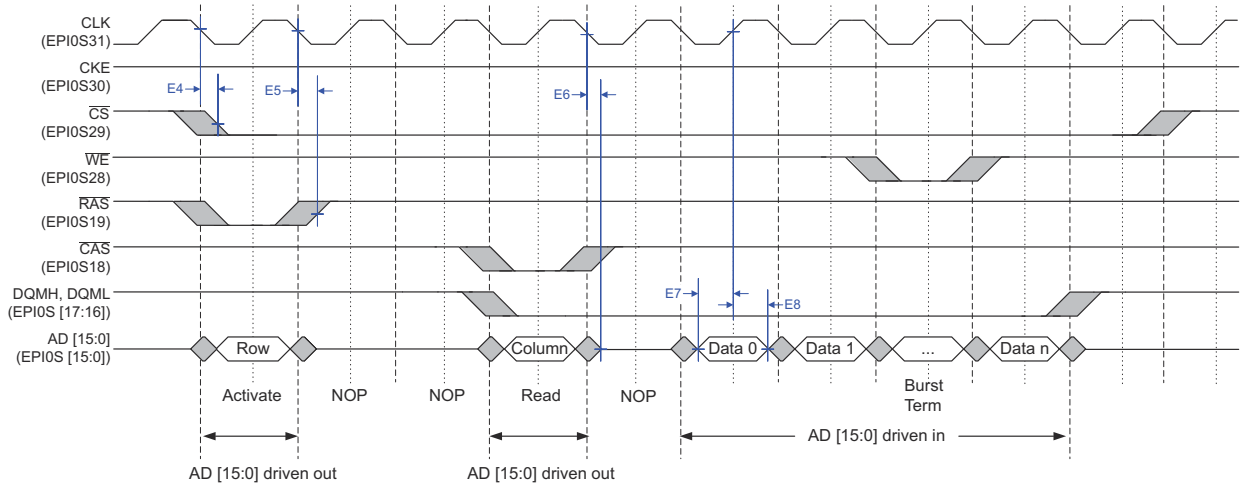


Figure 6-17. SDRAM Read Timing

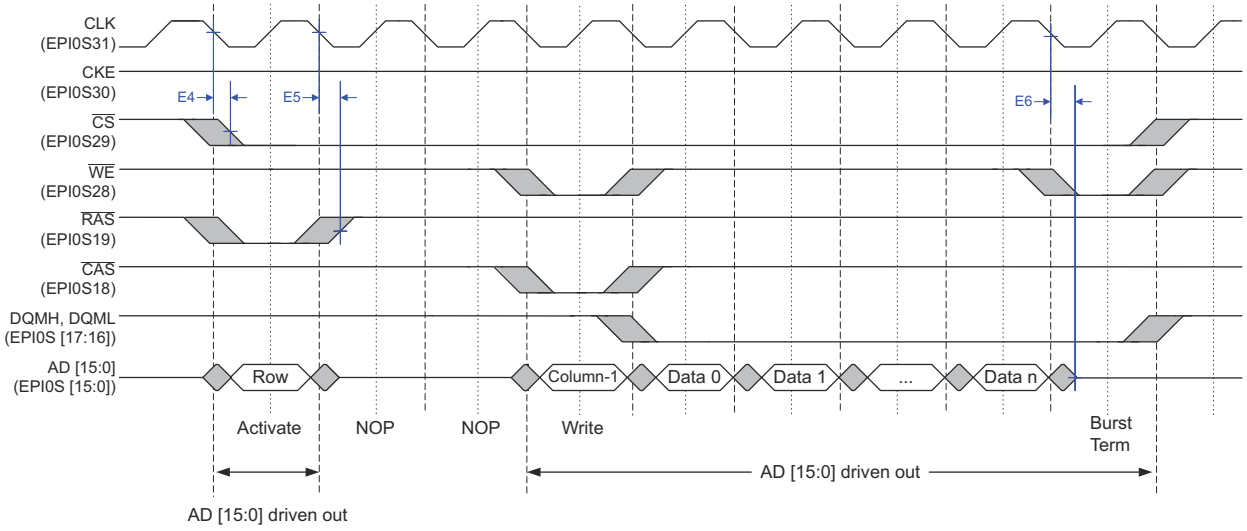


Figure 6-18. SDRAM Write Timing

6.12.3 EPI Host-Bus 8 and Host-Bus 16 Interface Switching Characteristics

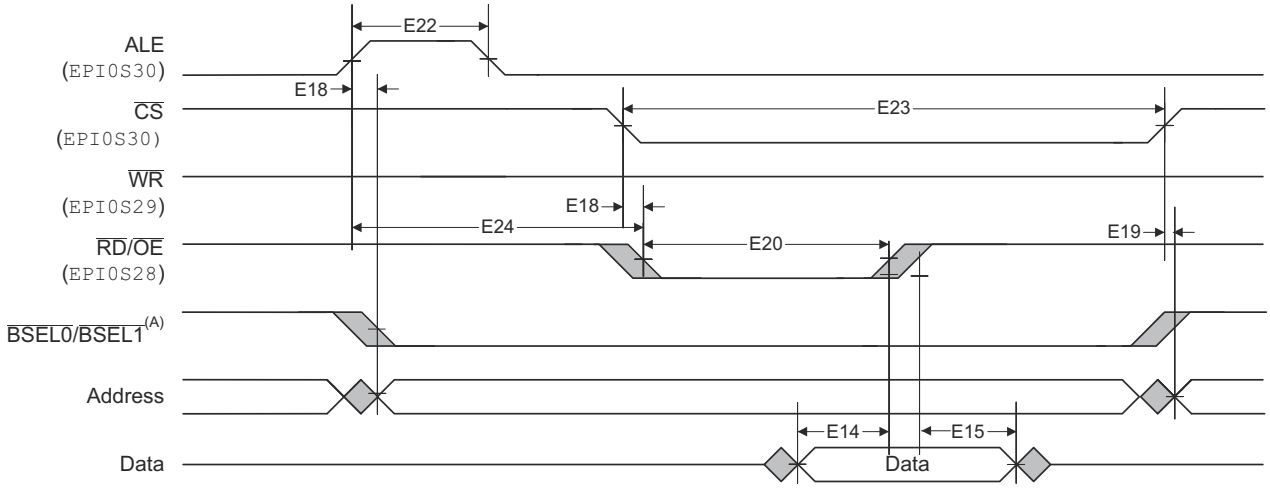
NO.	PARAMETER		MIN	TYP	MAX	UNIT
E16	td(WR-WDATAV)	Delay time, WR to write data valid			5	ns
E17	td(WRIV-DATA)	Delay time, WR invalid to data	2*E - 2	2*E		ns
E18	td(CS-OV)	Delay time, CS to output valid	–5		5	ns
E19	td(CS-OIV)	Delay time, CS to output invalid	–5		5	ns
E20	tw(STL)	Pulse duration, WR/ RD strobe low	2*E - 2	2*E		ns
E22	tw(ALEH)	Pulse duration, ALE high	1*E - 2	1*E		ns
E23	tw(CSL)	Pulse duration, CS low	4*E - 2	4*E		ns
E24	td(ALE-ST)	Delay time, ALE rising to WR/ RD strobe falling	2*E - 2	2*E		ns

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6.12.4 EPI Host-Bus 8 and Host-Bus 16 Interface Timing Requirements

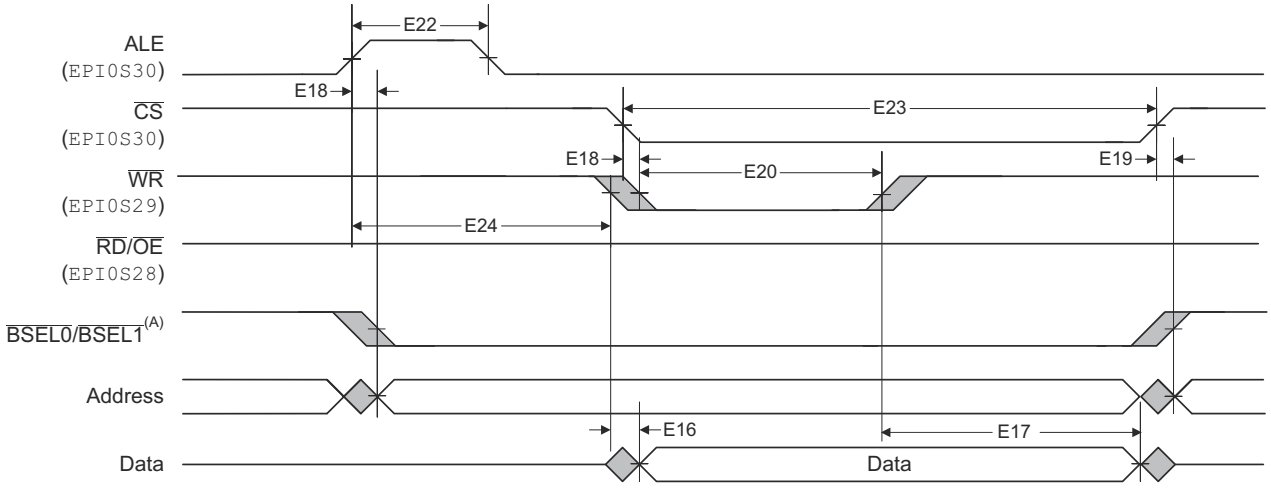
NO	PARAMETER		MIN	MAX	UNIT
E14	tsu(RDATA)	Setup time, read data	12		ns
E15	th(RDATA)	Hold time, read data	0		ns

6.12.5 EPI Host-Bus 8/16 Mode Timing Diagram



A. $\overline{BSEL0}$ and $\overline{BSEL1}$ are available in Host-Bus 16 mode only.

Figure 6-19. Host-Bus 8/16 Mode Read Timing



A. $\overline{BSEL0}$ and $\overline{BSEL1}$ are available in Host-Bus 16 mode only.

Figure 6-20. Host-Bus 8/16 Mode Write Timing

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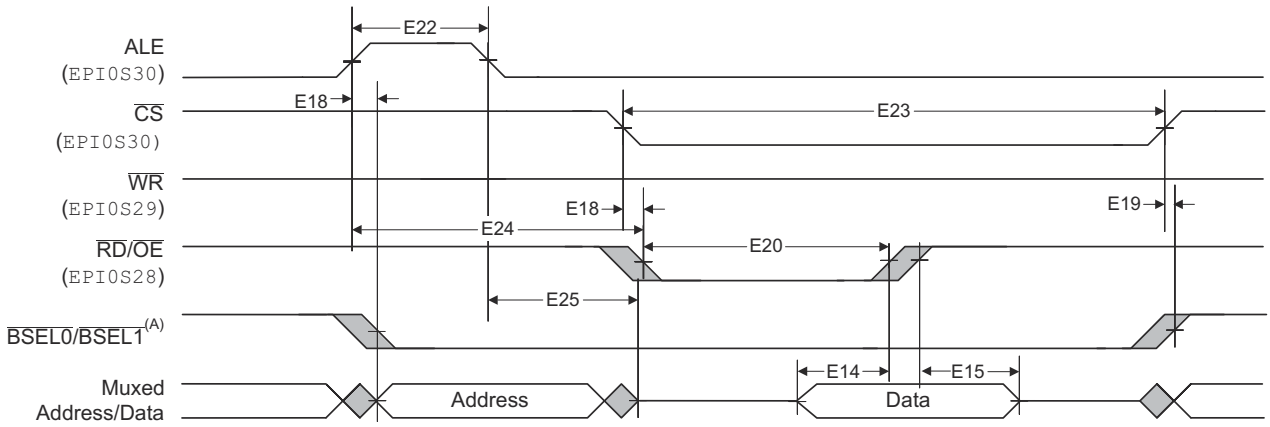


Figure 6-21. Host-Bus 8/16 Mode Muxed Read Timing

6.12.6 EPI General-Purpose Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
E26	tw(CKH)	Pulse duration, general-purpose clock high	10		ns
E27	tw(CKL)	Pulse duration, general-purpose clock low	10		ns
E30	td(CK-OV)	Delay time, falling clock edge to output valid	–5	5	ns
E31	td(CK-OIV)	Delay time, falling clock edge to output invalid	–5	5	ns
E33	tc(CK)	Cycle time, general-purpose clock	20		ns

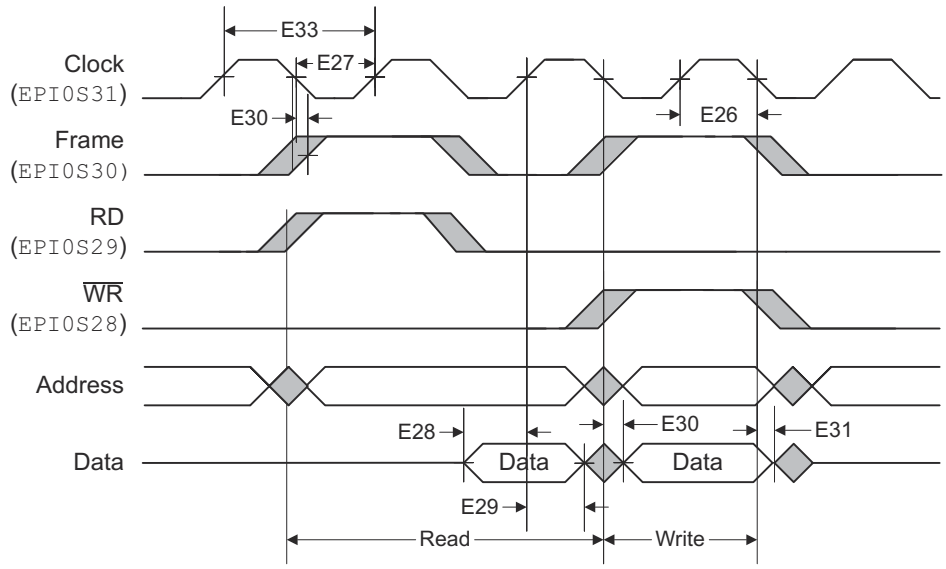
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6.12.7 EPI General-Purpose Interface Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
E28	tsu(IN-CK)	Setup time, input signal before rising clock edge	12		ns
E29	th(CK-IN)	Hold time, input signal after rising clock edge	0		ns
E32	tsu(IRDY-CK)	Setup time, iRDY assertion or deassertion before falling clock edge	12		ns

6.12.8 EPI General-Purpose Mode Timing Diagram



A. This figure illustrates accesses where the FRM50 bit is clear, the FRMCNT field is 0x0, the RD2CYC bit is clear, and the WR2CYC bit is clear.

Figure 6-22. General-Purpose Mode Read and Write Timing

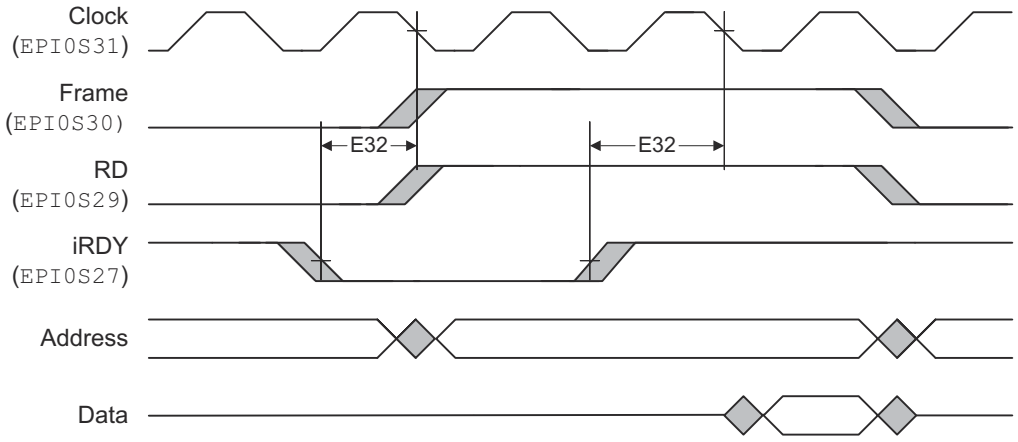


Figure 6-23. General-Purpose Mode iRDY Timing

6.13 Emulation and Debug

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6.13.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz
t_{setup}	SWDIO setup time		1.5			ns
t_{hold}	SWDIO hold time		1.6			ns
t_{ovalid}	SWDIO output valid time				15.5	ns
t_{ohold}	SWDIO output hold time		5			ns

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7 Detailed Description

7.1 Overview

The AM13E230x series of microcontrollers (MCUs) are cost-optimized 32-bit devices built for complex real-time control applications such as motor control. AM13E230x MCUs include a high-performance Arm® Cortex®-M33 core operating at up to 200MHz or 250MHz with a proprietary math accelerator for trigonometric operations (TMU) through a Custom Datapath Extension (CDE) and a TinyEngineTM Neural-network Processing Unit (NPU) Artificial Intelligence (AI) Engine to enable simultaneous motor control and AI model execution. Its rich analog integration offers industry-leading speed, precision, and reduced system cost. The digital peripherals offered on AM13E230x MCUs are specifically designed for motor control applications, and include tailored communications interfaces for appliance and industrial motor drive end equipment.

The AM13E230x series of microcontrollers (MCUs) provides up to 512KB of embedded flash program memory (2 banks of 256KB) with built-in error correction code (ECC) and up to 128KB SRAM (4 banks of 32KB) with hardware parity.

The AM13E230x series of microcontrollers (MCUs) offers a range of options in various memory, peripheral, and package configurations, enabling customers to find the most fitting solution that meets their specific project needs. The AM13E230x MCU platform combines the Arm® Cortex®-M33 platform with a holistic low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

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7.2 Memory

7.2.1 Memory Map

Table 7-1. Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
Flash Bank 0	256K x 16	0x0000 0000	0x0003 FFFF	ECC	Yes	Yes (2)
Flash Bank 1	256K x 16	0x0004 0000	0x0007 FFFF	ECC	Yes	Yes (2)
ROM(1)	48K x 16	0x0100 0000	0x0100 BFFF	Parity	No	No
SRAM0	32K x 16	0x2000 0000	0x2000 7FFF	Parity	Yes	Yes(2)
SRAM1	32K x 16	0x2000 8000	0x2000 FFFF	Parity	Yes	Yes (2)
SRAM2	32K x 16	0x2001 0000	0x2001 7FFF	Parity	Yes	Yes (2)
SRAM3	32K x 16	0x2001 8000	0x2001 FFFF	Parity	Yes	Yes (2)

(1) ROM is for TI internal use only.
(2) Global Security Controller (GSC) based secure.

7.2.2 Peripheral Registers Memory Map

Table 7-2. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address
MCLK/2 Domain		
EPI_REGS_GPCFG, EPI_REGS_SDRAMCFG, EPI_REGS_HB8CFG, EPI_REGS_HB16CFG	EPI0_BASE, EPI0SDRAM_BASE, PI0HB8_BASE, EPI0HB16_BASE	0x4001_A000
PGA_REGS	PGA0_BASE	0x400F_C000
PGA_REGS	PGA1_BASE	0x400F_D000
PGA_REGS	PGA2_BASE	0x400F_E000
MCAN_REGS	MCAN0_BASE	0x4011_0000
TIMG4_REGS	TIMG4_BASE	0x4018_0000
TIMG12_REGS	TIMG12_BASE	0x4018_8000
AES_REGS	AES_BASE	0x401B_0000
CRCP_REGS	CRC_BASE	0x401B_2000
KEYSTORE_REGS	KEYSTORE_BASE	0x401B_6000
UNICOMMUART_REGS	UC0_UART_BASE	0x4060_0000
UNICOMMUART_REGS	UC1_UART_BASE	0x4060_1000
UNICOMMUART_REGS	UC2_UART_BASE	0x4060_2000
UNICOMMI2CC_REGS	UC0_I2CC_BASE	0x4060_8000
UNICOMMI2CC_REGS	UC1_I2CC_BASE	0x4060_9000
UNICOMMI2CC_REGS	UC2_I2CC_BASE	0x4060_A000
UNICOMMI2CT_REGS	UC0_I2CT_BASE	0x4061_0000
UNICOMMI2CT_REGS	UC1_I2CT_BASE	0x4061_1000
UNICOMMI2CT_REGS	UC2_I2CT_BASE	0x4061_2000
UNICOMMSPI_REGS	UC0_SPI_BASE	0x4061_8000
UNICOMMSPI_REGS	UC1_SPI_BASE	0x4061_9000
UNICOMM_REGS	UNICOMM0_BASE	0x4063_0000
UNICOMM_REGS	UNICOMM1_BASE	0x4063_2000
UNICOMM_REGS	UNICOMM2_BASE	0x4063_4000
SPG_REGS	SPG0_BASE	0x4063_F000
UNICOMMUART_REGS	UC3_UART_BASE	0x4064_0000
UNICOMMUART_REGS	UC4_UART_BASE	0x4064_1000
UNICOMMUART_REGS	UC5_UART_BASE	0x4064_2000
UNICOMMI2CC_REGS	UC3_I2CC_BASE	0x4064_8000
UNICOMMI2CC_REGS	UC4_I2CC_BASE	0x4064_9000

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Table 7-2. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
UNICOMMI2CC_REGS	UC5_I2CC_BASE	0x4064_A000
UNICOMMI2CT_REGS	UC3_I2CT_BASE	0x4065_0000
UNICOMMI2CT_REGS	UC4_I2CT_BASE	0x4065_1000
UNICOMMI2CT_REGS	UC5_I2CT_BASE	0x4065_2000
UNICOMMSPI_REGS	UC3_SPI_BASE	0x4065_8000
UNICOMMSPI_REGS	UC4_SPI_BASE	0x4065_9000
UNICOMM_REGS	UNICOMM3_BASE	0x4067_0000
UNICOMM_REGS	UNICOMM4_BASE	0x4067_2000
UNICOMM_REGS	UNICOMM5_BASE	0x4067_4000
SPG_REGS	SPG1_BASE	0x4067_F000
MCLK/1 Domain		
ADC_LITE_REGS	ADC0_BASE	0x4000_0000
ADC_LITE_REGS	ADC1_BASE	0x4000_2000
ADC_LITE_REGS	ADC2_BASE	0x4000_4000
ADC_LITE_RESULT_REGS	ADC0RESULT_BASE	0x4000_A000
ADC_LITE_RESULT_REGS	ADC1RESULT_BASE	0x4000_B000
ADC_LITE_RESULT_REGS	ADC2RESULT_BASE	0x4000_C000
MCPWM_6CH_REGS	MCPWM0_BASE	0x4001_0000
MCPWM_6CH_REGS	MCPWM1_BASE	0x4001_1000
MCPWM_6CH_REGS	MCPWM2_BASE	0x4001_2000
MCPWM_6CH_REGS	MCPWM3_BASE	0x4001_3000
MCPWM_6CH_REGS	MCPWM4_BASE	0x4001_4000
DMA_REGS	DMA0_BASE	0x4002_0000
FLASH_CTRL_REGS	FLASH_BASE	0x4002_8000
MEM_CFG_REGS	MEMCFG_BASE	0x4002_A000
EAM_REGS	EAM_BASE	0x4002_C000
ECAP_REGS	ECAP0_BASE	0x4044_0000
ECAP_REGS	ECAP1_BASE	0x4044_1000
EQEP_REGS	EQEP0_BASE	0x4044_8000
EQEP_REGS	EQEP1_BASE	0x4044_9000
EQEP_REGS	EQEP2_BASE	0x4044_A000
CMPSS_LITE_REGS	CMPSS0_BASE	0x4046_0000
CMPSS_LITE_REGS	CMPSS1_BASE	0x4046_1000
CMPSS_LITE_REGS	CMPSS2_BASE	0x4046_2000
CMPSS_LITE_REGS	CMPSS3_BASE	0x4046_3000
INPUT_XBAR_REGS	INPUTXBAR_BASE	0x4046_8000
EPWM_XBAR_REGS	PWMXBAR_BASE	0x4046_9000
OUTPUTXBAR_REGS	OUTPUTXBAR_BASE	0x4046_A000
SYNC_SOC_REGS	SYNC_BASE	0x4046_B000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR0_FLAGS_BASE	0x4047_0000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR1_FLAGS_BASE	0x4047_1000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR2_FLAGS_BASE	0x4047_2000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR3_FLAGS_BASE	0x4047_3000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR4_FLAGS_BASE	0x4047_4000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR5_FLAGS_BASE	0x4047_5000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR6_FLAGS_BASE	0x4047_6000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR7_FLAGS_BASE	0x4047_7000
INPUT_FLAG_XBAR_REGS	INPUTXBAR_FLAGS_BASE	0x4049_0000
Power Domain 0 (Always ON)		
SYSCTL_REGS	SYSCTL_BASE	0x400A_F000

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Table 7-2. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
DEBUGSS_REGS	DEBUGSS_BASE	0x400C_7000
IOMUX_REGS	IOMUX_BASE	0x400C_C000
WWDT_REGS	WWDT_BASE	0x400D_0000
GPIO_REGS	GPIO0_BASE	0x400F_0000
GPIO_REGS	GPIO1_BASE	0x400F_2000
GPIO_REGS	GPIO2_BASE	0x400F_4000
GPIO_REGS	GPIO3_BASE	0x400F_6000
MCLK/4 Domain		
NVMNW_REGS	NVMNW_BASE	0x4004_2000
GSC_REGS	GSC_BASE	0x4004_6000

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7.2.3 Static RAM

The CPU subsystem has a dedicated static RAM block with hardware parity, with up to 128KB of SRAM.

7.2.4 Flash Memory

On the AM13E230x microcontrollers, two flash banks of up to 256KB each are available. Each Flash bank is made up of 2KB physical sectors. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

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7.3 Identification

All devices include a memory-mapped **FACTORY region** which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to the *Factory Constants* chapter of the *AM13E230x Microcontrollers Technical Reference Manual* for more information.

Table 7-3 lists DEVICEID register, its address is 0x60111004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Table 7-3. DEVICEID Register

Device	PARTNUM	MANUFACTURER
AM13E23019	0x0BBE	0x17
AM13E23018		
AM13E23017		

Table 7-4 USERID register, its address is 0x60111008, PART is bit 0 to 15, VARIANT is bit 16 to 23.

Table 7-4. USERID Register

OPN	USERID.PART	USERID.VARIANT
AM13E23019GTPDTR	0x5377	0x01
AM13E23019GTPZR	0x5377	0x02
AM13E23019GTPNR	0x5377	0x03
AM13E23019GTPMR	0x5377	0x04
AM13E23019GTPTR	0x5377	0x05
AM13E23019GTRGZR	0x5377	0x06
AM13E23019HTPZR	0x5377	0x07
AM13E23019HTPMR	0x5377	0x08
AM13E23018GTPDTR	0x6174	0x09
AM13E23018GTPZR	0x6174	0x0A
AM13E23018GTPNR	0x6174	0x0B
AM13E23018GTPMR	0x6174	0x0C
AM13E23018GTPTR	0x6174	0x0D
AM13E23018GTRGZR	0x6174	0x0E
AM13E23018HTPZR	0x6174	0x0F
AM13E23018HTPMR	0x6174	0x10
AM13E23017GTPDTR	0x6879	0x11
AM13E23017GTPZR	0x6879	0x12
AM13E23017GTPNR	0x6879	0x13
AM13E23017GTPMR	0x6879	0x14

7.4 Arm® Cortex®-M33 CPU

The Arm® Cortex®-M33 CPU is a 32-bit processor ideal for embedded applications that require efficient security or digital signal control. This CPU core includes features to enable such embedded applications, including memory protection units, a floating point unit, custom datapath instructions, and a micro trace buffer for instruction trace capabilities.

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7.4.1 Trigonometric Math Unit (TMU)

The Trigonometric Math Unit (TMU) extends the capabilities of the Arm® Cortex®-M33 CPU by leveraging instructions to speed up common trigonometric and arithmetic operations listed in Table 7-5.

Table 7-5. TMU Supported Instructions

Instructions	Description
SINPUF32	Returns the SINE of input value
COSPUF32	Returns the COSINE of input value
ATANPUF32	Returns the ATAN of input value
DIVF32	Returns DIV value of two input values
QUADF32	Returns the quadrant value and the ratio of X and Y inputs which are provided as per unit values
SQRTF32	Returns the square root of input value
IEXP2F32	Returns inverse exponent of input value
LOG2F32	Returns base-2 logarithm of input value
ISQRTF32	Returns the inverse square root of input value
RSCTFLG	Read/Set/Clear the LUF and LVF flags that are maintained inside the TMU CDE

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7.4.2 Debug Subsystem

The AM13E230x Debug Subsystem integrates the JTAG interface and accesses the Cortex®-M33 CPU debug registers through the Debug Access Port (DAP). The Cortex®-M33 DAP can be configured as a JTAG Debug Port (JTAG-DP), Serial Wire Debug Port (SW-DP), or Serial Wire/JTAG Debug Port (SWJ-DP).

Note

MCLK (CPUCLK) must be at 100MHz to use ETM tracing.

Micro Trace Buffer

The Micro Trace Buffer (MTB) on AM13E230x MCUs provides basic execution trace capability to the CPU core. When enabled, the MTB records changes in program flow, reported by the Cortex®-M33 processor over the execution trace interface. This information is stored as trace packets in the MTB memory. An external debugger can extract the trace information using the DAP. The debugger can then reconstruct the program flow from this information.

7.5 TinyEngine™ Neural-network Processing Unit (NPU)

The TinyEngine™ Neural-network Processing Unit (NPU) supports intelligent inferencing running pre-trained models. Capable of 600-1200MOPS (Mega Operations Per Second), the TinyEngine™ NPU provides up to 10x Neural Network (NN) inferencing cycle improvement compared to a software-only implementation. Load and train models with tools from TI for an advanced set of capabilities.

7.6 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

- DMA0: 12 independent DMA transfer channels
  - 6 full-feature channel supporting repeated transfer modes
  - 6 basic channels supporting single transfer modes and scatter mode
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

For more details, see the DMA chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

7.7 Error Aggregator Module (EAM)

The Error Aggregator Module (EAM) aggregates errors that include but are not limited to single error correction (SEC) and double error detection (DED) for the system memory and security errors. EAM latches the error into corresponding register that is forwarded to SYSCTL to generate an NMI or interrupt the CPU based on the priority of the error. The EAM module can be protected by a security firewall based on the GSC setting to allow customer critical code in secure mode of the application to handle the error in a context safe method.

The EAM supports the following features:

- ECC error logging for SEC and DED from flash and SRAM
- Security error logging for non-secure access to a firewall region for memory and peripherals
- Security error logging for hide protected region in the flash

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- First error logged with initiator and type of access error logged

7.8 Power Management and Clock Unit (PMCU)

7.8.1 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the band-gap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

7.8.2 Operating Modes

AM13E230x MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code when in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD/JTAG interface, a logic level match on certain IOs, or an interrupt from the low frequency sub system (LFSS).

To further balance performance and power consumption, AM13E230x devices implement two power domains: PD1, PD0. PD1 contains the CPU, memories, and high performance peripherals. PD1 contains is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 contains low speed, low power peripherals which are always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

7.8.2.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Table 7-6.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **RET**: The function's memory and configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but its use is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 7-6. Supported Functionality by Operating Modes

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
Supply State	VDD	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
	VDDC	1.35V	1.35V	1.0V	1.0V	1.0V	0V

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Table 7-6. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
PMU	POR monitor	EN					OFF
	BOR monitor	EN					OFF
	Main LDO	EN		OFF			
	STOP LDO	EN					OFF
	VOSC LDO	EN					OFF
Oscillators	SYSOSC	EN, 32MHz		EN, 4MHz	OFF		
	LFOSC	EN					
	XTAL	OPT		DIS			OFF
	HPLL	OPT		DIS			OFF
Clocks	MCLK	200MHz / 250MHz		DIS			OFF
	MCLK/2	100MHz / 125MHz		DIS			OFF
	MCLK/4	50MHz / 62.5MHz		DIS			OFF
	CPUCLK	200MHz / 250MHz	DIS				OFF
	LFCLK	32kHz					OFF
	ULPCLK	50MHz / 62.5MHz		4MHz	32kHz	OFF	OFF
	HFCLK	OPT		DIS			OFF
	CANCLK	OPT		DIS			OFF
	ADCCLK	100MHz / 125MHz		DIS			OFF
	LFCLK Monitor	OPT					OPT
	MCLK Monitor	OPT			DIS		OFF
Core Functions	CPU	EN	DIS				OFF
	Flash	EN		DIS			OFF
	SRAM0	EN		DIS + RET			OFF
	SRAM1/2/3	EN		DIS			OFF
PD1 Peripherals	ADC[0:2]	OPT		DIS + RET			OFF
	PGA[0:2]	OPT		DIS + RET			OFF
	CMPSS[0:3]	OPT		DIS + RET			OFF
	ECAP[0:1]	OPT		DIS + RET			OFF
	EQEP[0:2]	OPT		DIS + RET			OFF
	MCPWM[0:4]	OPT		DIS + RET			OFF
	UC[0:5]	OPT		DIS + RET			OFF
	MCAN0	OPT		DIS			OFF
	NPU	OPT		DIS			OFF
	EPI	OPT		DIS			OFF
	TIMG12_0	OPT		DIS + RET			OFF
	TIMG4_0	OPT		DIS + RET			OFF
	AES	OPT		DIS			OFF
	DMA0	OPT		DIS + RET			OFF
	XBAR	OPT		DIS			OFF
	EAM	OPT		DIS			OFF
	GSC	OPT		DIS + RET			OFF
	KEYSTORE	OPT		DIS + RET			OFF
	CRC	OPT		DIS + RET			OFF
	VREF	EN		EN (Sampled)			OFF

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Table 7-6. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
PD0 Peripherals	GPIO[0:3]	OPT					OFF
	SYSCTL	EN					OFF
	WWDT	OPT					OFF
IOMUX		EN		EN (Sampled)			OFF
IO Wakeup		EN		EN + RET			OFF
Wake Sources		N/A	• IRQ • IO • DMA Req • Debug Req • WWDT	• IO • Debug Req • WWD		• IO • Debug Req	• IO (subset) [1] • Debug Req

1. Select WAKEUP GPIOs. Refer to the device-specific data sheet.

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7.8.3 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim, 16 MHz or 24 MHz with user trim)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 200 MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals in MCLK domain, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **MCLK/2**: Main system clock for PD1 peripherals in MCLK/2 domain, derived MCLK and divided by 2
- **MCLK/4**: Main system clock for PD1 peripherals in MCLK/4 domain, derived MCLK and divided by 4
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **XCLKOUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High-frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High-speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL

For more details, see the CKM chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

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7.9 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register
- GPIO pins with Standard-drive with wake functionality can wake-up the device from SHUTDOWN mode

For more details, see the IOMUX chapter of the *AM13E230x Microcontrollers Technical Reference Manual*

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7.9.1 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *AM13E230x Microcontrollers Technical Reference Manual*

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 7-1. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

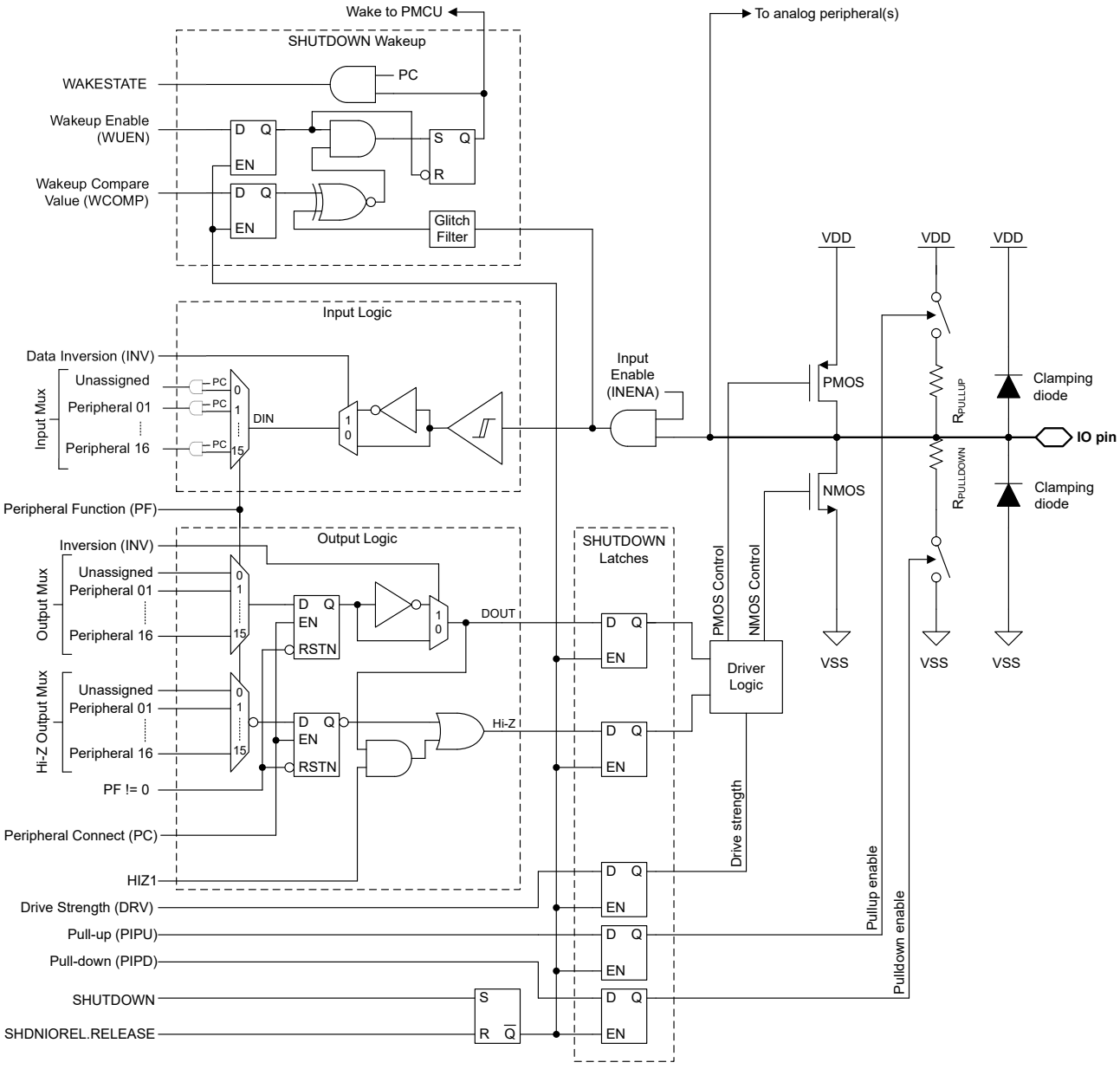


Figure 7-1. Superset Input/Output Diagram

7.10 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality, see the debug chapter of the *AM13E230x Microcontrollers Technical Reference Manual* .

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Table 7-7. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

7.11 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART, I2C, or MCAN serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined HASH password. The BSL can be completely disabled in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSL_UART_RX and BSL_UART_TX signals (for UART), or the BSL_I^{2}C_SCL and BSL_I^{2}C_SDA signals (for I^{2}C) or the BSL_CAN_RX and BSL_CAN_TX signals (for MCAN). Additionally, one or two additional pins (BSL_INVOKE and NRST) can be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL can be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device verifies the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI invokes the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL can be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 7-8. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSL_UART_RX	Required for UART	UART receive signal (RX), an input
BSL_UART_TX	Required for UART	UART transmit signal (TX) an output
BSL_I2C_SCL	Required for I2C	I^{2}C BSL clock signal (SCL)
BSL_I2C_SDA	Required for I2C	I^{2}C BSL data signal (SDA)
BSL_CAN_RX	Required for CAN	MCAN receive signal (RX), an input
BSL_CAN_TX	Required for CAN	MCAN receive signal (TX), an output
BSL_INVOKE	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the AM13E230x Bootloader User's Guide.

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7.12 Security

Security features are enforced by the Global Security Controller (GSC). The AM13E230x microcontroller supports the following security features using a combination of hardware blocks, BootROM software, and Customer Secure Code (CSC) programmable into the flash sectors:

- Secure boot
- Secure debug
- Secure firmware update
- Secure key storage
- Secure key management
- Privileged/Non-Privileged partitioning of on chip resources (flash sectors, RAM chunks, peripherals)

In addition to the GSC, AM13E230x has two other security hardware IPs present on the MCU: AESADV and the Keystore Controller.

7.12.1 Global Security Controller (GSC)

The Global Security Controller (GSC) is implemented on the AM13E230x microcontroller to support the following features:

- Provides privileged and non-privileged context information to access on-chip memory and peripherals
- Monitors the bus transactions from multiple initiators to ensure context of access to targets is maintained
- Logs errors for incorrect transactions on the bus
- Performs interrupt or reset generation when context is violated
- Provides mechanism to handle static and dynamic configuration of the security block
- Provides mechanism for managing the life cycle of the device.

The GSC is comprised of the following blocks:

- SRAM Protection Controller (SPC): Controls the context for SRAM
- Flash Protection Controller (FPC): Controls the context for on-chip flash
- Peripheral Protection Controller (PPC): Controls the context for peripherals
- Secure Exception Controller (SEC): Logs and provides action on a security exception

For more details, see the Global Security Controller (GSC) chapter of the *AM13E230x Microcontrollers Technical Reference Manual*

7.12.2 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- Support for AES-CCM and AES-GCM modes
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the Operating Modes section of the *AM13E230x Microcontrollers Technical Reference Manual*)

For more details, see the AESADV chapter of the *AM13E230x Microcontrollers Technical Reference Manual*

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7.12.3 Keystore Controller

The Keystore Controller on the AM13E230x MCU provides secure management of the Advanced Encryption Engine (AES) keys. During the execution of secure customer code, keys are securerly desposited into the Keystore Controller. The AES engine can then access keys in a secure manner without leaking any key data to observers.

Both 128- and 256-bit keys can be stored in the Keystore key slots.

For more details, see the KEYSTORE chapter of the *AM13E230x Microcontrollers Technical Reference Manual*

7.12.4 CRC Accelerator

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *AM13E230x Microcontrollers Technical Reference Manual*

7.13 Timers (TIMx)

The timer peripherals in these devices support the following key features, for specific configuration see Table 7-9:

Specific features for the general-purpose timer (TIMGx) include:

- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow CC/load register available
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

Table 7-9. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG4_0	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG12_0	PD1	32-bit	–	–	2	–	–	Yes	–	–	–

7.14 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

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8 Applications, Implementation, and Layout

8.1 JTAG and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS™) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.2 Schematic

TI recommends connecting a combination of a bulk decoupling capacitor (C_{VDD}) and a small-value low-ESR ceramic decoupling capacitor (C_{DEC}) across the VDD and VSS pins, the VDDA and VSSA pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The C_{VDD} bulk decoupling capacitor has a standard value referenced in the specifications section of the datasheet, but may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The $\overline{\text{NRST}}$ reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external pullup resistor (Rpu_{NRST}) with a pulldown capacitor (C_{NRST}) for most applications to ensure that the default $\overline{\text{NRST}}$ state is logic-high (not triggering MCU reset), while also enabling the $\overline{\text{NRST}}$ pin to be controlled by another device or a debug probe.

Note

Refer to the *AM13E230x Hardware Design Guidelines* for detailed application design guidance, such as recommended hardware connections and selection of external passive components.

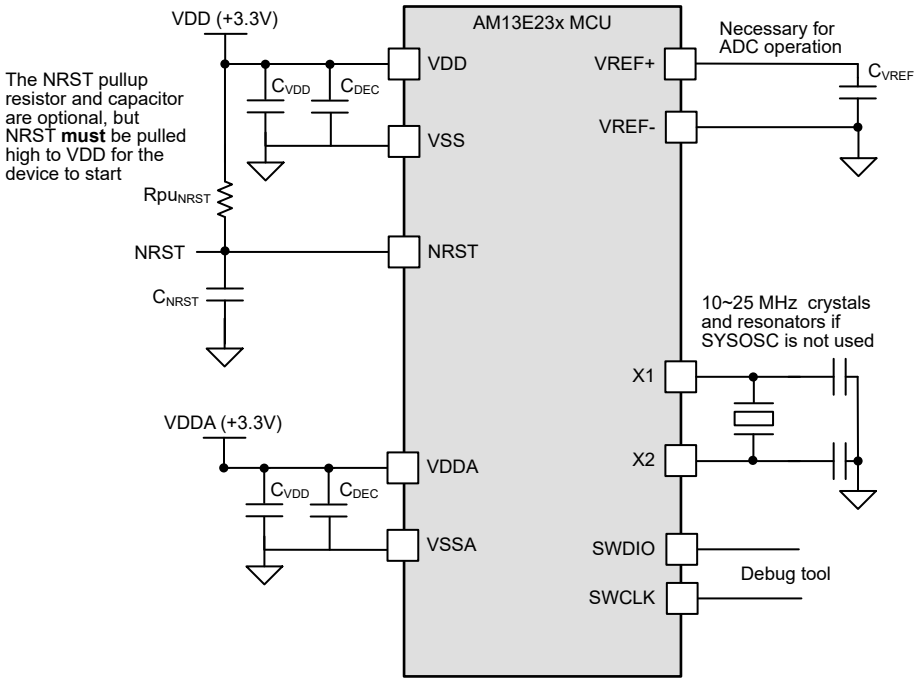


Figure 8-1. Basic Application Schematic

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8.3 Typical Applications

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Third-Party Products Disclaimer

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9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all ASM MCU devices and support tools. . Each ASM MCU commercial family member has one of two prefixes: ASM or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (ASM).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

ASM – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." ASM devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Device Nomenclature provides a legend for reading the complete device name.

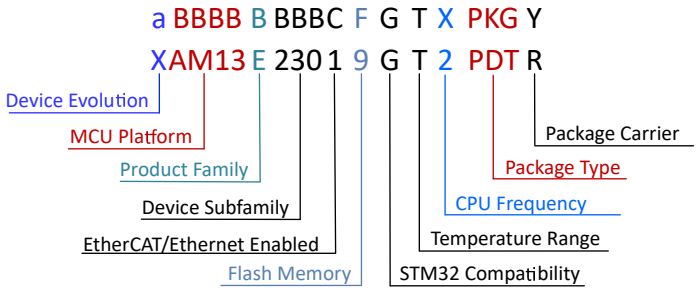


Figure 9-1. Device Nomenclature

Nomenclature Section	Device/Platform Subfamily	Descriptor	Device Options
Device Evolution		a	X = Prototype P = Preproduction (no reliability data) BLANK = Production
MCU Platform	Platform	B	AM1 = AM1x Family of MCU's
	CPU Type		3 = Cortex M33 CPU
Product/Family/Type		B	E = Entry Level Motor Control Device
Device Subfamily	Frequency Class	B	2 = 200/250 MHz Class Device
	Voltage	B	3 = 3.3V Design
	Variant	B	0 = Variant 0 in this family series

ADVANCE INFORMATION

Nomenclature Section	Device/Platform Subfamily	Descriptor	Device Options
EtherCAT/Ethernet Enabled		C	1 = Single CPU, No EtherCAT or Ethernet N = EtherCAT or Ethernet enabled
Flash Memory		F	7 = 128KB Flash 8 = 256KB Flash 9 = 512KB Flash
STM32 Compatibility		G	G = STM32G4 Pin Compatible H = STM32H5 Pin Compatible
Temperature Range		T	T = -40°C to 125°C (Ambient)
CPU Frequency		X	BLANK = 250MHz 2 = 200MHz
Package Type		PKG	PDT = LQFP128 PZ = LQFP100_G/H PN = LQFP80 PM = LQFP64_G/H PT = LQFP48 RGZ = QFN48
Package Carrier		Y	R = Tape & Reel Carrier

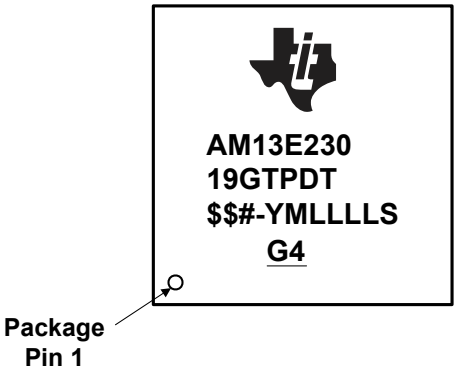
For orderable part numbers of ASM devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

ADVANCE INFORMATION

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9.3 Markings

Package Symbolization for PDT Package, *Package Symbolization for PZ Package*, *Package Symbolization for PNA Package*, *Package Symbolization for PM Package*, *Package Symbolization for PT Package*, and *Package Symbolization for RGZ Package* show the package symbolization.



19GTPDT or 19GT2PDT

BLANK = 250MHz, 2 = 200 MHz

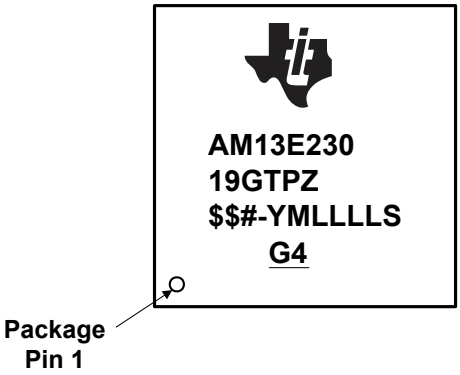
G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-2. Package Symbolization for PDT Package



19GTPZ or 19GT2PZ

BLANK = 250MHz, 2 = 200 MHz

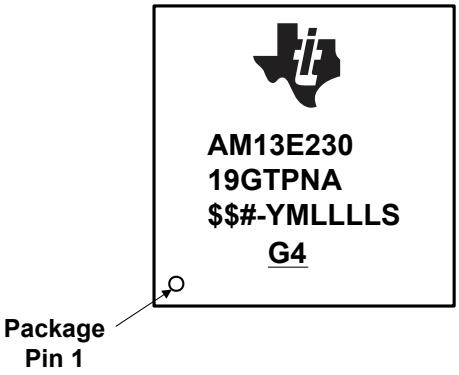
G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-3. Package Symbolization for PZ Package



19GTPNA or 19GT2PNA

BLANK = 250MHz, 2 = 200 MHz

G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-4. Package Symbolization for PNA Package

ADVANCE INFORMATION

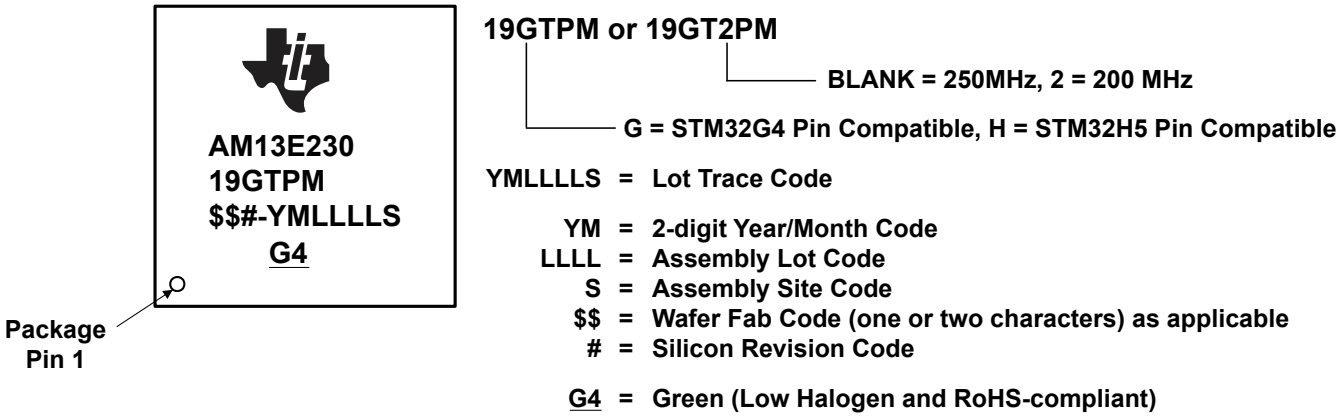


Figure 9-5. Package Symbolization for PM Package

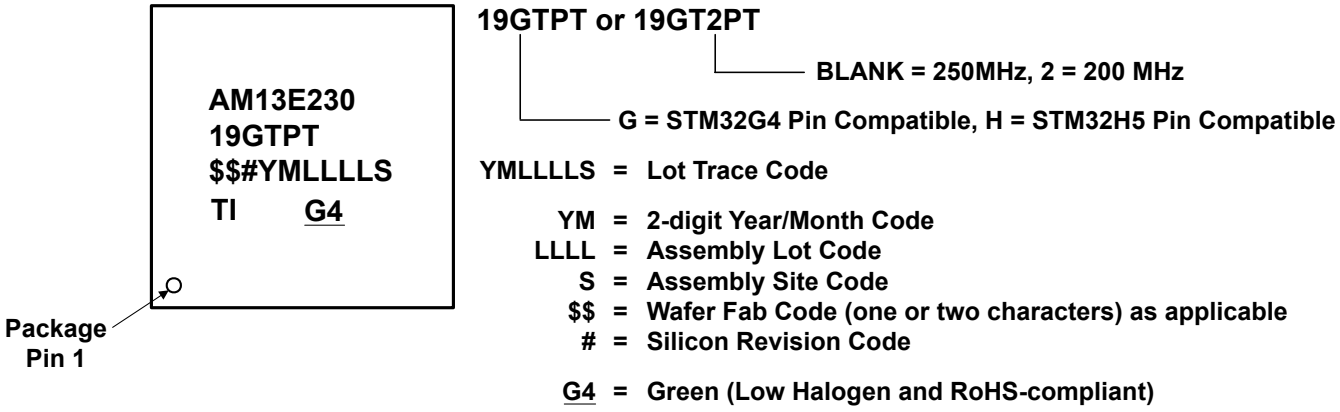


Figure 9-6. Package Symbolization for PT Package

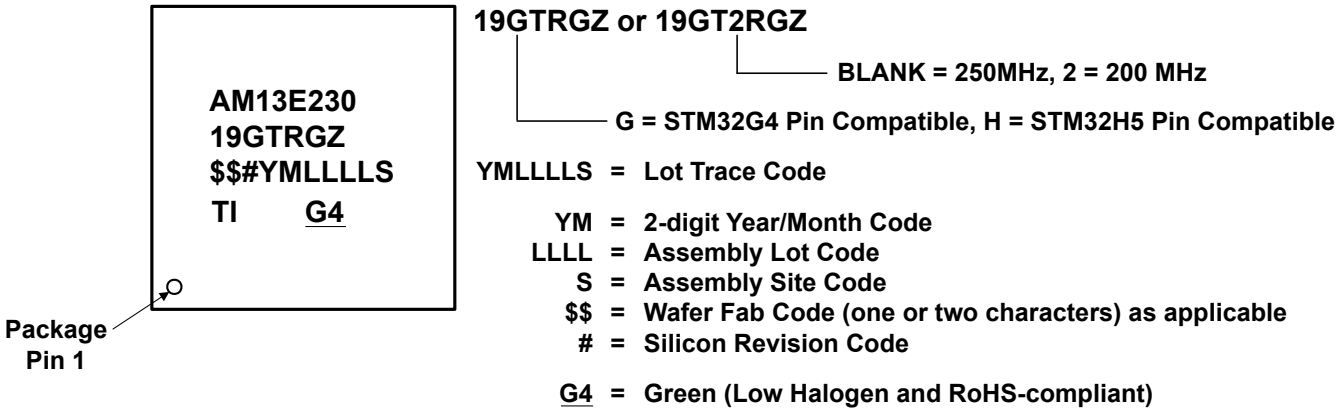


Figure 9-7. Package Symbolization for RGZ Package

9.4 Tools and Software

Design Kits and Evaluation Modules

AM13E230LaunchPad (LP) Boards: LP-AM13E230 ***Update link***	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose ASM MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging.

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	The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.
Embedded Software	
AM13 Software Development Kit (SDK)**(update link)**	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all AM13 devices.
Software Development Tools	
TI Developer Zone	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)
ASM Academy**(update the link)**	Great starting point for all developers to learn about the ASM MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain ASM MCU features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.
IDE & compiler toolchains	
Code Composer Studio™ (CCS)	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.
IAR Embedded Workbench® IDE	IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for ASM AM13.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.
Keil® MDK IDE	Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for ASM AM13.Keil MDK includes a fully integrated debugger for source and disassembly level debugging. MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in the Code Composer Studio IDE.
GNU Arm Embedded Toolchain	The ASM AM13 SDK supports development using the open-source Arm GNU Toolchain. Arm GCC is supported by Code Composer Studio IDE (CCS).

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM13E230x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

AM13E230x Microcontrollers	This manual describes the modules and peripherals of the AM13E230x family of devices. Each description presents the module or peripheral in a general sense. Not

ADVANCE INFORMATION

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Technical Reference Manual	all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in the exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device.

9.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 28, 2026 to August 30, 2026 (from Revision * (February 2026) to Revision A (August 2026))	Page
• (Signal Descriptions): Updated PIN TYPE to SIGNAL TYPE column name for all Signal Description tables within this document	58
• *Device Identification Registers* table: Changed PARTIDL Bits 14-13 from INSTASPIN to RESERVED. Added silicon revision number (REVID) for Revision C silicon	145

ADVANCE INFORMATION

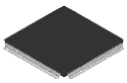
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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

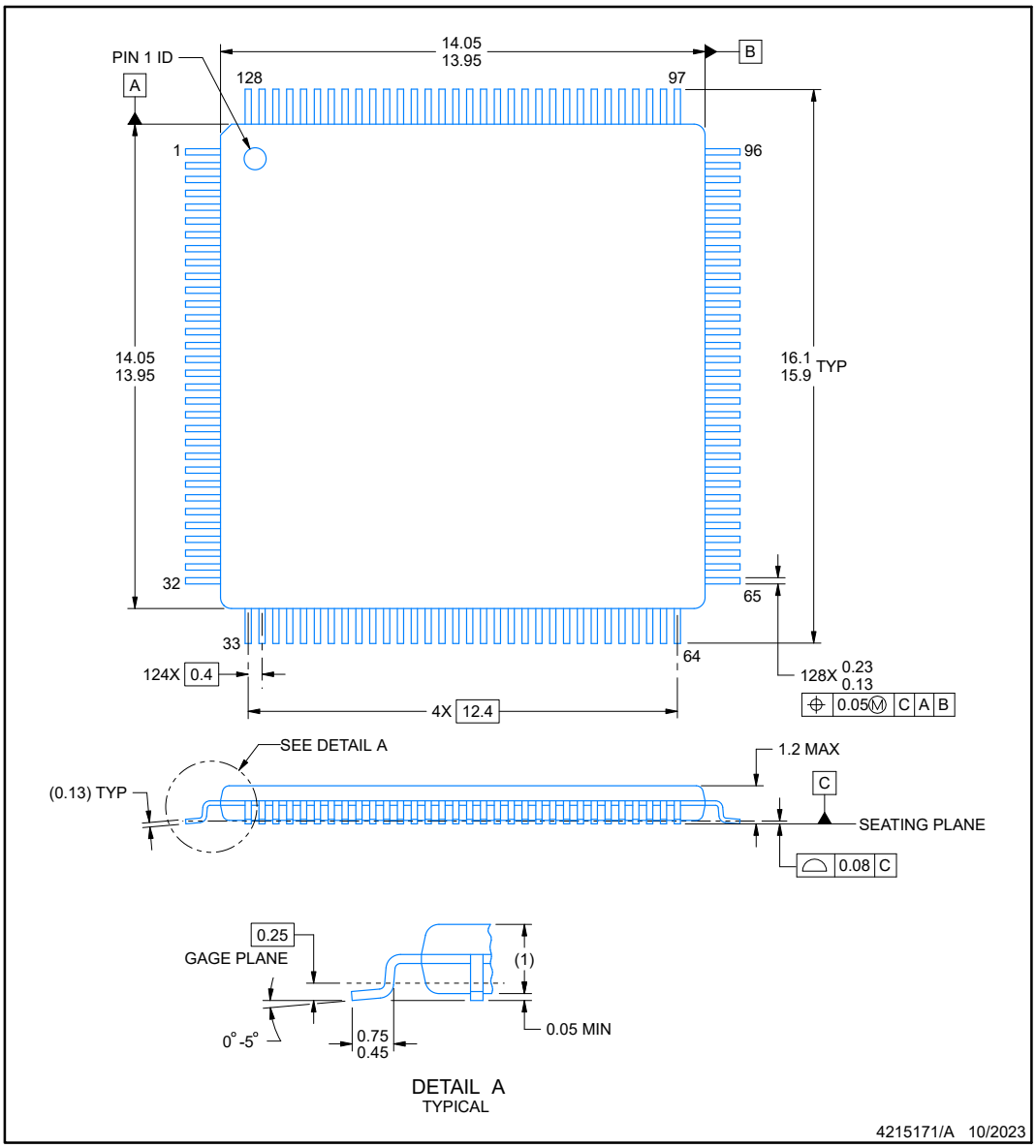


PACKAGE OUTLINE

PDT0128A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES:

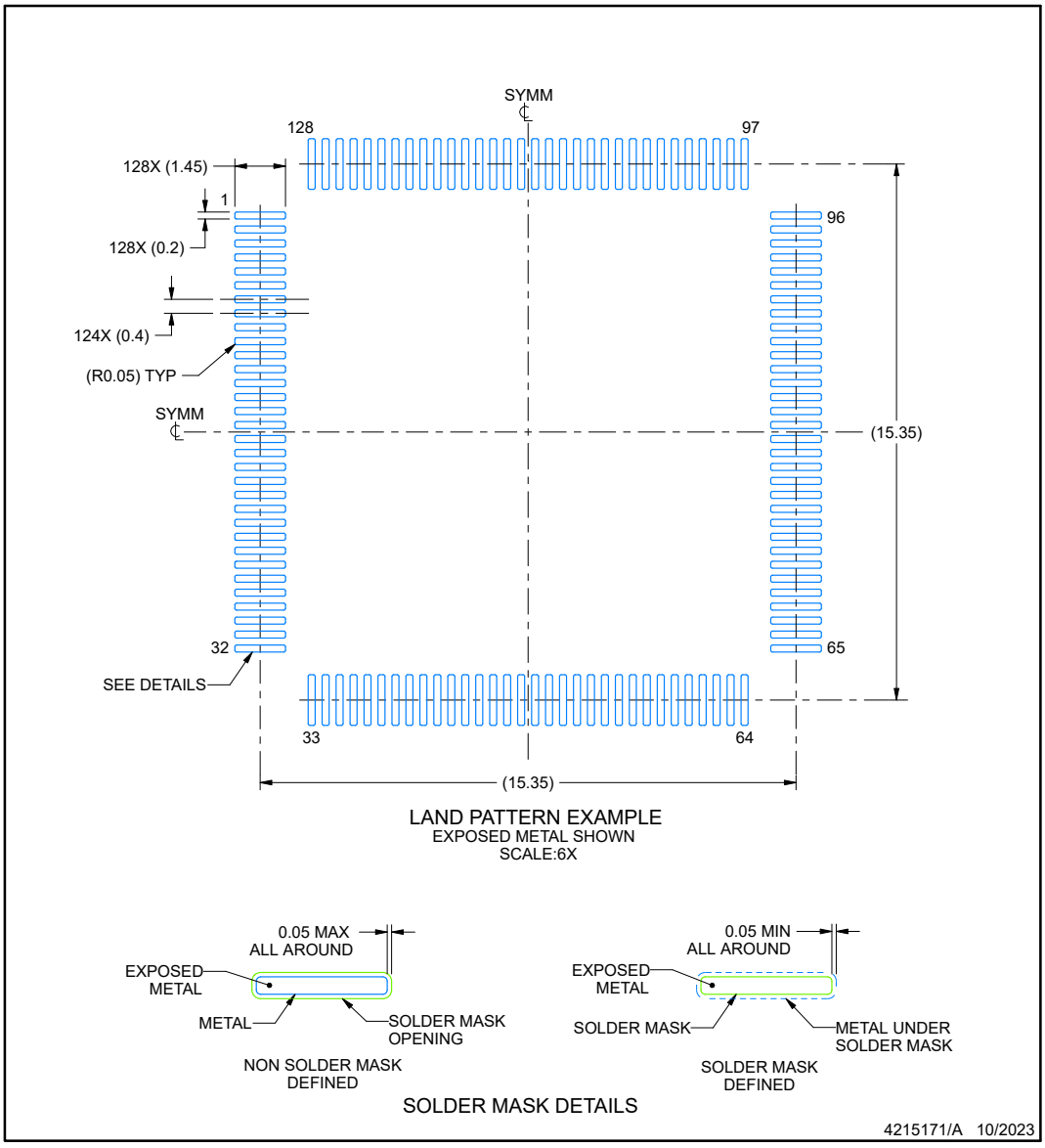
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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EXAMPLE BOARD LAYOUT

PDT0128A — **TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

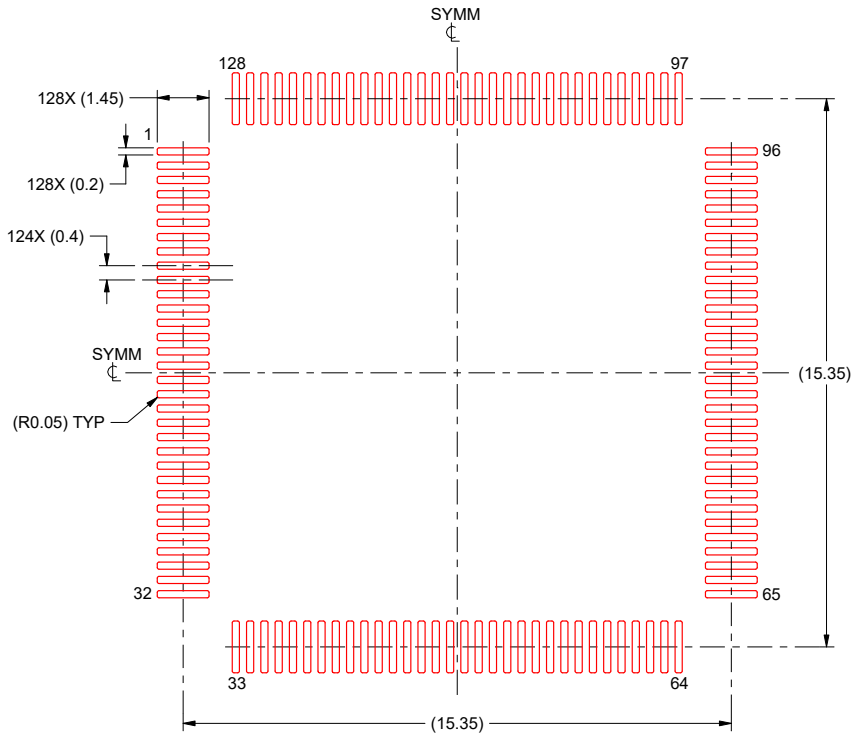
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PDT0128A — **TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



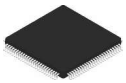
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215171/A 10/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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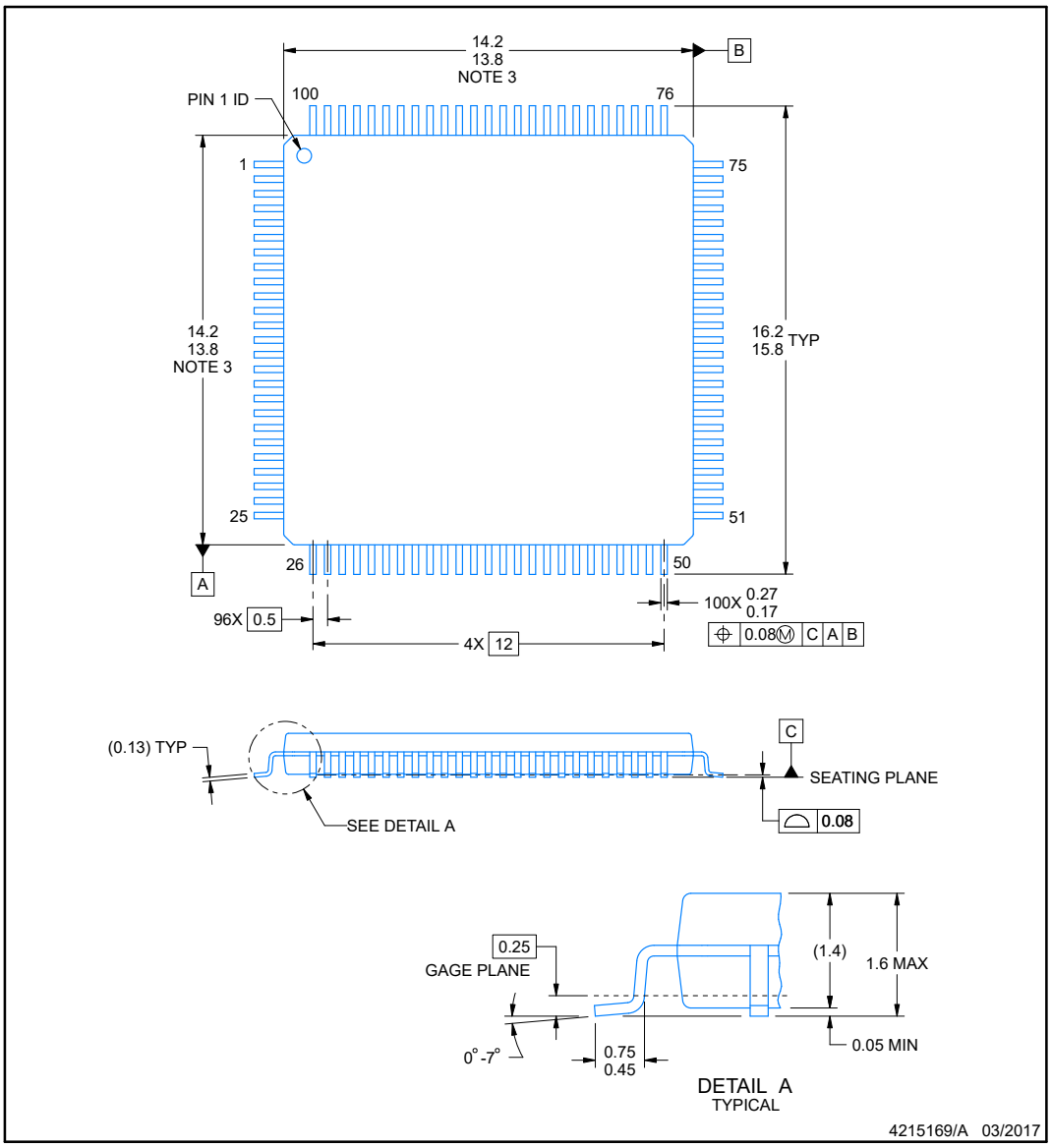


PACKAGE OUTLINE

PZ0100A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

www.ti.com

ADVANCE INFORMATION

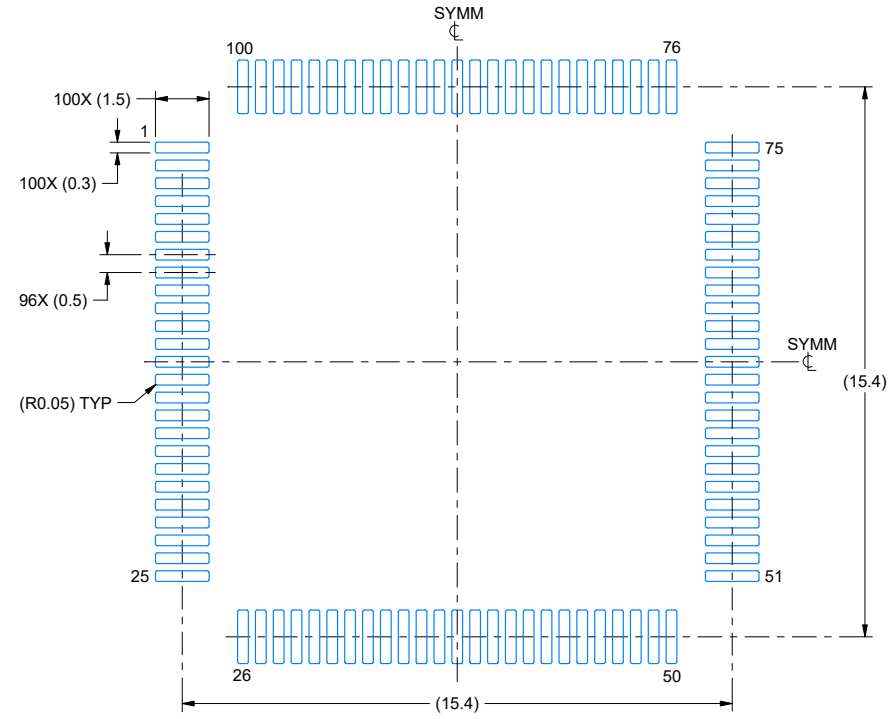
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ADVANCE INFORMATION

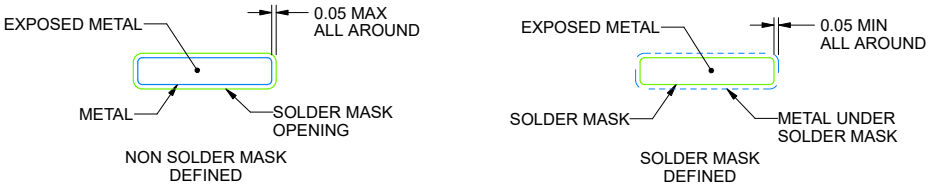
EXAMPLE BOARD LAYOUT

PZ0100A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

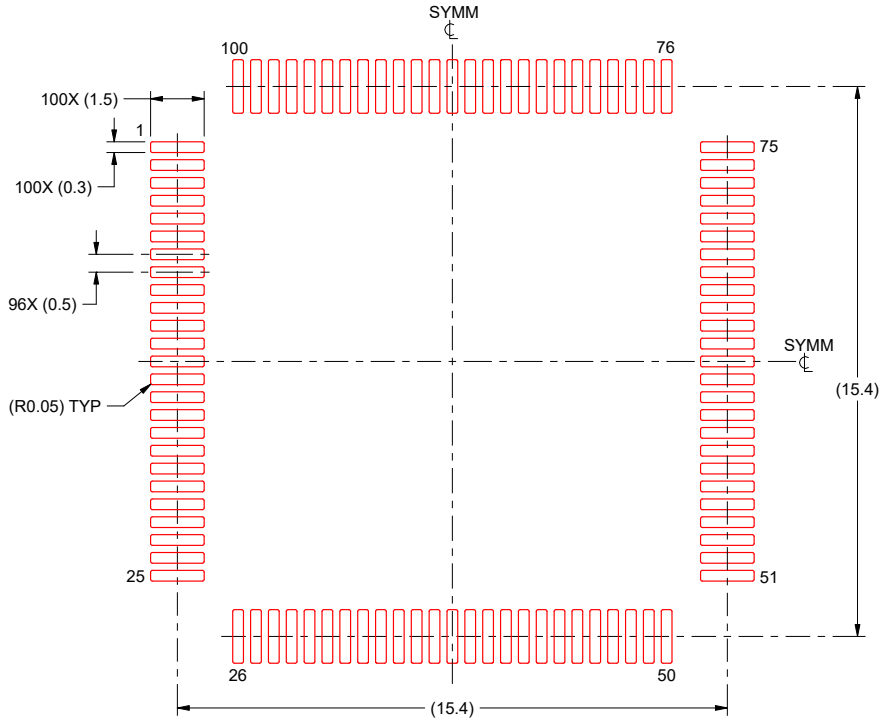
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

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EXAMPLE STENCIL DESIGN

PZ0100A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

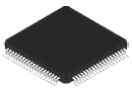
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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ADVANCE INFORMATION

ADVANCE INFORMATION

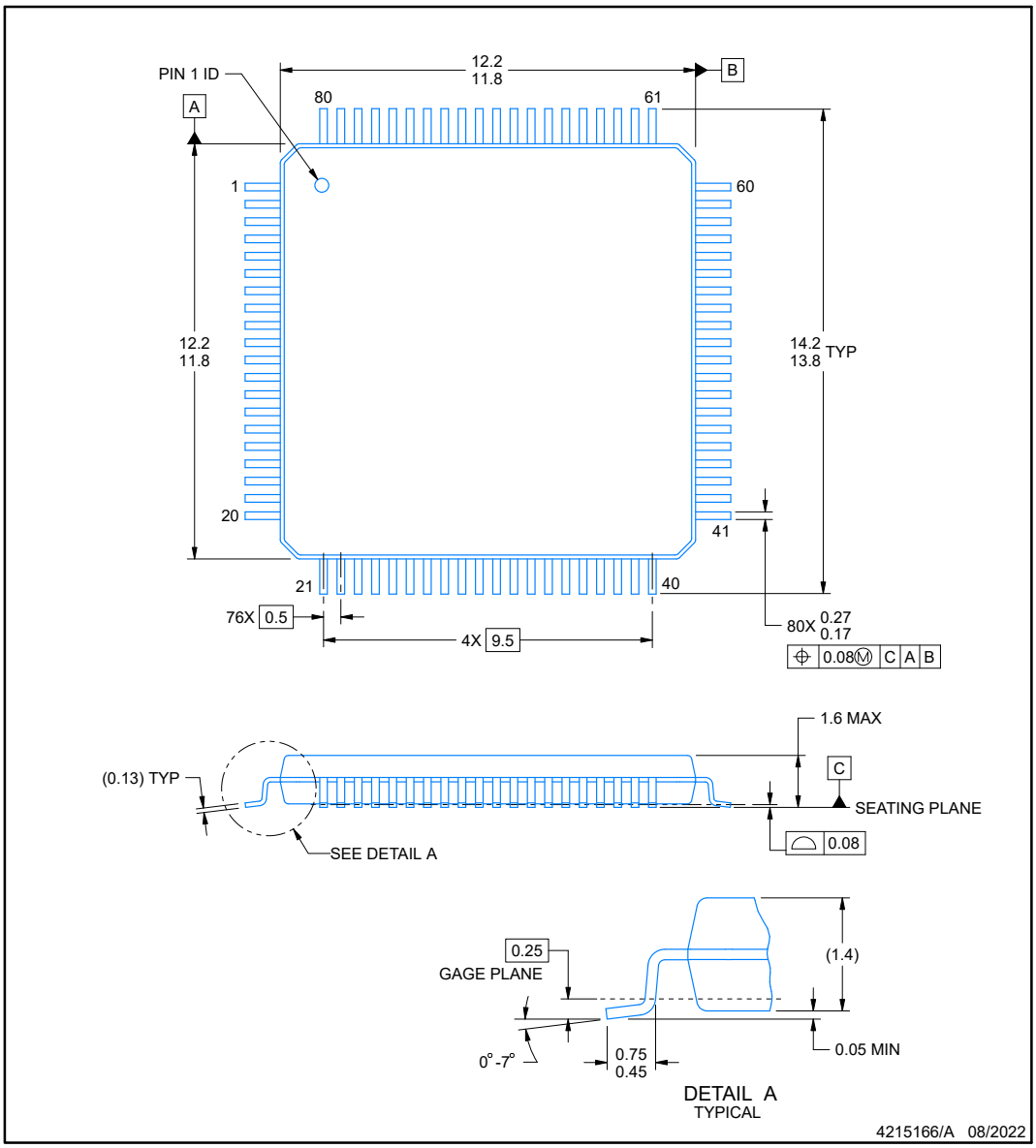


PACKAGE OUTLINE

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

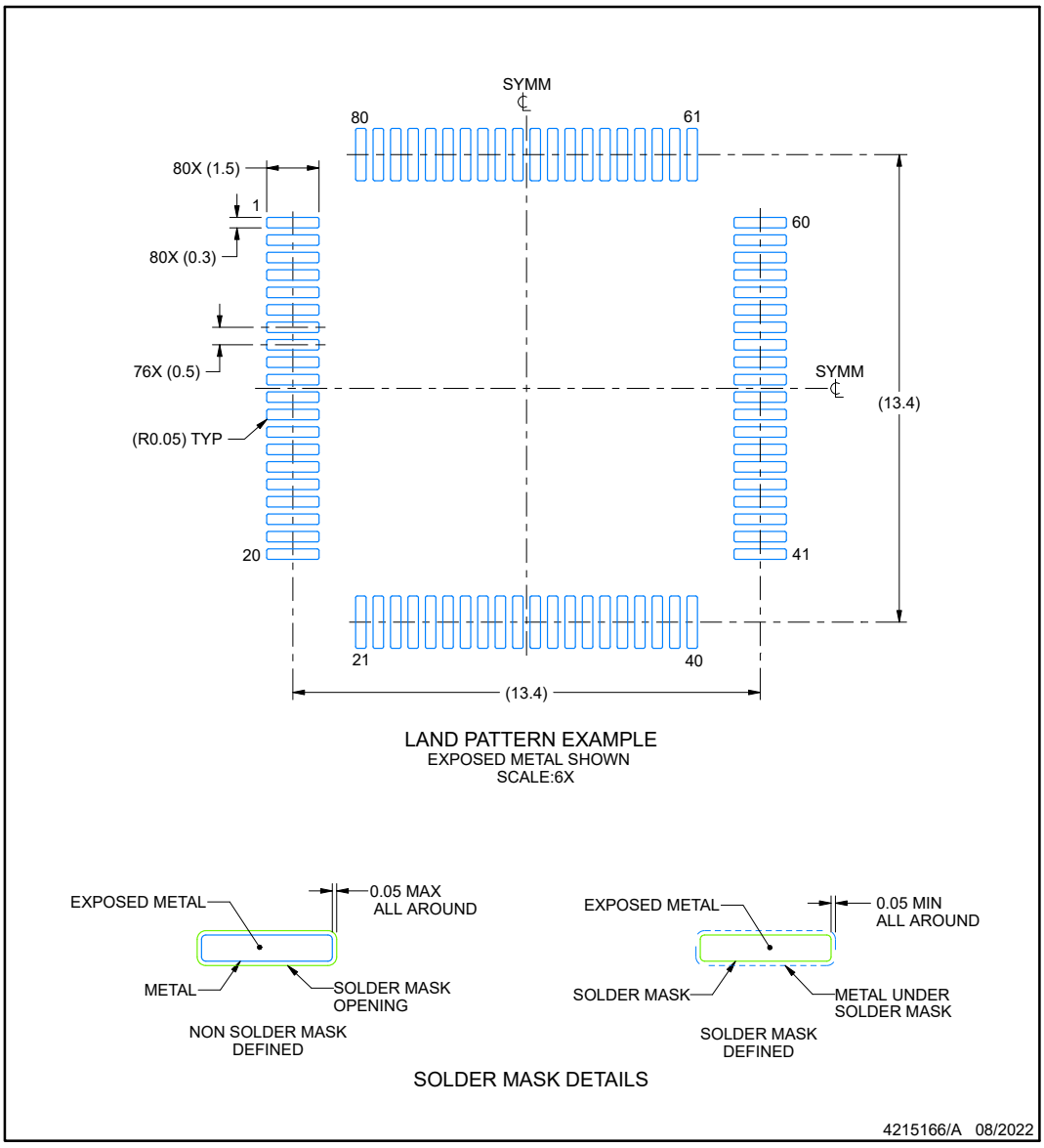
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EXAMPLE BOARD LAYOUT

PN0080A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

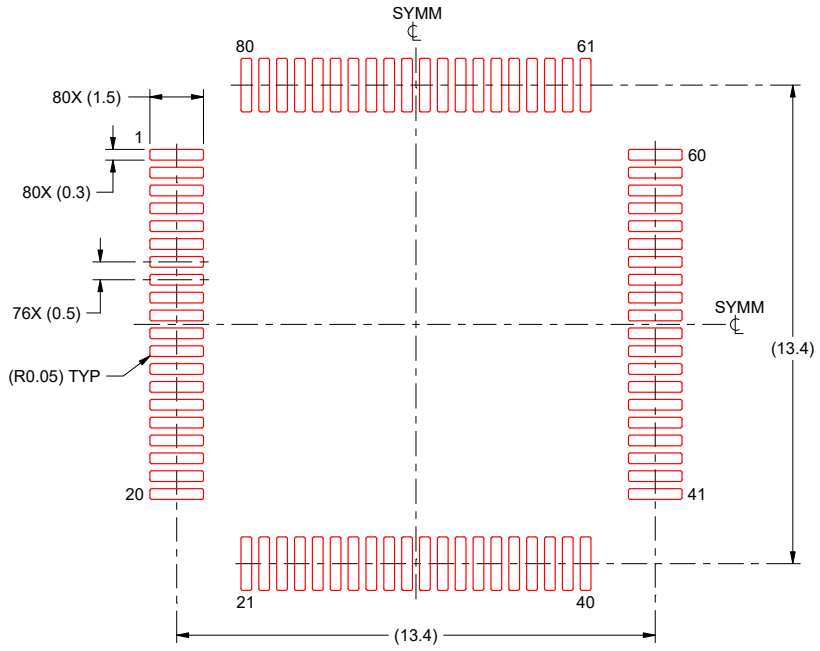
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PN0080A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



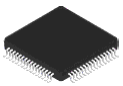
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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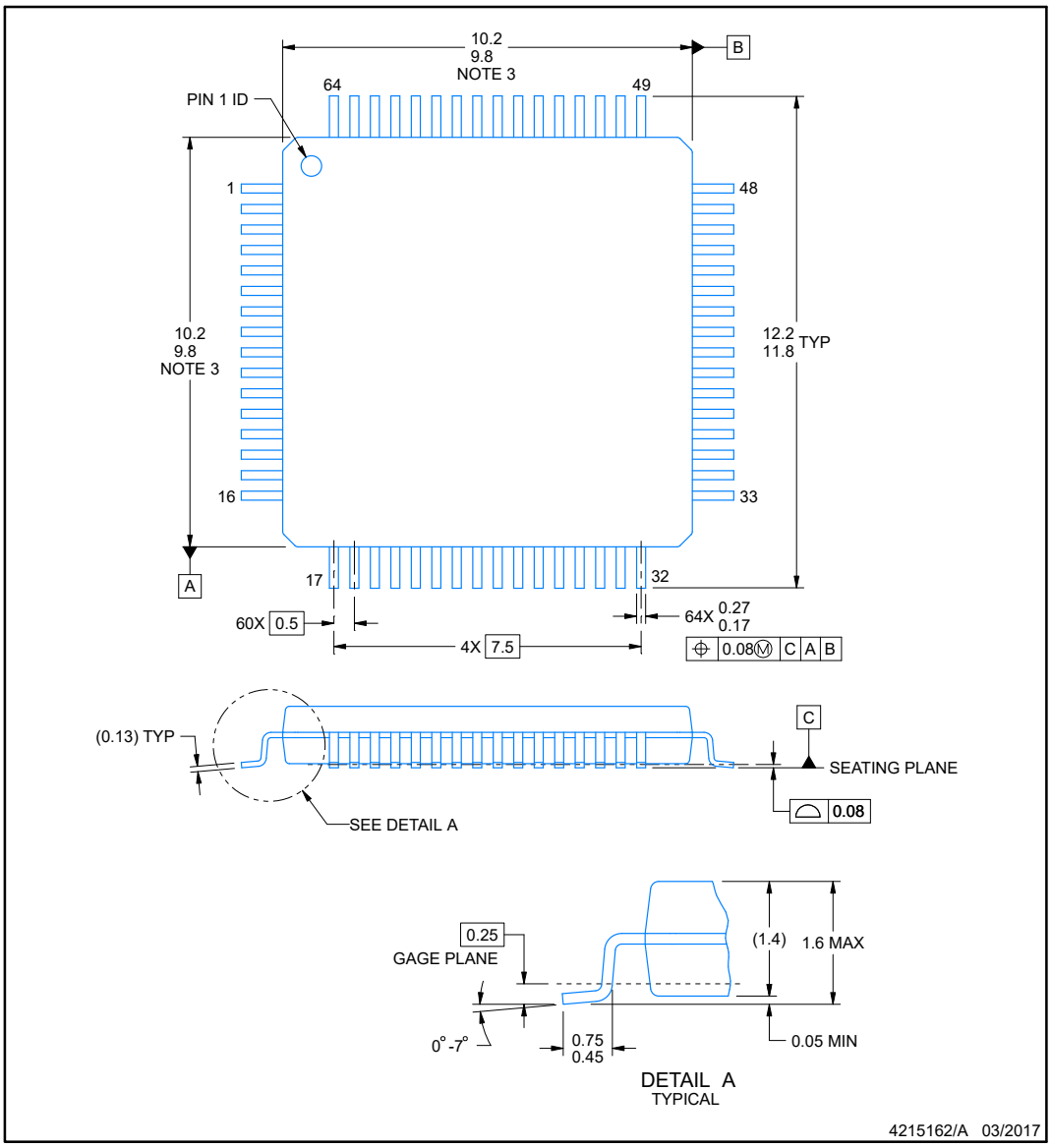


PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

www.ti.com

ADVANCE INFORMATION

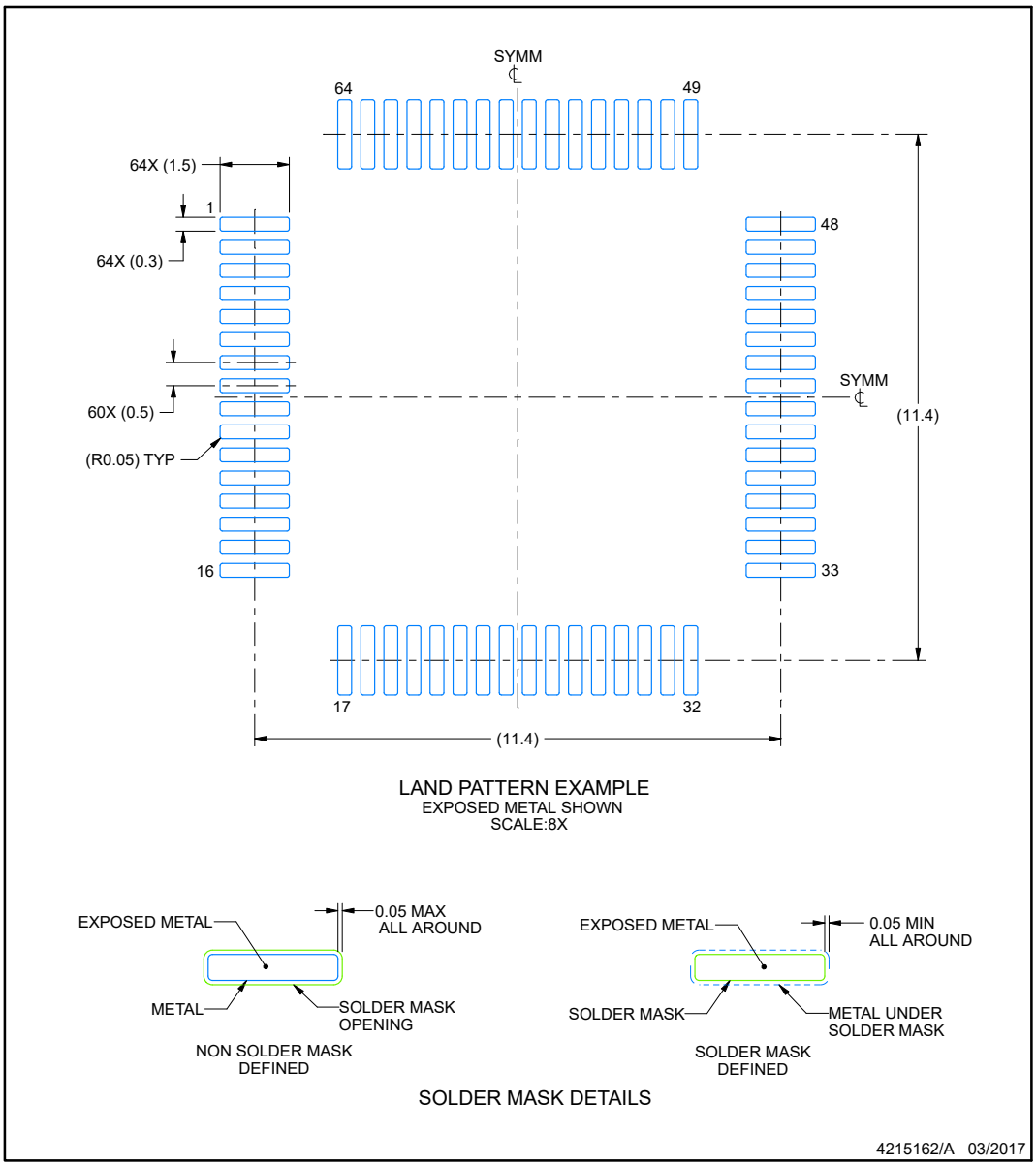
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ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PM0064A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

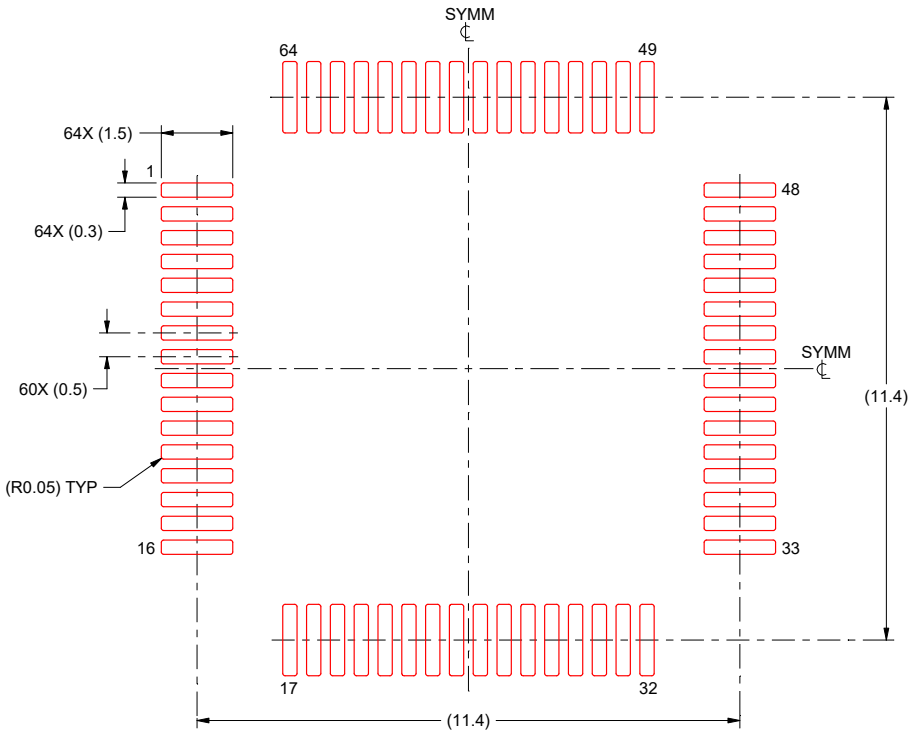
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

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EXAMPLE STENCIL DESIGN

PM0064A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

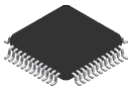
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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ADVANCE INFORMATION

ADVANCE INFORMATION

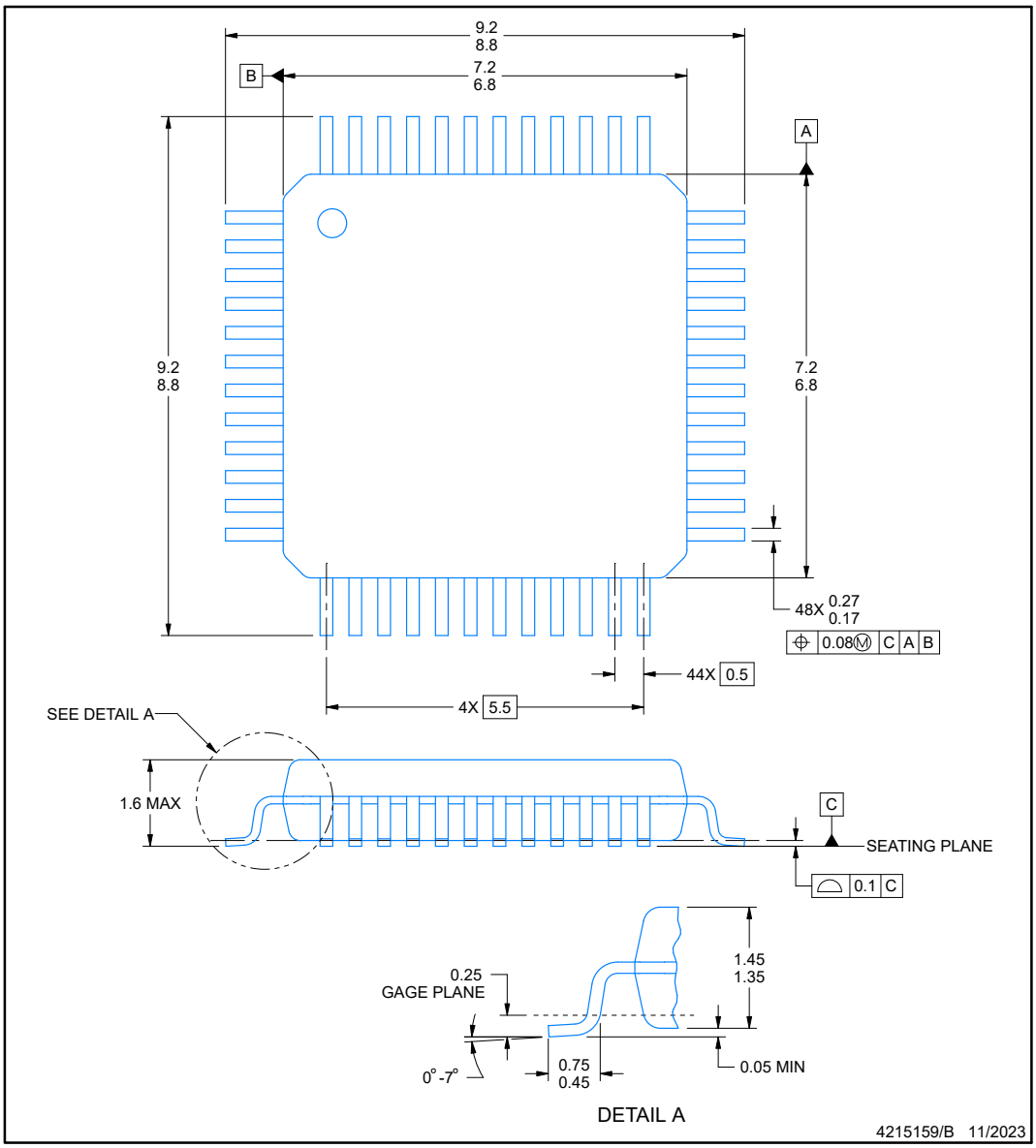


PACKAGE OUTLINE

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

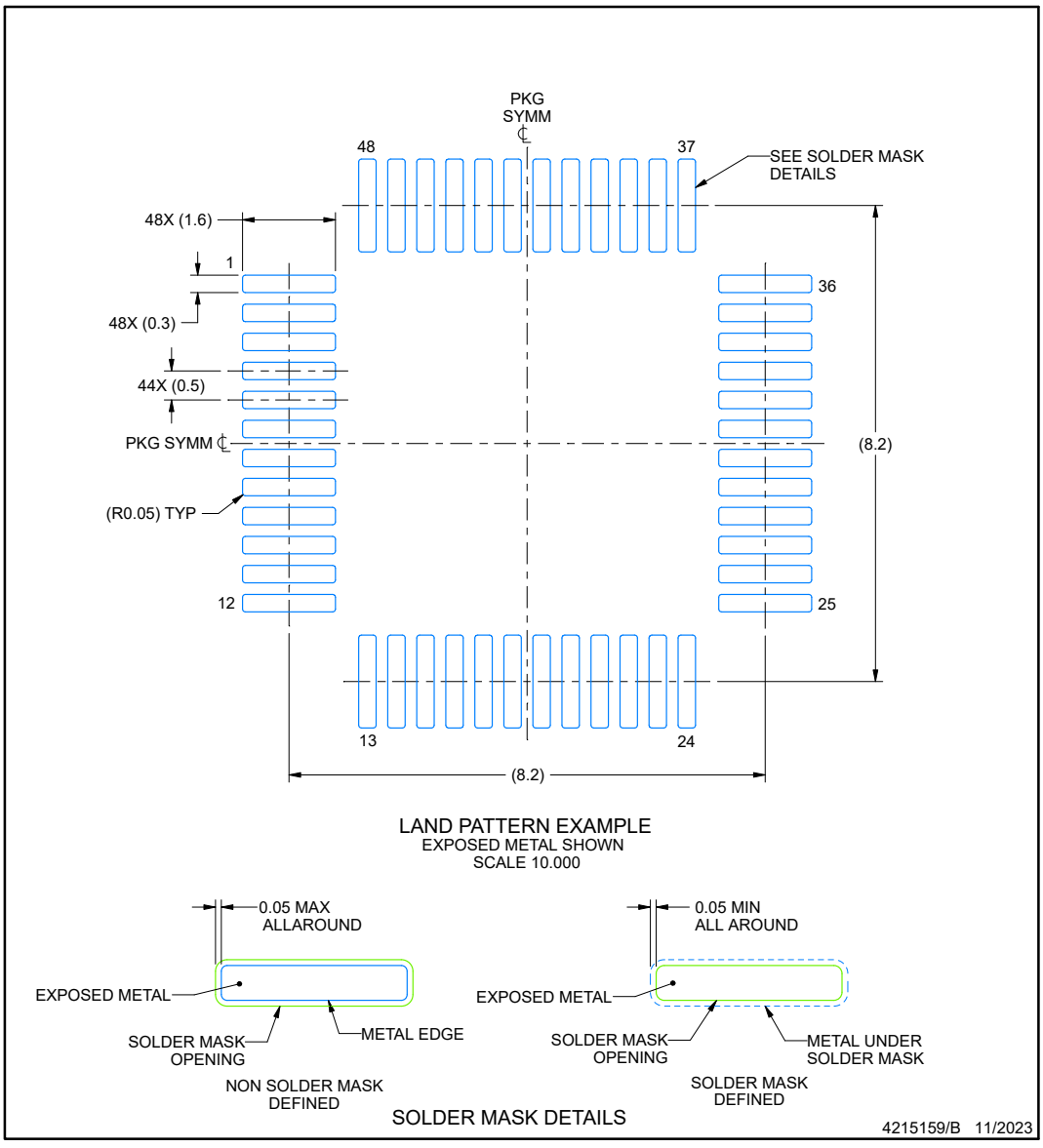
www.ti.com

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EXAMPLE BOARD LAYOUT

PT0048A — **LQFP - 1.6 mm max height**

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

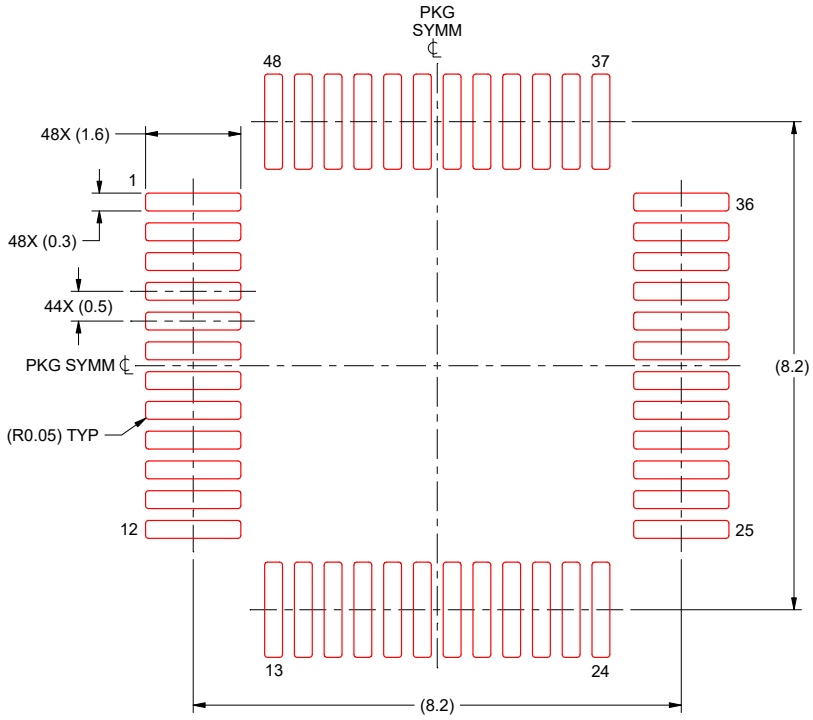
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PT0048A — **LQFP - 1.6 mm max height**

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

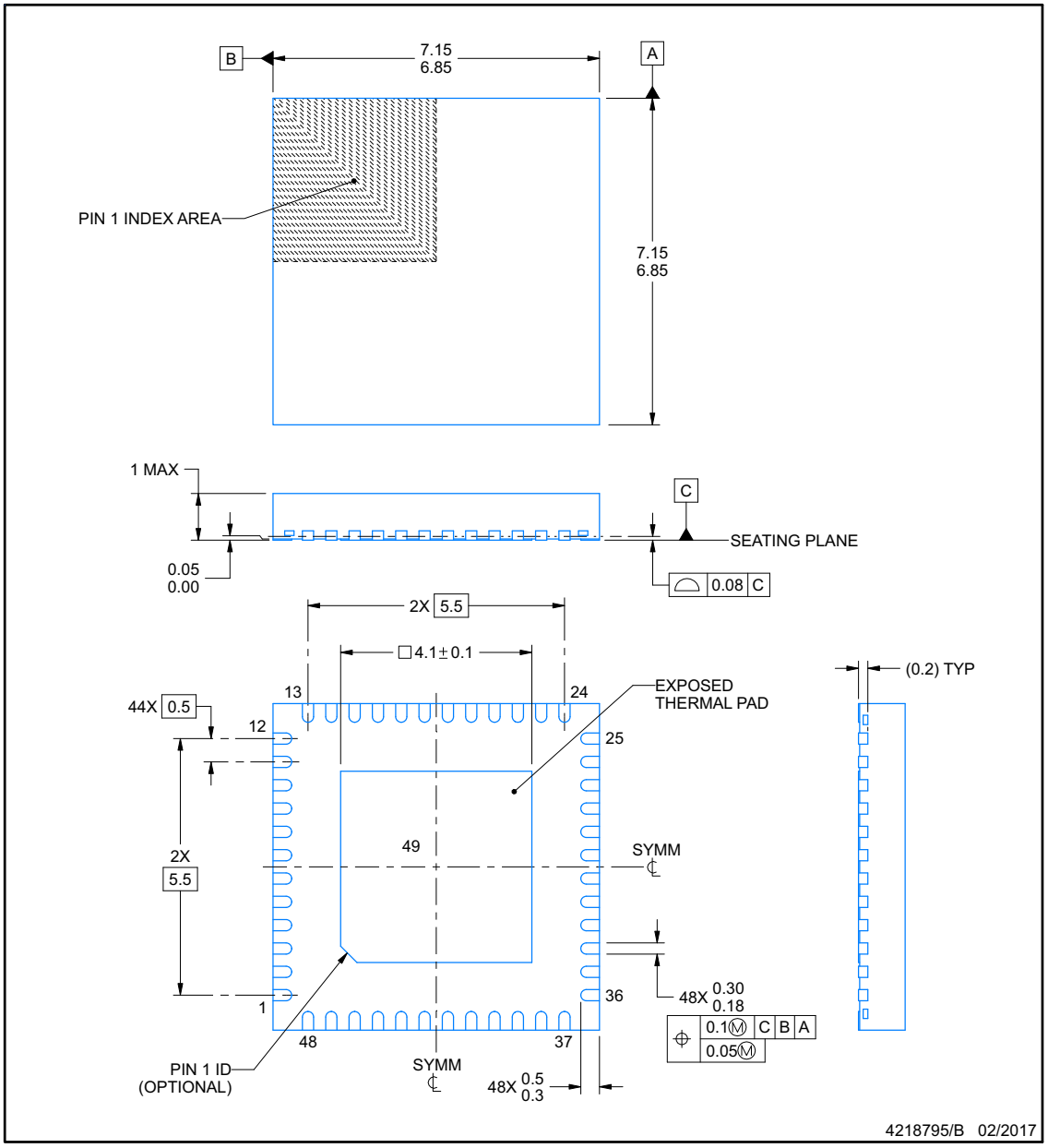
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PACKAGE OUTLINE

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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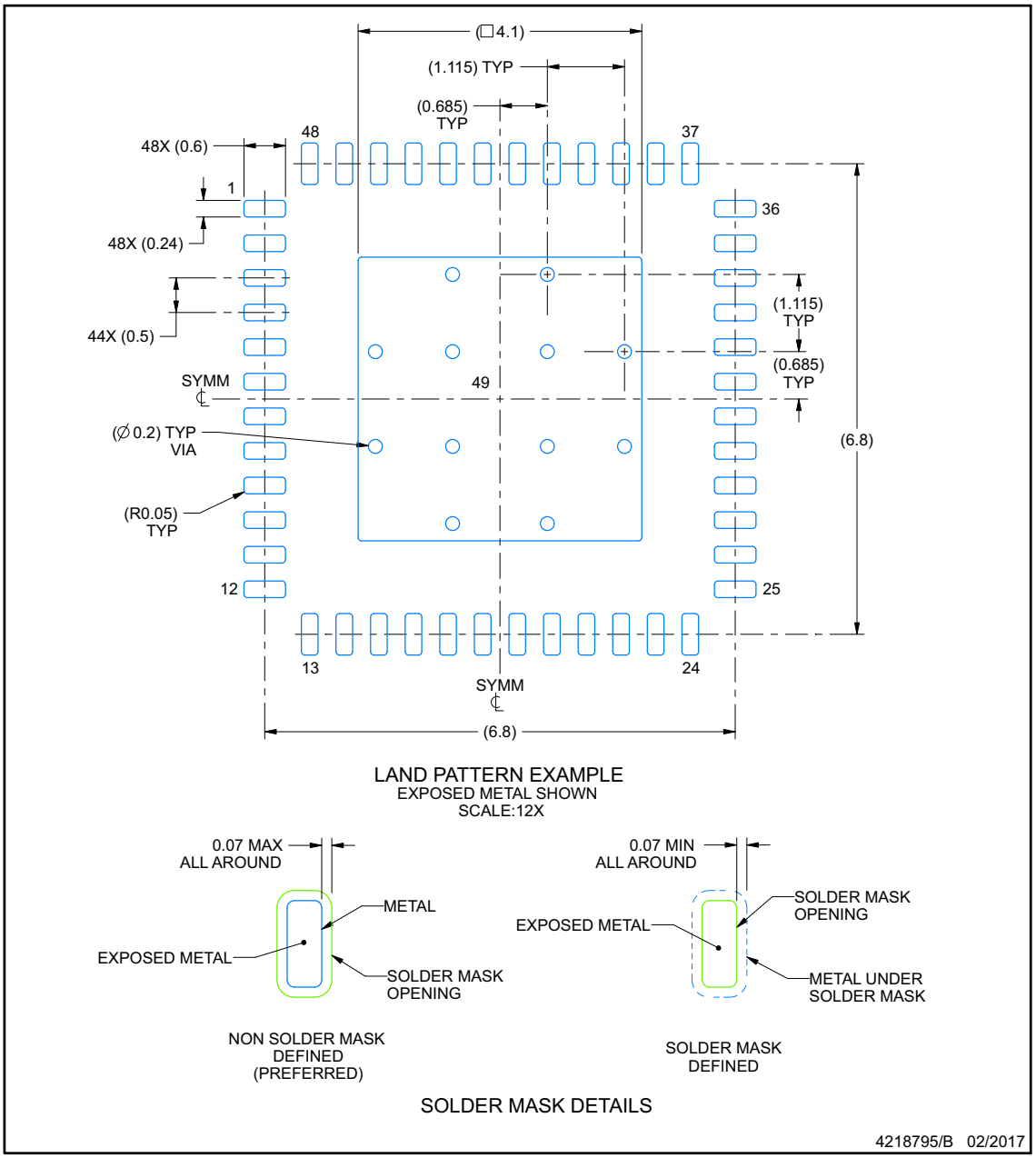
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

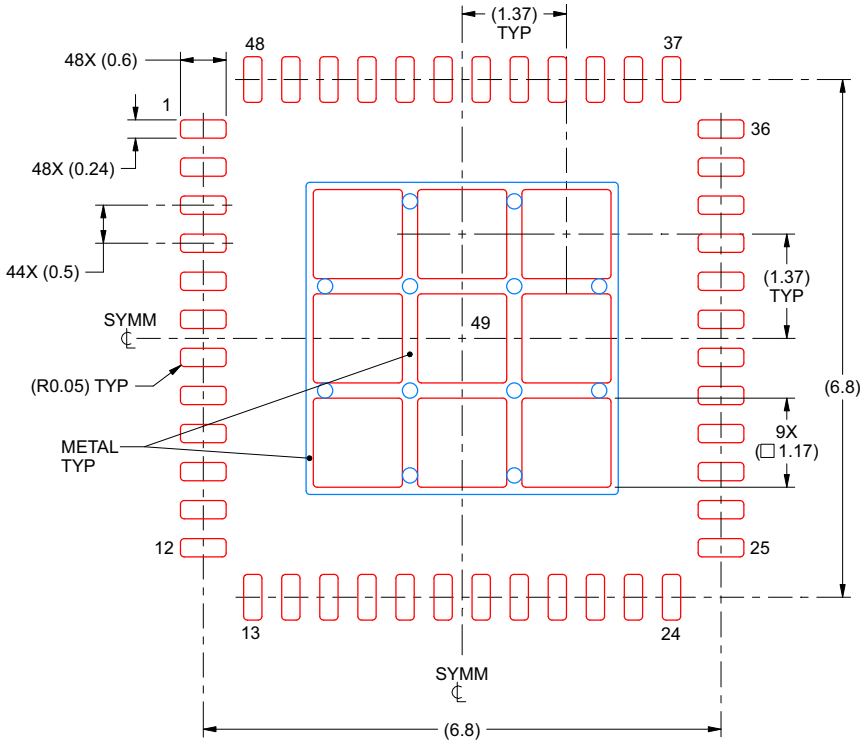
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package | Pins	Package qty | Carrier	RoHS	Lead finish/Ball material	MSL rating/Peak reflow	Op temp (°C)	Part marking
XAM13E23019GTPDT	Active	Preproduction	TQFP (PDT) | 128	90 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GTPDT
XAM13E23019GTPZ	Active	Preproduction	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GTPZ
XAM13E23019GTPN	Active	Preproduction	LQFP (PN) | 80	190 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GTPN
XAM13E23019GTPM	Active	Preproduction	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GTPM
XAM13E23019GTPT	Active	Preproduction	LQFP (PT) | 48	1,000 | LARGE T&R	Yes	Call TI	Call TI	-40 to 125	19GTPT
XAM13E23019GTRGZR	Active	Preproduction	VQFN (RGZ) | 48	4,000 | LARGE T&R	Yes	Call TI	Call TI	-40 to 125	19GTRGZ
XAM13E23019HTPZ	Active	Preproduction	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19HTPZ
XAM13E23019HTPM	Active	Preproduction	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19HTPM
XAM13E23019GT2PDT	Active	Preproduction	TQFP (PDT) | 128	90 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GT2PDT
XAM13E23019GT2PZ	Active	Preproduction	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GT2PZ
XAM13E23019GT2PM	Active	Preproduction	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	Call TI	Call TI	-40 to 125	19GT2PM
XAM13E23019GT2PT	Active	Preproduction	LQFP (PT) | 48	1,000 | LARGE T&R	Yes	Call TI	Call TI	-40 to 125	19GT2PT

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ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XAM13E23019GTPDT	Active	Preproduction	TQFP (PDT) | 128	90 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	
XAM13E23019GTPM	Active	Preproduction	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	
XAM13E23019GTPN	Active	Preproduction	LQFP (PN) | 80	190 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	
XAM13E23019GTPT	Active	Preproduction	LQFP (PT) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XAM13E23019GTPZ	Active	Preproduction	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	
XAM13E23019GTRGZR	Active	Preproduction	VQFN (RGZ) | 48	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XAM13E23019HTPM	Active	Preproduction	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	
XAM13E23019HTPZ	Active	Preproduction	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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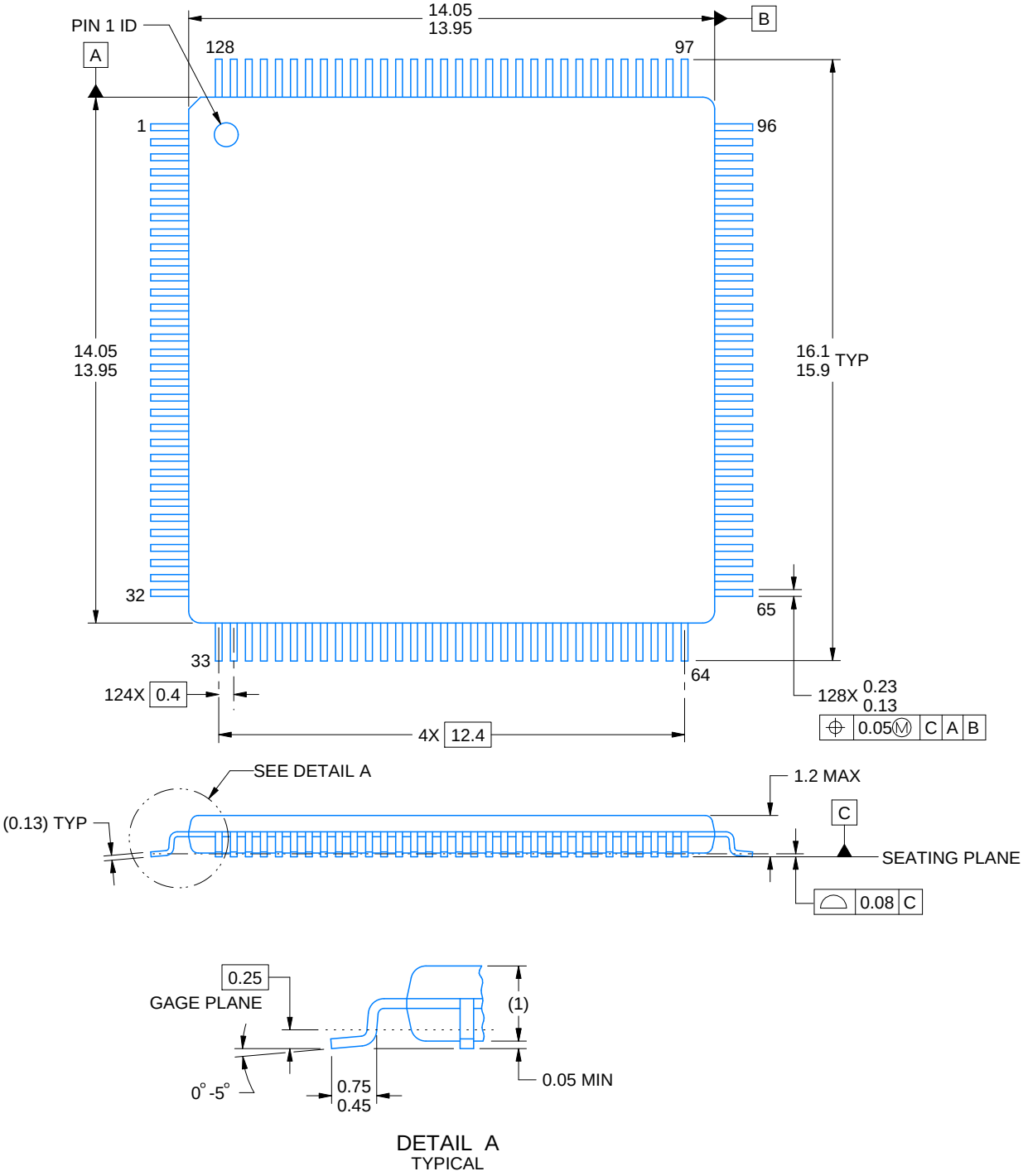
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PACKAGE OUTLINE

PDT0128A

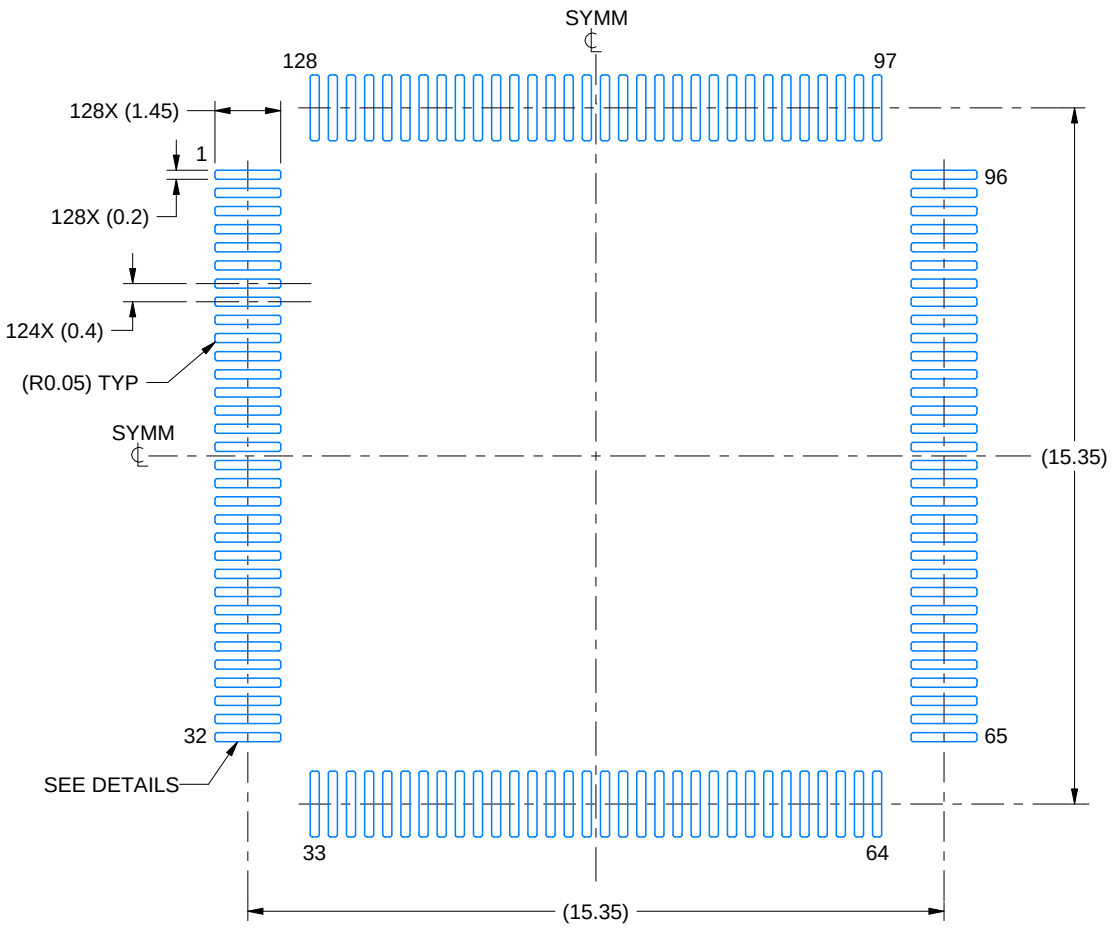
TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

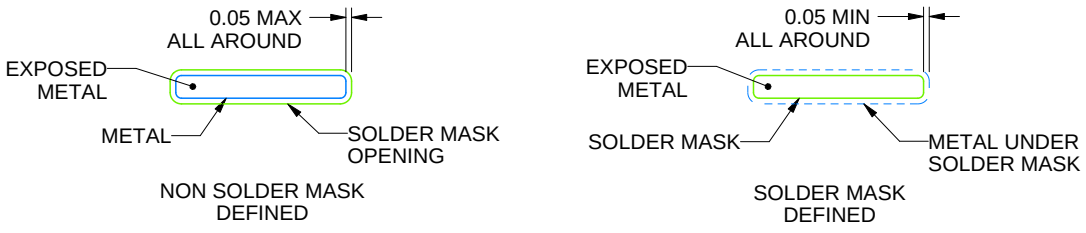


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

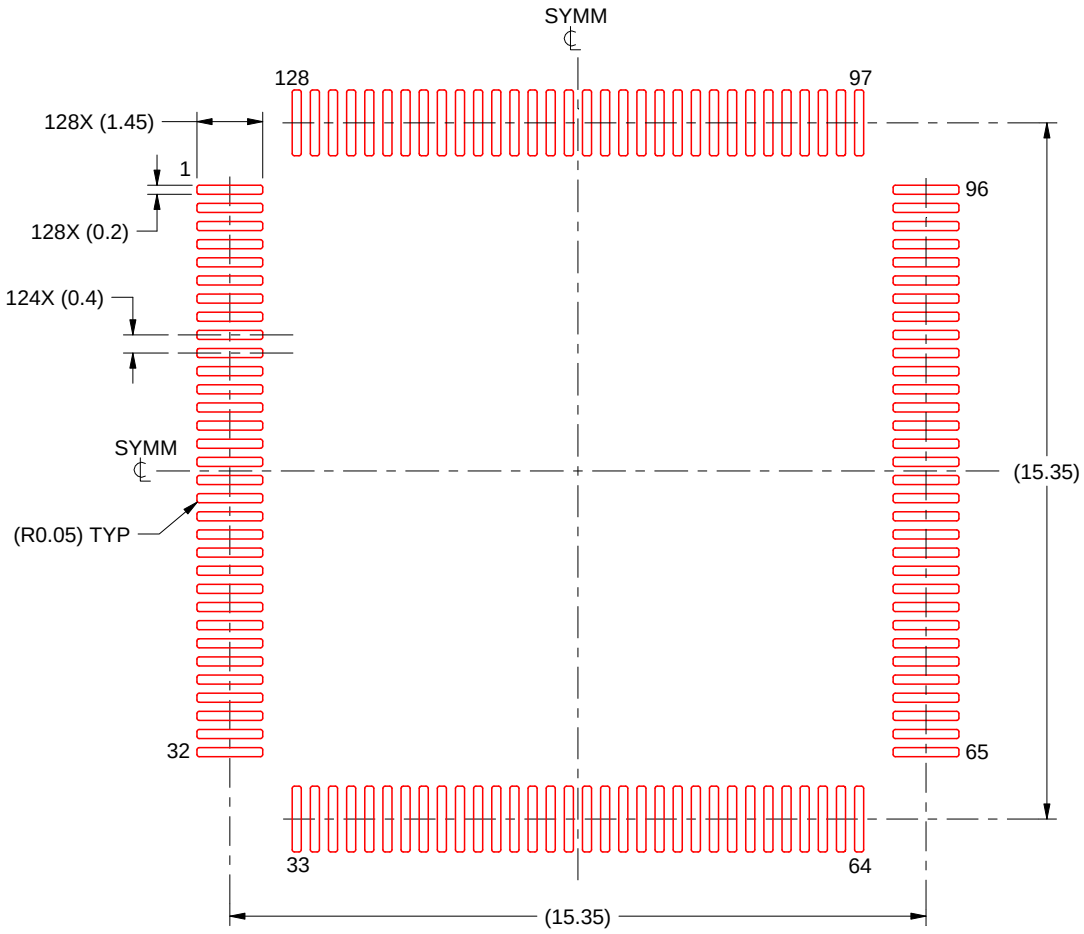


SOLDER MASK DETAILS

4215171/A 10/2023

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215171/A 10/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

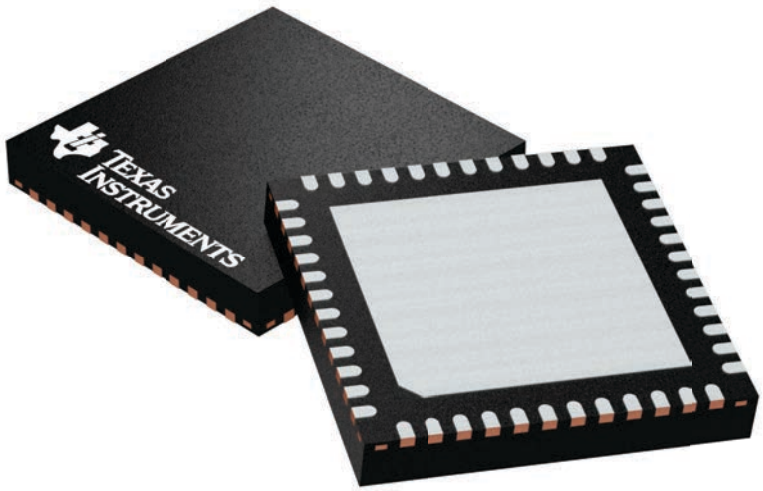
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

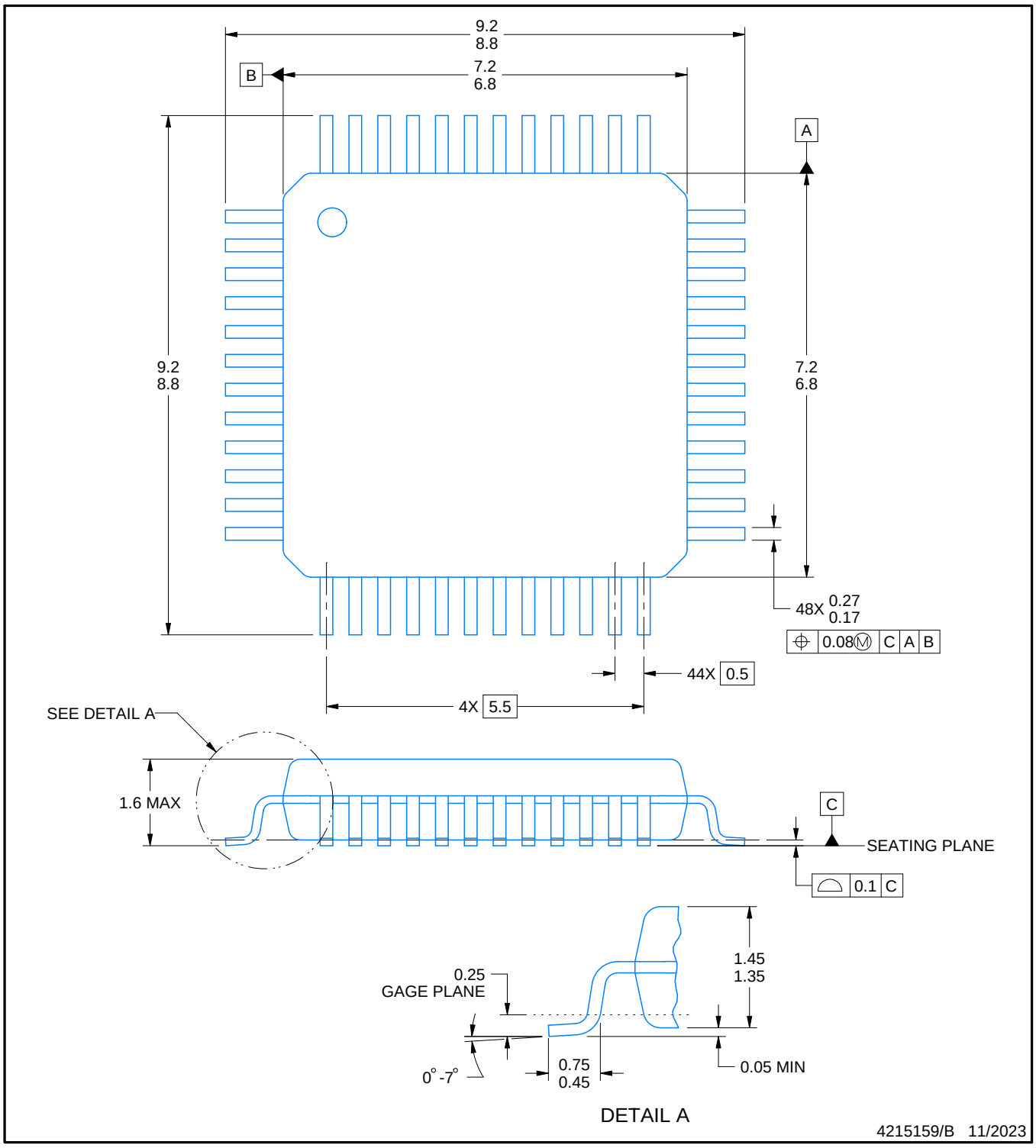
4224671/A

PACKAGE OUTLINE

PT0048A

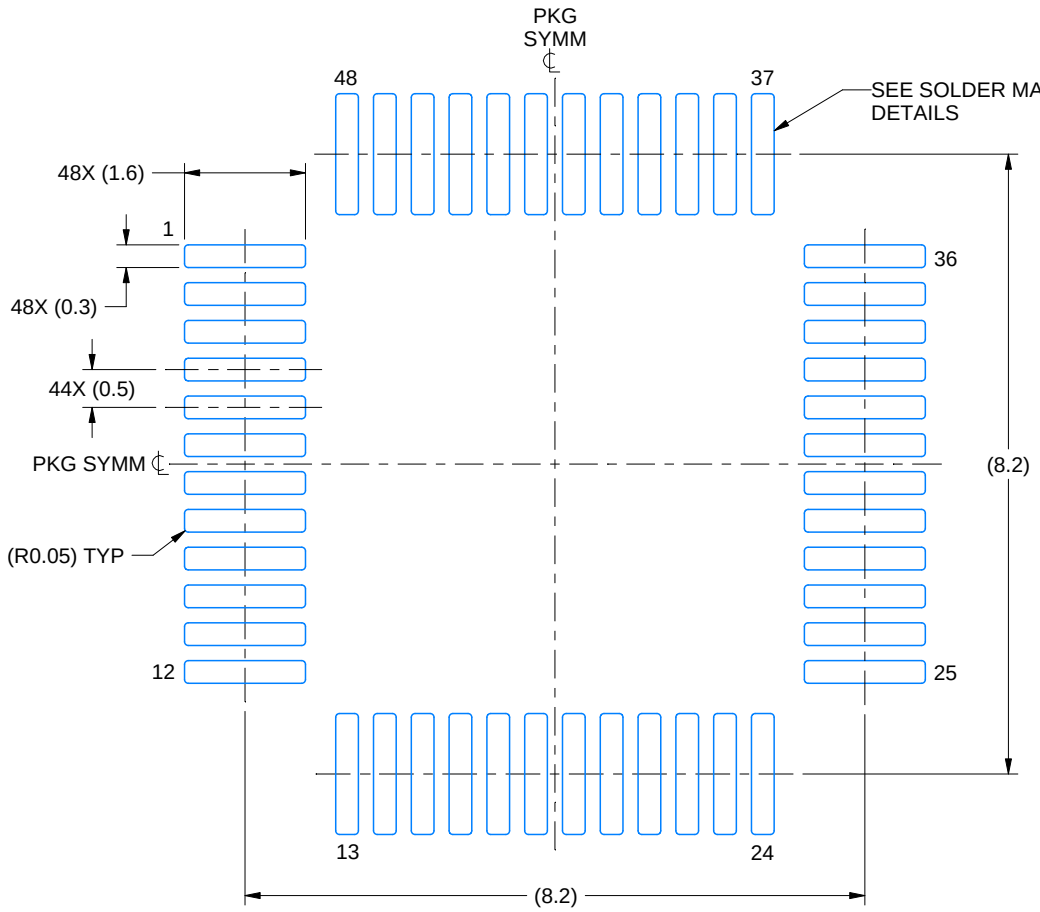
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

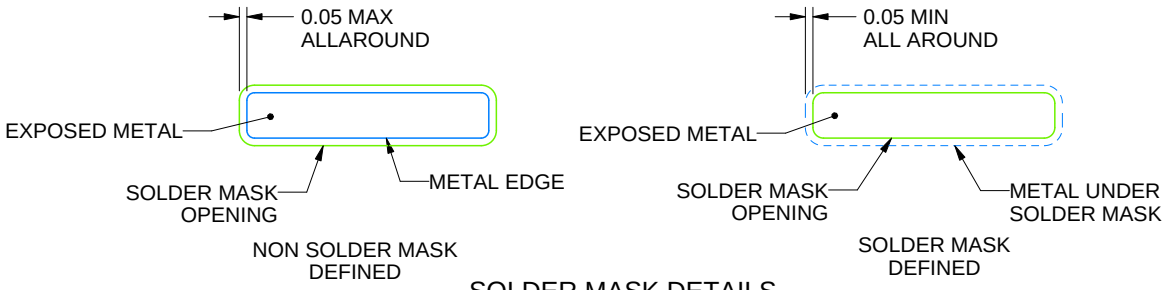


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

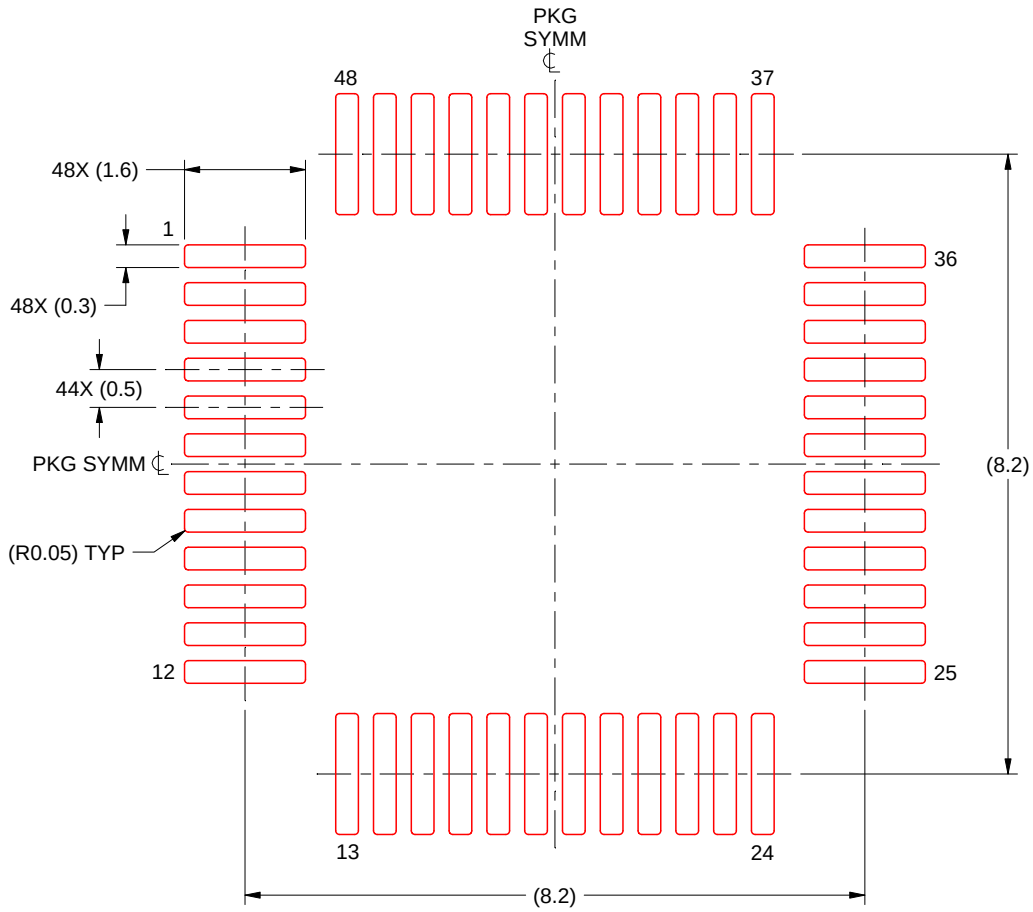


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

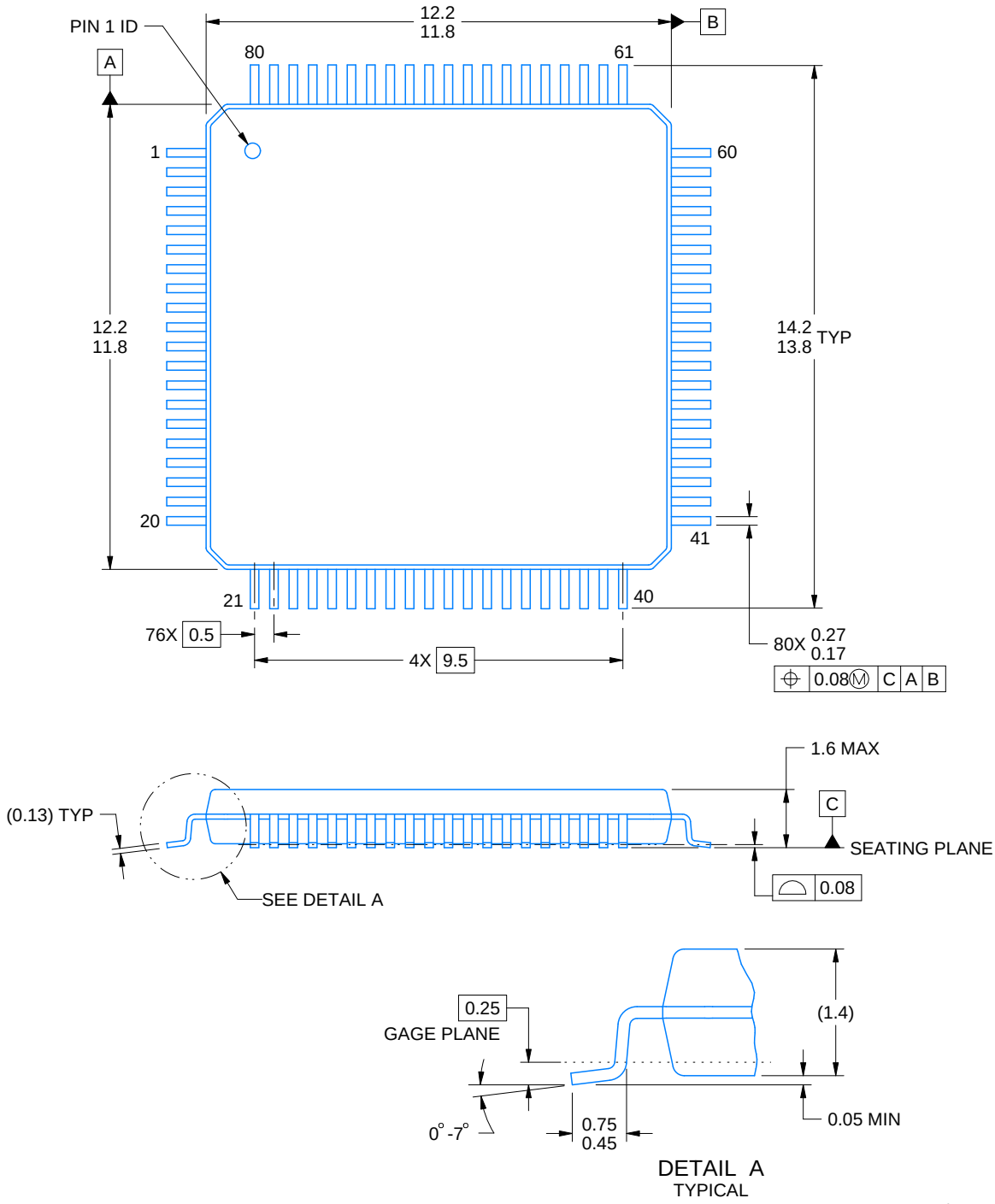
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PN0080A

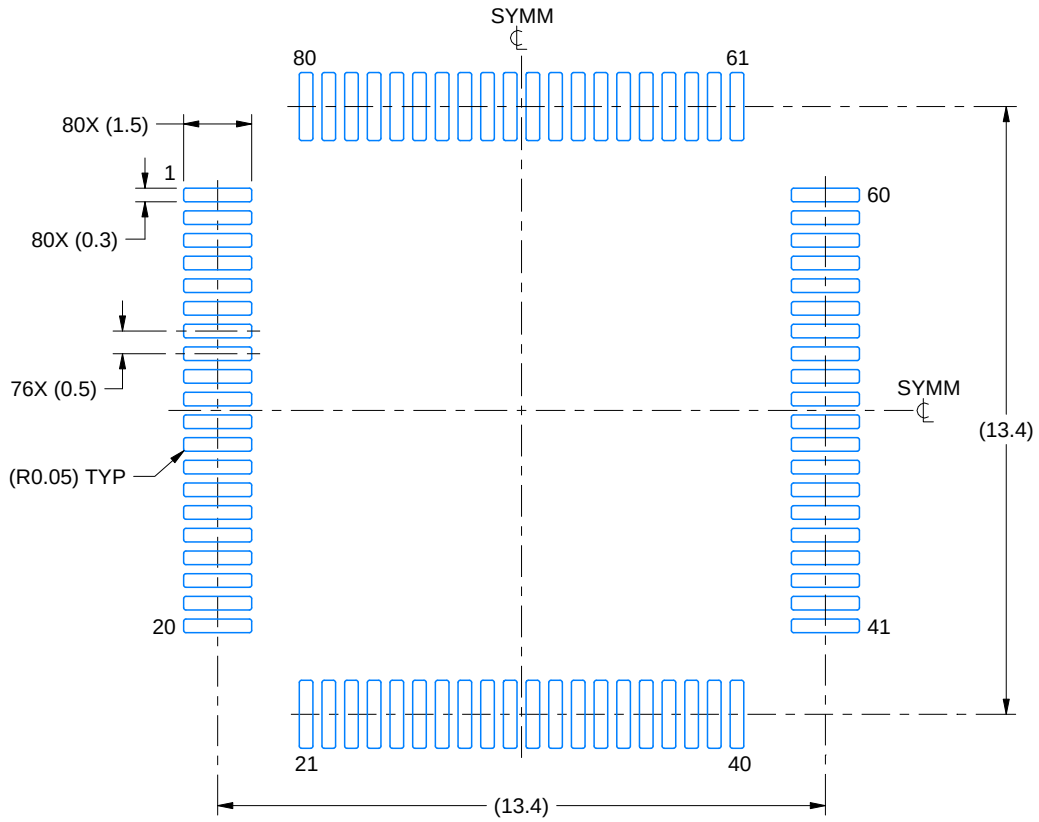
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

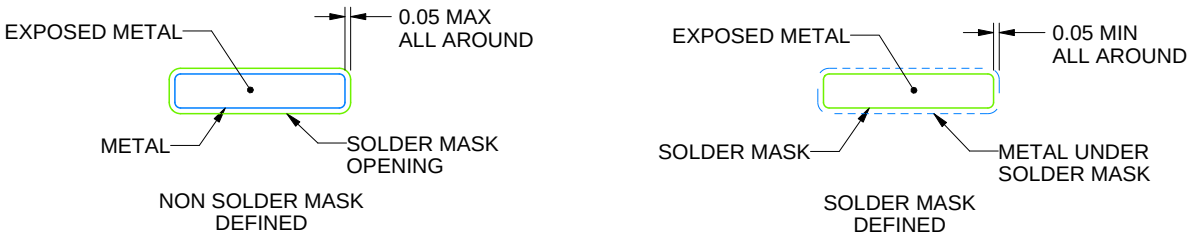


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

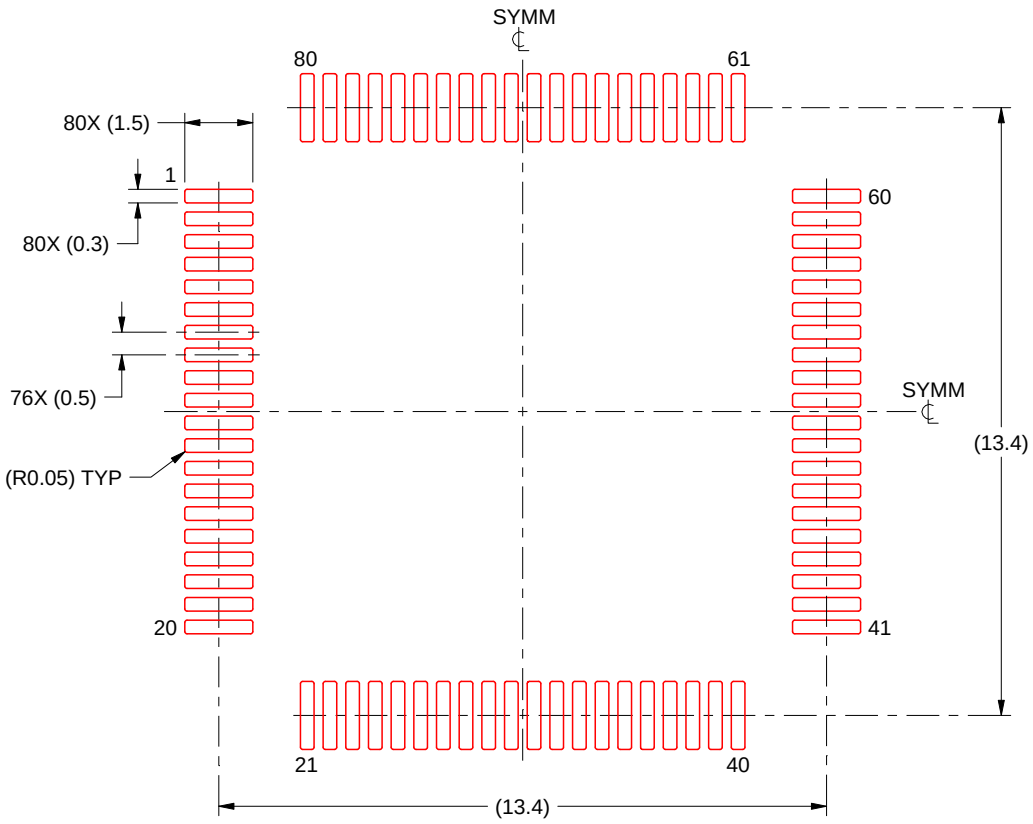


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

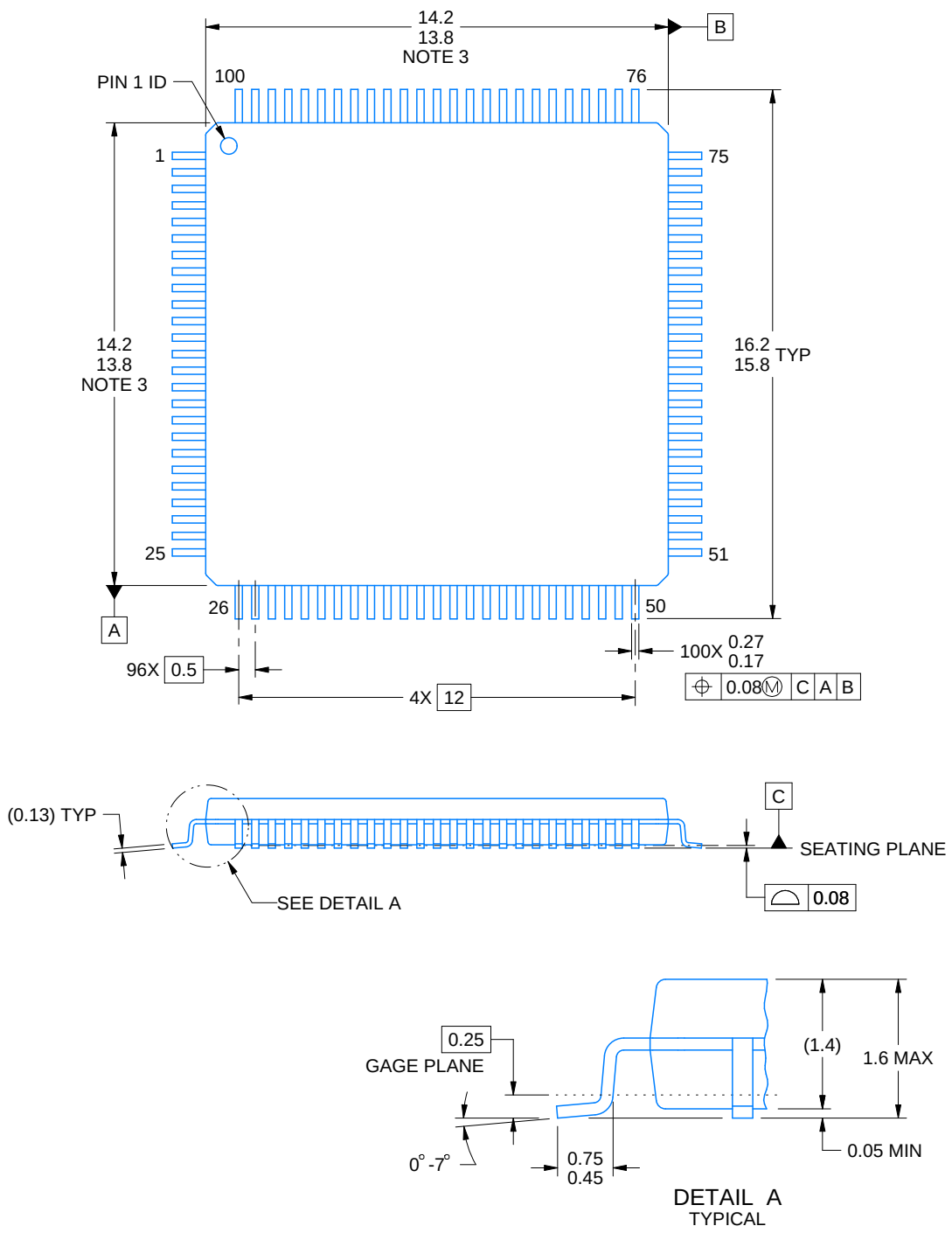
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PZ0100A

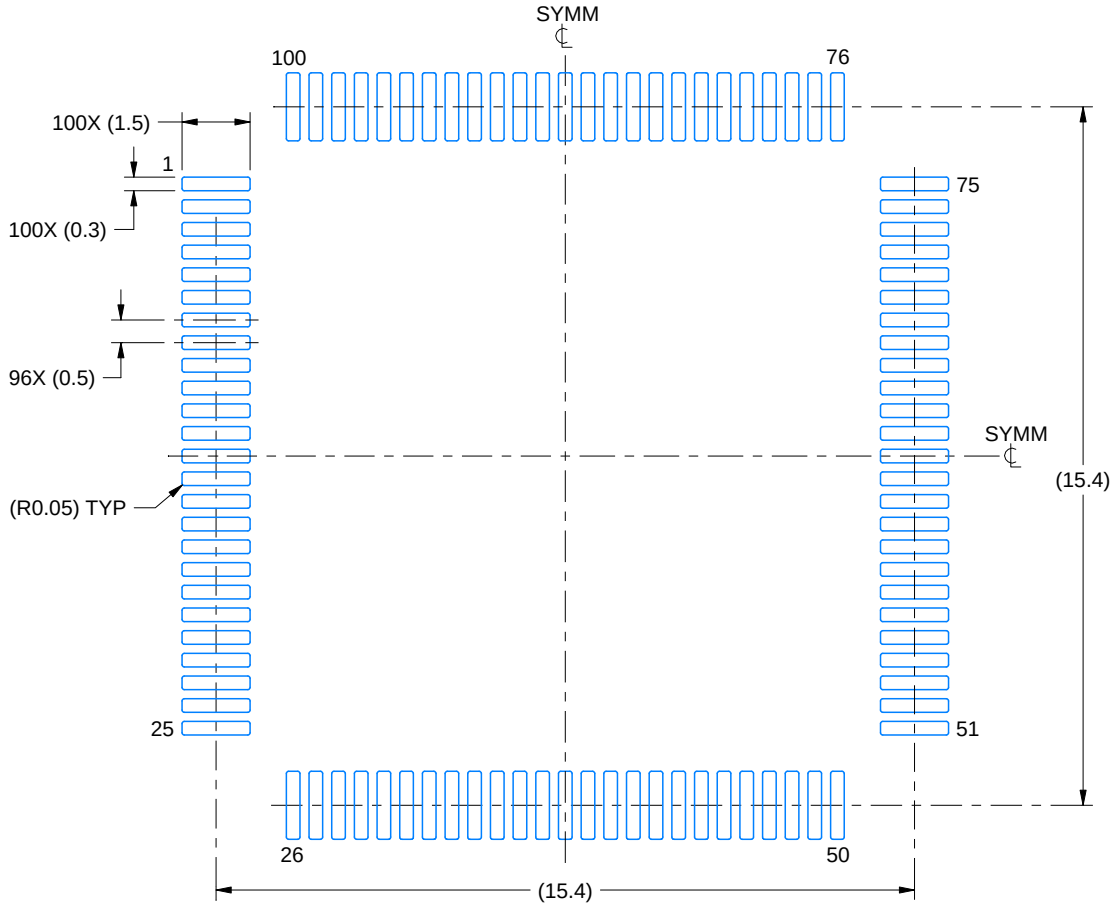
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

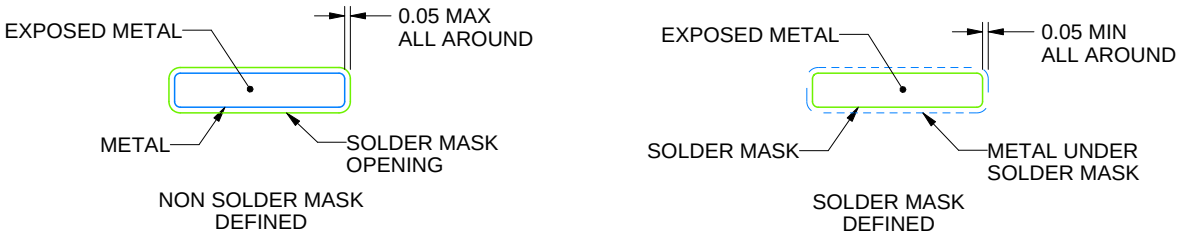


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

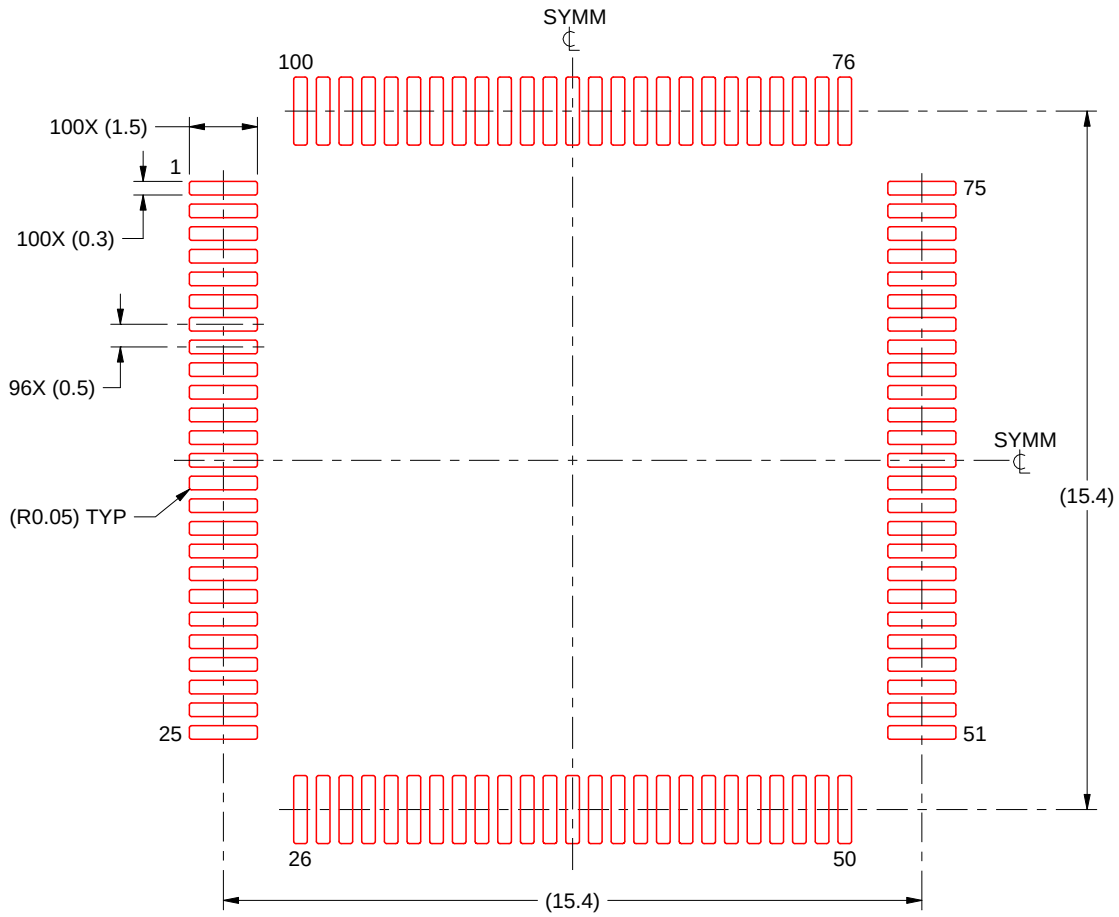


SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

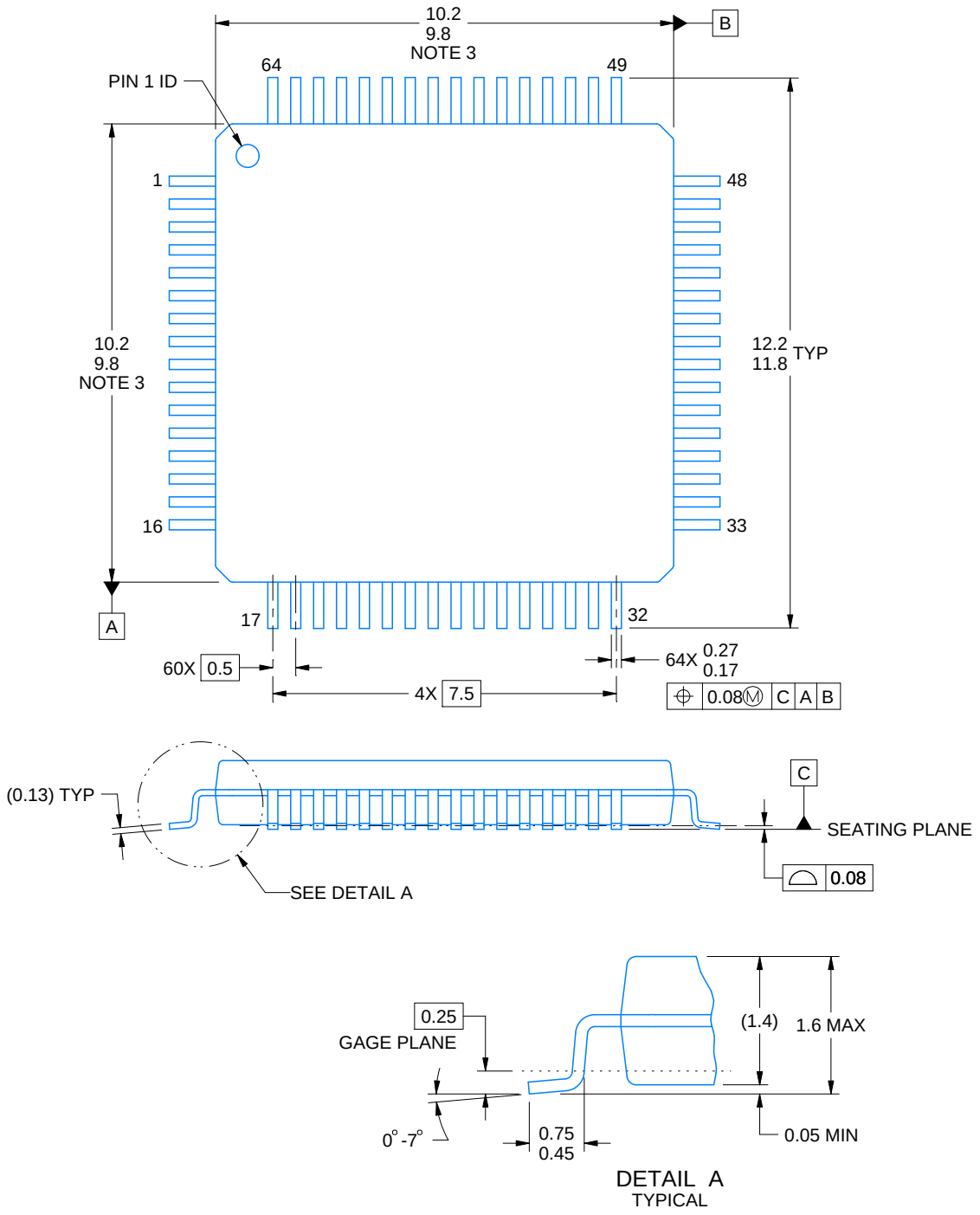
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

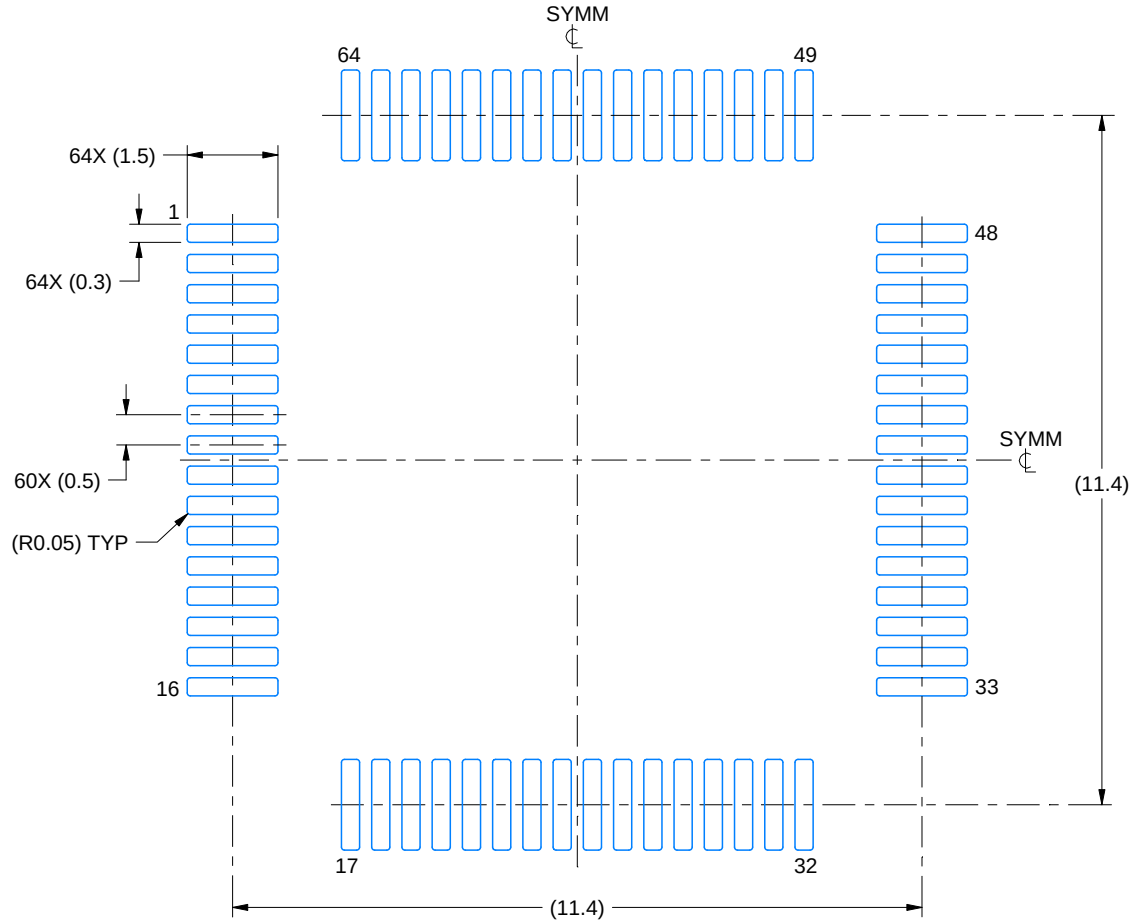
PLASTIC QUAD FLATPACK



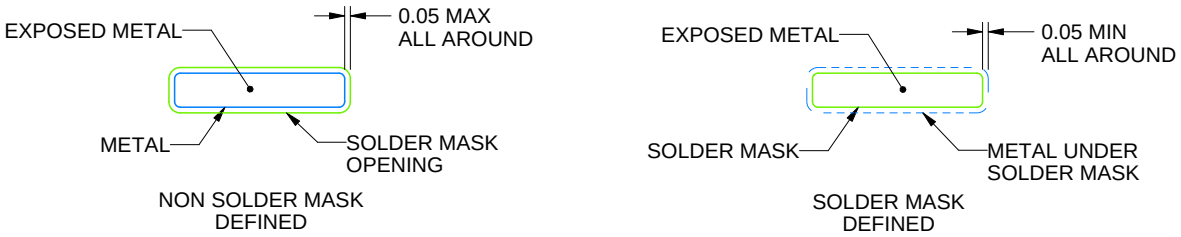
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

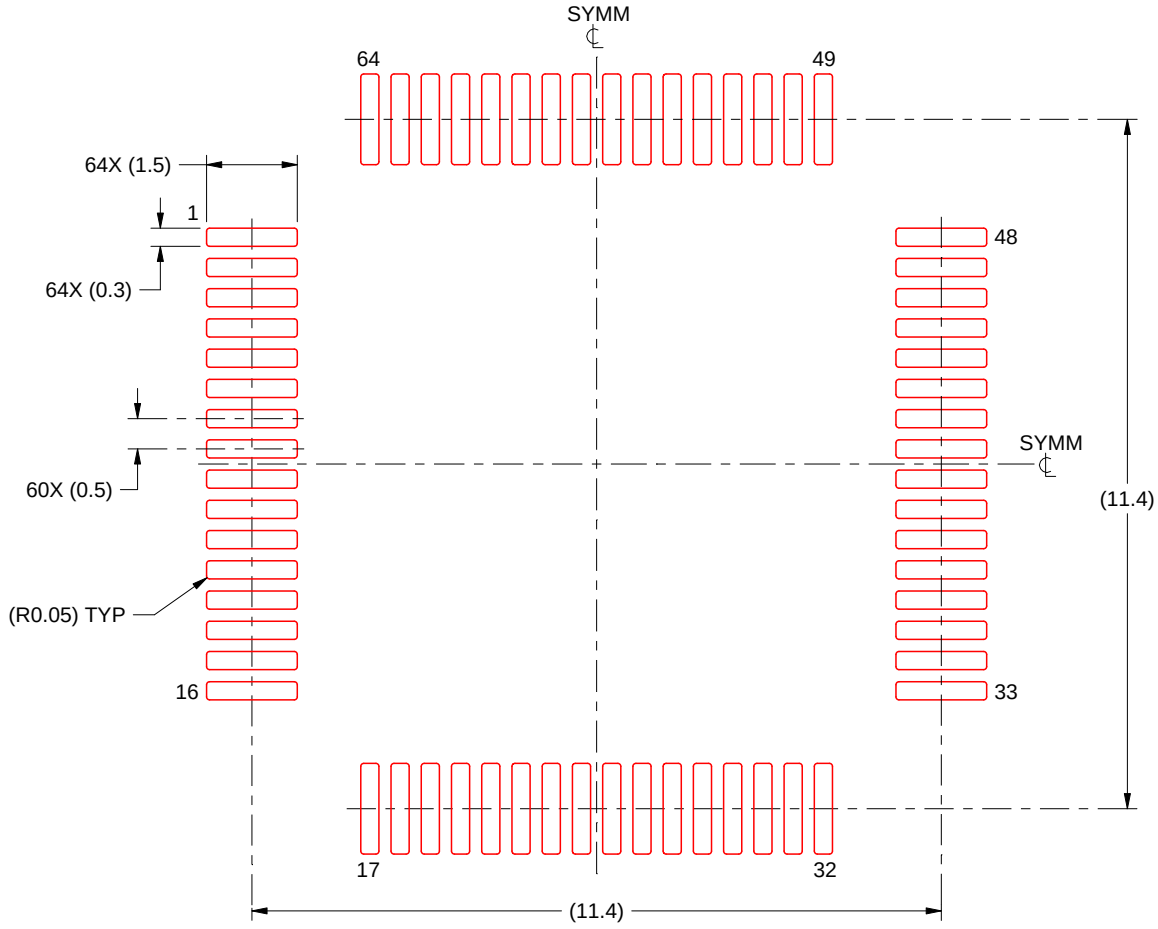


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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