

**UNITRODE**

bq2002E/G

NiCd/NiMH Fast-Charge Management ICs

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by $-\Delta V$, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002E and bq2002G Fast-Charge ICs are low-cost CMOS battery-charge controllers providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002E/G to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002E/G integrates fast charge with optional top-off and pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

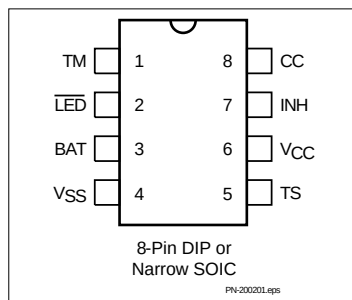
Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002E/G optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002E/G may also be placed in low-standby-power mode to reduce system power consumption.

The bq2002E differs from the bq2002G only in that a slightly different set of fast-charge and top-off time limits is available. All differences between the two ICs are illustrated in Table 1.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{\text{LED}}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

bq2002E/G Selection Guide

Part No.	LBAT	TCO	HTF	LTF	$-\Delta V$	PVD	Fast Charge	t_{MTO}	Top-Off	Maintenance
bq2002E	0.175 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	None		✓	C/2	200	None	C/32
						✓	1C	80	C/16	C/32
					✓		2C	40	None	C/32
bq2002G	0.175 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	None		✓	C/2	160	None	C/32
						✓	1C	80	C/16	C/32
					✓		2C	40	None	C/32

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Pin Descriptions

TM	Timer mode input
	A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.
LED	Charging output status
	Open-drain output that indicates the charging status.
BAT	Battery input voltage
	The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.
VSS	System ground
TS	Temperature sense input
	Input for an external battery temperature monitoring thermistor.
VCC	Supply voltage input
	5.0V ±20% power input.
INH	Charge inhibit input
	When high, INH suspends the fast charge in progress. When returned low, the IC re-

sumes operation at the point where initially suspended.

Charge control output

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002E/G.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

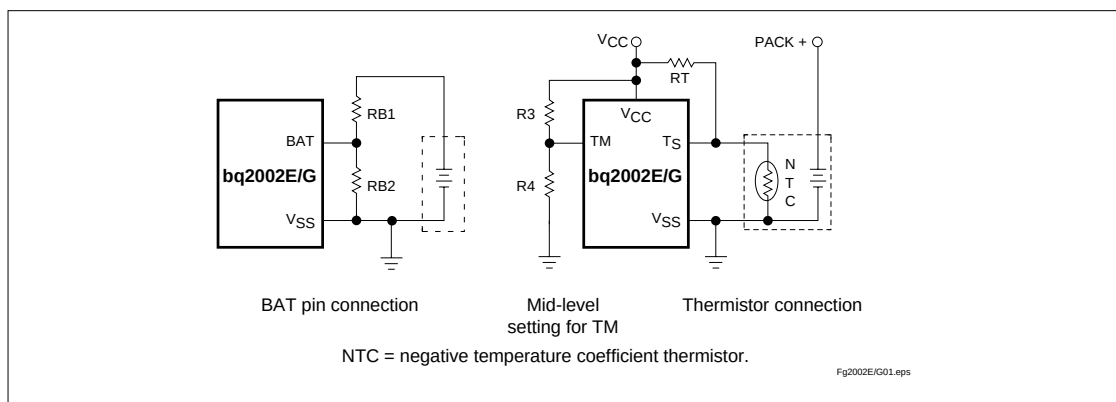


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

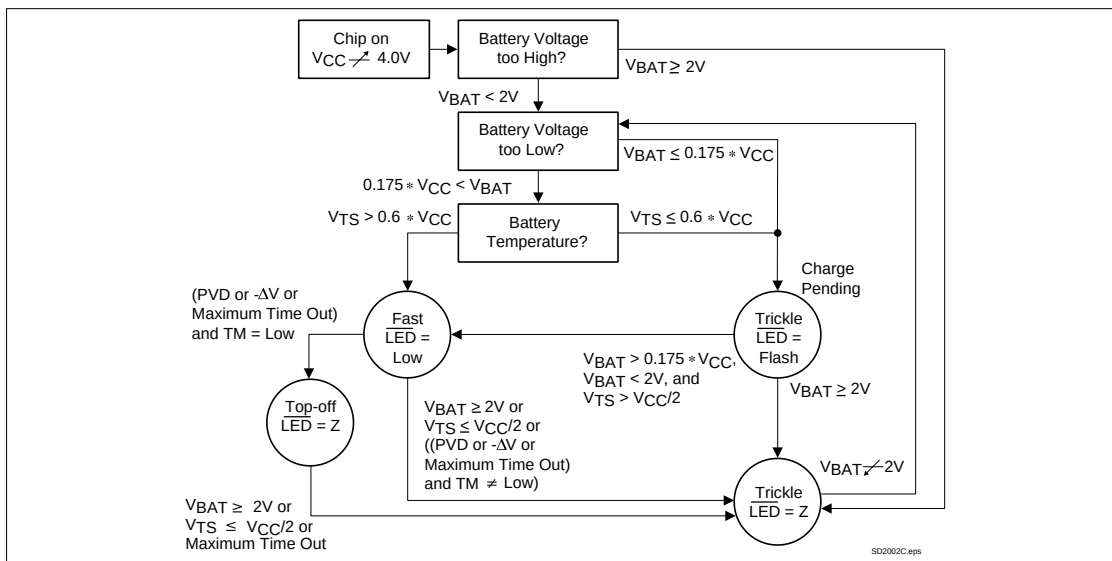


Figure 2. State Diagram

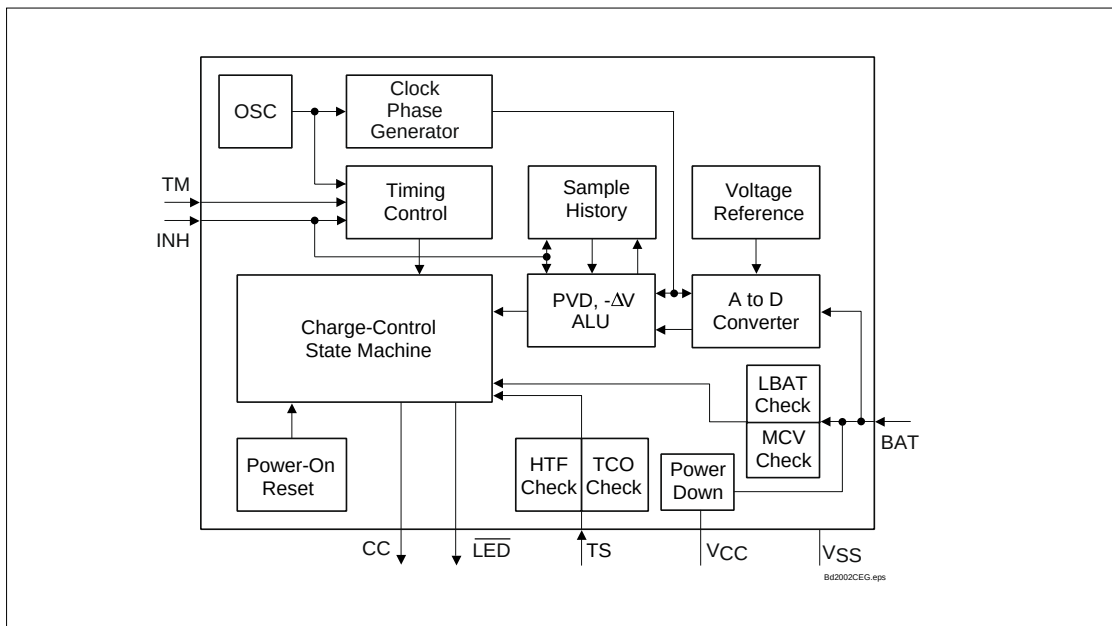


Figure 3. Block Diagram

bq2002E/G

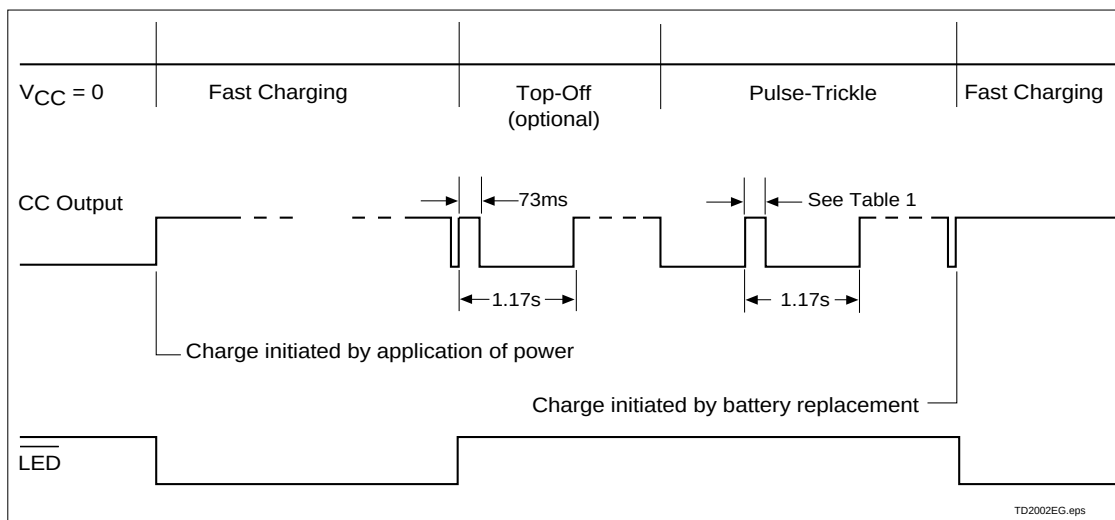


Figure 4. Charge Cycle Phases

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS} . See Figure 1.

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

1. Application of power to V_{CC} or
2. Voltage at the BAT pin falling through the maximum cell voltage V_{MCV} where

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{LBAT} < V_{BAT} < V_{MCV}$, where

Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM	Termination	Typical Fast-Charge and Top-Off Time Limits (minutes)		Typical PVD and ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Width (ms)	Maximum Synchronized Sampling Period (seconds)
			bq2002E	bq2002G					
C/2	Mid	PVD	200	160	300	Disabled	C/32	73	18.7
1C	Low	PVD	80	80	150	C/16	C/32	37	18.7
2C	High	ΔV	40	40	75	Disabled	C/32	18	9.4

Notes: Typical conditions = 25°C, $V_{CC} = 5.0V$
Mid = $0.5 * V_{CC} \pm 0.5V$
Tolerance on all timing is $\pm 12\%$.

$$V_{\text{LBAT}} = 0.175 * V_{\text{CC}} \pm 20\%$$

The valid temperature range is $V_{\text{TS}} > V_{\text{HTF}}$ where

$$V_{\text{HTF}} = 0.6 * V_{\text{CC}} \pm 5\%.$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the next new charge cycle begins.

If $V_{\text{MCV}} < V_{\text{BAT}} < V_{\text{PD}}$ (see “Low-Power Mode”) when a new battery is inserted, a delay of 0.35 to 0.9s is imposed before the new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and $-\Delta V$ Termination

There are two modes for voltage termination, depending on the state of TM. For $-\Delta V$ (TM = high), if V_{BAT} is lower than any previously measured value by $12\text{mV} \pm 3\text{mV}$, fast charge is terminated. For PVD (TM = low or mid), a decrease of $2.5\text{mV} \pm 2.5\text{mV}$ terminates fast charge. The PVD and $-\Delta V$ tests are valid in the range $1\text{V} < V_{\text{BAT}} < 2\text{V}$.

Synchronized Voltage Sampling

Voltage sampling at the BAT pin for PVD and $-\Delta V$ termination may be synchronized to an external stimulus using the INH input. Low-high-low input pulses between 100ns and 3.5ms in width must be applied at the INH pin with a frequency greater than the “maximum synchronized sampling period” set by the state of the TM pin as shown in Table 1. Voltage is sampled on the falling edge of such pulses.

If the time between pulses is greater than the synchronizing period, voltage sampling “free-runs” at once every 17 seconds. A sample is taken by averaging together voltage measurements taken $57\mu\text{s}$ apart. The IC takes 32 measurements in PVD mode and 16 measurements in $-\Delta V$ mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources.

If the INH input remains high for more than 12ms, the voltage sample history kept by the IC and used for PVD and $-\Delta V$ termination decisions is erased and a new history is started. Such a reset is required when transitioning from free-running to synchronized voltage sampling.

The response of the IC to pulses less than 100ns in width or between 3.5ms and 12ms is indeterminate. Tolerance on all timing is $\pm 12\%$.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and $-\Delta V$ terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage, V_{MCV} , fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{Tco} where

$$V_{\text{Tco}} = 0.5 * V_{\text{CC}} \pm 5\%.$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/2 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge before reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 73ms active for every 1097ms inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active once every 1.17s for the period specified in Table 1. This results in a trickle rate of C/32.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle

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rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge. Figure 2 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002E/G continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current is reduced to less than $1\mu A$ in this mode. When V_{BAT} returns to a value below V_{PD} , the IC pulse-trickle charges until the next new charge cycle begins.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V _{CC}	V _{CC} relative to V _{SS}	-0.3	+7.0	V	
V _T	DC voltage applied on any pin excluding V _{CC} relative to V _{SS}	-0.3	+7.0	V	
T _{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T _{STG}	Storage temperature	-40	+85	°C	
T _{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T _{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V _{TCO}	Temperature cutoff	0.5 * V _{CC}	±5%	V	V _{TS} ≤ V _{TCO} inhibits/terminates fast charge and top-off
V _{HTF}	High temperature fault	0.6 * V _{CC}	±5%	V	V _{TS} < V _{HTF} inhibits fast charge start
V _{MCV}	Maximum cell voltage	2	±5%	V	V _{BAT} ≥ V _{MCV} inhibits/terminates fast charge and top-off
V _{LBAT}	Minimum cell voltage	0.175 * V _{CC}	±20%	V	V _{BAT} < V _{LBAT} inhibits fast charge start
-ΔV	BAT input change for -ΔV detection	-12	±3	mV	
PVD	BAT input change for PVD detection	-2.5	±2.5	mV	

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Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V _{CC}	Supply voltage	4.0	5.0	6.0	V	
V _{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V _{BAT}	Battery input	0	-	V _{CC}	V	
V _{TS}	Thermistor input	0.5	-	V _{CC}	V	V _{TS} < 0.5V prohibited
V _{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V _{CC} - 0.5	-	-	V	TM
V _{IM}	Logic input mid	$\frac{V_{CC}}{2} - 0.5$	-	$\frac{V_{CC}}{2} + 0.5$	V	TM
V _{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V _{OL}	Logic output low	-	-	0.8	V	$\overline{\text{LED}}$, CC, I _{OL} = 10mA
V _{PD}	Power down	V _{CC} - 1.5	-	V _{CC} - 0.5	V	V _{BAT} ≥ V _{PD} max. powers down bq2002E/G; V _{BAT} < V _{PD} min. = normal operation.
I _{CC}	Supply current	-	-	500	μA	Outputs unloaded, V _{CC} = 5.1V
I _{SB}	Standby current	-	-	1	μA	V _{CC} = 5.1V, V _{BAT} = V _{PD}
I _{OL}	$\overline{\text{LED}}$, CC sink	10	-	-	mA	@V _{OL} = V _{SS} + 0.8V
I _L	Input leakage	-	-	±1	μA	INH, CC, V = V _{SS} to V _{CC}
I _{OZ}	Output leakage in high-Z state	-5	-	-	μA	$\overline{\text{LED}}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R _{BAT}	Battery input impedance	50	-	-	MΩ
R _{TS}	TS input impedance	50	-	-	MΩ

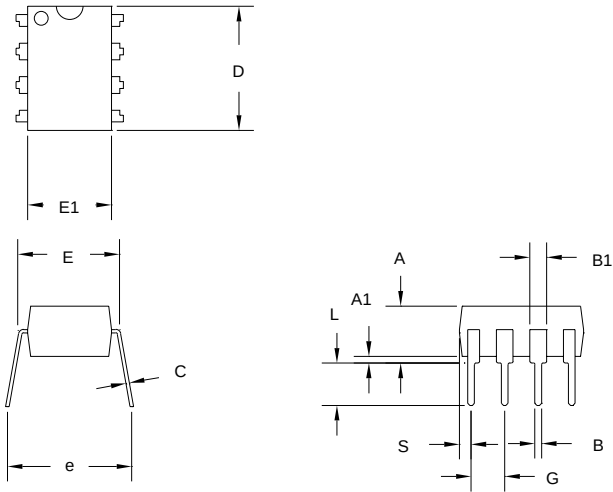
Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d _{FCV}	Time base variation	-12	-	12	%	
t _{DLY}	Start-up delay	0.35	-	0.9	s	Starting from V _{MCV} < V _{BAT} < V _{PD}

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

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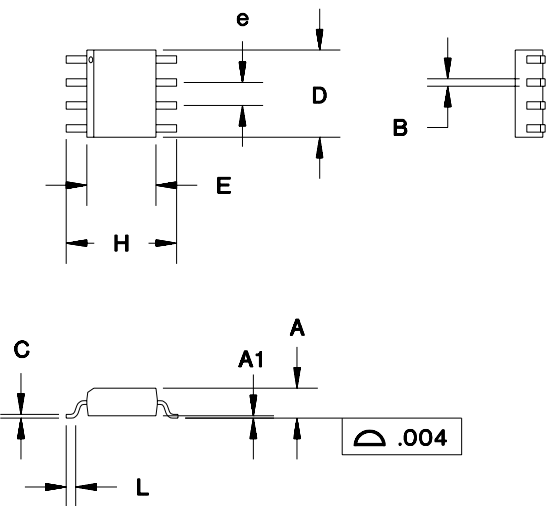
8-Pin DIP (PN)



8-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

8-Pin SOIC Narrow (SN)



8-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.185	0.200	4.70	5.08
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2002ESN	Last Time Buy	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002E
BQ2002ESN.B	Last Time Buy	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002E
BQ2002ESNTR	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002E
BQ2002ESNTR.B	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002E
BQ2002GSN	Last Time Buy	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002G
BQ2002GSN.B	Last Time Buy	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2002G
BQ2002GSNTR	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2002G
BQ2002GSNTR.B	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2002G

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

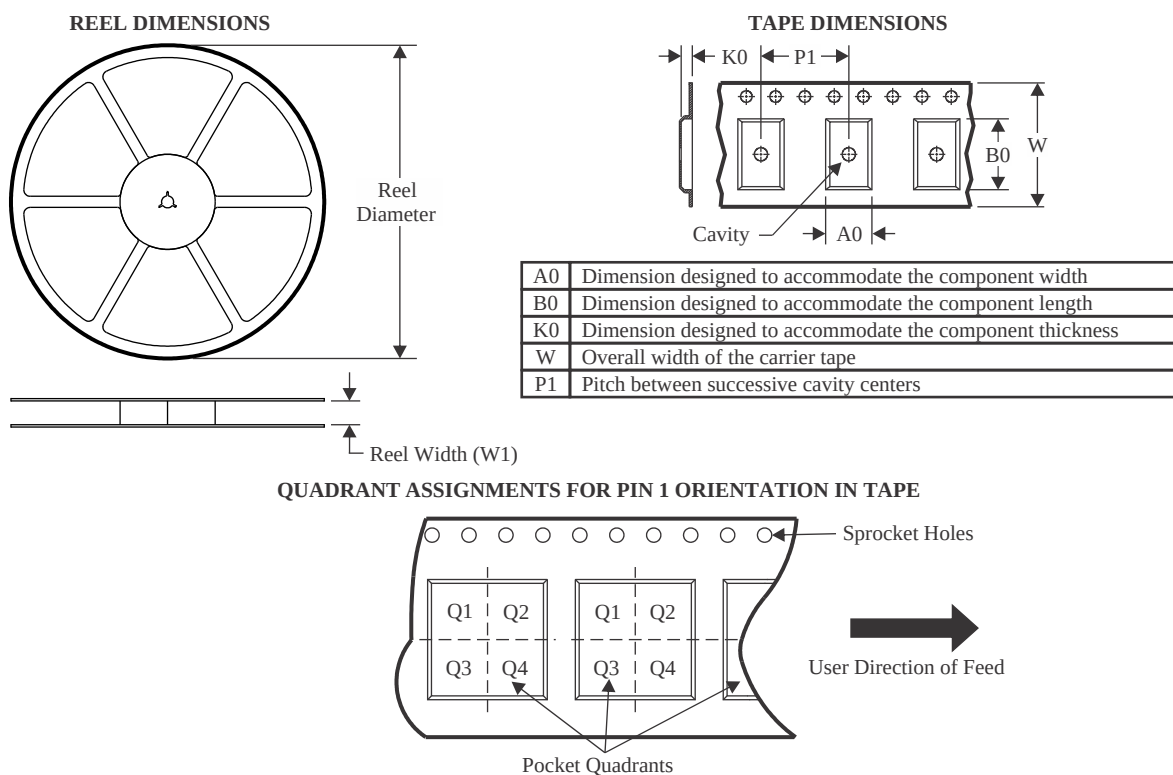
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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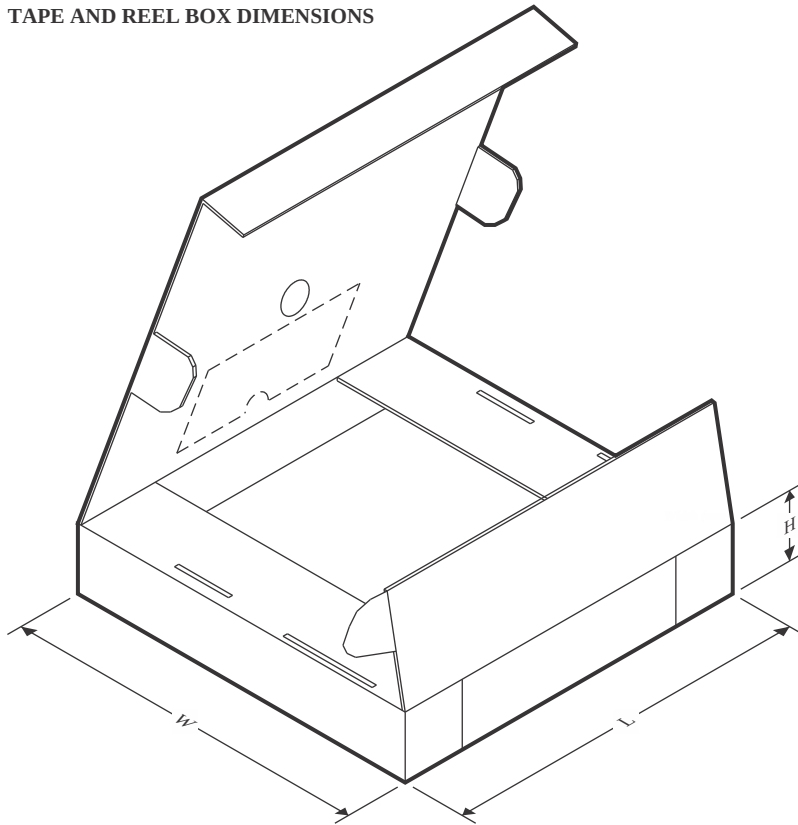
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2002ESNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ2002GSNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

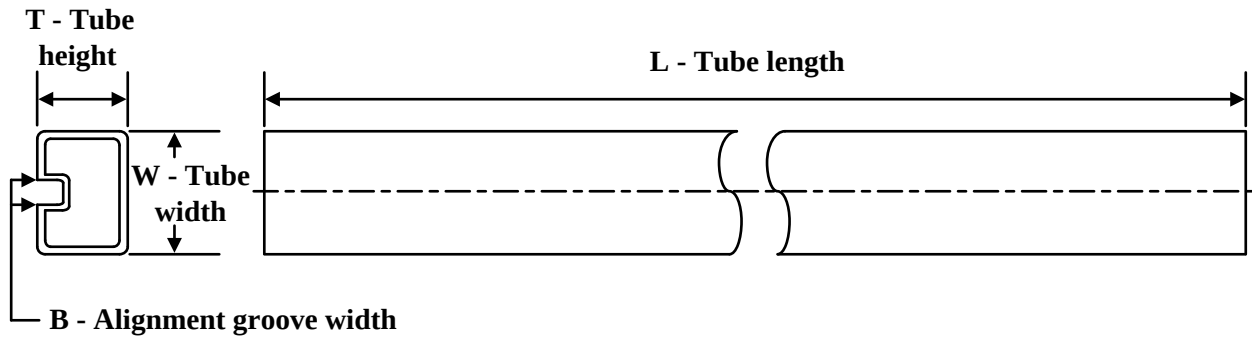
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

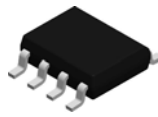
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2002ESNTR	SOIC	D	8	2500	353.0	353.0	32.0
BQ2002GSNTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ2002ESN	D	SOIC	8	75	507	8	3940	4.32
BQ2002ESN.B	D	SOIC	8	75	507	8	3940	4.32
BQ2002GSN	D	SOIC	8	75	507	8	3940	4.32
BQ2002GSN.B	D	SOIC	8	75	507	8	3940	4.32

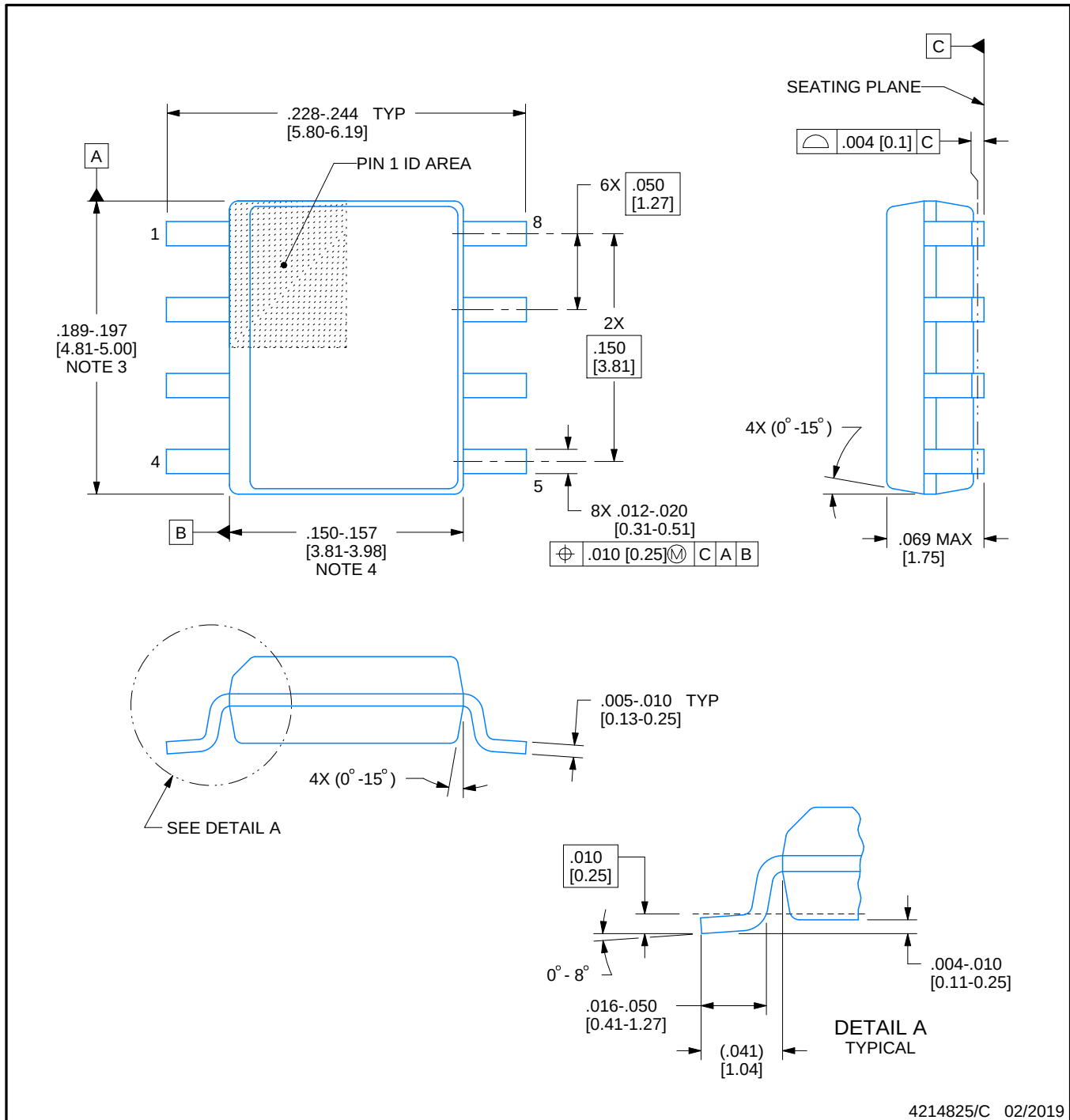


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PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

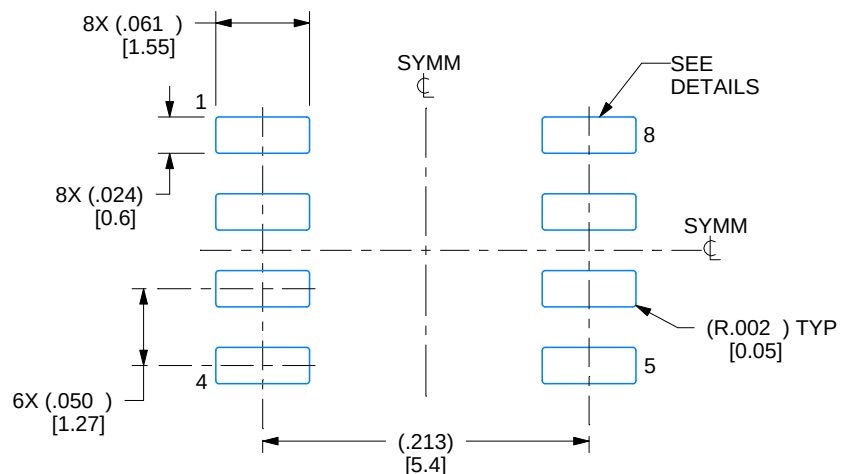
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

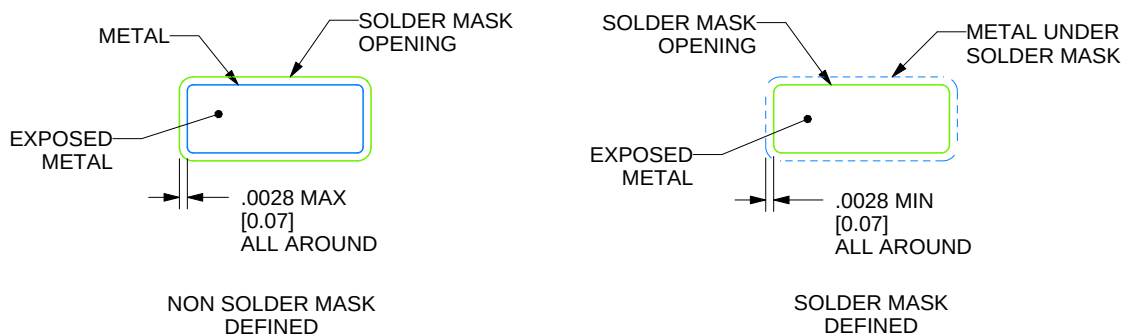
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

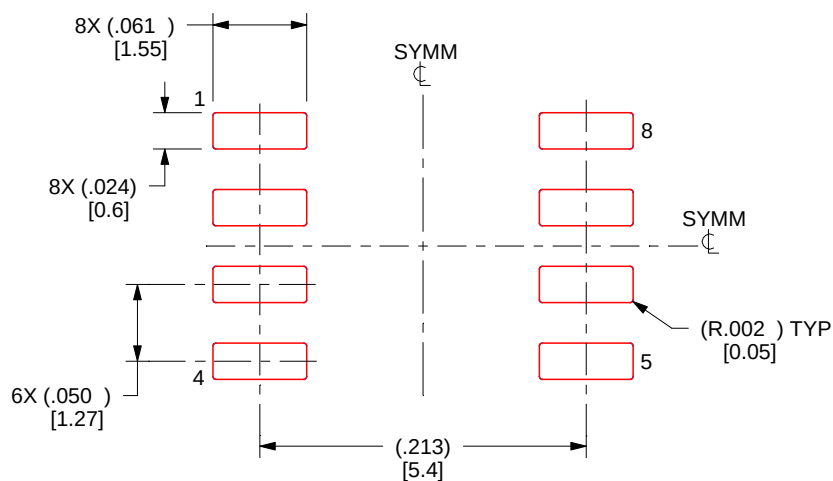
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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