BQ25350 I²C Controlled, 3A, Single Cell Integrated Buck-Boost Charger with NVDC Power Path Management

1 Features

- High-efficiency 3A synchronous buck-boost charger for single cell battery
  - Seamless automatic transition between Buck, Buck-Boost, and Boost operation
  - Charge current up to 3A in 20mA steps
  - Charge termination from 20 to 1000mA in 5mA steps
  - Flexible JEITA profile for safe charging over temperature and high configurability
  - Selectable switching frequency between 1MHz and 2MHz
- >95% peak efficiency
  - 95.9% efficiency when VBUS = 4.2V, VBAT = 3.6V, ICHG = 1A
  - 94.8% efficiency when VBUS = 4.2V, VBAT = 3.6V, ICHG = 2A
- NVDC power path management with high efficiency 15mΩ BATFET
  - System instant-on with depleted or no battery
  - Battery supplement when adapter is fully loaded
- 2.5V to 5.5V input voltage range
- Programmable VINDPM
  - 2.48 to 5V in 40mV steps
- BATFET control to support shutdown mode, standby mode, and full system reset
- Ultra low IQ
  - 2.5μA in battery-only mode
  - 0.16μA in shutdown mode
  - 0.6μA in standby mode
- High accuracy voltage/current regulation
  - ±0.4% charge voltage regulation
  - ±5% charge current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input, system, battery overvoltage protection
  - Battery, converter overcurrent protection
  - Charging safety timer

2 Applications

- Portable electronics
- Digital video camera, EPOS
- Portable speakers, wearables, microphones

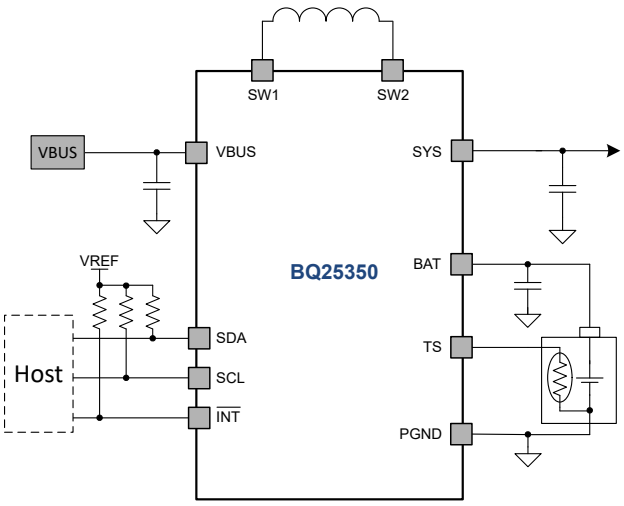
3 Description

BQ25350 is a highly-integrated 3A switch-mode battery charge management and system power-path management device for single cell Li-Ion and Li-polymer batteries. It provides high efficiency charging with a small solution size and low component count. BQ25350 operates over a 2.5V to 5.5V input range with seamless transition between Buck, Buck-Boost, and Boost modes. It uses NVDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. BQ25350 provides critical charging safety protections including battery temperature monitoring, charging safety timers, over-voltage and over-current protections. Charging and safety settings are highly configurable via the I²C serial bus, making BQ25350 a truly flexible solution.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BQ25350	YBG (DSBGA 16)	2.06mm × 2.06mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



BQ25350 Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

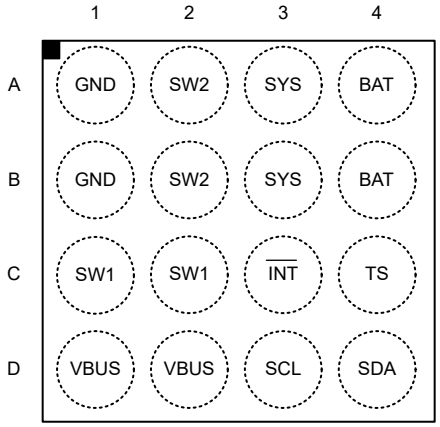


Figure 4-1. BQ25350 Pinout, 16-Ball YBG DSBGA Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BAT	A4	P	**Positive Terminal of Battery Pack Connection** – The internal BATFET is connected between SYS and BAT. Connect a 10µF ceramic capacitor closely to the BAT pin and GND.
	B4		
GND	A1	P	**Ground Return**
	B1		
$\overline{INT}$	C3	DO	**Open Drain Active Low Interrupt Output** – Connect /INT to the logic rail via a 10kΩ resistor. The INT pin sends an active low, 256µs pulse to the host to report charger device status and fault.
SCL	D3	DI	**I 2C Interface Clock** – Connect SCL to the logic rail through a 10kΩ resistor
SDA	D4	DIO	**I 2C Interface Data** – Connect SDA to the logic rail through a 10kΩ resistor.
SW1	C1	P	**Buck Side Switching Node** – Connect inductor from SW1 to SW2
	C2		
SW2	A2	P	**Boost Side Switching Node** – Connect inductor from SW1 to SW2
	B2		
SYS	A3	P	**Charger Output Voltage to System** – Output connection point to the system. The internal BATFET is connected between SYS and BAT. Connect a 22µF ceramic capacitor close to the SYS pin. For 1MHz switching, 2 × 22µF capacitors are recommended.
	B3		
TS	C4	AI	**Temperature Qualification Voltage Input** – Connect a negative temperature coefficient thermistor from TS to GND. If thermistor sensing is not required, connect a 10kΩ resistor from TS to GND.
VBUS	D1	P	**Charger Input Voltage** – Use at least 2 × 22µF ceramic capacitor close to VBUS, connected from VBUS to GND.
	D2		

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (converter not switching)	–0.3	7.5	V
	BAT, SYS	–0.3	6	V
	SW1, SW2	–2 (50ns)	6	V
	$\overline{INT}$, SCL, SDA, TS	–0.3	6	V
Differential Voltage	SYS-BAT	–0.3	6	V
Output Sink Current	$\overline{INT}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	2.5		5.5	V
V_{BAT}	Battery voltage			4.8	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			3	A
I_{BAT}	Fast charging current			3	A
I_{BAT}	RMS discharge current (continuously)			5	A
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C
L_{SW}	Inductor for the switching regulator, SET_CONV_FREQ=0 (1MHz)	0.4	0.47	1.5	µH
L_{SW}	Inductor for the switching regulator, SET_CONV_FREQ=1 (2MHz)	0.15	0.22	0.4	µH
C_{VBUS}	VBUS capacitor (without de-rating)	44			µF
C_{SYS}	SYS capacitor (without de-rating)	22			µF
C_{BAT}	BAT capacitor (without de-rating)	10			µF

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5.4 Thermal Information

THERMAL METRIC(1)		BQ25350 YBG (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (BQ25350EVM)	20.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, system is powered by battery. -40 °C < T_J < 60 °C		2.5	4	µA
$I_{Q_BAT_SD}$	Quiescent battery current (BAT) when the charger is in shutdown mode	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in shutdown mode, T_J < 60 °C		0.16	0.3	uA
$I_{Q_BAT_STANDBY}$	Quiescent battery current (BAT) when the charger is in standby	VBAT = 4V, No VBUS, BATFET is disabled, I2C enabled, in standby mode, T_J < 60 °C		0.6	1	uA
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 4V, VBAT = 3.8V, TS float, converter not switching		1.4		mA
		VBUS = 4V, VBAT = 4V, charge disabled, converter switching, ISYS = 0A, PFM enabled, TS float		1.8		mA
I_{SD_VBUS}	Quiescent input current (VBUS) in HIZ	VBUS = 4V, VBAT = 4V, HIZ mode		1.6	3	µA
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		2.5		5.5	V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling		1.7	2	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising		2.3	2.6	V
$V_{VBUS_PRESENT}$	VBUS rising threshold to enable converter	VBUS rising	2.45	2.6	2.75	V
$V_{VBUS_PRESENTZ}$	VBUS falling threshold to disbale converter	VBUS falling	2.25	2.4	2.55	V
V_{VBUS_EXITSD}	VBUS rising threshold to exit shutdown mode	T_J = 0℃ to 85℃		2.15	2.65	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.0	6.1	6.2	V
		VBUS rising, VBUS_OVP = 1	5.5	5.6	5.7	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 0	5.7	5.8	5.9	V
		VBUS falling, VBUS_OVP = 1	5.2	5.3	5.4	V
V_{BAT_UVLOZ}	BAT voltage for active I2C, turn on BATFET, no VBUS	VBAT rising		2.25	2.45	V

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V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_UVLO}	BAT voltage to turnoff I2C, turn off BATFET, no VBUS	VBAT falling	1.55	1.7	1.85	V
POWER-PATH MANAGEMENT						
$V_{SYS_REG_ACC}$	Typical system voltage regulation	ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT, T_J = -10°C - 65°C		50		mV
		ISYS = 0A, V_{BAT} < VSYSMIN, Charge Disabled. Offset above VSYSMIN, T_J = -10°C - 65°C		230		mV
V_{SYSMIN_RNG}	VSYSMIN register range		2.56		4.0	V
$V_{SYSMIN_REG_STEP}$	VSYSMIN register step size			80		mV
$V_{SYSMIN_REG_ACC}$	Minimum DC system voltage output	ISYS = 0A, V_{BAT} < VSYSMIN = B00h (3.52V), Charge Disabled	3.45	3.52		V
V_{SYS_SHORT}	VSYS short voltage falling threshold to enter forced PFM		1.9	2	2.1	V
V_{SYS_SHORTZ}	VSYS short voltage rising threshold to exit forced PFM			2.2		V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.50		4.80	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy	T_J = 25°C	–0.3		0.3	%
		T_J = -10°C - 65°C	–0.4		0.4	%
I_{CHG_RANGE}	Typical charge current regulation range		0.02		3.02	A
I_{CHG_STEP}	Typical charge current regulation step			20		mA
I_{CHG_ACC}	Typical charge current accuracy	VBAT = 3.1V or 3.8V, ICHG = 1760mA, T_J = -10°C - 65°C	–4		4	%
		VBAT = 3.1V or 3.8V, ICHG = 1000mA, T_J = -10°C - 65°C	–5		5	%
		VBAT = 3.1V or 3.8V, ICHG = 340mA, T_J = -10°C - 65°C	–7		7	%
I_{PRECHG_RANGE}	Typical pre-charge current range		20		1600	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Pre-charge current accuracy when V_{BAT} below V_{SYSMIN} setting	VBAT = 2.5V, IPRECHG = 340mA, T_J = -10°C - 65°C	–7		7	%
		VBAT = 2.5V, IPRECHG = 200mA, T_J = -10°C - 65°C	–10		10	%
		VBAT = 2.5V, IPRECHG = 100mA, T_J = -10°C - 65°C	–20		20	%
		VBAT = 2.5V, IPRECHG = 40mA, T_J = -10°C - 65°C	–30		30	%
I_{TERM_RANGE}	Typical termination current range		20		1000	mA
I_{TERM_STEP}	Typical termination current step			5		mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 40mA, T_J = -10°C - 65°C	–40		40	%
		ITERM = 120mA, T_J = -10°C - 65°C	–15		15	%
		ITERM = 200mA, T_J = -10°C - 65°C	–10		10	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V

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V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling		1.85		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}, ITRICKLE = 0	7	20	33	mA
V_{RECHG}	Battery recharge threshold below V_{REG}	VBAT falling		100		mV
		VBAT falling		200		mV
I_{SYS_LOAD}	System discharge load current		20			mA
BATFET						
V_{SUPPZ}	SYS < BAT threshold to exit supplement mode			5		mV
R_{BATFET}	MOSFET on resistance from SYS to BAT			15	23	mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage rising threshold	As percentage of VREG	103	104	105	%
V_{BAT_OVPZ}	Battery overvoltage falling threshold	As percentage of VREG	101	102	103	%
I_{BAT_PK}	Battery discharging peak current rising threshold		7			A
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		2.48		5.0	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=3V, T_J = -10°C - 65°C	–1		1	%
		VINDPM=4.48V, T_J = -10°C - 65°C	–1		1	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 1		120		°C
		TREG = 0		60		°C
T_{SHUT}	Thermal Shutdown Rising Threshold	Temperature Increasing		150		°C
T_{SHUT_HYS}	Thermal Shutdown Falling Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C
THERMISTOR COMPARATORS (CHARGE MODE)						
I_{TS}	TS bias current	EN_CHG=1, TS_IGNORE=0, TS=0V	36	38	40	µA
V_{TS_COLD}	TS_COLD entry voltage threshold	TS_TH_COLD=0 (-3°C)	1101	1150	1200	mV
		TS_TH_COLD=1 (0°C)	990	1035	1083	mV
V_{TS_COLDZ}	TS_COLD exit voltage threshold	TS_TH_COLD=0 (-3°C)	990	1035	1083	mV
		TS_TH_COLD=1 (0°C)	922	965	1009	mV
V_{TS_COOL}	TS_COOL entry voltage threshold	TS_TH_COOL=00 (5°C)	820	860	898	mV
		TS_TH_COOL=01 (10°C)	650	680	714	mV
		TS_TH_COOL=10 (15°C)	543	570	598	mV
		TS_TH_COOL=11 (20°C)	436	460	483	mV
V_{TS_COOLZ}	TS_COOL entry voltage threshold	TS_TH_COOL=00 (5°C)	752	790	825	mV
		TS_TH_COOL=01 (10°C)	607	640	668	mV
		TS_TH_COOL=10 (15°C)	500	525	552	mV
		TS_TH_COOL=11 (20°C)	408	430	453	mV

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V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TS_WARM}	TS_WARM entry voltage threshold	TS_TH_WARM=00 (35°C)	253	270	285	mV
		TS_TH_WARM=01 (40°C)	207	220	236	mV
		TS_TH_WARM=10 (45°C)	177	190	203	mV
		TS_TH_WARM=11 (50°C)	146	158	170	mV
V_{TS_WARMZ}	TS_WARM exit voltage threshold	TS_TH_WARM=00 (35°C)	271	290	304	mV
		TS_TH_WARM=01 (40°C)	244	252	262	mV
		TS_TH_WARM=10 (45°C)	189	200	216	mV
		TS_TH_WARM=11 (50°C)	159	170	183	mV
V_{TS_HOT}	TS_HOT entry voltage threshold	TS_TH_HOT=0 (55°C)	126	135	147	mV
		TS_TH_HOT=1 (60°C)	105	115	124	mV
V_{TS_HOTZ}	TS_HOT exit voltage threshold	TS_TH_HOT=0 (55°C)	134	145	159	mV
		TS_TH_HOT=1 (60°C)	113	125	137	mV
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency, 1MHz, SET_CONV_FREQ=0	0.8	1.0	1.2	MHz
		Oscillator frequency, 2MHz, SET_CONV_FREQ=1	1.75	2.0	2.25	MHz
MOSFET TURN-ON RESISTANCE						
R_{Q1_ON}	Buck High Side FET RDSON	T_j = –40°C-85°C (typical value is under 25°C)		16	27	mΩ
R_{Q2_ON}	Buck Low Side FET RDSON	T_j = –40°C-85°C (typical value is under 25°C)		24	44	mΩ
R_{Q3_ON}	Boost Low Side FET RDSON	T_j = –40°C-85°C (typical value is under 25°C)		20	35	mΩ
R_{Q4_ON}	Boost High Side FET RDSON	T_j = –40°C-85°C (typical value is under 25°C)		16	27	mΩ
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL		0.78			V
V_{IL}	Input low threshold level, SDA and SCL				0.42	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA, 1.2V VDD			0.3	V
I_{BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC OUTPUT PIN ($\overline{INT}$)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.3	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA

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5.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP						
t_{VBUS_OVP}	VBUS OVP deglitch time to set VBUS_OVP_STAT and VBUS_OVP_FLAG			200		µs
BATTERY CHARGER						
t_{TOP_OFF}	Typical top-off timer accuracy		12	15	18	min
			24	30	36	min
			36	45	54	min
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		0.9	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	1.8	2	2.2	hr
		PRECHG_TMR = 1	0.45	0.5	0.55	hr
t_{SAFETY}	Charge safety timer accuracy in fast charge	CHG_TMR = 0	10.8	12	13.2	hr
		CHG_TMR = 1	21.6	24	26.4	hr
BATFET CONTROL						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for standby or shutdown mode	BATFET_DLY = 1		10		s
		BATFET_DLY = 0		20		ms
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			350		ms
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1.0	MHz
C_b	Capacitive load for each bus line				550	pF
DIGITAL CLOCK AND WATCHDOG						
t_{LP_WDT}	Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 160s)		100	160		s
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 160s)		136	160		s

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5.7 Typical Characteristics

C_{VBUS} = 44µF, C_{SYS} = 44µF, L = 0.47µH (DCR = 21mΩ), F_{SW} = 1MHz (unless otherwise specified)

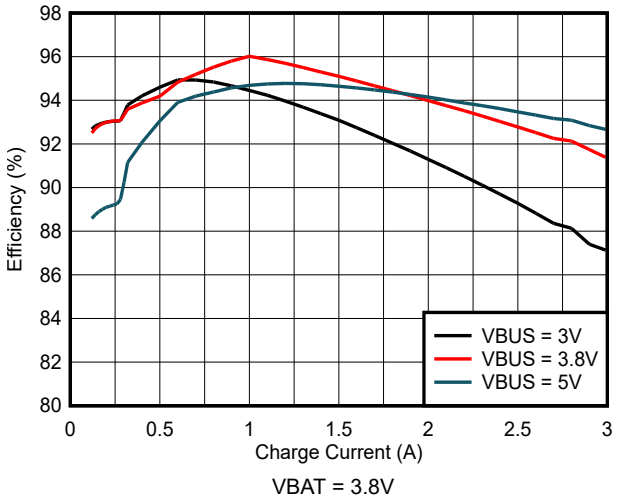


Figure 5-1. Charge Efficiency vs Charge Current

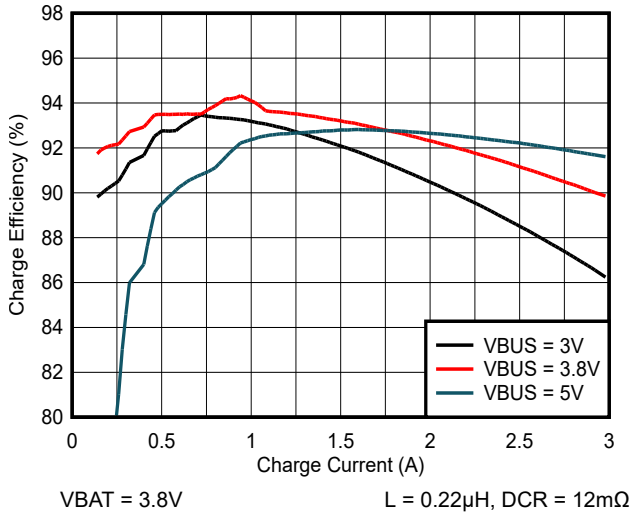


Figure 5-2. Charge Efficiency vs Charge Current (F_{SW} = 2MHz)

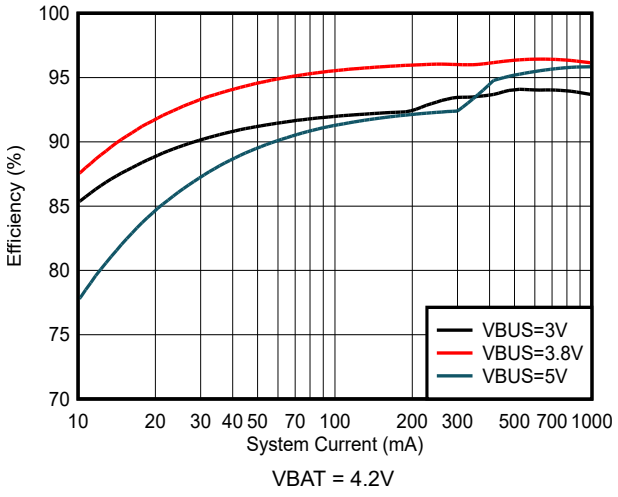


Figure 5-3. System Efficiency vs System Current

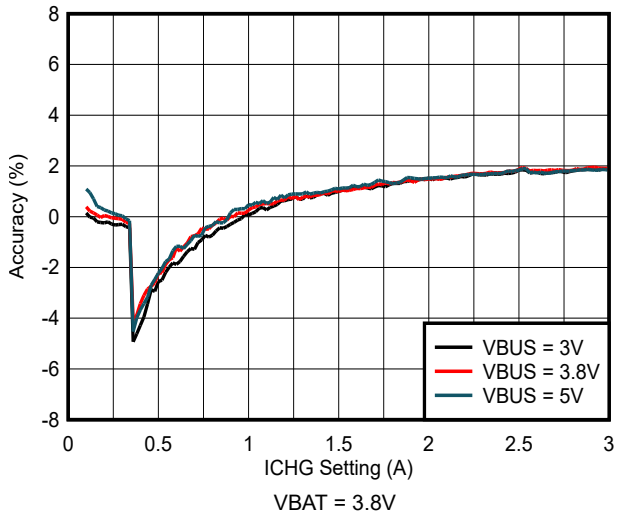


Figure 5-4. Charge Current Accuracy vs Charge Current I²C Setting

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5.7 Typical Characteristics (continued)

C_{VBUS} = 44µF, C_{SYS} = 44µF, L = 0.47µH (DCR = 21mΩ), F_{SW} = 1MHz (unless otherwise specified)

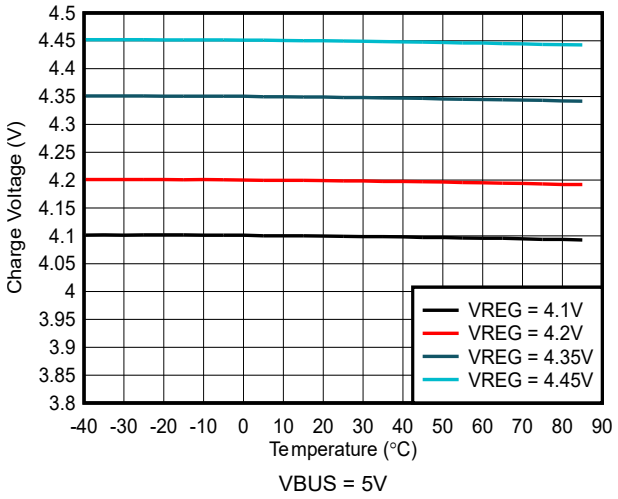


Figure 5-5. BAT Regulation Voltage vs Temperature

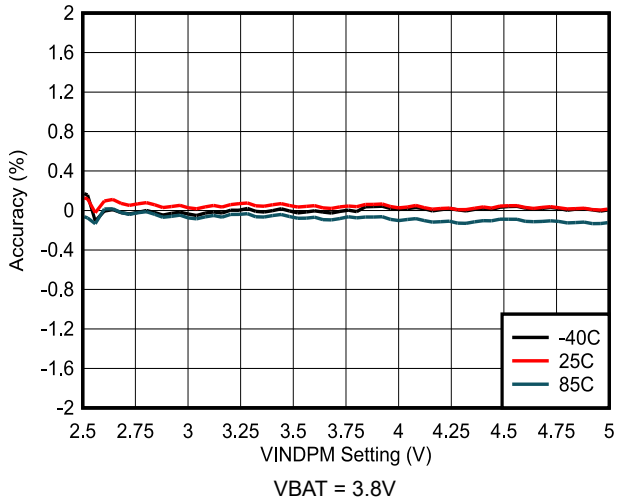


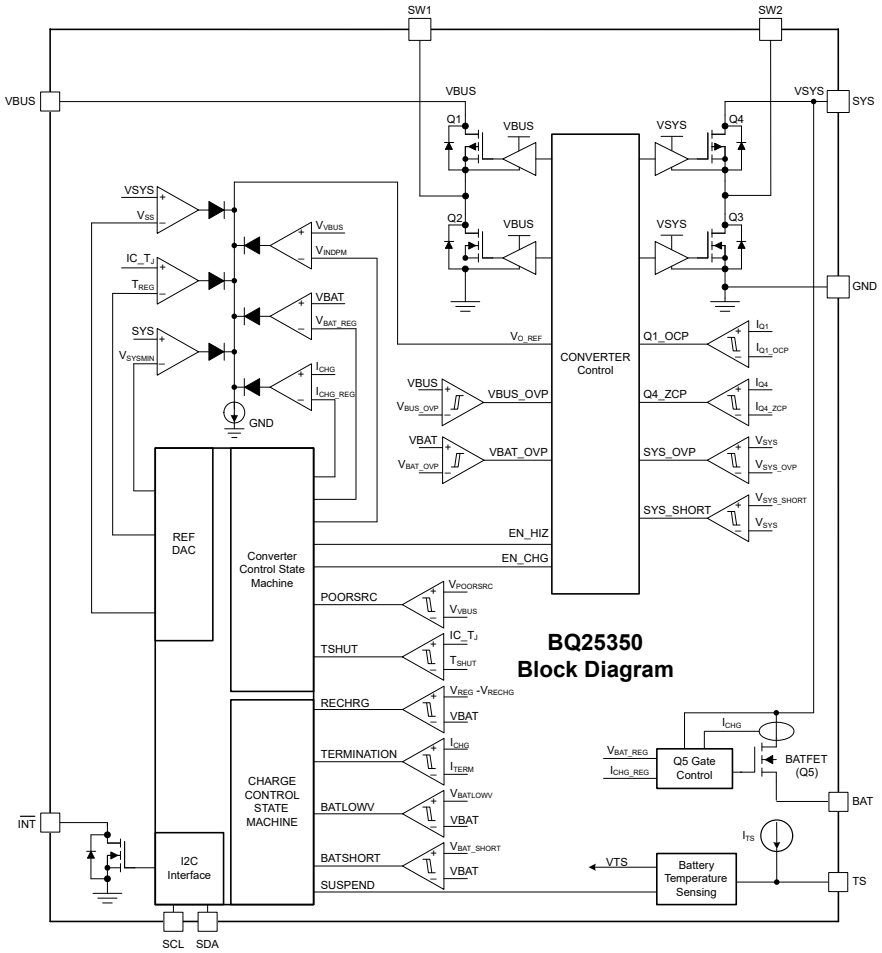
Figure 5-6. Input Voltage Limit vs VINDPM I²C Setting

6 Detailed Description

6.1 Overview

BQ25350 is a highly-integrated 3A buck-boost battery charger with NVDC power path management for single cell Li-Ion and Li-polymer batteries. It features fast charging with high efficiency and a low-impedance power path, reducing battery charge time and extended run-time during discharging. BQ25350 is also ideal for battery-to-battery charging with its low input voltage minimum and buck-boost topology. Additionally, it includes input voltage regulation to deliver maximum charging power to the battery without overloading the input source.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power-On-Reset (POR)

BQ25350 powers internal bias circuits from the higher voltage of VBUS versus BAT. When either voltage rises above its undervoltage lockout (UVLO) threshold, all registers are reset to their POR values and the I^2C interface is enabled for communication. A non-maskable $\overline{INT}$ pulse is generated, after which the host can access all of the registers.

6.3.2 Device Power Up from Battery

If only battery is present and the voltage is above depletion threshold (V_{BAT_UVLOZ}), BQ25350 performs a power-on reset then turns on BATFET to connect the battery to system. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

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6.3.3 Device Power Up from Input Source

When an input source is plugged in with VBAT < V_{BAT_UVLOZ}, BQ25350 performs a power-on reset then checks the input source voltage. It detects and sets the input voltage limit before the converter is started. If VBAT < V_{BAT_UVLOZ}, VBUS voltage must be above the input voltage limit threshold to power up successfully. The power up sequence from input source is as listed:

1. Internal bias circuits power up
2. Input voltage limit threshold setting (Section 6.3.3.1)
3. Converter power-up (Section 6.3.3.2)

6.3.3.1 Input Voltage Limit Threshold Setting (VINDPM Threshold)

BQ25350 supports a wide range of input voltage limit (2.5 V – 5V). When enabled, the input voltage limit will be set to the value of the VINDPM register.

6.3.3.2 Converter Power-Up

After the input voltage limit is set, the converter is enabled and the FETs start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery. Converter startup requires the following conditions:

- $V_{VBUS} < V_{VBUS_OVP}$
- EN_HIZ = 0
- $V_{SYS} < V_{SYS_OVP}$
- $T_J < T_{SHUT}$

BQ25350 provides soft start when system rail is ramped up. Concurrently, the system short protection limits the output current to approximately 0.5A when the system rail is below V_{SYS_SHORT}.

This device uses a highly efficient fixed frequency pulse width modulated (PWM) step-down switching regulator with F_{SW} configurable to 1MHz or 2MHz. The internally compensated feedback loop keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

To improve light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly when system load decreases. The minimum frequency can be limited to 25kHz when the Out of Audio (OOA) feature is enabled (EN_OOA=1b). The PFM_FWD_DIS bit can be used to disable PFM operation.

6.3.3.3 Maximum Power Point Tracking for Small PV Panel

The device implements a simple algorithm to track the maximum power point (MPP) when the input source is a solar photovoltaic (PV) panel. The I-V and P-V curves of a solar panel are most strongly dependent on irradiation and temperature. The MPP is most commonly located between 70%~90% of the Open Circuit Voltage (VOC) of the solar panel. The algorithm automatically and periodically detects the charger input source VOC, and sets the VINDPM to be a ratio of the measured VOC. It is recommended to set the charging current to the maximum value, so that the VINDPM is always triggered and activated. The MPPT algorithm is disabled by default at POR (EN_MPPT = 0). The algorithm runs automatically when EN_MPPT=1 unless FORCE_VINDPM = 1. Note that the maximum VINDPM setting is 5V, so the maximum VINDPM the MPPT algorithm can set is 5V. When VOC_PCT * VOC > 5V, VINDPM will be clamped at 5V.

When the battery voltage is lower than VSYSMIN, the MPPT algorithm can be enabled but the system voltage is likely to fall below VSYSMIN to the actual battery voltage. In the MPPT process, the buck-boost charger stops switching for a time period programmed by VOC_DLY[1:0]. When the charger stops switching, the system is powered by the battery discharging. After VOC_DLY[1:0], the charger measures the open-circuit voltage of the input source attached at VBUS and updates the VINDPM to be VOC_PCT[2:0]*VOC. The converter starts drawing power from the input source until the VOC_RATE[1:0] time interval expires, at which point it stops switching for another VOC_DLY[1:0], measures VOC, and updates the VINDPM register to complete the next cycle.

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6.3.3.4 Switching Frequency and Dithering Feature

Normally, the device switches with a fixed frequency. The charger also supports a frequency dithering function to improve EMI performance and help pass IEC-CISPR 22 specification. This function is disabled by default with setting EN_DITHER=00b. It can be enabled by setting EN_DITHER=01/10/11b, the switching frequency is not fixed when dithering is enabled, it varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. The larger dithering range is selected, the smaller EMI noise peak will be, but at same time slightly larger VBUS/VSYS capacitor voltage ripple is generated. Therefore the dithering frequency range selection is a trade-off between EMI noise peak and VSYS/VBUS voltage ripple, recommend to select the lowest dithering range which can pass IEC-CISPR 22 specification. The patented dithering pattern can improve EMI performance from switching frequency and up to 30MHz high frequency range which covers the entire conductive EMI noise range.

6.3.4 Power Path Management

BQ25350 accommodates a wide range of input sources from USB, wall adapter, to car charger. It provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

6.3.4.1 Narrow VDC Architecture

BQ25350 uses the Narrow VDC architecture (NVDC) with BATFET separating the system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on and the voltage difference between the system and battery is the R_{DSON} of BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above minimum system voltage setting, or charging is terminated, the system is regulated 50mV (typical) above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

6.3.4.2 Dynamic Power Management

To maximize input current without overloading the adapter, the charger features Dynamic Power Management (DPM), which continuously monitors the input voltage. When an input source is over-loaded, the voltage falls below the input voltage limit (VINDPM). To prevent overloading the adapter, the device reduces the charge current such that the input voltage stays above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters supplement mode where the BATFET turns on and the battery starts discharging to support the system from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT is set high. Figure 6-1 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current, and 3.4V minimum system voltage setting.

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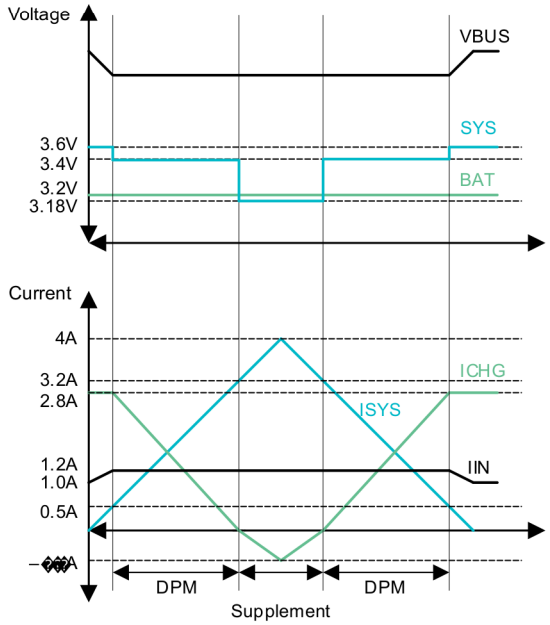


Figure 6-1. DPM Response

6.3.4.3 High Impedance (HIZ) Mode

The host may place the device into high impedance mode by writing EN_HIZ = 1 when an adpater is connected. In high impedance mode, the switching FETs (Q1-Q4) are turned off, blocking current flow to and from VBUS and putting the VBUS pin into a high impedance state. The BATFET (Q5) is turned on to connect the BAT to SYS. The device has very low power loss in HIZ mode.

6.3.5 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3A charge current. The 15 mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

6.3.5.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 6-1. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 6-1. Charging Parameter Default Settings

	VREG	VRECHG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
BQ25350	4.2V	VREG - 100mV	20mA	100mA	1,000mA	100 mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in Section 6.3.3.2
- EN_CHG = 1 or toggle EN_CHG bit
- No thermistor fault on TS
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold and charger is in CV mode, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling EN_CHG bit will also initiate a new charging cycle.

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The status register (CHG_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (V_{BAT} < V_{BAT_SHORTZ})
- 010 – Pre-charge (V_{BAT_SHORTZ} < V_{BAT} < $V_{BATLOWV}$)
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the CHG_STAT transitions to any of these states, including when the charge cycle completes, an INT pulse is asserted to notify the host.

6.3.5.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

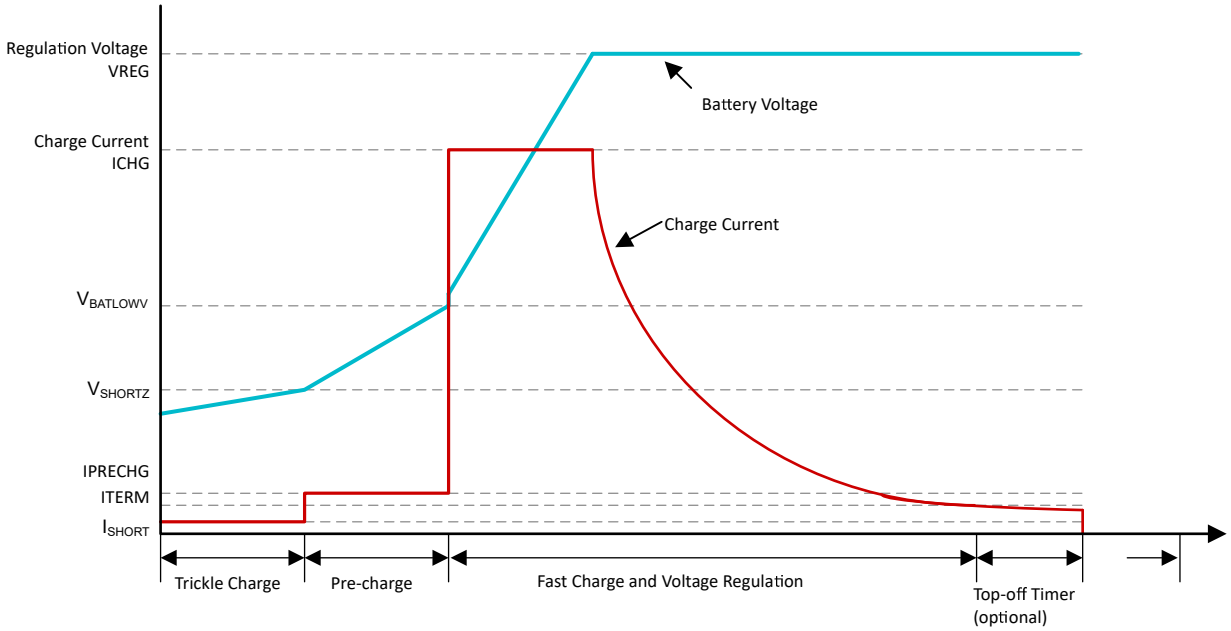


Figure 6-2. Battery Charging Profile

6.3.5.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the battery current is below ITERM. Because constant-voltage regulation is required for termination, the device does not terminate while VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

When termination occurs, the status register CHG_STAT is set to 111, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input voltage or thermal regulation. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

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To compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. When the top-off timer is enabled and termination occurs, the status register CHG_STAT is set to 110. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so will the top-off timer. Similarly, if the safety timers count at half-clock rate, so will the top-off timer. Refer to Section 6.3.5.7 for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

At low termination currents without battery presented, it is suggested to add capacitance at VBAT to prevent system instability. The suggested capacitance is 50µF.

6.3.5.4 BATFET Partition

The BATFET is partitioned to operate with either 15mΩ or 120mΩ R_{DSON}. By default, BQ25350 will switch between 15mΩ and 120mΩ R_{DSON} to support higher fast charging current using 15mΩ R_{DSON} with more precise termination using 120mΩ R_{DSON}. The device can also be forced to always use 15mΩ R_{DSON} for reduced power dissipation by setting Q5_FULLON= 1. The Q5_FULLON setting is only applied when V_{BAT} > VSYSMIN. When V_{BAT} < VSYSMIN, the BATFET operates in linear mode and does not have a fixed resistance.

If ICHG is set to 350mA or less, BQ25350 sets the BATFET at a constant 120mΩ, unless Q5_FULLON =1, in which case it sets the BATFET at a constant 15mΩ. If ICHG is set above 350mA and termination current is greater than 100mA, BQ25350 sets the BATFET at a constant 15mΩ, regardless of the Q5_FULLON setting.

If ICHG is set above 350mA and termination current is less than or equal to 100mA, BQ25350 sets 15mΩ BATFET during fast charge and will automatically transition to 120mΩ BATFET when charging current falls below 160mA if all of the following conditions are met:

- Q5_FULLON = 0
- ITERM ≤ 100mA
- EN_TERM = 1
- Charging Current measured below 160mA
- VINDPM_STAT=0, TREG_STAT = 0
- No fault is active that stops the converter

Regardless of settings, the BATFET is always put into low resistance 15mΩ state when the battery is discharging during supplement mode.

6.3.5.5 IR Compensation

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs, and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charging time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (VCLAMP) and the minimum resistance compensation (BATCOMP).

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Considering the voltage drop between BAT pin and battery terminal, the VREG_ACTUAL is the actual targeted voltage: VREG_ACTUAL = VREG + min(ICHG_ACTUAL x BATCOMP, VCLAMP)

6.3.5.6 Thermistor Qualification

The charger provides a single thermistor input (TS) for battery temperature monitor. The TS pin can be ignored by setting TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good, and TS_STAT will always report TS_NORMAL. It is recommended to use a 10K pulldown if TS is not being used to avoid suspending charging during startup before the host can configure TS_IGNORE = 1.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Section 6.3.5.6.1. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range, unless it is TS_NORMAL, which has no FLAG. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, will generate an $\overline{INT}$ pulse.

6.3.5.6.1 Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. BQ25350 features a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard.

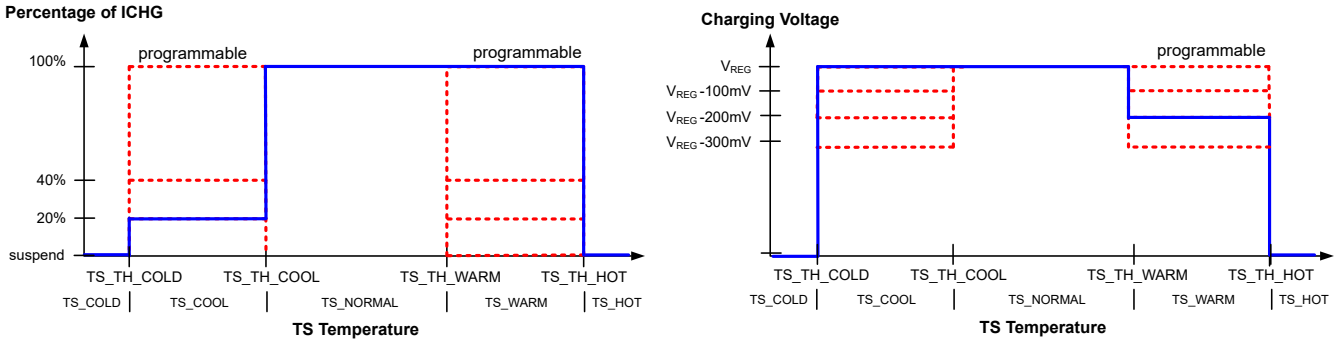


Figure 6-3. Advanced TS Charging Values

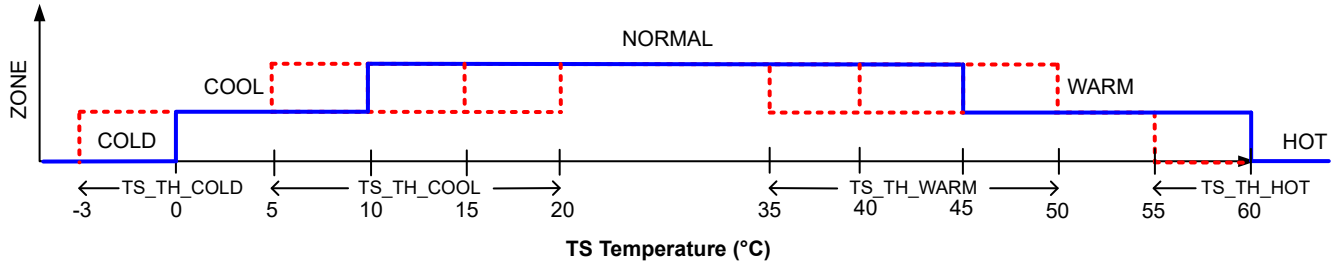


Figure 6-4. Advanced TS Charging Regions

Table 6-2. TS Threshold Settings (default values in bold)

REGION	CONTROL REGISTER	CONTROL VALUE
COLD	TS_TH_COLD	-3ºC
		0ºC

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Table 6-2. TS Threshold Settings (default values in bold) (continued)

REGION	CONTROL REGISTER	CONTROL VALUE
COOL	TS_TH_COOL	5ºC
		10ºC
		15ºC
		20ºC
WARM	TS_TH_WARM	35ºC
		40ºC
		45ºC
		50ºC
HOT	TS_TH_HOT	55ºC
		60ºC

Charging termination and the charging safety timer are adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer will count at half rate. If charging is suspended, the safety timer is suspended, CHG_STAT is set to 000 (not charging). Charging termination is still enabled (when EN_TERM=1) with termination current (ITERM) unchanged when charging current is reduced in cool or warm temperature zones.

6.3.5.6.2 JEITA Charge Rate Scaling

The TS_ISET_COOL and TS_ISET_WARM cool and warm charge current fold backs are based on a 1C charging rate. The 1C rate is the battery capacity in mA-hours divided by 1 hour, so that a 500mA-hour battery would have a 1C charging rate of 500mA. The same battery would have a 2C charging rate of 1,000mA. To convert the charging foldback, the host must set the CHG_RATE register to the C rate for the battery. This scales the foldback accordingly.

When TS_ISET_COOL or TS_ISET_WARM is set to either 00 (suspend) or 11 (unchanged), the CHG_RATE setting has no effect.

Table 6-3. ICHG Fold Back

TS_ISET_COOL or TS_ISET_WARM	CHG_RATE	FOLD-BACK CURRENT AS PERCENTAGE OF ICHG
00	Any	0% (Suspended)
01 (20%)	00 (1C)	20%
	01 (2C)	10%
	10 (4C)	5%
	11 (6C)	3.3%
10 (40%)	00 (1C)	40%
	01 (2C)	20%
	10 (4C)	10%
	11 (6C)	6.6%
11	Any	100%

6.3.5.7 Charging Safety Timers

BQ25350 has three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed as 1 hour. At the end of a safety timer expiration, charging is stopped (CHG_STAT = 000b) and the buck converter continues to operate to supply system load.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage

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the charger is in. Each timer will start to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current will also cause the charging safety timer to count at half-clock rate if EN_TMR2X bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the EN_TMR2X bit. Once the fault goes away, charging resumes and the safety timer resumes where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging will keep running until it is disabled by the host.

6.3.6 Interrupt to Host ($\overline{INT}$)

In many applications, the host does not continually poll the charger status registers. Instead, the $\overline{INT}$ pin may be used to notify the host of a status change with a 256-µs $\overline{INT}$ pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

The $\overline{INT}$ events can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X.) Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

6.3.7 BATFET Control

The device has an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports standby mode and shutdown mode. Additionally, the system power reset function is controlled by the SYS_RESET register bit.

Table 6-4. BATFET Control Modes

MODE	BATFET	I^2C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =1	EXIT
Normal	On	Active	N/A			N/A
Shutdown mode	Off	Off	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY and enters shutdown mode.	Writing BATFET_CTRL = 10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters shutdown mode. Writing BATFET_CTRL = 00 before adapter is removed aborts shutdown mode.	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters shutdown mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts shutdown mode.	Adapter plug-in

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Table 6-4. BATFET Control Modes (continued)

MODE	BATFET	I²C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =1	EXIT
Standby mode	Off	Active	Writing BATFET_CTRL = 11 turns off BATFET after BATFET_DLY and enters standby mode.	Writing BATFET_CTRL = 11 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters standby mode. Writing BATFET_CTRL = 00 before adapter is removed aborts standby mode.	Writing BATFET_CTRL = 11 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters standby mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts standby mode.	I²C, adapter plug-in
System reset	On to Off to On	Active	Writing SYS_RESET = 1 initiates system reset after BATFET_DLY.	Writing SYS_RESET = 1 is ignored and SYS_RESET resets to 0.	Writing SYS_RESET = 1 initiates system reset after BATFET_DLY. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A

6.3.7.1 Shutdown Mode

In shutdown mode, the BATFET is turned off to prevent the battery from powering the system. The host may place BQ25350 into shutdown mode by setting BATFET_CTRL = 10. The device is taken out of shutdown mode by adapter plug-in (V_{VBUS} > V_{VBUS_UVLOZ}).

When the charger enters shutdown mode, the registers are reset to their POR values.

Shutdown mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while V_{VBUS} > V_{VBUS_UVLOZ} (adapter present) will either disable the BATFET or have no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

6.3.7.2 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. A system reset also resets all registers to POR state. Any of the following conditions will initiate a system power reset:

- BATFET_CTRL_WVBUS = 1 and SYS_RESET = 1
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} and SYS_RESET = 1

When BATFET_CTRL_WVBUS is set to 1, system power reset will proceed if SYS_RESET = 1, regardless of whether or not VBUS is present. There is a delay of t_{BATFET_DLY} before initiating the system power reset.

The system power reset can be initiated from the battery only condition or from the forward charging mode with adapter present.

6.3.7.3 Standby Mode

In standby mode, the BATFET is turned off to prevent the battery from powering the system. The host may place BQ25350 into standby mode by setting BATFET_CTRL = 11b. Standby mode has slightly higher quiescent current than shutdown mode, but an I²C command may be used to exit from standby mode. The device is taken out of standby mode by either of these methods:

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- Write BATFET_CTRL to 00b via I^2C
- Write REG_RST to 1b via I^2C (Registers will be reset)
- $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter plug-in)

When waking up from standby mode via I^2C, the response to the first write will always be a NACK. It is necessary to perform two valid writes to either REG_RST = 1b or BATFET_CTRL = 00b in a row to exit from standby mode.

Standby mode is only entered when the adapter is not present. Setting BATFET_CTRL = 11b while $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter present) will either disable the BATFET or have no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

6.3.8 Protections

6.3.8.1 Voltage and Current Monitoring in Battery Only and HIZ Modes

The device monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode.

6.3.8.1.1 Battery Overcurrent Protection

The I_{BAT_PK} threshold provides a fast (100 µs) protection for the battery discharging. If the battery discharge current becomes higher than this threshold for its deglitch time, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode. The BAT_FAULT_STAT will return to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK}threshold is re-evaluated with its deglitch time.

6.3.8.1.2 Battery Undervoltage Lockout

In battery-only mode, BQ25350 will disable the BATFET if V_{BAT} falls below V_{BAT_UVLO}, separating the system from the battery. I^2C is disabled as well. Upon exit from the undervoltage lockout condition when either V_{BAT} rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^2C will be re-enabled and the registers are reset to their POR values.

6.3.8.2 Voltage and Current Monitoring in Forward Mode

6.3.8.2.1 Input Overvoltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching immediately to protect the internal power MOSFETs. VBUS_FAULT_FLAG is set to 1 and the VBUS_FAULT_STAT bit transitions to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_OVP_STAT will transition to 0 and the converter will resume switching.

6.3.8.2.2 System Overvoltage Protection (SYSOVP)

When VSYS rises above V_{SYS_OVP} (around 300mV above VBAT when not charging) in forward converter operation, the converter stops switching immediately to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG is set to 1 and the VSYS_FAULT_STAT transitions to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 30mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

6.3.8.2.3 Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In forward mode, if the current through Q1 exceeds the cycle-by-cycle limit, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

6.3.8.2.4 System Short

When the SYS voltage falls below V_{SYS_SHORT}, the charger immediately enters PFM operation to limit the output current to approximately 0.5A or less. SYS_FAULT_STAT and SYS_FAULT_FLAG bits are set to 1. If V_{SYS} rises above V_{SYS_SHORTZ}, the converter exits forced PFM mode, and the SYS_FAULT_STAT bit is set to 0.

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6.3.8.2.5 Battery Overvoltage Protection (BATOVP)

When V_{BAT} transitions above V_{BAT_OVP}, BQ25350 immediately disables charging by turning off the converter and applies I_{SYS_LOAD} pulldown current. With the BATFET still turned on, the battery will discharge via the load on SYS. BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once V_{BAT} falls below V_{BAT_OVPZ}, charging resumes and BAT_FAULT_STAT transitions back to 0.

6.3.8.3 Thermal Regulation and Thermal Shutdown

6.3.8.3.1 Thermal Protection in Battery-only Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

6.3.8.3.2 Thermal Protection in Forward Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the T_{REG} thermal regulation limit (TREG register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

6.4 Device Functional Modes

6.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables in Section 6.5.2.1. The watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

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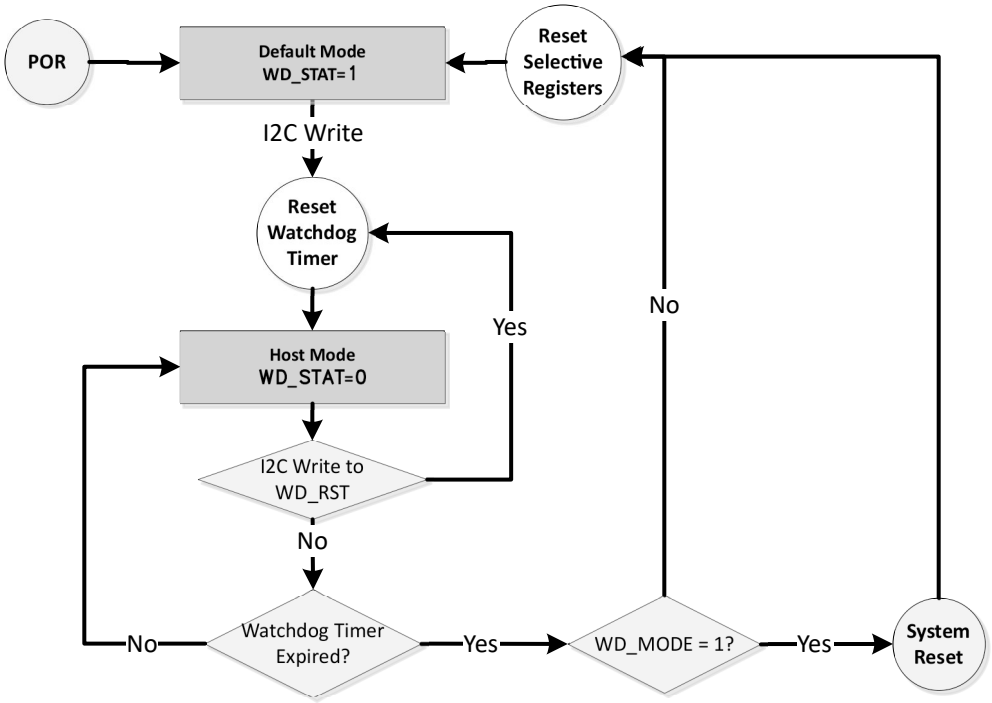


Figure 6-5. Watchdog Timer Flow Chart

6.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

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6.5 Programming

6.5.1 Serial Interface

BQ25350 uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^{2}C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses defined in the Register Map. The host device initiates all transfers and the charger responds. Register reads outside of these adresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^{2}C interface supports standard mode (up to 100kbits/s), fast mode (up to 400kbits/s) and fast mode plus (up to 1Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^{2}C detection thresholds support a communication reference voltage between 1.2V - 5V.

6.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

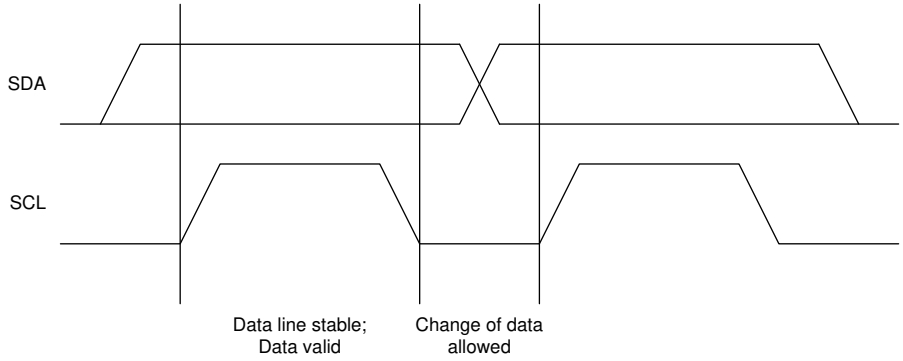


Figure 6-6. Bit Transfer on the I^{2}C Bus

6.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

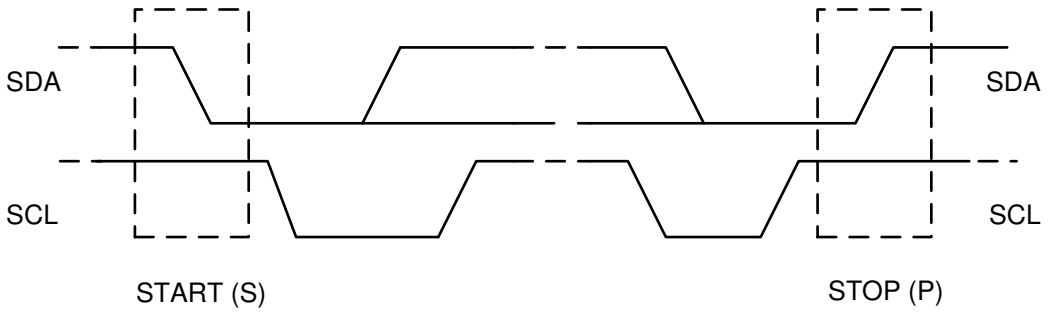


Figure 6-7. START and STOP Conditions on the I^{2}C Bus

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6.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

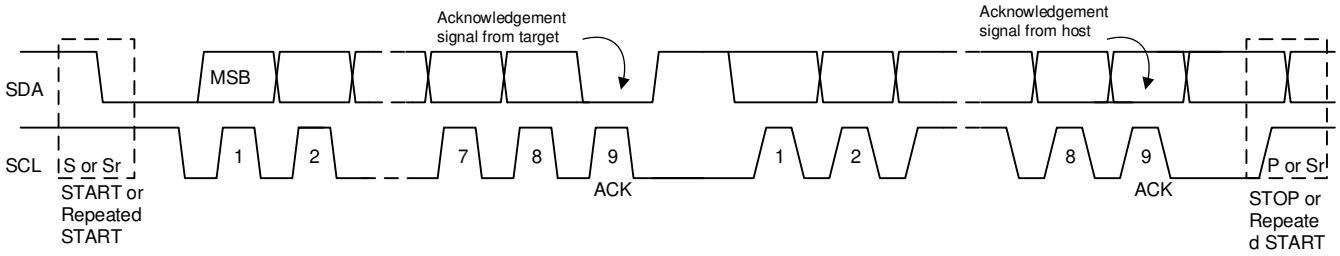


Figure 6-8. Data Transfer on the I²C Bus

6.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the host to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the host can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

6.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as



Figure 6-9. 7-Bit Addressing (0x6B)

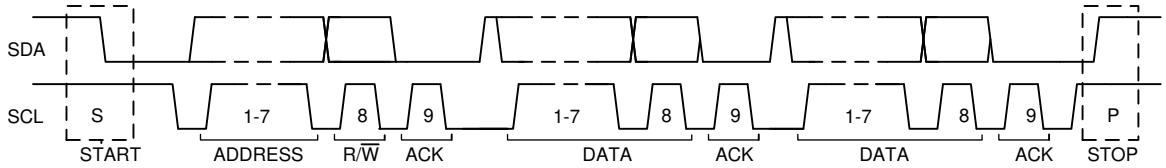


Figure 6-10. Complete Data Transfer on the I²C Bus

6.5.1.6 Single Write and Read

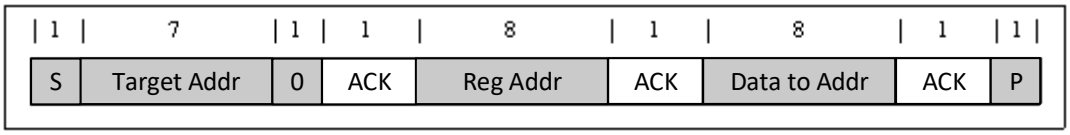


Figure 6-11. Single Write

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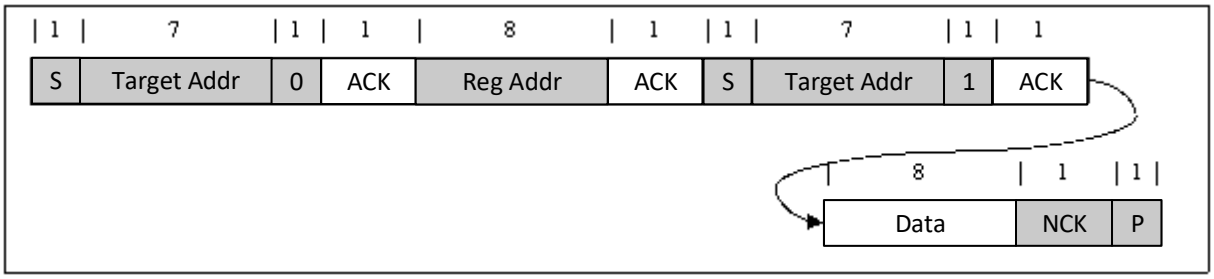


Figure 6-12. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

6.5.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

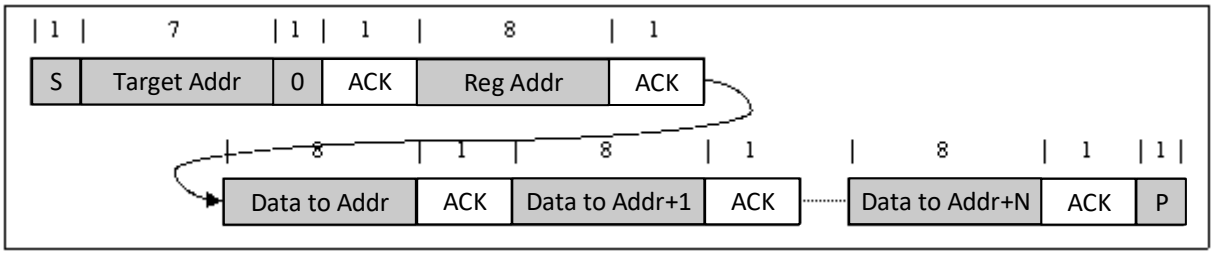


Figure 6-13. Multi-Write

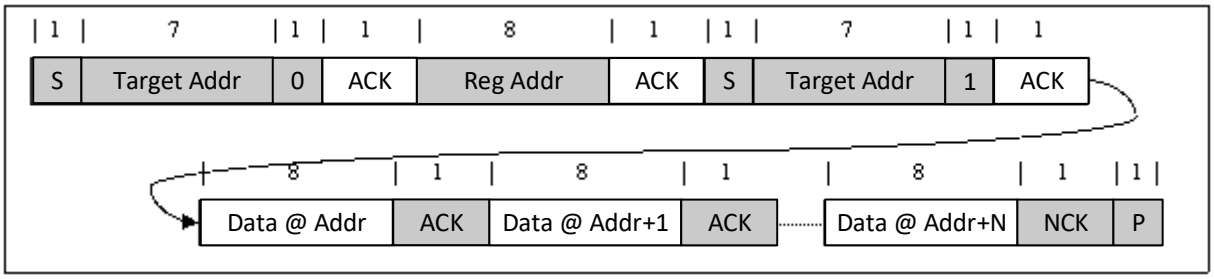


Figure 6-14. Multi-Read

6.5.2 Register Maps

6.5.2.1 BQ25350 Registers

Table 6-5 lists the memory-mapped registers for the BQ25350 registers. All register offset addresses not listed in Table 6-5 should be considered as reserved locations and the register contents should not be modified.

Table 6-5. BQ25350 Registers

Address	Acronym	Register Name	Section
2h	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
4h	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit	Go
6h	REG0x06_Input_Voltage_Limit	Input Voltage Limit	Go
8h	REG0x08_Minimal_System_Voltage	Minimal System Voltage	Go
Ah	REG0x0A_Precharge_Control	Precharge Control	Go
Ch	REG0x0C_Termination_Control	Termination Control	Go
Eh	REG0x0E_Charger_Control_0	Charger Control 0	Go

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Table 6-5. BQ25350 Registers (continued)

Address	Acronym	Register Name	Section
Fh	REG0x0F_Charger_Control_1	Charger Control 1	Go
10h	REG0x10_Charger_Control_2	Charger Control 2	Go
11h	REG0x11_Charger_Control_3	Charger Control 3	Go
12h	REG0x12_Charger_Control_4	Charger Control 4	Go
13h	REG0x13_Charger_Control_5	Charger Control 5	Go
14h	REG0x14_MPPT_Control	MPPT Control	Go
15h	REG0x15_Charge_Timer_Control	Charge Timer Control	Go
16h	REG0x16_NTC_Control_0	NTC Control 0	Go
17h	REG0x17_NTC_Control_1	NTC Control 1	Go
18h	REG0x18_Charger_Status_0	Charger Status 0	Go
19h	REG0x19_Charger_Status_1	Charger Status 1	Go
1Ah	REG0x1A_FAULT_Status	FAULT Status	Go
1Bh	REG0x1B_Charger_Flag_0	Charger Flag 0	Go
1Ch	REG0x1C_FAULT_Flag	FAULT Flag	Go
1Dh	REG0x1D_Charger_Mask_0	Charger Mask 0	Go
1Eh	REG0x1E_FAULT_Mask	FAULT Mask	Go
1Fh	REG0x1F_Part_Information	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 6-6 shows the codes that are used for access types in this section.

Table 6-6. BQ25350 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.5.2.1.1 REG0x02_Charge_Current_Limit Register (Address = 2h) [Reset = 0320h]

REG0x02_Charge_Current_Limit is shown in Figure 6-15 and described in Table 6-7.

Return to the Summary Table.

Figure 6-15. REG0x02_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICHG			
R-0h				R/W-32h			
7	6	5	4	3	2	1	0
ICHG				RESERVED			
R/W-32h				R-0h			

Table 6-7. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved

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Table 6-7. REG0x02_Charge_Current_Limit Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
11:4	ICHG	R/W	32h	This 16-bit register follows the little-endian convention. Watchdog Timer expiration sets ICHG to 1/2 its previous value (rounded down) NOTE: When Q5_FULLON=1, this register has a minimum value of 160mA Reset by: REG_RESET	POR: 1000mA (32h) Range: 20mA-3020mA (1h-97h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h		Reserved

6.5.2.1.2 REG0x04_Charge_Voltage_Limit Register (Address = 4h) [Reset = 0D20h]

REG0x04_Charge_Voltage_Limit is shown in Figure 6-16 and described in Table 6-8.

Return to the Summary Table.

Figure 6-16. REG0x04_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VREG			
R-0h				R/W-1A4h			
7	6	5	4	3	2	1	0
VREG					RESERVED		
R/W-1A4h					R-0h		

Table 6-8. REG0x04_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	VREG	R/W	1A4h	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Battery Voltage Regulation Limit: POR: 4200mV (1A4h) Range: 3500mV-4800mV (15Eh-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0h		Reserved

6.5.2.1.3 REG0x06_Input_Voltage_Limit Register (Address = 6h) [Reset = 08C0h]

REG0x06_Input_Voltage_Limit is shown in Figure 6-17 and described in Table 6-9.

Return to the Summary Table.

Figure 6-17. REG0x06_Input_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VINDPM			
R-0h				R/W-46h			
7	6	5	4	3	2	1	0
VINDPM				RESERVED			
R/W-46h				R-0h			

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Table 6-9. REG0x06_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:5	VINDPM	R/W	46h	This 16-bit register follows the little-endian convention	Absolute Input Voltage Regulation Limit: POR: 2800mV (46h) Range: 2480mV-5000mV (3Eh-7Dh) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0h		Reserved

6.5.2.1.4 REG0x08_Minimal_System_Voltage Register (Address = 8h) [Reset = 0B00h]

REG0x08_Minimal_System_Voltage is shown in Figure 6-18 and described in Table 6-10.

Return to the Summary Table.

Figure 6-18. REG0x08_Minimal_System_Voltage Register

15	14	13	12	11	10	9	8
RESERVED				VSYSMIN			
R-0h				R/W-2Ch			
7	6	5	4	3	2	1	0
VSYSMIN			RESERVED				
R/W-2Ch			R-0h				

Table 6-10. REG0x08_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:6	VSYSMIN	R/W	2Ch	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Minimal System Voltage: POR: 3520mV (2Ch) Range: 2560mV-4000mV (20h-32h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h		Reserved

6.5.2.1.5 REG0x0A_Precharge_Control Register (Address = Ah) [Reset = 0050h]

REG0x0A_Precharge_Control is shown in Figure 6-19 and described in Table 6-11.

Return to the Summary Table.

Figure 6-19. REG0x0A_Precharge_Control Register

15	14	13	12	11	10	9	8
RESERVED					IPRECHG		
R-0h					R/W-5h		
7	6	5	4	3	2	1	0
IPRECHG				RESERVED			
R/W-5h				R-0h			

Table 6-11. REG0x0A_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0h		Reserved

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Table 6-11. REG0x0A_Precharge_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
10:4	IPRECHG	R/W	5h	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Pre-charge current regulation limit: NOTE: When Q5_FULLON=1, this register has a minimum value of 80mA POR: 100mA (5h) Range: 20mA-1600mA (1h-50h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h		Reserved

6.5.2.1.6 REG0x0C_Termination_Control Register (Address = Ch) [Reset = 0050h]

REG0x0C_Termination_Control is shown in Figure 6-20 and described in Table 6-12.

Return to the Summary Table.

Figure 6-20. REG0x0C_Termination_Control Register

15	14	13	12	11	10	9	8
RESERVED						ITERM	
R-0h						R/W-14h	
7	6	5	4	3	2	1	0
ITERM						RESERVED	
R/W-14h						R-0h	

Table 6-12. REG0x0C_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0h		Reserved
9:2	ITERM	R/W	14h	Reset by: REG_RESET	Termination Current Threshold: NOTE: When Q5_FULLON=1, this register has a minimum value of 120mA POR: 100mA (14h) Range: 20mA-1000mA (4h-C8h) Clamped Low Clamped High Bit Step: 5mA
1:0	RESERVED	R	0h		Reserved

6.5.2.1.7 REG0x0E_Charger_Control_0 Register (Address = Eh) [Reset = A0h]

REG0x0E_Charger_Control_0 is shown in Figure 6-21 and described in Table 6-13.

Return to the Summary Table.

Figure 6-21. REG0x0E_Charger_Control_0 Register

7	6	5	4	3	2	1	0
EN_CHG	EN_HIZ	EN_TERM	ITRICKLE	VRECHG	Q5_FULLON	BATLOWV	
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 6-13. REG0x0E_Charger_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_CHG	R/W	1h	Reset by: REG_RESET WATCHDOG	Charger enable configuration 0b = Charge Disable 1b = Charge Enable (default)

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Table 6-13. REG0x0E_Charger_Control_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	EN_HIZ	R/W	0h	Reset by: REG_RESET WATCHDOG Adapter Plug In Adapter Unplug	Enable HIZ mode. This bit will be reset to 0, when the adapter is plugged in at VBUS. 0b = Disable (default) 1b = Enable
5	EN_TERM	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable termination 0b = Disable 1b = Enable (default)
4	ITRICKLE	R/W	0h	When Q5_FULLON, this setting is forced to 80mA Reset by: REG_RESET	Trickle charging current setting: 0b = 20mA (Default) 1b = 80mA
3	VRECHG	R/W	0h	Reset by: REG_RESET	Battery Recharge Threshold Offset (Below VREG) 0b = 100mV (default) 1b = 200mV
2	Q5_FULLON	R/W	0h		Forces BATFET (Q5) into low resistance state (15 mOhm), regardless of ICHG setting. 0b = BATFET RDSON determined by charge current (Default) 1b = BATFET RDSON is always 15 mOhm
1:0	BATLOWV	R/W	0h		Battery precharge to fast-charge threshold: 00b = 3.0V (Default) 01b = 2.8V 10b = 2.7V 11b = 2.2V

6.5.2.1.8 REG0x0F_Charger_Control_1 Register (Address = Fh) [Reset = 40h]

REG0x0F_Charger_Control_1 is shown in Figure 6-22 and described in Table 6-14.

Return to the Summary Table.

Figure 6-22. REG0x0F_Charger_Control_1 Register

7	6	5	4	3	2	1	0
WATCHDOG		WD_RST	WD_MODE	TOPOFF_TMR		FORCE_ISYS_DSCHG	TERM_DG_SEL
R/W-1h		R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 6-14. REG0x0F_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	WATCHDOG	R/W	1h	Reset by: REG_RESET	Watchdog timer setting 00b = Disable 01b = 40s (default) 10b = 80s 11b = 160s
5	WD_RST	R/W	0h	Reset by: REG_RESET	I2C watch dog timer reset 0b = Normal (default) 1b = Reset (this bit goes back to 0 after timer reset)
4	WD_MODE	R/W	0h	Reset by: REG_RESET	Enable System Reset when Watchdog Timer expires. 0b = No System Reset on Watchdog Timer Expiration (Default) 1b = System Reset on Watchdog Timer Expiration

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Table 6-14. REG0x0F_Charger_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
3:2	TOPOFF_TMR	R/W	0h	Reset by: REG_RESET	Top-off timer control: 00b = Disabled (default) 01b = 15 mins 10b = 30 mins 11b = 45 mins
1	FORCE_ISYS_DSCHG	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable SYS pull down current source 0b = Disable (Default) 1b = Enable
0	TERM_DG_SEL	R/W	0h	Reset by: REG_RESET WATCHDOG	Termination deglitch select 0b = 50ms (Default) 1b = 12.5ms

6.5.2.1.9 REG0x10_Charger_Control_2 Register (Address = 10h) [Reset = 12h]

REG0x10_Charger_Control_2 is shown in Figure 6-23 and described in Table 6-15.

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Figure 6-23. REG0x10_Charger_Control_2 Register

7	6	5	4	3	2	1	0
REG_RST	SYS_RESET	BATFET_CTRL_WVBUS	BATFET_DLY	BATFET_CTRL		TREG	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h

Table 6-15. REG0x10_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0h		Reset registers to default values Value resets to 0 after reset completes. 0b = Not reset (default) 1b = Reset
6	SYS_RESET	R/W	0h	Reset by: REG_RESET WATCHDOG	Reset system by opening BATFET. The bit is reset to 0 after reset is complete. Also resets all registers to POR value. 0b = Disable 1b = System Reset
5	BATFET_CTRL_WVBUS	R/W	0h		Start system power reset with or without adapter present. 0b = Start system power reset after adapter is removed from VBUS. (default) 1b = Start system power reset whether or not adapter is present on VBUS.
4	BATFET_DLY	R/W	1h	Reset by: REG_RESET	Delay time added to the taking action in bits [1:0] of the BATFET_CTRL 0b = Add 20ms delay 1b = Add 10s delay (Default)
3:2	BATFET_CTRL	R/W	0h	Reset by: REG_RESET	BATFET control The control logic of the BATFET to force the device enter different modes. 00b = Idle (Default) 10b = Shutdown mode 11b = Standby mode
1	TREG	R/W	1h	Reset by: REG_RESET	Thermal regulation thresholds. 0b = 60°C 1b = 120°C (Default)

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Table 6-15. REG0x10_Charger_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	RESERVED	R/W	0h		Reserved

6.5.2.1.10 REG0x11_Charger_Control_3 Register (Address = 11h) [Reset = 74h]

REG0x11_Charger_Control_3 is shown in Figure 6-24 and described in Table 6-16.

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Figure 6-24. REG0x11_Charger_Control_3 Register

7	6	5	4	3	2	1	0
PFM_FWD_DIS	RESERVED		RESERVED	EN_OOA	RESERVED	EN_DITHER	
R/W-0h	R-3h		R-1h	R/W-0h	R-1h	R/W-0h	

Table 6-16. REG0x11_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PFM_FWD_DIS	R/W	0h	Reset by: REG_RESET	Disable PFM in forward buck mode 0b = Enable (Default) 1b = Disable
6:5	RESERVED	R	3h		Reserved
4	RESERVED	R	1h		Reserved
3	EN_OOA	R/W	0h		Out-of-Audio Enable Switching frequency reduces with diminishing load, under extreme light load condition the switching frequency could be lower than 25kHz which is already in audible frequency range. By configuring EN_OOA=1b, the minimum PFM burst frequency is clamped at around 25kHz to avoid any audible noise. 0b = No limit of PFM burst frequency (Default) 1b = Set minimum PFM burst frequency to above 25 kHz to avoid audio noise
2	RESERVED	R	1h		Reserved
1:0	EN_DITHER	R/W	0h	Reset by: REG_RESET	Frequency Dither configuration: 00b = Disable (Default) 01b = 1X 10b = 2X 11b = 3X

6.5.2.1.11 REG0x12_Charger_Control_4 Register (Address = 12h) [Reset = 40h]

REG0x12_Charger_Control_4 is shown in Figure 6-25 and described in Table 6-17.

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Figure 6-25. REG0x12_Charger_Control_4 Register

7	6	5	4	3	2	1	0
RESERVED	VBUS_OVP	RESERVED	FORCE_VBUS_DSCHG	RESERVED			
R-0h	R/W-1h	R-0h	R/W-0h	R-0h			

Table 6-17. REG0x12_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved

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Table 6-17. REG0x12_Charger_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	VBUS_OVP	R/W	1h	Reset by: REG_RESET	Set VBUS overvoltage protection threshold 0b = 6.0V 1b = 5.5V (Default)
5	RESERVED	R	0h		Reserved
4	FORCE_VBUS_DSCHG	R/W	0h	Reset by: REG_RESET	Enable VBUS pull down current source 0b = Disable (Default) 1b = Enable
3:0	RESERVED	R	0h		Reserved

6.5.2.1.12 REG0x13_Charger_Control_5 Register (Address = 13h) [Reset = 01h]

REG0x13_Charger_Control_5 is shown in Figure 6-26 and described in Table 6-18.

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Figure 6-26. REG0x13_Charger_Control_5 Register

7	6	5	4	3	2	1	0
BAT_COMP			VCLAMP			SET_CONV_FREQ	FORCE_VINDPM
R/W-0h			R/W-0h			R/W-0h	R/W-1h

Table 6-18. REG0x13_Charger_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	BAT_COMP	R/W	0h	Reset by: REG_RESET	IR Compensation Resistor Setting POR: 0mOhm (0h) Range: 0mOhm-140mOhm (0h-7h) Bit Step: 20mOhm
4:2	VCLAMP	R/W	0h	Reset by: REG_RESET	IR Compensation Voltage Clamp above VREG POR: 0mV (0h) Range: 0mV-140mV (0h-7h) Bit Step: 20mV
1	SET_CONV_FREQ	R/W	0h	Reset by: REG_RESET	Converter Frequency 0b = 1MHz (Default) 1b = 2MHz
0	FORCE_VINDPM	R/W	1h	Reset by: REG_RESET WATCHDOG	VINDPM threshold setting method 0b = Run relative VINDPM threshold 1b = Run absolute VINDPM threshold

6.5.2.1.13 REG0x14_MPPT_Control Register (Address = 14h) [Reset = AAh]

REG0x14_MPPT_Control is shown in Figure 6-27 and described in Table 6-19.

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Figure 6-27. REG0x14_MPPT_Control Register

7	6	5	4	3	2	1	0
VOC_PCT			VOC_DLY		VOC_RATE		EN_MPPT
R/W-5h			R/W-1h		R/W-1h		R/W-0h

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Table 6-19. REG0x14_MPPT_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	VOC_PCT	R/W	5h	Reset by: REG_RESET	Sets the input operating voltage (VINDPM) as a percentage of open-circuit voltage (VOC) 000b = 62.5% of VOC 001b = 68.75% of VOC 010b = 75% of VOC 011b = 78.125% of VOC 100b = 81.25% of VOC 101b = 84.375% of VOC (Default) 110b = 87.5% of VOC 111b = 93.75% of VOC
4:3	VOC_DLY	R/W	1h	Reset by: REG_RESET	Time delay before making VOC measurement after converter stops 00b = 50ms 01b = 300ms (Default) 10b = 2s 11b = 5s
2:1	VOC_RATE	R/W	1h	Reset by: REG_RESET	Time interval between two VOC measurements 00b = 30s 01b = 2min (Default) 10b = 10min 11b = 30min
0	EN_MPPT	R/W	0h	Reset by: REG_RESET	Enable MPPT routine 0b = Disable (Default) 1b = Enable

6.5.2.1.14 REG0x15_Charge_Timer_Control Register (Address = 15h) [Reset = C0h]

REG0x15_Charge_Timer_Control is shown in Figure 6-28 and described in Table 6-20.

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Figure 6-28. REG0x15_Charge_Timer_Control Register

7	6	5	4	3	2	1	0
EN_TMR2X	EN_SAFETY_TMRS	PRECHG_TMR	CHG_TMR	CHG_RATE		RESERVED	
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		R-0h	

Table 6-20. REG0x15_Charge_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_TMR2X	R/W	1h	Reset by: REG_RESET	2X charging timer control 0b = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1b = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
6	EN_SAFETY_TMRS	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable fast charge, pre-charge and trickle charge timers 0b = Disable 1b = Enable (default)
5	PRECHG_TMR	R/W	0h	Reset by: REG_RESET	Pre-charge safety timer setting 0b = 2 hrs (default) 1b = 0.5 hrs
4	CHG_TMR	R/W	0h	Reset by: REG_RESET	Fast charge safety timer setting 0b = 12 hrs (default) 1b = 24 hrs

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Table 6-20. REG0x15_Charge_Timer_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
3:2	CHG_RATE	R/W	0h	Reset by: REG_RESET	The charge rate used when device is in fast-charge. Once device enters JEITA region where charge current is reduced, the resulting current is = (ICHG * foldback ratio)/CHG_RATE: 00b = 1C (Default) 01b = 2C 10b = 4C 11b = 6C
1:0	RESERVED	R	0h		Reserved

6.5.2.1.15 REG0x16_NTC_Control_0 Register (Address = 16h) [Reset = 5Ah]

REG0x16_NTC_Control_0 is shown in Figure 6-29 and described in Table 6-21.

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Figure 6-29. REG0x16_NTC_Control_0 Register

7	6	5	4	3	2	1	0
TS_IGNORE	TS_TH_COLD	TS_TH_COOL		TS_TH_WARM		TS_TH_HOT	RESERVED
R/W-0h	R/W-1h	R/W-1h		R/W-2h		R/W-1h	R-0h

Table 6-21. REG0x16_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TS_IGNORE	R/W	0h	Reset by: REG_RESET WATCHDOG	Ignore the TS feedback, the charger will consider the TS is always good to allow charging, TS_STAT always reports TS_NORMAL 0b = Not ignore (Default) 1b = Ignore
6	TS_TH_COLD	R/W	1h	Reset by: REG_RESET	TS Cold Threshold 0b = -3°C 1b = 0°C (Default)
5:4	TS_TH_COOL	R/W	1h	Reset by: REG_RESET	TS COOL Treshold 00b = 5°C 01b = 10°C (Default) 10b = 15°C 11b = 20°C
3:2	TS_TH_WARM	R/W	2h	Reset by: REG_RESET	TS WARM Threshold 00b = 35°C 01b = 40°C 10b = 45°C (Default) 11b = 50°C
1	TS_TH_HOT	R/W	1h	Reset by: REG_RESET	TS Hot Threshold 0b = 55°C 1b = 60°C (Default)
0	RESERVED	R	0h		Reserved

6.5.2.1.16 REG0x17_NTC_Control_1 Register (Address = 17h) [Reset = 7Dh]

REG0x17_NTC_Control_1 is shown in Figure 6-30 and described in Table 6-22.

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Figure 6-30. REG0x17_NTC_Control_1 Register

7	6	5	4	3	2	1	0

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Figure 6-30. REG0x17_NTC_Control_1 Register (continued)

TS_VSET_WARM	TS_ISET_WARM	TS_VSET_COOL	TS_ISET_COOL
R/W-1h	R/W-3h	R/W-3h	R/W-1h

Table 6-22. REG0x17_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_VSET_WARM	R/W	1h	Reset by: REG_RESET	TS_WARM Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV (Default) 10b = Set VREG to VREG-100mV 11b = VREG unchanged
5:4	TS_ISET_WARM	R/W	3h	Reset by: REG_RESET	TS_WARM Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged (Default)
3:2	TS_VSET_COOL	R/W	3h	Reset by: REG_RESET	TS_COOL Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged (Default)
1:0	TS_ISET_COOL	R/W	1h	Reset by: REG_RESET	TS_COOL Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% (Default) 10b = Set ICHG to 40% 11b = ICHG unchanged

6.5.2.1.17 REG0x18_Charger_Status_0 Register (Address = 18h) [Reset = 00h]

REG0x18_Charger_Status_0 is shown in Figure 6-31 and described in Table 6-23.

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Figure 6-31. REG0x18_Charger_Status_0 Register

7	6	5	4	3	2	1	0
VBUS_STAT	VSYS_STAT	TREG_STAT	VINDPM_STAT	SAFETY_TMR_STAT	WD_STAT	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 6-23. REG0x18_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_STAT	R	0h	VBUS status: 0b = Not Powered from VBUS 1b = Powered from VBUS
6	VSYS_STAT	R	0h	VSYS Regulation Status 0b = Not in VSYSMIN regulation (BAT>VSYSMIN) 1b = In VSYSMIN regulation (BAT<VSYSMIN)
5	TREG_STAT	R	0h	IC Thermal regulation status 0b = Normal 1b = Device in thermal regulation
4	VINDPM_STAT	R	0h	VINDPM status 0b = Normal 1b = In VINDPM regulation
3	SAFETY_TMR_STAT	R	0h	Fast charge, trickle charge and pre-charge timer status 0b = Normal 1b = Safety timer expired

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Table 6-23. REG0x18_Charger_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WD_STAT	R	0h	I2C watch dog timer status 0b = Normal 1b = WD timer expired
1:0	RESERVED	R	0h	Reserved

6.5.2.1.18 REG0x19_Charger_Status_1 Register (Address = 19h) [Reset = 00h]

REG0x19_Charger_Status_1 is shown in Figure 6-32 and described in Table 6-24.

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Figure 6-32. REG0x19_Charger_Status_1 Register

7	6	5	4	3	2	1	0
CHG_STAT			RESERVED				
R-0h			R-0h				

Table 6-24. REG0x19_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	CHG_STAT	R	0h	Charge Status: 000b = Not Charging 001b = Trickle Charge 010b = Pre-charge 011b = Fast Charge (CC) 100b = Taper Charge (CV) 101b = Reserved 110b = Top-off Timer Active Charging 111b = Charge Termination Done
4:0	RESERVED	R	0h	Reserved

6.5.2.1.19 REG0x1A_FAULT_Status Register (Address = 1Ah) [Reset = 00h]

REG0x1A_FAULT_Status is shown in Figure 6-33 and described in Table 6-25.

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Figure 6-33. REG0x1A_FAULT_Status Register

7	6	5	4	3	2	1	0
VBUS_FAULT_STAT	BAT_FAULT_STAT	VSYS_FAULT_STAT	TSHUT_STAT	TS_STAT			RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h			R-0h

Table 6-25. REG0x1A_FAULT_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_STAT	R	0h	VBUS over-voltage status 0b = Normal 1b = Device in over voltage protection
6	BAT_FAULT_STAT	R	0h	Battery fault status 0b = Normal 1b = Dead, under-voltage, or over-voltage battery detected
5	VSYS_FAULT_STAT	R	0h	VSYS under voltage and over voltage status 0b = Normal 1b = SYS in SYS short circuit or over voltage

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Table 6-25. REG0x1A_FAULT_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TSHUT_STAT	R	0h	IC temperature shutdown status 0b = Normal 1b = Device in thermal shutdown protection
3:1	TS_STAT	R	0h	The TS temperature zone. 000b = TS_NORMAL 001b = TS_COLD 010b = TS_HOT 011b = TS_COOL 100b = TS_WARM
0	RESERVED	R	0h	Reserved

6.5.2.1.20 REG0x1B_Charger_Flag_0 Register (Address = 1Bh) [Reset = 00h]

REG0x1B_Charger_Flag_0 is shown in Figure 6-34 and described in Table 6-26.

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Figure 6-34. REG0x1B_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
VBUS_FLAG	VSYS_FLAG	TREG_FLAG	VINDPM_FLAG	SAFETY_TMR_FLAG	WD_FLAG	CHG_FLAG	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 6-26. REG0x1B_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FLAG	R	0h	Reset by: REG_RESET	VBUS status flag 0b = Normal 1b = VBUS status changed
6	VSYS_FLAG	R	0h		VSYS min regulation flag Access: R (ClearOnRead) 0b = Normal 1b = Entered or exited VSYS min regulation
5	TREG_FLAG	R	0h		IC Thermal regulation flag Access: R (ClearOnRead) 0b = Normal 1b = TREG signal rising threshold detected
4	VINDPM_FLAG	R	0h		VINDPM flag Access: R (ClearOnRead) 0b = Normal 1b = VINDPM regulation signal rising edge detected
3	SAFETY_TMR_FLAG	R	0h		Fast charge, trickle charge and pre-charge timer flag Access: R (ClearOnRead) 0b = Normal 1b = Fast charging timer expired rising edge detected
2	WD_FLAG	R	0h		I2C watchdog timer flag Access: R (ClearOnRead) 0b = Normal 1b = WD timer signal rising edge detected
1	CHG_FLAG	R	0h	Reset by: REG_RESET	Charge status flag 0b = Normal 1b = Charging status changed
0	RESERVED	R	0h		Reserved

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6.5.2.1.21 REG0x1C_FAULT_Flag Register (Address = 1Ch) [Reset = 00h]

REG0x1C_FAULT_Flag is shown in Figure 6-35 and described in Table 6-27.

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Figure 6-35. REG0x1C_FAULT_Flag Register

7	6	5	4	3	2	1	0
VBUS_FAULT_FLAG	BAT_FAULT_FLAG	VSYS_FAULT_FLAG	TSHUT_FLAG	TS_FLAG	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		

Table 6-27. REG0x1C_FAULT_Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_FLAG	R	0h	VBUS over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBUS OVP
6	BAT_FAULT_FLAG	R	0h	VBAT over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBAT OVP
5	VSYS_FAULT_FLAG	R	0h	VSYS over voltage and SYS short flag Access: R (ClearOnRead) 0b = Normal 1b = Stopped switching due to system over-voltage or SYS short fault
4	TSHUT_FLAG	R	0h	IC thermal shutdown flag Access: R (ClearOnRead) 0b = Normal 1b = TS shutdown signal rising threshold detected
3	TS_FLAG	R	0h	TS status flag Access: R (ClearOnRead) 0b = Normal 1b = A change to TS status was detected
2:0	RESERVED	R	0h	Reserved

6.5.2.1.22 REG0x1D_Charger_Mask_0 Register (Address = 1Dh) [Reset = 00h]

REG0x1D_Charger_Mask_0 is shown in Figure 6-36 and described in Table 6-28.

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Figure 6-36. REG0x1D_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
VBUS_MASK	VSYS_MASK	TREG_MASK	VINDPM_MASK	SAFETY_TMR_MASK	WD_MASK	CHG_MASK	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 6-28. REG0x1D_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_MASK	R/W	0h	Reset by: REG_RESET	VBUS status INT mask 0b = VBUS status change does produce INT 1b = VBUS status change does not produce INT

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Table 6-28. REG0x1D_Charger_Mask_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	VSYS_MASK	R/W	0h	Reset by: REG_RESET	VSYS min regulation INT mask 0b = Enter or exit VSYSMIN regulation does produce INT pulse 1b = Enter or exit VSYSMIN regulation does not produce INT pulse
5	TREG_MASK	R/W	0h	Reset by: REG_RESET	IC thermal regulation INT mask 0b = Entering TREG does produce INT 1b = Entering TREG does not produce INT
4	VINDPM_MASK	R/W	0h	Reset by: REG_RESET	VINDPM INT mask 0b = Enter VINDPM does produce INT pulse 1b = Enter VINDPM does not produce INT pulse
3	SAFETY_TMR_MASK	R/W	0h	Reset by: REG_RESET	Fast charge, trickle charge and pre-charge timer INT mask 0b = Fast charge, trickle charge or pre-charge timer expiration does produce INT 1b = Fast charge, trickle charge or pre-charge timer expiration does not produce INT
2	WD_MASK	R/W	0h	Reset by: REG_RESET	I2C watch dog timer INT mask 0b = I2C watch dog timer expired does produce INT pulse 1b = I2C watch dog timer expired does not produce INT pulse
1	CHG_MASK	R/W	0h	Reset by: REG_RESET	Charge status INT mask 0b = Charging status change does produce INT 1b = Charging status change does not produce INT
0	RESERVED	R/W	0h		Reserved

6.5.2.1.23 REG0x1E_FAULT_Mask Register (Address = 1Eh) [Reset = 00h]

REG0x1E_FAULT_Mask is shown in Figure 6-37 and described in Table 6-29.

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Figure 6-37. REG0x1E_FAULT_Mask Register

7	6	5	4	3	2	1	0
VBUS_FAULT_MASK	BAT_FAULT_MASK	VSYS_FAULT_MASK	TSHUT_MASK	TS_MASK	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		

Table 6-29. REG0x1E_FAULT_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	VBUS over-voltage INT mask 0b = Entering VBUS OVP does produce INT 1b = Entering VBUS OVP does not produce INT
6	BAT_FAULT_MASK	R/W	0h	Reset by: REG_RESET	IBAT/VBAT over-current/over-voltage INT mask 0b = Entering IBAT OCP or VBAT OVP does produce INT 1b = Entering IBAT OCP or VBAT OVP does not produce INT
5	VSYS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	VSYS over voltage and SYS short INT mask 0b = System over-voltage or SYS short fault does produce INT 1b = Neither system over voltage nor SYS short fault produces INT

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Table 6-29. REG0x1E_FAULT_Mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4	TSHUT_MASK	R/W	0h	Reset by: REG_RESET	IC thermal shutdown INT mask 0b = TSHUT does produce INT 1b = TSHUT does not produce INT
3	TS_MASK	R/W	0h	Reset by: REG_RESET	Temperature charging profile INT mask 0b = A change to TS temperature zone does produce INT 1b = A change to the TS temperature zone does not produce INT
2:0	RESERVED	R	0h		Reserved

6.5.2.1.24 REG0x1F_Part_Information Register (Address = 1Fh) [Reset = 01h]

REG0x1F_Part_Information is shown in Figure 6-38 and described in Table 6-30.

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Figure 6-38. REG0x1F_Part_Information Register

7	6	5	4	3	2	1	0
TEST_REV		PN				DEV_REV	
R-0h		R-0h				R-1h	

Table 6-30. REG0x1F_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TEST_REV	R	0h	Test Revision
5:2	PN	R	0h	Device Part number BQ25350: 0h
1:0	DEV_REV	R	1h	Device Revision

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an a buck-boost charger (Q1-Q4), and battery FET (BATFET Q5) between the system and battery.

7.2 Typical Application

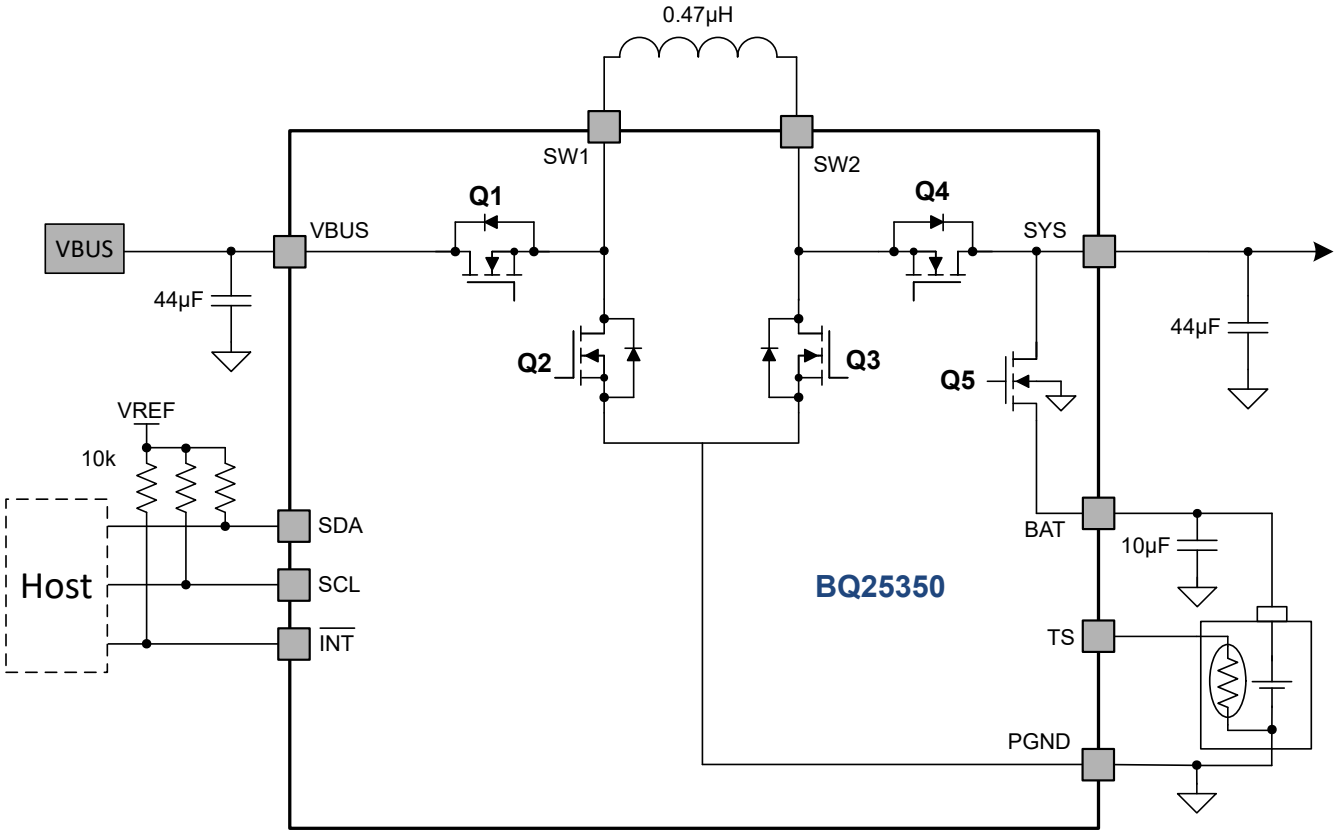


Figure 7-1. BQ25350 Typical Application

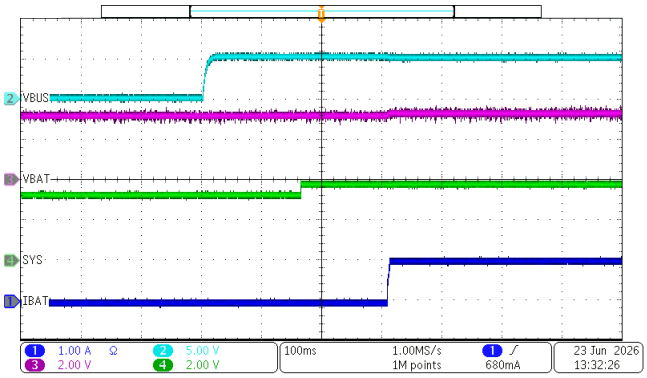
7.2.1 Design Requirements

Table 7-1. Design Requirements

PARAMETER	VALUE
VBUS range	2.5 - 5.5V
Fast charge current (REG0x02)	20-3020mA
Minimum system voltage (REG0x08)	2560-4000mV
Battery regulation voltage (REG0x04)	4200mV

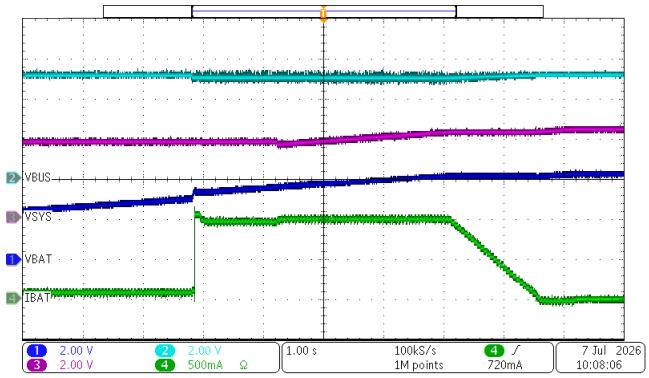
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7.2.2 Application Curves



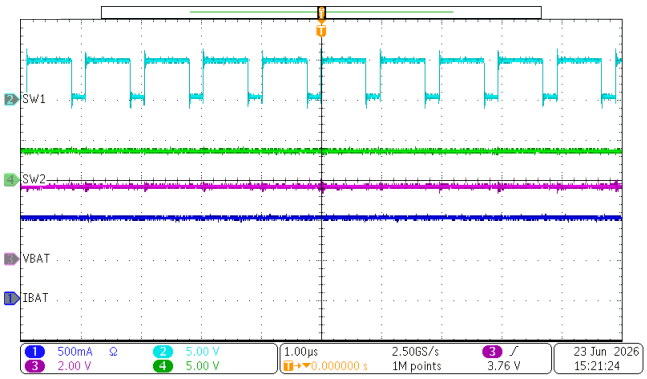
V_{BUS} = 5V
V_{SYSMIN} = 3.52V
V_{BAT} = 3.2V
I_{CHG} = 1A

Figure 7-2. Power-Up Sequence



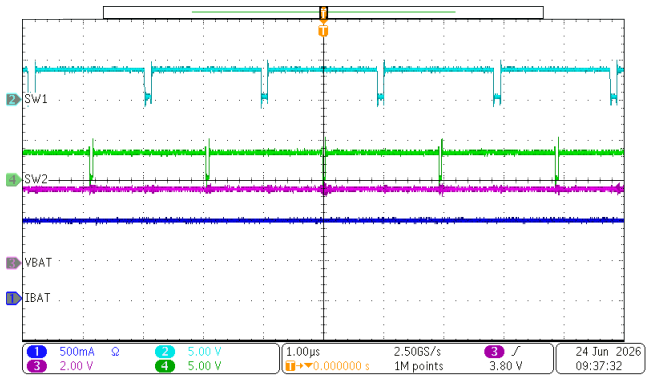
V_{BUS} = 5V
I_{CHG} = 1A
V_{SYSMIN} = 3.52V

Figure 7-3. Charging Profile



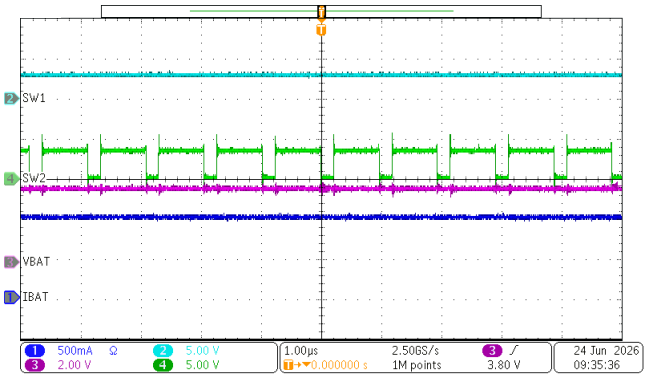
V_{BUS} = 5V
V_{SYSMIN} = 3.52V
V_{BAT} = 3.8V
V_{CHG} = 1A

Figure 7-4. Charging Switching Waveform - Buck



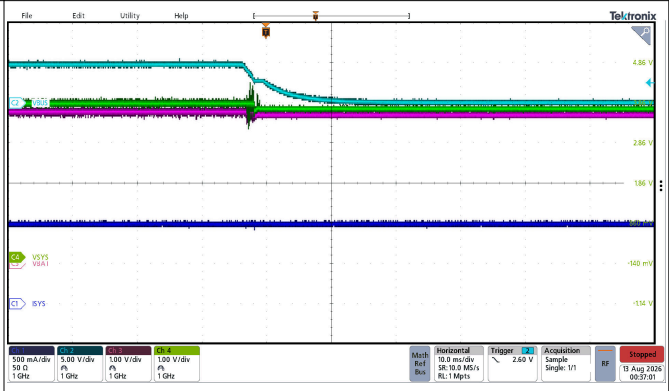
V_{BUS} = 3.8V
V_{SYSMIN} = 3.52V
V_{BAT} = 3.8V
V_{CHG} = 1A

Figure 7-5. Charging Switching Waveform - Buck-Boost



V_{BUS} = 3V
V_{SYSMIN} = 3.52V
V_{BAT} = 3.8V
V_{CHG} = 1A

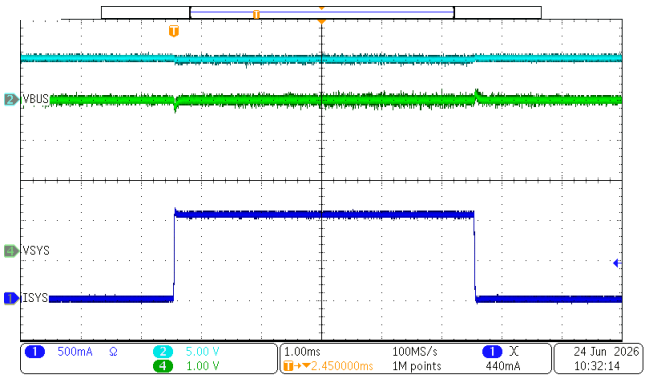
Figure 7-6. Charging Switching Waveform - Boost



V_{BUS} = 5 V
V_{SYSMIN} = 3.52V
V_{BAT} = 3.8V
I_{SYS} = 1A

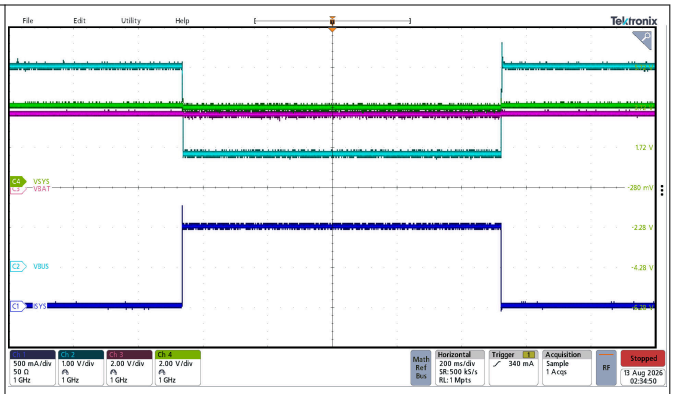
Figure 7-7. Shutdown VBUS Unplug

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V_{BUS} = 5 V
I_{CHG} = 1A
V_{BAT} = 3.8V
I_{SYS} = 0A - 1A - 0A

Figure 7-8. System Load Transient



V_{BUS} = 5 V
I_{CHG} = 0A
V_{BAT} = 3.8V
I_{SYS} = 0A - 1A - 0A

Figure 7-9. VINDPM Transient

7.3 Power Supply Recommendations

To provide an output voltage on SYS, the device requires a power supply lower than 6V with at least 100mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > V_{BAT_UVLO} connected to BAT.

7.4 Layout

7.4.1 Layout Guidelines

The switching node rise and fall times must be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to VBUS pin and GND pin connections.
2. Place inductor pins to SW pins as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
5. Verify that the number and sizes of vias allow enough copper for a given current path.

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7.4.2 Layout Example

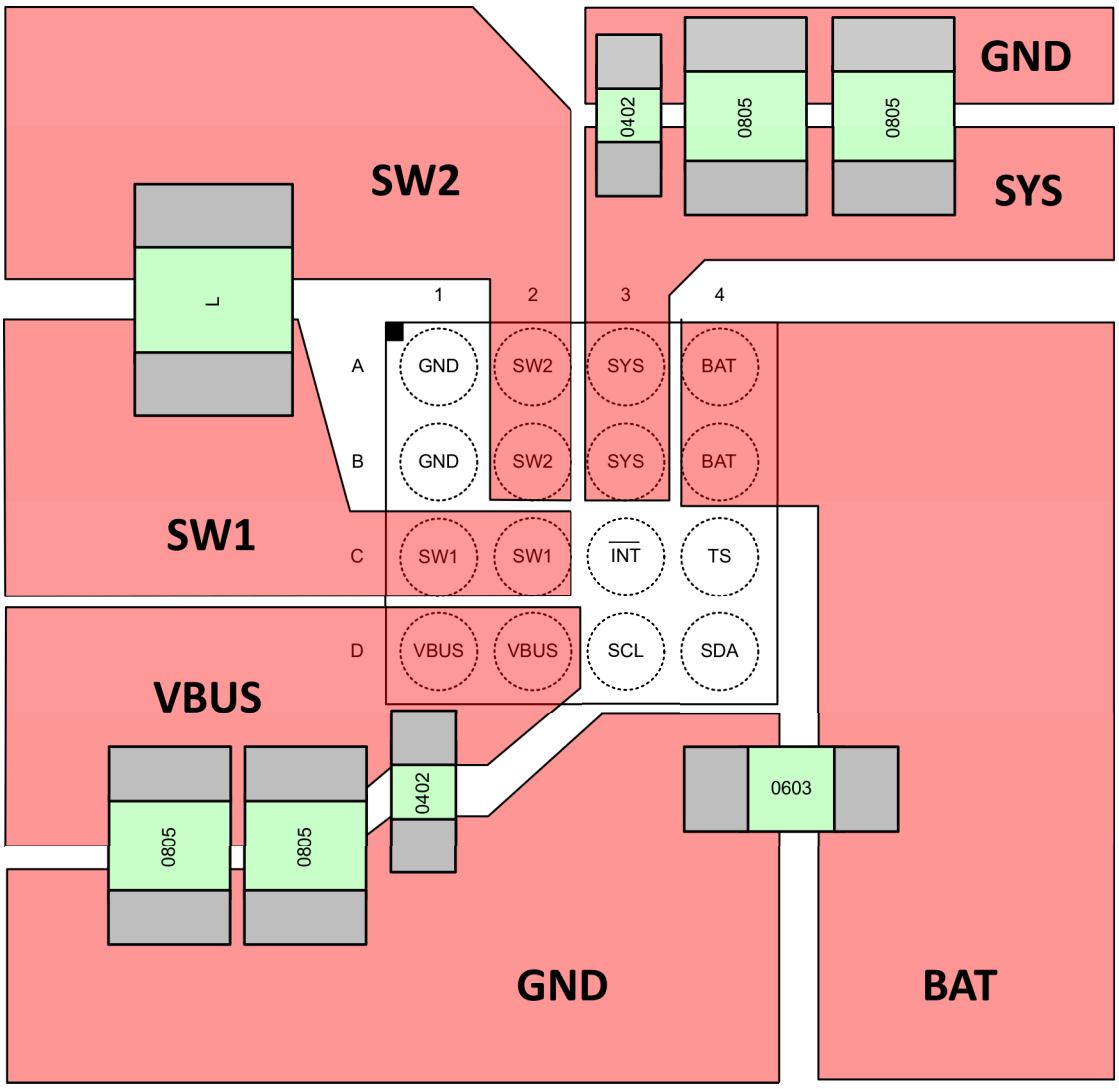


Figure 7-10. Layout of BQ25350

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2026) to Revision A (October 2026) — **Page**

- Removed REGN from pin max ratings 3
- Corrected ITERM value 15

DATE	REVISION	NOTES
August 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25350YBGR	Active	Production	DSBGA (YBG-16)	3000	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25350

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

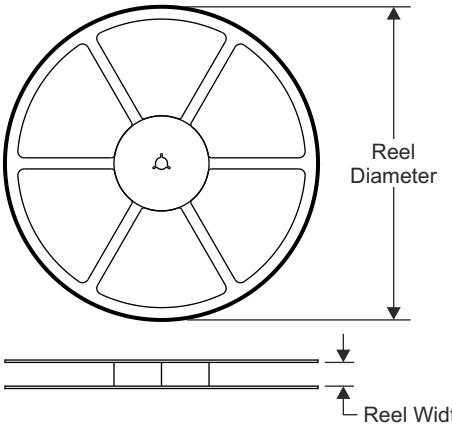
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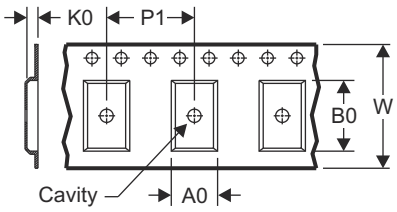
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10.1 Tape and Reel Information

REEL DIMENSIONS

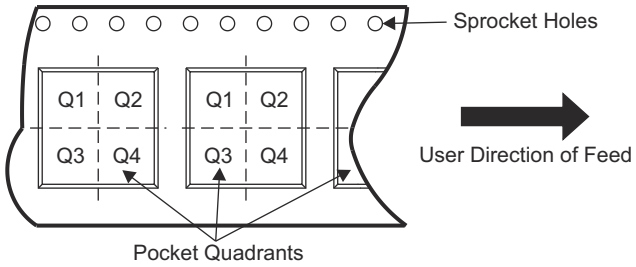


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

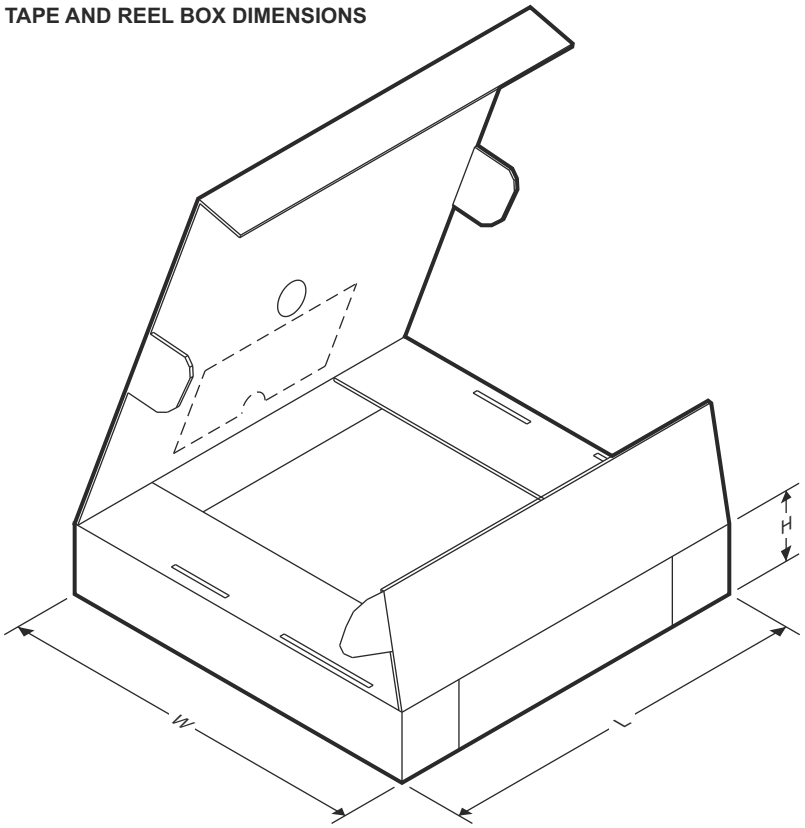
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25350YBGR	DSBGA	YBG	16	3000	180	8.4	2.14	2.14	0.7	4	12	Q1
BQ25350YBGR	DSBGA	YBG	16	3000	180	8.4	2.14	2.14	0.7	4	8	Q1

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TAPE AND REEL BOX DIMENSIONS

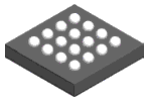


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25350YBGR	DSBGA	YBG	16	3000	182	182	20
BQ25350YBGR	DSBGA	YBG	16	3000	210	185	35

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10.2 Mechanical Data

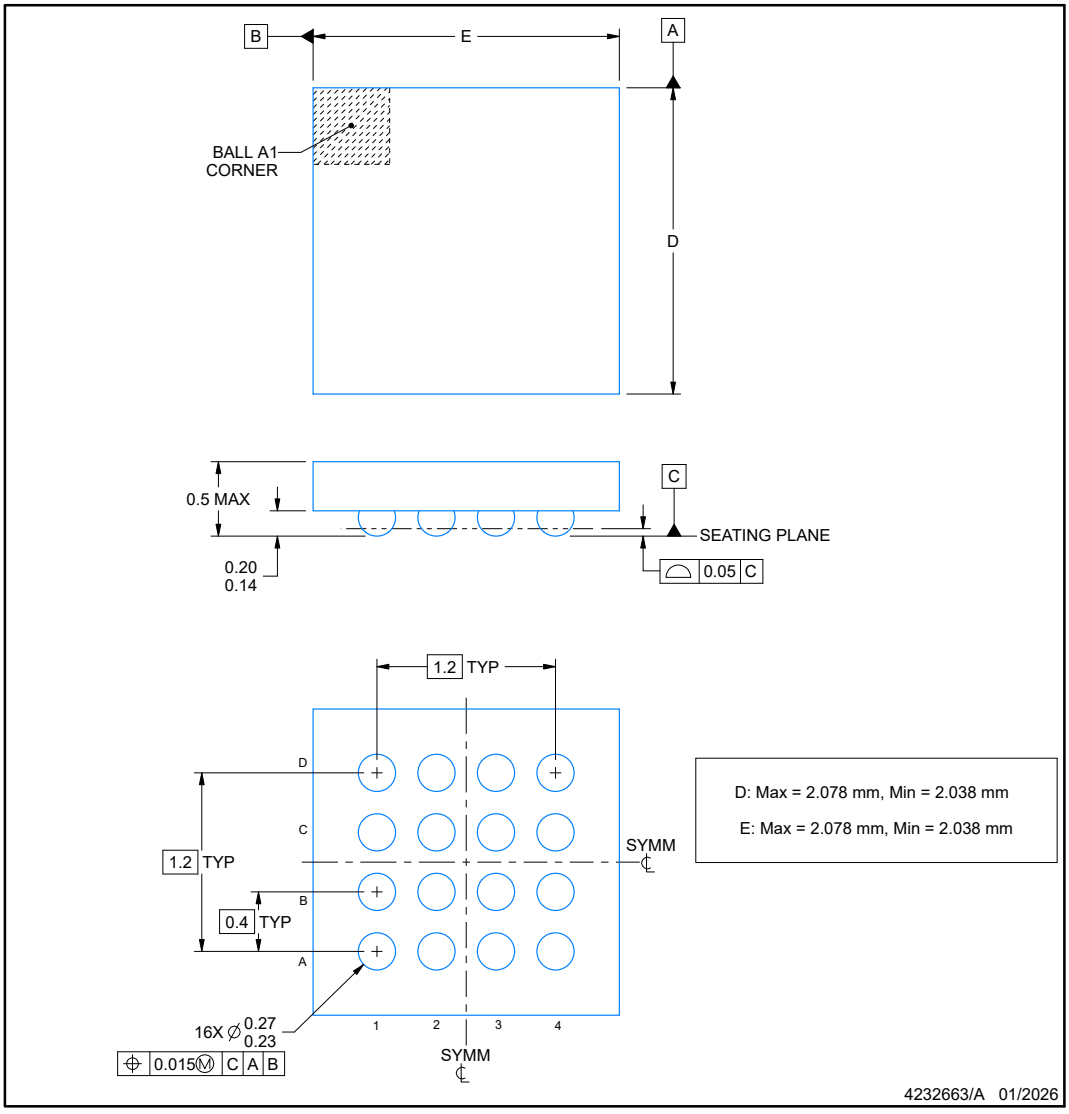
YBG0016-C02



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

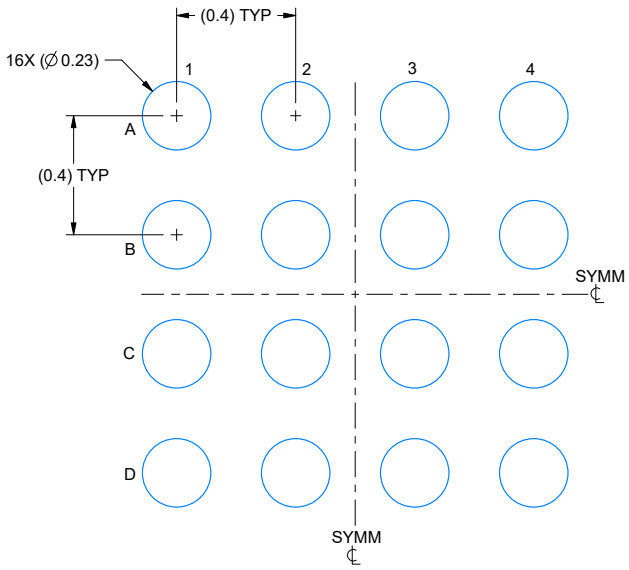
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EXAMPLE BOARD LAYOUT

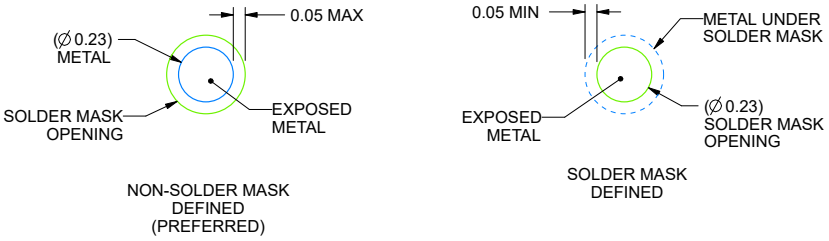
YBG0016-C02

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4232663/A 01/2026

NOTES: (continued)

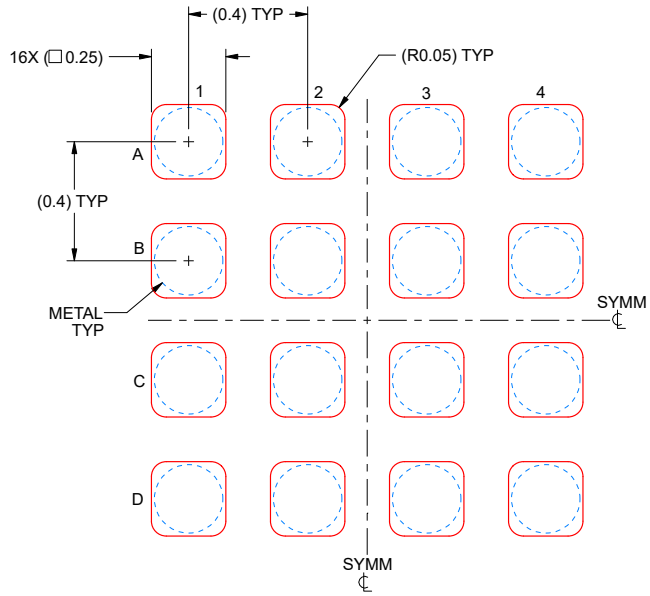
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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EXAMPLE STENCIL DESIGN

YBG0016-C02 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4232663/A 01/2026

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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