BQ27Z855 Dynamic Z-Track™ Battery Fuel Gauge with Integrated JEITA-Compliant Linear Battery Charger, Protection, and Authentication for 1-Series Cell Battery Packs

1 Features

- Fully integrated battery fuel gauge, linear battery charger, protector, and authenticator
- Battery chemistries supported include Li-ion with LCO, NMC, or LFP cathodes
- Battery fuel gauging based on patented Dynamic Z-Track™ technology
  - Automatically adjusts for aging, temperature, and rate-induced effects on the battery
- Fully featured battery linear charger
  - CC/CV charging up to 2A with JEITA-compliant integrated Advanced Charge Algorithm (ACA)
  - Dynamic Power Path Management
    - MINSYS mode to ensure system voltage does not drop below target threshold while charging with a weak input
    - SUPPLEMENT mode with ultra fast switching time to ensure system does not brown out during loads while charging
  - Ideal diode (ID) mode during discharge to prevent voltage drop to system load
  - PACK+ terminal voltage tolerance of +24V with 1kΩ RPACK value
- High-accuracy analog front end with two independent ADCs:
  - 18-bit low offset delta-sigma ADC for Coulomb counting with ±100mV input range
  - 16-bit delta-sigma ADC for cell voltage and internal and external temperature sensors
- Programmable safety and protection:
  - Hardware-level protections
    - Over Voltage Protection (OVP)
    - Under Voltage Protection (UVP)
    - Over Current Charging (OCC)
    - Over Current Discharging (OCD)
    - Short Circuit Discharging (SCD)
  - Firmware-level protections
    - OVP, UVP, OCC, and OCD
    - Under Temperature (UT)
    - Over Temperature (OT)
    - FET Failure (FETF)
    - Charge Timeout (CTO)
- ECC ECDSA authentication support with secure memory
- True zero-volt charging to support dead battery charging
- Integrated RTC with calendar and time of day
- Ultra-compact, 15-ball DSBGA package (YAH)

2 Applications

- Any end equipment with 1-series rechargeable batteries:
  - Personal electronics
  - Smartphones
  - Portable wearables/medical
  - Gaming

3 Description

The Texas Instruments BQ27Z855 Dynamic Z-Track™gas gauge solution is a fully integrated, accurate 1-series cell gas gauge, JEITA-compliant linear battery charger, protection, and authentication solution.

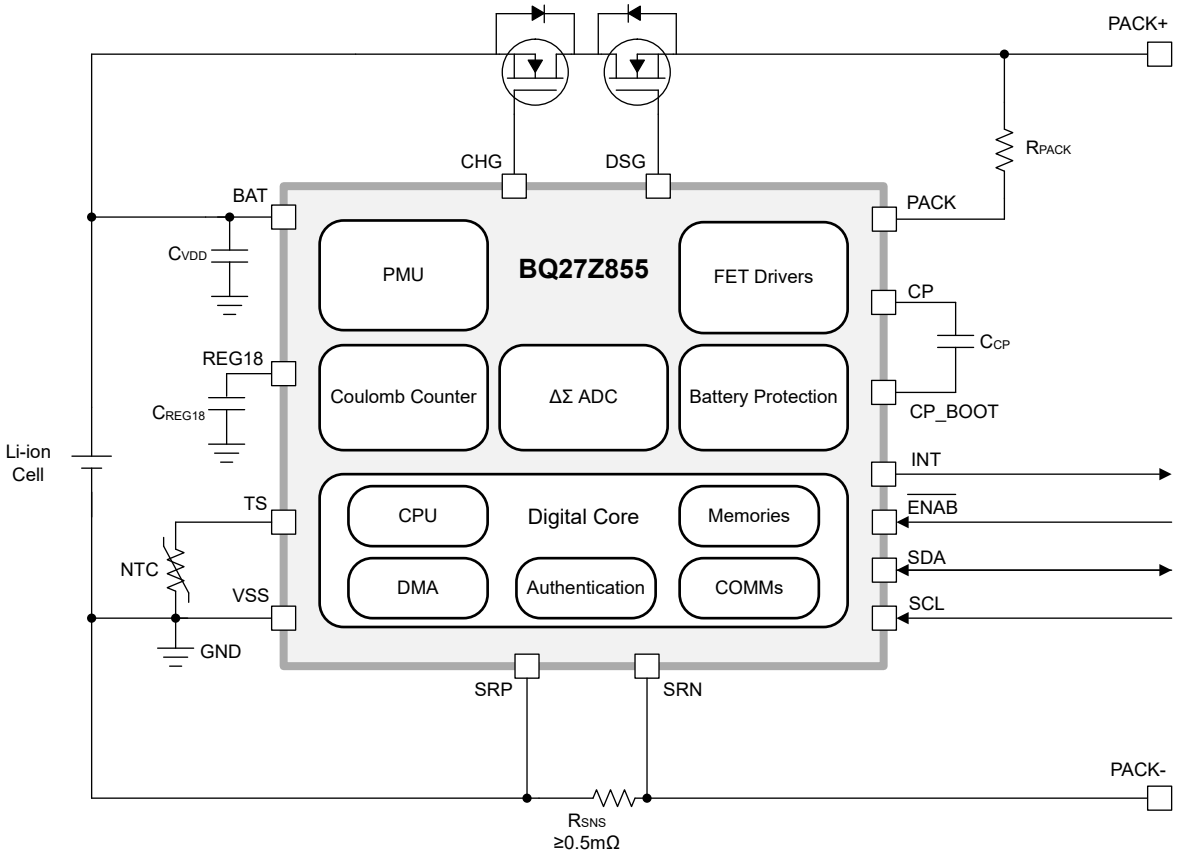
The BQ27Z855 gas gauge communicates through an I^2C compatible interface and combines an ultra-low power ARM M0 RISC processor, high accuracy analog measurement capabilities, integrated flash memory, high-side NMOS FET drivers, and ECC ECDSA authentication to provide a complete, high-performance battery management solution.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BQ27Z855	DSBGA (YAH, 15)	1.51mm × 2.55mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



BQ27Z855 Simplified Schematic

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4 Pin Configurations and Functions

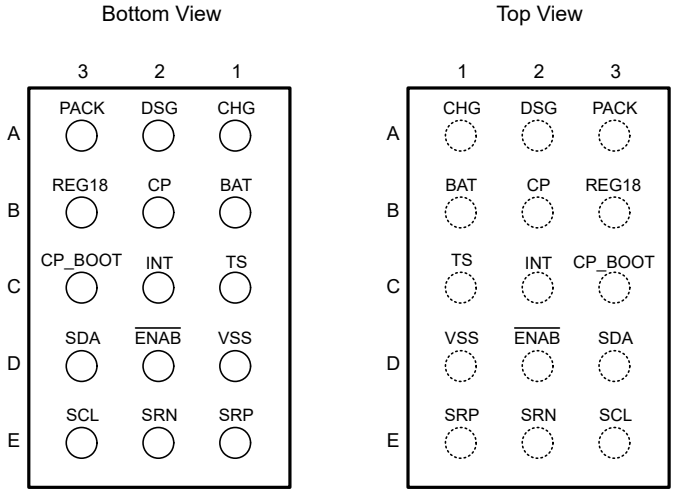


Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE(1)	
CHG	A1	AO	High-side NMOS charge FET driver output
DSG	A2	AO	High-side NMOS discharge FET driver output
PACK	A3	AI	Pack input voltage sensing pin and path for zero-volt charge (ZVCHG) current to flow within the device from PACK to BAT. Connect a series 500 Ω typical resistor (R_{PACK}) between the PACK pin and the PACK+ positive terminal.
BAT	B1	P, AI	LDO regulator input and battery voltage measurement sense input. Connect a capacitor (C_{BAT}) with the recommended typical capacitance of 1 µF between BAT and VSS. Place the capacitor close to the gauge.
CP	B2	AO	Internal charge pump connection to the top of an external bypass capacitor (C_{CP}) with the recommended typical capacitance of 1 µF. Connect the capacitor between CP and CP_BOOT. Place the capacitor close to the gauge.
REG18	B3	P	Internal regulator output. Requires a capacitor (C_{REG18}) with the recommended typical capacitance of 1.5 µF connected between REG18 and VSS. Place the capacitor close to the gauge.
TS	C1	AI	Thermistor input to VADC with internal 18 kΩ pull-up resistor. If not used, connect directly to VSS or leave floating and configure data flash accordingly.
INT	C2	I/O	Programmable output interrupt to host. Can also be configured as a programmable push-pull GPIO via device firmware. If not used, leave floating and configure data flash accordingly.
CP_BOOT	C3	AO	Internal charge pump connection to the bottom of an external bypass capacitor (C_{CP}) with the recommended typical capacitance of 1µF. Connect the capacitor between CP and CP_BOOT. Place the capacitor close to the gauge.
VSS	D1	P	Device ground
$\overline{\text{ENAB}}$	D2	I	Active low digital input with weak internal pull-up to BAT. Driving this signal to the PACK- battery pack terminal while the device is in a SHELF or SHUTDOWN mode will enable the device to wake up. If used, $\overline{\text{ENAB}}$ must be driven low with 1kΩ series resistor.
SDA	D3	I/O	Digital input, open drain output for I^2C serial data
SRP	E1	AI	Analog input pin connected to the internal Coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
SRN	E2	AI	Analog input pin connected to the internal Coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
SCL	E3	I/O	Digital input, open drain output for I^2C serial clock

(1) I/O = Digital Input/Output, AI = Analog Input, AO = Analog Output, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}	BAT	-0.3	6	V
Input voltage range, V_{IN}	BAT	-0.3	6	V
	PACK (R_{PACK} Shorted)	-0.3	8	
	PACK+ external battery pack input terminal with 1kΩ resistor in series to device PACK input pin	-0.3	24	
	$\overline{ENAB}$	-0.3	6	
	SDA, SCL	-0.3	6	
	INT, TS	-0.3	6	
	SRP, SRN	-0.3	V_{BAT} + 0.3	
Output voltage range, V_{OUT}	CHG, DSG	-0.3	8.5	V
	CP	-0.3	8.5	
	CP_BOOT	-0.3	2.1	
Output voltage range, V_{REG18}	REG18	-0.3	2	V
Junction temperature, T_J			105	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range	BAT	2.0		5.5	V
V_{IN}	Input voltage range	BAT	1.5		5.5	V
		PACK (with 1kΩ R_{PACK} current limit)	0		6	
		PACK (no R_{PACK} current limit)	0		5.5	
		$\overline{ENAB}$	-0.3		BAT	
		SDA, SCL	-0.3		3.6	
		TS	V_{SS}		V_{REG18}	
		SRP, SRN	V_{CCADC_CM} - 0.1		V_{CCADC_CM} + 0.1	

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Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OUT}	Output voltage range	INT	0		V_{REG18}	V
		CHG, DSG	V_{SS}		$V_{FET_ON(MAX)}$	
C_{BAT}(1)	External decoupling capacitor on BAT pin	Derated capacitance	0.5	1		µF
C_{REG18}(1)	External decoupling capacitor on REG18 pin	Derated capacitance	1	1.5	2	µF
C_{TS}(1)	External decoupling capacitor on TS pin	Derated capacitance			0.01	µF
C_{CP}(1)	External bypass capacitor between CP and CP_BOOT pins	Derated capacitance	0.5	1	2	µF
R_{PACK}(1)	External resistor from PACK+ terminal to device PACK pin	Nominal resistance, MIN/MAX is ±5% tolerance of nominal	0	500		Ω
R_{SENSE}(1)	External sense resistor between SRP and SRN pins		0.5			mΩ
T_A	Operating temperature	Operating ambient temeprature	-40		85	°C

(1) Specified by Design. Not production tested.

5.4 Thermal Information

THERMAL METRIC(1)		BQ27Z855 YAH 15 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.68	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.8	
Ψ_{JT}	Junction-to-top characterization parameter	0.09	
Ψ_{JB}	Junction-to-board characterization parameter	18.79	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Supply Current

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ACTIVE}(1)(2)	ACTIVE mode	V_{BAT} = 4V, CHG ON, DSG ON, No I²C communication		55		µA
I_{SLEEP}(1)(2)	SLEEP mode	Measured Current ≤ ***Sleep Current***(3), V_{BAT} = 4V, CHG ON, DSG ON, No I²C communication		30		µA
I_{SHIP}(1)(2)	SHIP mode	SHIP mode enabled, V_{BAT} = 4V, CHG ON, DSG ON, No I²C communication		30		µA
I_{SHELF}(1)(2)	SHELF mode	SHELF mode enabled, V_{BAT} = 4V, CHG OFF, DSG OFF, LFO ON for timekeeping, Wakeup via PACK detection and $\overline{ENAB}$ pin enabled		5.5		µA

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Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SHUTDOWN}$(1)	SHUTDOWN mode	SHUTDOWN mode enabled or V_{BAT} < ***Shutdown Voltage***(3), Wakeup via PACK detection and $\overline{ENAB}$ pin enabled		0.2		µA

(1) Specified by Bench Evaluation with device firmware. Not production tested.
(2) Average current over 60s with default firmware settings. Device power consumption dependent on firmware configuration.
(3) Firmware-based parameter. The data flash configuration value can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the BQ27Z855 Technical Reference Manual.

5.6 1.8V LDO Regulator (REG18)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG18}	Regulator output voltage	During device power-up	1.6	1.8	2.0	V
		After device power-up	1.74	1.8	1.86	
$\Delta V_{REG18TEMP}$ (2)	Regulator output change with temperature, $\Delta V_{REG18}/V_{REG18}$	I_{REG18} = 1mA	-1.7		1.1	%
$\Delta V_{REG18LINE}$	Line regulation, $\Delta V_{REG18}/\Delta V_{BAT}$	I_{REG18} = 1mA	-0.25		0.25	%
I_{REG18_SHORT}	Short circuit current limit	V_{REG18} = 0V	10		68	mA
V_{POR_TH}	POR threshold	Rising threshold	1.55	1.75	1.90	V
V_{POR_HYS}(2)	POR hysteresis		75	90	100	mV
V_{ENAB}(1)	$\overline{ENAB}$ pin voltage for device wake-up from SHELF or SHUTDOWN state	Active low falling threshold			0.65	V
R_{ENAB}(1)	$\overline{ENAB}$ pin pull-up resistance			1		MΩ
V_{WAKEUP}(1)	Minimum PACK pin voltage for device wake-up from SHELF or SHUTDOWN state			2.0		V

(1) Specified by Design. Not production tested.
(2) Specified by Characterization. Not production tested.

5.7 Low Frequency Oscillator (LFO)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{LFO}	Operating frequency			65.536		kHz
F_{LFO_DRIFT}(1) (2)	Frequency drift		-2.5		2.5	%

(1) Specified by Characterization. Not production tested.
(2) The frequency drift is included and measured from the trimmed frequency at T_A = 25°C, with the minimum and maximum based on characterization, actual value stored in OTP

5.8 High Frequency Oscillator (HFO)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{HFO}	Operating frequency			16.384		MHz

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Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{HFO_DRIFT} (1) (2)	Frequency drift	T_A = -25°C to 65°C	-2		2	%
		T_A = -40°C to 85°C	-3.5		3.5	

(1) Specified by Characterization. Not production tested.
(2) The frequency drift is included and measured from the trimmed frequency at T_A = 25°C, with the minimum and maximum based on characterization, actual value stored in OTP

5.9 PACK Clamp (PACK_CLAMP)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PACK_CLAMP}	Rising voltage on PACK when clamp is active and gauge is not in SHUTDOWN mode	I_{PACK_CLAMP} < 1mA, R_{PACK} = 1kΩ, SHUTDOWN mode not active	5.5		8	V
$V_{PACK_CLAMP_SHTDWN}$ (2)	Rising voltage on PACK when clamp is active and gauge is in SHUTDOWN mode	I_{PACK_CLAMP} < 1mA, R_{PACK} = 1kΩ, SHUTDOWN mode active			4	V
$I_{PACK_CLAMP_PEAK}$ (2)	Peak clamp current when clamp fully active	For a time < 2.5ms, R_{PACK} = 1kΩ			22	mA
$I_{PACK_CLAMP_ON}$ (1)	Clamp current when clamp fully active	R_{PACK} = 1kΩ		18	19	mA

(1) Specified by Characterization. Not production tested.
(2) Specified by Bench Evaluation. Not production tested.

5.10 Analog-to-Digital Converter (VADC)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_FS}	Battery voltage measurement full scale range	V_{IN} = V_{BAT}	-0.2		5.5	V
V_{BAT_ERR}	Battery voltage measurement error	V_{IN} = V_{BAT}, V_{BAT} = 2.5 to 5.0V, T_A = 25°C, Post-Calibration	-4	±2	4	mV
V_{TS_FS}	External thermistor voltage measurement full scale range	V_{IN} = V_{TS}	-0.2		V_{REG18}	V
t_{ADC_CONV} (4)	Conversion time	Single conversion		11.72		ms
B_{ADC_ER} (2)(3)	Effective resolution	Single conversion	14	15		bits
R_{VADC_IN} (1)	Effective input resistance			8		MΩ

(1) Specified by Design. Not production tested.
(2) Specified by Characterization. Not production tested.
(3) Effective Resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.
(4) Timing accuracy is relative to F_{LFO} accuracy

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5.11 Coulomb Counter (CCADC)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCADC_IN} (3)	Input voltage range		-100		100	mV
V_{CCADC_CM}	Common mode voltage range	V_{SS} = 0V, 2V ≤ V_{BAT} ≤ 5V	V_{SS}		V_{BAT}	V
V_{CCADC_IN}	Input voltage range with common mode voltage range		V_{CCADC_CM} - 0.1		V_{CCADC_CM} + 0.1	V
V_{CCADC_OFF} (2)	Offset error	18-bit, T_A = 25℃, Post-Calibration	-2		2	LSB(3)
R_{CCADC_IN} (1)	Effective input resistance			1.5		MΩ

(1) Specified by Design. Not production tested.
(2) Specified by Characterization. Not production tested.
(3) The LSB size for an 18-bit, 1000ms CCADC result is 923nV

5.12 Coulomb Counter Digital Filter (CC1)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CC1_CONV} (4)	Conversion time	Single conversion		1000		ms
B_{CC1_ER} (1)(2)(3)	Effective resolution	Single conversion		18		bits

(1) Specified by Characterization. Not production tested.
(2) Effective Resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.
(3) Input signal DC = ±1mV, Harmonic Free Full Scale
(4) Timing accuracy is relative to F_{LFO} accuracy

5.13 Current Measurement Digital Filter (CC2)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CC2_CONV} (4)	Conversion time	Single conversion		11.72		ms
B_{CC2_ER} (1)(2)(3)	Effective resolution	Single conversion	14	15		bits

(1) Specified by Characterization. Not production tested.
(2) Effective Resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.
(3) Input signal DC = ±1mV, Harmonic Free Full Scale
(4) Timing accuracy is relative to F_{LFO} accuracy

5.14 Charge Current Measurement Digital Filter (CC3)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CC3_CONV} (4)	Conversion time	Single conversion		11.72		ms
B_{CC3_ER} (1)(2)(3)	Effective resolution	Single conversion	14	15		bits

(1) Specified by Characterization. Not production tested.
(2) Effective Resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.
(3) Input signal DC = ±1mV, Harmonic Free Full Scale
(4) Timing accuracy is relative to F_{LFO} accuracy

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5.15 Wake-up Comparator (I-WAKE)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE_THR} (1) (3)	Wake-up voltage threshold range	Nominal settings, threshold based on $V_{SRP} – V_{SRN}$, 0.5mV steps, typical value is default threshold	-7.5	±4.5	7.5	mV
$V_{WAKE_THR_ERR}$ (2)	Wake-up voltage threshold error	All V_{WAKE_THR} settings, $V_{WAKE} = V_{SRP} – V_{SRN}$	–1000		1000	µV

(1) Specified by Design. Not production tested.
(2) Specified by Characterization. Not production tested.
(3) Specified typical value is the factory default setting. The setting in data flash can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the BQ27Z855 Technical Reference Manual.

5.16 Internal Temperature Sensor (INT_TEMP)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INT_TEMP} (1)	Internal temperature sensor voltage drift	V_{INT_TEMP}	-1.96	-1.83	-1.71	mV/°C

(1) Specified by Characterization. Not production tested.

5.17 Thermistor Measurement Support

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TS_PU}	Internal pull-up resistance	Setting for nominal 18kΩ	14.4	18	21.6	kΩ
$R_{TS_PU_DRIFT}$ (1)	Resistance drift over temperature	Change over –40°C to +85°C vs value at 25°C for nominal 18-kΩ	-200		200	Ω

(1) Specified by Characterization. Not production tested.

5.18 Hardware-based Protection (SCOMP) Thresholds (OVP, UVP, OCC, OCD, SCD)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP} (1)(4)	Hardware overvoltage protection (OVP) detection range	$V_{IN} = V_{BAT}$, threshold range, 50mV steps, typical value is default	3500	4300	5000	mV
V_{OVP_ACC} (2)(3)	Hardware OVP detection accuracy	$V_{IN} = V_{BAT}$, T_A = 0°C to 60°C, C_{LOAD} at CHG/DSG < 1uA	–25		25	mV
		$V_{IN} = V_{BAT}$, T_A = -40°C to 85°C, C_{LOAD} at CHG/DSG < 1uA	–53		53	mV
V_{UVP} (1)(4)	Hardware undervoltage protection (UVP) detection range	$V_{IN} = V_{BAT}$, threshold range, 50mV steps, typical value is default	2000	2300	4000	mV
V_{UVP_ACC} (2)(3)	Hardware UVP detection accuracy	$V_{IN} = V_{BAT}$, T_A = 0°C to 60°C, C_{LOAD} at CHG/DSG < 1uA	-30		30	mV
		$V_{IN} = V_{BAT}$, T_A = -40°C to 85°C, C_{LOAD} at CHG/DSG < 1uA	-50		50	mV
$R_{PACK-VSS}$	Resistance between PACK and VSS	SHELF and SHUTDOWN modes only	100	300	550	kΩ
V_{OCC} (1)(4)	Hardware overcurrent in charge (OCC) detection range	$V_{IN} = V_{SRP} - V_{SRN}$, threshold range, 1mV steps, typical value is default	4	14	100	mV

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Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCD} (1)(4)	Hardware overcurrent in discharge (OCD) detection range	$V_{IN} = V_{SRP} - V_{SRN}$, threshold range, 1mV steps, typical value is default	–4	-16	–100	mV
V_{SCD} (1)(4)	Hardware short circuit current in discharge (SCD) detection range	$V_{IN} = V_{SRP} - V_{SRN}$, threshold range, 1mV steps, typical value is default	–5	-20	–120	mV
V_{OCx_ACC} (2)	Overcurrent (OCC, OCD, SCD) detection accuracy	$V_{IN} = V_{SRP} - V_{SRN}$, |Setting| < 20mV, T_A = -25ºC to 65ºC	-2.1		2.1	mV
		$V_{IN} = V_{SRP} - V_{SRN}$, |Setting| < 20mV	-2.1		2.1	mV
		$V_{IN} = V_{SRP} - V_{SRN}$, |Setting| = 20 to 55mV	-3		3	mV
		$V_{IN} = V_{SRP} - V_{SRN}$, |Setting| = 56 to 100mV	-5		5	mV
		$V_{IN} = V_{SRP} - V_{SRN}$, |Setting| > 100mV	-12		12	mV

(1) Specified by Design. Not production tested.
(2) Specified by Characterization. Not production tested.
(3) Accuracy assured by specified default threshold.
(4) Specified typical value is the factory default setting. The setting in data flash can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the BQ27Z855 Technical Reference Manual.

5.19 Hardware-based Protections (SCOMP) Timing (OVP, UVP, OCC, OCD, SCD)

Typical values stated where T_A = 25°C and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40°C to 85°C and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP} (1)(2)(3)	OVP detection delay options	Configurable with 8191 delay steps. To calculate expected delay time = 1.708 + DelayStep# * 0.854 . Factory default = 1171 counts = 1.708 + 1171 * 0.854 = 1001ms	2.56	1001	6996	ms
t_{UVP} (1)(2)(3)	UVP detection delay options	Configurable with 255 delay steps. To calculate expected delay time = 1.708 + DelayStep# * 0.854 . Factory default = 117 counts = 1.708 + 117 * 0.854 = 101ms	2.56	101	219	ms
t_{OCC} (1)(2)(3)	OCC detection delay options	Configurable with 127 delay steps. To calculate expected delay time = 1.708 + DelayStep# * 0.854 . Factory default = 10 counts = 1.708 + 10 * 0.854 = 10.2ms	2.56	10.2	110	ms
t_{OCD} (1)(2)(3)	OCD detection delay options	Configurable with 127 delay steps. To calculate expected delay time = 1.708 + DelayStep# * 0.854 . Factory default = 18 counts = 1.708 + 18 * 0.854 = 17ms	2.56	17	110	ms
t_{SCD} (1)(2)(3)	SCD detection delay options	Configurable with 7 delay options. To calculate expected delay time = DelayStep# * 0.122 + 0.2745 Factory default = 1 count = 1 * 0.122 + 0.2745	396	396	1128	µs
t_{WAKE_CC} (1)(2)(3)	Current wake in charge detection delay options	Configurable with 31 delay steps. To calculate expected delay time = 1.708 + (14 + DelayStep# - 2) * 0.854 . Factory default = 7 counts = 1.708 (14 + 7 - 2) * 0.854 = 17.93ms	12.81	17.93	38.43	ms

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Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE_CD} (1)(2)(3)	Current wake in discharge detection delay options	Configurable with 31 delay steps. To calculate expected delay time = 1.708 + (14 + DelayStep# - 2) * 0.854 . Factory default = 7 counts = 1.708 (14 + 7 - 2) * 0.854 = 17.93ms	12.81	17.93	38.43	ms

(1) Specified by Bench Evaluation. Not production tested.
(2) Specified typical value is the factory default setting. The setting in data flash can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the BQ27Z855 Technical Reference Manual.
(3) Not including LFO Frequency Error

5.20 Linear Battery Charger

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Constant Voltage (CV) Regulation						
$V_{BAT_REG_RNG}$ (1)(4)	BAT charge voltage regulation range	Firmware programmable range, 10mV steps	3500	4200	4650	mV
$V_{BAT_REG_ACC}$ (2)	BAT charge voltage accuracy	All V_{BAT_REG} settings, typical measurement at V_{BAT_REG} = 4200mV, Post-Calibration	-0.5		0.5	%
Constant Current (CC) Regulation						
I_{CHG_RNG} (1)(3)(4)	Charge current regulation range	Firmware programmable range	5		2000	mA
I_{CHG_ACC} (2)	Charge current accuracy	V_{SRP} - V_{SRN}, I_{CHG} = 50mA, R_{SENSE} = 10mΩ, Post-Calibration	45	50	55	mA
I_{CHG_ACC} (2)	Charge current accuracy	V_{SRP} - V_{SRN}, I_{CHG} = 150mA, R_{SENSE} = 10mΩ, Post-Calibration	135	150	165	mA
I_{CHG_ACC} (2)	Charge current accuracy	V_{SRP} - V_{SRN}, I_{CHG} = 800mA, R_{SENSE} = 10mΩ, Post-Calibration	720	800	880	mA
I_{TERM_RNG} (1)(4)	Termination current regualtion range	Firmware programmable range	1		400	mA
I_{TERM_ACC} (2)	Termination current accuracy	V_{SRP} - V_{SRN}, T_A = 25℃, V_{BAT_REG} = 4.2V, I_{TERM} = 5mA, R_{SENSE} = 10mΩ, Post-Calibration	4	5	6	mA
Linear and MINSYS Modes						
V_{LIN_RNG}	Linear mode operating voltage range	Linear mode starts (V_{LIN_START}) at V_{BAT} = 2.4V with V_{BAT} rising after firmware-based exit from ZVCHG	2.05		5.0	V
V_{MINSYS} (1)(4)	PACK voltage threshold when charge current is reduced	Firmware programmable range, 25mV steps	2750	3800	4500	mV
V_{MINSYS_ACC}	V_{MINSYS} accuracy	DC accuracy	-200		200	mV
V_{DPPM}	Recommended PACK-BAT differential for linear charging	Linear mode		200		mV
Supplement Mode and Ideal Diode (ID) Modes						
V_{TH_ON}	Supplement Mode or ID_ON entry threshold	V_{BAT} = 3.6V, V_{BAT} > V_{UVP}, V_{PACK} (5) – V_{BAT}, R_{PACK} = 1kΩ	-27.5	-20	-15	mV
V_{TH_OFF}	Supplement mode exit threshold	V_{BAT} = 3.6V, V_{BAT} > V_{UVP}, V_{PACK} (5) – V_{BAT}, R_{PACK} = 1kΩ	-10	-5	-1	mV
	ID_OFF entry threshold	V_{BAT} = 3.6V, V_{BAT} > V_{UVP}, V_{PACK} (5) – V_{BAT}, R_{PACK} = 1kΩ	1	5	10	

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Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TH_OFF_FINE}$	Supplement or ID charge current detection threshold	V_{SRP} - V_{SRN}		450		µV

(1) Specified by Design. Not production tested.
(2) Specified by Bench Evaluation. Not production tested.
(3) Includes precharge (PCHG) and fast charge current settings
(4) Specified typical value is the factory default setting. The setting in data flash can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the BQ27Z855 Technical Reference Manual.
(5) Including R_{PACK} error

5.21 CHG, DSG NFET Drivers

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DSG_ON}	DSG FET driver ON output voltage	C_{LOAD} = 10nF, V_{BAT} ≥ 4V	7.9	8.2	8.4	V
		C_{LOAD} = 10nF, V_{BAT} < 4V	1.95 × V_{BAT}	2 × V_{BAT}	2.1 × V_{BAT}	
V_{CHG_ON}	CHG FET driver ON output voltage	C_{LOAD} = 10nF, V_{BAT} ≥ 4V	7.9	8.2	8.4	V
		C_{LOAD} = 10nF, V_{BAT} < 4V	1.95 × V_{BAT}	2 × V_{BAT}	2.1 × V_{BAT}	
V_{DSG_OFF}	DSG FET driver OFF output voltage	C_{LOAD}= 10nF, V_{DSG_OFF} = V_{DSG} - V_{SS}			0.1	V
V_{CHG_OFF}	CHG FET driver OFF output voltage	C_{LOAD}= 10nF, V_{CHG_OFF} = V_{CHG} - V_{SS}			0.1	V
t_{DSG_RISE}(1)	DSG FET driver rise time	C_{LOAD} = 10nF, V_{DSG_ON} changes from 10% to 90% of V_{BAT} to $V_{DSG_ON(TYP)}$		400	800	µs
t_{CHG_RISE}(1)	CHG FET driver rise time without CP capacitor	C_{LOAD} = 10nF, V_{CHG_ON} changes from 10% to 90% of V_{BAT} to $V_{CHG_ON(TYP)}$		400	800	µs
t_{FET_FALL}(1)	DSG and CHG FET driver fall time	C_{LOAD} = 10nF, V_{FET} changes from $V_{FET_ON(TYP)}$ to V_{FET_OFF}		50	200	µs

(1) Specified by Bench Evaluation. Not production tested.

5.22 Zero-Volt Charging (ZVCHG)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ZVCHG}	Zero-volt charging current	V_{PACK+} = 5V, V_{BAT} = 0V, R_{PACK} = 1kΩ			5	mA

5.23 General Purpose Input-Outputs (INT)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	INT	0.7 × V_{REG18}			V
V_{IL}	Low-level input voltage	INT			0.3 × V_{REG18}	V
V_{OH}	Output voltage high	INT, I_{OH} = -450µA	0.85 × V_{REG18}			V
V_{OL}	Output voltage low	INT, I_{OL} = 1mA			0.35	V
R_{PD}	Internal pull-down resistance	INT	80	100	120	kΩ

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Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PU}	Internal pull-up resistance	INT	80	100	120	kΩ
C_{IN}(1)	Input capacitance	INT		1.5		pF
I_{LKG}(1)	Input leakage current	INT		1		µA

(1) Specified by Design. Not production tested.

5.24 I²C Interface I/O (SDA, SCL)

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDIO}	External I/O supply voltage		1.1		3.6	V
V_{IH}	Input voltage high	SDA, SCL	0.7 × V_{DDIO}			V
V_{IL}	Input voltage low	SDA, SCL			0.3 × V_{DDIO}	V
V_{OL}	Output low voltage	SDA, SCL, I_{OL} = –3mA			0.4	V
C_{IN} (1)	Input capacitance	SDA, SCL			10	pF
I_{LKG}(1)	Input leakage current	SDA, SCL		0.5		µA

(1) Specified by Design. Not production tested.

5.25 I²C Interface Timing

Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I²C 100kHz						
f_{SCL}(1)	Clock frequency				100	kHz
$t_{HD:STA}$(1)	START condition hold time		4			µs
t_{LOW}(1)	Low period of SCL clock		4.7			µs
t_{HIGH}(1)	High period of SCL clock		4			µs
$t_{SU:STA}$(1)	Setup time for repeated START		4.7			µs
$t_{HD:DAT}$(1)	Data in hold time		0			µs
$t_{SU:DAT}$(1)	Data in setup time		250			ns
	Data out setup time		250			
t_r(1)(2)	SDA and SCL rise time	30% to 70% of V_{DDIO}			1000	ns
t_F(1)(2)	SDA and SCL fall time	30% to 70% of V_{DDIO}			300	ns
$t_{SU:STO}$(1)	STOP condition setup time		4			µs
t_{BUF}(1)	Bus free time between STOP and START		4.7			µs
C_D	Capacitive load for each bus line				400	pF
I²C 400kHz						
f_{SCL}(1)	Clock frequency				400	kHz
$t_{HD:STA}$(1)	START condition hold time		0.6			µs
t_{LOW}(1)	Low period of SCL clock		1.3			µs
t_{HIGH}(1)	High period of SCL clock		0.6			µs
$t_{SU:STA}$(1)	Setup time for repeated START		0.6			µs
$t_{HD:DAT}$(1)	Data in hold time		0			µs

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Typical values stated where T_A = 25℃ and V_{BAT} = 3.8V, MIN/MAX values stated where T_A = -40℃ to 85℃ and V_{BAT} = 2.0V to 5.0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{SU:DAT}$(1)	Data in setup time		100			ns
	Data out setup time		100			
t_r(1)(2)	SDA and SCL rise time	30% to 70% of V_{DDIO}	20		300	ns
t_F(1)(2)	SDA and SCL fall time	30% to 70% of V_{DDIO}	20 × (V_{DDIO}/ 5.5)		300	ns
$t_{SU:STO}$(1)	STOP condition setup time		0.6			µs
t_{BUF}(1)	Bus free time between STOP and START		1.3			µs
C_D	Capacitive load for each bus line				400	pF
I²C 1MHz						
f_{SCL}(1)	Clock frequency				1000	kHz
$t_{HD:STA}$(1)	START condition hold time		0.26			µs
t_{LOW}(1)	Low period of SCL clock		0.5			µs
t_{HIGH}(1)	High period of SCL clock		0.26			µs
$t_{SU:STA}$(1)	Setup time for repeated START		0.26			µs
$t_{HD:DAT}$(1)	Data in hold time		0			µs
$t_{SU:DAT}$(1)	Data in setup time		50			ns
	Data out setup time		50			
t_r(1)(2)	SDA and SCL rise time	30% to 70% of V_{DDIO}			120	ns
t_F(1)(2)	SDA and SCL fall time	30% to 70% of V_{DDIO}	20 × (V_{DDIO}/ 5.5)		120	ns
$t_{SU:STO}$(1)	STOP condition setup time		0.26			µs
t_{BUF}(1)	Bus free time between STOP and START		0.5			µs
C_D	Capacitive load for each bus line				100	pF

(1) Specified by Characterization. Not production tested.
(2) V_{DDIO} = 1.2V

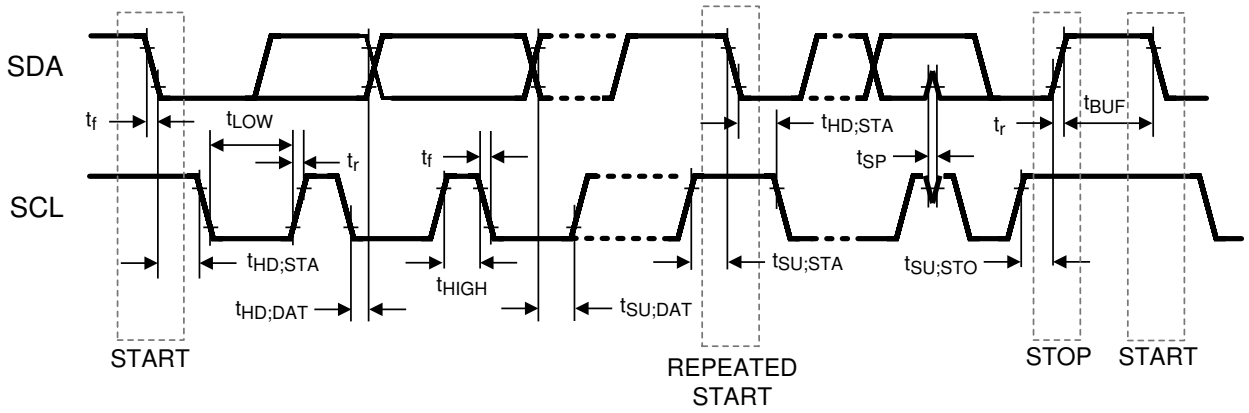


Figure 5-1. I²C Timing Diagram

5.26 Typical Characteristics

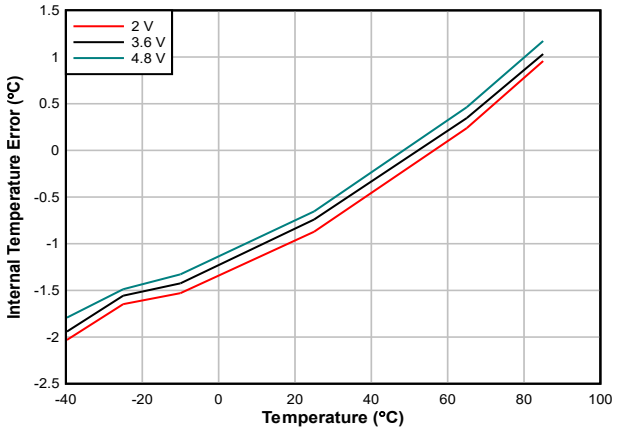


Figure 5-2. Internal Temperature Error vs Battery Voltage and Temperature

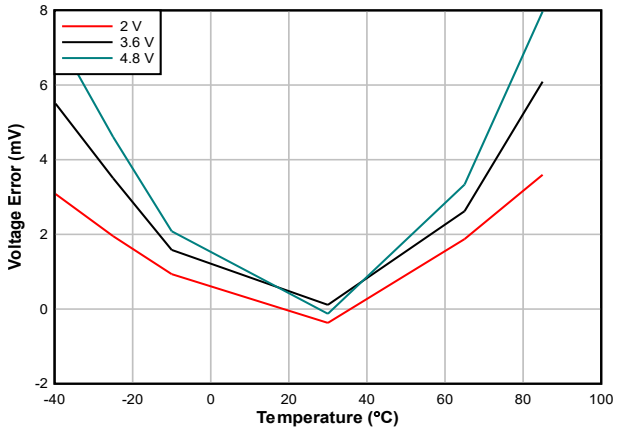


Figure 5-3. Cell Voltage Error vs Battery Voltage and Temperature

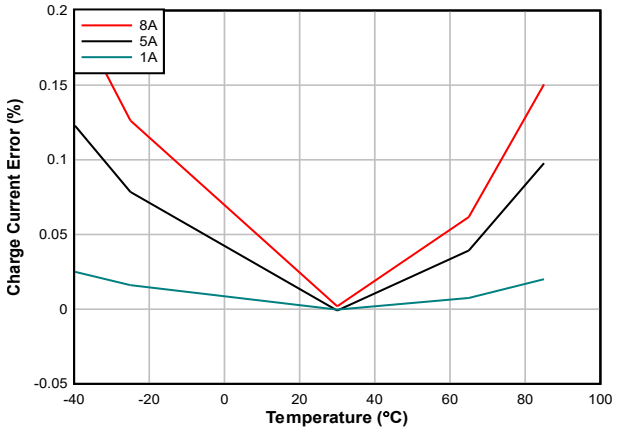


Figure 5-4. Charge Current Error vs Temperature and Charger Current with 10mΩ sense, After Calibration

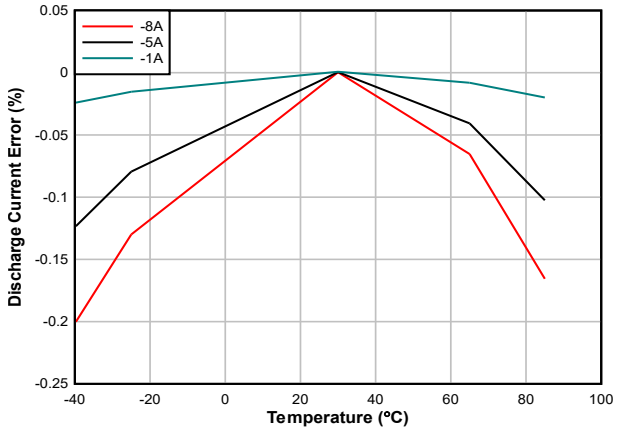


Figure 5-5. Discharge Current Error vs Temperature and Load Current with 10mΩ sense, After Calibration

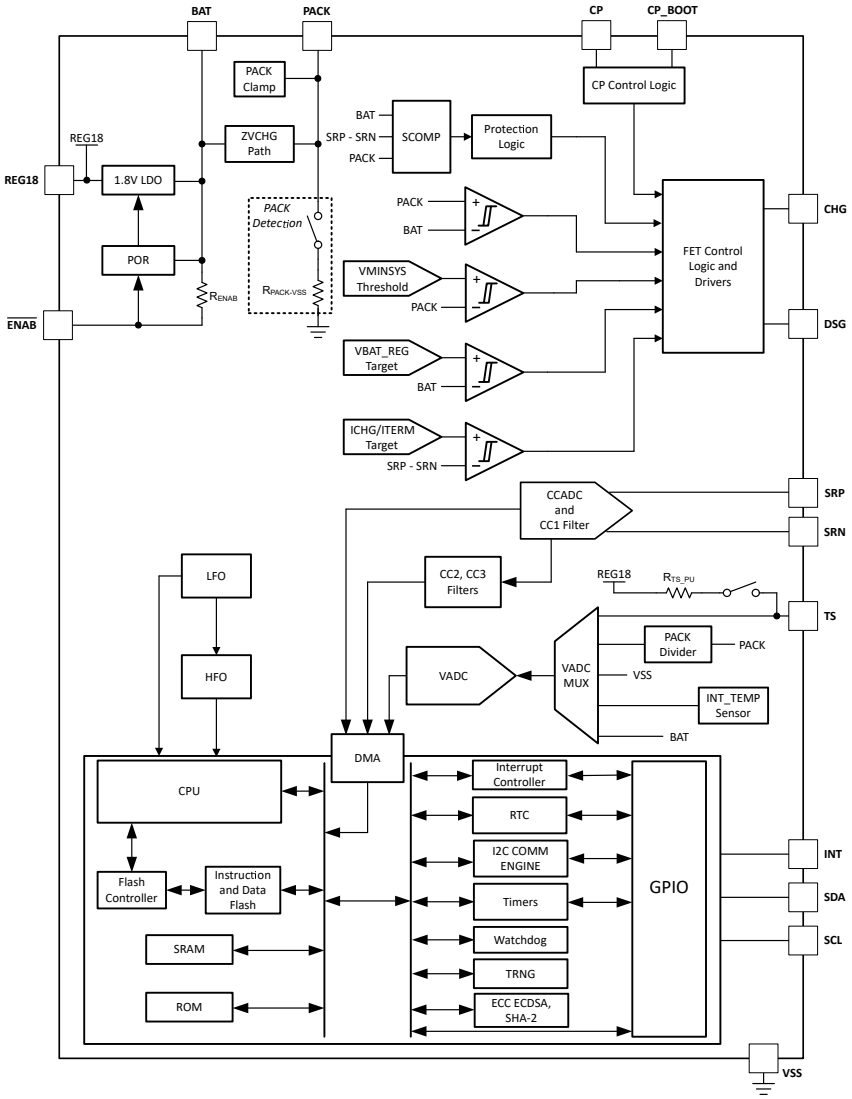
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6 Detailed Description

6.1 Overview

The BQ27Z855 Single Cell Battery Fuel Gauge is a fully integrated battery management solution that employs integrated flash-based firmware, hardware- and firmware-based protections, and ECC ECDSA and SHA-2 authentication to provide a complete solution for single-cell battery architectures. The BQ27Z855 device also incorporates an integrated JEITA-compliant linear battery charger and ideal diode detector that can perform tasks such as constant current-constant voltage (CC-CV) charge profile control and dynamic power path management with MINSYS and battery supplement modes. The BQ27Z855 interfaces with a host system via an I^2C interface and processes instructions and data using a state-of-the-art, ultra-low-power 32-bit RISC processor. High-performance, integrated analog peripherals allow support for a sense resistor down to 0.5mΩ and simultaneous current and voltage data conversion for instant power calculations. The following sections detail the overall block diagram and major component blocks included as part of the BQ27Z855 Single Cell Battery Fuel Gauge.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 BQ27Z855 Processor

The BQ27Z855 processor incorporates a 32-bit RISC Arm M0+ processor, a single-cycle 32-bit multiplier, 24-bit SysTick timer, and a nested vector interrupt controller (NVIC). All are all integrated in the processor.

6.3.2 Battery Parameter Measurements

The BQ27Z855 device measures cell voltage and current simultaneously using two independent ADCs and also measures temperature to calculate the information related to remaining capacity, full charge capacity, state-of-health, and other gauging parameters.

6.3.2.1 Analog-to-Digital Converter (VADC)

The first ADC is a 16-bit delta-sigma converter designed for general-purpose voltage measurements. The VADC automatically scales the input voltage range during sampling based on channel selection. The converter resolution is a function of its full-scale range and number of bits yielding a 38µV resolution.

6.3.2.2 VADC Multiplexer

The VADC multiplexer provides selectable connections to the device's external BAT, PACK, and TS pins as well as the internal temperature sensor (INT_TEMP). In addition, the multiplexer can independently enable the TS input connection to the internal biasing circuitry for an external thermistor and enables the user to short the multiplexer inputs for test and calibration purposes.

6.3.2.3 Coulomb Counter (CCADC) and Digital Filter (CC1)

The second ADC is an integrating analog-to-digital converter designed specifically for tracking charge and discharge activity, or Coulomb counting, of a rechargeable battery. It features a single-channel differential input that converts the voltage difference across a sense resistor between the SRP and SRN terminals with a resolution of 923nV. The differential input common mode voltage range is from V_{SS} to V_{BAT} and supports a 1-series cell high-side or low-side sensing option with a ±100mV input range.

The CC1 digital filter generates an 18-bit conversion value from the delta-sigma CCADC front-end. New conversions are available every 1s.

6.3.2.4 Internal Temperature Sensor (INT_TEMP)

An internal temperature sensor is available on the BQ27Z855 device to reduce the cost, power, and size of the external components necessary to measure temperature. It is measured by the VADC using the multiplexer and is ideal for quickly determining pack temperature under a variety of operating conditions.

The internal temperature sensor reports the measured temperature in terms of voltage and device firmware converts this voltage to temperature in units of °C to be reported for gauging and protection tasks. As an example, a difference in 0.05mV/°C between the $V_{INT_TEMP(TYP)}$ value as stated in the Internal Temperature Sensor (INT_TEMP) Specifications table and the actual voltage drift value reported by the internal temperature sensor approximately equates to a temperature error of ±1°C.

6.3.2.5 External Temperature Sensor Support

The TS input is enabled with an internal 18kΩ (TYP) linearization pull-up resistor to support the use of a 10kΩ (25°C) NTC external thermistor with B value of 3324 K, such as the Semitec 103AT-2. The NTC thermistor must be connected between VSS and the individual TS pin. The analog measurement is then taken by the VADC through its input multiplexer.

If a different thermistor type is required, then changes to configurations in the device firmware may be required.

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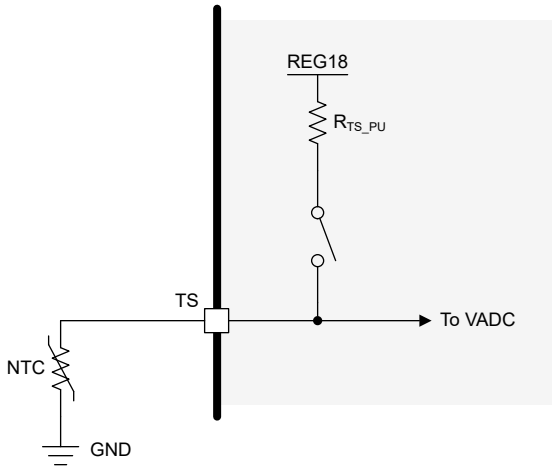


Figure 6-1. External Thermistor Biasing

6.3.3 Power Supply Control

The BQ27Z855 device uses the BAT pin as its power source. BAT powers the internal voltage sources and 1.8V LDO that supply references for the device.

6.3.4 $\overline{\text{ENAB}}$ Pin

The BQ27Z855 device can use the active low digital input $\overline{\text{ENAB}}$ pin to exit the device's SHELF and SHUTDOWN power modes. The digital input is connected to a weak internal pullup to BAT. A push-button can be connected to the $\overline{\text{ENAB}}$ pin to drive the pin to a low state for the device to exit SHELF or SHUTDOWN mode. If $\overline{\text{ENAB}}$ is used, it must be driven low with a 1kΩ series resistor.

If the $\overline{\text{ENAB}}$ pin is connected through a 1kΩ to the device's GND reference (VSS), the BQ27Z855 device is not able to enter SHELF or SHUTDOWN mode.

The $\overline{\text{ENAB}}$ pin can be left floating if using a push-button to exit SHELF or SHUTDOWN mode is not needed. The $\overline{\text{ENAB}}$ pin can also be left floating if the device needs the capability to enter SHELF or SHUTDOWN mode.

6.3.5 I^2C Bus Communication Interface

The BQ27Z855 device has an I^2C bus communication interface capable of supporting as low as 1.2V-level logic and up to a 1MHz I^2C clock frequency.

The device also implements timeouts for scenarios where SCL is held low or high between a START and STOP condition. The timeouts are used to conserve power as anytime the I2C engine is active the device remains in a high power state. If SCL is held low for longer than 26 ms, the I²C packet will be dropped and the device will disconnect from the bus. A new transaction must be started. If the SCL line is held high for more than 512 µs, this will also trigger the bus to disconnect and a new I²C transaction must be started.

When writing to the gauge, a timeout effectively results in a NACK of any data bytes, since the device will no longer drive the SDA line. When reading from the device, all bits will be read as 0xFF, since the device will no longer drive the SDA line. This makes it important for the host to be aware of the clock-low timeout case, and to guarantee that SCL is never left high during a transaction.

6.3.6 Low Frequency Oscillator (LFO)

The BQ27Z855 device includes a low frequency oscillator (LFO) running at 65.536kHz.

6.3.7 High Frequency Oscillator (HFO)

The BQ27Z855 includes a high frequency oscillator (HFO) running at 16.384MHz.

The HFO is frequency locked to the LFO output.

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6.3.8 Real Time Clock (RTC)

The BQ27Z855 includes a real time clock (RTC) that can provide the following information:

- Calendar
  - 4-digit year with automatic leap-year adjustment
  - Month
  - Day of the month
  - Day of the week
- Time of Day
  - Hours (24-hour format with optional daylight savings adjustment)
  - Minutes
  - Seconds

The RTC is sourced from the integrated LFO and can be enabled in all power modes except SHUTDOWN.

6.3.9 1.8V Low Dropout Regulator (REG18)

The BQ27Z855 device contains an integrated 1.8V LDO (REG18) that provides regulated supply voltage for the device CPU and internal digital logic.

This LDO requires a capacitor (C_{REG18}) with the recommended typical capacitance of 1.5µF connected between the device's REG18 and VSS pins. The capacitor must be placed as close as possible to the device.

6.3.10 FET Drivers (CHG, DSG)

The BQ27Z855 gas gauge includes two high-side NMOS FET drivers for charge (CHG) and discharge (DSG) control to disconnect the cell from the system and to control the flow of charge and discharge current. The device controls two external N-Channel MOSFETs in a back-to-back configuration for battery protection. The CHG and DSG FETs are automatically disabled if a protection fault is detected and can be re-enabled if the recovery conditions programmed in the device firmware are met.

6.3.10.1 Charge (CHG) FET Driver

The device's charge (CHG) FET driver allows for independent control of the CHG FET. The CHG FET is disabled automatically if a charge-related protection fault is detected, such as battery overvoltage (OVP) and overcurrent in charge (OCC). The CHG FET can be re-enabled if the recovery conditions programmed in the device firmware are met.

Additionally, the BQ27Z855 device's CHG FET can be enabled to be controlled in a linear operating mode to function as a current limiter and control the CC-CV charge profile of the battery. This also allows the CHG FET to be able to operate in an Ideal Diode mode where the CHG FET can be enabled to allow discharge current to flow through the CHG FET instead of the body diode and can be disabled if charge current is detected by the device's integrated ideal diode controller.

Refer to Section 6.3.15 and Section 6.3.16 for more information on the device's current limiter and ideal diode detector respectively.

6.3.10.2 Discharge (DSG) FET Driver

The device's discharge (DSG) FET driver allows for independent control of the DSG FET. The DSG FET is disabled automatically if a discharge-related protection fault is detected, such as battery undervoltage (UVP), overcurrent in discharge (OCD), and short circuit in discharge (SCD). The DSG FET can be re-enabled if the recovery conditions programmed in the device firmware are met.

6.3.11 Zero-volt Charging (ZVCHG)

ZVCHG (0-V charging) is a special function that allows charging a severely depleted battery. The BQ27Z855 device has ZVCHG enabled with no inhibit. This means a severely depleted battery with a voltage as low as 0V can be charged.

With a voltage applied at the PACK+ terminal of the battery pack, the BQ27Z855 device conducts ZVCHG current within the device via an internal path from the PACK pin to the BAT pin. The resistor between the

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PACK+ terminal of the battery pack and the PACK pin of the device current limits the ZVCHG current (I_{ZVCHG}) through the device effectively setting what ZVCHG current the battery charges at or is used to wake a secondary protector. I_{ZVCHG} is limited to $I_{ZVCHG(MAX)}$ as stated in the Zero-volt Charging Specifications table.

If V_{BAT} is below the entry threshold set by device firmware to qualify the battery as being in a ZVCHG state, the device disables the CHG FET and can start zero-volt charging once a voltage is applied at the PACK+ terminal of the battery pack. CHG FET will be in ideal diode state as long as DSG FET is enabled, otherwise both FETs are disabled. Once the battery is charged enough and V_{BAT} reaches the exit threshold programmed in device firmware, the device stops conducting zero-volt charging and assesses if the both FETs can be turned ON.

Both FETs are disabled while the device is in a ZVCHG state and V_{BAT} is below the POR threshold (V_{POR_TH} - V_{POR_HYS}).

The ZVCHG path through the device is always enabled when V_{BAT} is below the device POR threshold. Once the device is above the POR threshold, the ZVCHG path will be enabled when *Voltage()* is below the ***ZVCHG Exit Threshold.***

If the ZVCHG function is unused, a larger resistance value of R_{PACK} can be used.

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the ZVCHG battery charger function.

For safety purposes, the BQ27Z855 is specifically designed to be used in battery systems with at least 1 additional protector unit with an inhibitied zero-volt charging feature. This prevents unwanted battery self-discharge to severely low voltage levels or initiating charging at very low battery voltages that can cause irreversible damage to the battery.

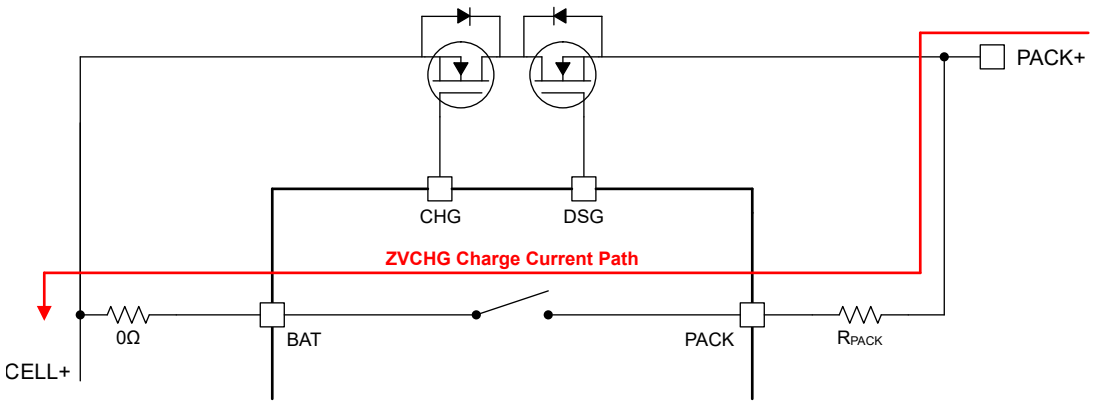


Figure 6-2. Zero-volt Charging Path

6.3.12 Integrated Protections

The BQ27Z855 gas gauge supports a wide range of hardware- and firmware-based protections for battery and system protection that can be easily configured using device firmware.

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6.3.12.1 Hardware-based Protections

The BQ27Z855 device includes a module for hardware fault detection using a shared comparator (SCOMP) utilized for multiple voltage and current condition detections and can turn the CHG or DSG FET OFF if an abnormal voltage or current condition is detected. These detections include:

- Overvoltage Protection
- Undervoltage Protection
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Short Circuit Current in Discharge Protection

6.3.12.1.1 Overvoltage Protection (OVP)

The overvoltage (OVP or HCOV) function detects abnormally high battery voltage. The OVP threshold and delay time are configurable through the device firmware. The detection circuit incorporates the delay setting before disabling the CHG FET. When an OVP event occurs, the ***Safety Status*** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.12.1.2 Undervoltage Protection (UVP)

The undervoltage (UVP or HCUV) function detects abnormally low battery voltage. The UVP threshold and delay time are configurable through the device firmware. The detection circuit incorporates the delay setting before disabling the DSG FET. When an UVP event occurs, the ***Safety Status*** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.12.1.3 Overcurrent in Charge Protection (OCC)

The overcurrent in charge (OCC or HOCC) function detects abnormally high current in the charge direction. The OCC threshold and delay time are configurable through the device firmware. The detection circuit incorporates the delay setting before disabling the CHG FET. When an OCC event occurs, the ***Safety Status*** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.12.1.4 Overcurrent in Discharge Protection (OCD)

The overcurrent in discharge (OCD or HOCD) function detects abnormally high current in the discharge direction. The OCD threshold and delay time are configurable through the device firmware. The detection circuit incorporates the delay setting before disabling the DSG FET. When an OCD event occurs, the ***Safety Status*** flag is set to 1 and is latched until it is cleared and the fault condition his removed.

6.3.12.1.5 Short Circuit Current in Discharge Protection (SCD)

The short circuit current in discharge (SCD or HSCD) function detects catastrophic current conditions in the discharge direction. The SCD thresholds and delay times are configurable through the device firmware. The detection circuit incorporates the delay setting before disabling the DSG FET. When an SCD event occurs, the ***Safety Status*** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

6.3.12.1.6 Wake-up Comparator (I-WAKE)

The BQ27Z855 device has the ability to wake from SLEEP mode if substantial charge or discharge current is detected flowing across the external sense resistor. The device has two independent current wake thresholds for detecting charge current (WAKE_CC) and discharge current (WAKE_CD) that are configurable through device firmware.

6.3.12.2 Firmware-based Protections

In addition to hardware-based protections, the BQ27Z855 device includes a large suite of firmware-based protections to detect multiple voltage and current conditions and turn the CHG or DSG FET OFF if an abnormal voltage or current condition is detected. These firmware-based protections are divided into primary and secondary level protections.

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6.3.12.2.1 Primary Level Protection Features

Primary level protections are protection features that can disable the CHG or DSG FET when an abnormal voltage or current condition is detected and the device can recover from to turn the appropriate FET back ON when the abnormal condition is removed.

The BQ27Z855 gas gauge supports the following primary level protection features for battery and system protection, which can be configured using device firmware:

- Cell Undervoltage Protection (CUV)
- Cell Overvoltage Protection (COV)
- Overcurrent in CHARGE (OCC)
- Overcurrent in DISCHARGE (OCD)
- Overtemperature in CHARGE (OTC)
- Overtemperature in DISCHARGE (OTD)
- Undertemperature in CHARGE (UTC)
- Undertemperature in DISCHARGE (UTD)
- Precharge Timeout (PTO)
- Fast Charge Timeout (CTO)

6.3.12.2.2 Secondary Level Protection Features

Secondary level protections are protection features that can be used to indicate more serious faults and permanently disable the use of the battery pack.

The BQ27Z855 gas gauge supports the following secondary level protection features for battery and system protection, which can be configured using device firmware:

- Safety Cell Undervoltage (SUV)
- Safety Cell Overvoltage (SOV)
- CHG FET Failure (CFETF)
- DSG FET Failure (DFETF)

6.3.13 Gas Gauging

The BQ27Z855 uses the Dynamic Z-Track™ algorithm to measure and calculate the available capacity in battery cells. The BQ27Z855 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature, state-of-charge, and relaxation time constants of the battery. The BQ27Z855 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature.

6.3.14 Advanced Battery Algorithms

In addition to gas gauging via the Dynamic Z-Track™ algorithm, the BQ27Z855 device includes a suite of advanced battery algorithms to support Li-ion cell chemistries and to provide an extra layer of battery monitoring and additional information to the system host device.

For more details on each individual algorithm, refer to their respective sections in the BQ27Z855 Technical Reference Manual.

6.3.15 Integrated Current Limiter and Charge Control Features

The BQ27Z855 device supports charge control features using the device's integrated current limiter or when using a smart charger with the BQ27Z855 device in a system.

The device can be configured via firmware to charge a battery or interact with a smart charger in a system. In both configurations, the charging current and charging voltage for the device's integrated current limiter or a smart charger to regulate at are programmable within data flash.

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6.3.15.1 Integrated Current Limiter

The BQ27Z855 has an integrated current limiter feature to control the CHG FET in a linear operating mode to function as a linear charger. This linear charger function allows the BQ27Z855 device to directly and autonomously control battery charging with a large suite of firmware programmable settings and controls.

These battery charging features and controls include:

- Regulates charging current and charging voltage based on programmable charge profile thresholds and settings in device data flash
- Supports charging a battery using a step-charging profile with up to 3 programmable constant current and constant voltage steps
- Adjusts charging voltage and charging current for a constant current – constant voltage (CC–CV) charging profile based on the active temperature range—JEITA temperature ranges T1, T2, T3, T4, T5, and T6
- Provides more complex charging profiles, including sub-ranges within a standard temperature range
- Provides precharging and zero-volt charging
- Supports dynamic power path management with MINSYS and battery supplement modes
- Disables charge when certain safety conditions such as hardware- or firmware-based protections are detected
- Employs charge inhibit and charge suspend if battery temperature is out of programmed range
- Activates charge and discharge alarms to report charging faults and to indicate charge status
- Reports the charging current and charging voltage to a system-side host using the I^2C bus communication interface
- Reduces charging current and charging voltage to account for cell aging

6.3.15.1.1 CHG FET Control

The BQ27Z855 CHG FET output is controlled by CHG FET state machine logic, which can be manipulated by device firmware and several system parameters.

There are 4 distinct modes device firmware transitions between depending on programmable settings in device data flash and system parameters: OFF, ON, Linear, and Ideal Diode. Depending on the current mode the device is operating in, the device can operate in a particular state and make hardware-based transitions between states within modes.

Device firmware determines the mode the device operates in while device digital hardware determines the state within a mode the device operates in.

The ideal diode mode hardware control is entered when the charger is enabled, but there is no charger present. The CHG FET will allow power to transfer from the battery, but it will not allow power to transfer into the battery. Once the charger detection occurs, the BQ27z855 will transition to Linear mode.

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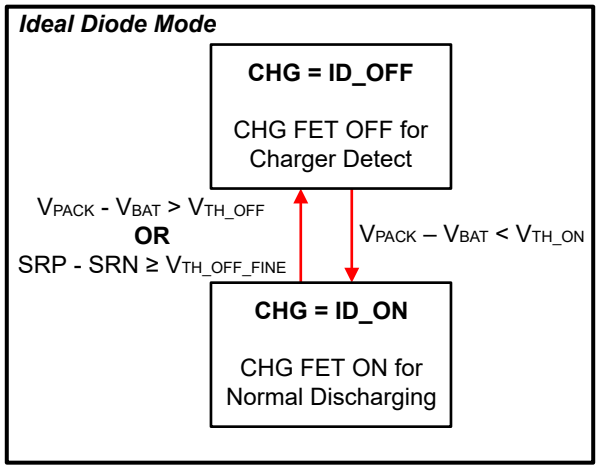


Figure 6-3. CHG FET Ideal Diode Mode Control

The linear mode hardware control is entered when the CHG FET is actively regulating current. The V_{PACK}-V_{BAT} differential is constantly being evaluated by the dedicated voltage comparator (DCOMP) to determine if the CHG FET should be fully ON in supplement mode, or if the CHG FET should remain regulating in the charging or MINSYS modes.

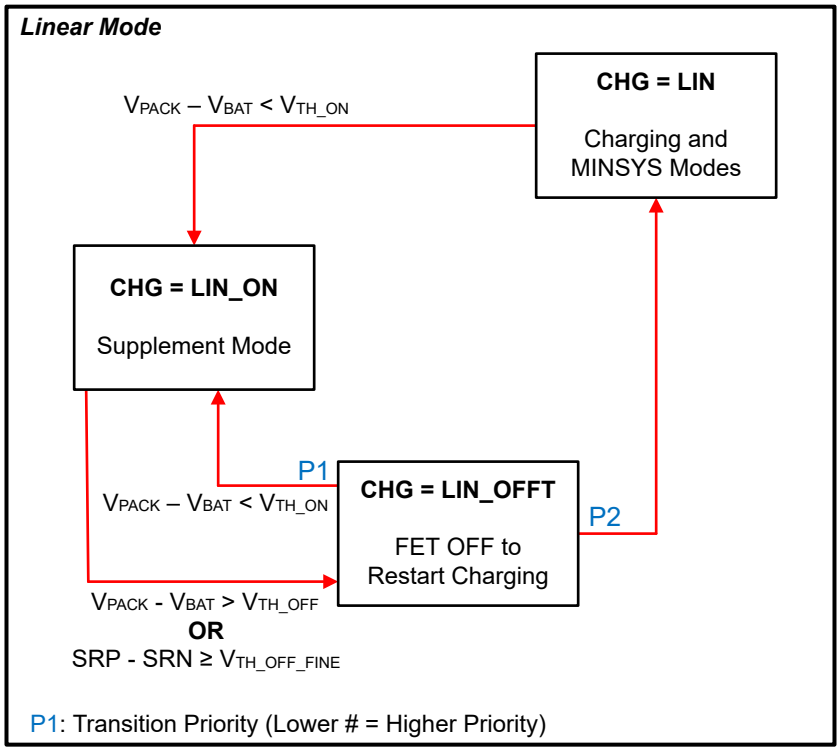


Figure 6-4. CHG FET Linear Mode Control

The CHG FET state machine logic controls the CHG FET with the following key considerations:

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1. Firmware transitions override hardware transitions and takes highest priority after hardware-based protection circuits
2. Available hardware transitions in Linear and Ideal Diode modes check several system parameters to ensure proper device and system operation:
   a. The DCOMP comparator between the PACK and BAT pin voltages detects when V_{PACK} - V_{BAT} < V_{TH_ON} to turn the CHG FET ON and V_{PACK} - V_{BAT} > V_{TH_OFF} to turn the CHG FET OFF
   b. A Coulomb counter-based charge current measurement digital filter (CC3) detects when V_{SRP} - V_{SRN} ≥ $V_{TH_OFF_FINE}$ to turn the CHG FET OFF
3. State exit transition priorities are indicated as P1, P2, and so on where P1 is the highest priority transition
4. The HFO is automatically enabled when the device is in all states except OFF, ON, and ID_ON to reduce device power consumption.

Table 6-1. CHG FET FSM Modes and States

Modes	States	Charger Function
OFF	OFF	Charging Disabled
ON	ON	Normal Charging or Discharging
Linear	LIN	PCHG, CC, CV, MINSYS
	LIN_ON	Supplement
	LIN_OFFT	
Ideal Diode	ID_OFF	Charger Detect, VCT
	ID_ON	Normal Discharging, Charger Removed, ZVCHG

6.3.15.1.2 Linear Mode

During Linear mode, the BQ27Z855 device controls the external CHG FET in a linear operating mode to regulate charging current, charging voltage, and the CHG FET state.

There are several control loops that influence the charge current and charge voltage:
- Constant Current loop (CC)
- Constant Voltage loop (CV)
- MINSYS loop
- Battery supplement loop

During battery charging, all control loops are enabled and the dominant loop takes control over the other loops.

The device supports several different battery chemistries and system requirements for single-cell applications through programmable battery charge profile parameters such as charge voltage regulation (V_{BAT_REG}), charge current regulation (I_{CHG}), and PACK voltage threshold to reduce charge current (V_{MINSYS}) in device firmware. Refer to the BQ27Z855 Technical Reference Manual for a list of all programmable battery charge profile parameters in device data flash.

6.3.15.1.2.1 Battery Charging Process

When the device detects a valid input voltage source is connected to the PACK+ terminal of the battery pack and the device's integrated current limiter function is enabled, the state of the *[CHGR_DET]* bit determines if battery charging is initiated. If the *[CHGR_DET]* bit goes high and battery charging can be initiated, the device transitions to Linear mode. During battery charging, the CHG FET is in the CHG = LIN state within Linear mode.

Battery charging is disabled via turning the CHG FET OFF. The CHG FET can turn OFF and transition to the CHG = ID_OFF state if the *[XCHG]* bit is set, such as when a hardware- or firmware-based charge mode protection like OVP or OCC trips, or the *[LINCHGR]* bit is cleared. If the device's current limiter is disabled, the CHG FET will instead transition to the CHG = OFF state.

Figure 6-5 shows a typical CC-CV battery charge profile.

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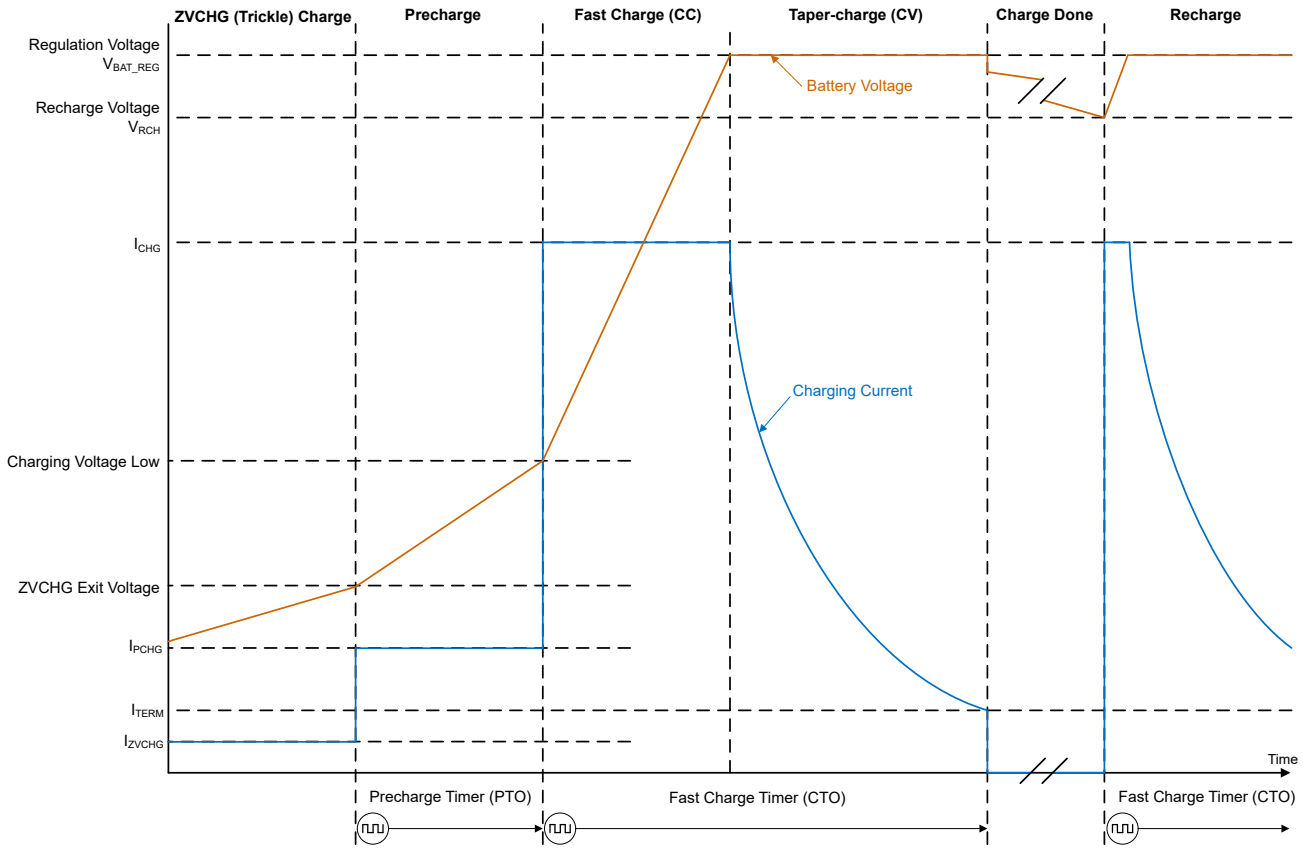


Figure 6-5. Typical CC-CV Battery Charge Profile

Figure 6-6 shows a CC-CV battery charge cycle the BQ27Z855 device steps through and tracks via a state machine regardless of the state of the *[CHGR_DET]* bit. The device controls what charge profile state the battery is currently operating at in parallel to controlling what state the CHG FET is in via the CHG FET FSM.

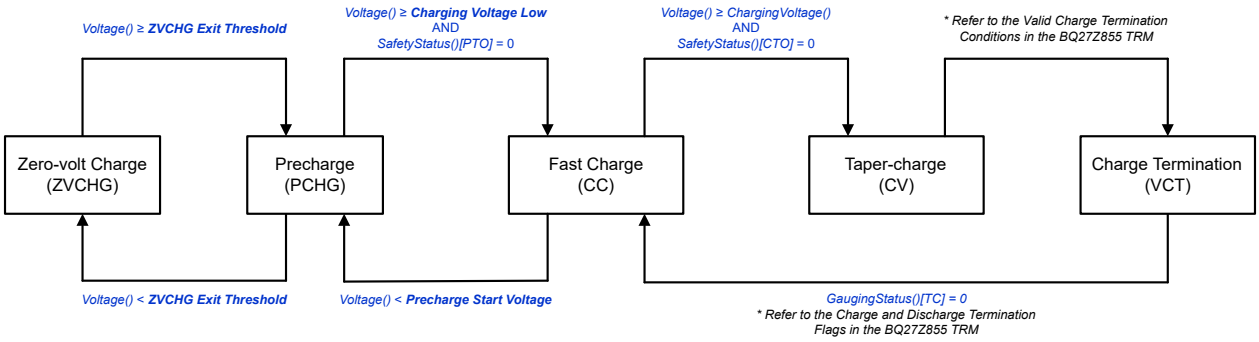


Figure 6-6. Linear Charge Profile State Machine

The BQ27z855 can also be configured in a parallel pack mode. In this mode the charger detection function in hardware is no longer used, and the host controls when there is an upstream converter present. This prevents scenarios where one battery charges the other, since the PACK pin for both devices is connected to the same node in the system. Care must be taken by the host in this mode to properly set each one of the parallel packs charger detection to prevent cross charging.

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When the device is configured for parallel pack operation, it is the responsibility of the host to manage conditions when the upstream converter cannot supply enough power for the load and charging the battery, causing the BQ27z855 to enter supplement mode. The BQ27z855 must enable the DSG FET to charge the cell and recover from protections which disable the DSG FET and set the *[XDSG]* flag. If the upstream converter cannot supply sufficient power it's possible the cells can continue discharging until another protection triggers. The host can disable the charger detection when a protection event causes *[XDSG]* to set. Charger detection should only be re-enabled when the system load has reduced, or the upstream current compliance has increased which can sustain both charging and system load.

6.3.15.1.2.2 Zero-volt Charge (ZVCHG)

The BQ27Z855 device supports charging severely depleted batteries using a zero-volt charge (ZVCHG) or trickle charge feature. To prevent damage to the battery, the device will charge the battery at a very low current level (I_{ZVCHG}) when the battery is below the programmable ***ZVCHG Exit Threshold*** data flash parameter and a valid input voltage source at PACK+ is present.

Both FETs are disabled while the device is in a ZVCHG state and V_{BAT} is below the POR threshold (V_{POR_TH} - V_{POR_HYS}).

For a more detailed description on the BQ27Z855 device's ZVCHG feature, refer to Section 6.3.11.

6.3.15.1.2.3 Precharge (PCHG)

When the battery voltage rises to or above the programmed ***ZVCHG Exit Threshold*** value, the device transitions to Linear mode with the CHG FET now in the CHG = LIN state to operate in Precharge mode. In Precharge mode, the device charges the battery via the Constant Current (CC) loop at the charge current regulation level I_{CHG}. The device regulates I_{CHG} according to the programmed ***Pre-Charging:Current*** value in device data flash. Once the battery reaches the programmed ***Charging Voltage Low*** value, the device will then operate in Fast Charge mode and charge the battery according to the programmed I_{CHG} value.

If enabled, the Precharge Timeout Protection (PTO) safety timer counts the time the device spends in Precharge mode and can disable charging if the accumulated time exceeds the ***PTO:Delay*** threshold.

6.3.15.1.2.4 Fast Charge (CC)

The BQ27Z855 device has two main loops to control battery charging when the battery voltage reaches the programmed ***Charging Voltage Low*** value: the Constant Current (CC) and Constant Voltage (CV) loops.

When the device is in Fast Charge (CC) mode, the CC loop is dominant and the battery is charged at the charge current regulation level I_{CHG} based on the temeprature range and battery voltage range the device is presently operating in. The different I_{CHG} settings the CC loop can regulate charging current at is configurable within device data flash (Refer to the Charging Current section of the BQ27Z855 Technical Reference Manual). The CC loop regulates charging current at the appropriate I_{CHG} setting unless charging is disabled due to a hardware- or firmware-based protection tripping (including JEITA temeprature-related protections) or the MINSYS loop is active.

If enabled, the Fast Charge Timeout Protection (CTO) safety timer counts the time the device spends in Fast Charge and Taper-charge modes and can disable charging if the accumulated time exceeds the ***CTO:Delay*** threshold.

6.3.15.1.2.5 Taper-charge (CV)

Once the battery voltage reaches the charge voltage regulation target (V_{BAT_REG}), the device operates in Taper-charge mode. The CV loop becomes dominant and the charging current begins to naturally taper off. The different V_{BAT_REG} settings the CV loop can regulate charging voltage at based on the present temperature range is configurable within device data flash (Refer to the Charging Voltage section of the BQ27Z855 Technical Reference Manual). Once the charging current reaches the termiantion current target (I_{TERM}) programmed by the ***Charge Term Taper Current*** data flash parameter and all Valid Charge Termination conditions stated in the BQ27Z855 Technical Reference Manual are met, battery charging is done and the device sets the *[VCT]* bit.

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6.3.15.1.2.6 Charge Termination (VCT)

The device will automatically terminate charging once the charge current reaches the programmable I_{TERM} value and all Valid Charge Termination conditions stated in the BQ27Z855 Technical Reference Manual are met. After termination, the device operates in Charge Termination mode and disables the CHG FET to disconnect the battery to the system load. The device disables the CHG FET by transitioning the CHG FET to Ideal Diode mode to set CHG = ID_OFF. Power is still provided to the system load as long as the input voltage source is connected.

Termination is only enabled when the CV loop is active and dominant during taper-charge operation. Termination is disabled if the charge current reaches I_{TERM} while the MINSYS loop or battery supplement is active. The device's current limiter will only terminate charging when the current drops to I_{TERM} due to the battery reaching the target CV voltage and not due to charge current limitations imposed by the previously mentioned control loops.

After termination, the CHG FET is disabled and the battery voltage is monitored to check if it has dropped to the programmable Recharge Voltage (V_{RCH}) threshold. If it does, a new charge cycle is established. The safety timers are reset. During charging or even when termination is reached, the device will still support the higher system loads using battery supplement mode.

6.3.15.1.2.7 Step-charging Profile Support

In addition to a CC-CV battery charging profile, the BQ27Z855 supports a step-charging battery charge profile with up to 3 configurable CC-CV steps using device firmware. The device uses the same control loops as during a CC-CV battery charging profile.

Figure 6-7 shows an example step-charging battery charge profile with 3 CC-CV steps.

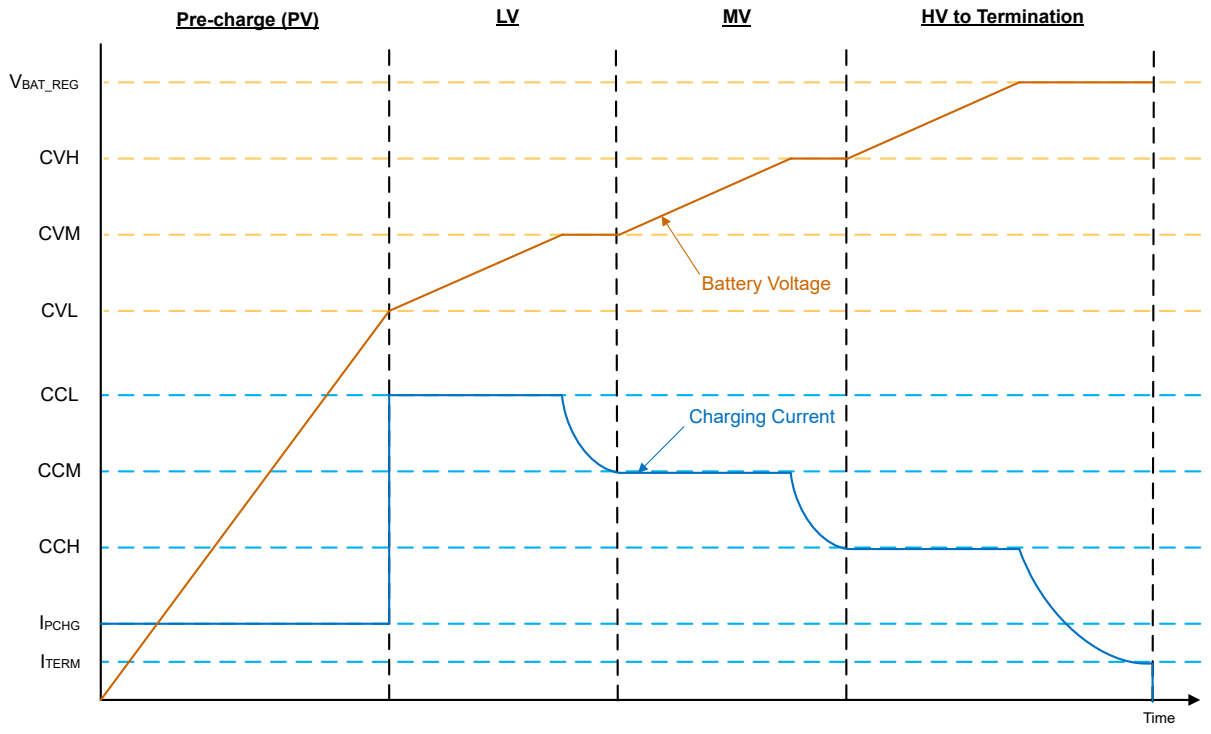


Figure 6-7. Example Step-charging Battery Charge Profile with 3 CC-CV Steps

Figure 6-8 shows an N-step step-charging battery charge cycle the BQ27Z855 device steps through and tracks via a state machine regardless of the state of the *[CHGR_DET]* bit. The device controls what charge profile state

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and CC-CV or CC step the battery is currently operating at in parallel to controlling what state the CHG FET is in via the CHG FET FSM.

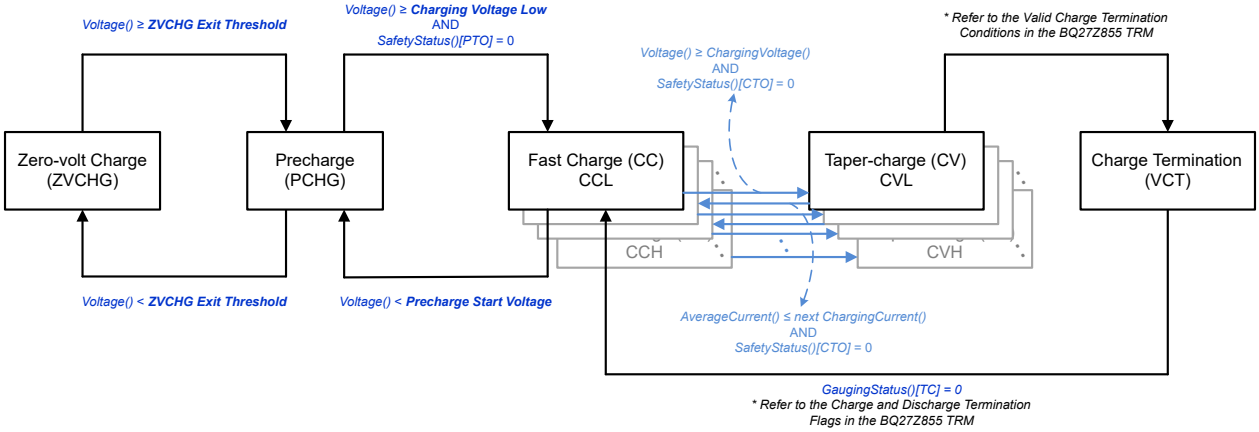


Figure 6-8. Step-charging Charge Profile State Machine

6.3.15.1.3 MINSYS Mode

When the device is in Linear Mode in the CHG = LIN state, the MINSYS regulation loop can be active. With a valid input power source connected at the PACK+ node of the system, the current into the PACK+ node is shared between charging the battery and powering the system load. If the sum of the battery charging current and load current exceeds the output current limit of the input power source, the MINSYS loop activates to reduce battery charging current and prioritize the system load.

During MINSYS mode, the device will increase or decrease the CHG FET gate drive voltage to reduce charging current and maintain the PACK voltage at or above V_{MINSYS}. The V_{MINSYS} threshold setting is programmable using device firmware.

PACK voltage is maintained above battery voltage when the MINSYS loop is active. If PACK voltage falls below the supplement mode threshold (V_{TH_ON}), the device will enter supplement mode (CHG = LIN_ON).

Battery termination is disabled when the MINSYS loop is active.

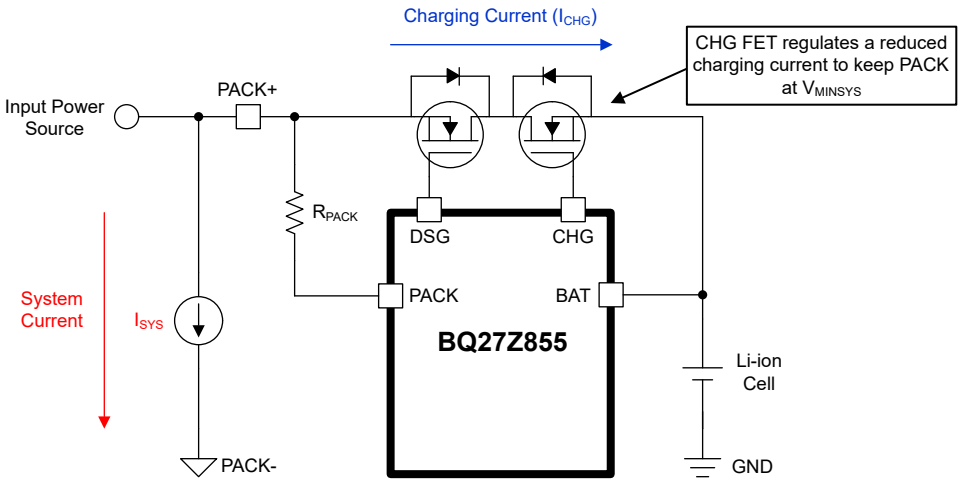


Figure 6-9. MINSYS Mode Operation

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6.3.15.1.4 Battery Supplement Mode

While in MINSYS mode (CHG = LIN), if the charging current falls to zero and the system load current increases beyond the output current limit of the input power source connected at PACK+, the voltage at PACK reduces further. When the PACK voltage drops below the battery voltage to V_{TH_ON}, the battery supplements the system load and the device enters the CHG = LIN_ON state. The battery stops supplementing the system load when either the voltage on the PACK pin rises within the battery voltage to V_{TH_OFF} or sufficient positive or charging current flows through the sense resistor to produce a differential voltage that reaches or exceeds $V_{TH_OFF_FINE}$. The device then transitions to the CHG = LIN_OFFT state.

If the voltage at PACK falls below the battery voltage to V_{TH_ON} while in the CHG = LIN_OFFT state, the device enters the CHG = LIN_ON state. If the voltage at PACK stays above the V_{TH_OFF} threshold while in the CHG = LIN_OFFT state, the device will return to the CHG = LIN state to resume linear charging. Entry into CHG = LIN_ON from CHG = LIN_OFFT is always prioritized over entry to CHG = LIN to support the current load needed by the system.

The device uses the following hardware-based modules to transition in and out of supplement mode based on several system parameters:

- A dedicated voltage comparator (DCOMP) between the device's BAT and PACK pins to assess if the differential voltage between the BAT and PACK reaches the V_{TH_ON} and V_{TH_OFF} thresholds
- A Coulomb counter-based charge current measurement digital filter (CC3) to assess if the current flowing across the sense resistor produces a differential voltage that reaches or exceeds the $V_{TH_OFF_FINE}$ threshold

To support supplement mode and consecutive high system load pulses, the device turns the CHG FET ON using an external capacitor (C_{CP}) connected between the device's CP and CP_BOOT pins. This capacitor is discharged to the device's CHG pin when the device enters the CHG = LIN_ON state and is recharged immediately after the CHG FET turns ON. Additionally if the device's current limiter is enabled, the external CP capacitor is charged during device operation regardless of whether the device is actively charging a battery.

During supplement mode, the battery supplement current is not regulated. However, the device's hardware-based and firmware-based OCD and SCD protections are active if enabled.

Battery termination is disabled while the device is in supplement mode.

Battery voltage must be higher than the hardware-based undervoltage protection (V_{UVP}) in order for the device to support supplement mode.

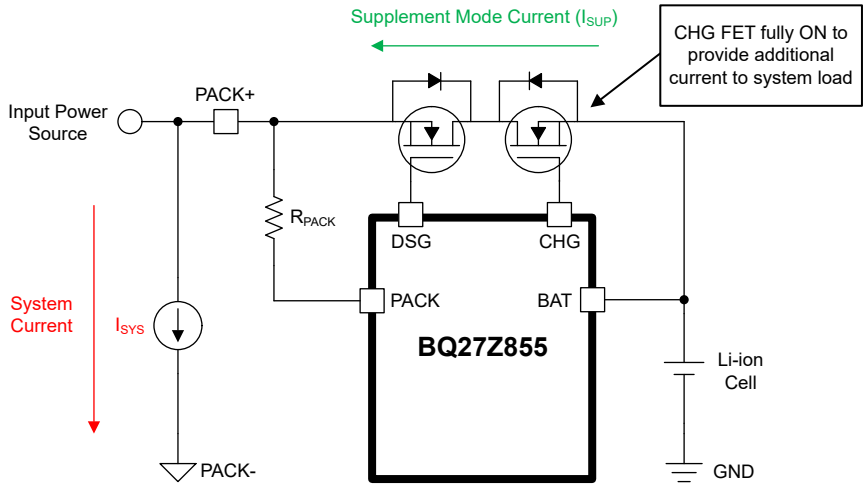


Figure 6-10. Supplement Mode Operation

6.3.15.2 Interaction with a Smart Charger

When the BQ27Z855 device's integrated current limiter is not enabled, the device can interact with a smart charger in a system to support charge control features.

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These charge control features include:

- Reports charging voltage and charging current based on the active temperature range—JEITA temperature ranges T1, T2, T3, T4, T5, and T6
- Provides more complex charging profiles, including sub-ranges within a standard temperature range
- Reports the appropriate charging current and charging voltage needed for constant current – constant voltage (CC–CV) charging profile to the smart charger using the I^2C bus communication interface
- Provides pre-charging and zero-volt charging
- Employs charge inhibit and charge suspend if battery pack temperature is out of programmed range
- Activates charge and discharge alarms to report charging faults and to indicate charge status
- Request reduced charging current and charging voltage from the smart charger to account for cell aging

Refer to the Advanced Charge Algorithm chapter of the BQ27Z855 Technical Reference Manual for more information on the device's suite of charge control features.

6.3.16 Ideal Diode Mode

The BQ27Z855 device can control the CHG FET to function as an ideal diode to block charging current when the device detects a valid input voltage source is present.

When the device is in Ideal Diode mode during battery discharging, the device enters the CHG = ID_ON state and the CHG FET is enabled to allow discharge current to flow through the FET instead of the CHG FET's body diode. However when the device is in the CHG = ID_ON state and PACK voltage exceeds the battery voltage or charging current is detected, then the CHG FET transitions to the CHG = ID_OFF state to turn the FET OFF.

The device uses the following hardware-based modules to control the FET state within Ideal Diode mode based on several system parameters:

- A dedicated voltage comparator (DCOMP) between the device's BAT and PACK pins to assess if the differential voltage between the BAT and PACK reaches the V_{TH_ON} and V_{TH_OFF} thresholds
- A Coulomb counter-based charge current measurement digital filter (CC3) to assess if the current flowing across the sense resistor produces a differential voltage that reaches or exceeds the $V_{TH_OFF_FINE}$ threshold

Additionally, the device is in Ideal Diode mode after battery charging termination. After termination, the device operates in Charge Termination mode and disables the CHG FET to disconnect the battery from the system load. The device disables the CHG FET by transitioning the CHG FET to Ideal Diode mode to set CHG = ID_OFF. Power is still provided to the system load as long as the input voltage source is connected. The device will still support any high system loads that may occur with the input voltage source still connected using battery supplement mode via transitioning the CHG FET to the CHG = ID_ON state.

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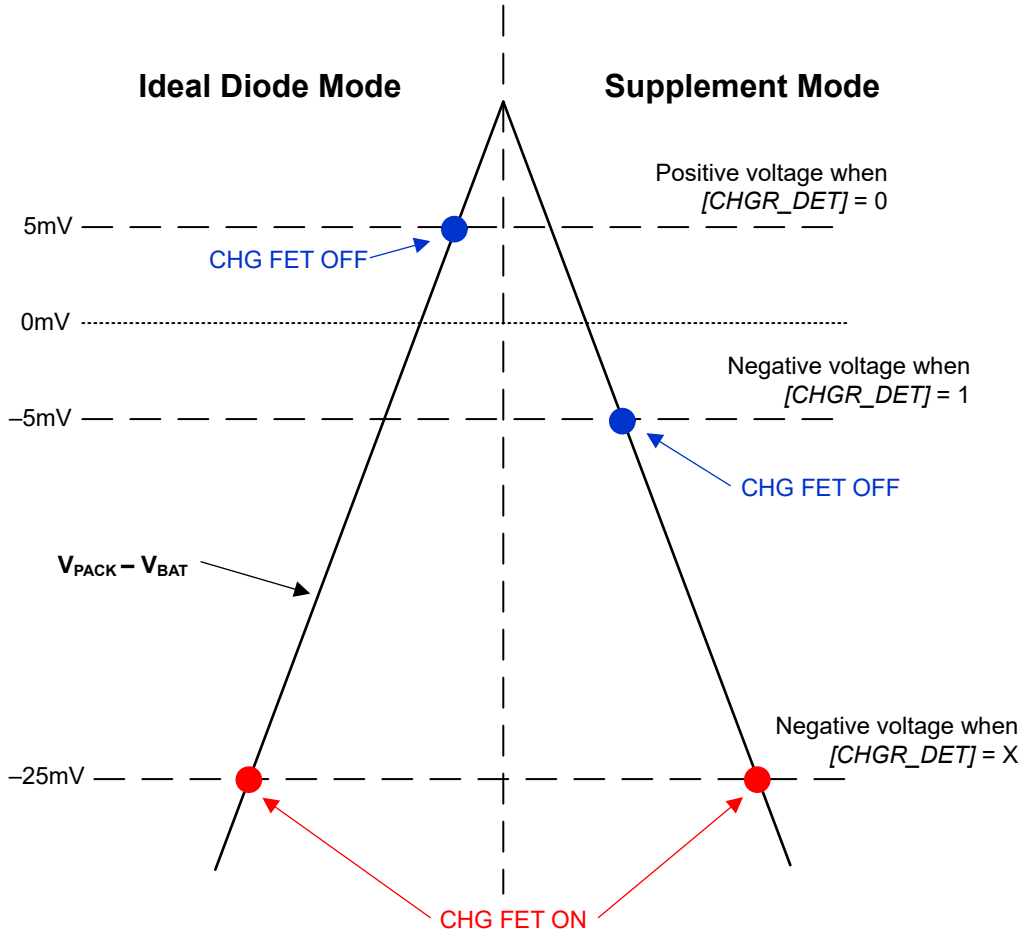


Figure 6-11. DCOMP-based Detection Thresholds in Ideal Diode and Supplement Modes

6.3.17 Lifetime Data Logging Features

The device supports data logging of several key parameters for warranty and analysis:

- Maximum and Minimum Cell Voltages
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum and Minimum Internal Temperature Sensor Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Total FW Runtime and Time Spent in Each Temperature Range (This data is updated every 2 hours if a difference is detected.)

Refer to the Lifetime Data Collection chapter of the BQ27Z855 Technical Reference Manual for more information on the device's lifetime data logging features.

6.3.18 Authentication

The BQ27Z855 device supports authentication by the host using Elliptic Curve Cryptography (ECC) or SHA-256.

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6.3.18.1 ECC ECDSA Authentication

The BQ27Z855 device supports authentication by the host using ECC, which uses a 256-bit key system for the authentication process. The BQ27Z855 device employs the ECDSA variant of ECC authentication. Additionally, the ECC private key is required to be stored only in the battery pack, which makes ECC-based key management more simple and secure. The signing time would be less than 200ms and the overall hardware and firmware architecture to support this response time enables an additional level of protection.

For additional information on ECC authentication on the TI gas gauges, refer to the following Application Note: Implementation of Elliptic Curve Cryptography Authentication on TI Battery Fuel Gauges.

6.3.18.2 SHA-256 Authentication

The device supports authentication by the host using SHA-256.

The gas gauge can be configured to require SHA-256 authentication before the device can be unsealed or allow full access.

6.3.19 Over the Air (OTA) Field Updater

The BQ27Z855 device incorporates support for the optional field updater to allow the device to apply firmware changes in the field. The updates can upgrade device firmware version and apply modified configuration parameters while maintaining device specific data.

The Section 6.3.12.1 provide safety protection during OTA updates.

For more details on OTA updates on the BQ27Z855 device, refer to the BQ27Z855 Technical Reference Manual.

6.3.20 Configuration

The device supports accurate data measurements and data logging of several key parameters.

6.3.20.1 Cell Voltage Measurements

The BQ27Z855 gas gauge measures the cell voltage at 1s intervals using the VADC. This measured value is internally scaled for the VADC and is calibrated to reduce any errors due to offsets. This data is also used for calculating the impedance of the cell for Dynamic Z-Track™ gas gauging.

6.3.20.2 Coulomb Counting

The device uses an integrating delta-sigma analog-to-digital converter (CCADC) for current measurement. The CCADC measures charge and discharge flow of the battery by measuring the voltage drop across a very small external sense resistor. The CCADC measures a bipolar signal from a range of –100mV to 100mV where a positive value of $V_{SRP} – V_{SRN}$ indicates charge current and a negative value indicates discharge current.

The external sense resistor can be as low as 0.5mΩ and the polarity of the differential voltage determines if the cell is in the CHARGE or DISCHARGE mode.

6.3.20.3 Temperature Measurements

The BQ27Z855 device has an internal temperature sensor (INT_TEMP) for on-die temperature measurements and the ability to support an external temperature measurement using an external NTC connected to the TS pin. These two measurements can be individually enabled and configured via device firmware.

6.4 Device Functional Modes

The BQ27Z855 device supports multiple power modes to accommodate different modes the battery pack can be in and reduce device power consumption:

- In ACTIVE mode, the BQ27Z855 performs measurements, calculations, protection decisions, and data updates in 1s intervals. Between these intervals, the BQ27Z855 is in a reduced power stage to minimize device power consumption. Battery protections are continuously monitored in this mode.
- In SLEEP mode, the BQ27Z855 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the BQ27Z855 is in a reduced power stage. While in SLEEP mode, the device's Coulomb counter is continuously integrating. Battery protections are

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continuously monitored in this mode. The BQ27Z855 has a wake function that enables exit from SLEEP mode when current flow, a battery protection event, or a failure is detected.

- In SHIP mode, the BQ27Z855 is in a further reduced power state while still having the protection FETs turned on and protections running. While in SHIP mode, the device deos not coulomb count, and assumes and reports that current as 0mA. The device will take cell voltage, pack voltage, thermistor input, and internal die temeprature every programmed time interval.
- In SHELF mode, the BQ27Z855 is placed in a very low power state for shipping or shelf life purposes. The device measures voltage and temperature very infrequently and at shorter ADC conversion times, and current is not measured or Coulomb counted. Additionally, the CHG and DSG FETs and all hardware-based protections are OFF. Due to this, no external power is available to the system when the gauge is in SHELF mode. Current is assumed to be and reported as 0mA.
- In SHUTDOWN mode, the BQ27Z855 firmware is not running. There are no periodic checks for voltage, current, and temperature. The CHG and DSG FETs are disabled. Either the $\overline{\text{ENAB}}$ pin or PACK detection must be used to wake the device.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The BQ27Z855 can be used with a 1-series Li-ion or Li-polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the user needs Battery Management Studio (BQStudio), which is a graphical user-interface tool installed on a PC during development, and a USB-based PC interface board such as the EV2500 or EV2400 to program and communicate with the gauge. The firmware installed in the product has default values, which are summarized in the associated BQ27Z855 Technical Reference Manual. Using the BQStudio tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as enable or disable certain features for operation, cell configuration, chemistry that best matches the cell used, and more. The final flash image, which is extracted once configuration and testing are complete, is used for mass production and is referred to as the "golden image."

Note

Preloaded device firmware can contain potential untested features. Please update to the latest firmware found on the device firmware page, which also contains information on the features and release quality level. See the technical reference manual for details about the firmware.

7.2 Typical Application Schematics

The following are example BQ27Z855 application schematics for a single-cell battery pack.

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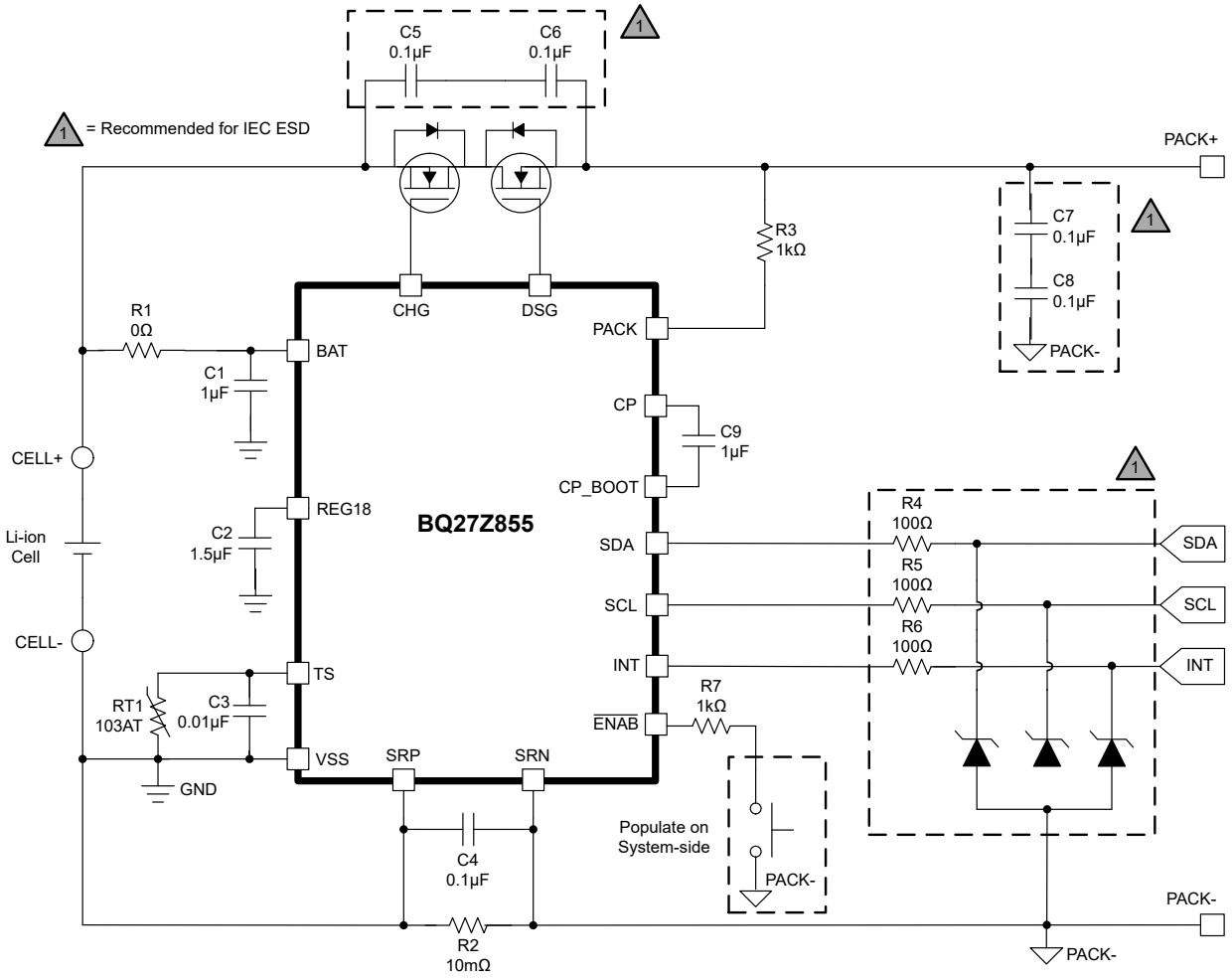


Figure 7-1. BQ27Z855 Typical Application Schematic with Low Side Current Sensing

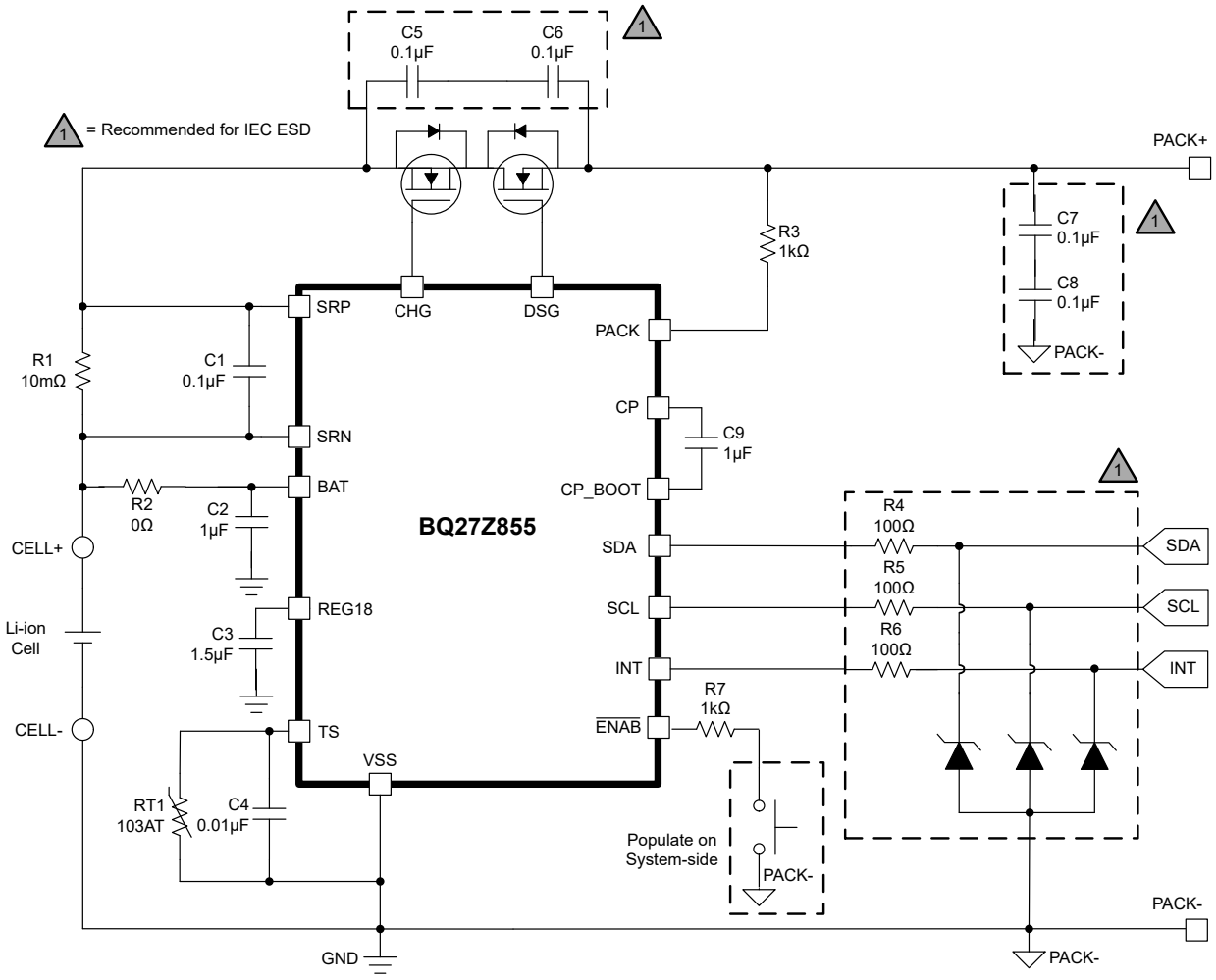


Figure 7-2. BQ27Z855 Typical Application Schematic with High Side Current Sensing

7.2.1 Design Requirements

Table 7-1 shows the default settings for the main parameters. Use the bqStudio tool to update the settings to meet the specific application or battery pack configuration requirements.

The device must be calibrated before any gauging test. Follow the bqStudio **Calibration** page to calibrate the device, and use the bqStudio **Chemistry** page to update the chemistry profile on the device.

Table 7-1. Example Design Parameters

Design Parameter	Example
Cell Configuration	1S1P: 1 series with 1 parallel
Design Capacity	250mAh
Device Chemistry	Li-Ion
Cell Undervoltage	2500mV
Cell Overvoltage at Standard Temperature	4400mV
Shutdown Voltage	2300mV
Overcurrent in CHARGE Threshold	1000mA
Overcurrent in DISCHARGE Threshold	-1000mA

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Table 7-1. Example Design Parameters (continued)

Design Parameter	Example
Short Circuit in DISCHARGE Threshold	-1500mA
Internal and External Temperature Sensor	Only External Temperature Sensor used
Undertemperature in CHARGE Threshold	0°C
Undertemperature in DISCHARGE Threshold	0°C
Zero-volt Charge Exit Threshold	2400mV
Zero-volt PACK Threshold	1500mV
Precharge Current	50mA
Charging Voltage Low	2900mV
Falling Precharge Entry Voltage	2500mV
Charging Current at Standard Temeprature	250mA
Charging Voltage at Standard Temeprature	4200mV
Termination Current	25mA
Recharge Voltage	100mV
MINSYS Voltage Threshold	3800mV
BROADCAST Mode	Disabled

The design parameters needed to fit the design requirements can be adjusted in the device firmware. For more information on particular design parameters, refer to the BQ27Z855 Technical Reference Manual.

7.2.2 Detailed Design Procedure

7.2.2.1 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels from the PACK+ terminal, it finds its way through protection FETs, the battery cell and cell connections, the sense resistor, and then returns to the PACK– terminal. In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

7.2.2.1.1 Protection FETs

The BQ27Z855 device supports driving external N-channel protection FETs using integrated NFET drivers. Select the N-channel CHG and DSG FETs for a given application.

If the device's current limiter is enabled, select the N-channel CHG and DSG FETs based on the FET parameter guidelines outlined in Section 7.2.2.3.1 to ensure proper linear charging functionality.

The gates of the CHG and DSG protection FETs are pulled to the device GND reference (VSS) to ensure the FETs are turned off if the gate drive is open.

Table 7-2. Dual N-Channel MOSFET Examples

Part Number	Continuous Drain Current (I_D)	Drain-Source Voltage (V_{DS})	Gate-Source Voltage (V_{GS})
DMN2008LFU-7	14.5 A	20 V	+/- 12 V
KFCAB12004NL	10.3 A	12 V	+/- 8 V

Capacitors C5 and C6 help protect the FETs during an ESD event. Using two devices ensures normal operation if one capacitor becomes shorted. For more robust ESD performance, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C5 and C6 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

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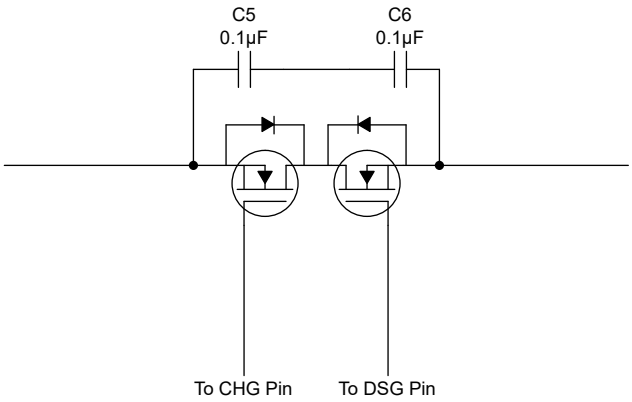


Figure 7-3. Protection FETs

7.2.2.1.2 Battery Cell Connections

The high current flows through the top and bottom connections of the battery cell. Therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a voltage drop caused by the copper trace. The location marked 1P in Figure 7-4 indicates the Kelvin connection at the positive terminal of the cell. This Kelvin connection to the device's BAT pin also reduces the trace resistance between the connection point and the input power supply of the device.

The Kelvin connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the cell voltage.

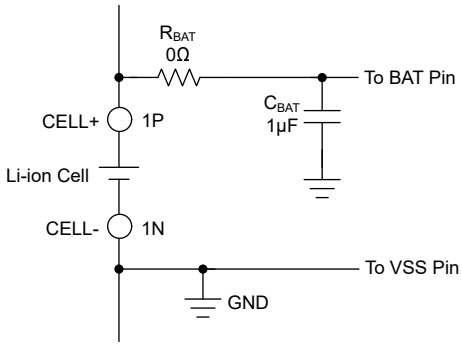


Figure 7-4. Battery Cell Connections

7.2.2.1.3 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short circuit protection ranges and desired protection threshold setting of the BQ27Z855. It is recommended to select the smallest value possible for a given application to minimize the negative voltage generated on the BQ27Z855 V_{SS} node during a short circuit in discharge event. This pin has an absolute minimum voltage of –0.3V.

Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a minimum sense resistor value of 0.5mΩ.

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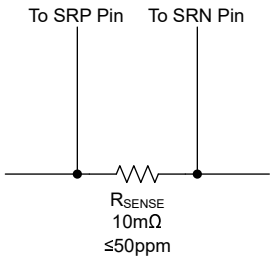


Figure 7-5. Sense Resistor

7.2.2.1.4 ESD Mitigation

A pair of series 0.1µF ceramic capacitors (C7 and C8) is placed across the PACK+ and PACK– terminals to help in the mitigation of external system-level electrostatic discharges. The two devices in series ensure continued operation of the battery pack if one of the capacitors becomes shorted.

7.2.2.2 Gas Gauge Circuit

The gas gauge circuit includes the BQ27Z855 and its peripheral components. These components are divided into the following groups:

- Cell voltage measurement interface
- Coulomb counter interface
- Temperature measurement
- 1.8V LDO (REG18)
- I^2C communication
- Interrupt to host interface via the INT pin

7.2.2.2.1 Cell Voltage Measurement Interface

The cell input is conditioned with a bypass capacitor (C_{BAT}) with a recommended typical value of 1µF connected between the device's BAT pin and GND reference (VSS). This capacitor acts to filter unwanted voltage transients and provides some ESD protection during cell connect. The BQ27Z855 device uses the BAT pin as the device's power source, so this bypass capacitor connected between the device's BAT pin and V_{SS} also acts to filter unwanted voltage ripples at the input of the device's internal 1.8V LDO.

A 0Ω resistor (R_{BAT}) can be placed between the postivie terminal of the cell and device BAT pin if needed to split the net names, but a higher resistor value is not recommended to ensure the proper linear charger functionality and entry in and out of supplement mode. See Section 7.2.2.3.2 and Section 7.2.2.3.3 for more details.

Also, as described in Figure 7-4, the top node of the cell must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a voltage drop from the PCB copper trace.

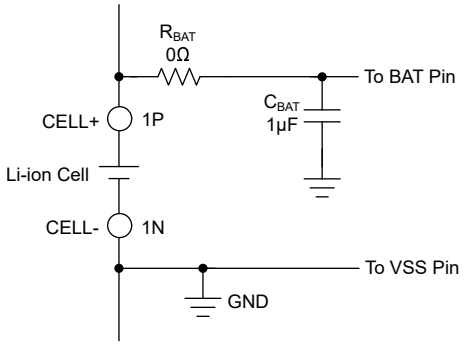


Figure 7-6. Cell Voltage Measurement Input

7.2.2.2.2 Coulomb Counter Interface

The BQ27Z855 uses an integrating delta-sigma ADC, or Coulomb counter, for current measurements. For more robust noise immunity, a capacitor can be added between the device's SRP and SRN pins to provide some low-pass filtering. Place a 0.1µF (C_{CCADC}) filter capacitor across the SRP and SRN inputs.

One key item to consider when choosing a sense resistor value is the tradeoff between the sense resistor value and the current resolution the device's Coulomb counter will report for gauging calculations. This tradeoff is detailed as follows:

- A higher sense resistor value yields a lower current resolution and can be more appropriate for applications using lower battery capacities and or lower currents
- A lower sense resistor value yields a higher current resolution and can be more appropriate for applications using higher battery capacities and or higher currents

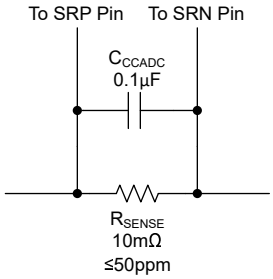


Figure 7-7. Coulomb Counter Interface

7.2.2.2.3 Temperature Measurement

For the BQ27Z855 device, the TS pin provides an internal thermistor bias network under firmware control to measure cell temeprature using an external NTC thermistor. The TS pin can be enabled with an integrated 18kΩ (TYP) linearization pull-up resistor to support the use of a 10kΩ at 25°C NTC external thermistor such as a Semitec 103AT-2. The BQ27Z855 device supports one external thermistor.

Optionally, a small 0.01µF capacitor (C_{TS}) can be connected in parallel to the external NTC thermistor for more robust noise immunity during temperature measurement and ESD performance.

The BQ27Z855 device also includes an internal temperature sensor that can be used for in place of or in addition to an external thermistor. This internal temeprature sensor can enabled and disabled via devie firmware.

Temperature-based protection settings can be configured via device firmware. Refer to the BQ27Z855 Technical Reference Manual for more details.

If the TS pin is unused, connect the pin to VSS or leave floating and configure data flash accordingly to disable measuring temperature on the unused TS pin. If the internal temeprature sensor is unused, configure data flash accordingly to disable the sensor.

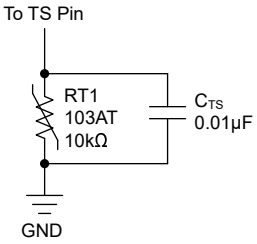


Figure 7-8. External NTC Thermistor Support

7.2.2.2.4 1.8V Low Dropout Regulator (REG18)

The BQ27Z855 includes a 1.8V low dropout regulator to support the device and provide regulated supply voltage for the device CPU and internal digital logic.

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A capacitor (C_{REG18}) with the recommended typical capacitance of 1.5µF is required to be connected as close to the REG18 pin as possible for optimal operation.

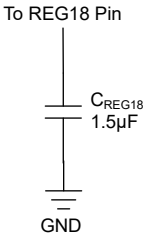


Figure 7-9. REG18 External Capacitor

7.2.2.2.5 I²C Communication (SDA, SCL)

The device's I²C clock and data pins have an absolute maximum voltage rating of 6V and have integrated high-voltage ESD protection circuits. However, adding a Zener diode or ESD TVS diode and 100Ω series resistors can provide more robust ESD performance.

The SDA and SCL pins have internal pull-down resistors. When the gas gauge senses that both lines are low (such as during removal of the battery pack), the device goes into SLEEP mode to conserve power.

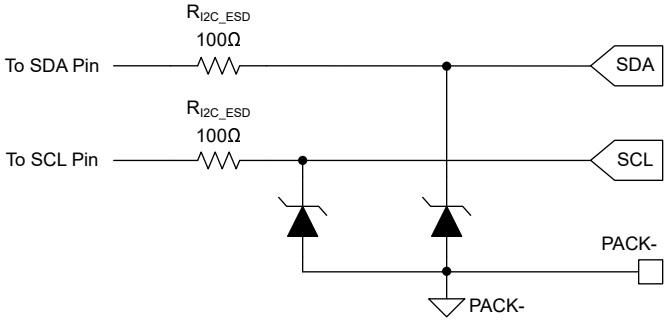


Figure 7-10. ESD Protection for I²C Communication

7.2.2.2.6 Interrupt to Host Interface (INT)

The device's INT pin also has an absolute maximum voltage rating of 6V and integrated high-voltage ESD protection circuits. Similar to the I²C pins, a Zener diode or ESD TVS diode and a 100Ω series resistor can be added for more robust ESD performance.

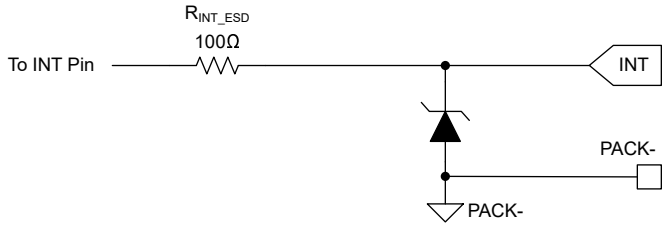


Figure 7-11. ESD Protection for INT Output to System-side Host

7.2.2.3 Current Limiter Circuit

The current limiter circuit includes the BQ27Z855 and its peripheral components. These components are divided into the following groups:

- Protection FETs
- CP control logic and capacitor
- Voltage-based feedback interface

- Current-based feedback interface
- BAT-PACK dedicated voltage comparator (DCOMP)

7.2.2.3.1 Protection FETs and Compatibility with BQ27Z855

The BQ27Z855 device supports driving external N-channel protection FETs using integrated NFET drivers. When the device's current limiter feature is enabled, the device controls the CHG FET in a linear operating mode to function as a linear charger. To ensure proper charging functionality by the device's current limiter, select the N-channel CHG and DSG FETs for a given application based on the following NFET parameters typically specified in the FET datasheet:

1. The gate resistance (R_G) of the CHG FET
2. The input capacitance (C_{ISS}) of the CHG FET

For the selected NFETs to be compatible with the BQ27Z855 device, the product of R_G and C_{ISS} must be less than 7µΩ×F. In other words:

$$R_G \times C_{ISS} < 7\mu\Omega \times F = R_G \times (C_{GS} + C_{GD}) < 7\mu\Omega \times F \quad (1)$$

For example, if the FET's maximum R_G = 700Ω, the FET's maximum C_{ISS} value cannot exceed 10nF.

Following this criteria ensures the device's CC and CV loops remain stable and no unwanted oscillations occur during charging.

Additionally, the thermal performance of the FETs must also be carefully considered based on the battery charging parameters for a particular application.

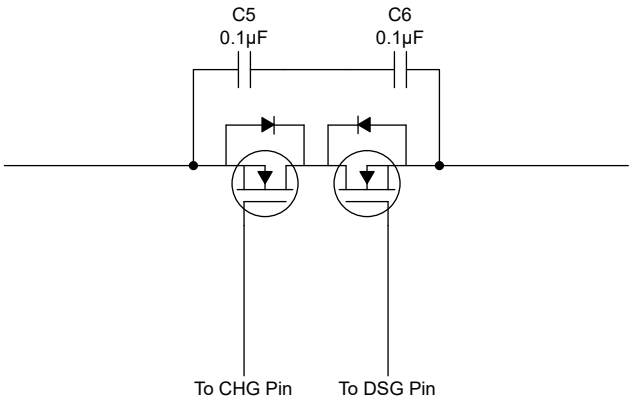


Figure 7-12. Protection FETs for Current Limiting

7.2.2.3.2 CP Control Logic and Capacitor

To support supplement mode and consecutive high system load pulses, the device turns the CHG FET ON using internal control logic and an external capacitor (C_{CP}) connected between the device's CP and CP_BOOT pins. This capacitor is discharged to the device's CHG pin when the device enters the CHG = LIN_ON state and is recharged immediately after the CHG FET turns ON. Additionally if the device's current limiter is enabled, the external C_{CP} capacitor is charged during device operation regardless of whether the device is actively charging a battery.

When the external CP capacitor charges, the capacitor charges using the available battery voltage. To ensure the device properly enters and exits supplement mode, additional resistance between the positive terminal of the cell (CELL+) and the device's BAT pin is not recommended. This prevents unintended device brownouts when the CP capacitor must be recharged in between high system load pulses to support the next entry into supplement mode. The total resistance between CELL+ and the device BAT pin is not recommended to exceed 110mΩ.

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Place the external CP capacitor with the recommended typical capacitance of 1µF connected between the CP and CP_BOOT pins as close to the device as possible.

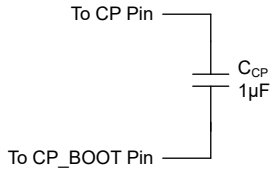


Figure 7-13. CP Capacitor

7.2.2.3.3 Voltage-based Feedback Interface

As stated in Section 7.2.2.2.1, the device measures cell voltage using the device's BAT pin. The measured cell voltage value provides the feedback needed for the device's current limiter to properly regulate charging current and charging voltage.

There are no additional external componenets required at the device's BAT pin to support the current limiter functionality besides the required components stated in Section 7.2.2.2.1.

In addition to the recommendation on the total resistance between CELL+ and the device BAT pin stated in Section 7.2.2.3.2, the following resistances must also be carefully considered to ensure proper charging and supplement mode behavior:

- The parasitic resistance between the BAT capacitor (C_{BAT}) and device BAT pin is not recommended to exceed 60mΩ
- The connection resistance between CELL+ and the C_{BAT} capacitor is not recommended to exceed 140mΩ

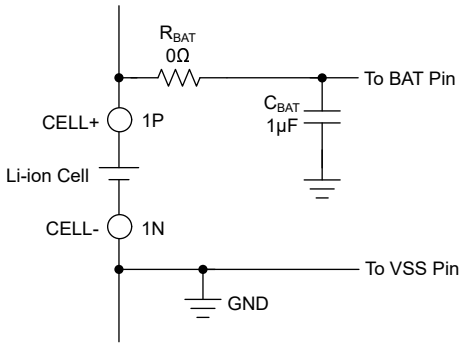


Figure 7-14. Voltage-based Feedback Interface

7.2.2.3.4 Current-based Feedback Interface

As stated in Section 7.2.2.2.2, the device uses an integrating delta-sigma ADC, or Coulomb counter, for current measurements by converting the voltage difference across a sense resistor between the SRP and SRN terminals. The measured current value provides the feedback needed for the device's current limiter to properly regulate charging current and charging voltage.

There are no additional external componenets required at the device's SRP and SRN pins to support the current limiter functionality besides the required components stated in Section 7.2.2.2.2.

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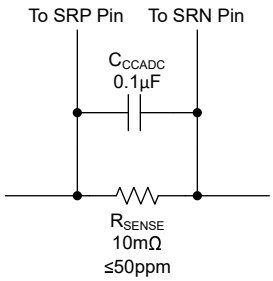


Figure 7-15. Current-based Feedback Interface

7.2.2.3.4.1 Sense Resistor Impact on Current-based Feedback

As stated in Section 7.2.2.2.2, choosing a sense resistor (R_{SENSE}) value presents a tradeoff between the sense resistor value and the current resolution reported by the device's Coulomb counter for gauging calculations. This tradeoff is also present when the device's current limiter is enabled and impacts the current resolution the device senses and regulates charging current at.

This tradeoff is detailed as follows:

- A higher sense resistor value yields a lower current resolution and can be more appropriate for applications using lower battery capacities and or lower charging currents
- A lower sense resistor value yields a higher current resolution and can be more appropriate for applications using higher battery capacities and or higher charging currents

Using a combination of a particular sense resistor value and particular charging currents impacts the charging current resolution of the device since the device's battery charging functionality scales based on the sense resistor value.

In addition to the resolution, the sense resistor value also impacts the minimum charging current setting to achieve particular charging current accuracy. As a general guideline to achieve charging current accuracy of ±10%, the charging current settings programmed in device data flash is not recommended to be below the minimum values given in Table 7-3. Charging current settings below the recommended range when using a particular sense resistor value can still be programmed, but charging current regulated by the device may not be as accurate as ±10%. The charging current programmed in device data flash should also not exceed $I_{CHG(MAX)}$ as specified in the Current Limiter Specifications table. The combination of sense resistor value and charging current settings must be considered carefully then.

The sense resistor value's impact on charging current resolution and accuracy must be considered when programming the fast charge and precharge current settings in device data flash.

Table 7-3 provides guidance on how the sense resistor value impacts the charging current (I_{CHG}) resolution and recommended range of the device:

Table 7-3. I_{CHG} Resolution and Accuracy Versus R_{SENSE}

	0.5mΩ	1mΩ	2mΩ	5mΩ	10mΩ	20mΩ	50mΩ	100mΩ
I_{CHG} Resolution (mA)	29.30	14.65	7.32	2.93	1.46	0.73	0.29	0.15
Minimum I_{CHG} Setting (mA)(1)	925	463	231	93	46	23	9	5

(1) General guideline on minimum I_{CHG} setting to achieve ±10% I_{CHG} accuracy. Programming lower currents in device data flash may not be as accurate.

A lower termiantion current (I_{TERM}) setting below the recommended I_{CHG} range is allowed, but must not exceed $I_{TERM(MAX)}$ as specified in the Current Limiter Specifications table. Similar to the above general guideline to achieve ±10% I_{CHG} accuracy, the I_{TERM} setting programmed in device data flash is not recommended to be

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below the minimum values given in Table 7-4 to achieve ±10% I_{TERM} accuracy. I_{TERM} settings below the recommended range when using a particular sense resistor value can still be programmed, but the I_{TERM} value detected by the device may not be as accurate as ±10%.

Table 7-4 provides guidance on how the sense resistor value impacts the I_{TERM} resolution and recommended range of the device:

Table 7-4. I_{TERM} Resolution and Accuracy Versus R_{SENSE}

	0.5mΩ	1mΩ	2mΩ	5mΩ	10mΩ	20mΩ	50mΩ	100mΩ
I_{TERM} Resolution (mA)	1.85	0.92	0.46	0.18	0.09	0.05	0.02	0.01
Minimum I_{TERM} Setting (mA)(1)	55	28	14	6	3	1	1(2)	1(2)

(1) General guideline on minimum I_{TERM} setting to achieve ±10% I_{TERM} accuracy. Programming lower currents in device data flash may not be as accurate.
(2) There is no recommended minimum I_{TERM} value to consider with this R_{SENSE} to achieve ±10% I_{TERM} accuracy. The programmable step size and minimum nonzero setting for ***Charge Term Taper Current*** in device data flash is 1mA.

7.2.2.3.4.2 Sense Resistor Impact on CHG FET State Transitions

The value of the sense resistor also impacts when the device can trigger a CHG FET state transition in Linear or Ideal Diode mode. The device uses a Coulomb counter-based charge current measurement digital filter (CC3) to detect when V_{SRP} - V_{SRN} ≥ $V_{TH_OFF_FINE}$ to turn the CHG FET OFF. Since any positive or charging current flowing through the sense resistor creates a differential voltage across the sense resistor, the CC3 digital filter effectively triggers a CHG FET state transition at higher or lower detected charging current based on the value of R_{SENSE}.

This tradeoff in the "detected charging current threshold" caused by the value of R_{SENSE} is detailed as follows:

- A higher R_{SENSE} value yields a lower detected charging current threshold
- A lower R_{SENSE} value yields a higher detected charging current threshold

For example, with a combination of $V_{TH_OFF_FINE}$ = 450µV and R_{SENSE} = 20mΩ the device's CC3 digital filter can detect charging currents as low as 22.5mA to turn the CHG FET OFF (CHG = LIN_OFFT in Linear mode or CHG = ID_OFF in Ideal Diode mode). Using R_{SENSE} = 1mΩ increases this "detected charging current threshold" to 450mA.

This consideration is particularly crucial for Ideal Diode mode if the device needs to detect smaller charge currents to turn the CHG FET OFF when a valid input voltage source is connected at PACK+.

7.2.2.3.5 BAT-PACK Dedicated Voltage Comparator (DCOMP)

The BQ27Z855 device uses an integrated dedicated voltage comaprator (DCOMP) to assess the difference in voltage between V_{BAT} and V_{PACK}. This DCOMP is used to control the state of the CHG FET depending on several system parameters when the device is in Linear mode and Ideal Diode mode.

The differential voltage DCOMP senses and compares the voltage thresholds (V_{TH_ON} and V_{TH_OFF}) to transition between CHG FET states is based on the voltage from node A to node B as seen in Figure 7-16.

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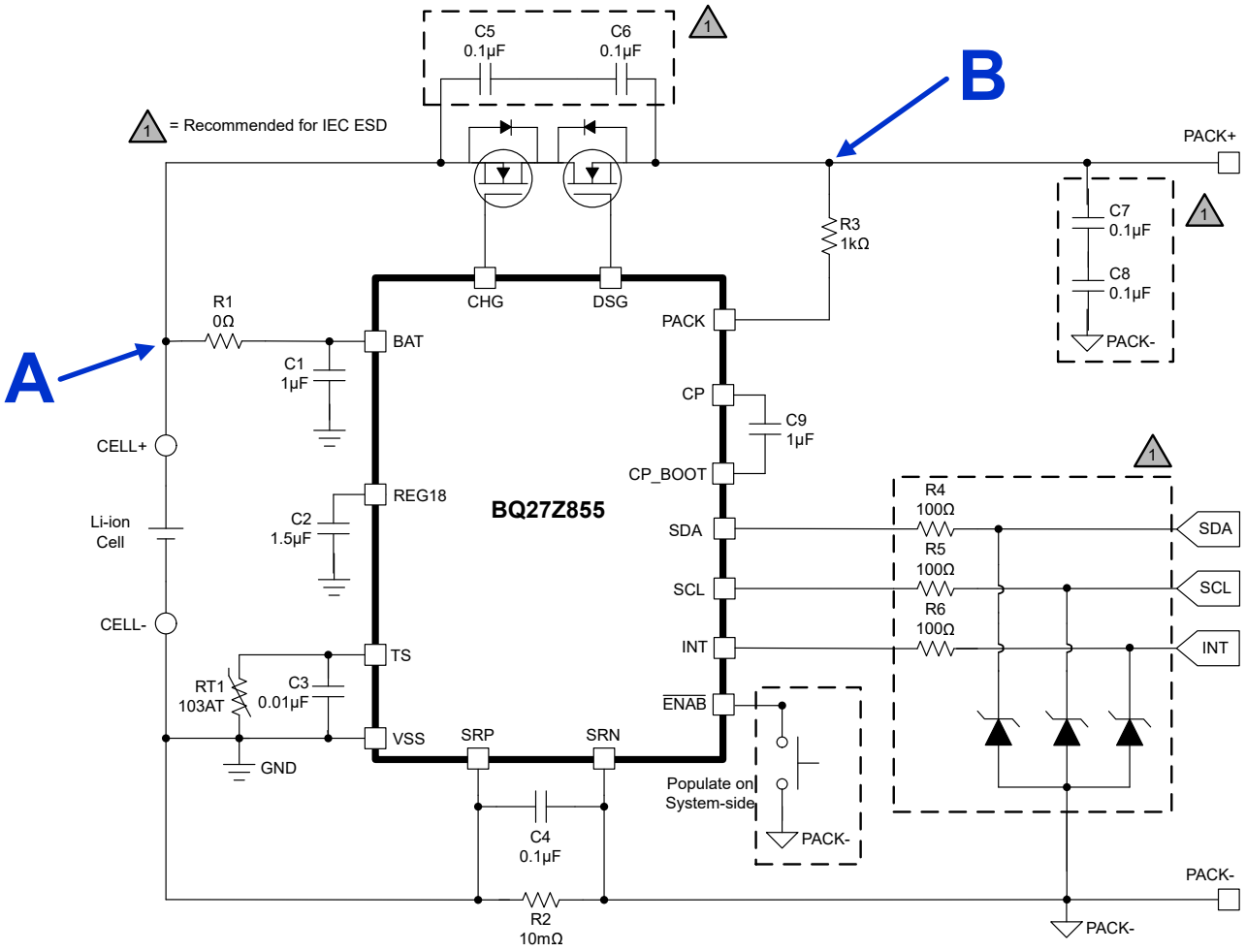


Figure 7-16. DCOMP Sense Points

To ensure optimal DCOMP sensing performance, the total external resistance (including parasitic resistance) and parasitic capacitance between node B and the device PACK pin is not recommended to exceed a time constant value of 20ns.

The resistor divider network or total resistance between the DCOMP sense points at node A and node B (designated in red in Figure 7-17) determines the actual voltage sensed by the device's DCOMP input.

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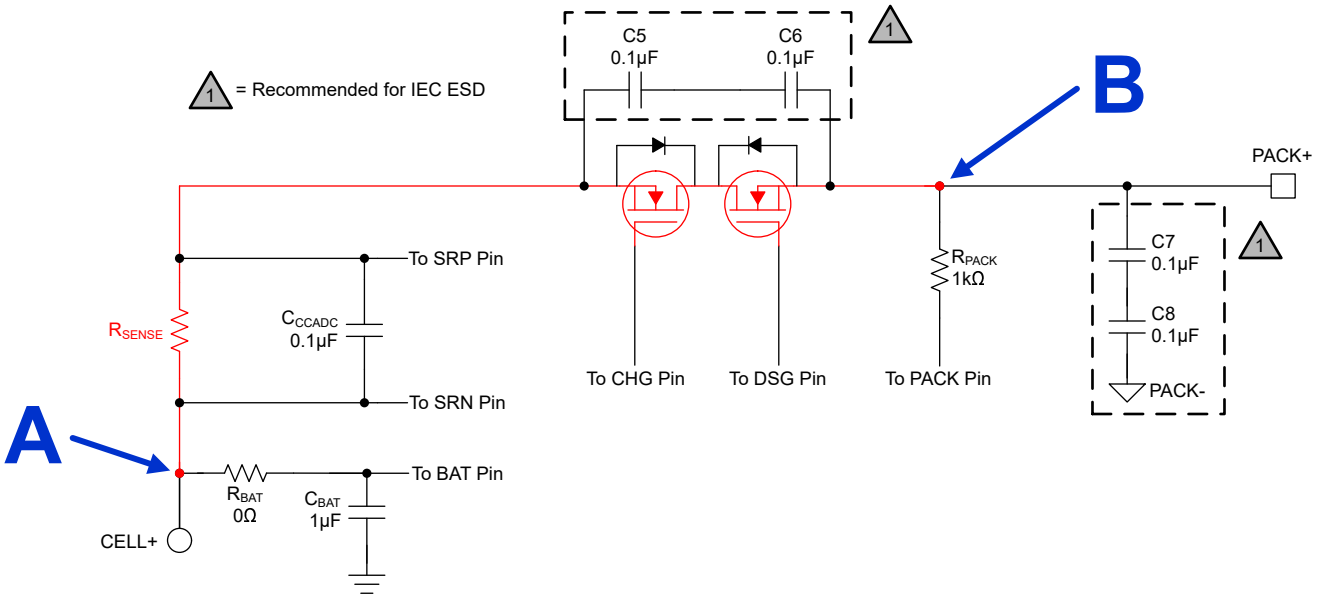


Figure 7-17. DCOMP Sense Resistances

In other words, for the device to transition between CHG FET states within Linear and Ideal Diode modes, DCOMP effectively triggers a CHG FET state transition based on the current flowing from PACK+ to CELL+ or vice versa. This "effective current threshold" (or "$I_{TRIGGER}$") is determined based on the following:

1. Voltages at the sense points of node A (device BAT pin) to node B (device PACK pin)
2. Total resistance between the BAT and PACK sense points, including all parasitic resistances ($R_{PACK-TO-BAT}$)

At what current DCOMP can trigger the CHG FET to turn ON or OFF is then determined by:

$$I_{TRIGGER} \geq \frac{V_{TH_X}}{R_{PACK-TO-BAT}} \quad (2)$$

Where:

V_{TH_X} can be either V_{TH_ON} or V_{TH_OFF} depending on if the device is in Linear or Ideal Diode mode as stated in the Current Limiter Specifications table.

7.2.2.3.5.1 Impact of Sense Resistor Configuration on DCOMP Sensing

When using the current limiter function of the BQ27Z855 device, a key aspect to consider is whether to configure the external sense resistor between the SRP and SRN terminals for low-side or high-side current sensing. The location of the sense resistor presents a tradeoff of at what "effective current threshold" ($I_{Trigger}$) the device's DCOMP will trigger CHG FET state transitions. This is because the location of the sense resistor impacts the total resistance between the BAT and PACK sense points ($R_{PACK-TO-BAT}$) of the DCOMP.

If the sense resistor is configured as high-side, the sense resistor value contributes to the $R_{PACK-TO-BAT}$ value. This results in a decreased $I_{TRIGGER}$ threshold at which the DCOMP turns the CHG FET ON or OFF.

For example as seen in the below Figure 7-18 diagram, the sense resistor is included within the total $R_{PACK-TO-BAT}$ designated in red. If the device is in Ideal Diode mode and currently in the CHG = ID_ON state, then the voltage threshold for DCOMP to transition the CHG FET state from CHG = ID_ON to CHG = ID_OFF is V_{TH_OFF} = 5mV. In this example, if the sense resistor value is 20mΩ and the combined source-to-source On resistance of the protection FETs and all parasitic resistance between the BAT and PACK sense points is 5mΩ, $I_{TRIGGER}$ is then the following:

$$I_{TRIGGER} \geq \frac{V_{TH_X}}{R_{PACK-TO-BAT}} = \frac{V_{TH_OFF}}{R_{SENSE} + R_{SS(ON)} + R_{PARASITIC}} \quad (3)$$

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$$I_{TRIGGER} \geq \frac{5mV}{20m\Omega + 5m\Omega} \quad (4)$$

$$I_{TRIGGER} \geq 200mA \quad (5)$$

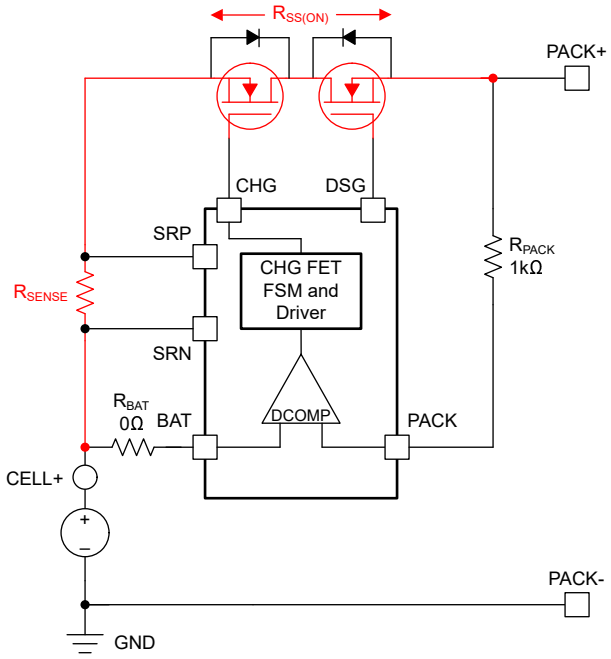


Figure 7-18. DCOMP Sense Resistances with High-side Current Sensing

If the sense resistor is configured as low-side, the sense resistor value does not contribute to the $R_{PACK\text{-}TO\text{-}BAT}$ value. This results in an increased $I_{TRIGGER}$ threshold at which the DCOMP turns the CHG FET ON or OFF.

For example as seen in the below Figure 7-19 diagram, the sense resistor is not included within the total $R_{PACK\text{-}TO\text{-}BAT}$ designated in red. Using the same example scenario and parameter values described above in the high-side sense resistor case, the total $R_{PACK\text{-}TO\text{-}BAT}$ value would now decrease by the example R_{SENSE} = 20mΩ in this low-side sense resistor case. The $I_{TRIGGER}$ threshold then becomes the following:

$$I_{TRIGGER} \geq \frac{V_{TH_X}}{R_{PACK-TO-BAT}} = \frac{V_{TH_OFF}}{R_{SS(ON)} + R_{PARASITIC}} \quad (6)$$

$$I_{TRIGGER} \geq \frac{5mV}{5m\Omega} \quad (7)$$

$$I_{TRIGGER} \geq 1A \quad (8)$$

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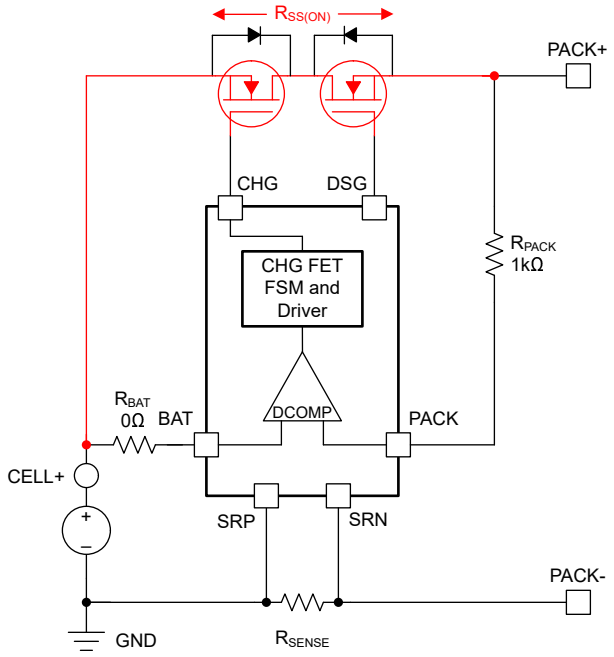


Figure 7-19. DCOMP Sense Resistances with Low-side Current Sensing

The key takeaway to consider when using the BQ27Z855 for an application based on these two examples is how the high-side or low-side configuration of the sense resistor impacts at what current the device's DCOMP will trigger a CHG FET state transition.

- High-side R_{SENSE}: DCOMP can turn the CHG FET OFF or ON at lower currents
- Low-side R_{SENSE}: DCOMP can turn the CHG FET OFF or ON at higher currents

This consideration is particularly crucial for Ideal Diode mode if an overall faster response by the device is needed to turn the CHG FET OFF when a valid input voltage source is connected at PACK+.

7.2.2.3.6 System-level Recommendations

To ensure proper system-level performance and device battery charging functionality, the following system-level recommendations must be followed:

- The total system capacitance (C_{SYS}) must be within the inclusive range of 20µF to 1.2mF
  - This ensures when the device's MINSYS regulation loop remains stable when active and no unwanted oscillations occur during charging

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7.2.3 Application Curves

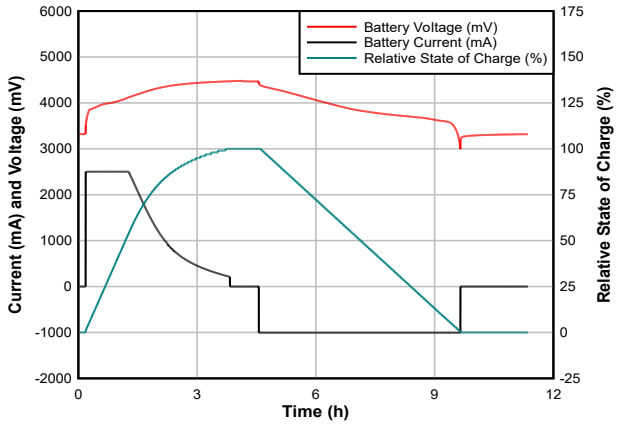


Figure 7-20. Charge and Discharge Cycle Tracking SoC Accuracy

8 Power Supply Recommendations

The BQ27Z855 device uses the BAT pin as its power source. The BAT pin powers the internal voltage sources and 1.8V LDO that supply references for the device.

A capacitor (C_{BAT}) with the recommended typical capacitance of 1µF connected between the BAT and VSS pins is recommended and must be placed as close to the BAT pin as possible.

9 Layout

9.1 Layout Guidelines

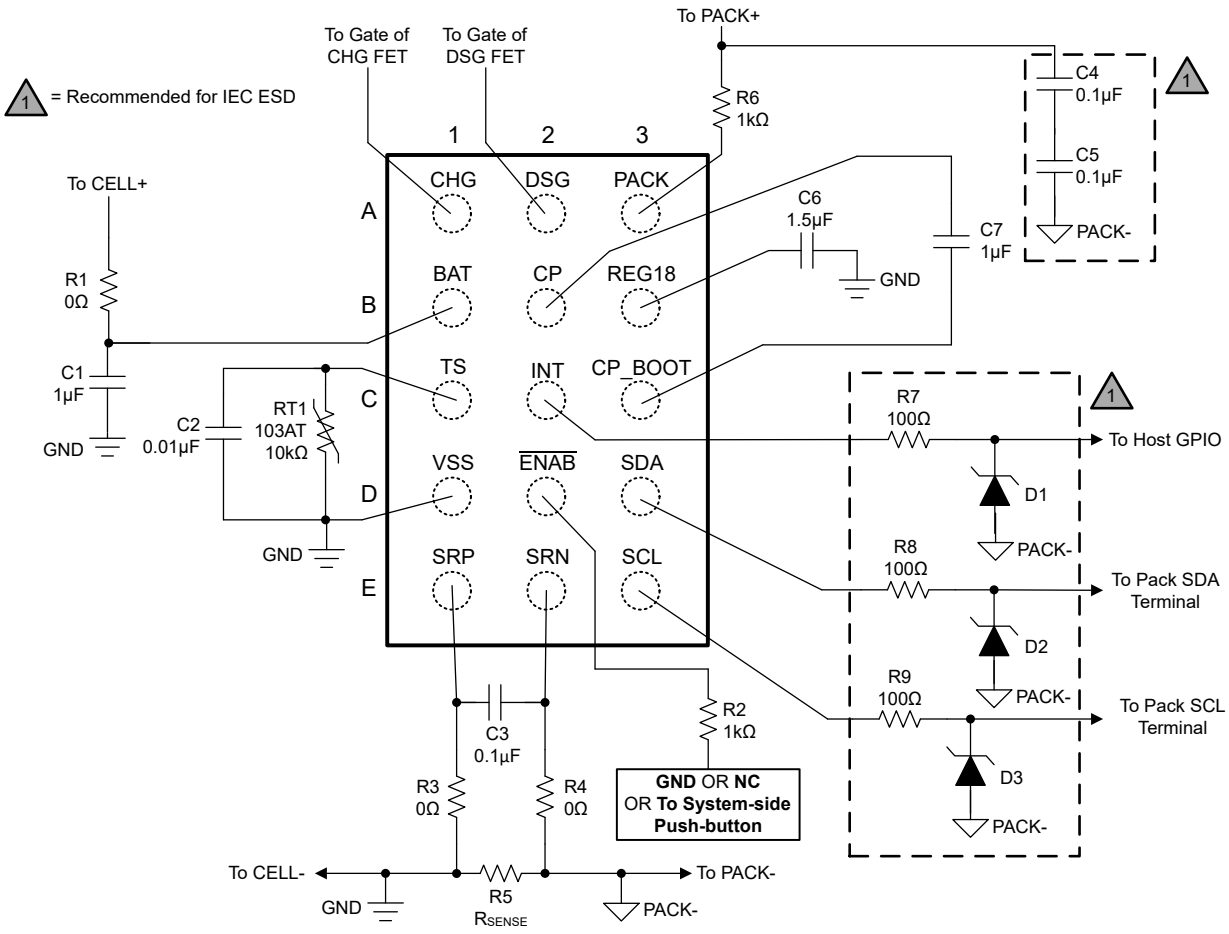
- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short circuit protection ranges and desired protection threshold setting of the BQ27Z855. Select the smallest sense resistor value possible to minimize thermal dissipation and still maintain required measurement accuracy. The value of the sense resistor impacts the differential voltage generated across the BQ27Z855 SRP and SRN nodes during a short circuit. These pins have a differential voltage and must not exceed V_{CCADC_IN} of ±0.1V for normal operation. Parallel sense resistors can be used as long as good Kelvin sensing is maintained. The device is designed to support a minimum sense resistor value of 0.5mΩ.
- The BAT pin must be tied directly to the positive terminal of the battery cell. The quality of the Kelvin connection to the battery cell is critical. The Kelvin connection at the positive terminal of the cell (CELL+) avoids any errors due to a voltage drop or impact on the input power supply of the device caused by the copper trace. The Kelvin connection to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the cell voltage.
- In reference to the gas gauge circuit, the following features require attention for component placement and layout:
  - **BAT decoupling capacitor:** Place a capacitor (C_{BAT}) with the recommended typical capacitance of 1µF connected between the BAT and VSS pins as close to the BAT pin as possible.
  - **Coulomb counter interface at the SRP and SRN pins:** The BQ27Z855 gas gauge uses an integrating delta-sigma ADC for current measurements. Place a 0.1µF filter capacitor across the SRP and SRN pins. Place the capacitor as close as possible to the device. Route the traces from the sense resistor as differential pairs to the filter capacitor and SRP and SRN pins. Adding a ground plane around the filter network can provide additional noise immunity.
  - **REG18 decoupling capacitor:** The device's internal 1.8V LDO requires an external decoupling capacitor to support proper device operation. Place a capacitor (C_{REG18}) with the recommended typical capacitance of 1.5µF connected between the REG18 and VSS pins as close to the REG18 pin as possible.

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  - **I²C communication and INT pin ESD external protection:** The I²C clock and data pins and INT pin have integrated high-voltage ESD protection circuits. However, adding a Zener diode and series resistor provides more robust ESD performance. The I²C clock and data lines have internal pull-down resistors. When the gas gauge senses that both lines are low (such as during removal of the pack), the device goes into SLEEP mode to conserve power.
- In reference to the current limiter circuit, the following features require attention for component placement and layout:
  - **CP capacitor:** Place a capacitor (C_{CP}) with the recommended typical capacitance of 1µF connected between the CP and CP_BOOT pins as close to the device as possible. Any trace resistance between the CELL+ terminal of the battery cell and the device BAT pin must be carefully considered as the total resistance between CELL+ and the device BAT pin is not recommended to exceed 110mΩ to prevent unintended device brownouts during charging.
  - **Voltage-based Feedback Interface:** Follow the same layout guidelines stated above for the BAT decoupling capacitor in addition to carefully consideration of the total resistance between the BAT capacitor (C_{BAT}) and device BAT pin and between CELL+ and the C_{BAT} capacitor to ensure proper charging and supplement mode behavior. The parasitic resistance between the C_{BAT} capacitor and device BAT pin is not recommended to exceed 60mΩ. The connection resistance between CELL+ and the C_{BAT} capacitor is not recommended to exceed 140mΩ.
  - **Current-based Feedback Interface:** Follow the same layout guidelines stated above for the Coulomb counter interface at the SRP and SRN pins.
  - **BAT-PACK DCOMP:** To ensure optimal DCOMP sensing performance, the total external resistance (including parasitic resistance) and parasitic capacitance between the PACK+ node (node B in Figure 7-16) and the device PACK pin is not recommended to exceed a time constant value of 20ns. Additionally, any parasitic trace resistance between the BAT and PACK sense points of the device must be carefully considered as the parasitic trace resistance impacts at what current the device's DCOMP will trigger a CHG FET state transition.

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9.2 Layout Example



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10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *BQ27Z855 Technical Reference Manual*
- Texas Instruments, *BQ27Z855 EVM User's Guide*
- Texas Instruments, *BQStudio Software*
- Texas Instruments, *Dynamic Z-Track™ Technology: An Advanced Battery Gauging Algorithm for Dynamic Load Applications*
- Texas Instruments, *Implementation of Elliptic Curve Cryptography Authentication on TI Battery Fuel Gauges*
- Texas Insturments, *IC Package Thermal Metrics*

10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2026) to Revision A (November 2026)	Page
• Updated datasheet status from *Advanced Information* to *Production Data*	1
• Increased PACK pin Absolute Maximum Rating	5
• Updated the supply current modes and typical values	6
• Updated V_{REG18} POR Hysteresis	7
• Added $V_{PACK_CLAMP_SHTDWN}$ for the PACK_CLAMP voltage threshold while in shutdown	8
• Updated the wake-up voltage threshold error	10
• Added V_{DPPM}, Updated I_{TERM_ACC}	12
• Added Typical Characteristics	16
• Added 1kΩ series resistor for $\overline{ENAB}$	19
• Added I^2C timeout description regarding t_{LOW} and t_{HIGH} for SCL	19
• Updated ZVCHG description to align with the implementation	20
• Removed Si-anode support	23
• Edited CHG FET Control section	24
• Updated Linear Charge Profile State Machine diagram	26
• Updated 5-step CC-CV to 3-step CC-CV, removed 5-step CC operation	29
• Updated Step-charging Charge Profile State Machine diagram	29
• Updated OTA description to align with the implementation	34
• Edited SHUTDOWN mode description	34
• Added example table for dual N-channel MOSFETs which can be used with BQ27z855	39
• Added Application Curves	52
• Removed co-layout example, added layout example	54

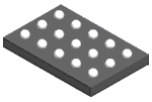
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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12.1 Mechanical Data

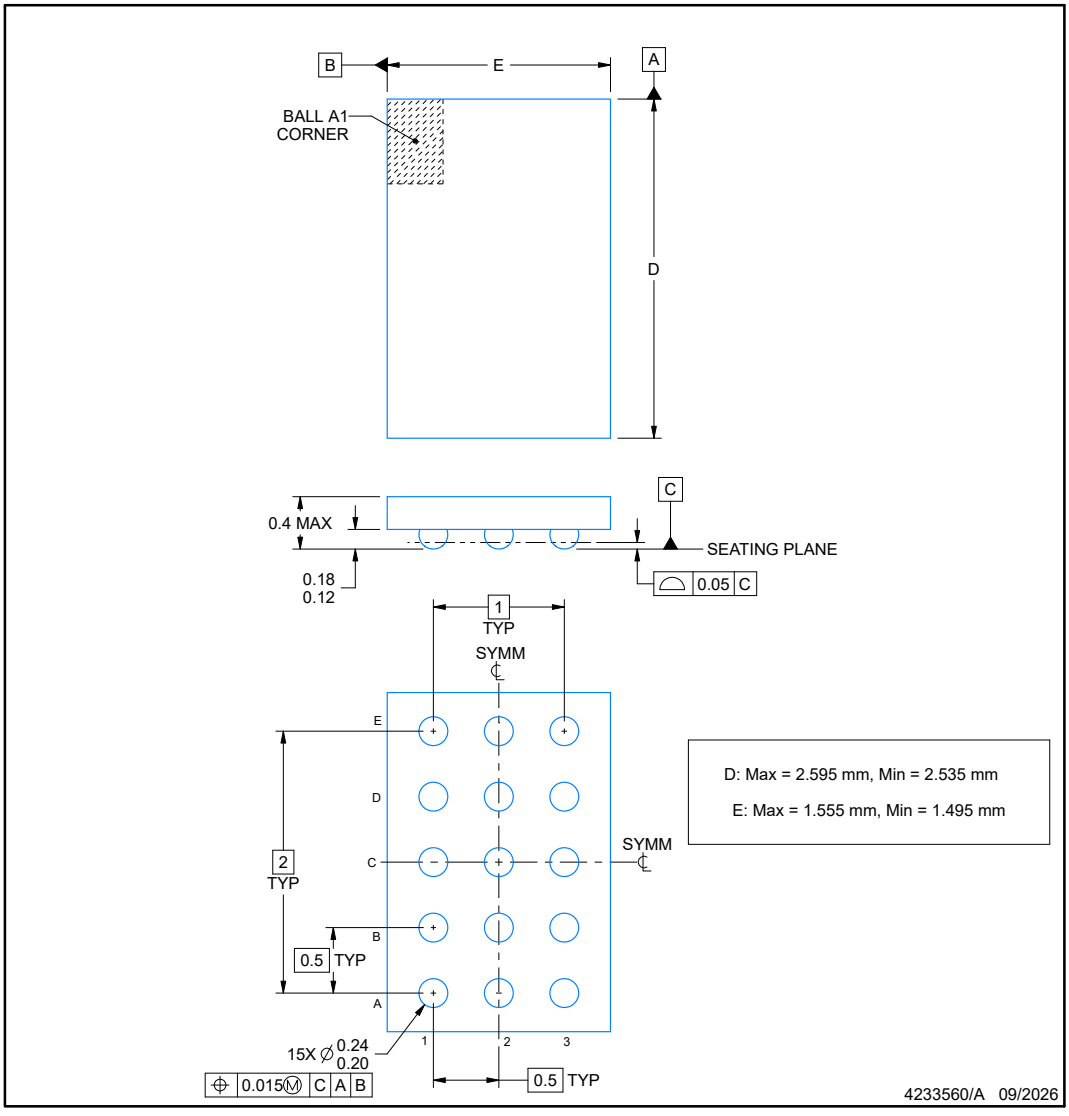
YAH0015-C02



PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

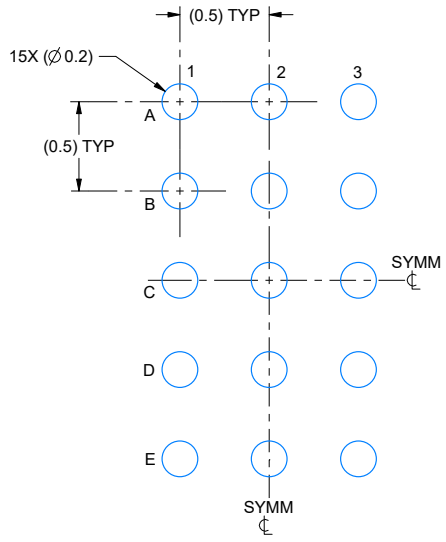
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EXAMPLE BOARD LAYOUT

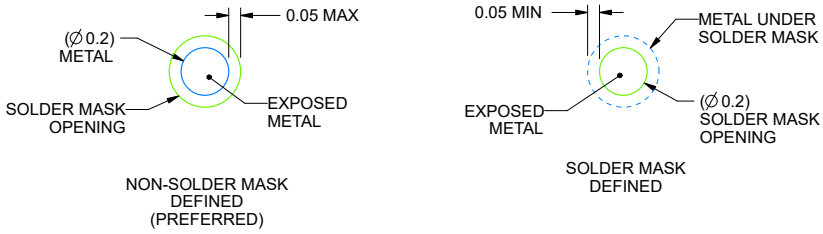
YAH0015-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4233560/A 09/2026

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

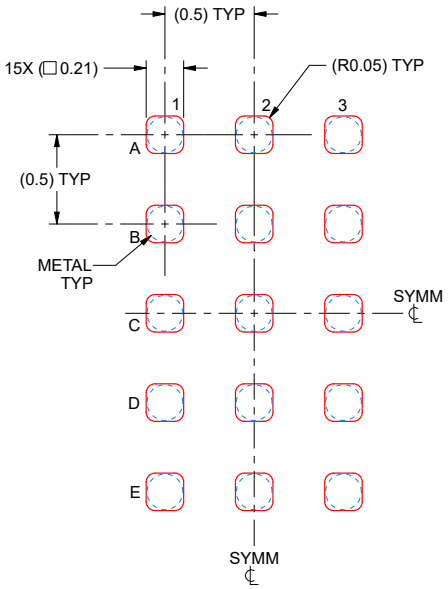
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EXAMPLE STENCIL DESIGN

YAH0015-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4233560/A 09/2026

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ27Z855YAHR	Active	Production	DSBGA (YAH) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B855

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

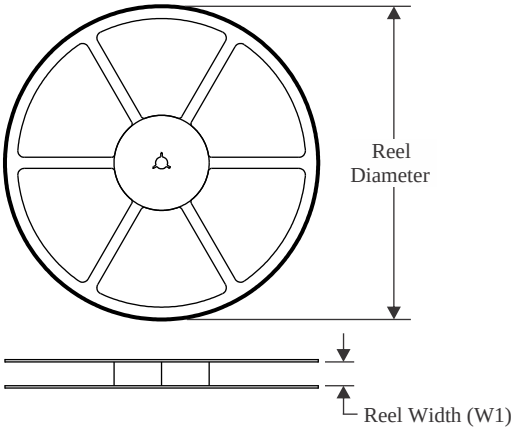
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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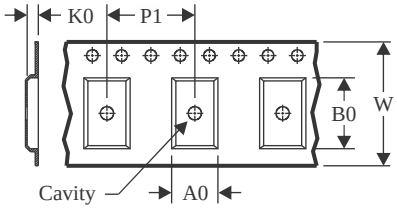
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

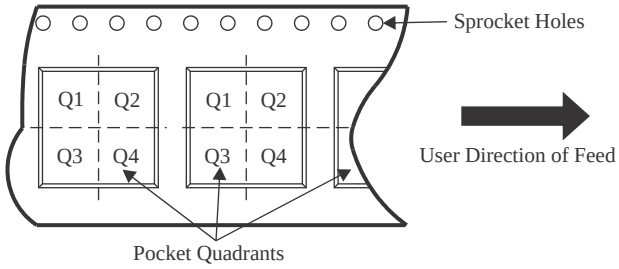


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

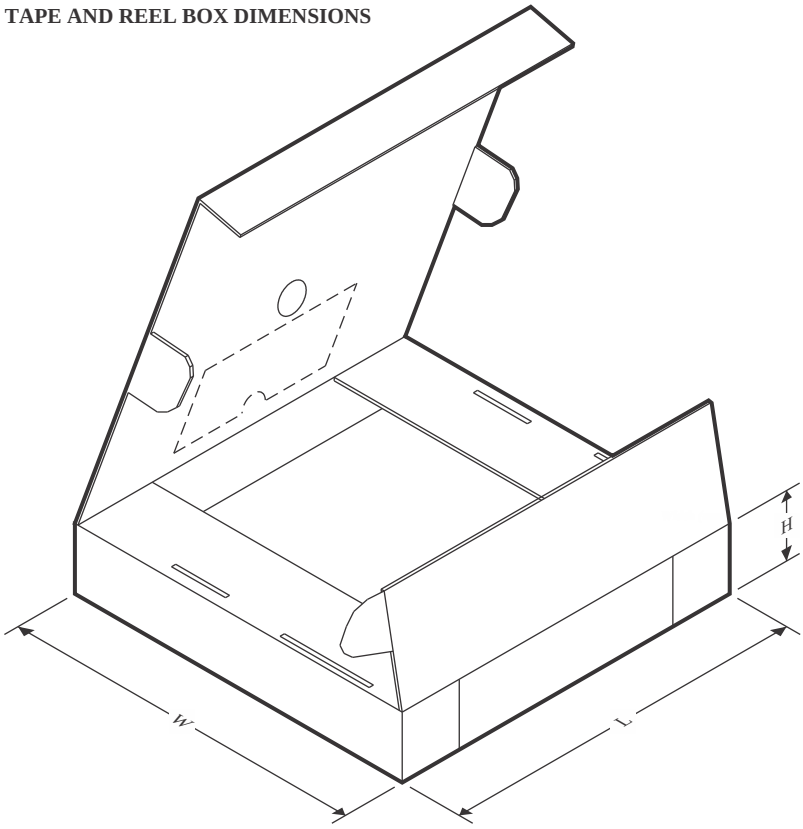
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27Z855YAHR	DSBGA	YAH	15	3000	180.0	8.4	1.7	2.76	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27Z855YAHR	DSBGA	YAH	15	3000	182.0	182.0	20.0

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Last updated 10/2025