

# CDx4AC109 Dual J- $\bar{K}$ Positive-Edge-Triggered Flip-flops with Clear and Preset

## 1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Balanced propagation delays
- $\pm 24\text{mA}$  output drive current
  - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

## 2 Description

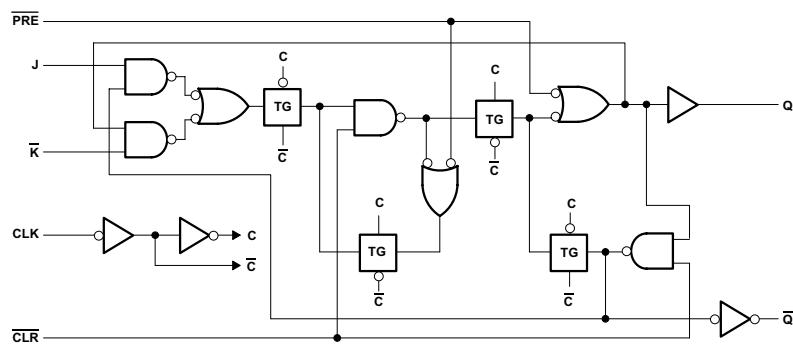
The CD74AC109-Q1 device contains two independent J-K positive edge triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs that meets the setup-time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. The device is qualified for automotive applications.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE <sup>(2)</sup>
CDx4AC109	D (SOIC, 16)	9.90mm x 3.90mm
	N (PDIP, 16)	19.3mm x 6.35mm
	J (CDIP, 16)	19.56mm x 6.92mm

(1) For more information, see [Mechanical, Packaging, and Orderable Information](#).

(2) The body size (length  $\times$  width) is a nominal value and does not include pins.



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**Logic Diagram**



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### 3 Pin Configuration and Functions

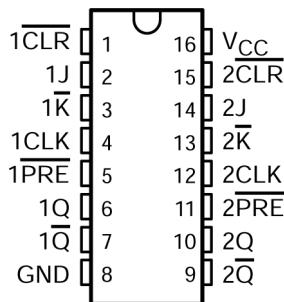


Figure 3-1. CD54AC109 J Package; CD74AC109 D or N Package; 16-Pin CDIP, SOIC or PDIP (Top View)

Table 3-1. Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1CLR	1	I	Active low clear for first channel
1J	2	I	J input for first channel
1K	3	I	Active low K input for first channel
1CLK	4	I	CLK input for first channel
1PRE	5	I	Active low Preset input for first channel
1Q	6	O	True Q output for first channel
1Q	7	O	Inverted Q output for first channel
GND	8	-	Ground
2Q	9	O	True Q output for second channel
2Q	10	O	Inverted Q output for second channel
2PRE	11	I	Active low preset for second channel
2CLK	12	I	Clock input for second channel
2K	13	I	Active low K input for second channel
2J	14	I	J input for second channel
2CLR	15	I	Active low clear for second channel
V <sub>CC</sub>	16	-	Power pin

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6	V
I <sub>IK</sub> <sup>(2)</sup>	Input clamp current (V <sub>I</sub> < 0 V or V <sub>I</sub> > V <sub>CC</sub> )		±20	mA
I <sub>OK</sub> <sup>(2)</sup>	Output clamp current (V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> )		±50	mA
I <sub>O</sub>	Continuous output current (V <sub>O</sub> > 0 V or V <sub>O</sub> < V <sub>CC</sub> )		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), Level H0 <sup>(1)</sup>	±2000 V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

(over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>)

		T <sub>A</sub> = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.5 V	1.2	1.2	1.2			V
		V <sub>CC</sub> = 3 V	2.1	2.1	2.1			
		V <sub>CC</sub> = 5.5 V	3.85	3.85	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.5 V	0.3	0.3	0.3	0.3		V
		V <sub>CC</sub> = 3 V	0.9	0.9	0.9	0.9		
		V <sub>CC</sub> = 5.5 V	1.65	1.65	1.65	1.65		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		-24	-24	-24	-24	mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		24	24	24	24	mA
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.5 V to 3 V		50	50	50		ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V		20	20	20	20	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>				CD74AC109		UNIT
				D (SOIC)	N (PDIP)	
				16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance			73	67	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ C$		$-55^\circ C$ to $125^\circ C$		$-40^\circ C$ to $85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	1.5 V	1.4	1.4		1.4		V
			3 V	2.9	2.9		2.9		
			4.5 V	4.4	4.4		4.4		
		$I_{OH} = -4 \text{ mA}$	3 V	2.58	2.4		2.48		
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94	3.7		3.8		
		$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V		3.85				
		$I_{OH} = -75 \text{ mA}^{(1)}$	5.5 V				3.85		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	1.5 V		0.1	0.1	0.1		V
			3 V		0.1	0.1	0.1		
			4.5 V		0.1	0.1	0.1		
		$I_{OL} = 12 \text{ mA}$	3 V		0.36	0.5	0.44		
		$I_{OL} = 24 \text{ mA}$	4.5 V		0.36	0.5	0.44		
		$I_{OL} = 50 \text{ mA}^{(1)}$	5.5 V			1.65			
		$I_{OL} = 75 \text{ mA}^{(1)}$	5.5 V				1.65		
$I_I$	$V_I = V_{CC}$ or GND		5.5 V		$\pm 0.1$	$\pm 1$	$\pm 1$	$\mu A$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V		4	80	40	$\mu A$	
$C_i$					10	10	10	$pF$	

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- $\Omega$  transmission-line drive capability at  $85^\circ C$  and 75- $\Omega$  transmission-line drive capability at  $125^\circ C$ .

## 4.6 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 1.5 \text{ V}$  (unless otherwise noted)

			$-55^\circ C$ to $125^\circ C$		$-40^\circ C$ to $85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency			8		9	MHz
$t_w$	Pulse duration	CLK high or low		63		55	ns
		CLR or PRE low		56		49	
$t_{su}$	Setup time, before $CLK\uparrow$	J or $\bar{K}$		69		61	ns
$t_h$	Hold time, after $CLK\uparrow$	J or $\bar{K}$		0		0	ns
$t_{rec}$	Recovery time, before $CLK\uparrow$	CLR $\uparrow$ or PRE $\uparrow$		31		27	ns

## 4.7 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency			71		81	MHz
$t_W$	Pulse duration	CLK high or low	7		6		ns
		CLR or $\overline{PRE}$ low	6.3		5.5		
$t_{su}$	Setup time, before CLK↑	J or $\overline{K}$	7.7		6.8		ns
$t_h$	Hold time, after CLK↑	J or $\overline{K}$	0		0		ns
$t_{rec}$	Recovery time, before CLK↑	CLR↑ or $\overline{PRE}$ ↑	3.5		3.1		ns

## 4.8 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency			100		114	MHz
$t_W$	Pulse duration	CLK high or low	5		4.4		ns
		CLR or $\overline{PRE}$ low	4.5		3.9		
$t_{su}$	Setup time, before CLK↑	J or $\overline{K}$	5.5		4.8		ns
$t_h$	Hold time, after CLK↑	J or $\overline{K}$	0		0		ns
$t_{rec}$	Recovery time, before CLK↑	CLR↑ or $\overline{PRE}$ ↑	2.5		2.2		ns

## 4.9 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 1.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			8		9		MHz
$t_{PLH}$	CLK	Q or $\overline{Q}$		129		117	ns
	CLR or $\overline{PRE}$			153		139	
$t_{PHL}$	CLK	Q or $\overline{Q}$		129		117	ns
	CLR or $\overline{PRE}$			153		139	

## 4.10 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			71		81		MHz
$t_{PLH}$	CLK	Q or $\overline{Q}$	3.6	14.4	3.7	13.1	ns
	CLR or $\overline{PRE}$		4.3	17.1	4.4	15.5	
$t_{PHL}$	CLK	Q or $\overline{Q}$	3.6	14.4	3.7	13.1	ns
	CLR or $\overline{PRE}$		4.3	17.1	4.4	15.5	

## 4.11 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ ,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

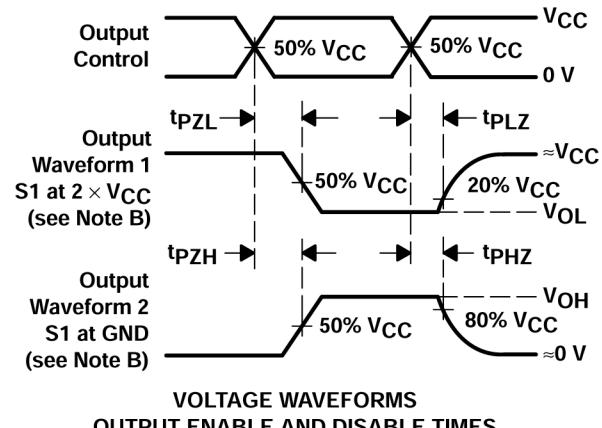
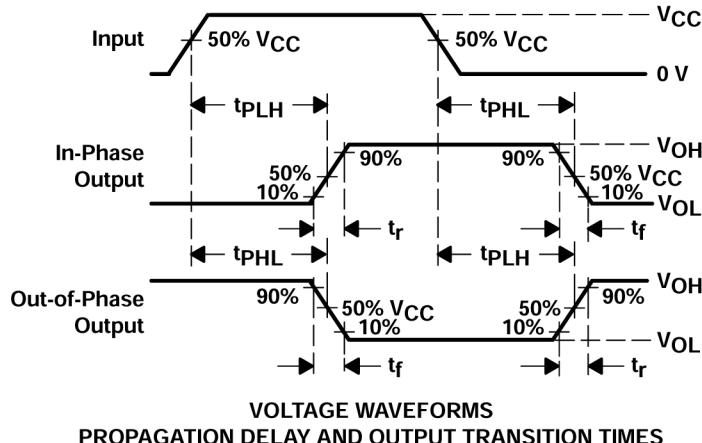
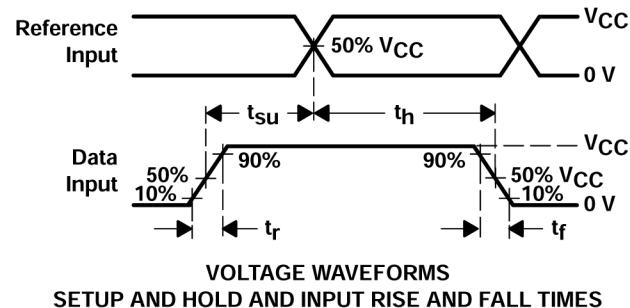
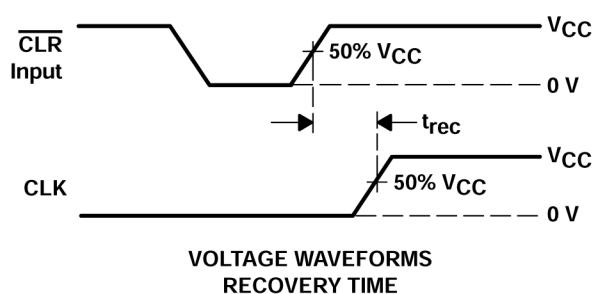
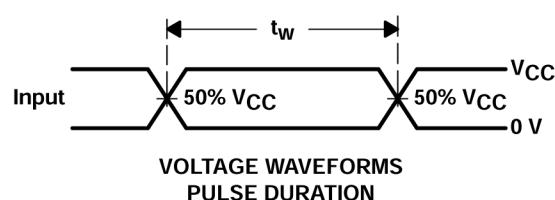
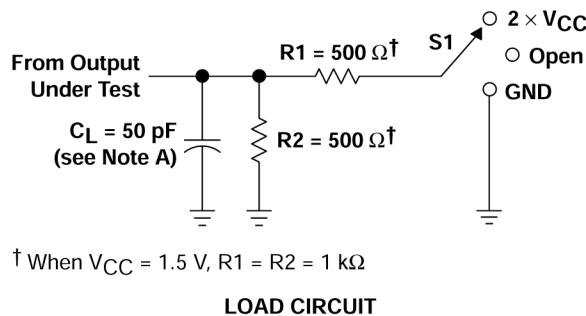
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			100		114		MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$	2.6	10.3	2.7	9.4	ns
	CLR or PRE		3.1	12.2	3.2	11.1	
$t_{PHL}$	CLK	Q or $\bar{Q}$	2.6	10.3	2.7	9.4	ns
	CLR or PRE		3.1	12.2	3.2	11.1	

## 4.12 Operating Characteristics

$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	56	pF

## 5 Parameter Measurement Information



- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
- For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

## 6 Detailed Description

### 6.1 Overview

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the  $\text{J}$  and  $\overline{\text{K}}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock ( $\text{CLK}$ ) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the  $\text{J}$  and  $\overline{\text{K}}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\overline{\text{K}}$  and tying  $\text{J}$  high. They also can perform as D-type flip-flops if  $\text{J}$  and  $\overline{\text{K}}$  are tied together.

### 6.2 Functional Block Diagram

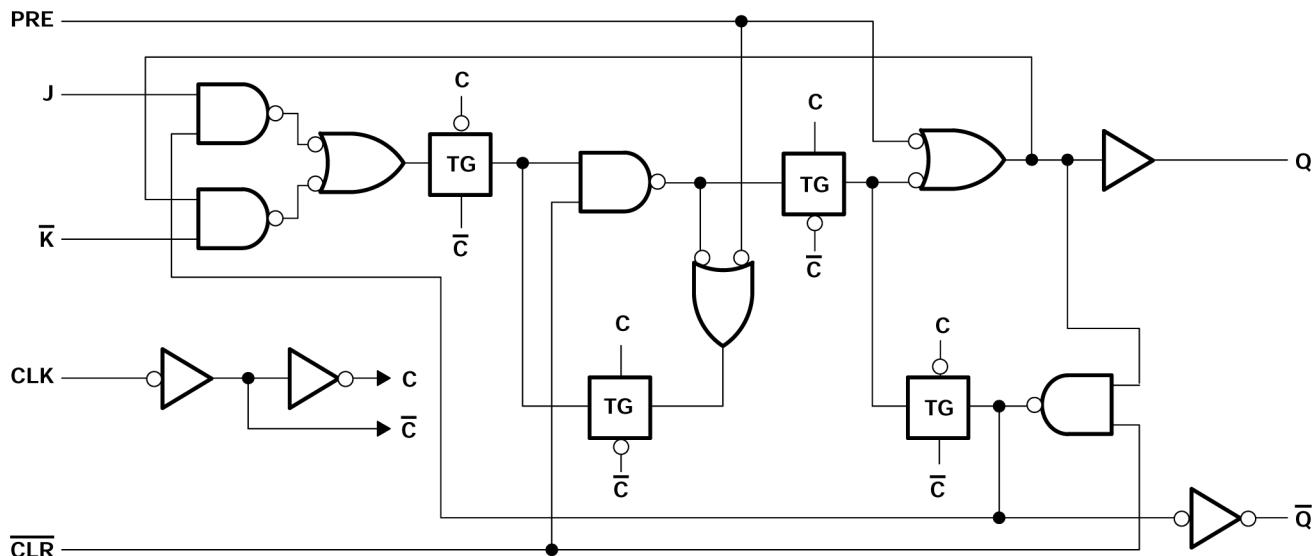


Figure 6-1. Logic Diagram, Each Flip-flop (Positive Logic)

### 6.3 Device Functional Modes

Table 6-1. Function Table (Each Flip-flop)

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	$\text{CLK}$	$\text{J}$	$\overline{\text{K}}$	$\text{Q}$	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{\text{Q}}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

(1) Unpredictable and unstable condition if both  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  go low simultaneously

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

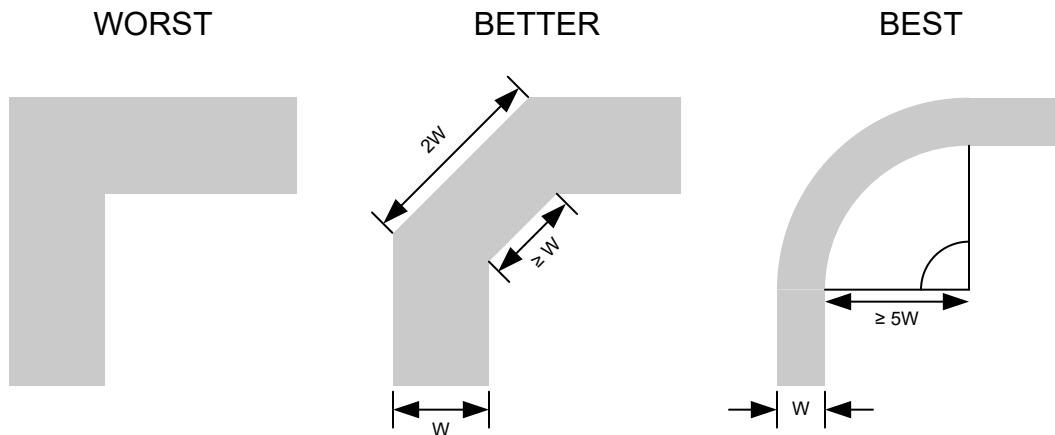
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu F$  and  $1\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

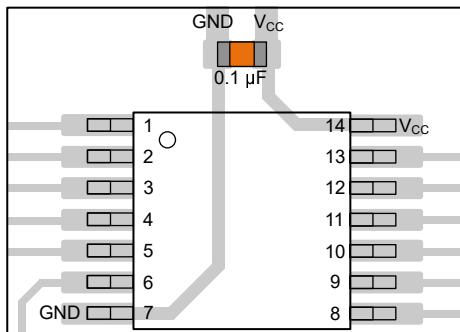
#### 7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

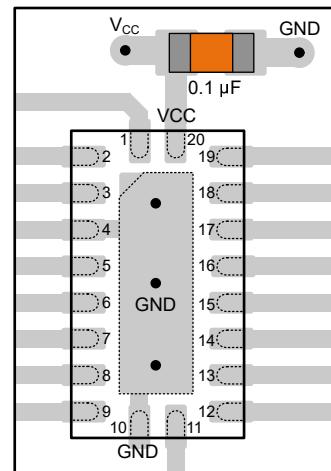
#### 7.2.2 Layout Example



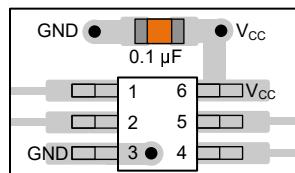
**Figure 7-1. Example Trace Corners for Improved Signal Integrity**



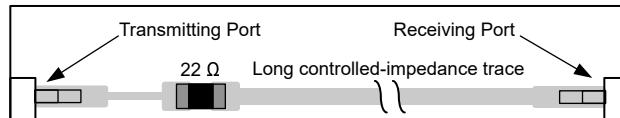
**Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages**



**Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages**



**Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**



**Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#) application report
- Texas Instruments, [Designing With Logic](#) application report
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application report

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2003) to Revision A (December 2024)	Page
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD54AC109F3A</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC109F3A
CD54AC109F3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC109F3A
<a href="#">CD74AC109E</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC109E
CD74AC109E.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC109E
<a href="#">CD74AC109M96</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC109M
CD74AC109M96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC109M

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

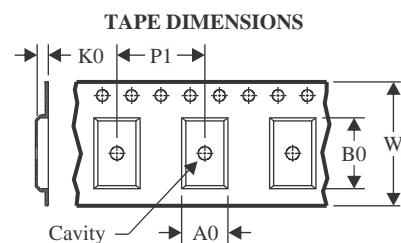
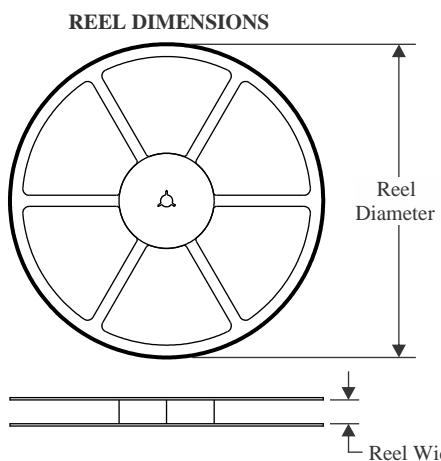
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC109, CD74AC109 :**

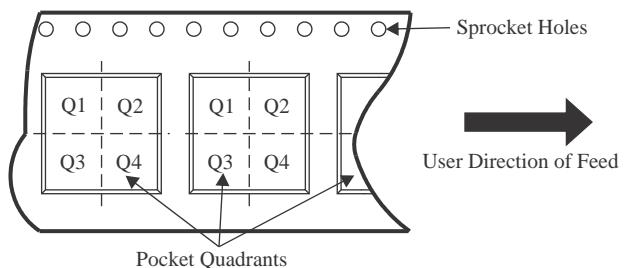
- Catalog : [CD74AC109](#)
- Military : [CD54AC109](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


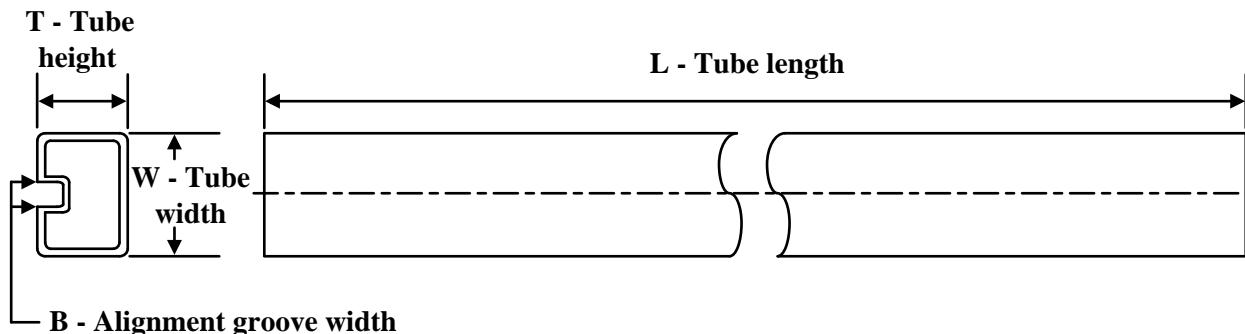
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC109M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC109M96	SOIC	D	16	2500	353.0	353.0	32.0

**TUBE**


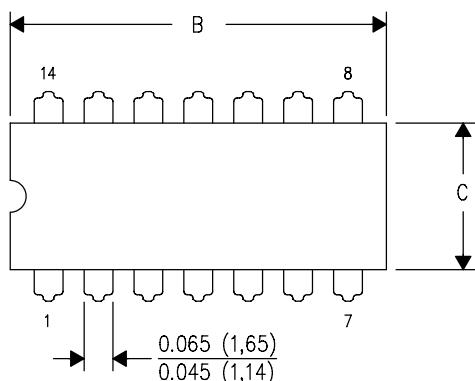
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
CD74AC109E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC109E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC109E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC109E.A	N	PDIP	16	25	506	13.97	11230	4.32

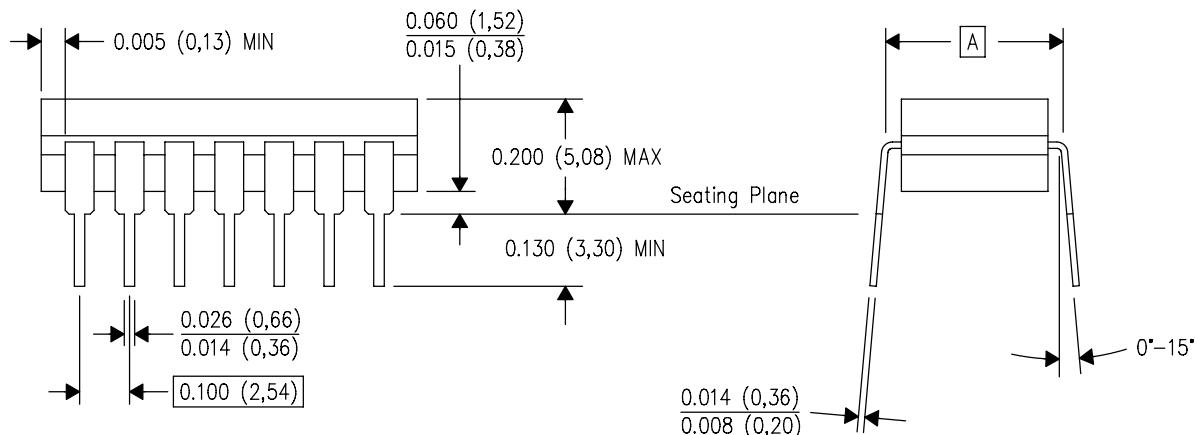
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



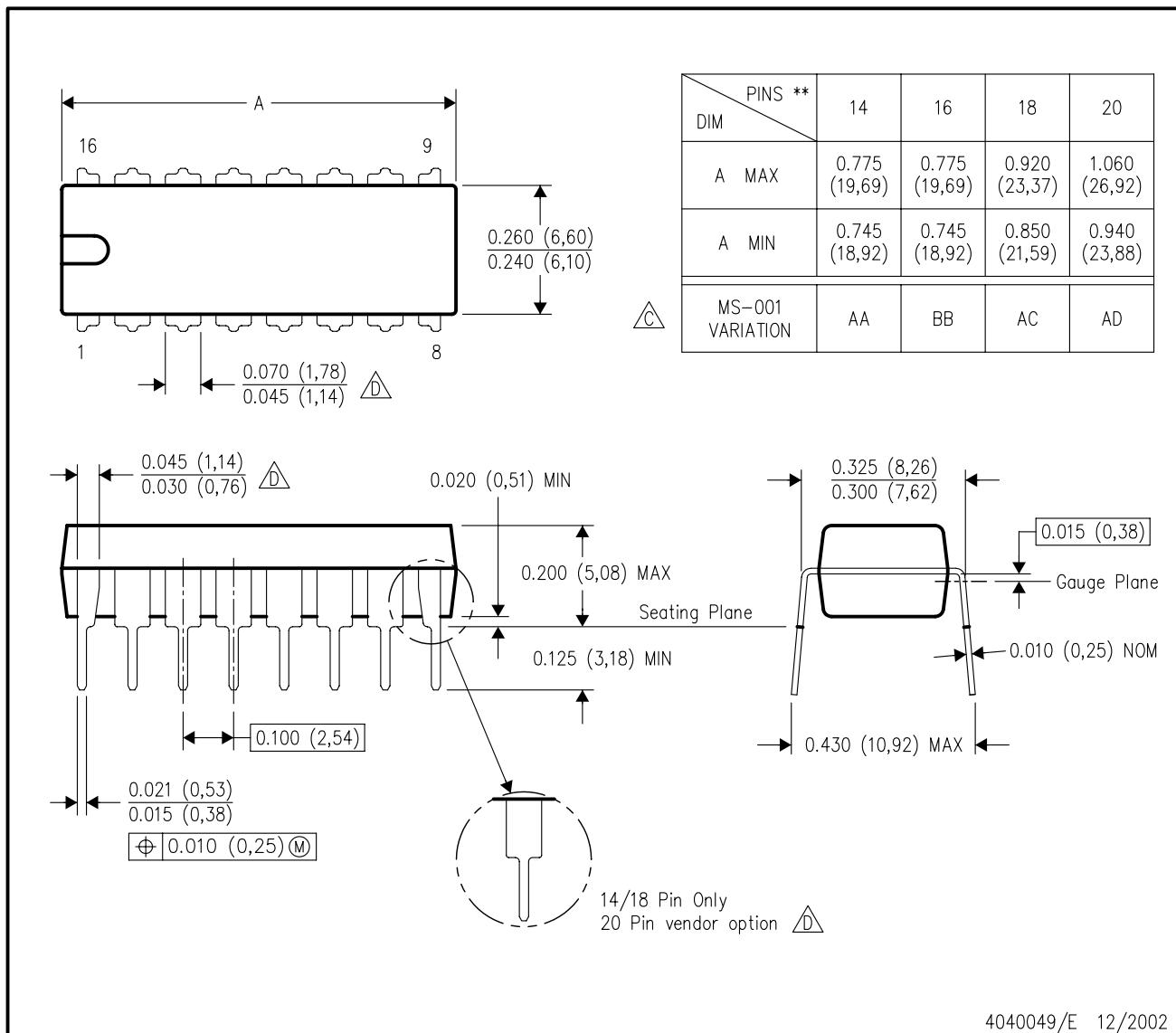
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



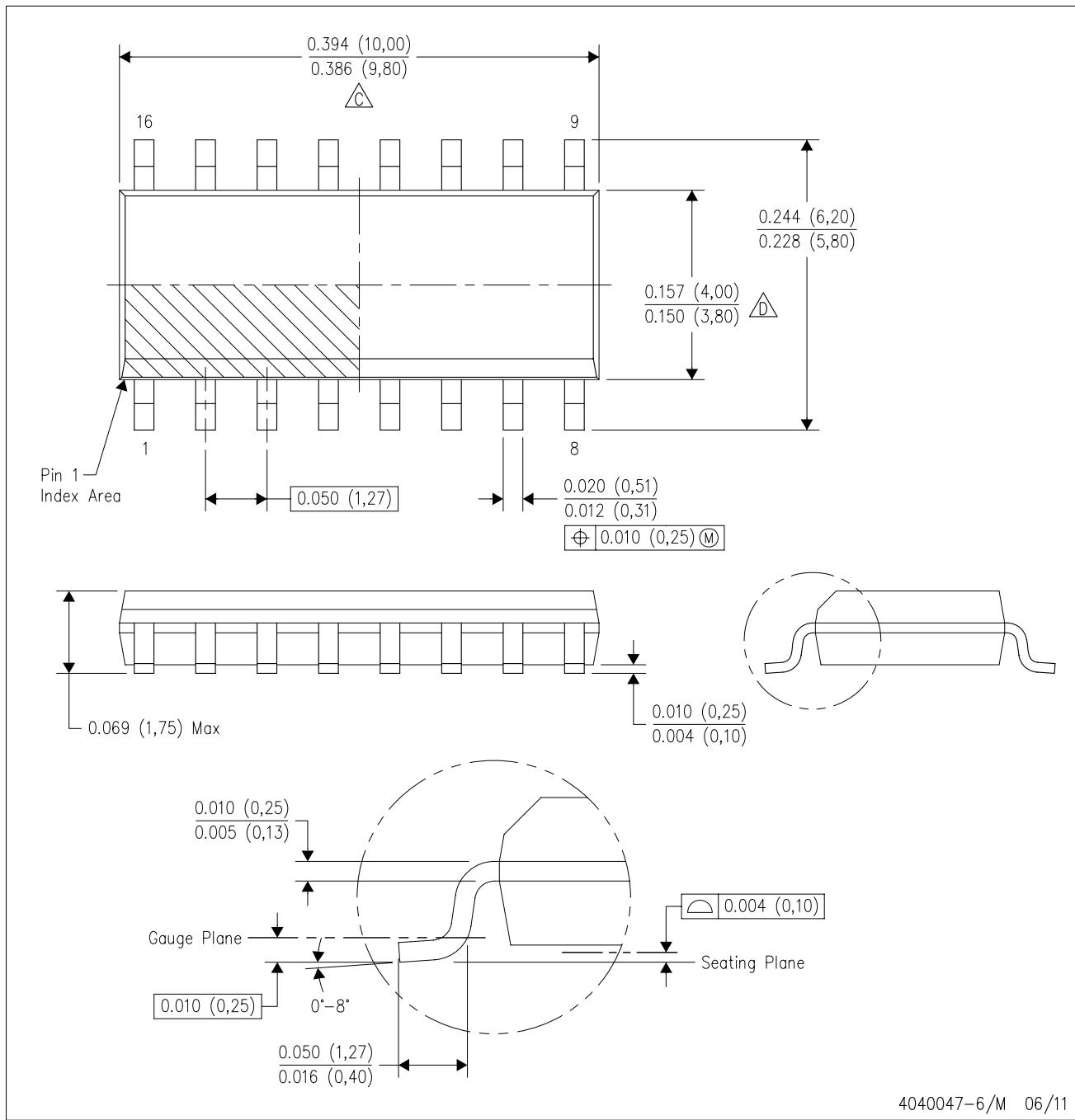
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

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