

# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable

## description/ordering information

The 'AC163 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change, coincident with each other, when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

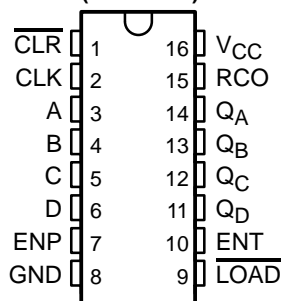
The counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is synchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to  $\overline{\text{CLR}}$  to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15, with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These devices feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

CD54AC163 . . . F PACKAGE  
CD74AC163 . . . E OR M PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74AC163E	CD74AC163E
	SOIC – M	Tube	CD74AC163M	AC163M
		Tape and reel	CD74AC163M96	
	CDIP – F	Tube	CD54AC163F3A	CD54AC163F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

FUNCTION TABLE

INPUTS						OUTPUTS		FUNCTION
CLR	CLK	ENP	ENT	LOAD	A,B,C,D	Q <sub>n</sub>	RCO	
L	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	Note 1	
h	↑	h	h	h	X	Count	Note 1	Count
h	X	l	X	h	X	q <sub>n</sub>	Note 1	Inhibit
h	X	X	l	h	X	q <sub>n</sub>	L	

H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, l = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, and ↑ = CLK low-to-high transition.

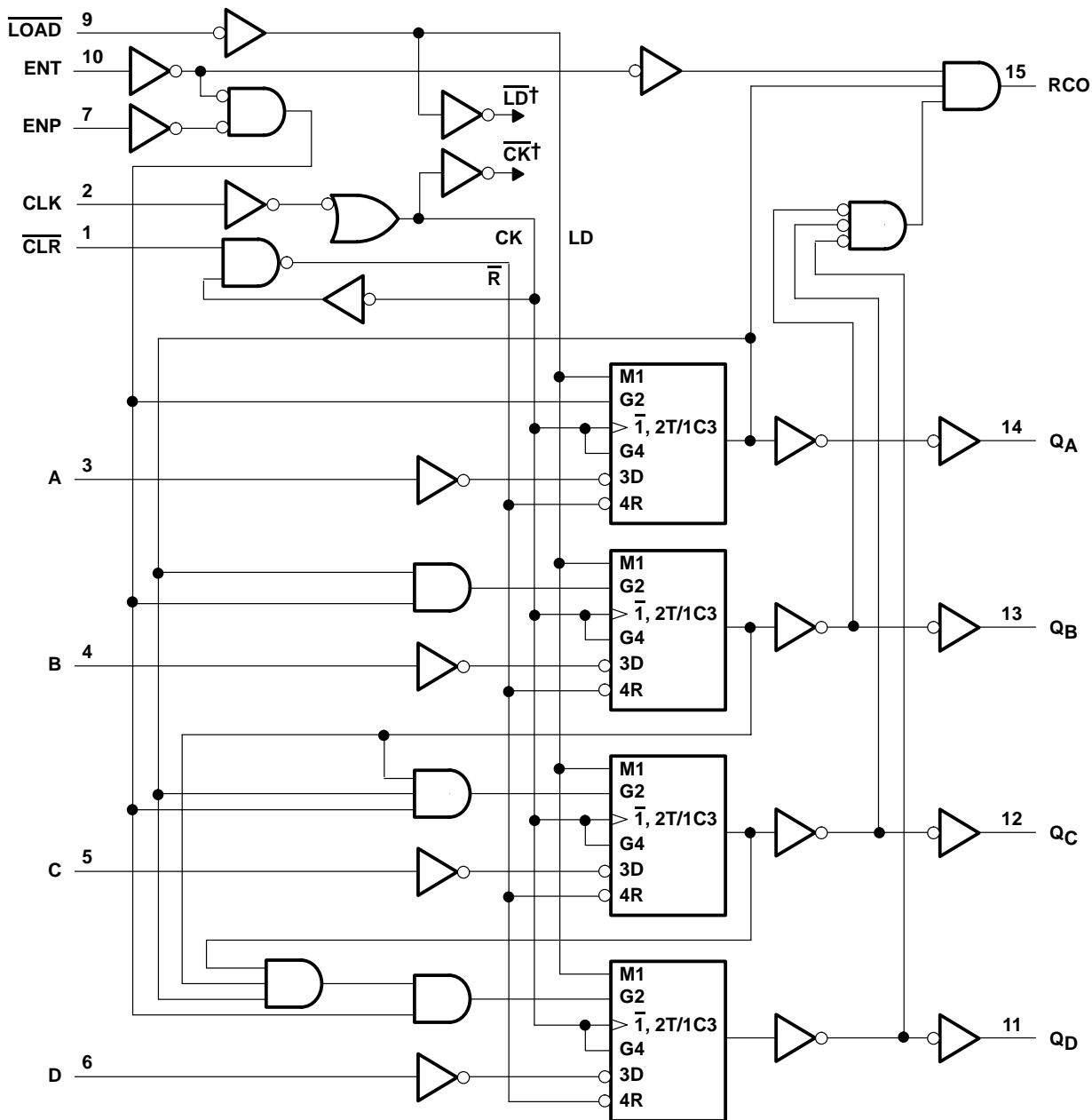
NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).



# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

## logic diagram (positive logic)

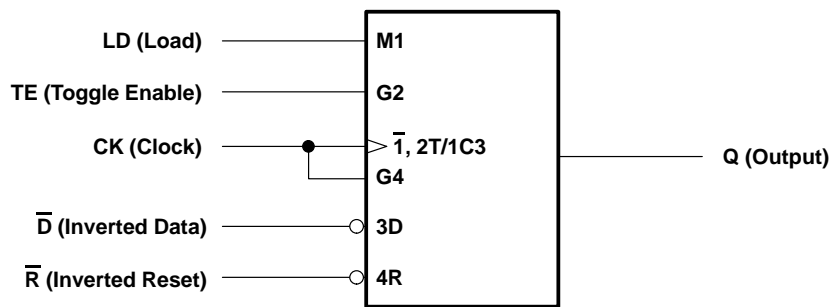


† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

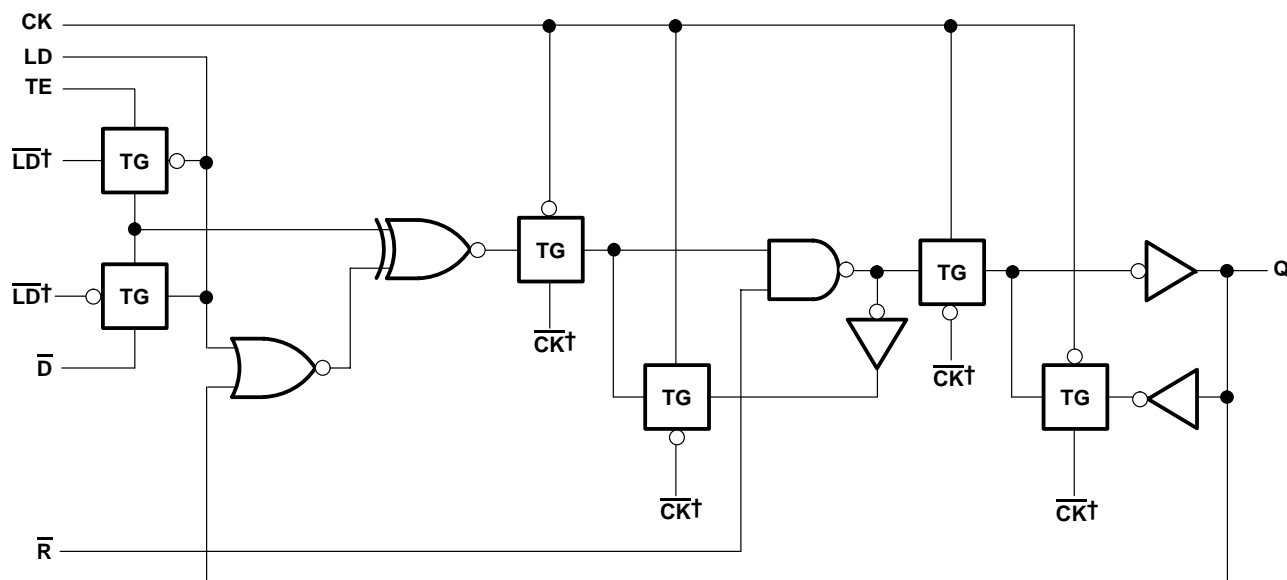
# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

## logic symbol, each D/T flip-flop



## logic diagram, each D/T flip-flop (positive logic)

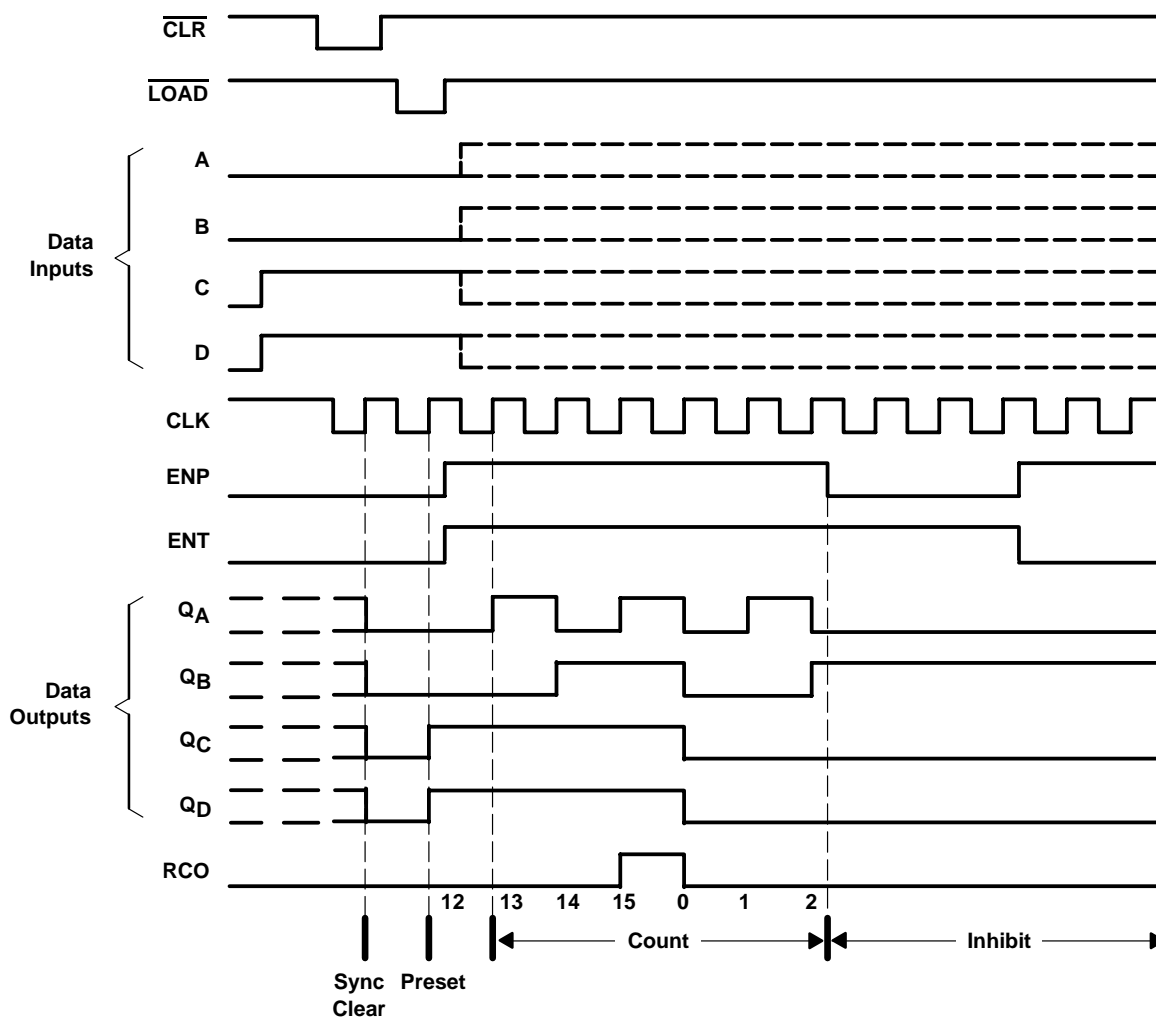


† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

**typical clear, preset, count, and inhibit sequence**

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 2)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 2)	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): E package	67°C/W
M package	73°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.5\text{ V}$		1.2		1.2		V
		$V_{CC} = 3\text{ V}$		2.1		2.1		
		$V_{CC} = 5.5\text{ V}$		3.85		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.5\text{ V}$			0.3		0.3	V
		$V_{CC} = 3\text{ V}$			0.9		0.9	
		$V_{CC} = 5.5\text{ V}$			1.65		1.65	
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24		-24	mA
$I_{OL}$	Low-level output current		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5\text{ V to } 3\text{ V}$		50		50		ns
		$V_{CC} = 3.6\text{ V to } 5.5\text{ V}$		20		20		

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –50 μA	1.5 V	1.4	1.4	1.4			V
			3 V	2.9	2.9	2.9			
			4.5 V	4.4	4.4	4.4			
		I <sub>OH</sub> = –4 mA	3 V	2.58	2.4	2.48			
		I <sub>OH</sub> = –24 mA	4.5 V	3.94	3.7	3.8			
		I <sub>OH</sub> = –50 mA <sup>†</sup>	5.5 V	–	3.85	–			
		I <sub>OH</sub> = –75 mA <sup>†</sup>	5.5 V	–	–	3.85			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	1.5 V	0.1	0.1	0.1			V
			3 V	0.1	0.1	0.1			
			4.5 V	0.1	0.1	0.1			
		I <sub>OL</sub> = 12 mA	3 V	0.36	0.5	0.44			
		I <sub>OL</sub> = 24 mA	4.5 V	0.36	0.5	0.44			
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V	–	1.65	–			
		I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V	–	–	1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1	±1	±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	160	80		μA	
C <sub>i</sub>				10	10	10		pF	

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	1.5 V		7		8	MHz
		3.3 V ± 0.3 V		64		73	
		5 V ± 0.5 V		90		103	
t <sub>w</sub>	Pulse duration	CLK high or low	1.5 V	69	61		ns
			3.3 V ± 0.3 V	7.7	6.8		
			5 V ± 0.5 V	5.5	4.8		
t <sub>su</sub>	A, B, C, or D	1.5 V	63	55		ns	
			3.3 V ± 0.3 V	7	6.1		
			5 V ± 0.5 V	5	4.4		
		ENP or ENT	1.5 V	63	55		
			3.3 V ± 0.3 V	9.6	8.2		
			5 V ± 0.5 V	5	4.4		
	LOAD low	1.5 V	75	66			
		3.3 V ± 0.3 V	8.4	7.4			
		5 V ± 0.5 V	6	5.3			
	CLR inactive	1.5 V	75	66			
		3.3 V ± 0.3 V	8.4	7.4			
		5 V ± 0.5 V	6	5.3			
t <sub>h</sub>	A, B, C, or D	1.5 V	0	0		ns	
			3.3 V ± 0.3 V	0	0		
			5 V ± 0.5 V	0	0		
	ENP or ENT	1.5 V	0	0			
			3.3 V ± 0.3 V	0	0		
			5 V ± 0.5 V	0	0		
	LOAD low	1.5 V	0	0			
			3.3 V ± 0.3 V	0	0		
			5 V ± 0.5 V	0	0		
	CLR inactive	1.5 V	0	0			
			3.3 V ± 0.3 V	0	0		
			5 V ± 0.5 V	0	0		





# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
f <sub>max</sub>			1.5 V	7		8		MHz
			3.3 V ± 0.3 V	64		73		
			5 V ± 0.5 V	90		103		
t <sub>pd</sub>	CLK	RCO	1.5 V	–	209	–	190	ns
			3.3 V ± 0.3 V	6	23.4	6	21	
			5 V ± 0.5 V	4.3	16.7	4.3	15.2	
		Any Q	1.5 V	–	207	–	188	
			3.3 V ± 0.3 V	5.9	23.1	5.9	21	
			5 V ± 0.5 V	4.2	16.5	4.2	15	
	ENT	RCO	1.5 V	–	129	–	117	
			3.3 V ± 0.3 V	3.6	14.4	3.7	13.1	
			5 V ± 0.5 V	2.6	10.3	2.7	9.4	

operating characteristics, T<sub>A</sub> = 25°C

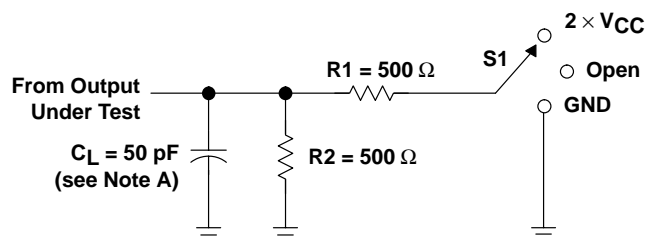
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	66	pF



# CD54AC163, CD74AC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299B – APRIL 2000 – REVISED MARCH 2003

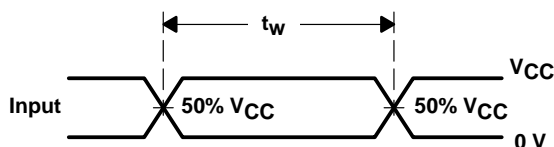
## PARAMETER MEASUREMENT INFORMATION



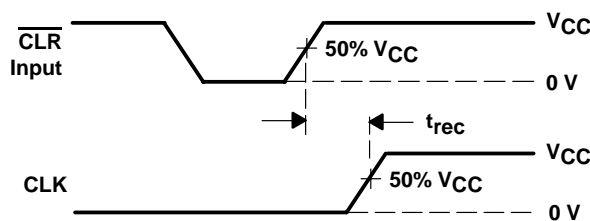
NOTE: When  $V_{CC} = 1.5 \text{ V}$ ,  $R_1$  and  $R_2 = 1 \text{ k}\Omega$ .

LOAD CIRCUIT

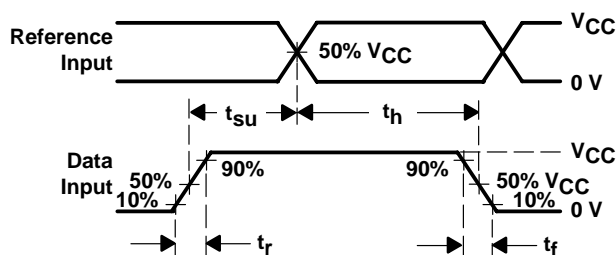
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



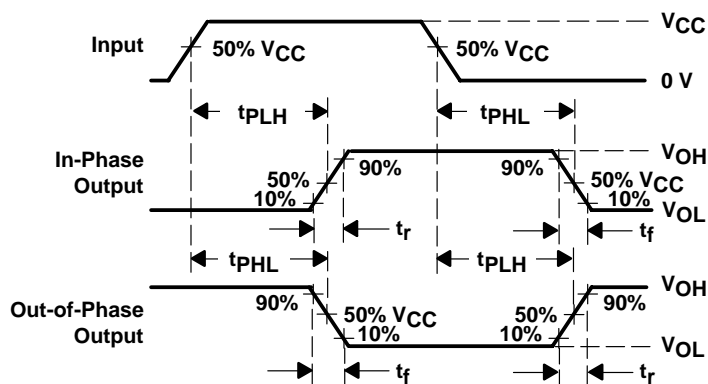
VOLTAGE WAVEFORMS  
PULSE DURATION



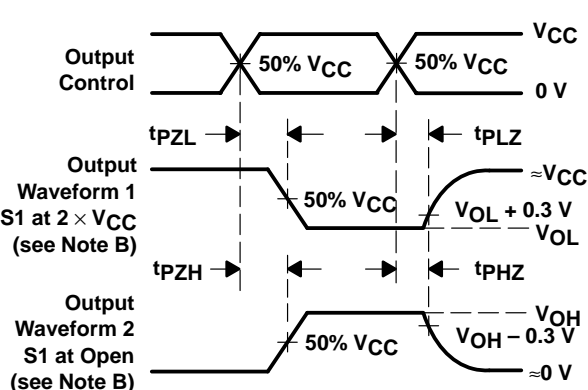
VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC163F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54AC163F3A	<a href="#">Samples</a>
CD74AC163E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC163E	<a href="#">Samples</a>
CD74AC163M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC163M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC163, CD74AC163 :**

- Catalog : [CD74AC163](#)
- Military : [CD54AC163](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC163M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC163M96	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74AC163E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC163E	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated