

# CDx4AC299, CD74AC323, CDx4ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

## 1 Features

### Type Features

- Buffered inputs
- Typical propagation delay:

6ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$

### Family Features

- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- $\pm 24mA$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50ohm transmission lines

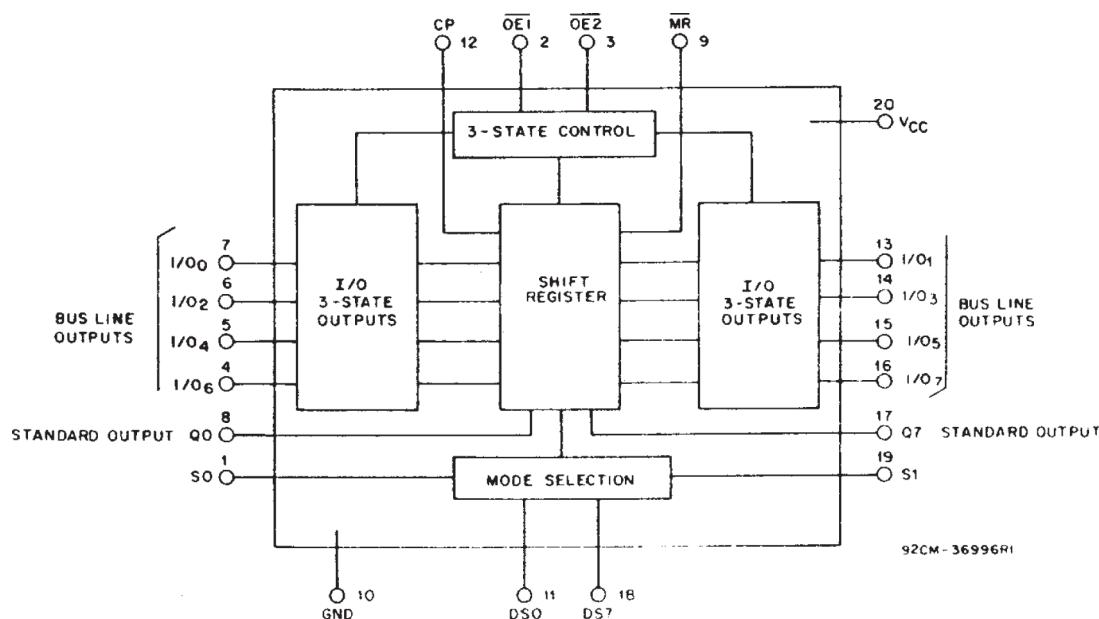
## 2 Description

The RCA CDx4AC299 and CD74AC323 and the CDx4ACT299 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins.

### Device Information

| PART NUMBER                | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|----------------------------|------------------------|-----------------------------|--------------------------|
| CDx4AC(T)299/<br>CD74AC323 | DW (SOIC, 20)          | 12.80mm ×<br>10.3mm         | 12.80mm × 7.50mm         |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



**Functional Diagram**

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



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## 3 Pin Configuration and Functions

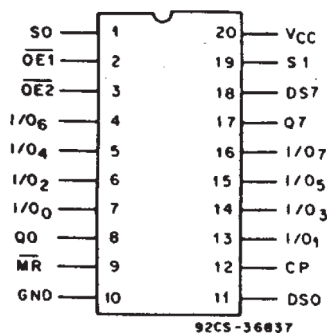


Figure 3-1. Terminal Assignment

### Pin Functions

| PIN |                 | TYPE <sup>1</sup> | DESCRIPTION                  |
|-----|-----------------|-------------------|------------------------------|
| NO. | NAME            |                   |                              |
| 1   | SO              | I                 | Mode select 0                |
| 2   | !OE1            | I                 | Output enable, active low    |
| 3   | !OE2            | I                 | Output enable, active low    |
| 4   | I/O6            | O                 | Parallel data input/output   |
| 5   | I/O4            | O                 | Parallel data input/output   |
| 6   | I/O2            | O                 | Parallel data input/output   |
| 7   | I/O0            | O                 | Parallel data input/output   |
| 8   | Q0              | O                 | Serial output                |
| 9   | !MR             | I                 | Master reset, active low     |
| 10  | GND             | -                 | Ground                       |
| 11  | DSO             | I                 | Serial data input            |
| 12  | CP              | I                 | Clock, rising edge triggered |
| 13  | I/O1            | O                 | Parallel data input/output   |
| 14  | I/O3            | O                 | Parallel data input/output   |
| 15  | I/O5            | O                 | Parallel data input/output   |
| 16  | I/O7            | O                 | Parallel data input/output   |
| 17  | Q7              | O                 | Serial output                |
| 18  | DS7             | I                 | Serial data input            |
| 19  | S1              | I                 | Mode select                  |
| 20  | V <sub>CC</sub> | -                 | Supply                       |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 4 Specifications

### 4.1 Absolute Maximum Ratings

|           |                                                                                                            | MIN  | MAX       | UNIT              |
|-----------|------------------------------------------------------------------------------------------------------------|------|-----------|-------------------|
| $V_{CC}$  | Supply voltage range                                                                                       | -0.5 | 7         | V                 |
| $I_{IK}$  | Input diode current<br>( $V_I < -0.5\text{ V}$ or $V_I > V_{CC} \pm 0.5\text{ V}$ )                        |      | $\pm 20$  | mA                |
| $I_{OK}$  | Output diode current<br>( $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )                         |      | $\pm 50$  | mA                |
| $I_O$     | Output source or sink current per output pin<br>( $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ ) |      | $\pm 50$  | mA                |
|           | $V_{CC}$ or ground current, $I_{CC}$ or $I_{GND}$                                                          |      | $\pm 100$ | mA <sup>(1)</sup> |
| $T_A$     | Operating-temperature range                                                                                | -55  | +125      | °C                |
| $T_{stg}$ | Storage temperature                                                                                        | -65  | +150      | °C                |

(1) For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.

### 4.2 ESD Ratings

|             |                                                                                              | VALUE      | UNIT |
|-------------|----------------------------------------------------------------------------------------------|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge<br>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | $\pm 2000$ | V    |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

|                         |                                                                  | MIN | MAX      | UNIT |
|-------------------------|------------------------------------------------------------------|-----|----------|------|
| $V_{CC}$ <sup>(1)</sup> | Supply-Voltage :<br>(For $T_A$ = Full Package-Temperature Range) |     |          |      |
|                         | AC Types                                                         | 1.5 | 5.5      | V    |
|                         | ACT Types                                                        | 4.5 | 5.5      | V    |
| $V_I, V_O$              | Input or Output voltage                                          | 0   | $V_{CC}$ | V    |
| $T_A$                   | Operating Temperature                                            | -55 | +125     | °C   |
| dt/dv                   | Input Rise and Fall Slew Rate                                    |     |          |      |
|                         | at 1.5 V to 3 V (AC Types)                                       | 0   | 50       | ns/V |
|                         | at 3.6 V to 5.5 V (AC Types)                                     | 0   | 20       | ns/V |
|                         | at 4.5 V to 5.5 V (ACT Types)                                    | 0   | 10       | ns/V |

(1) Unless otherwise specified, all voltages are referenced to ground.

### 4.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | CDx4AC(T)299/<br>CD74AC323             | UNIT |      |
|-------------------------------|----------------------------------------|------|------|
|                               | DW (SOIC, 20)                          |      |      |
|                               | 20 PINS                                |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 40   | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 4.5 Static Electrical Characteristics, AC Series

| CHARACTERISTICS |                               | TEST CONDITIONS                                                               |                     | V <sub>CC</sub> (V) | AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C |      |           |      |             |      | UNIT |
|-----------------|-------------------------------|-------------------------------------------------------------------------------|---------------------|---------------------|--------------------------------------------|------|-----------|------|-------------|------|------|
|                 |                               |                                                                               |                     |                     | +25                                        |      | -40 to+85 |      | -55 to +125 |      |      |
|                 |                               | V <sub>I</sub> (V)                                                            | I <sub>O</sub> (mA) |                     | MIN                                        | MAX  | MIN       | MAX  | MIN         | MAX  |      |
| V <sub>IH</sub> | High-Level Input Voltage      |                                                                               |                     | 1.5                 | 1.2                                        | —    | 1.2       | —    | 1.2         | —    | V    |
|                 |                               |                                                                               |                     | 3                   | 2.1                                        | —    | 2.1       | —    | 2.1         | —    |      |
|                 |                               |                                                                               |                     | 5.5                 | 3.85                                       | —    | 3.85      | —    | 3.85        | —    |      |
| V <sub>IL</sub> | Low-Level Input Voltage       |                                                                               |                     | 1.5                 | —                                          | 0.3  | —         | 0.3  | —           | 0.3  | V    |
|                 |                               |                                                                               |                     | 3                   | —                                          | 0.9  | —         | 0.9  | —           | 0.9  |      |
|                 |                               |                                                                               |                     | 5.5                 | —                                          | 1.65 | —         | 1.65 | —           | 1.65 |      |
| V <sub>OH</sub> | High-Level Output Voltage     | V <sub>IH</sub> or V <sub>IL</sub>                                            | -0.05               | 1.5                 | 1.4                                        | —    | 1.4       | —    | 1.4         | —    | V    |
|                 |                               |                                                                               | -0.05               | 3                   | 2.9                                        | —    | 2.9       | —    | 2.9         | —    |      |
|                 |                               |                                                                               | -0.05               | 4.5                 | 4.4                                        | —    | 4.4       | —    | 4.4         | —    |      |
|                 |                               |                                                                               | -4                  | 3                   | 2.58                                       | —    | 2.48      | —    | 2.4         | —    |      |
|                 |                               |                                                                               | -24                 | 4.5                 | 3.94                                       | —    | 3.8       | —    | 3.7         | —    |      |
|                 |                               | { <sup>(1)</sup> , <sup>(2)</sup>                                             | -75                 | 5.5                 | —                                          | —    | 3.85      | —    | —           | —    |      |
|                 |                               |                                                                               | -50                 | 5.5                 | —                                          | —    | —         | —    | 3.85        | —    |      |
| V <sub>OL</sub> | Low-Level Output Voltage      | V <sub>IH</sub> or V <sub>IL</sub>                                            | 0.05                | 1.5                 | —                                          | 0.1  | —         | 0.1  | —           | 0.1  | V    |
|                 |                               |                                                                               | 0.05                | 3                   | —                                          | 0.1  | —         | 0.1  | —           | 0.1  |      |
|                 |                               |                                                                               | 0.05                | 4.5                 | —                                          | 0.1  | —         | 0.1  | —           | 0.1  |      |
|                 |                               |                                                                               | 12                  | 3                   | —                                          | 0.36 | —         | 0.44 | —           | 0.5  |      |
|                 |                               |                                                                               | 24                  | 4.5                 | —                                          | 0.36 | —         | 0.44 | —           | 0.5  |      |
|                 |                               | { <sup>(1)</sup> , <sup>(2)</sup>                                             | 75                  | 5.5                 | —                                          | —    | —         | 1.65 | —           | —    |      |
|                 |                               |                                                                               | 50                  | 5.5                 | —                                          | —    | —         | —    | —           | 1.65 |      |
| I <sub>I</sub>  | Input Leakage Current         | V <sub>CC</sub> or GND                                                        |                     | 5.5                 | —                                          | ±0.1 | —         | ±1   | —           | ±1   | μA   |
| I <sub>OZ</sub> | 3-Stage Leakage Current       | V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>O</sub> = V <sub>CC</sub> or GND |                     | 5.5                 | —                                          | ±0.5 | —         | ±5   | —           | ±10  | μA   |
| I <sub>ce</sub> | Quiescent Supply Current, MSI | V <sub>CC</sub> or GND                                                        | 0                   | 5.5                 | —                                          | 8    | —         | 80   | —           | 160  | μA   |

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

## 4.6 Static Electrical Characteristics, ACT Series

| CHARACTERISTICS  |                                                   | TEST CONDITIONS                                                             |                     | V <sub>CC</sub> (V) | AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C |      |            |      |             |      | UNIT |
|------------------|---------------------------------------------------|-----------------------------------------------------------------------------|---------------------|---------------------|--------------------------------------------|------|------------|------|-------------|------|------|
|                  |                                                   |                                                                             |                     |                     | +25                                        |      | -40 to +85 |      | -55 to +125 |      |      |
|                  |                                                   | V <sub>I</sub> (V)                                                          | I <sub>O</sub> (mA) |                     | MIN                                        | MAX  | MIN        | MAX  | MIN         | MAX  |      |
| V <sub>IH</sub>  | High-Level Input Voltage                          |                                                                             |                     | 4.5 to 5.5          | 2                                          | —    | 2          | —    | 2           | —    | V    |
| V <sub>IL</sub>  | Low-Level Input Voltage                           |                                                                             |                     | 4.5 to 5.5          | —                                          | 0.8  | —          | 0.8  | —           | 0.8  | V    |
| V <sub>OH</sub>  | High-Level Output Voltage                         | V <sub>IH</sub> or V <sub>IL</sub>                                          | -0.05               | 4.5                 | 4.4                                        | —    | 4.4        | —    | 4.4         | —    | V    |
|                  |                                                   |                                                                             | -24                 | 4.5                 | 3.94                                       | —    | 3.8        | —    | 3.7         | —    |      |
|                  |                                                   | { <sup>(1)</sup> , <sup>(2)</sup>                                           | -75                 | 5.5                 | —                                          | —    | 3.85       | —    | —           | —    |      |
|                  |                                                   |                                                                             | -50                 | 5.5                 | —                                          | —    | —          | —    | 3.85        | —    |      |
| V <sub>OL</sub>  | Low-Level Output Voltage                          | V <sub>IH</sub> or V <sub>IL</sub>                                          | 0.05                | 4.5                 | —                                          | 0.1  | —          | 0.1  | —           | 0.1  | V    |
|                  |                                                   |                                                                             | 24                  | 4.5                 | —                                          | 0.36 | —          | 0.44 | —           | 0.5  |      |
|                  |                                                   | { <sup>(1)</sup> , <sup>(2)</sup>                                           | 75                  | 5.5                 | —                                          | —    | —          | 1.65 | —           | —    |      |
|                  |                                                   |                                                                             | 50                  | 5.5                 | —                                          | —    | —          | —    | —           | 1.65 |      |
| I <sub>I</sub>   | Input Leakage Current                             | V <sub>CC</sub> or GND                                                      |                     | 5.5                 | —                                          | ±0.1 | —          | ±1   | —           | ±1   | μA   |
| I <sub>OZ</sub>  | 3-State Leakage Current                           | V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>O</sub> V <sub>CC</sub> or GND |                     | 5.5                 | —                                          | ±0.5 | —          | ±5   | —           | ±10  | μA   |
| I <sub>CC</sub>  | Quiescent Supply Current, MSI                     | V <sub>CC</sub> or GND                                                      | 0                   | 5.5                 | —                                          | 8    | —          | 80   | —           | 160  | μA   |
|                  | Additional Quiescent Supply Current per Input Pin | V <sub>CC</sub> -2.1                                                        |                     | 4.5 to 5.5          | —                                          | 2.4  | —          | 2.8  | —           | 3    | mA   |
| ΔI <sub>CC</sub> | TTL Inputs High                                   |                                                                             |                     |                     |                                            |      |            |      |             |      |      |
|                  | 1 Unit Load                                       |                                                                             |                     |                     |                                            |      |            |      |             |      |      |

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**Table 4-1. Act Input Loading Table**

| INPUT                                              | UNIT LOADS <sup>(1)</sup> |      |
|----------------------------------------------------|---------------------------|------|
|                                                    | 299                       | 323  |
| S1.S0, OE1, OE2                                    | 0.83                      | 0.83 |
| I/O <sub>0</sub> - I/O <sub>7</sub> , CP, DS0, DS7 | 0.67                      | 0.67 |
| MR                                                 | 1.33                      | 0.67 |

(1) Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

## 4.7 Switching Characteristics, AC Series

 $t_r, t_f = 3 \text{ ns}, C_L = 50 \text{ pF}$ 

| SYMBOL                                                                    | CHARACTERISTICS                      | V <sub>CC</sub> (V)                           | AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C |                     |                 |                     | UNIT |
|---------------------------------------------------------------------------|--------------------------------------|-----------------------------------------------|--------------------------------------------|---------------------|-----------------|---------------------|------|
|                                                                           |                                      |                                               | -40 to +85                                 |                     | -55 to +125     |                     |      |
|                                                                           |                                      |                                               | MIN                                        | MAX                 | MIN             | MAX                 |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub>                                      | Propagation Delays: CP to Q0, Q7     | 1.5<br>3.3 <sup>(1)</sup><br>5 <sup>(2)</sup> | —<br>4.7<br>3.3                            | 147<br>16.5<br>11.7 | —<br>4.5<br>3.2 | 162<br>18.1<br>12.9 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub>                                      | CP to (I/O)n                         | 1.5<br>3.3<br>5                               | —<br>4.9<br>3.5                            | 154<br>17.2<br>12.3 | —<br>4.7<br>3.4 | 169<br>18.9<br>13.5 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub>                                      | $\overline{MR}$ to Q0, Q7 (299 only) | 1.5<br>3.3<br>5                               | —<br>4<br>2.9                              | 127<br>14.3<br>10.2 | —<br>3.9<br>2.8 | 140<br>15.7<br>11.2 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub>                                      | $\overline{MR}$ to (I/O)n            | 1.5<br>3.3<br>5                               | —<br>5<br>3.6                              | 158<br>17.7<br>12.6 | —<br>4.9<br>3.5 | 174<br>19.5<br>13.9 | ns   |
| t <sub>PZL</sub><br>t <sub>PZH</sub><br>t <sub>PLZ</sub> t <sub>PHZ</sub> | Enable and Disable Times             | 1.5<br>3.3<br>5                               | —<br>5.8<br>3.8                            | 169<br>20.4<br>13.5 | —<br>5.6<br>3.7 | 186<br>22.4<br>14.9 | ns   |
| C <sub>pd</sub> <sup>(3)</sup>                                            | Power Dissipation Capacitance        | —                                             | 280 Typ.                                   |                     | 280 Typ.        |                     | pF   |
| C <sub>I</sub>                                                            | Input Capacitance                    | —                                             | —                                          | 10                  | —               | 10                  | pF   |
| C <sub>O</sub>                                                            | 3-State Output Capacitance           | —                                             | —                                          | 15                  | —               | 15                  | pF   |

(1) 3.3 V: min. is @ 3.6 V

(2) 5 V: min. is @ 5.5 V

(3)  $C_{pd}$  is used to determine the dynamic power consumption, per function.

## 4.8 Switching Characteristics, ACT Series

 $t_r, t_f = 3 \text{ ns}, C_L = 50 \text{ pF}$ 

| SYMBOL                                                                 | CHARACTERISTICS                  | V <sub>CC</sub> (V) | AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C |      |             |      | UNIT |
|------------------------------------------------------------------------|----------------------------------|---------------------|--------------------------------------------|------|-------------|------|------|
|                                                                        |                                  |                     | -40 to +85                                 |      | -55 to +125 |      |      |
|                                                                        |                                  |                     | MIN                                        | MAX  | MIN         | MAX  |      |
| t <sub>PLH</sub> t <sub>PHL</sub>                                      | Propagation Delays: CP to Q0, Q7 | 5 <sup>(1)</sup>    | 3.3                                        | 11.7 | 3.2         | 12.9 | ns   |
| t <sub>PLH</sub> t <sub>PHL</sub>                                      | CP to (I/O)n                     | 5                   | 3.7                                        | 13.2 | 3.6         | 14.5 | ns   |
| t <sub>PLH</sub> t <sub>PHL</sub>                                      | MR to Q0, Q7 (299 only)          | 5                   | 3.1                                        | 11.1 | 3.1         | 12.2 | ns   |
| t <sub>PLH</sub> t <sub>PHL</sub>                                      | MR to (I/O)n                     | 5                   | 4.8                                        | 16.9 | 4.7         | 18.6 | ns   |
| t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub><br>t <sub>PZH</sub> | Enable and Disable Times         | 5                   | 3.8                                        | 13.5 | 3.7         | 14.9 | ns   |
| C <sub>PD</sub> §                                                      | Power Dissipation Capacitance    | —                   | 280 Typ.                                   |      | 280 Typ.    |      | pF   |
| C <sub>I</sub>                                                         | Input Capacitance                | —                   | — 10                                       |      | — 10        |      | pF   |
| C <sub>O</sub>                                                         | 3-State Output Capacitance       | —                   | — 15                                       |      | — 15        |      | pF   |

(1) 5 V: min. is @ 5.5 V

## 5 Parameter Measurement Information

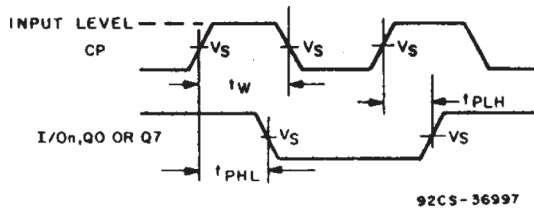


Figure 5-1. Clock Prerequisite and Propagation Delays

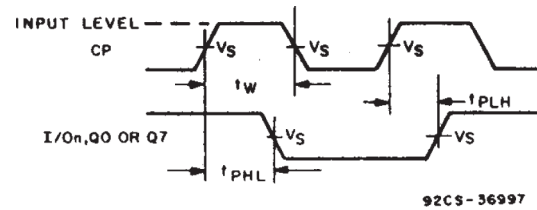


Figure 5-2. Clock Prerequisite and Propagation Delays

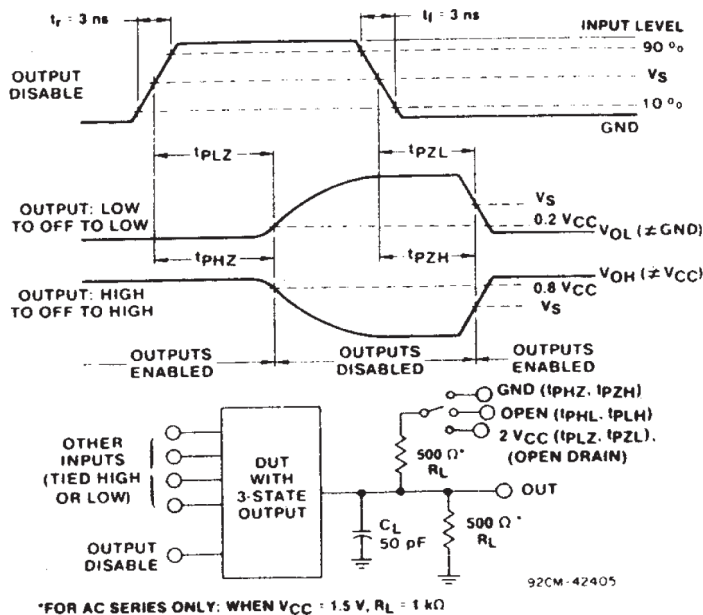


Figure 5-3. Three-state Propagation Delay Times and Test Circuit

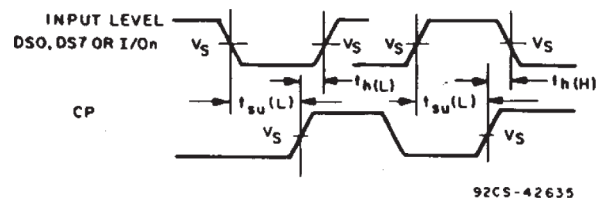


Figure 5-4. Data Prerequisite Times

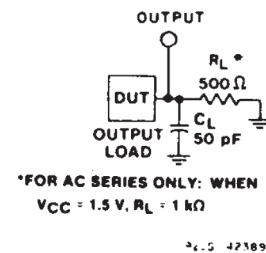


Figure 5-5. Test Circuit

|                                 | CD54/74AC    | CD54/74ACT   |
|---------------------------------|--------------|--------------|
| Input Level                     | $V_{CC}$     | 3 V          |
| Input Switching Voltage, $V_S$  | $0.5 V_{CC}$ | 1.5 V        |
| Output Switching Voltage, $V_S$ | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

## 6 Detailed Description

### 6.1 Overview

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O<sub>0</sub> - I/O<sub>7</sub>) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ( $\overline{MR}$ ) is an asynchronous active-LOW input. When  $\overline{MR}$  is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset ( $\overline{MR}$ ) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ( $\overline{OE1}$  and  $\overline{OE2}$ ) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of  $\overline{OE1}$  and  $\overline{OE2}$ .
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

### 6.2 Functional Block Diagram

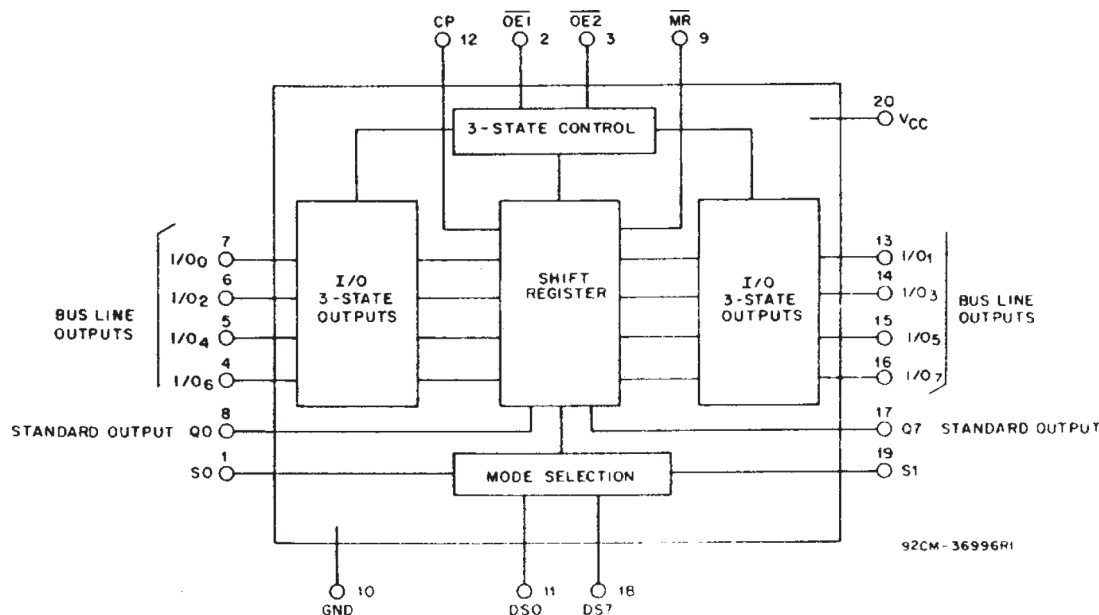


Figure 6-1. Functional Diagram

### 6.3 Device Functional Modes

| FUNCTION          | INPUTS |                                                                                   |    |    |     |     |                  | REGISTER OUTPUTS |                |     |                |                |
|-------------------|--------|-----------------------------------------------------------------------------------|----|----|-----|-----|------------------|------------------|----------------|-----|----------------|----------------|
|                   | MR     | CP                                                                                | S0 | S1 | DS0 | DS7 | I/O <sub>n</sub> | Q0               | Q1             | ... | Q6             | Q7             |
| Reset (Clear)     | L      | X <sup>(1)</sup>                                                                  | X  | X  | X   | X   | X                | L                | L              | ... | L              | L              |
| Shift Right       | H      |  | h  | l  | l   | X   | X                | L                | q <sub>0</sub> | ... | q <sub>5</sub> | q <sub>6</sub> |
|                   | H      |  | h  | l  | h   | X   | X                | H                | q <sub>0</sub> | ... | q <sub>5</sub> | q <sub>6</sub> |
| Shift Left        | H      |  | l  | h  | X   | l   | X                | q <sub>1</sub>   | q <sub>2</sub> | ... | q <sub>7</sub> | L              |
|                   | H      |  | l  | h  | X   | h   | X                | q <sub>1</sub>   | q <sub>2</sub> | ... | q <sub>7</sub> | H              |
| Hold (do nothing) | H      |  | l  | l  | X   | X   | X                | q <sub>0</sub>   | q <sub>1</sub> | ... | q <sub>6</sub> | q <sub>7</sub> |
| Parallel Load     | H      |  | h  | h  | X   | X   | l                | L                | L              | ... | L              | L              |
|                   | H      |  | h  | h  | X   | X   | h                | H                | H              | ... | H              | H              |

**Table 6-1. Mode Select**

Function table 3-state I/O port operating mode

| FUNCTION      | INPUTS |     |    |    |                       | INPUTS/OUTPUTS                    |
|---------------|--------|-----|----|----|-----------------------|-----------------------------------|
|               | OE1    | OE2 | S0 | S1 | Qn (Register)         | I/O <sub>0</sub> I/O <sub>7</sub> |
| Read Register | L      | L   | L  | X  | L                     | L                                 |
|               | L      | L   | L  | X  | H                     | H                                 |
|               | L      | L   | X  | L  | L                     | L                                 |
|               | L      | L   | X  | L  | H                     | H                                 |
| Load Register | X      | X   | H  | H  | Qn = I/O <sub>n</sub> | I/O <sub>n</sub> = Inputs         |
| Disable I/O   | H      | X   | X  | X  | X                     | (Z)                               |
|               | X      | H   | X  | X  | X                     | (Z)                               |

(1) H = Input voltage high level.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1  $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

#### 7.2.2 Layout Example

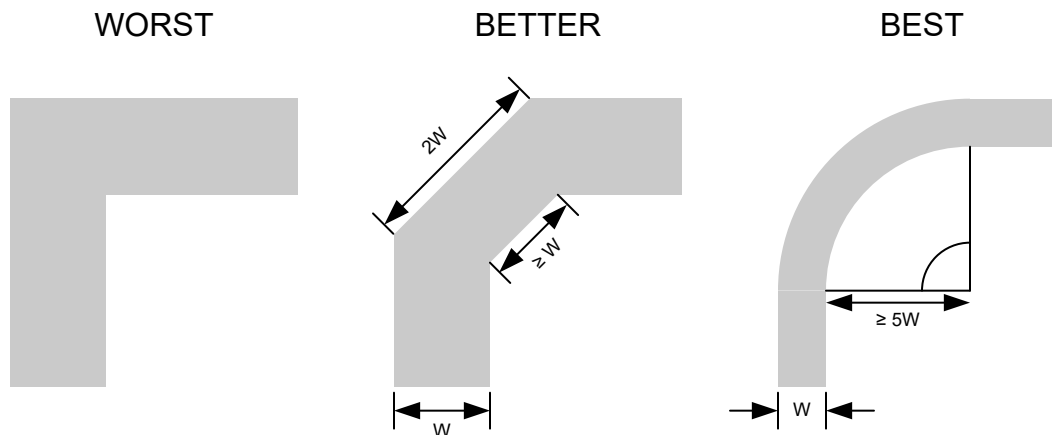


Figure 7-1. Example Trace Corners for Improved Signal Integrity

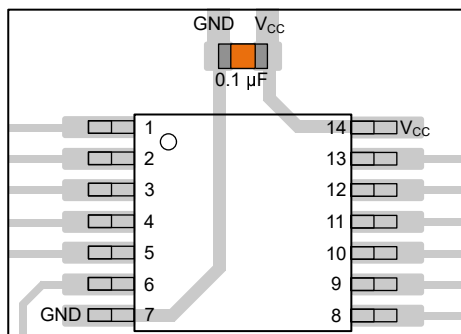


**Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

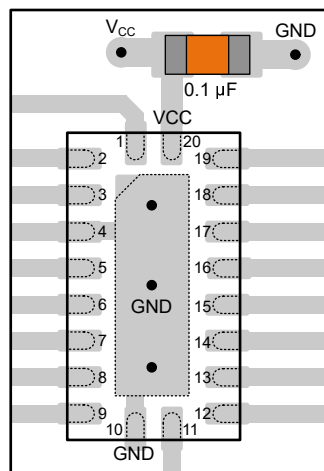


**Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages**

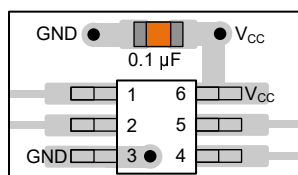


**Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

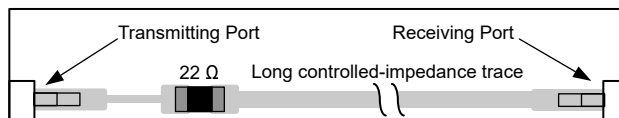


**Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity**

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54AC299  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74AC299  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD54ACT299 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74ACT299 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74AC323  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (April 2002) to Revision A (December 2024)                                                                                                                                                                                                                                                                                                       | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD54AC299F3A</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC299F3A        |
| CD54AC299F3A.A                | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC299F3A        |
| <a href="#">CD54ACT299F3A</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT299F3A       |
| CD54ACT299F3A.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT299F3A       |
| <a href="#">CD74AC299M96</a>  | Last Time Buy | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC299M              |
| CD74AC299M96.A                | Last Time Buy | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC299M              |
| <a href="#">CD74AC323M</a>    | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC323M              |
| CD74AC323M.A                  | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC323M              |
| <a href="#">CD74ACT299M96</a> | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | ACT299M             |
| CD74ACT299M96.A               | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | ACT299M             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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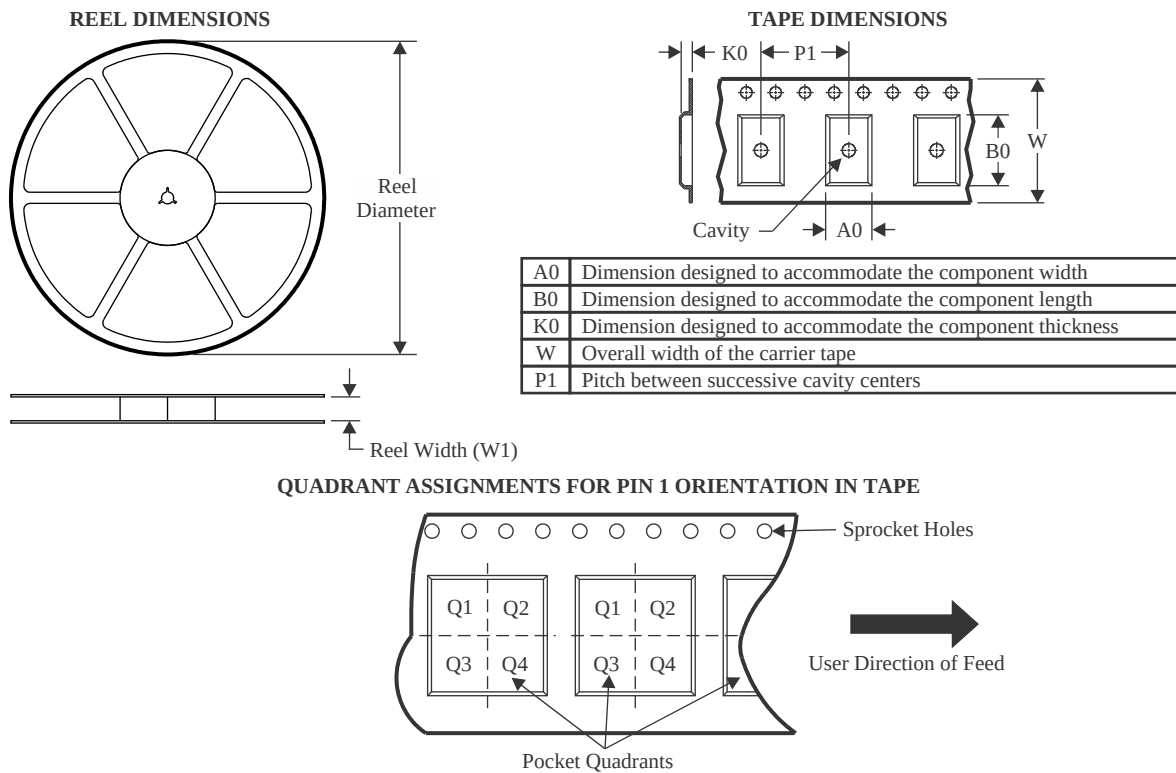
**OTHER QUALIFIED VERSIONS OF CD54AC299, CD54ACT299, CD74AC299, CD74ACT299 :**

- Catalog : [CD74AC299](#), [CD74ACT299](#)
- Military : [CD54AC299](#), [CD54ACT299](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

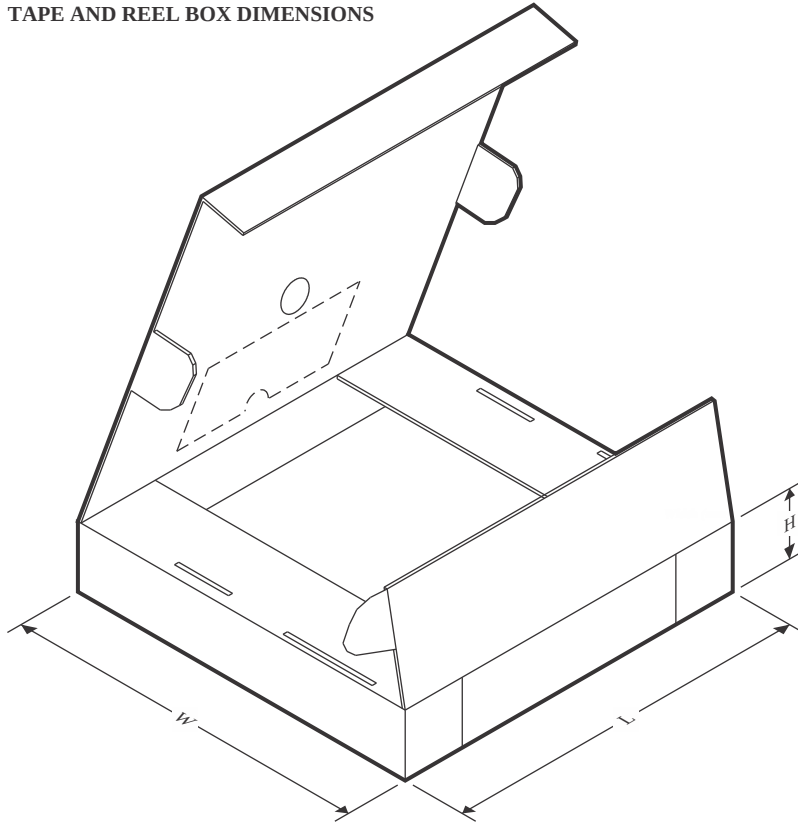
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC299M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74ACT299M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

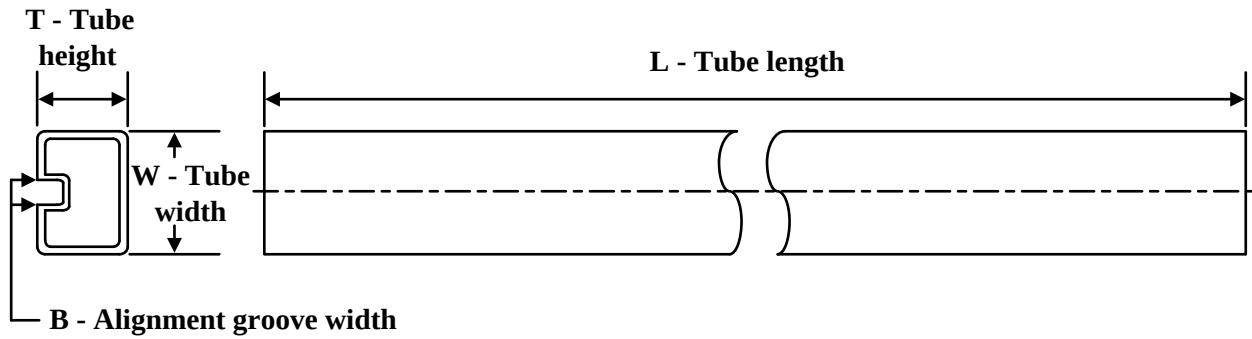
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC299M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74ACT299M96 | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

## TUBE



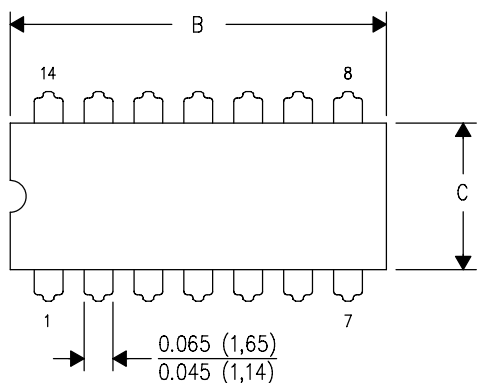
\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74AC323M   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| CD74AC323M.A | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |

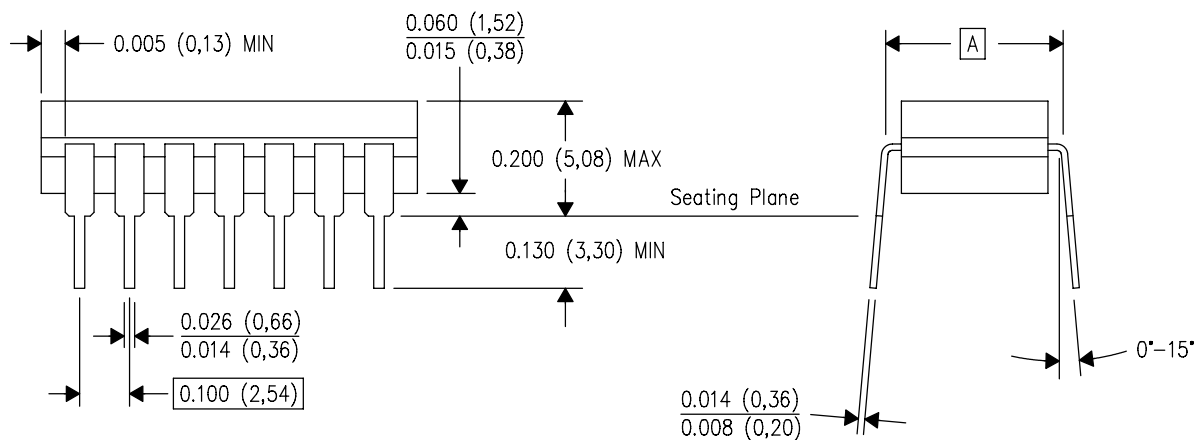
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE

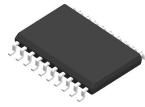
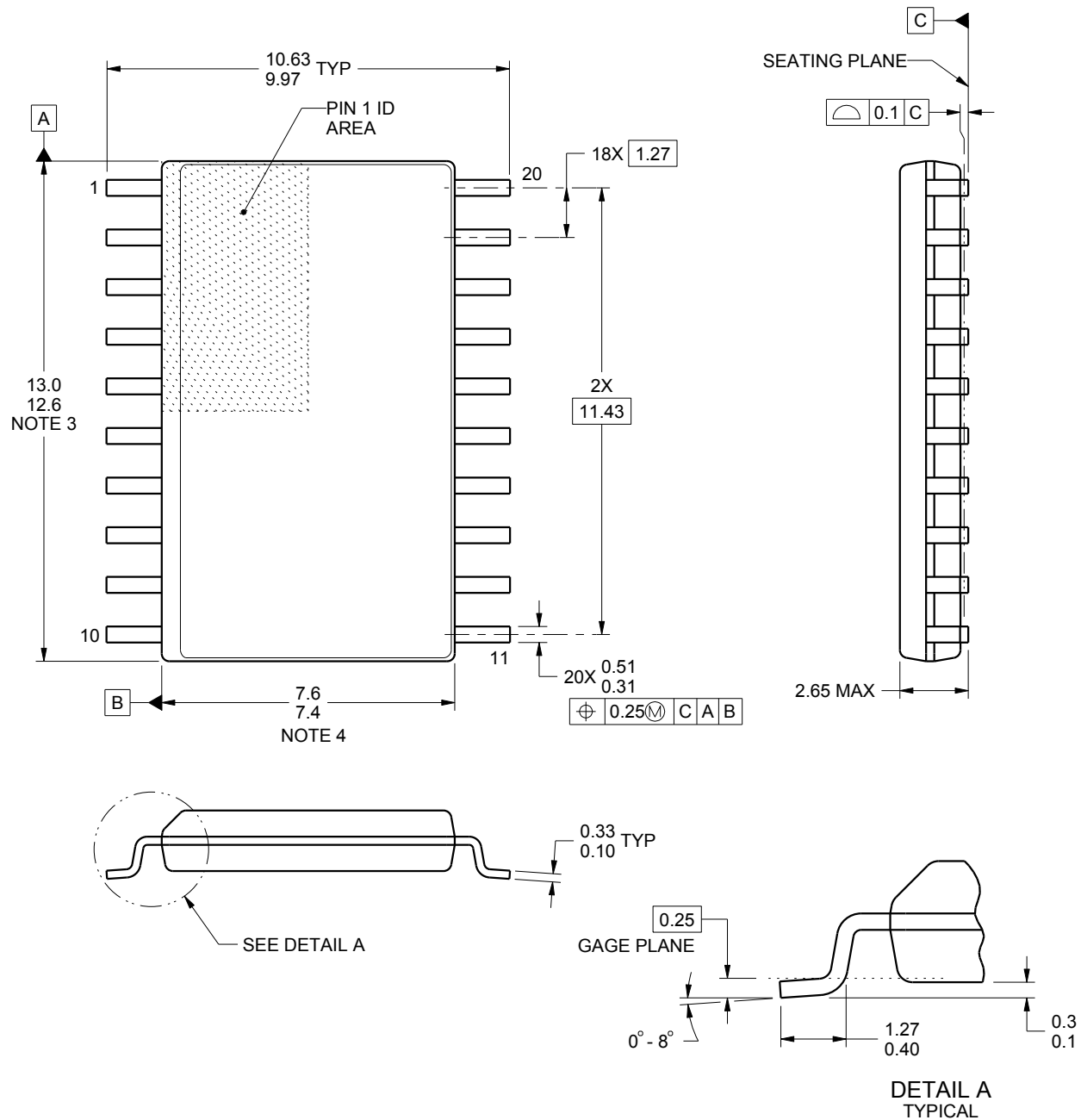


| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220724/A 05/2016

## NOTES:

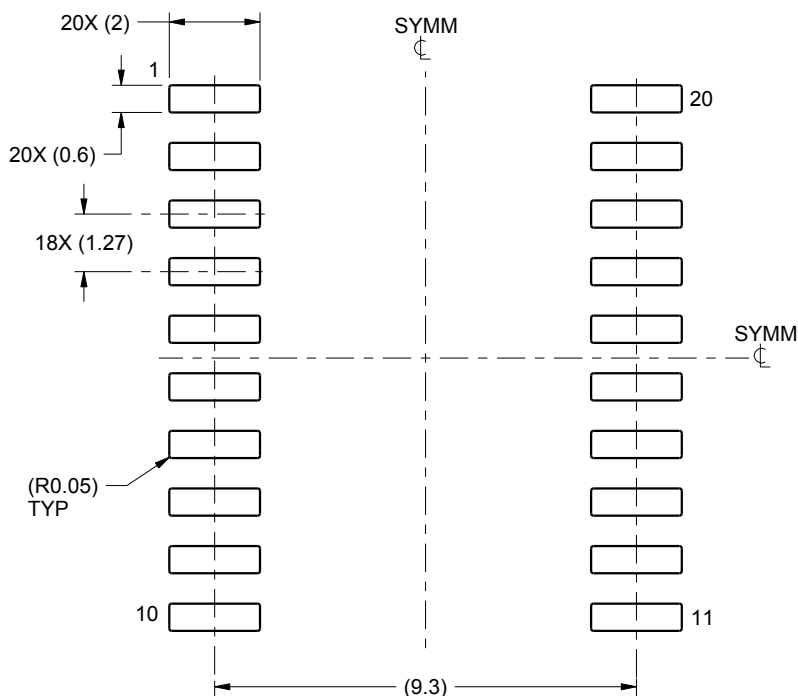
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

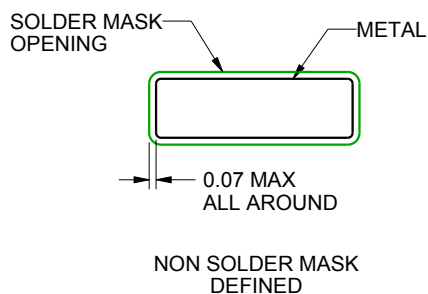
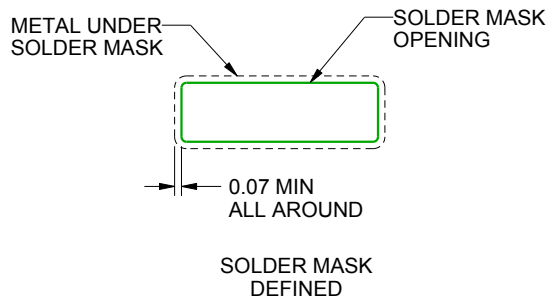
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

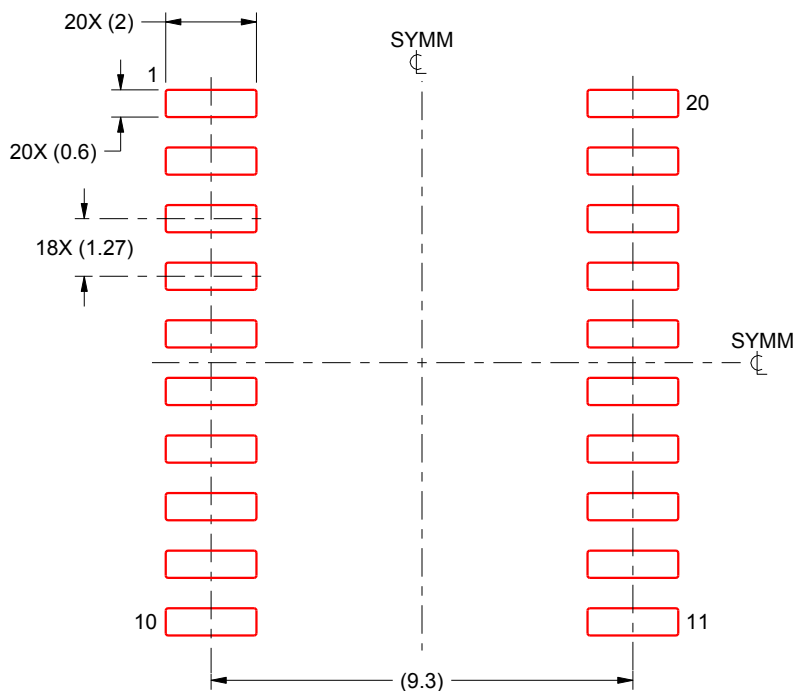
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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