

# CDx4HC534, CDx4HCT534, CDx4HC564, CDx4HCT564 High-Speed CMOS Logic Octal D-Type Flip-Flop, Three-State Inverting Positive-Edge Triggered

## 1 Features

- Buffered inputs
- Common three-state output-enable control
- Three-state outputs
- Bus line driving capability
- Typical propagation delay = 13 ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (clock to output)
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range:  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V}$  (max),  $V_{IH} = 2\text{ V}$  (min)
  - CMOS input compatibility,  $I_I \leq 1\text{ }\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

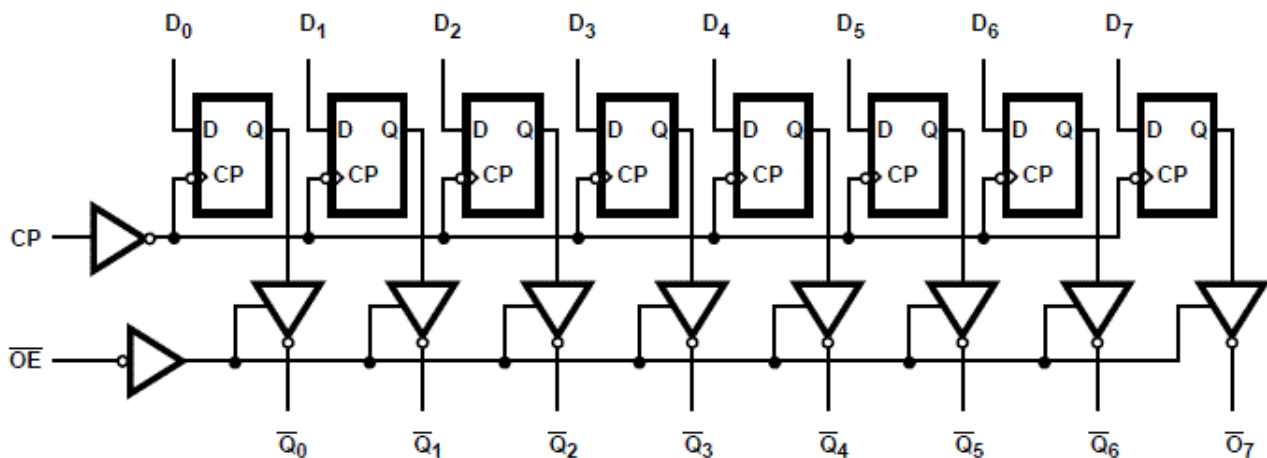
## 2 Description

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are high speed Octal D-Type Flip-Flops manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the three-state feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD74HC564M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT564M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC534E	PDIP (20)	25.40 mm × 6.35 mm
CD74HC564E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT534E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT564E	PDIP (20)	25.40 mm × 6.35 mm
CD54HC534F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT534F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT564F3A	CDIP (20)	26.92 mm × 6.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet



Functional Diagram

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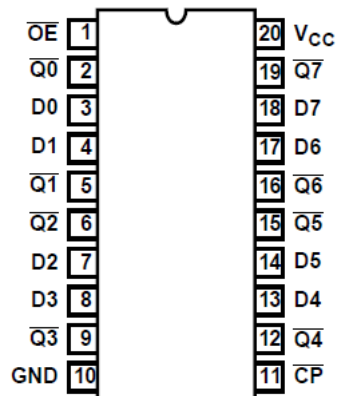
### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

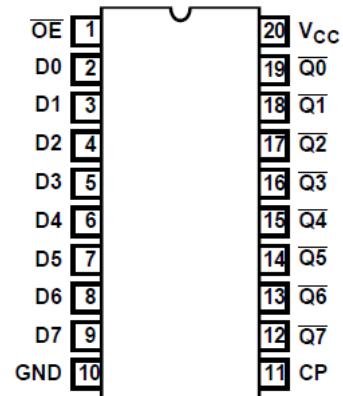
<b>Changes from Revision D (January 2022) to Revision E (October 2022)</b>	<b>Page</b>
• Increased R $\theta$ JA for packages: DW (58 to 109.1); N (69 to 84.6).....	4

<b>Changes from Revision C (April 2004) to Revision D (January 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

## 4 Pin Configuration and Functions



**HC/HCT534**  
 J or N package  
 20-Pin CDIP or PDIP  
 Top View



**HC/HCT564**  
 J, N, or DW package  
 20-Pin CDIP, PDIP, or SOIC  
 Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Drain current, per output	For -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±35 mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25 mA
Continuous current through V <sub>CC</sub> or GND				±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature range	-65	150	°C
Lead temperature (Soldering 10s) (SOIC - lead tips only)				300 °C

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub> , V <sub>O</sub>	Input or output voltage	0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input rise and fall time	2 V	1000	ns	
		4.5 V	500		
		6 V	400		
T <sub>A</sub>	Temperature range	-55	125	°C	

### 5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	UNIT
		20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	84.6	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	76	72.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	77.6	65.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	51.5	55.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.1	65.2	°C/W
R <sub>θJC (bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER	TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
V <sub>IH</sub>	High level input voltage		2	1.5		1.5		1.5		V
			4.5	3.15		3.15		3.15		
			6	4.2		4.2		4.2		
V <sub>IL</sub>	Low level input voltage		2		0.5		0.5		0.5	V
			4.5		1.35		1.35		1.35	
			6		1.8		1.8		1.8	
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = –20 μA	2	1.9		1.9		1.9		V
		I <sub>OH</sub> = –20 μA	4.5	4.4		4.4		4.4		
		I <sub>OH</sub> = –20 μA	6	5.9		5.9		5.9		
	High level output voltage	I <sub>OH</sub> = –6 mA	4.5	3.98		3.84		3.7		
		I <sub>OH</sub> = –7.8 mA	6	5.48		5.34		5.2		
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	2		0.1		0.1		0.1	V
		I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1	
		I <sub>OL</sub> = 20 μA	6		0.1		0.1		0.1	
	Low level output voltage	I <sub>OL</sub> = 6 mA	4.5		0.26		0.33		0.4	
		I <sub>OL</sub> = 7.8 mA	6		0.26		0.33		0.4	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6		±0.1		±1		±1	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	6		8		80		160	μA
I <sub>OZ</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6		±0.5		±5.0		±10	μA
<b>HCT TYPES</b>										
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2		2		2		V
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8	V
V <sub>OH</sub>	High level output voltage	V <sub>OH</sub> = –20 μA	4.5	4.4		4.4		4.4		V
	High level output voltage	V <sub>OH</sub> = –6 mA	4.5	3.98		3.84		3.7		
V <sub>OL</sub>	Low level output voltage	V <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1	V
	Low level output voltage	V <sub>OL</sub> = 6 mA	4.5		0.26		0.33		0.4	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5		±0.1		±1		±1	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5		8		80		160	μA
I <sub>OZ</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5		±0.5		±5.0		±10	μA

## 5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\Delta I_{CC}$ <sup>(1)</sup>	Additional supply current per input pin	D0 - D7 inputs held at V <sub>CC</sub> –2.1	4.5 to 5.5		100	54		67.5		73.5	μA
		CP input held at V <sub>CC</sub> –2.1	4.5 to 5.5		100	108		135		147	
		$\overline{OE}$ input held at V <sub>CC</sub> –2.1	4.5 to 5.5		100	198		247.5		269.5	

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>.

## 5.5 Prerequisite for Switching Characteristics

PARAMETER		V <sub>CC</sub> (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>HC TYPES</b>												
f <sub>MAX</sub>	Maximum clock frequency	2	6		5		4				MHz	
		4.5	30		25		20					
		6	35		29		23					
t <sub>W</sub>	Clock pulse width	2	80		100		120				ns	
		4.5	16		20		24					
		6	14		17		20					
t <sub>SU</sub>	Setup time data to clock	2	60		75		90				ns	
		4.5	12		15		18					
		6	10		13		15					
t <sub>H</sub>	Hold time data to clock	2	5		5		5				ns	
		4.5	5		5		5					
		6	5		5		5					
<b>HCT TYPES</b>												
f <sub>MAX</sub>	Maximum clock frequency	4.5	25		20		16				MHz	
t <sub>W</sub>	Clock pulse width	4.5	20		25		30				ns	
t <sub>SU</sub>	Setup time data to clock	4.5	20		25		30				ns	
t <sub>H</sub>	Hold time Data to clock (534)	4.5	5		5		5				ns	
t <sub>H</sub>	Hold time Data to clock (564)	4.5	3		3		3				ns	

## 5.6 Switching Characteristics

 $C_L = 50 \text{ pF}$ , Input  $t_r$ ,  $t_f = 6 \text{ ns}$ 

PARAMETER		$V_{CC}$ (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
$t_{PLH}$ , $t_{PHL}$	Propagation delay clock to output	2		165		205		250	ns	
		4.5		13 <sup>(3)</sup>	33		41	50		
		6		28		35		43		
$t_{PL}$ , $t_{PHZ}$	Output disable to Q (534)	2		150		190		225	ns	
		4.5		12 <sup>(3)</sup>	30		38	45		
		6		26		33		38		
$t_{PLZ}$ , $t_{PHZ}$	Output disable to Q (564)	2		135		170		205	ns	
		4.5		12 <sup>(3)</sup>	27		34	41		
		6		23		29		35		
$t_{PZL}$ , $t_{PZH}$	Output enable to Q	2		150		190		225	ns	
		4.5		12 <sup>(3)</sup>	30		38	45		
		6		26		33		38		
$f_{MAX}$	Maximum clock frequency	5		60 <sup>(4)</sup>					MHz	
$t_{THL}$ , $t_{TLH}$	Output transition time	2		60		75		90	ns	
		4.5		12		15		18		
		6		10		13		15		
$C_I$	Input capacitance		10	10		10		10	pF	
$C_O$	Three-state output capacitance		20	20		20		20	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	5		32					pF	
<b>HCT TYPES</b>										
$t_{PHL}$ , $t_{PLH}$	Propagation delay clock to output	4.5		14 <sup>(3)</sup>	35		44		53	ns
$t_{PLZ}$ , $t_{PHZ}$	Output disable to Q	4.5		12 <sup>(3)</sup>	30		38		45	ns
$t_{PHL}$ , $t_{PZH}$	Output enable to Q	4.5		14 <sup>(3)</sup>	35		44		53	ns
$f_{MAX}$	Maximum clock frequency	5		50 <sup>(4)</sup>						MHz
$t_{TLH}$ , $t_{THL}$	Output transition time	4.5		12		15		18	ns	
$C_I$	Input capacitance		10	10		10		10	pF	
$C_O$	Three-state output capacitance		20	20		20		20	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	5		36					pF	

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per package.

(2)  $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

(3)  $C_L = 15 \text{ pF}$  and  $V_{CC} = 5 \text{ V}$ .

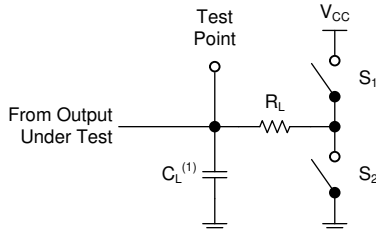
(4)  $C_L = 15 \text{ pF}$ .

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

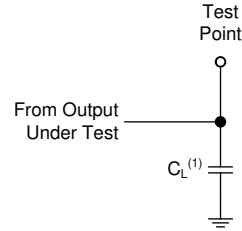
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



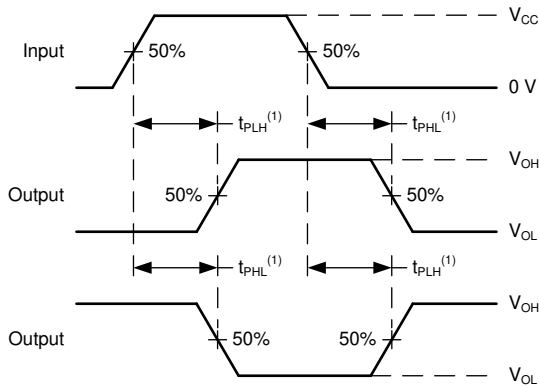
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**



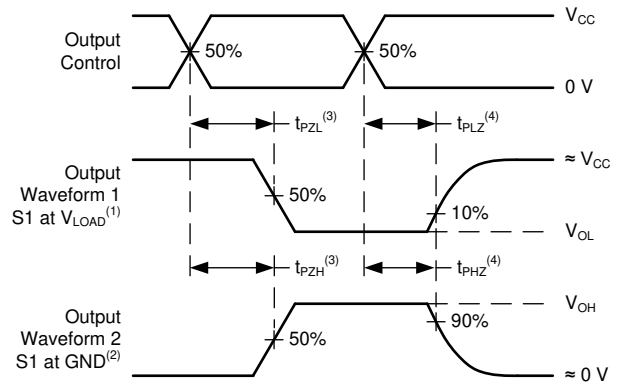
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-2. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-3. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



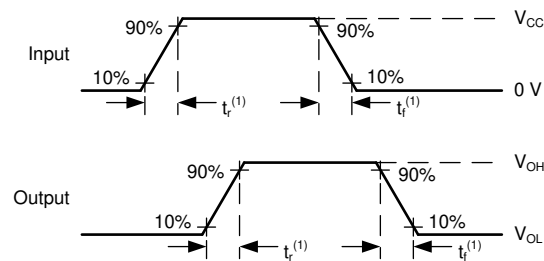
(1) S1 = CLOSED; S2 = OPEN.

(2) S1 = OPEN; S2 = CLOSED.

(3)  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(4)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

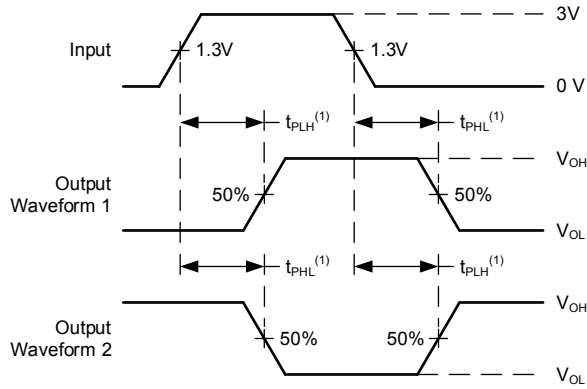
**Figure 6-4. Voltage Waveforms, Standard CMOS Inputs Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

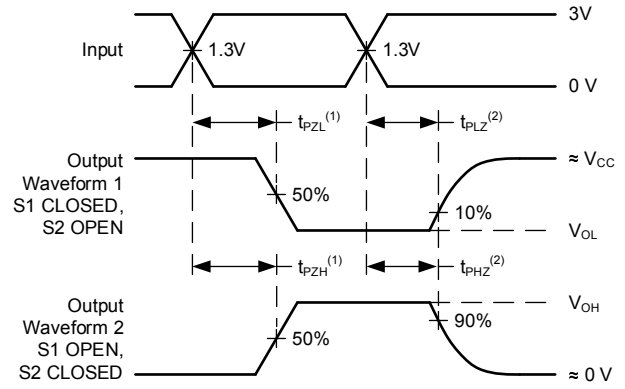
**Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**





(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-6. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**



(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**

## 7 Detailed Description

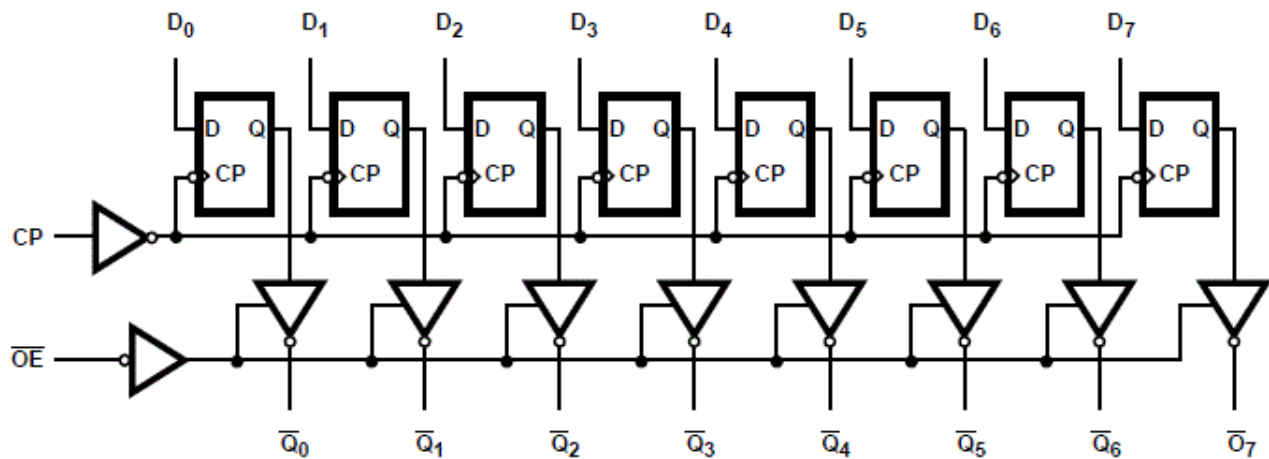
### 7.1 Overview

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are high speed Octal D-Type Flip-Flops manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the three-state feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the Q outputs on the positive going transition of the CLOCK input. When a high logic level is applied to the OUTPUT ENABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The HCT logic family is speed, function, and pin compatible with the standard LS logic family.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)</sup>

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	$\overline{Qn}$
L	↑	H	L
L	↑	L	H
L	L	X	No change
H	X	X	Z

- (1) H = high level (steady state), L = low level (steady state), X = don't care, ↑ = transition from low to high level, Z = High impedance state

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8681401RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681401RA CD54HC534F3A
<a href="#">5962-8681501RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681501RA CD54HC564F3A
<a href="#">5962-8984901RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984901RA CD54HCT534F3A
<a href="#">CD54HC534F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681401RA CD54HC534F3A
CD54HC534F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681401RA CD54HC534F3A
<a href="#">CD54HC564F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681501RA CD54HC564F3A
CD54HC564F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681501RA CD54HC564F3A
<a href="#">CD54HCT534F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984901RA CD54HCT534F3A
CD54HCT534F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8984901RA CD54HCT534F3A
<a href="#">CD54HCT564F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT564F3A
CD54HCT564F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT564F3A
<a href="#">CD74HC534E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC534E
CD74HC534E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC534E
<a href="#">CD74HC564E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC564E
CD74HC564E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC564E
<a href="#">CD74HC564M</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC564M
CD74HC564M.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC564M
<a href="#">CD74HC564M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC564M
CD74HC564M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC564M
<a href="#">CD74HCT534E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT534E
CD74HCT534E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT534E
<a href="#">CD74HCT564E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT564E

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT564E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT564E
<a href="#">CD74HCT564M</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT564M
CD74HCT564M.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT564M
CD74HCT564MG4	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT564M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD54HC534, CD54HC564, CD54HCT534, CD54HCT564, CD74HC534, CD74HC564, CD74HCT534, CD74HCT564 :**

● Catalog : [CD74HC534](#), [CD74HC564](#), [CD74HCT534](#), [CD74HCT564](#)

- Military : [CD54HC534](#), [CD54HC564](#), [CD54HCT534](#), [CD54HCT564](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC564M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC564M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC564M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HC564M96	SOIC	DW	20	2000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC534E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC534E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC564E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC564E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC564M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HC564M.A	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT534E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT534E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT564E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT564E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT564M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT564M.A	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT564MG4	DW	SOIC	20	25	507	12.83	5080	6.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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