High Speed CMOS Logic Hex Buffer/Line Driver, Three-State Non-Inverting and Inverting

1 Features

- Buffered inputs
- High current bus driver outputs
- Typical propagation delay t_{PLH}, t_{PHL} = 8 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL Loads
  - Bus driver outputs: 15 LSTTL Loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL},V_{OH}

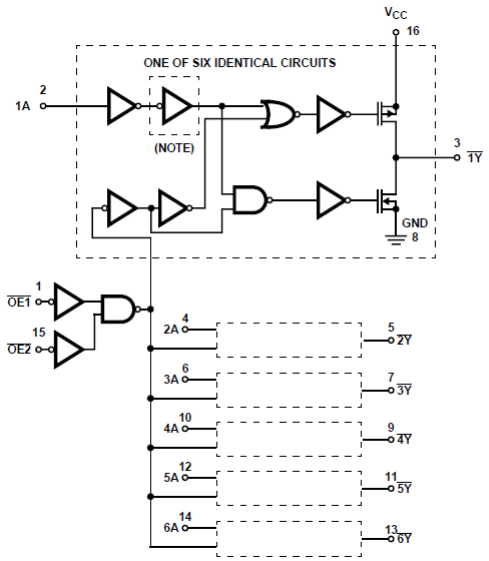
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC365	J (CERDIP, 16)	19.56 x 6.92 mm
CD54HC366	J (CERDIP, 16)	19.56 x 6.92 mm
CD54HCT365	J (CERDIP, 16)	19.56 x 6.92 mm
CD74HC365	N (PDIP, 16)	19.30 x 6.35 mm
	D (SOIC, 16)	9.90 x 3.90 mm
	D (SOIC, 16)	9.90 x 3.90 mm
	D (SOIC, 16)	9.90 x 3.90 mm
CD74HC366	N (PDIP, 16)	19.30 x 6.35 mm
	D (SOIC, 16)	9.90 x 3.90 mm
	D (SOIC, 16)	9.90 x 3.90 mm
CD74HCT365	N (PDIP, 16)	19.30 x 6.35 mm
	D (SOIC, 16)	9.90 x 3.90 mm
	D (SOIC, 16)	9.90 x 3.90 mm
	D (SOIC, 16)	9.90 x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

2 Description

The ’HC365, ’HCT365, and ’HC366 silicon gate CMOS three-state buffers are general purpose high-speed non-inverting and inverting buffers.



Logic Diagram for the HC/HCT365 and HC366 (Outputs for HC/HCT365 are Complements of Those Shown, i.e., 1Y, 2Y, etc.)

A. Inverter not included in HC/HCT 365.

Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2003) to Revision D (July 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions

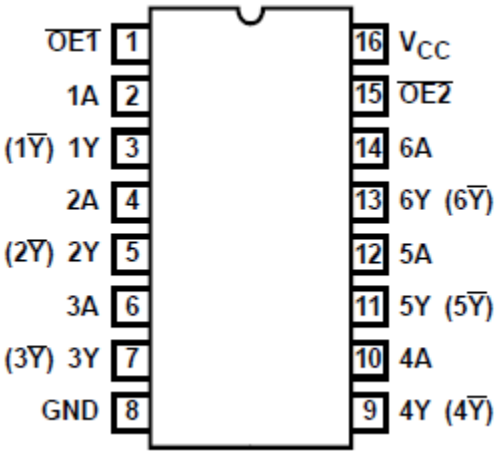


Figure 4-1. CD54HC365, CD54HCT365, CD54HC366 (CERDIP) CD74HC365, CD74HCT365, CD74HC366 (PDIP, SOIC) Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output Enable 1, Active Low
2	1A	I	1A Input
3	1Y	O	1Y Output
4	2A	I	2A Input
5	2Y	O	2Y Output
6	3A	I	3A Input
7	3Y	O	3Y Output
8	GND	—	Ground Pin
9	4Y	O	4Y Output
10	4A	I	4A Input
11	5Y	O	5Y Output
12	5A	I	5A Input
13	6Y	O	6Y Output
14	6A	I	6A Input
15	$\overline{OE2}$	I	Output Enable 2, Active Low
16	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	DC supply voltage		-0.5	7	V
I_{IK}	DC input diode current	For V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	DC output diode current	For V_O < -0.5 V or V_O > V_{CC} + 0.5		±20	mA
I_O	DC drain current, per output	For -0.5 V < V_O < V_{CC} + 0.5 V		±35	mA
I_O	DC output source or sink current per output pin	For V_O > -0.5 V or V_O < V_{CC} + 0.5 V		±25	mA
I_{CC}	DC V_{CC} or ground current			±50	mA
T_J	Maximum junction temperature			150	℃
T_{stg}	Maximum storage temperature range		-65	150	℃
	Maximum lead temperature (soldering 10s)SOIC - lead tips only			300	℃

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	V
V_I, V_O	DC input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		-55	125	℃

5.3 Thermal Information

THERMAL METRIC		N (PDIP) 16 PINS	D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	67	73	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51 - 7

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
V_{IH}	High level input voltage			2	1.5			1.5		1.5		V
				4.5	3.15			3.15		3.15		
				6	4.2			4.2		4.2		
V_{IL}	Low level input voltage			2			0.5		0.5		0.5	V
				4.5			1.35		1.35		1.35	
				6			1.8		1.8		1.8	
V_{OH}	High level output voltage CMOS loads	V_{IH} or V_{IL}	-0.02	2	1.9			1.9		1.9		V
			-0.02	4.5	4.4			4.4		4.4		
			-0.02	6	5.9			5.9		5.9		
	High level output voltage TTL loads		-6	4.5	3.98			3.84		3.7		
			-7.8	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage CMOS loads	V_{IH} or V_{IL}	0.02	2			0.1		0.1		0.1	V
			0.02	4.5			0.1		0.1		0.1	
			0.02	6			0.1		0.1		0.1	
	Low level output voltage TTL loads	V_{IH} or V_{IL}	6	4.5			0.26		0.33		0.4	
			7.8	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND		6			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_{CC} or GND	0	6			8		80		160	µA
I_{OZ}	Three-state leakage current	V_{IH} or V_{IL}	V_O = V_{CC} or GND	6			±0.5		±5		±10	µA
HCT TYPES												
V_{IH}	High level input voltage			4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage CMOS loads	V_{IH} or V_{IL}	-0.02	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads		-4	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage CMOS loads	V_{IH} or V_{IL}	0.02	4.5			0.1		0.1		0.1	V
	Low level output voltage TTL loads		4	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	0	5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_{CC} or GND	0	5.5			8		80		160	µA
ΔI_{CC}	Additional supply current per input pin: 1 Unit Load(1)	V_{CC} - 2.1		4.5 to 5.5		100	360		450		490	µA
I_{OZ}	Three-state leakage current	V_{IL} or V_{IH}	V_O = V_{CC} or GND	5.5			±0.5		±5		±10	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA

5.5 HCT Input Loading Table

Input	Unit Loads(1)
$\overline{OE1}$	0.6
All others	0.55

(1) Unit Load is ΔI_{CC} limit specified in Section 5.4, e.g., 360 µA max at 25°C.

5.6 Switching Characteristics

t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C		40°C to 85°C	55°C to 125°C	UNIT
				TYP	MAX	MAX	MAX	
HC TYPES								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs HC/HCT 365	C_L = 50 pF	2		105	130	160	ns
			4.5		21	26	32	ns
			6		18	22	27	ns
		C_L = 15 pF	5	8				ns
t_{PLH}, t_{PHL}	Propagation delay, data to outputs HC 366	C_L = 50 pF	2		110	140	165	ns
			4.5		22	28	33	ns
			6		19	24	28	ns
		C_L = 15 pF	5	9				ns
t_{PLH}, t_{PHL}	Propagation delay time, output enable and disable to outputs	C_L = 50 pF	2		150	190	225	ns
			4.5		30	38	45	ns
			6		26	33	38	ns
		C_L = 15 pF	5	12				ns
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	2		60	75	90	ns
			4.5		12	15	18	ns
			6		10	13	15	ns
C_I	Input capacitance				10	10	10	pF
C_O	Three-state ouput capacitance				20	20	20	pF
C_{PD}	Power dissipation capacitance(1) (2)		5	40				pF
HCT TYPES								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs HC/HCT 365	C_L = 50 pF	4.5		25	31	38	ns
								ns
		C_L = 15 pF	5	9				ns
								ns
t_{PLH}, t_{PHL}	Propagation delay, data to outputs HC 366	C_L = 50 pF	4.5		27	34	41	ns
		C_L = 15 pF	5	11				ns
t_{PLH}, t_{PHL}	Propagation delay time, output enable and disable to ouputs	C_L = 50 pF	4.5		35	44	53	ns
		C_L = 15 pF	5	14				ns
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5		12	15	18	ns
C_{IN}	Input capacitance				10	10	10	pF
C_O	Three-stage capacitance				20	20	20	pF
C_{PD}	Power dissipation capacitance(1) (2)		5	42				pF

(1) C_{PD} is used to determine the dynamic power consumption, per buffer.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_l)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

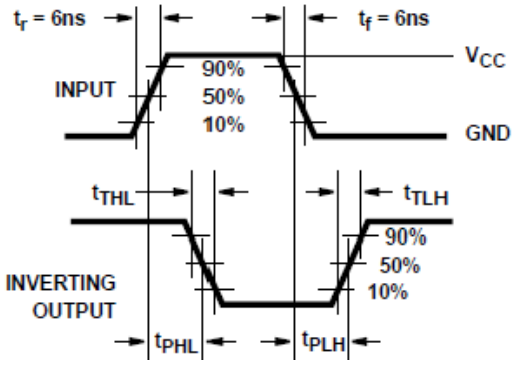


Figure 6-1. HC Transition Times and Propagation Delay Times, Combination Logic

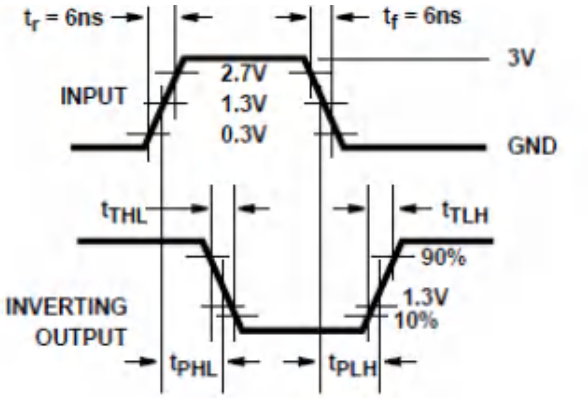


Figure 6-2. HCT Transition Times and Propagation Delay Times, Combination Logic

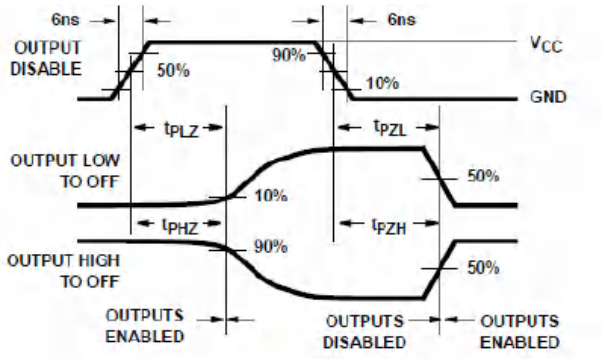


Figure 6-3. HC Three-State Propagation Delay Waveform

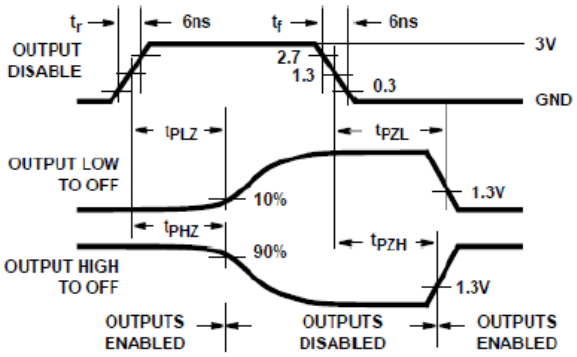
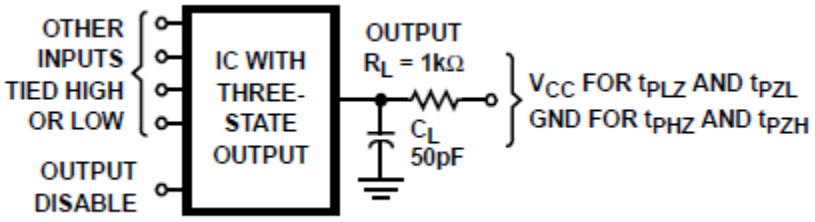


Figure 6-4. HCT Three-State Propagation Delay Waveform



A. Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is output R_L = 1 kΩ to V_{CC}, C_L = 50 pF.

Figure 6-5. HC and HCT Three-State Propagation Delay Test Circuit

7 Detailed Description

7.1 Overview

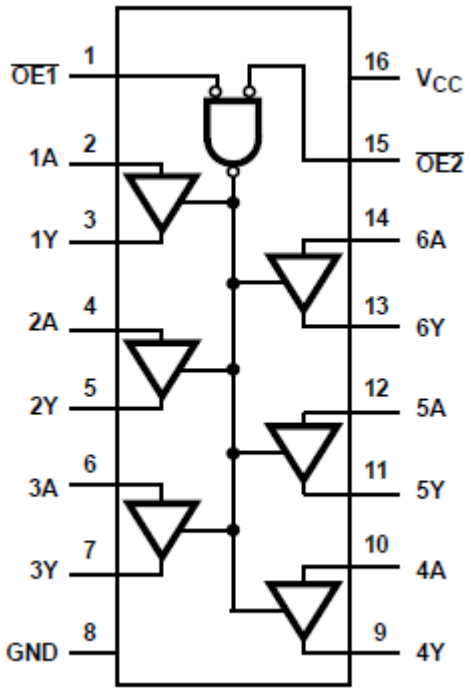
The ’HC365, ’HCT365, and ’HC366 silicon gate CMOS three-state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The ’HC365 and ’HCT365 are non-inverting buffers, whereas the ’HC366 is an inverting buffer. These devices have two three-state control inputs ($\overline{OE1}$ and $\overline{OE2}$) which are NORed together to control all six gates.

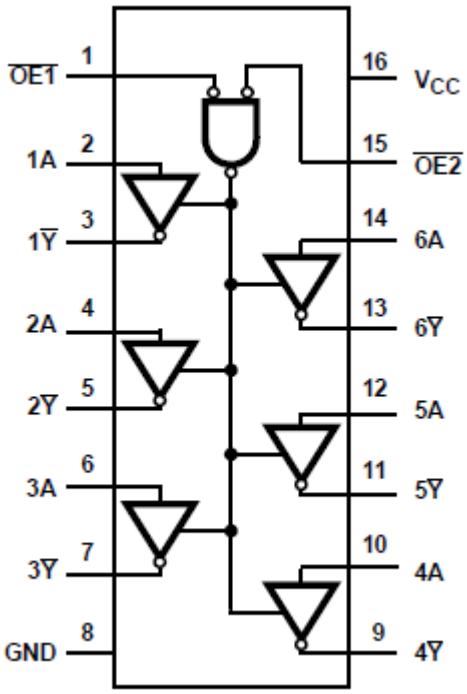
The ’HCT365 logic families are speed, function and pin compatible with the standard LS logic family.

7.2 Functional Block Diagram

Functional Diagrams



HC365, HCT365



HC366

7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS[1]			OUTPUTS (Y)[2]	
$\overline{OE\ 1}$	$\overline{OE\ 2}$	A	HC/HCT 365	HCT 366
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC365F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500101EA CD54HC365F3A
CD54HC365F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500101EA CD54HC365F3A
CD54HC366F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682801EA CD54HC366F3A
CD54HC366F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682801EA CD54HC366F3A
CD54HCT365F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT365F3A
CD54HCT365F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT365F3A
CD74HC365E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC365E
CD74HC365E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC365E
CD74HC365M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC365M
CD74HC365M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC365M
CD74HC365M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC365M
CD74HC365MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC365M
CD74HC366E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC366E
CD74HC366E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC366E
CD74HC366M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC366M
CD74HC366M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC366M
CD74HC366M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC366M
CD74HCT365E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT365E
CD74HCT365E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT365E
CD74HCT365M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT365M
CD74HCT365M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT365M
CD74HCT365M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT365M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC365, CD54HC366, CD54HCT365, CD74HC365, CD74HC366, CD74HCT365 :

- Catalog : CD74HC365, CD74HC366, CD74HCT365
- Automotive : CD74HC366-Q1, CD74HC366-Q1
- Military : CD54HC365, CD54HC366, CD54HCT365

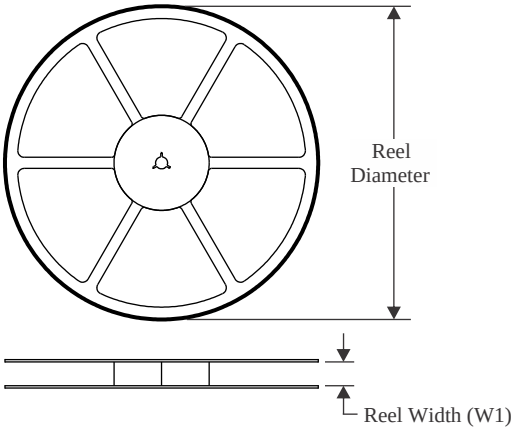
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

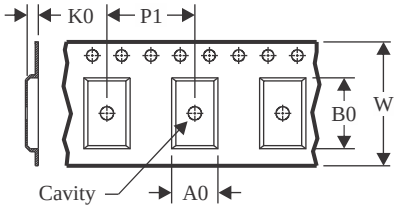
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

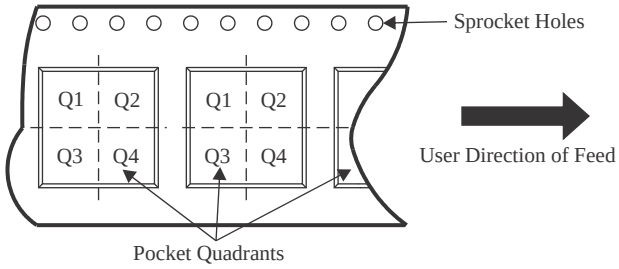


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

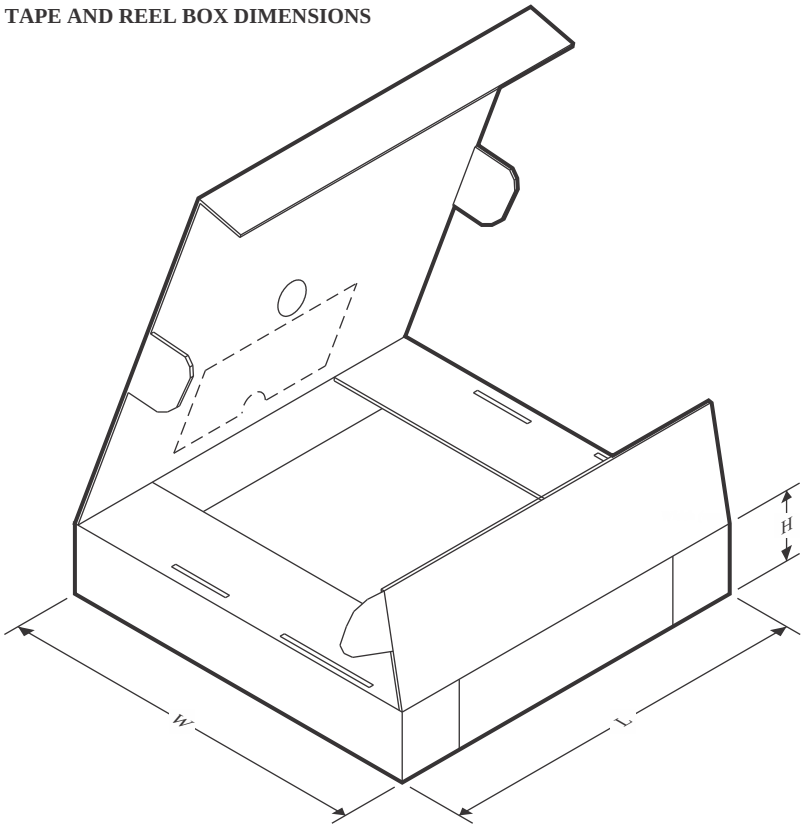
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC365M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC366M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT365M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

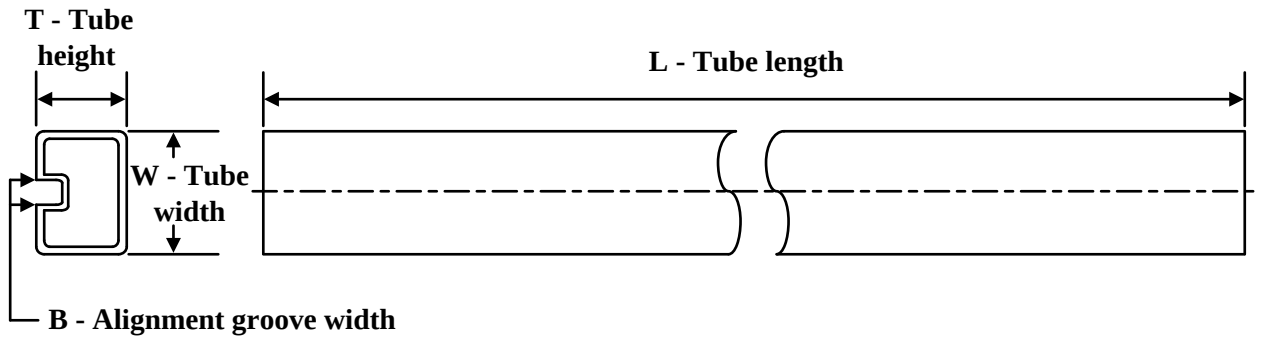
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC365M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC366M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT365M96	SOIC	D	16	2500	353.0	353.0	32.0

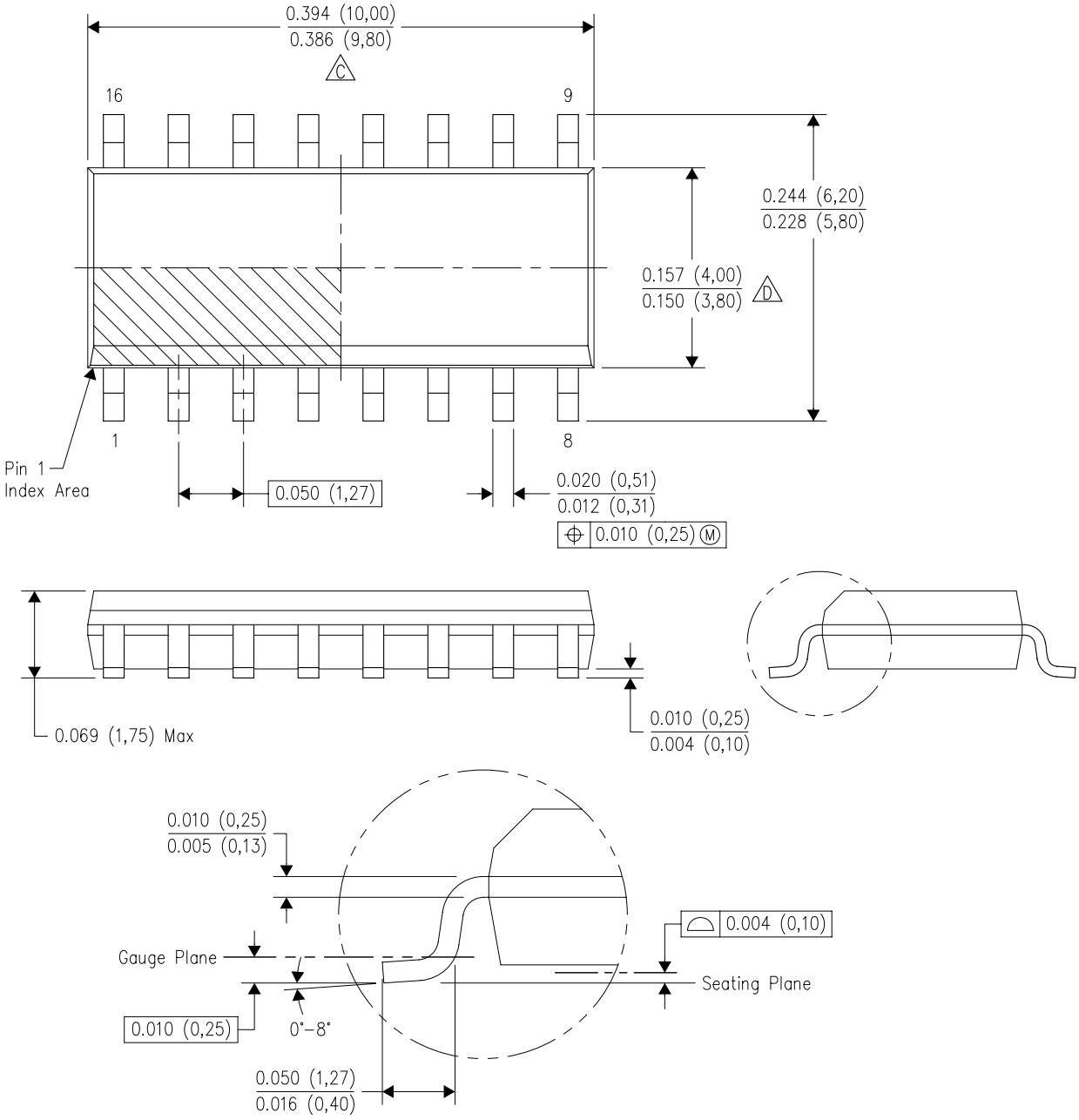
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC365E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC365E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC365E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC365E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC366E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC366E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC366E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC366E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT365E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT365E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT365E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT365E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

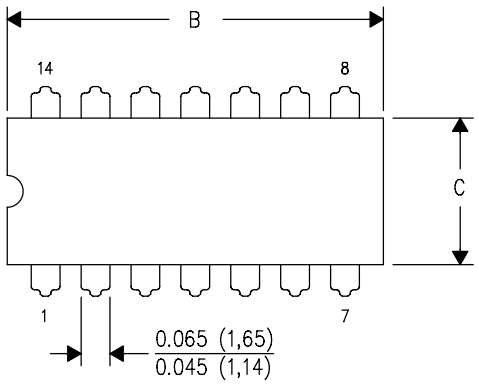


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

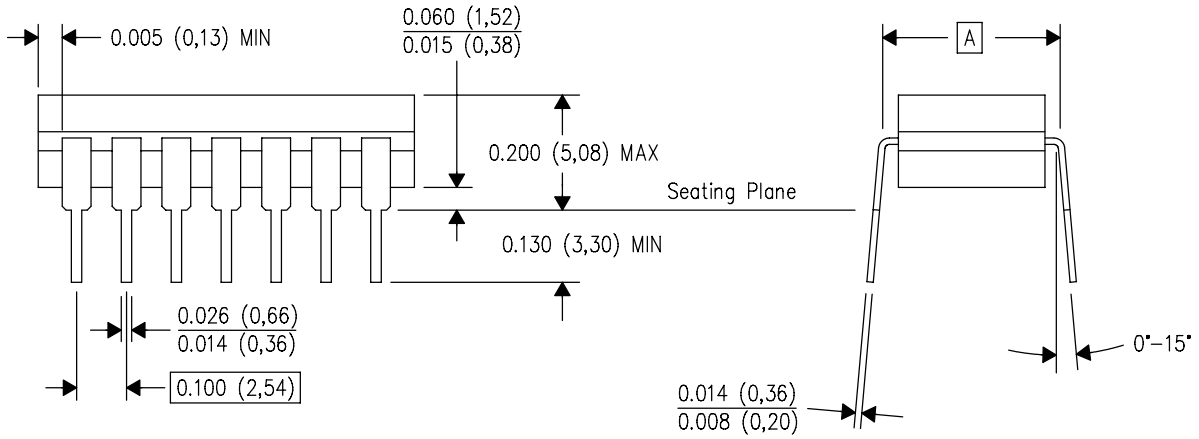
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



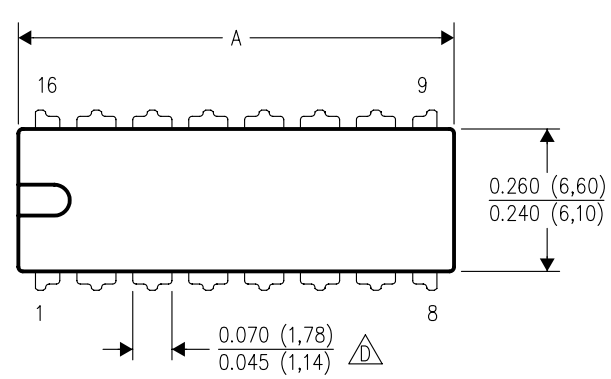
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

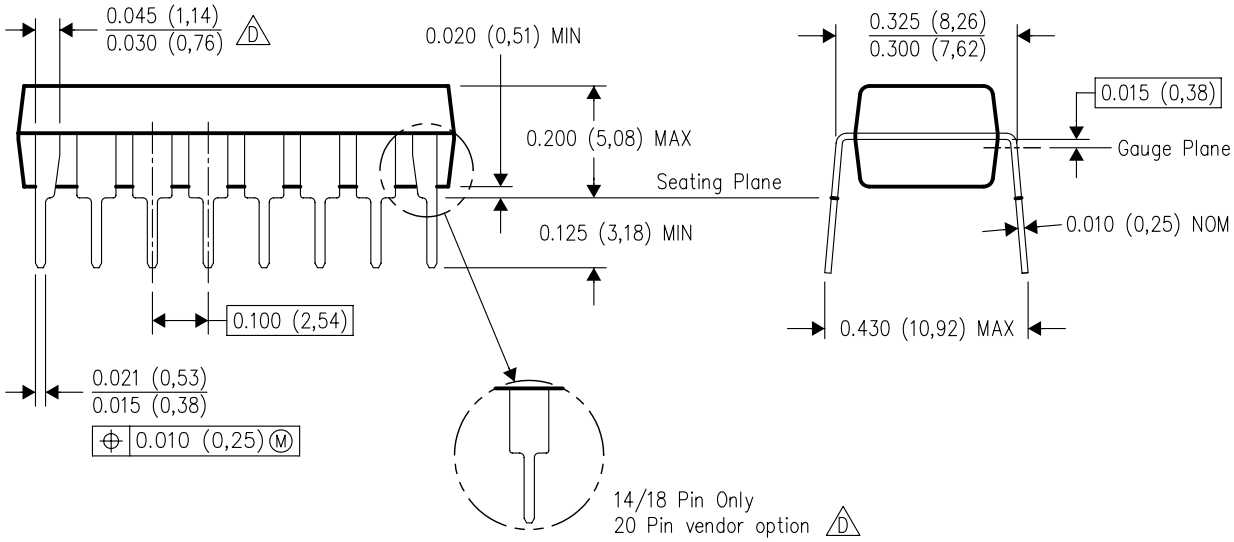
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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