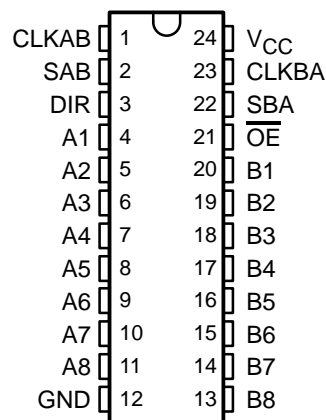


# CD54HC646, CD74HCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

- 2-V to 6-V  $V_{CC}$  Operation (CD54HC646)
- 4.5-V to 5.5-V  $V_{CC}$  Operation (CD74HCT646)
- Wide Operating Temperature Range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive Up To 15 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs
- Inputs Are TTL-Voltage Compatible (CD74HCT646)
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths

CD54HC646 . . . F PACKAGE  
CD74HCT646 . . . M PACKAGE  
(TOP VIEW)



## description/ordering information

The CD54HC646 and CD74HCT646 consist of bus-transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with these devices.

Output-enable ( $\overline{\text{OE}}$ ) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when  $\overline{\text{OE}}$  is active (low). In the isolation mode ( $\overline{\text{OE}}$  high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – M	Tape and reel	CD74HCT646M96	HCT646M
	CDIP – F	Tube	CD54HC646F3A	CD54HC646F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**CD54HC646, CD74HCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCHS278B – APRIL 2003 – REVISED APRIL 2003

**FUNCTION TABLE**

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions can be enabled or disabled by various signals at  $\overline{OE}$  and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



CD54HC646, CD74HCT646  
 OCTAL BUS TRANSCEIVERS AND REGISTERS  
 WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

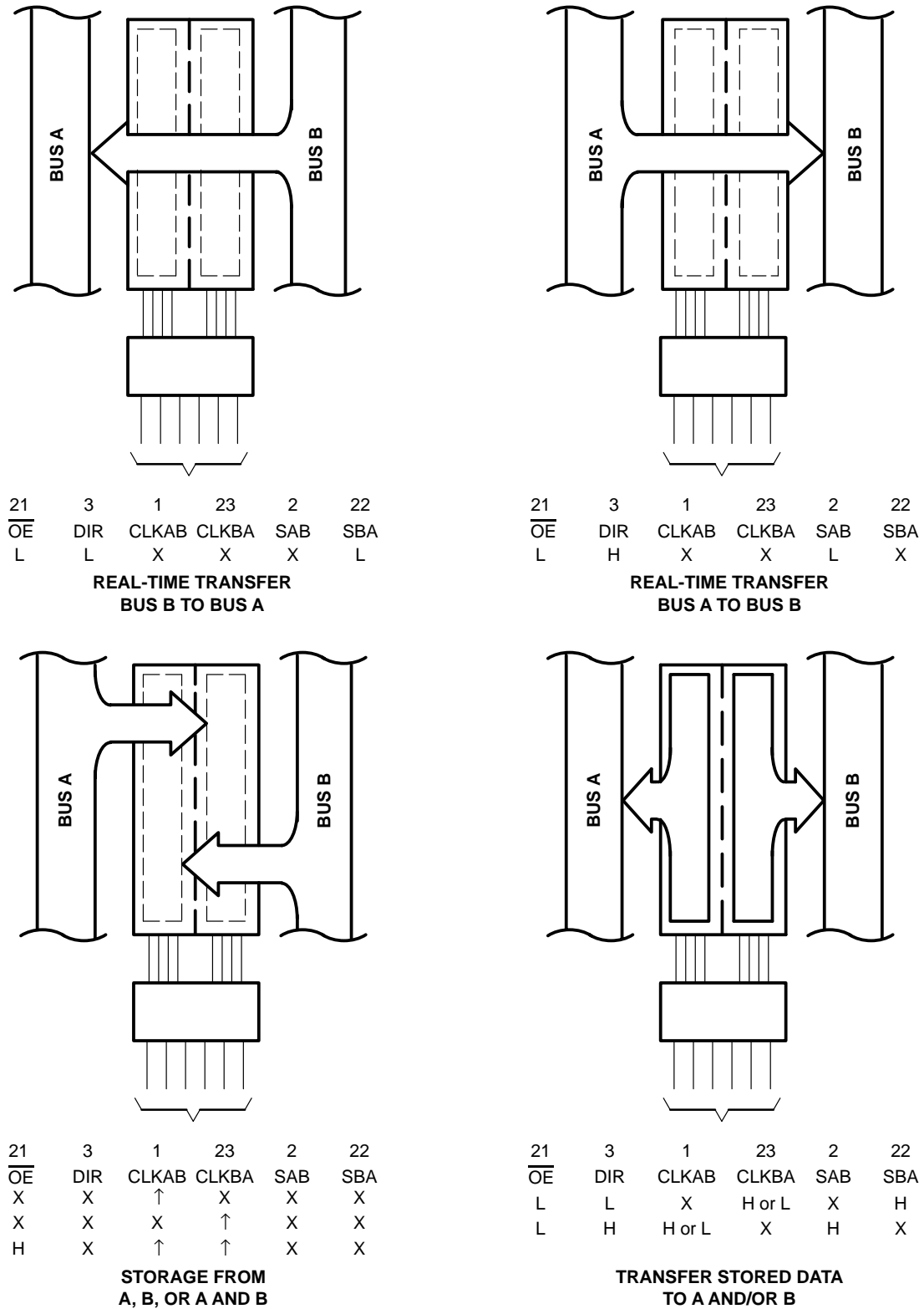
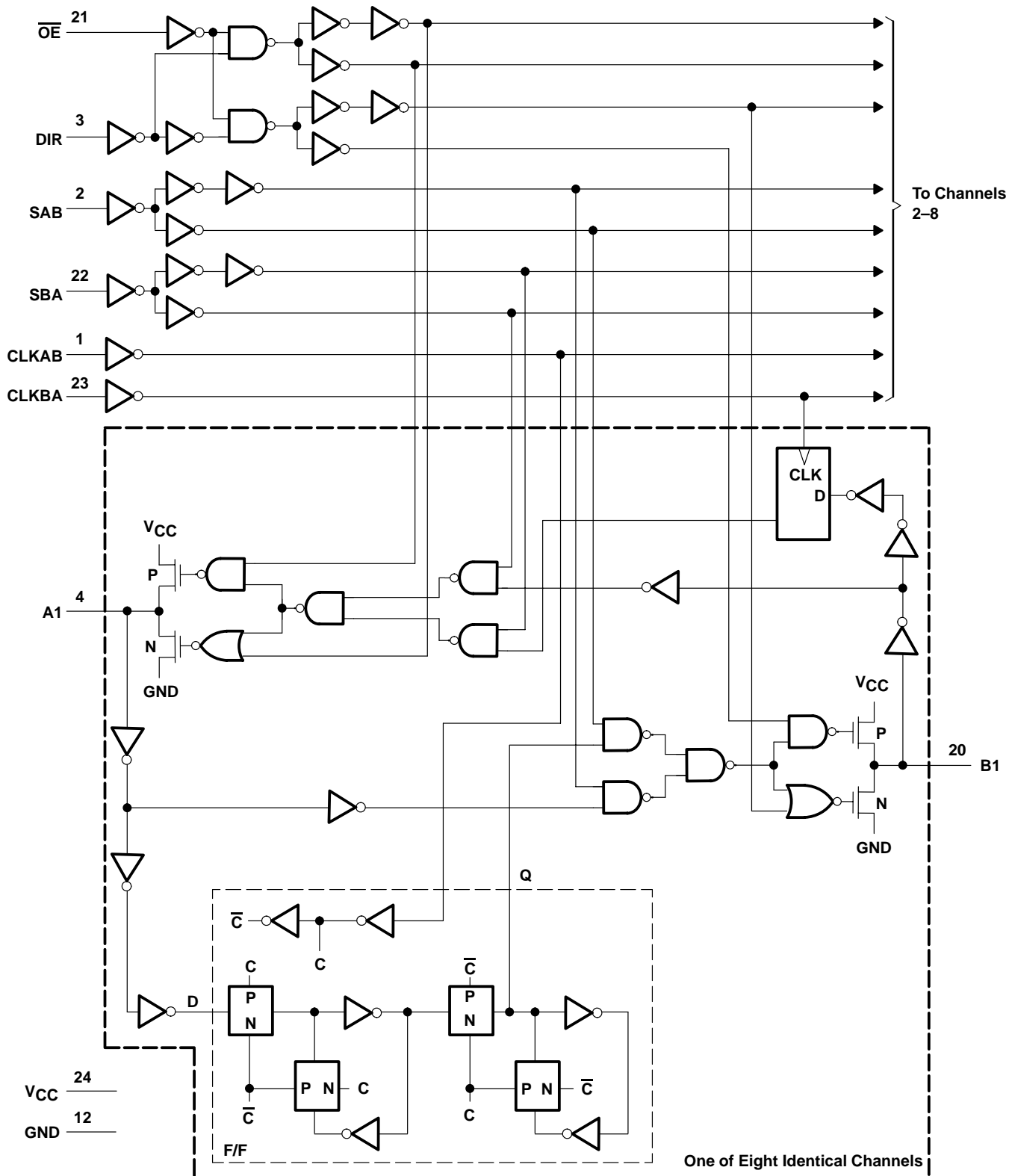


Figure 1. Bus-Management Functions

# CD54HC646, CD74HCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

## logic diagram (positive logic)



# CD54HC646, CD74HCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	±20 mA
Continuous output drain current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±35 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) M package .....	46°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions for CD54HC646 (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 4.5$ V	3.15	
		$V_{CC} = 6$ V	4.2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 4.5$ V	1.35	
		$V_{CC} = 6$ V	1.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	1000	ns
		$V_{CC} = 4.5$ V	500	
		$V_{CC} = 6$ V	400	
$T_A$	Operating free-air temperature	–55	125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## recommended operating conditions for CD74HCT646 (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		$V_{CC}$	V
$V_O$	Output voltage		$V_{CC}$	V
$t_t$	Input transition (rise and fall) time		500	ns
$T_A$	Operating free-air temperature	–55	125	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**CD54HC646, CD74HCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCHS278B – APRIL 2003 – REVISED APRIL 2003

**electrical characteristics for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I <sub>OH</sub> = -6 mA	4.5 V	3.98		3.7		3.84		
		I <sub>OH</sub> = -7.8 mA	6 V	5.48		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I <sub>OL</sub> = 6 mA	4.5 V		0.26		0.4		0.33	
		I <sub>OL</sub> = 7.8 mA	6 V		0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1		±1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		6 V		±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V		8		160		80	μA
C <sub>i</sub>					10		10		10	pF
C <sub>o</sub>					20		20		20	pF

**electrical characteristics for CD74HCT646 over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4			4.4		4.4	V	
		I <sub>OH</sub> = -6 mA		3.98			3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V		0.1		0.1		0.1	V	
		I <sub>OL</sub> = 6 mA			0.26		0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> to GND		5.5 V		±0.1		±1		±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		5.5 V		±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V		8		160		80	μA	
ΔI <sub>CC</sub> †	One input at V <sub>CC</sub> - 2.1 V, Other inputs at 0 or V <sub>CC</sub>		4.5 V to 5.5 V	100	360		490		450	μA	
C <sub>i</sub>					10		10		10	pF	
C <sub>o</sub>					20		20		20	pF	

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load



**CD54HC646, CD74HCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCHS278B – APRIL 2003 – REVISED APRIL 2003

**HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD†
$\overline{OE}$	1.3
DIR	0.75
CLKAB or CLKBA	0.6
SAB or SBA	0.45
A or B	0.3

† Unit Load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 360  $\mu$ A max at 25°C).

**timing requirements for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$ Clock frequency	2 V		6		4		5	MHz
	4.5 V		30		20		25	
	6 V		35		23		29	
$t_w$ Pulse duration, CLKBA or CLKAB high or low	2 V		80		120		100	ns
	4.5 V		16		24		20	
	6 V		14		20		17	
$t_{su}$ Setup time, A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	2 V		60		90		75	ns
	4.5 V		12		18		15	
	6 V		10		15		13	
$t_h$ Hold time, A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	2 V		35		55		45	ns
	4.5 V		7		11		9	
	6 V		6		9		8	

**timing requirements for CD74HCT646 over recommended operating free-air temperature range,  $V_{CC} = 4.5$  V (unless otherwise noted) (see Figure 3)**

	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$ Clock frequency		25		17		20	MHz
$t_w$ Pulse duration, CLKBA or CLKAB high or low		25		38		31	ns
$t_{su}$ Setup time, A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$		12		18		15	ns
$t_h$ Hold time, A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$		5		5		5	ns

# CD54HC646, CD74HCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

switching characteristics for CD54HC646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>			C <sub>L</sub> = 50 pF	2 V	6			4		5	MHz		
				4.5 V	30			20		25			
				6 V	35			23		29			
			C <sub>L</sub> = 15 pF	5 V	60								
t <sub>pd</sub>	CLKBA or CLKAB	A or B	C <sub>L</sub> = 50 pF	2 V		220		330		275	ns		
				4.5 V		44		66		55			
				6 V		37		56		47			
			C <sub>L</sub> = 15 pF	5 V	18								
	A or B	B or A	C <sub>L</sub> = 50 pF	2 V		135		205		170			
				4.5 V		27		41		34			
				6 V		23		35		29			
			C <sub>L</sub> = 15 pF	5 V	12								
			SBA or SAB†	A or B	C <sub>L</sub> = 50 pF	2 V		170		255			215
						4.5 V		34		51			43
	6 V					29		43		37			
	C <sub>L</sub> = 15 pF	5 V			14								
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF	2 V		175		265		220			
				4.5 V		35		53		44			
				6 V		30		45		37			
			C <sub>L</sub> = 15 pF	5 V	14								
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF	2 V		175		265		220			
				4.5 V		35		53		44			
				6 V		30		45		37			
			C <sub>L</sub> = 15 pF	5 V	14								
t <sub>t</sub>		Any	C <sub>L</sub> = 50 pF	2 V		60		90		75			
				4.5 V		12		18		15			
				6 V		10		15		13			

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.





**CD54HC646, CD74HCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCHS278B – APRIL 2003 – REVISED APRIL 2003

**switching characteristics for CD74HCT646 over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 50 pF	4.5 V	25			17		20	MHz	
			C <sub>L</sub> = 15 pF	5 V		45						
t <sub>pd</sub>	CLKBA or CLKAB	A or B	C <sub>L</sub> = 50 pF	4.5 V			44		66	55	ns	
			C <sub>L</sub> = 15 pF	5 V		18						
	A or B	B or A	C <sub>L</sub> = 50 pF	4.5 V			37		56	46		
			C <sub>L</sub> = 15 pF	5 V		15						
	SBA or SAB†	A or B	C <sub>L</sub> = 50 pF	4.5 V			46		69	58		
			C <sub>L</sub> = 15 pF	5 V		19						
t <sub>en</sub>	$\overline{OE}$	A or B	C <sub>L</sub> = 50 pF	4.5 V			45		68	56	ns	
			C <sub>L</sub> = 15 pF	5 V		19						
t <sub>dis</sub>	$\overline{OE}$	A or B	C <sub>L</sub> = 50 pF	4.5 V			35		53	44	ns	
			C <sub>L</sub> = 15 pF	5 V		14						
t <sub>t</sub>			C <sub>L</sub> = 50 pF	4.5 V			12		18	15	ns	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

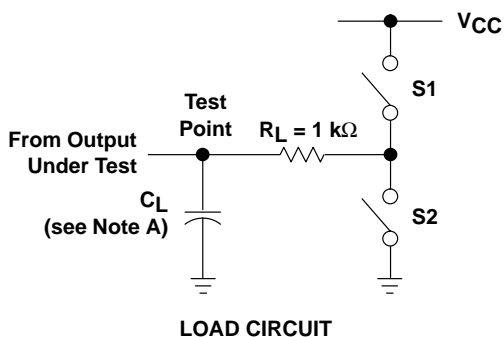
**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	52	pF

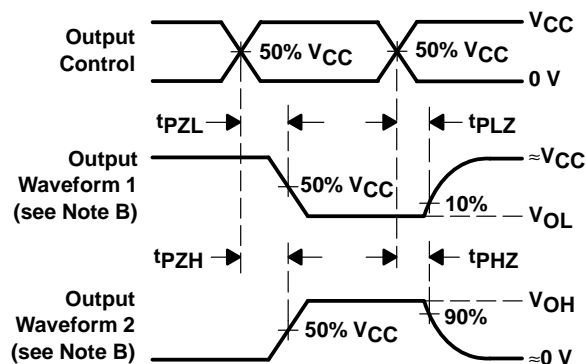
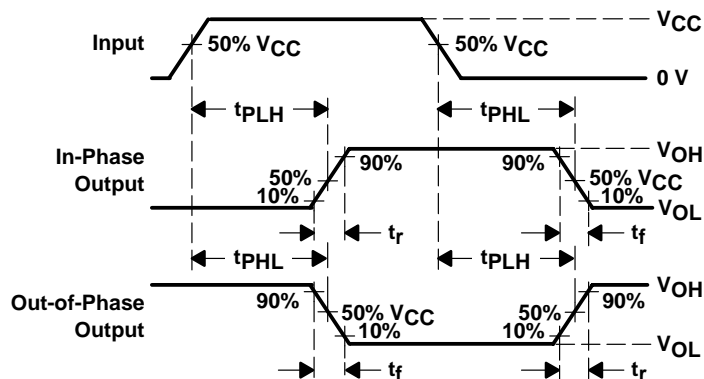
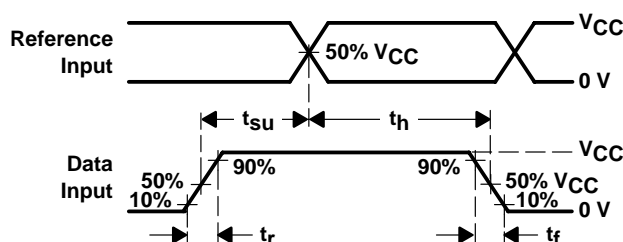
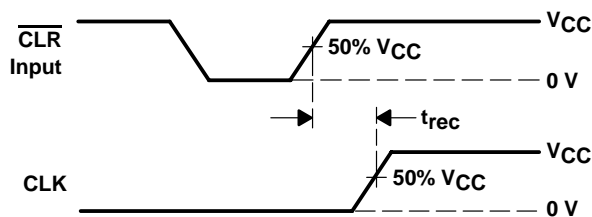
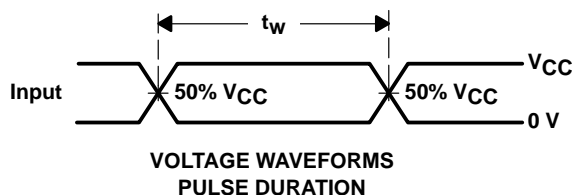
# CD54HC646, CD74HCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCHS278B – APRIL 2003 – REVISED APRIL 2003

## PARAMETER MEASUREMENT INFORMATION – CD54HC646



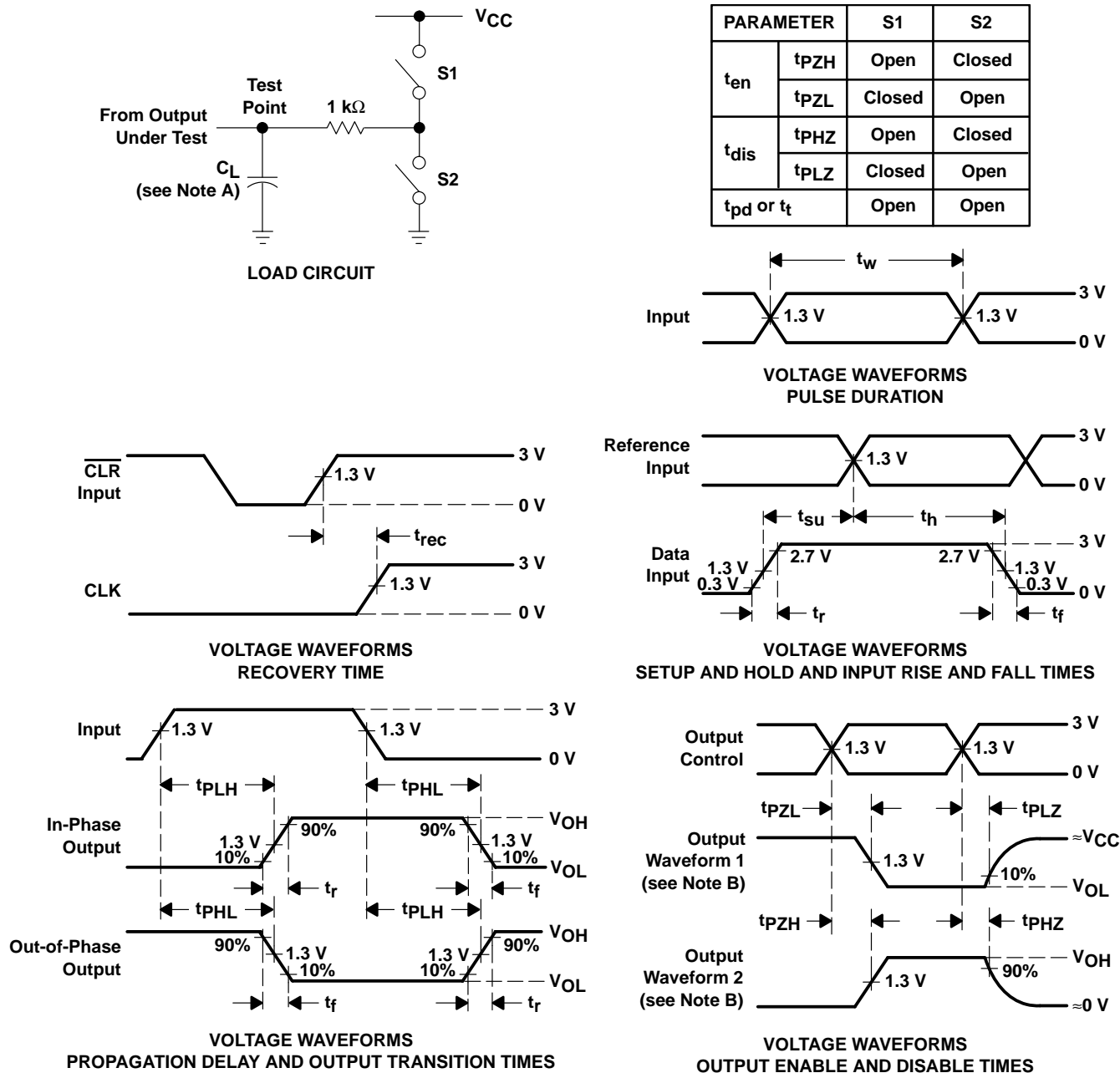
PARAMETER	S1	S2	
$t_{en}$	tPZH	Open	Closed
	tPZL	Closed	Open
$t_{dis}$	tPHZ	Open	Closed
	tPLZ	Closed	Open
$t_{pd}$ or $t_t$	Open	Open	



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 6\text{ ns}$ ,  $t_f = 6\text{ ns}$ .  
 D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.  
 E. The outputs are measured one at a time with one input transition per measurement.  
 F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION – CD74HCT646



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - H.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8688501JA</a>	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
<a href="#">CD54HC646F3A</a>	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
CD54HC646F3A.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8688501JA CD54HC646F3A
<a href="#">CD74HCT646M96</a>	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT646M
CD74HCT646M96.A	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT646M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

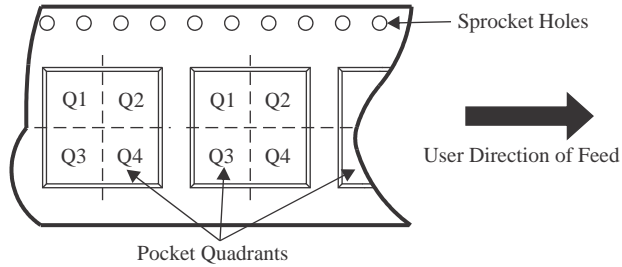
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



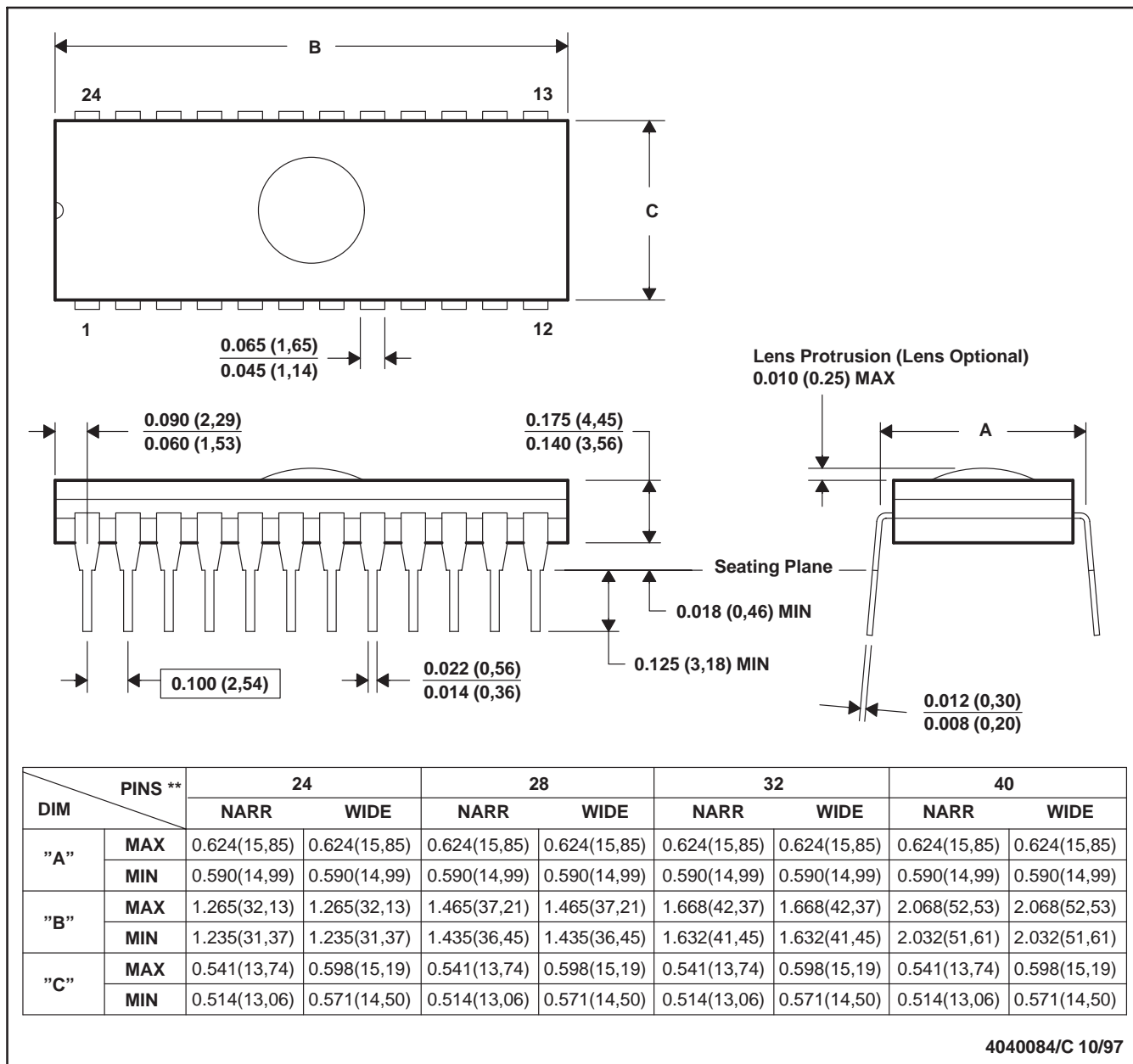
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT646M96	SOIC	DW	24	2000	350.0	350.0	43.0

J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025