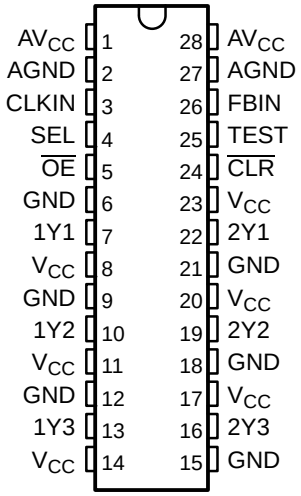
3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS

FEATURES

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **On-Chip Series Damping Resistors**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic 28-Pin Shrink Small-Outline Package**

DB PACKAGE
(TOP VIEW)



DESCRIPTION

The CDC2536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with synchronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC2536 operates at 3.3-V V_{CC} and is designed to drive a 50-W transmission line. The CDC2536 also provides on-chip series-damping resistors, eliminating the need for external termination components.

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency, depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) is provided for output control. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the CDC2536 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2536 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, as well as following any changes to the PLL reference or feedback signals. Such changes occur upon change of SEL, enabling the PLL via TEST, and upon enable of all outputs via $\overline{OE}$.

The CDC2536 is characterized for operation from 0°C to 70°C.

DETAILED DESCRIPTION OF OUTPUT CONFIGURATIONS

The voltage-controlled oscillator (VCO) used in the CDC2536 has a frequency range of 100 MHz to 200 MHz, twice the operating frequency of the CDC2536 outputs. The output of the VCO is divided by two and by four to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. SEL determines which of the two signals is buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency of the output matches that of CLKIN. In the case that a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN frequency resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at the same or twice the CLKIN frequency.

Output Configuration A

Output configuration A is valid when any output configured as a 1× frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2× outputs operate at half the CLKIN frequency, while outputs configured as 1× outputs operate at the same frequency as CLKIN.

Table 1. Output Configuration A

INPUT	OUTPUTS	
SEL	**1/2× FREQUENCY**	**1× FREQUENCY**
L	None	All
H	1Yn	2Yn

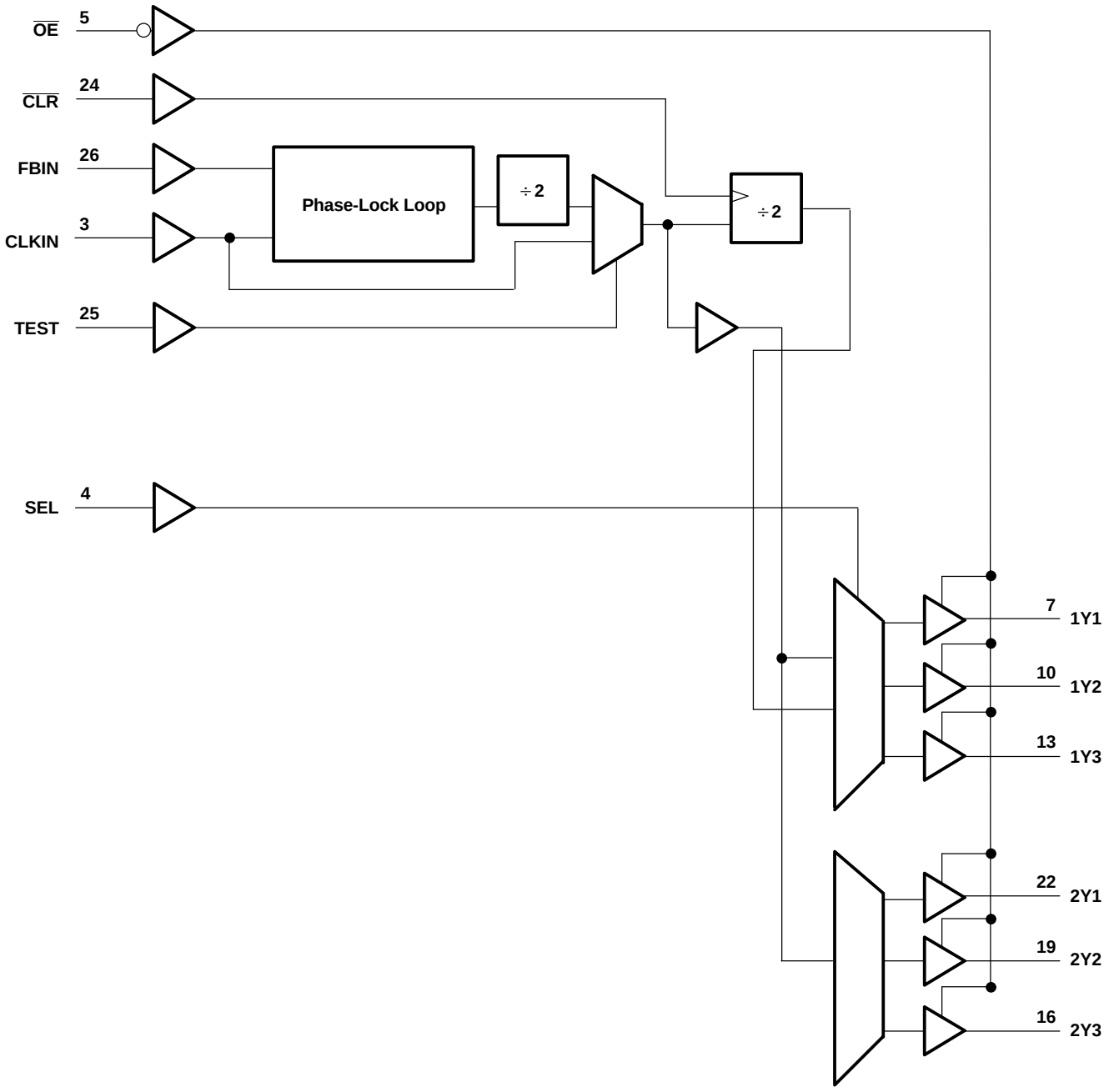
Output Configuration B

Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the CLKIN frequency, while outputs configured as 2× outputs operate at double the frequency of CLKIN.

Table 2. Output Configuration B

INPUT	OUTPUTS	
SEL	**1× FREQUENCY**	**2× FREQUENCY**
H	1Yn	2Yn
L	All	None

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM (continued)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	3	I	Clock input. CLKIN provides the clock signal to be distributed by the CDC2536 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	24	I	$\overline{CLR}$ is used for testing purposes only. Connect $\overline{CLR}$ to GND for normal operation.
FBIN	26	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the six clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and differential CLKIN inputs.
$\overline{OE}$	5	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL	4	I	Output configuration select. SEL selects the output configuration for each output bank (e.g. 1×, 1/2×, or 2×).(see Tables 1 and 2).
TEST	25	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be grounded for normal operation.
1Y1-1Y3	7, 10, 13	O	These outputs are configured by SEL to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
2Y1-2Y3	22, 19, 16	O	These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see (2))	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see (2))	-0.5 V to 5.5 V
Current into any output in the low state, I_O	24 mA
Input clamp current, $I_{IK}(V_I < 0)$	-20 mA
Output clamp current, $I_{OK}(V_O < 0)$	-50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see (3))	0.68 W
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

RECOMMENDED OPERATING CONDITIONS (SEE (1))

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

(1) Unused inputs must be held high or low to prevent them from floating.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = -18 mA			1.2	V
V_{OH}	V_{CC} = MIN to MAX(1),	I_{OH} = -100 µA		V_{CC}- 0.2		V
	V_{CC} = 3 V,	I_{OH} = -12 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8	
I_I	V_{CC} = 0 or MAX(1),	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		2	mA
			Outputs low		2	
			Outputs disabled		2	
C_i	V_I = V_{CC} or GND				6	pF
C_o	V_O = V_{CC} or GND				9	pF

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	When VCO is operating at four times the CLKIN frequency	25	50	MHz
		When VCO is operating at double the CLKIN frequency	50	100	
	Duty cycle, CLKIN		40%	60%	
	Stabilization time(1)	After SEL		50	µs
		After $\overline{OE}\downarrow$		50	
		After power up		50	
		After CLKIN		50	

(1) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

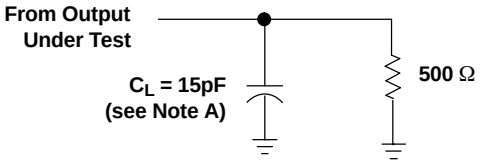
SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see (1) and Figure 1, Figure 2 and Figure 3)

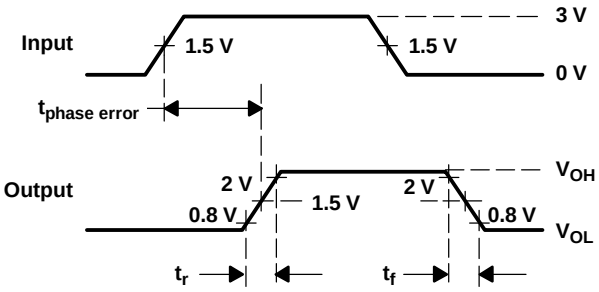
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
Duty cycle		Y	45%	55%	
$t_{phase\ error}$ (2)	CLKIN↑	Y↑	500	+500	ps
$t_{jitter\ (RMS)}$	CLKIN↑	Y↑		200	ps
$t_{sk(o)}$ (2)				0.5	ns
$t_{sk(pr)}$ (2)				1	ns
t_r				1.4	ns
t_f				1.4	ns

(1) The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
(2) The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specfications are only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

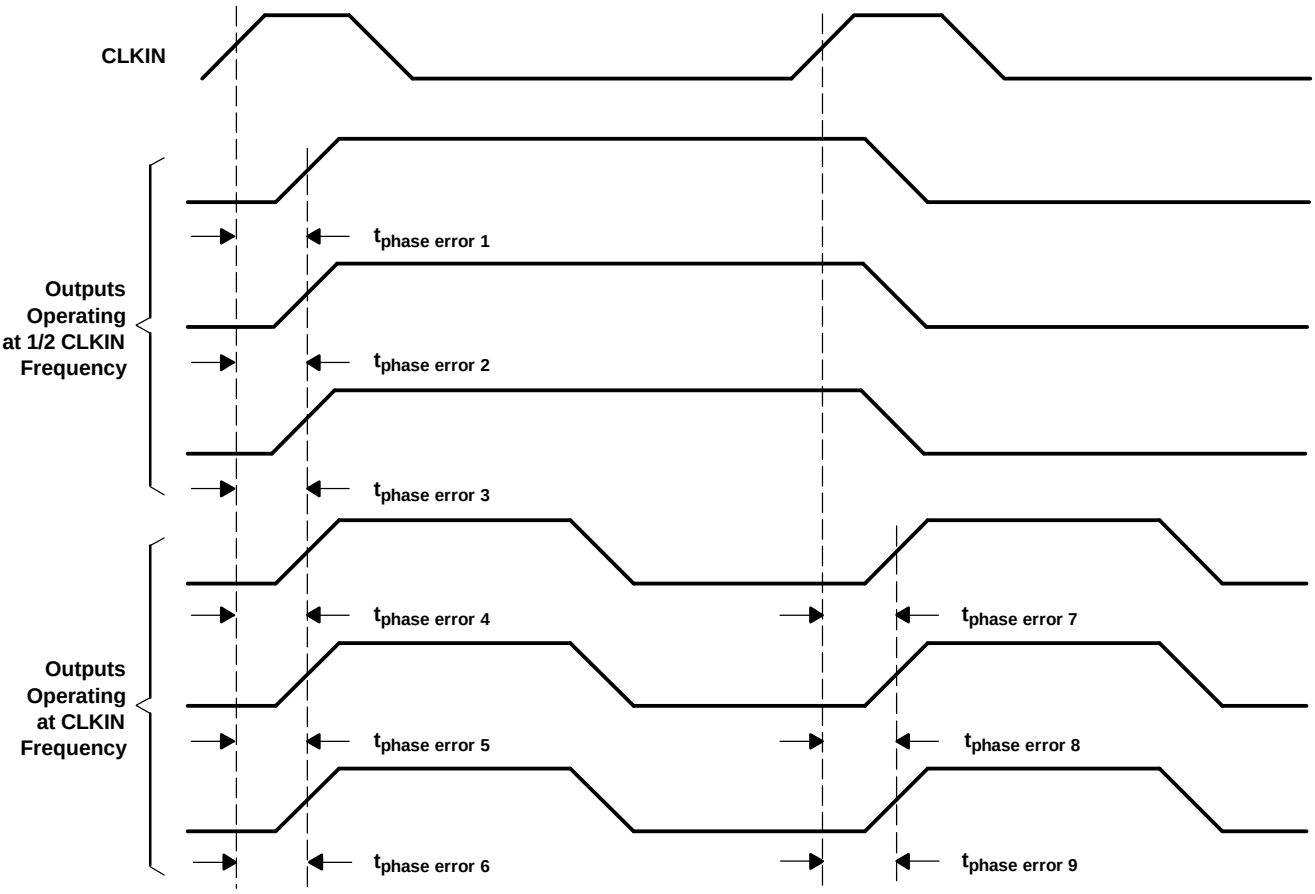


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

A. NOTES: . C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 100 MHz, Z_O = 50 Ω, t_r≤ 2.5 ns, t_f≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

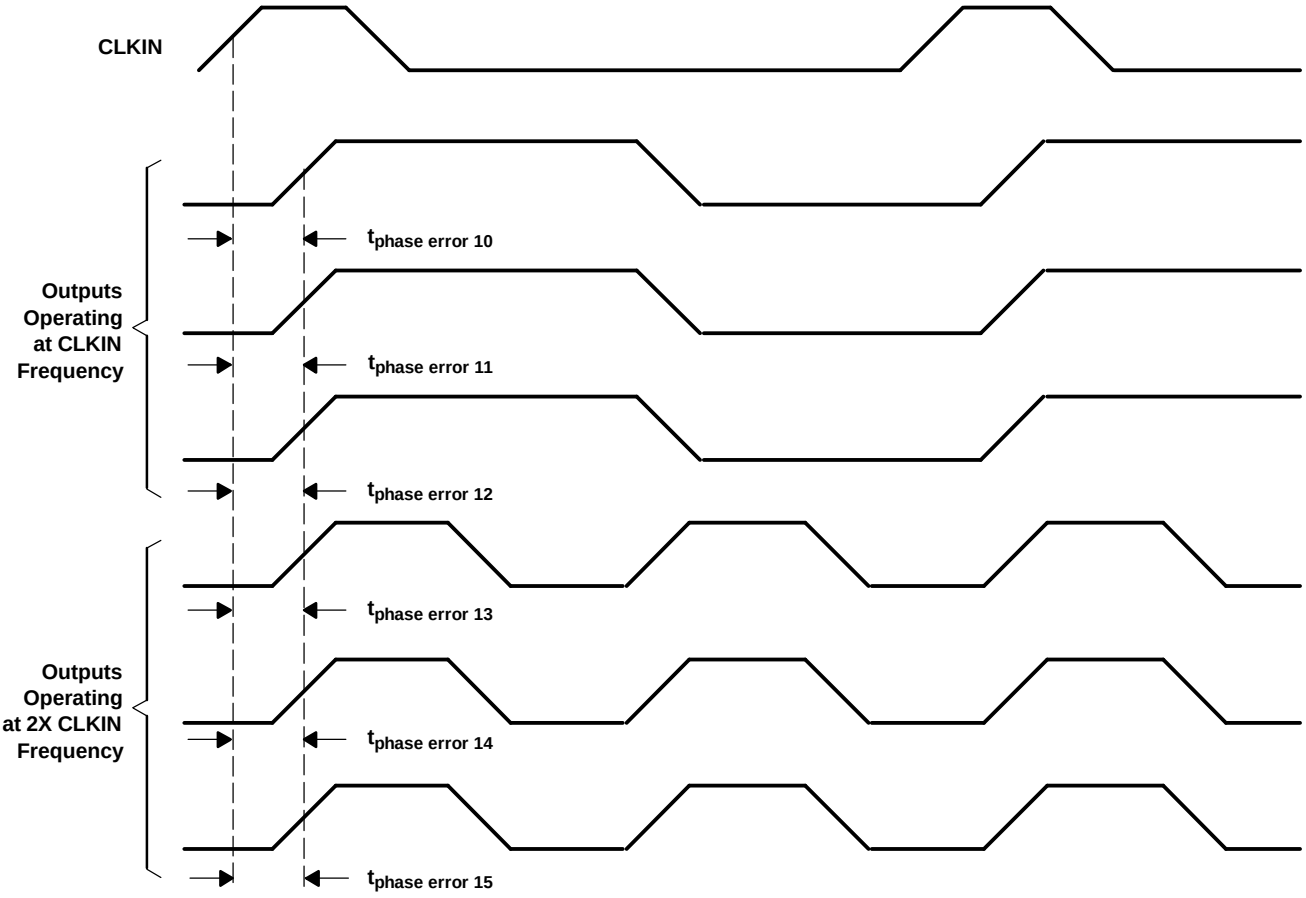


A. NOTES: . Output skew, $t_{sk(o)}$, is calculated as the greater of:
   - The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
   - The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
   - The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions
   - The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculations of $t_{sk(o)}$ and $t_{sk(pr)}$

PARAMETER MEASUREMENT INFORMATION (continued)



A. NOTES: . Output skew, $t_{sk(o)}$, is calculated as the greater of:
   - The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
   - The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions.

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC2536DB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2536
CDC2536DB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2536
CDC2536DBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2536
CDC2536DBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2536

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

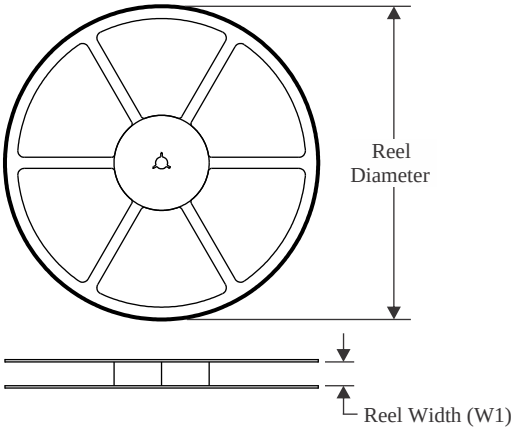
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

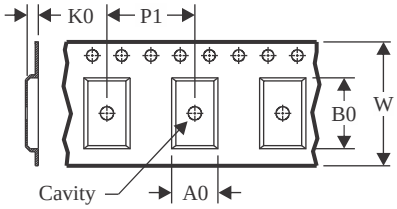
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

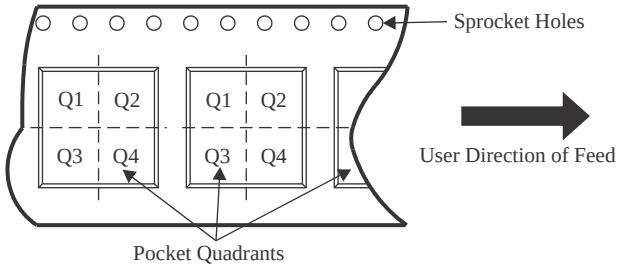


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

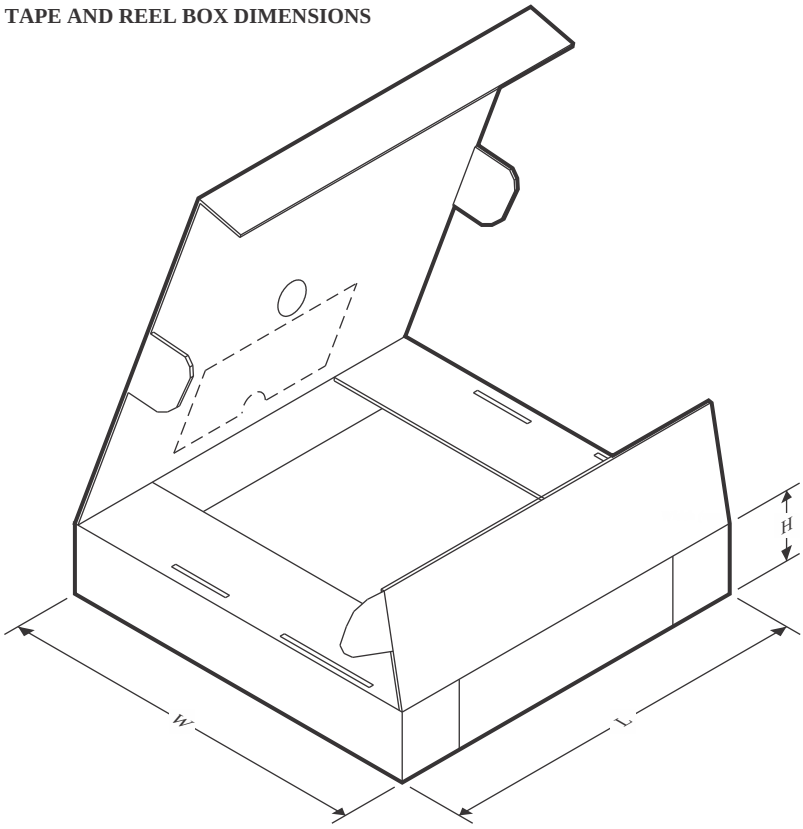
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC2536DBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

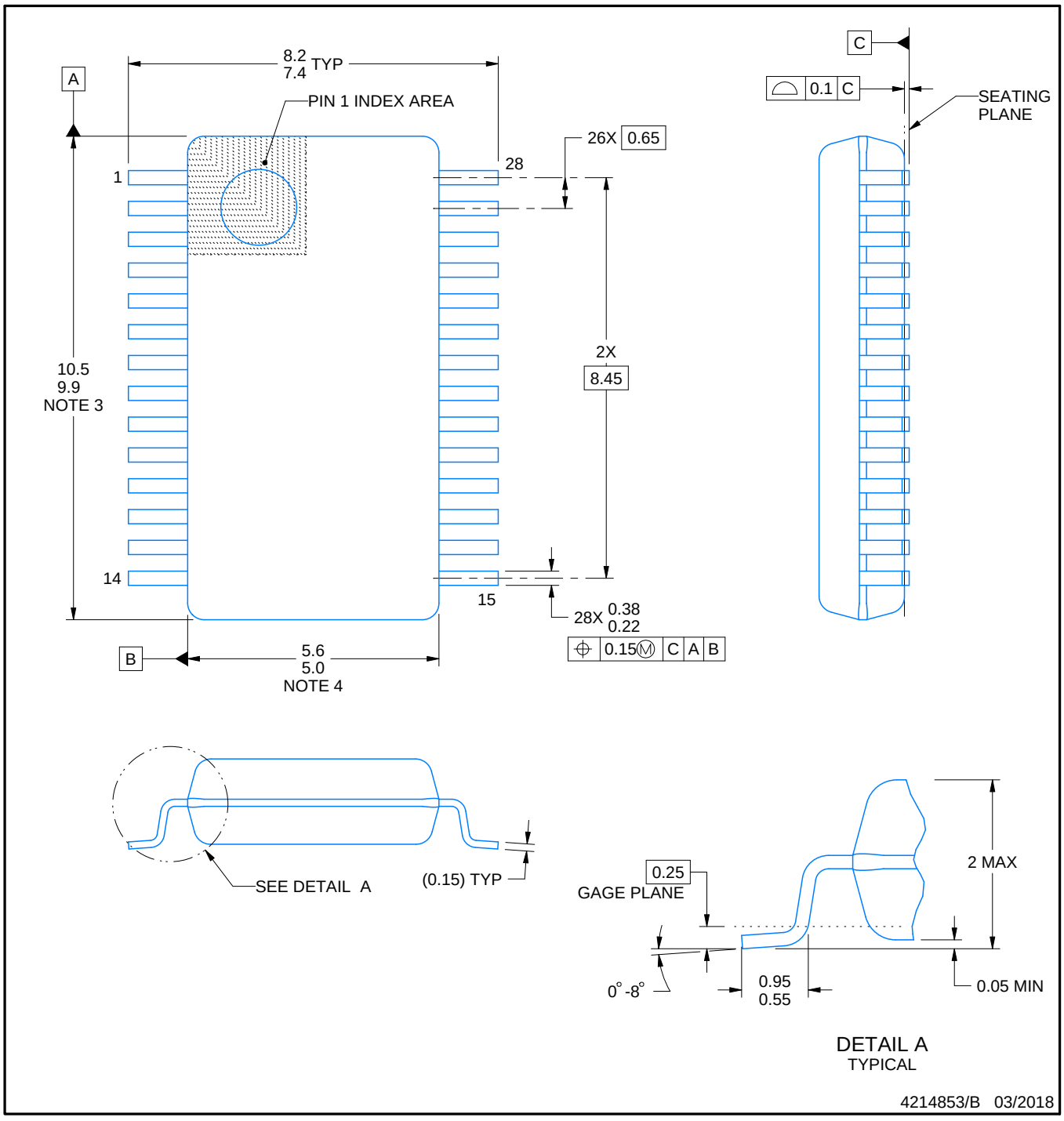
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC2536DBR	SSOP	DB	28	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DB0028A

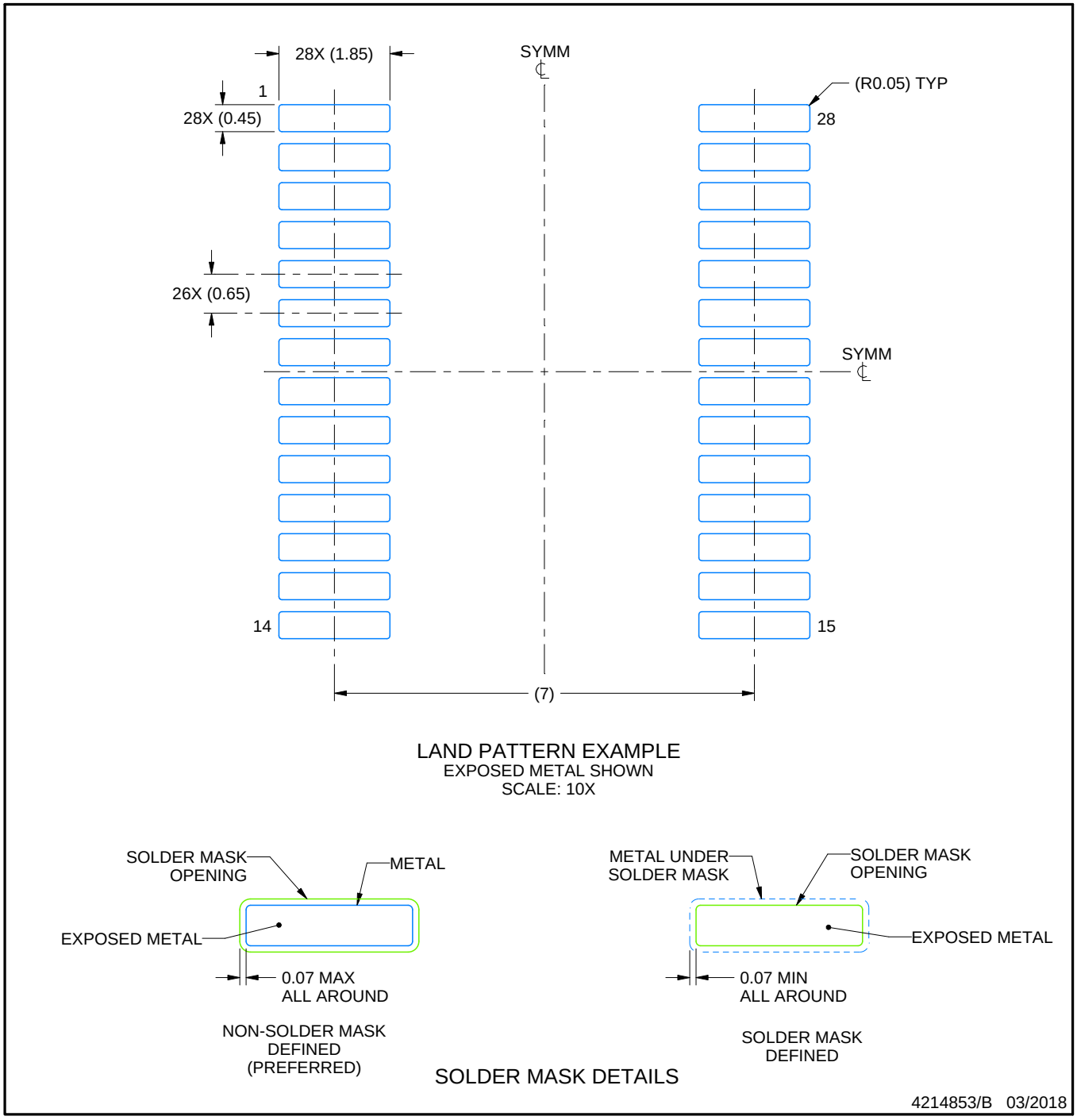
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



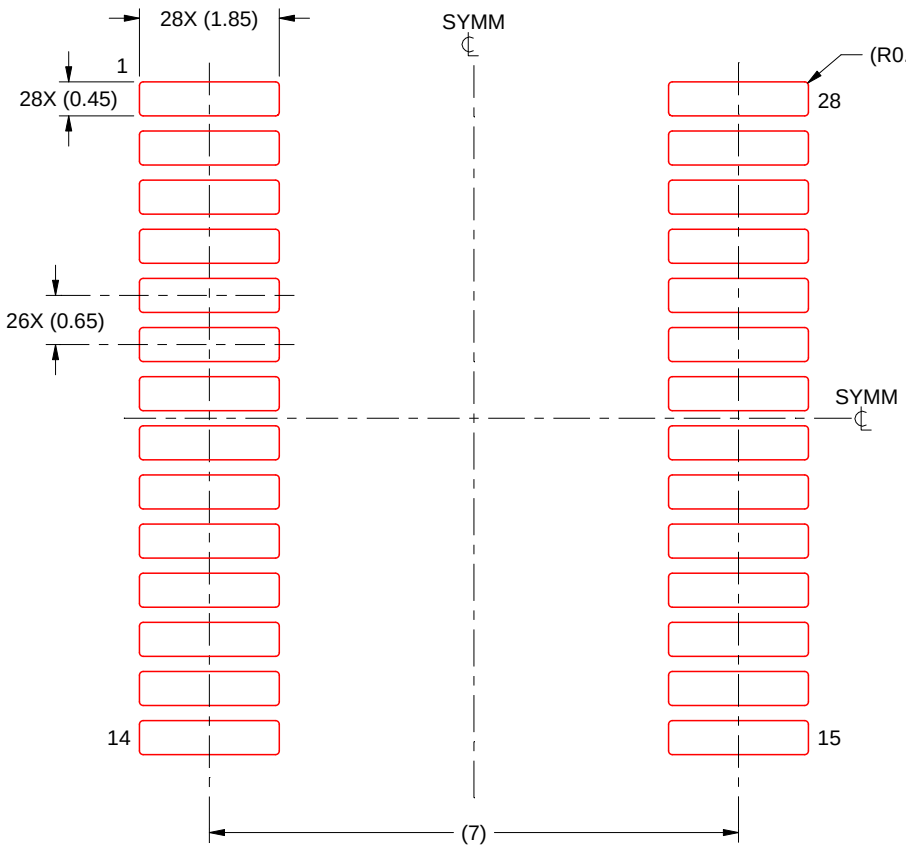
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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