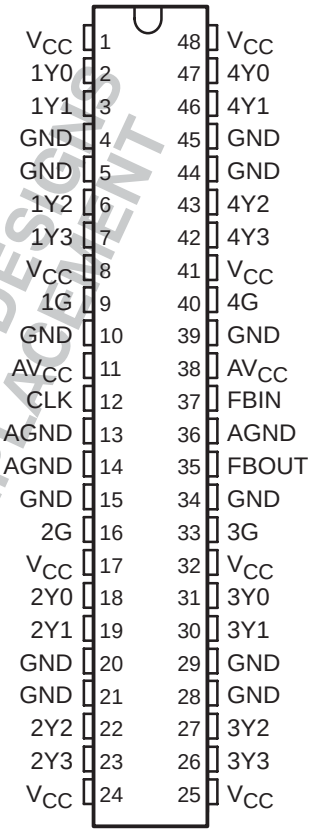
- **Use *CDCVF2510A* as a Replacement for this Device**
- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to Four Banks of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **No External RC Network Required**
- **Operates at 3.3-V V_{CC}**
- **Packaged in Plastic 48-Pin Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

The CDC516 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC516 operates at 3.3-V V_{CC} and is designed to drive up to five clock loads per output.

Four banks of four outputs provide 16 low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the 1G, 2G, 3G, and 4G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC516 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC516 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL may be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC516 is characterized for operation from 0°C to 70°C.

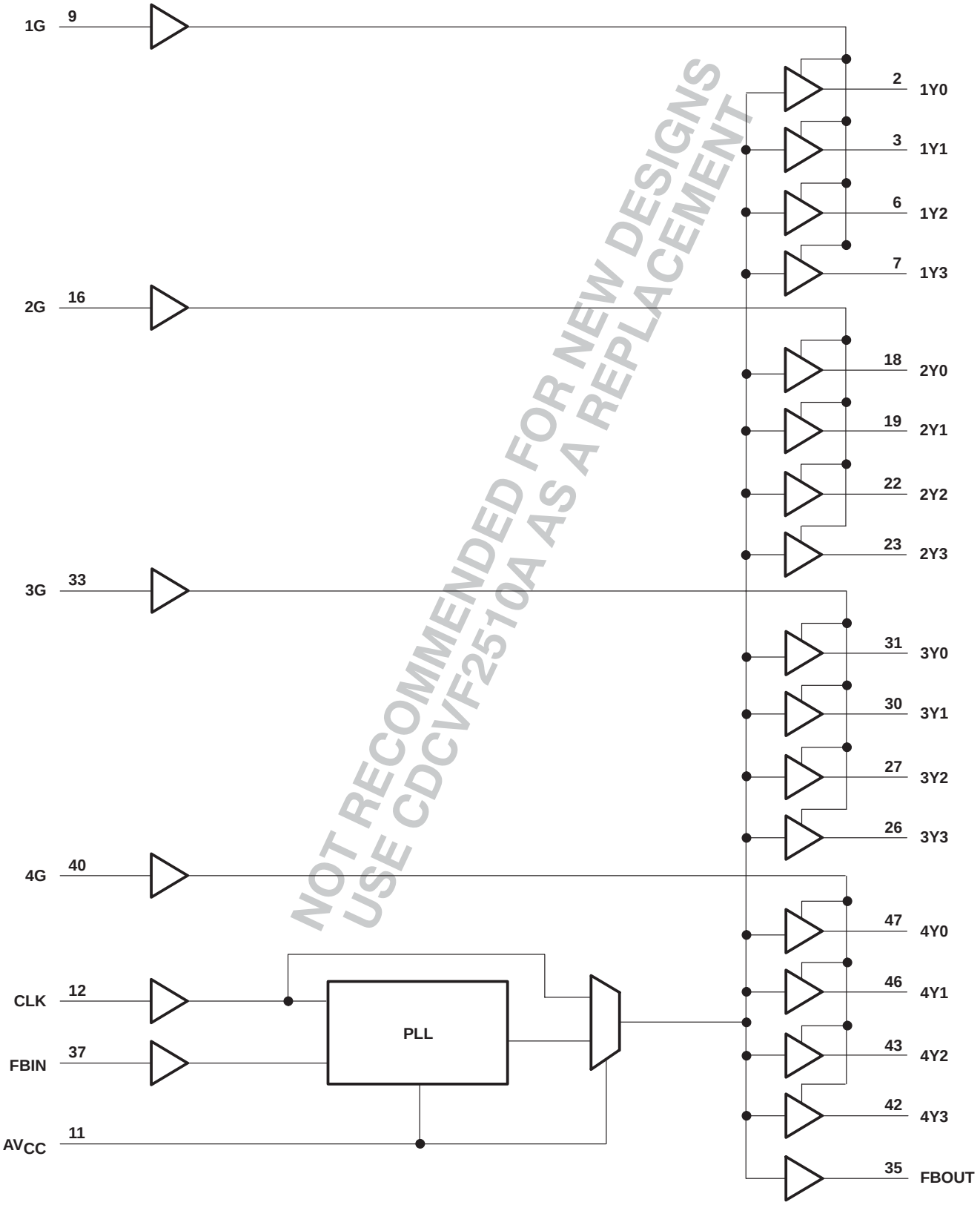
FUNCTION TABLE

INPUTS					OUTPUTS				
1G	2G	3G	4G	CLK	1Y (0:3)	2Y (0:3)	3Y (0:3)	4Y (0:3)	FBOUT
X	X	X	X	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	H
L	L	L	H	H	L	L	L	H	H
L	L	H	L	H	L	L	H	L	H
L	L	H	H	H	L	L	H	H	H
L	H	L	L	H	L	H	L	L	H
L	H	L	H	H	L	H	L	H	H
L	H	H	L	H	L	H	H	L	H
L	H	H	H	H	L	H	H	H	H
H	L	L	L	H	H	L	L	L	H
H	L	L	H	H	H	L	L	H	H
H	L	H	L	H	H	L	H	L	H
H	L	H	H	H	H	L	H	H	H
H	H	L	L	H	H	H	L	L	H
H	H	L	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 70°C	CDC516DGGR

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	12	I	Clock input. CLK provides the clock signal to be distributed by the CDC516 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	37	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	9	I	Output bank enable. 1G is the output enable for outputs 1Y(0:3). When 1G is low, outputs 1Y(0:3) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:3) are enabled and switch at the same frequency as CLK.
2G	16	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic-low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
3G	33	I	Output bank enable. 3G is the output enable for outputs 3Y(0:3). When 3G is low, outputs 3Y(0:3) are disabled to a logic-low state. When 3G is high, all outputs 3Y(0:3) are enabled and switch at the same frequency as CLK.
4G	40	I	Output bank enable. 4G is the output enable for outputs 4Y(0:3). When 4G is low, outputs 4Y(0:3) are disabled to a logic-low state. When 4G is high, all outputs 4Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	35	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:3)	2, 3, 6, 7	O	Clock outputs. These outputs provide low-skew copies of CLK. Outputs 1Y(0:3) are enabled via 1G. These outputs can be disabled to a logic-low state by deasserting the 1G control input.
2Y(0:3)	18, 19, 22, 26	O	Clock outputs. These outputs provide low-skew copies of CLK. Outputs 2Y(0:3) are enabled via 2G. These outputs can be disabled to a logic-low state by deasserting the 2G control input.
3Y(0:3)	31, 30, 27, 26	O	Clock outputs. These outputs provide low-skew copies of CLK. Outputs 3Y(0:3) are enabled via 3G. These outputs can be disabled to a logic-low state by deasserting the 3G control input.
4Y(0:3)	47, 46, 43, 42	O	Clock outputs. These outputs provide low-skew copies of CLK. Outputs 4Y(0:3) are enabled via 4G. These outputs can be disabled to a logic-low state by deasserting the 4G control input.
AV_{CC}	11, 38	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, the PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	13, 14, 36	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	1, 8, 17, 24, 25, 32, 41, 48	Power	Power supply
GND	4, 5, 10, 15, 20, 21, 28, 29, 34, 39, 44, 45	Ground	Ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 0.85 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−20	mA
I_{OL}	Low-level output current		20	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	I_I = −18 mA		3 V			−1.2	V
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC} −0.2			V
	I_{OH} = −20 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 20 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
I_{CC}§	V_I = V_{CC} or GND	I_O = 0, Outputs: low or high	3.6 V			20	µA
ΔI_{CC}	One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	V_I = V_{CC} or GND		3.3 V		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		6		pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ For I_{CC} of AV_{CC}, see Figure 5. For dynamic digital I_{CC}, see Figure 6.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clock}	Clock frequency	25	125	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time†		1	ms

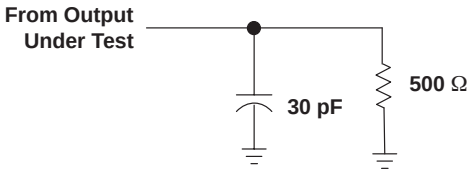
† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 5 and Figures 1 and 2)‡

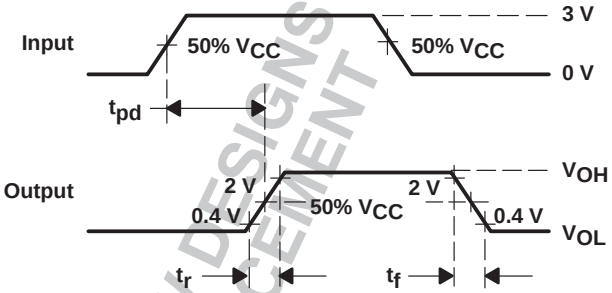
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.165 V			V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{phase\ error}$ reference (see Figure 3)	66 MHz < CLKIN↑ < 100 MHz	FBIN↑					−80...400		ps
$t_{phase\ error,\ -\ jitter,}$ (see Note 6)	CLKIN↑ = 100 MHz	FBIN↑	170		360		240		ps
$t_{sk(o)}$§	Any Y or FBOUT	Any Y or FBOUT						200	ps
$Jitter_{(pk-pk)}$	F(clkin > 66 MHz)	Any Y or FBOUT				−100		100	ps
Duty cycle	F(clkin ≤ 66 MHz)	Any Y or FBOUT				45%		55%	
	F(clkin > 66 MHz)	Any Y or FBOUT				43%		57%	
t_r		Any Y or FBOUT		1.1	1.5	0.7		1.6	ns
t_f		Any Y or FBOUT		0.8	1.3	0.5		1.5	ns

‡ These parameters are not production tested.
§ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
NOTES: 5. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
6. Phase error does not include jitter. The total phase error is 70 ps to 460 ps for the 5% V_{CC} range.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

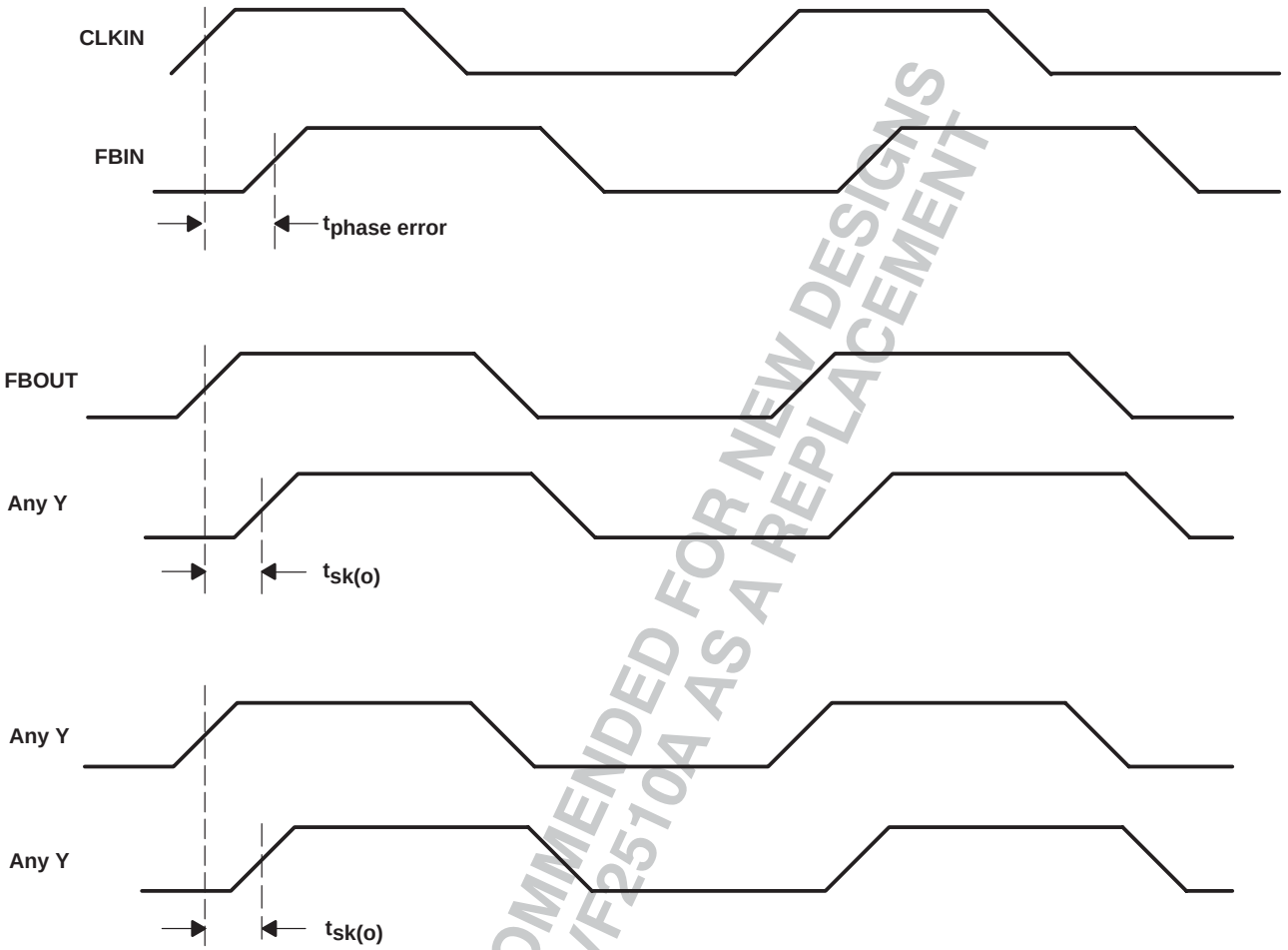


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

PHASE ERROR
vs
CLOCK FREQUENCY

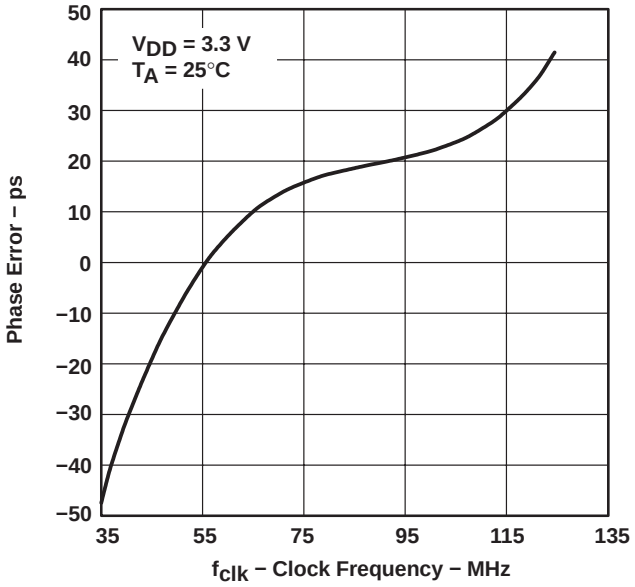


Figure 3

OUTPUT DUTY CYCLE
vs
CLOCK FREQUENCY

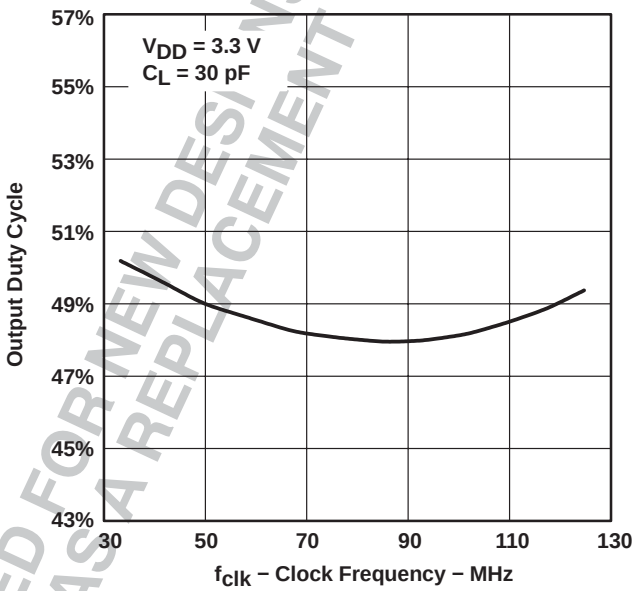


Figure 4

ANALOG SUPPLY CURRENT
vs
CLOCK FREQUENCY

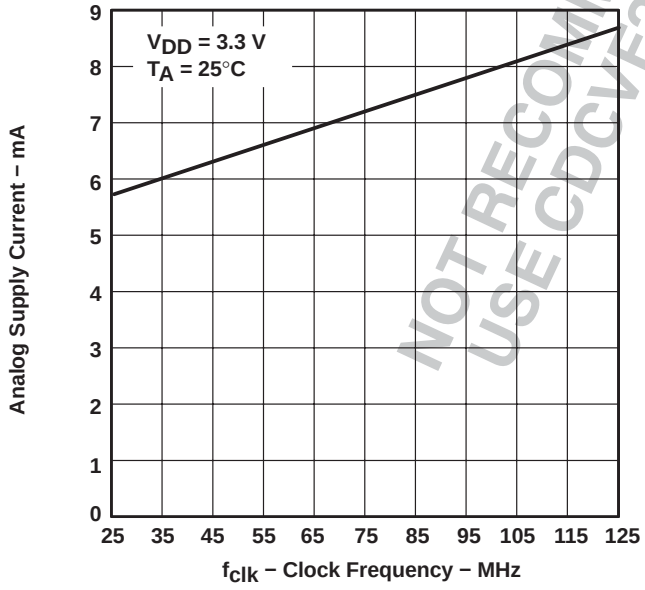


Figure 5

DYNAMIC SUPPLY CURRENT
vs
CLOCK FREQUENCY

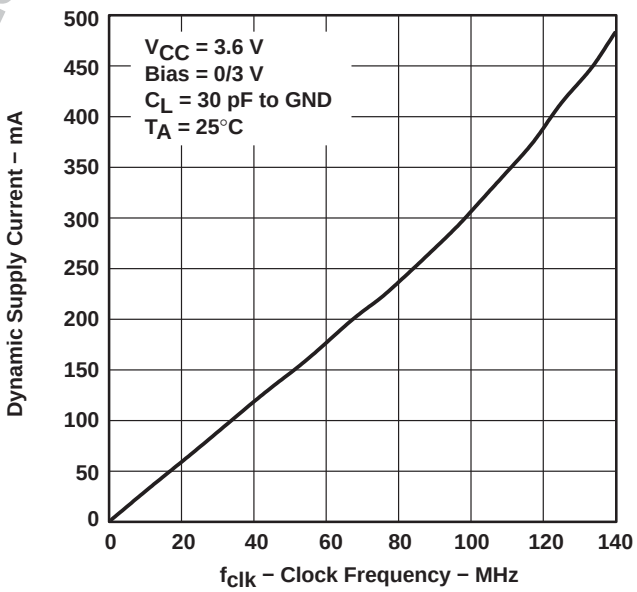


Figure 6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC516DGG	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC516
CDC516DGG.B	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC516
CDC516DGGG4	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC516
CDC516DGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC516
CDC516DGGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC516

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

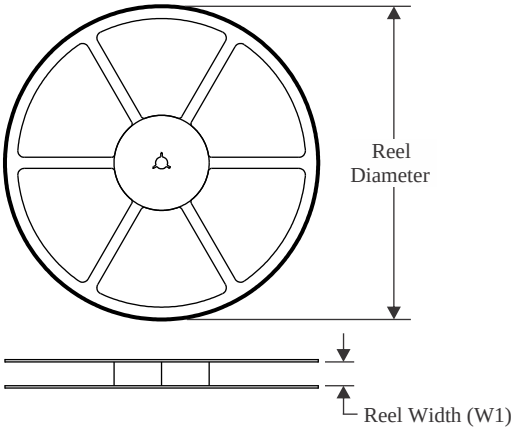
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

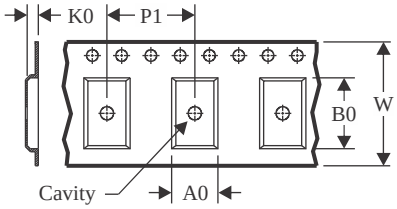
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

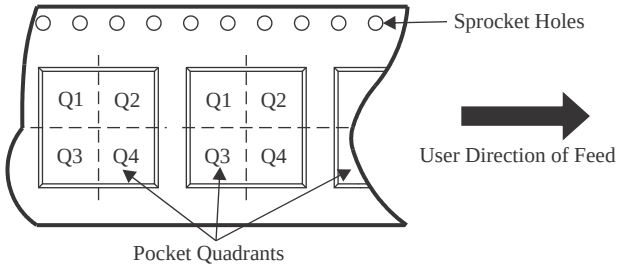


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

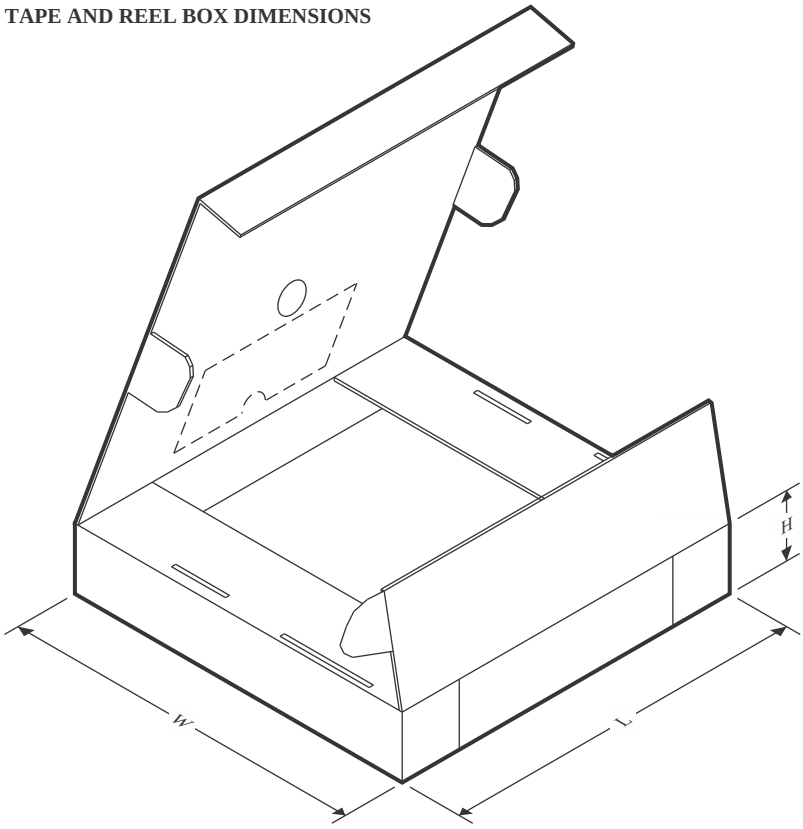
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC516DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

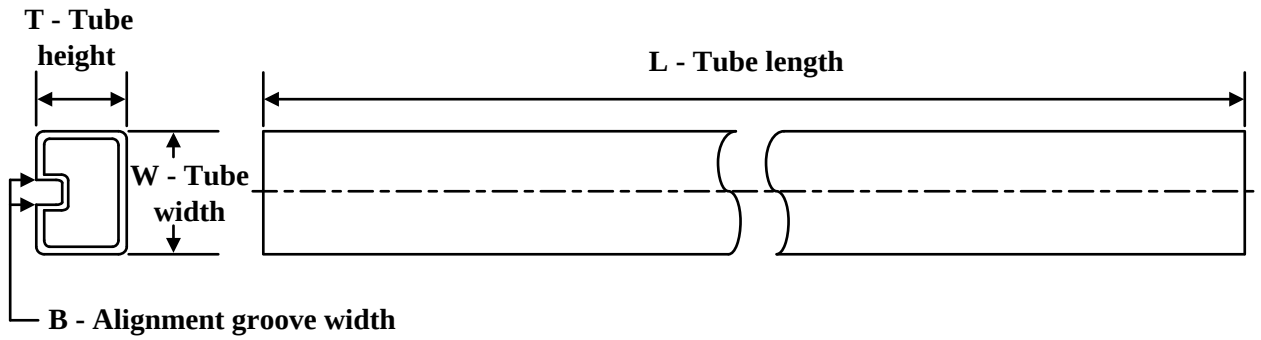
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

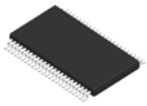
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC516DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC516DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
CDC516DGG.B	DGG	TSSOP	48	40	530	11.89	3600	4.9
CDC516DGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9

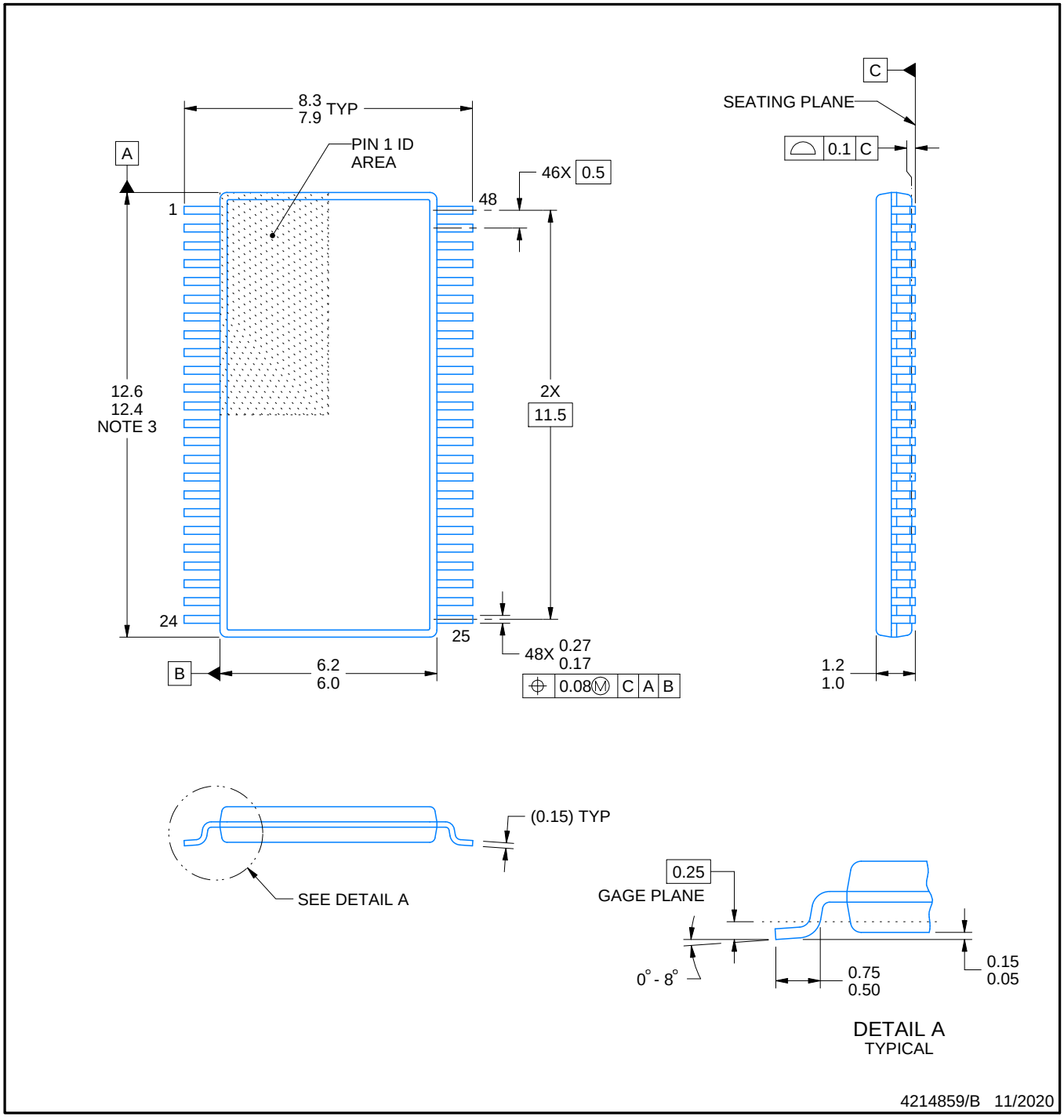


PACKAGE OUTLINE

DGG0048A

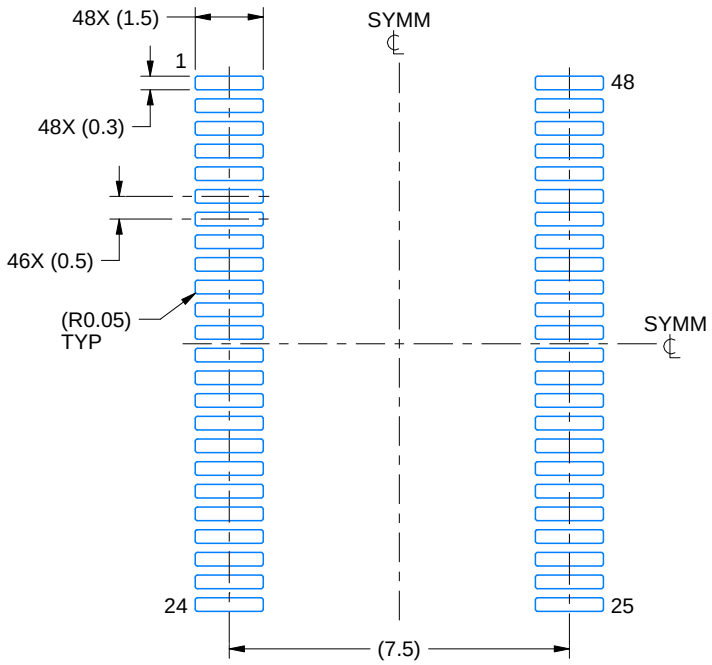
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

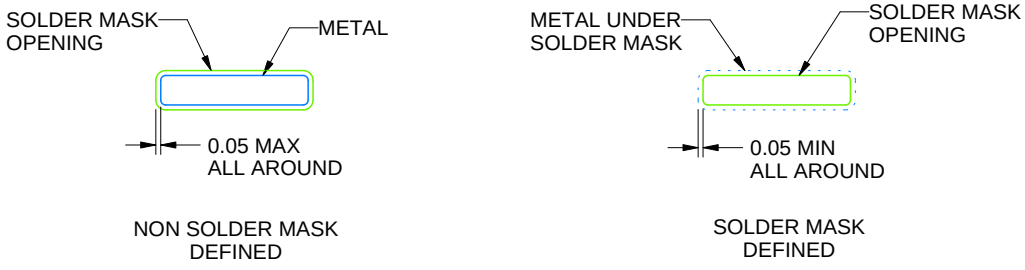


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

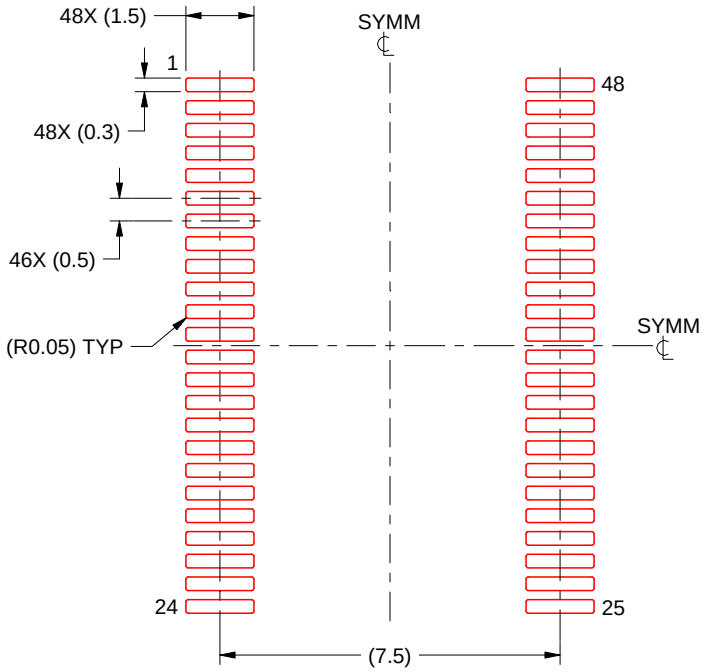


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

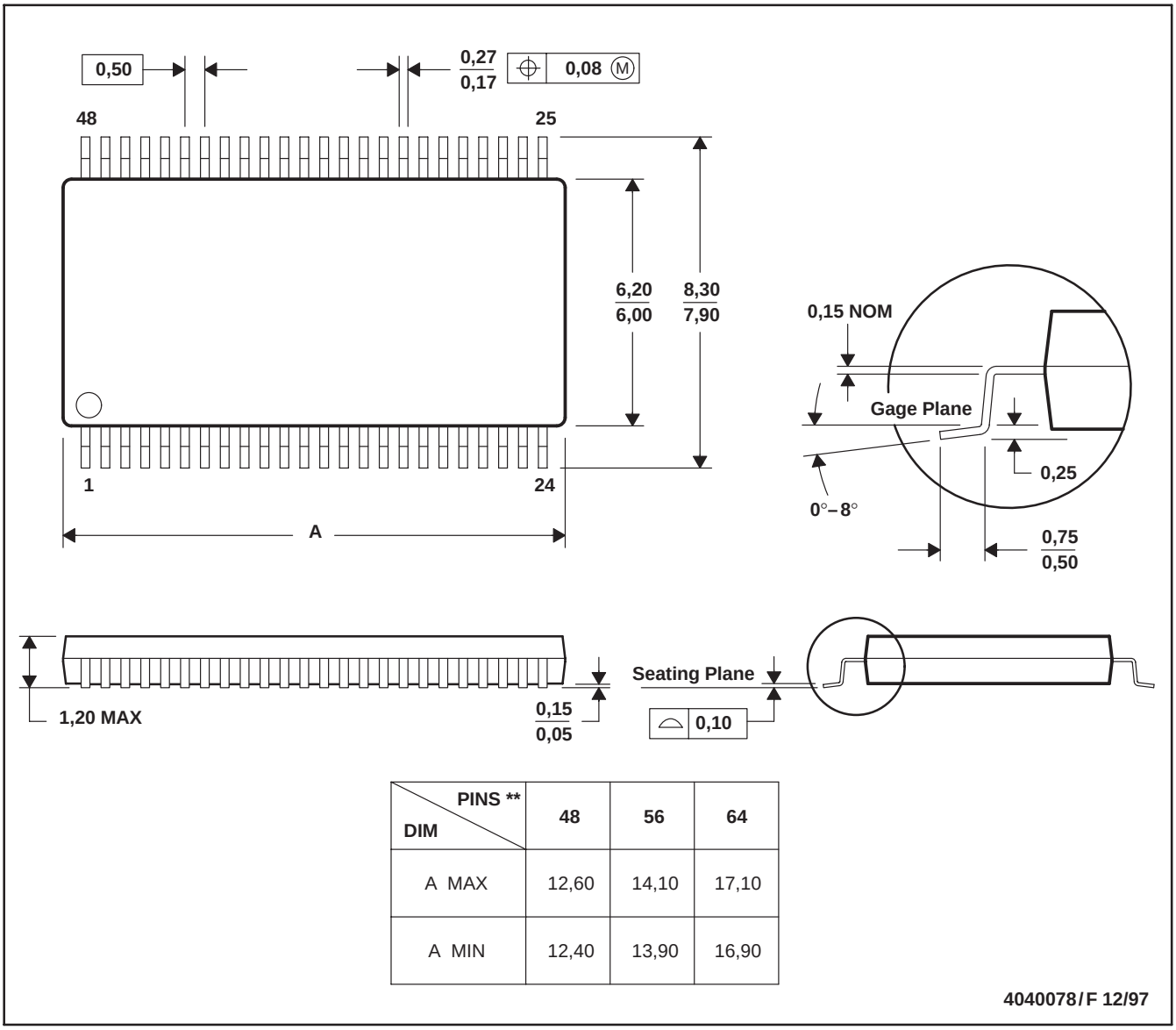
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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