CDC6Cx-Q1 Low Power LVCMOS Output BAW Oscillator

1 Features

- AEC Q-100 qualified:
  - Device temperature grade 1: –40°C to +125°C
- Functional Safety-Capable:
  - Documentation available to aid functional safety system design
- LVCMOS output oscillator supporting frequency range from 250kHz to 200MHz
- Supply voltage supports 1.8V to 3.3V ±10%.
- Very low power consumption: 4.57mA typical and 7.9mA maximum for 25MHz at 1.8V
- Stand by current 1.5µA typical at 1.8V helps for battery powered applications
- Low jitter: < 750fs RMS jitter for F_{out} ≥ 10MHz
- Smallest industry wettable flank standard package: 1.60mm × 1.20mm (DLY), 2.00mm × 1.60mm (DLR), 2.5mm × 2.00mm (DLF), 3.20mm × 2.5mm (DLN)
  - Universal land pattern footprint under *Mechanical, Packaging, and Orderable Information*
- Integrated LDO for robust supply noise immunity
- Start-up time < 3ms
  - Contact TI for different start-up times.
- Orderable options for slow rise and fall time for EMI reduction
- Supported frequencies (MHz):
  - 1.2, 2.048, 4, 5.12, 6.78, 8, 8.192, 10, 12, 12.288, 16, 19.2, 20, 24, 24.576, 25, 26, 27, 30, 33.33, 33.333, 38.4, 40, 48, 50, 66.666, 76.8, 100, 125, 156.25, and more
- Contact TI representative for any frequency and samples needed.

2 Applications

- ADAS, Automotive Camera, Sensor fusion, automotive radar, ECU
- Automotive Gateway, Body Control Modules
- Automotive infotainment and cluster, Head Units, Digital cockpit controllers, telematics
- Crystal oscillator replacement
- FPGA, MCU, Processor and ASIC clocking

3 Description

Texas Instruments' high-precision bulk-acoustic wave (BAW) micro-resonator technology is integrated directly into a package allowing for low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

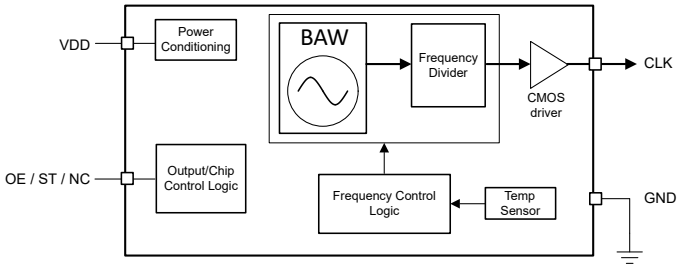
The CDC6Cx-Q1 device is a low jitter, low-power, fixed-frequency oscillator which incorporates the BAW as the resonator source. The device is factory-programmed per specific frequency and function pin. With a frequency control logic and output frequency divider, the CDC6Cx-Q1 can produce any frequency within the specified range, providing one device family for all frequency needs.

The high-performance clocking, mechanical stability, lower power consumption, flexibility, and small package options for this device are designed for reference clock and core clocks in automotive applications.

Packaging Information

PART NUMBER	OUTPUT TYPE	PACKAGE(1)	PACKAGE SIZE(2)
CDC6Cx-Q1	LVCMOS	VSON (DLN, 4)	3.20mm × 2.50mm
		VSON (DLF, 4)	2.50mm × 2.00mm
		VSON (DLR, 4)	2.00mm × 1.60mm
		VSON (DLY, 4)	1.60mm × 1.20mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



CDC6Cx-Q1 Simplified Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison....3
5 Pin Configuration and Functions....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Environmental Compliance....5
6.4 Recommended Operating Conditions....5
6.5 Thermal Information....6
6.6 Electrical Characteristics....6
6.7 Timing Diagrams....8
6.8 Typical Characteristics....10
7 Parameter Measurement Information....12
7.1 Device Output Configurations....12
8 Detailed Description....13
8.1 Overview....13
8.2 Functional Block Diagram....13
8.3 Feature Description....13
9 Application and Implementation....19
9.1 Application Information....19
9.2 Typical Application....19
9.3 Power Supply Recommendations....24
9.4 Layout....25
10 Device and Documentation Support....31
10.1 Documentation Support....31
10.2 Receiving Notification of Documentation Updates....31
10.3 Support Resources....31
10.4 Trademarks....31
10.5 Electrostatic Discharge Caution....31
10.6 Glossary....31
11 Revision History....31
12 Mechanical, Packaging, and Orderable Information....33

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4 Device Comparison

Use the *CDC6C OPN Decoder* to understand the device nomenclature of the CDC6Cx-Q1 orderable options. The *CDC6C OPN Decoder* provides a quick summary of how to decode the frequency, package information and a list of the CDC6Cx-Q1 orderable part numbers (OPNs) with associated configurations, packaging information, and device top marking.

Section 8.3.5.1 explains the different normal and slow mode options and Section 8.3.3 explains stand by and output enable options.

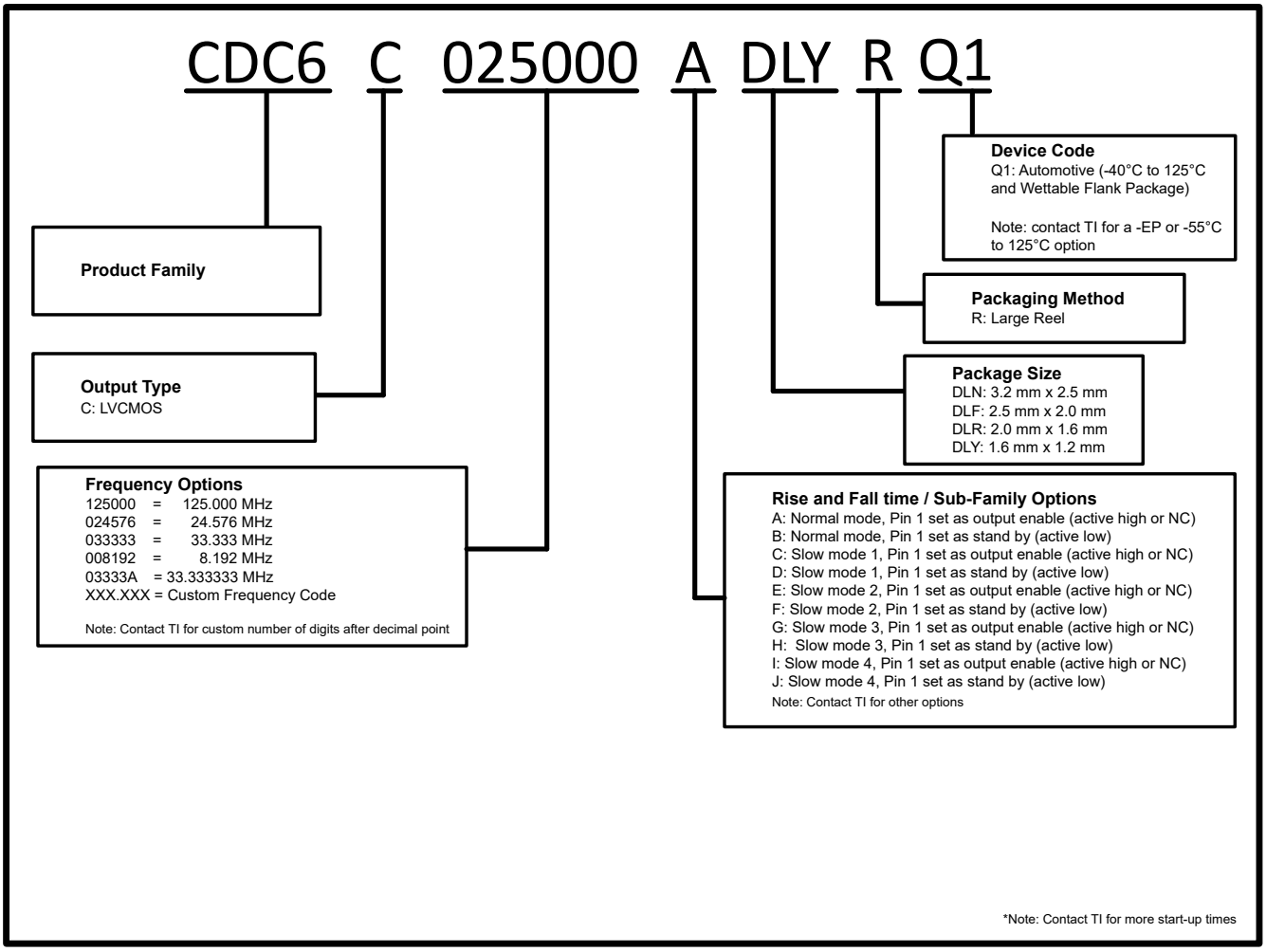

Figure 4-1. Part Number Guide: CDC6Cx-Q1

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

5 Pin Configuration and Functions

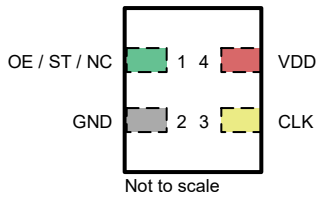

Figure 5-1. CDC6Cx-Q1 4-Pin VSON (Top View)

Legend	
Input	Power
Ground	Output

Table 5-1. CDC6Cx-Q1 Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
OE / ST / NC	1	I / NC	Output Enable (OE) or Stand By (ST) pin on No Connect (NC). See the *Function Pin Descriptions* for more details.
GND	2	G	Device ground
CLK	3	O	LVCMOS output clock
VDD	4	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage(2)	–0.3	3.63	V
EN	Logic input voltage	–0.3	3.63	V
CLK	Clock output voltage	–0.3	3.63	V
T_J	Junction temperature		130	℃
T_{STG}	Storage temperature	–65	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For all devices with the recommended operating voltage of 1.8V ±10%, 2.5V ±10% and 3.3V ±10%

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, HBM ESD Classification Level 2(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4A(1)	±750	V

(1) For Automotive Grade device

6.3 Environmental Compliance

		VALUE	UNIT
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007, Condition A	20	g
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Moisture Sensitivity Level (MSL)		MSL1	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage(1)	1.62	1.8, 2.5, 3.3	3.63	V
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature			130	°C
t_{RAMP}	V_{DD} power-up ramp time(2)	0.1		100	ms

(1) For all devices with the recommended operating voltage of 1.8V ±10%, 2.5V ±10% and 3.3V ±10%
(2) V_{DD} power-up ramp time is defined as minimum time taken for power supply to exceed 95% of nominal VDD. Monotonic power supply ramp is assumed.

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6.5 Thermal Information

THERMAL METRIC(1)	DEVICE				UNIT
	DLN (VSON)	DLF (VSON)	DLR (VSON)	DLY (VSON)	
	4-PIN	4-PIN	4-PIN	4-PIN	
Junction-to-ambient thermal resistance	151	151.7	178.3	189.1	°C/W
Junction-to-case (top) thermal resistance	88.6	99.3	114.6	137.3	°C/W
Junction-to-board thermal resistance	71.2	64.4	82.7	85	°C/W
Junction-to-top characterization parameter	11.1	9.2	8.5	6.2	°C/W
Junction-to-board characterization parameter	70.2	63.5	81.1	83.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Electrical Characteristics

over the recommended operating conditions (V_{DD} = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10%; typical values are at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD}	Device current consumption (excluding load current)	-40°C to 125°C, F_{out} = 20MHz, Vdd = 1.8V±10%		4.22	7.8	mA
		-40°C to 125°C, F_{out} = 20MHz, Vdd = 3.3V±10%		4.41	7.9	mA
I_{DD}	Device current consumption (excluding load current)	-40°C to 125°C, F_{out} = 25MHz, Vdd = 1.8V±10%		4.32	7.9	mA
		-40°C to 125°C, F_{out} = 25MHz, Vdd = 3.3V±10%		4.57	8	mA
I_{DD}	Device current consumption (excluding load current)	-40°C to 125°C, F_{out} = 50MHz, Vdd = 1.8V±10%		4.84	8.2	mA
		-40°C to 125°C, F_{out} = 50MHz, Vdd = 3.3V±10%		5.33	8.3	mA
I_{DD}	Device current consumption (excluding load current)	-40°C to 125°C, F_{out} = 100MHz, Vdd = 1.8V±10%		5.86	8.7	mA
		-40°C to 125°C, F_{out} = 100MHz, Vdd = 3.3V±10%		6.77	8.9	mA
I_{DD}	Device current consumption (excluding load current)	-40°C to 125°C, F_{out} = 150MHz, Vdd = 1.8V±10%		7.14	10.0	mA
		-40°C to 125°C, F_{out} = 150MHz, Vdd = 3.3V±10%		8.72	11.5	mA
I_{DD_stdby}	Device standby current	-40°C to 125°C, ST = GND, Vdd=1.8V±10%		1.5		µA
		-40°C to 125°C, ST = GND, Vdd=2.5V±10%		2		µA
		-40°C to 125°C, ST = GND, Vdd=3.3V±10%		2.7		µA
I_{DD-OD}	Device current with output disabled	-40°C to 125°C, F_{out} = 25MHz, Vdd = 1.8V±10%		3.75	7.5	mA
		-40°C to 125°C, F_{out} = 25MHz, Vdd = 3.3V±10%		3.76	7.6	mA
Output Characteristics						
F_{out}	Output frequency		0.25		200	MHz
V_{OL}	Output low voltage	I_{OL} = 3.6mA, VDD = 1.8V			0.36	V
		I_{OL} = 5.0mA, VDD = 2.5V			0.5	V
		I_{OL} = 6.6mA, VDD = 3.3V			0.66	V
V_{OH}	Output high voltage	I_{OH} = 3.6mA, VDD = 1.8V	VDD × 0.88			V
		I_{OH} = 5.0mA, VDD = 2.5V	VDD × 0.85			V
		I_{OH} = 6.6mA, VDD = 3.3V	VDD × 0.85			V
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 2pF, normal mode, F_{out} = 25MHz		0.62	1.01	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 2pF, slow mode 1, F_{out} = 25MHz		0.81	1.06	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 5pF, normal mode, F_{out} = 25MHz		0.76	1.24	ns

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over the recommended operating conditions (V_{DD} = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10%; typical values are at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 5pF, slow mode 2, F_{out} = 25MHz		1.47	1.62	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 10pF, normal mode, F_{out} = 25MHz		1.4	1.7	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 10pF, slow mode 3, F_{out} = 25MHz		2.44	2.61	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 15pF, normal mode, F_{out} = 25MHz		1.88	2.11	ns
t_R/t_F	Output rise/fall time	20% to 80% of V_{OH}-V_{OL}, C_L = 15pF, slow mode 4, F_{out} = 25MHz		3.29	3.5	ns
t_R/t_F	Output rise/fall time	10% to 90% of V_{OH}-V_{OL}, no load, normal mode, F_{out} = 25MHz		0.42		ns
t_R/t_F	Output rise/fall time	10% to 90% of V_{OH} - V_{OL}, C_L = 15pF, normal mode, F_{out} = 25MHz		2.05		ns
t_R/t_F	Output rise/fall time	10% to 90% of V_{OH} - V_{OL}, C_L = 15pF, slow mode 4, F_{out} = 25MHz		3.81		ns
ODC	Output duty cycle		45	50	55	%
PN-Floor	Output phase noise floor (f_{OFFSET} > 10MHz)	F_{out} = 50MHz		–155		dBc/Hz
C_L	Maximum capacitive load	F_{out} < 50MHz			30	pF
C_L		F_{out} > 50MHz			15	pF
$R_{out-high}$	Output impedance			50		Ω
Function Pin Characteristics (OE/ST)						
V_{IL}	Input low voltage	VDD = 1.8V			0.45	V
		VDD = 2.5V			0.475	V
		VDD = 3.3V			0.5	V
V_{IH}	Input high voltage		1.3			V
I_{IL}	Input low current	EN = GND	–70			µA
I_{IH}	Input high current	EN = VDD			40	µA
C_{IN}	Input capacitance(1)			2		pF
Frequency Tolerance						
F_T	Total frequency stability	Inclusive of: solder shift, initial tolerance, variation over –40°C to 125°C, variation over supply voltage range, and 10 years aging at 25°C.			±25	ppm
F_T	Total frequency stability	Inclusive of: solder shift, initial tolerance, variation over –40°C to 125°C, variation over supply voltage range, and 1st year aging at 25°C.			±20	ppm
PSRR Characteristics						
PSRR	Spur induced by 50mV power supply ripple at 50MHz output, VDD = 2.5V/3.3V, no power supply decoupling capacitor	Sine wave at 50kHz		–80		dBc
		Sine wave at 100kHz		–75		dBc
		Sine wave at 500kHz		–63		dBc
		Sine wave at 1MHz		–59		dBc
Power-On Characteristics						
t_{START_UP}	Start-up time	Time elapsed from 0.95 × VDD until output is enabled and output is within specification. OE / ST = High; Tested with a power supply ramp time of 200µs		1.5	3	ms
t_{ST-EN}	Chip enable time	Time elapsed from standby (ST = V_{IH}) until output is enabled and output is within specification			3	ms
t_{ST-DIS}	Chip disable time	Time elapsed from standby (ST = V_{IL}) until chip is in standby mode			250	ns

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over the recommended operating conditions (V_{DD} = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10%; typical values are at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OE-EN}	Output enable time	Time elapsed from OE = V_{IH} until output is enabled and output is within specification. Output may be invalid during enable time.			250	ns
t_{OE-DIS}	Output disable Time	Time elapsed from OE = V_{IL} until output is disabled			250	ns
Clock Output Jitter						
R_J	Random phase jitter	10MHz ≤ F_{out} ≤ 40MHz, integration BW: 12kHz to 5MHz, maximum temperature = 125°C		340	750	fs
		40MHz < F_{out} ≤ 200MHz, integration BW: 12kHz to 20MHz, maximum temperature = 125°C		340	750	fs
SPN_{100k}	Spot phase noise at 1kHz offset	F_{out} = 100MHz		–86		dBc/Hz
SPN_{100k}	Spot phase noise at 10kHz offset	F_{out} = 100MHz		–120		dBc/Hz
SPN_{100k}	Spot phase noise at 100kHz offset	F_{out} = 100MHz		–138		dBc/Hz
SPN_{1M}	Spot phase noise at 1MHz offset	F_{out} = 100MHz		–143		dBc/Hz
$R_{JITT,RMS}$	RMS period jitter	F_{out} ≥ 25MHz		3		ps
$R_{JITT,PK}$	Peak-peak period jitter	F_{out} ≥ 25MHz		26		ps

(1) Proven by Design. Not characterised

6.7 Timing Diagrams

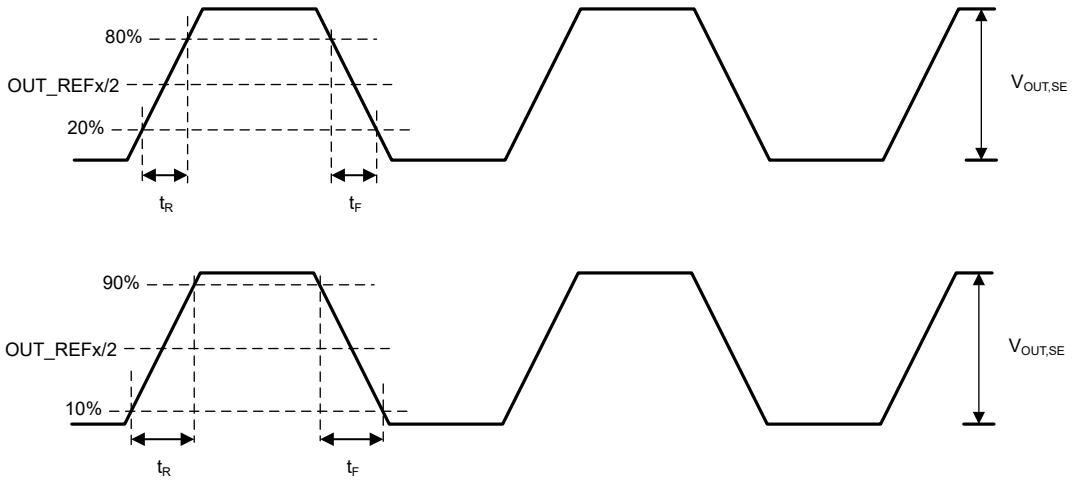

Figure 6-1. Single-Ended Output Voltage and Rise/Fall Time

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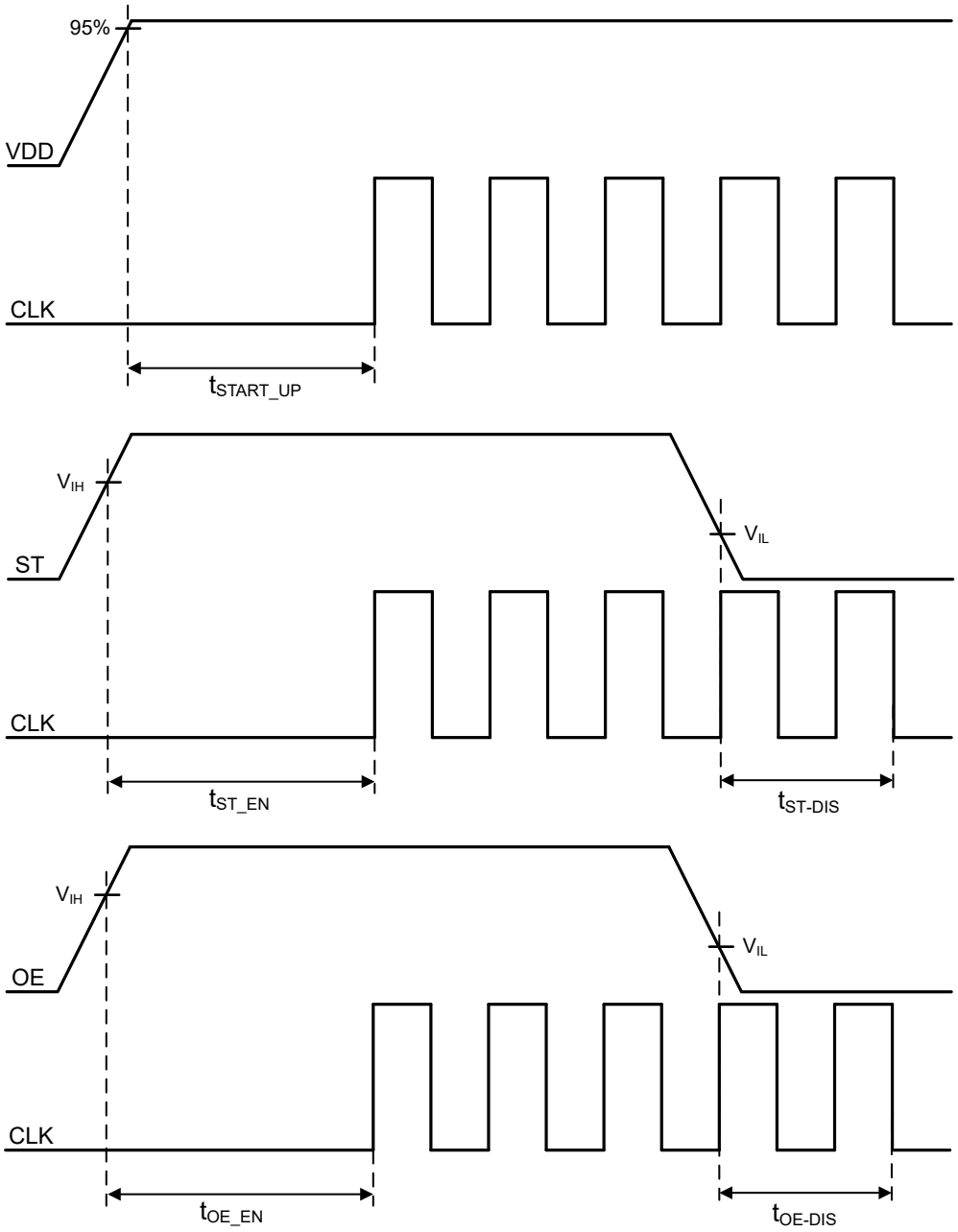

Figure 6-2. Power-On Characteristics

6.8 Typical Characteristics

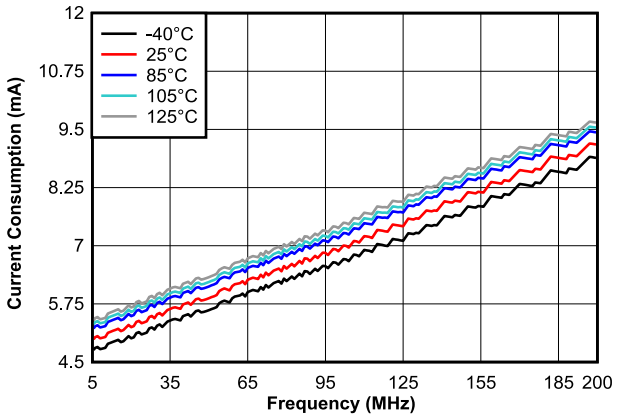

Figure 6-3. Current Consumption vs Frequency and Temperature at 1.8V Supply

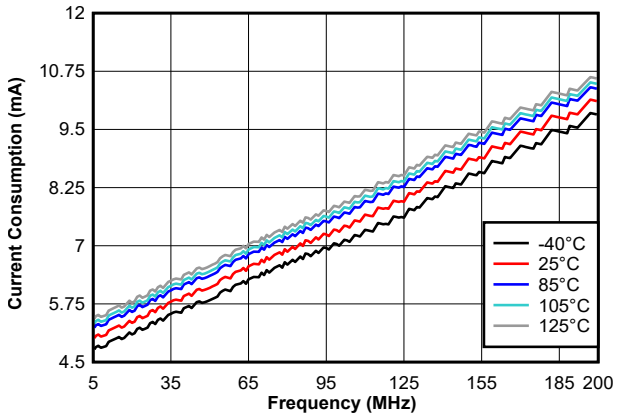

Figure 6-4. Current Consumption vs. Frequency and Temperature at 2.5V Supply

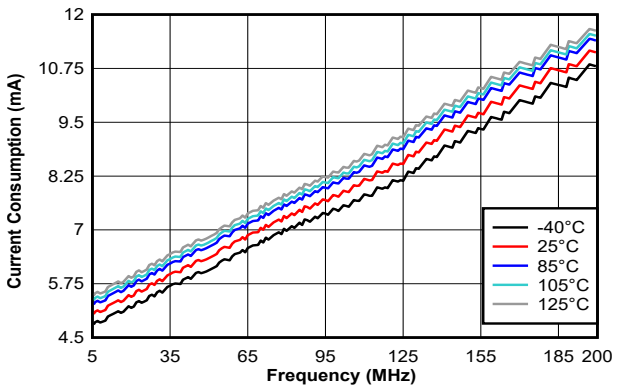

Figure 6-5. Current Consumption vs Frequency and Temperature at 3.3V Supply

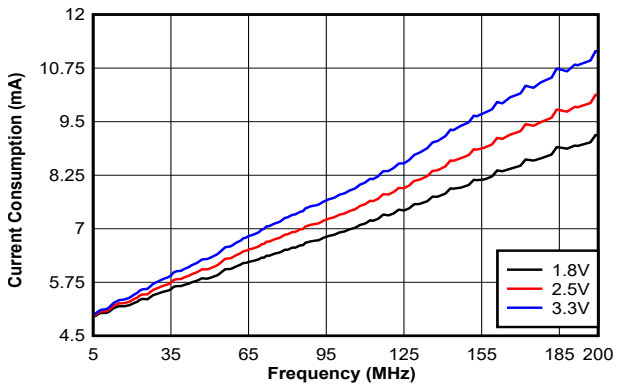

Figure 6-6. Current Consumption vs Frequency and Supply Voltage at 25°C

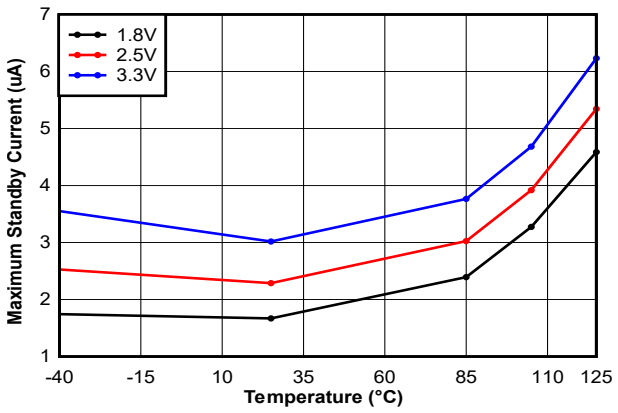

Figure 6-7. Maximum Standby Current vs Temperature and Supply Voltage

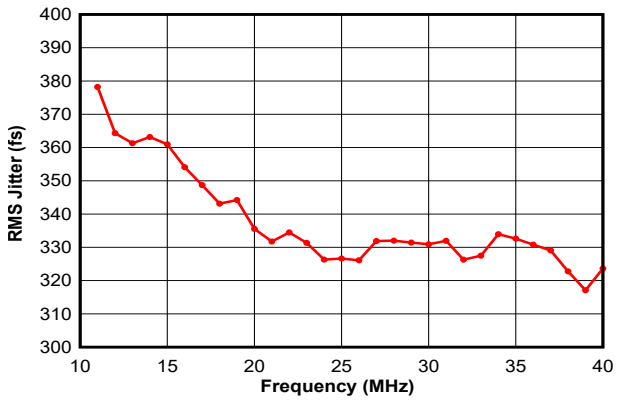

Figure 6-8. Typical RMS Jitter vs Frequency at 3.3V Supply and 25°C (BW 12kHz to 5MHz)

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6.8 Typical Characteristics (continued)

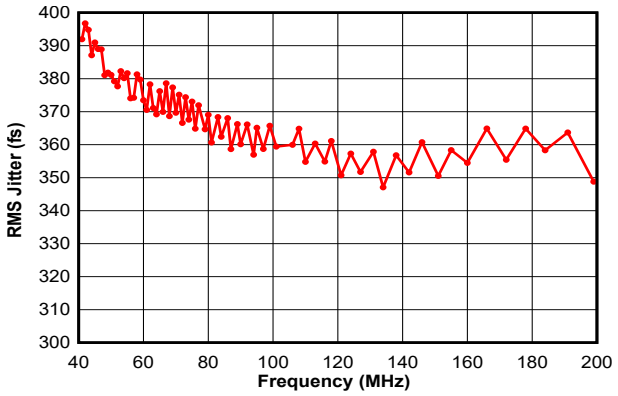

Figure 6-9. Typical RMS Jitter vs Frequency at 3.3V Supply and 25°C (BW 12kHz to 20MHz)

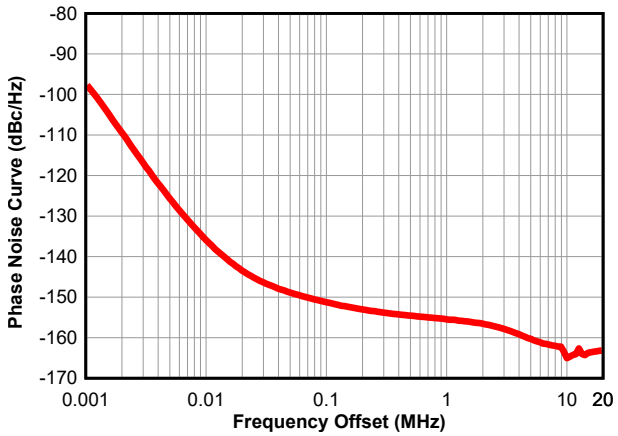

Figure 6-10. Phase Noise Curve at 25MHz, 25°C, and 3.3V Supply

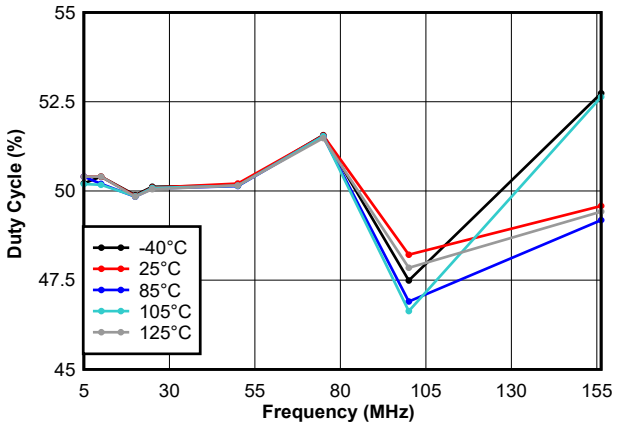

Figure 6-11. Duty Cycle vs Frequency and Temperature at 3.3V Supply, No Capacitative Load, Normal Mode Device

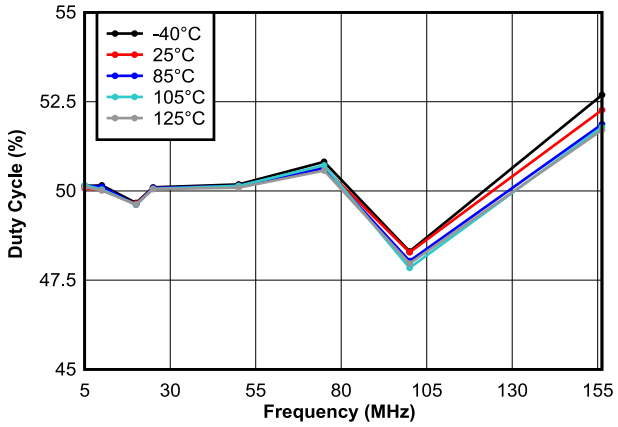

Figure 6-12. Duty Cycle vs Frequency and Temperature at 2.5V Supply, No Capacitative Load, Normal Mode Device

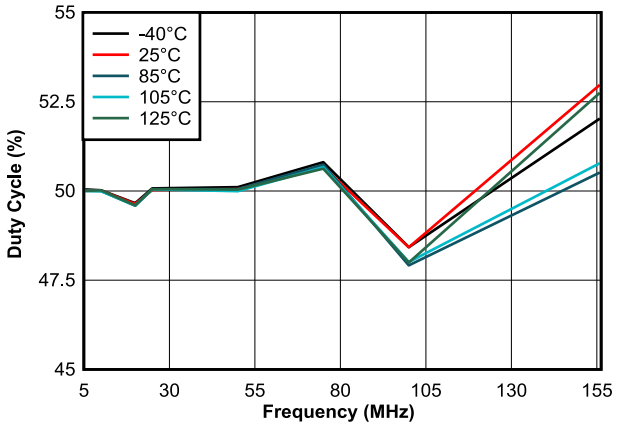

Figure 6-13. Duty Cycle vs Frequency and Temperature at 1.8V Supply, No Capacitative Load, Normal Mode Device

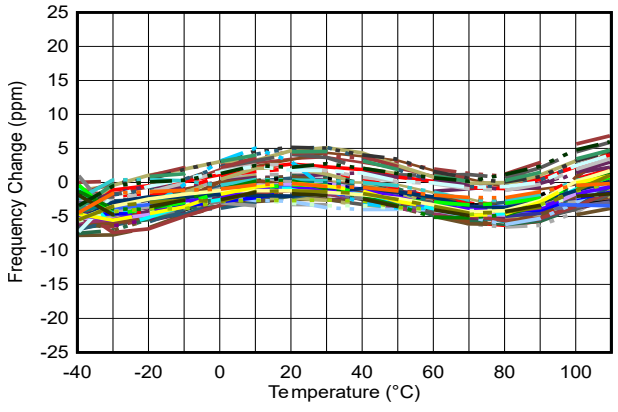

Figure 6-14. Frequency Change vs Temperature at 25MHz and 2.5V Supply, 100 Devices

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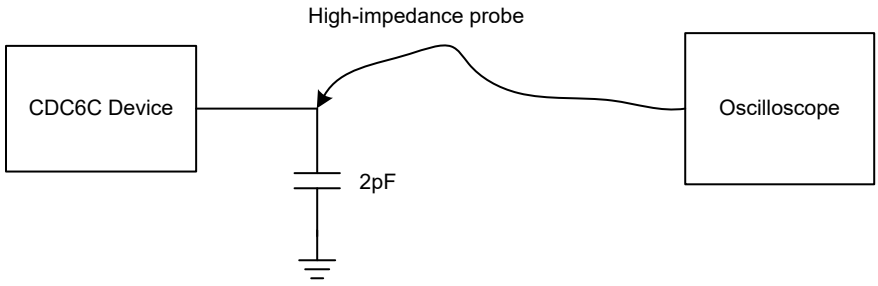
7 Parameter Measurement Information

7.1 Device Output Configurations



Load capacitor modified based on measurement condition.

Figure 7-1. CDC6Cx-Q1 Output Test Configuration

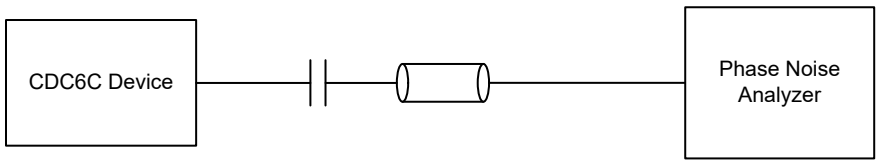


Figure 7-2. CDC6Cx-Q1 Output Phase Noise Test Configuration

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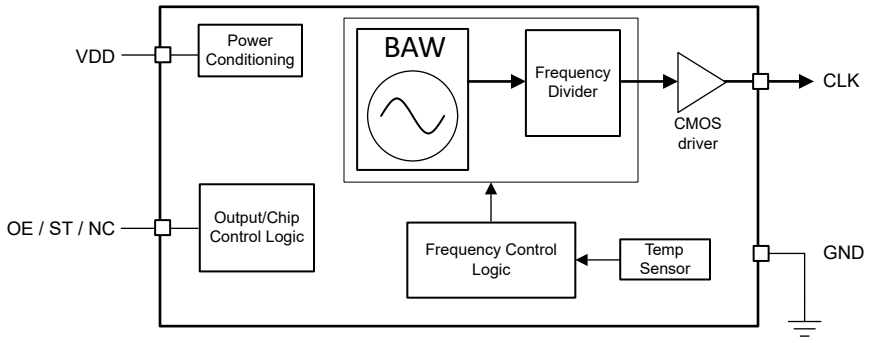
8 Detailed Description

8.1 Overview

The CDC6Cx-Q1 is a fixed-frequency, BAW based oscillator that supports a CMOS output format within the range from 250kHz to 200MHz.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5GHz. The quadrilateral area overlaid by top and bottom electrodes defines the resonator. Alternating high-acoustic and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by absorption of surface contaminants and can be directly placed in a non-hermetic plastic package with the oscillator IC in small standard oscillator footprints.

8.3.2 Device Block-Level Description

The device contains a BAW oscillator, frequency integer divider, and CMOS driver which together generates a pre-programmed output frequency. An internal precision temperature sensor continuously monitors temperature variations for oscillation frequency and is an input to the frequency control logic block. Using this frequency control logic block, frequency corrections are performed internally for maintaining the output frequency within ±25ppm across temperature range and aging. The device contains an internal LDO which reduces the power supply noise, resulting in low-noise clock output.

8.3.3 Function Pin

Pin 1 on the CDC6Cx-Q1 is the function pin which have multiple functions based on the orderable part number. Use the function as Output Enable (OE), Stand By (ST) or No Connect (NC). Options for Active High and Active Low are available for OE and ST. Contact TI for Active Low options. *Function Pin Descriptions* table lists the functions of pin 1.

Table 8-1. Function Pin Descriptions for CDC6Cx-Q1

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
A, C, E, G, or I (Pin 1)	Output Enable (Active High / NC)	**HIGH or No Connect** : Output active at Specified Frequency **LOW** : Output disabled, high impedance; I_{DD-OD} gives the current consumption

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Table 8-1. Function Pin Descriptions for CDC6Cx-Q1 (continued)

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
B, D, F, H, or J (Pin 1)	Standby (Active Low)	**HIGH or No Connect**: Output active at Specified Frequency **LOW** : High Impedance; standby mode; the standby current, $I_{DD-stdby}$, gives the current consumption

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of *Electrical Characteristics*. The return to the output clock active time corresponds to the same as the initial start-up time.

The function pin is driven internally with resistance > 100kΩ.

8.3.4 Clock Output Interfacing and Termination

The following figure shows the recommended output interfacing and termination circuits.

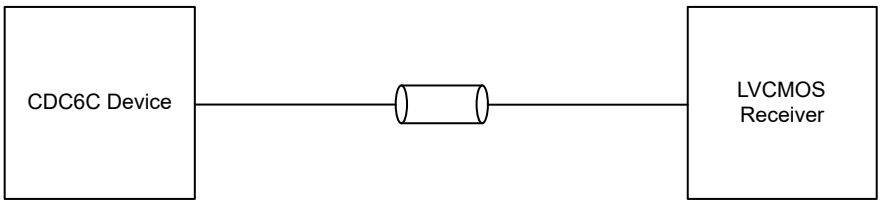

Figure 8-1. CDC6Cx-Q1 Output to LVCMOS Receiver

8.3.5 CDC6Cx-Q1 CISPR25 Radiated Emission Performance

The CDC6Cx-Q1 radiated EMI emissions performance passed up to CISPR-25 Class 5 for all bands except GPS L1 (1567.42MHz to 1583.42MHz) where the device passes Class 3. The CDC6Cx-Q1 is configured for slow mode 2 with a 5pF termination. The boards used have 50mil trace lengths, and the boards are tested in Texas Instruments' pre-compliant EMI chamber set up for CISPR-25 with antennas operating up to 13GHz. For more information, refer to *CDC6Cx-Q1 CISPR25 Radiated Emission Performance Report*.

8.3.5.1 EMI Reduction and Slow Mode Options

For EMI reduction, the CDC6Cx-Q1 has orderable options to reduce slew rate and increase rise and fall times. Slowing down the sharp rising and falling edges of a clock output, or lowering the output slew rate, decreases high-frequency harmonics, thereby lessening EMI. For applications requiring lesser EMI, select the appropriate rise and fall time options and see the *CDC6Cx-Q1 CISPR25 Radiated Emission Performance Report* for more EMI reduction strategies.

The CDC6Cx-Q1 has four slow mode options other than the normal mode. Based on the desired rise and fall times, select the right slow mode option and load capacitance value. Table 8-2 shows the minimum recommended capacitance for each slow mode.

Table 8-2. Minimum Recommended Capacitance per Slow Mode

SLOW MODE	MINIMUM RECOMMENDED CAPACITANCE (pF)
Slow Mode 1	2
Slow Mode 2	5
Slow Mode 3	10
Slow Mode 4	15

Table 8-3 has recommended slow mode options for various load capacitance for a 25MHz output clock. For example, with load capacitance 15pF, Slow Mode 4 option results in the slowest rise and fall times. You can also select Slow Mode 1, Slow Mode 2, or Slow Mode 3 with 15pF but the rise and fall times are faster.

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Table 8-3. Rise / Fall Time Options (25MHz Output)

SLOW MODE OPTION	LOAD CAPACITANCE	RISE AND FALL TIME (ns) WITH SLOW MODE (TYP / MAX)	RISE AND FALL TIME (ns) WITH NORMAL MODE (TYP / MAX)
Slow Mode 1	2pF	0.81 / 1.06	0.62 / 1.01
Slow Mode 2	5pF	1.47 / 1.62	0.76 / 1.24
Slow Mode 3	10pF	2.44 / 2.61	1.4 / 1.7
Slow Mode 4	15pF	3.29 / 3.5	1.88 / 2.11

8.3.6 Temperature Stability

Figure 8-2 shows the CDC6Cx-Q1 frequency change across temperature. The figure illustrates the frequency change of 100 different devices at different temperatures across the temperature range of –40°C to 125°C. This demonstrates the typical temperature stability of the device, remaining below ±10ppm.

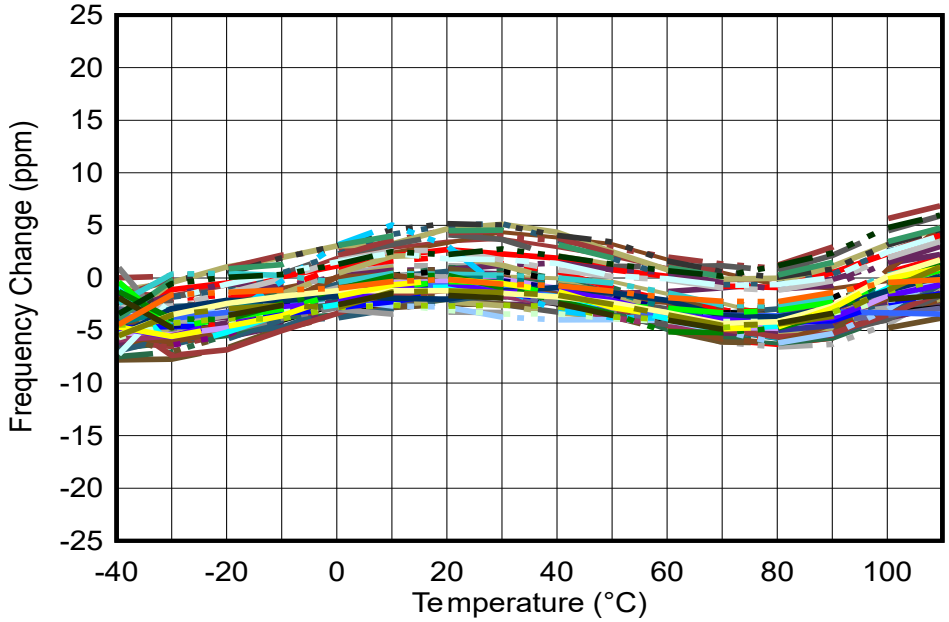

Figure 8-2. Typical Frequency Change From 25MHz Over Temperature Over 100 Devices

8.3.7 Frequency Aging

Table 8-4 the CDC6Cx-Q1 shows typical frequency shift from aging at different temperatures. Frequency drift is measured over 1000 hours for each temperature and extrapolated using MIL-PRF-55310-REV-F to predict frequency stability for up to 20 years. After aging for 20 years at 75°C, the predicted frequency stability is ±26ppm.

Table 8-4. Typical Frequency Aging for the CDC6Cx-Q1 at 55°C through 20 Years

TEMPERATURE (°C)	1-YEAR AGING (ppm)		10-YEAR AGING (ppm)		20-YEAR AGING (ppm)	
	Frequency Drift from Aging	Total Frequency Stability	Frequency Drift from Aging	Total Frequency Stability	Frequency Drift from Aging	Total Frequency Stability
55	±1.9	±21	±2.66	±22.51	±2.89	±22.85

8.3.8 Mechanical Robustness

For reference oscillators, vibration and shock are common causes for increased phase noise and jitter, frequency shift and spikes, or even physical damages to the resonator and package. Compared to quartz crystals, the BAW resonator is more immune to vibration and shock due to the orders of magnitude smaller mass and higher frequency—that is force applied to the device from acceleration is much smaller due to smaller mass.

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Figure 8-3 shows the CDC6Cx-Q1 BAW oscillator vibration performance. TI followed MIL-STD-883 Method 2026 Conditions C (10g) and Method 2007 Condition A (20g) for testing. In this test, the CDC6Cx-Q1 oscillator is mounted on an EVM and subjected to a 10g acceleration force, ranging from 50Hz to 2kHz in the x, y, and z-axis. Phase noise trace with spur due to vibration is captured using Keysight E5052B and frequency deviation is calculated from the spur power. Then the frequency deviation is converted to ppb by noting the carrier frequency and normalized to ppb/g. Finally, the RMS sum of ppb/g along all three axes is reported as the Vibration sensitivity in ppb/g. CDC6Cx-Q1 performance under vibration is approximately 2ppb/g while most quartz oscillators best case is 3ppb/g and worse can be above 10ppb/g.

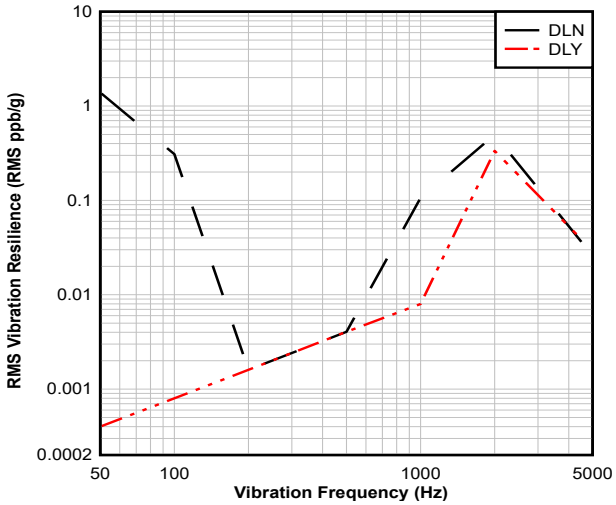

Figure 8-3. Vibration Resilience vs Vibration Frequency at 25MHz, 25°C, Supply 1.8V - X-Axis

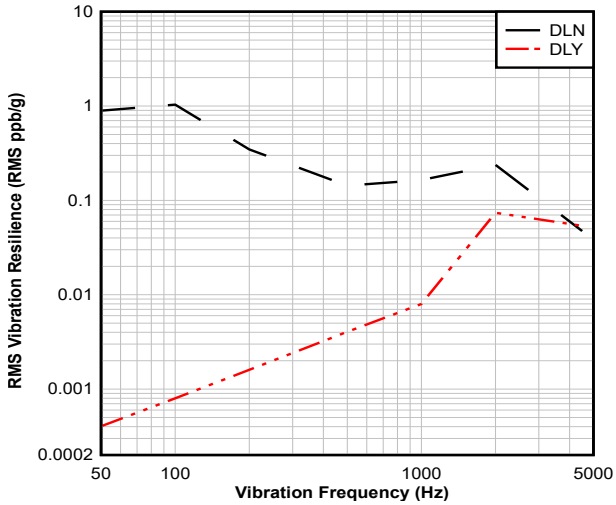

Figure 8-4. Vibration Resilience vs. Vibration Frequency at 25MHz, 25°C, Supply 1.8V - Y-Axis

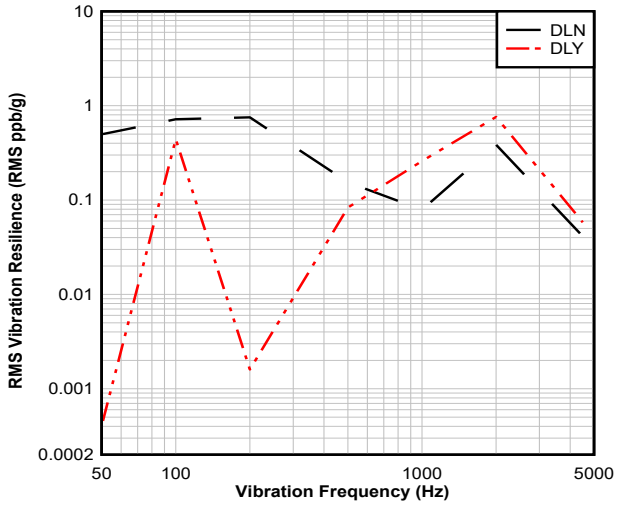

Figure 8-5. Vibration Resilience vs. Vibration Frequency at 25MHz, 25°C, Supply 1.8V - Z-Axis

For the mechanical shock test, TI followed MIL-STD-883F Method 2002 Condition A (1500g) for testing. For more information on BAW technology mechanical robustness, see the *Standalone BAW Oscillators Advantages Over Quartz Oscillators* application note.

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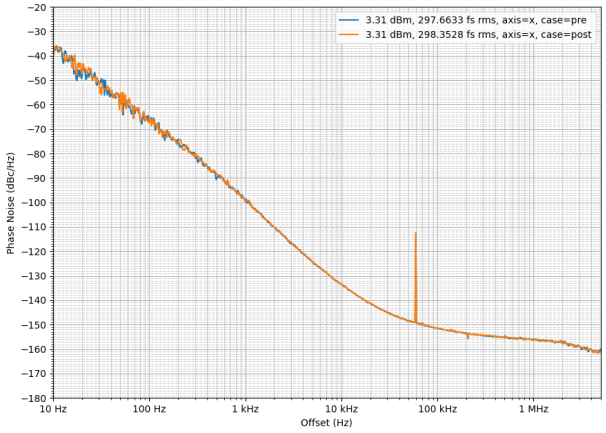

Figure 8-6. Pre and Post 1500g Mechanical Shock at 25MHz and 25°C, X-Axis

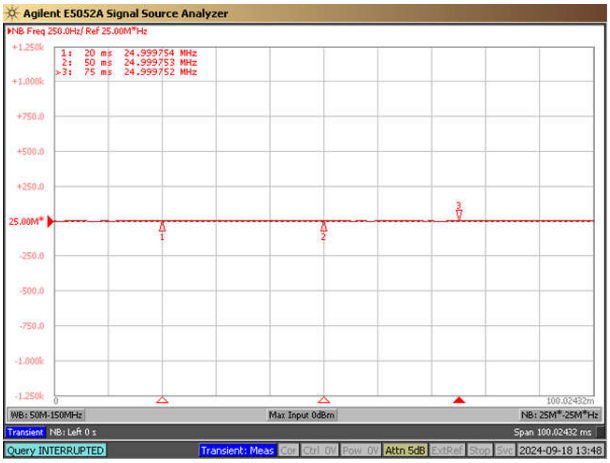

Figure 8-7. During 1500g Mechanical Shock at 25MHz and 25°C, X-Axis

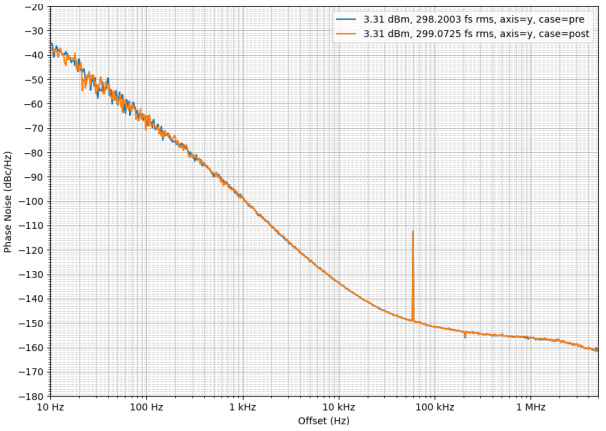

Figure 8-8. Pre and Post 1500g Mechanical Shock at 25MHz and 25°C, Y-Axis

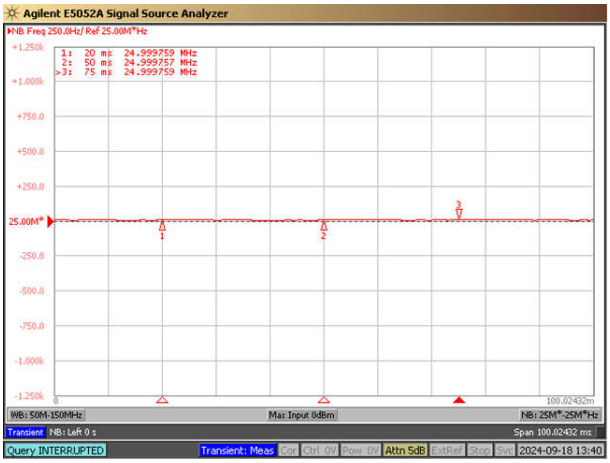

Figure 8-9. During 1500g Mechanical Shock at 25MHz and 25°C, Y-Axis

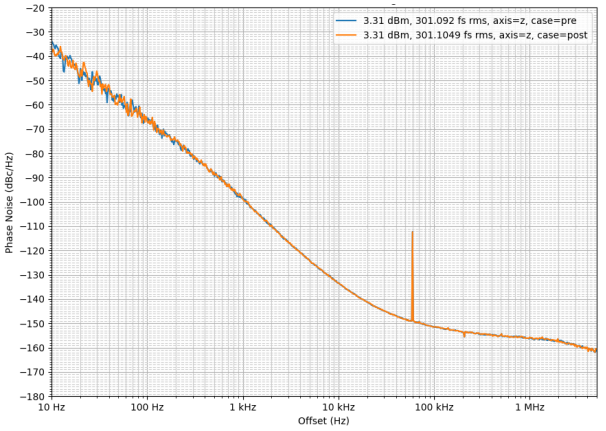

Figure 8-10. Pre- and Post- 1500g Mechanical Shock at 25MHz and 25°C, Z-Axis

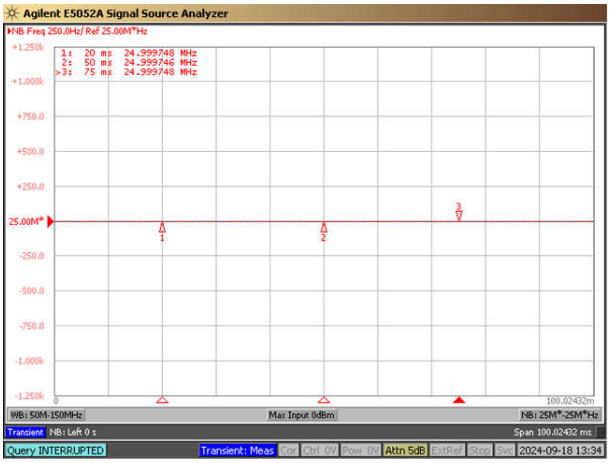

Figure 8-11. During 1500g Mechanical Shock at 25MHz and 25°C, Z-Axis

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8.3.9 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the datasheet where packages include this feature.

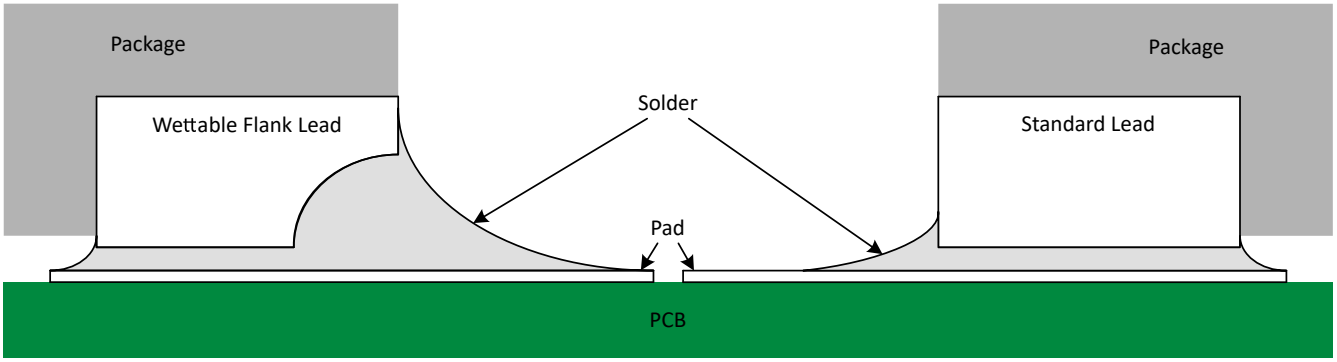

Figure 8-12. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-12, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.3.10 Device Functional Modes

The CDC6Cx-Q1 oscillator is a fixed-frequency device and does not require any programming. The device pin 1 has different functions and the device can come pre-programmed with a specific clock output slew rate. See Section 8.3.3 for more information on the function pins and Section 8.3.5.1 for more information on the different slow modes.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The CDC6Cx-Q1 is a low power, fixed-frequency oscillator that can be used as a reference clock. The device supports any output frequency between 250kHz to 200MHz, single-ended output type, and 1.8V to 3.3V supply rails.

9.1.1 Driving Multiple Loads With a Single CDC6Cx-Q1

The CDC6Cx-Q1 oscillator can be used to drive multiple loads to achieve cost reduction and BOM simplification. Be aware that using this technique degrades signal integrity and decreases performance. A good set of guidelines to follow when driving multiple loads include aiming to drive only two loads, maximizing common trace lengths across loads, and limiting total receiver capacitance to maximize fast rise and fall times. For more information on the effects of this technique and an implementation guide, see the *Driving Multiple Loads With a Single LVCMOS Oscillator* application note.

9.2 Typical Application

For a reference schematic implementation for CDC6Cx-Q1 oscillator, see the *Layout Examples* for bypass capacitor and AC-coupling capacitor value recommendations. See the *Clock Output Interfacing and Termination* section for output clock required termination and biasing.

Figure 9-1 shows a typical application example. The CDC6Cx-Q1 oscillator is used as a reference clock for a microcontroller or an FPGA in this example.

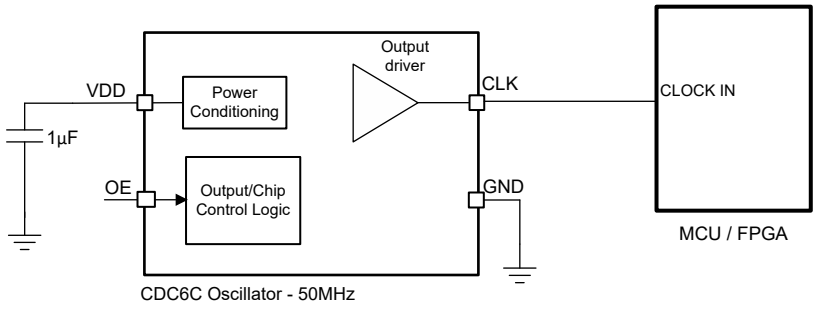

Figure 9-1. CDC6Cx-Q1 Application Example

9.2.1 Design Requirements

The CDC6Cx-Q1 is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in the *Clock Output Interfacing and Termination* section closely. See Section 8.3.3 to understand pin 1 function, and order the part number as per your requirements for Output Enable (OE), or Standby (ST) options.

9.2.2 Detailed Design Procedure

The CDC6Cx-Q1 has an integrated LDO and has excellent PSRR performance as shown in the *Electrical Characteristics* table. See the *CDC6CEVM User's Guide* for the reference layout recommendation while designing with the CDC6Cx-Q1 BAW oscillator.

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To set the pin 1 function for the CDC6Cx-Q1, connect typical 10kΩ or smaller resistor to VDD for driving the OE pin High. The device has an internal pullup resistor > 100kΩ, therefore this pin can be left open if an external pullup resistor is not desired. For driving the OE pin to Low, use the typical 10kΩ or smaller resistor as a pulldown resistor.

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9.2.3 Application Curves

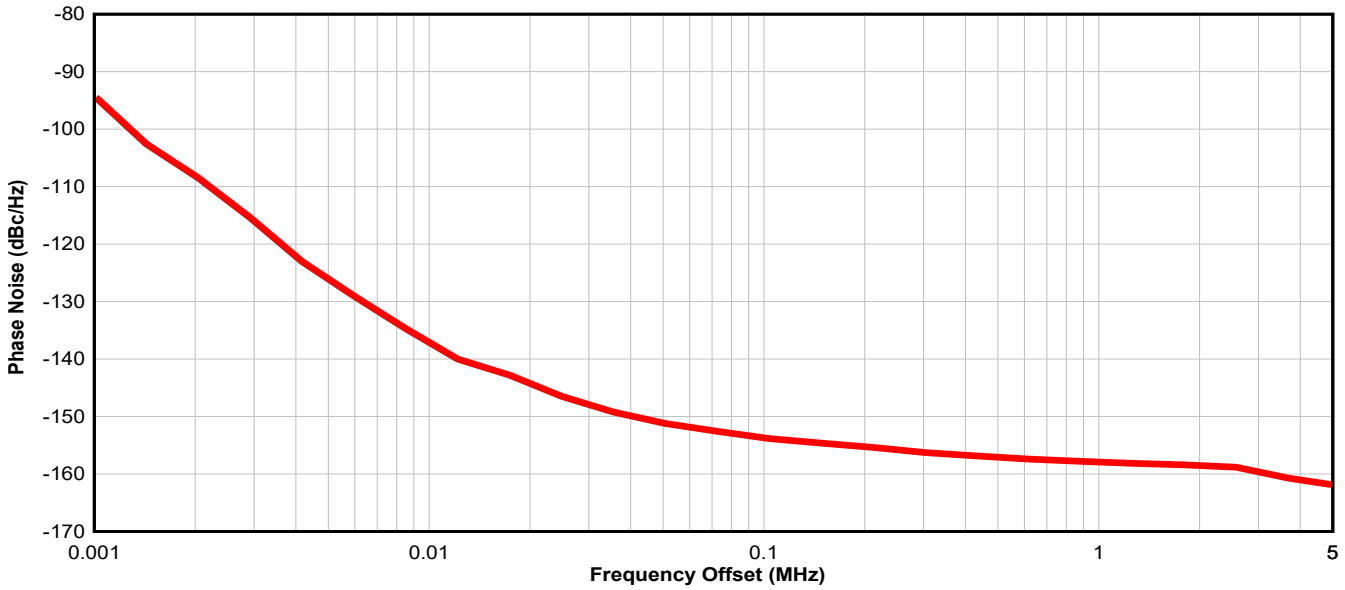

Figure 9-2. 19.2MHz LVCMOS, 25°C, 3.3V Supply

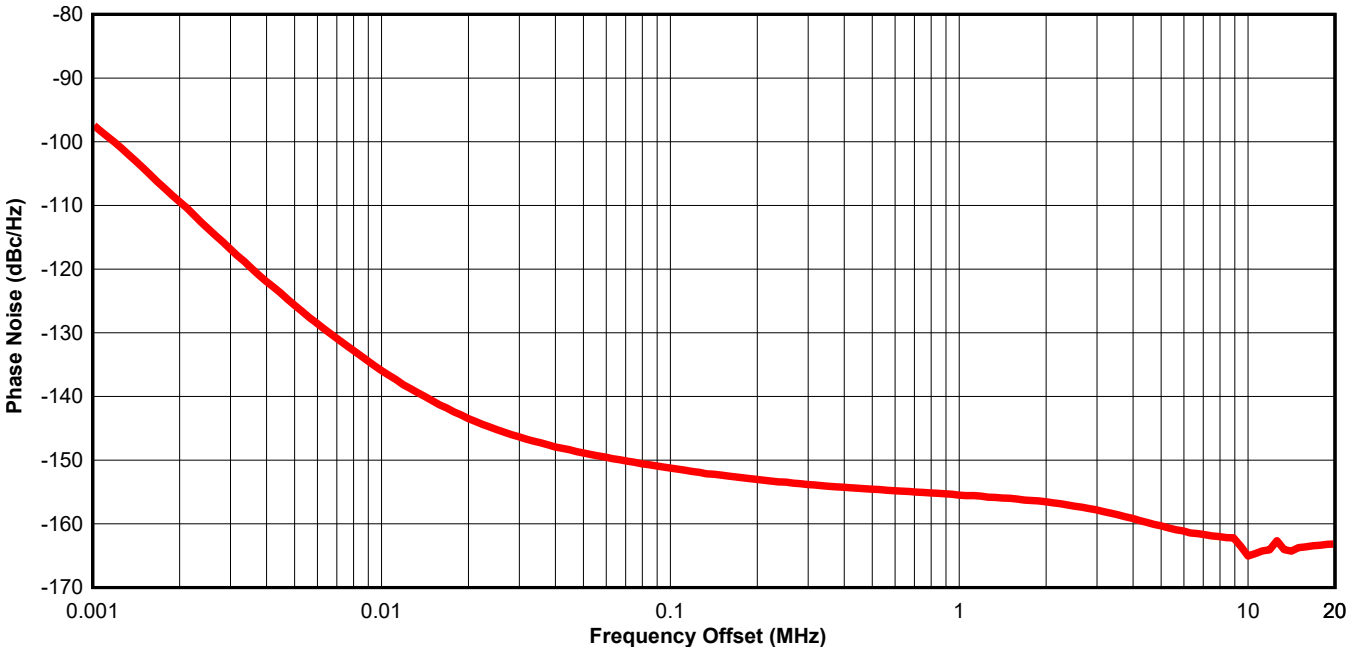

Figure 9-3. 25MHz LVCMOS, 25°C, 3.3V Supply

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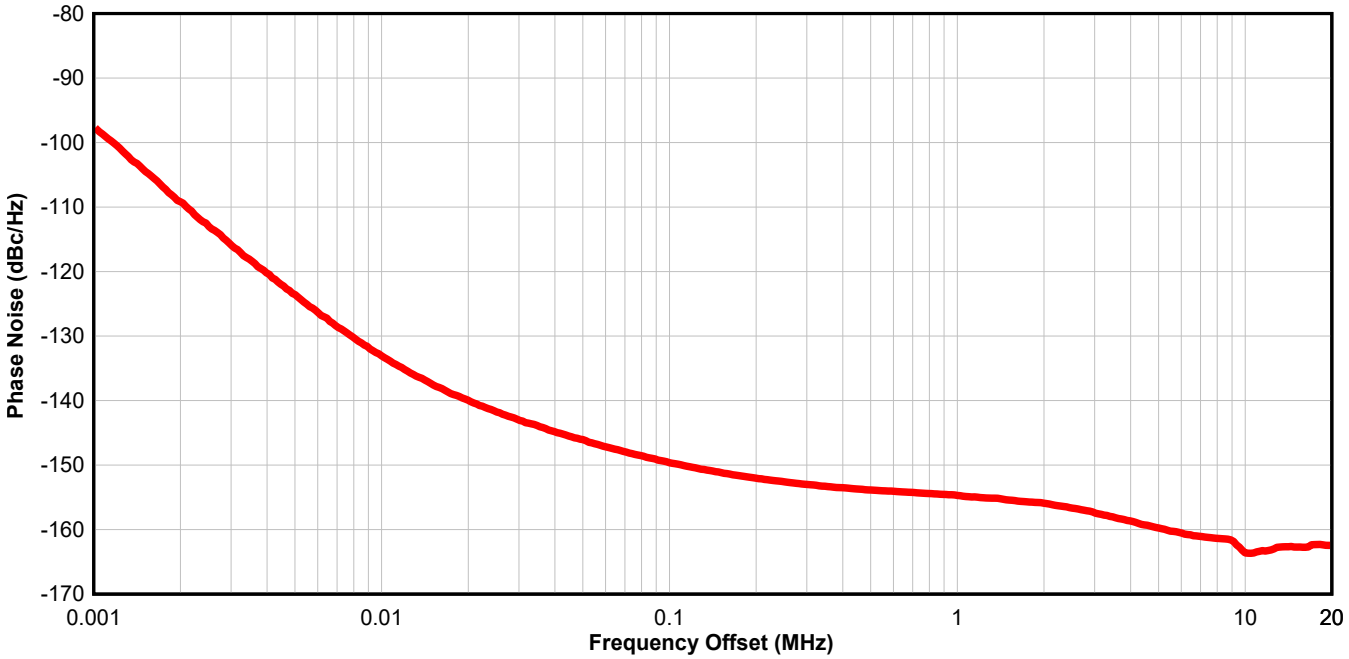

Figure 9-4. 27MHz LVCMOS, 25°C, 3.3V Supply

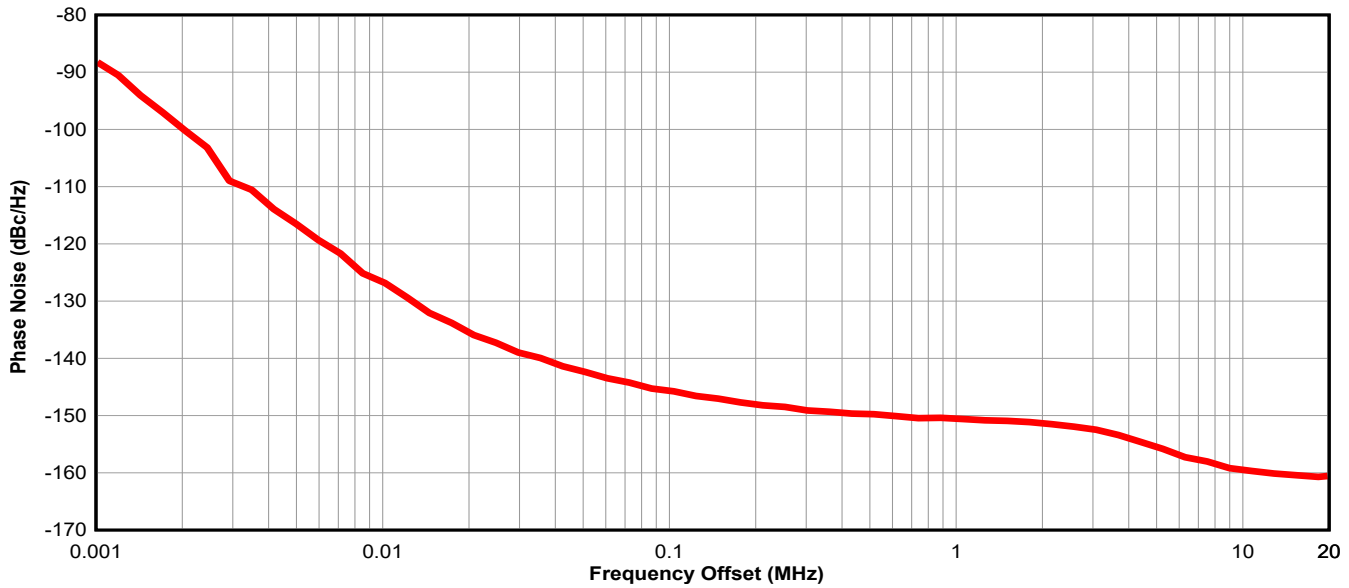

Figure 9-5. 50MHz LVCMOS, 25°C, 3.3V Supply

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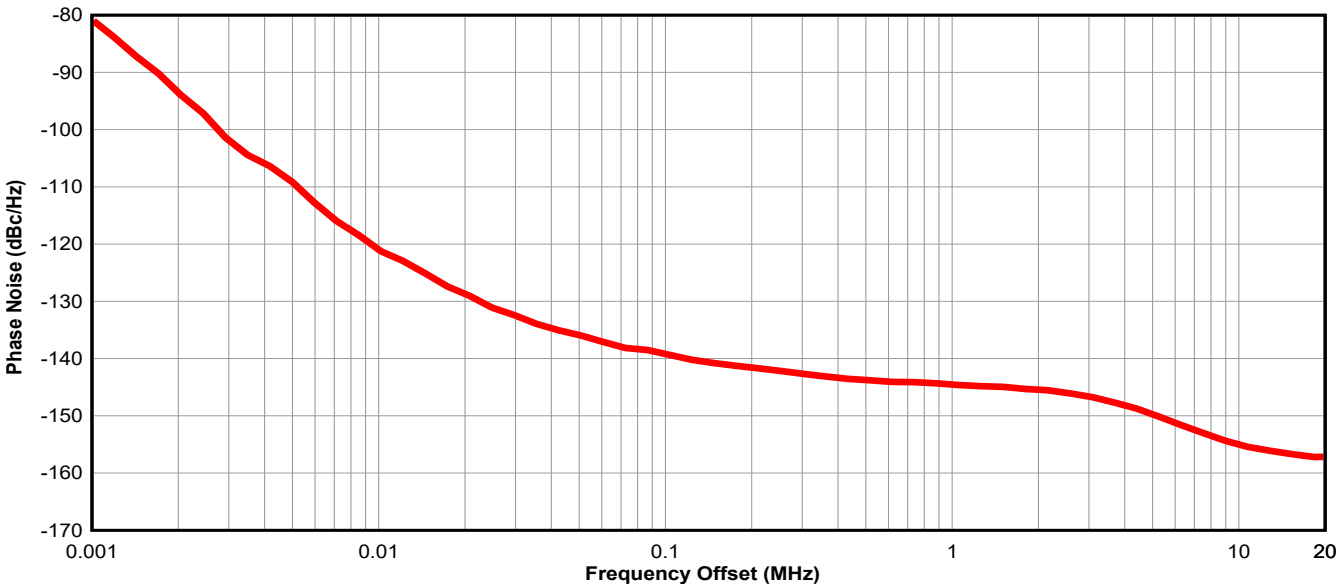

Figure 9-6. 100MHz LVCMOS, 25°C, 3.3V Supply

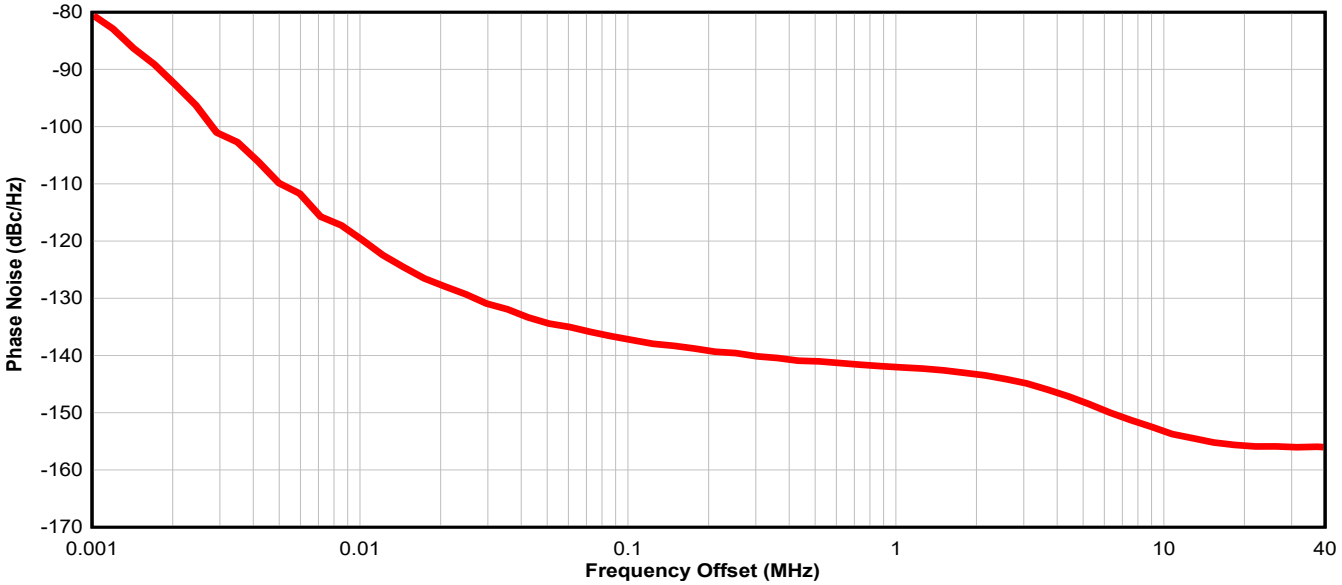

Figure 9-7. 125MHz LVCMOS, 25°C, 3.3V Supply

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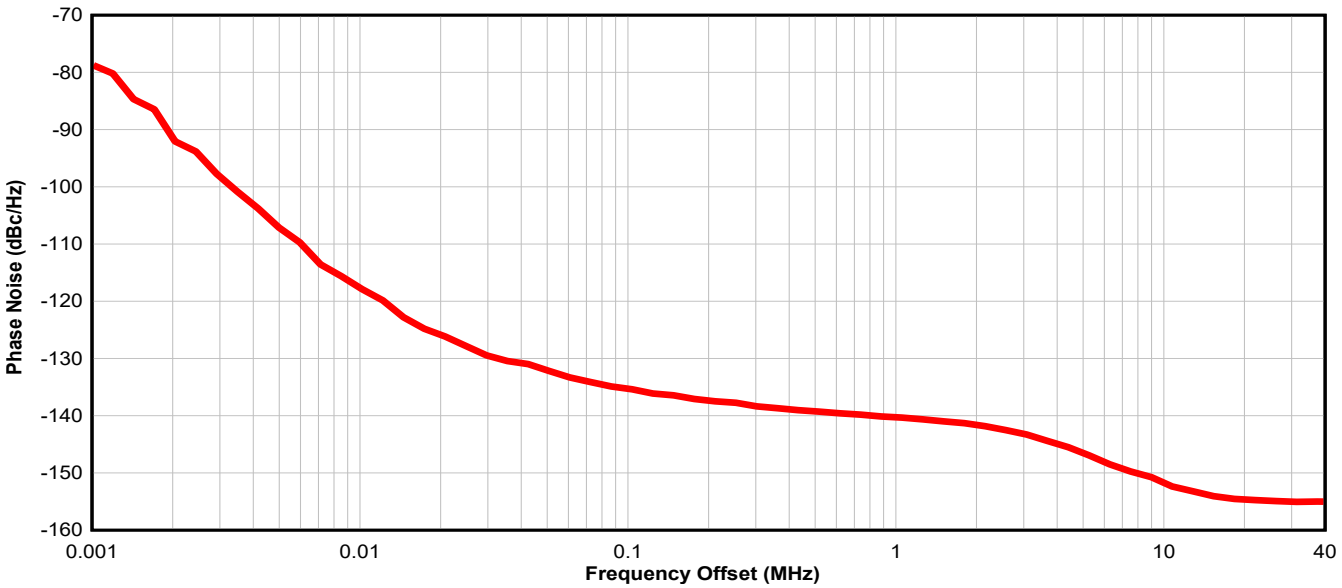

Figure 9-8. 156.25MHz LVCMOS, 25°C, 3.3V Supply

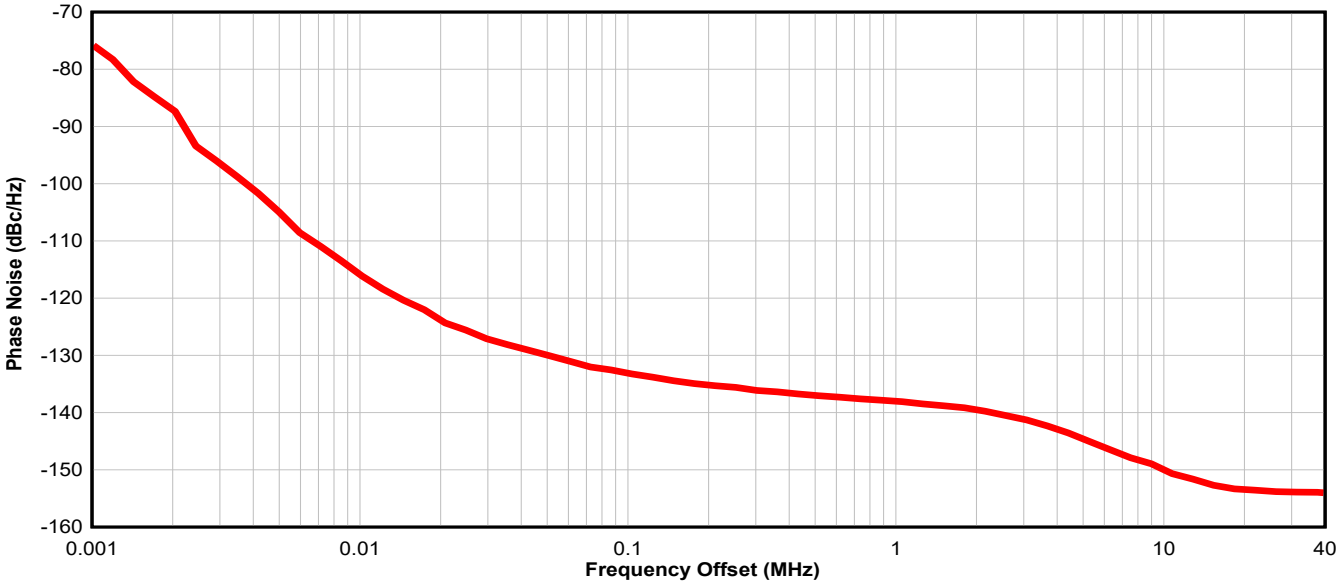

Figure 9-9. 200MHz LVCMOS, 25°C, 3.3V Supply

9.3 Power Supply Recommendations

For the best electrical performance of the CDC6Cx-Q1, TI recommends using a single 1µF power supply bypass capacitor. TI also recommends using component side mounting of the power supply bypass capacitors. 0201 or 0402 body size capacitors facilitate best signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

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9.4 Layout

9.4.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power-supply bypassing when using the CDC6Cx-Q1 to provide good thermal and electrical performance and signal integrity of the entire system.

9.4.1.1 Providing Thermal Reliability

The CDC6Cx-Q1 is a low power, high performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

The equation below describes the relationship between the PCB temperature around the CDC6Cx-Q1 and the junction temperature.

$$T_B = T_J – \Psi_{JB} \times P \quad (1)$$

where

- T_B: PCB temperature around the CDC6Cx-Q1
- T_J: Junction temperature of CDC6Cx-Q1
- Ψ_{JB}: Junction-to-board thermal resistance parameter of CDC6Cx-Q1 (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- P: On-chip power dissipation of CDC6Cx-Q1

9.4.1.2 Recommended Solder Reflow Profile

TI recommends following the recommendations from the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-020E. Processing the CDC6Cx-Q1 with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferable. The exact temperature profile depends on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, solder manufactures recommended profile, and capability of the reflow equipment as confirmed by the SMT assembly operation.

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9.4.2 Layout Examples

Figure 9-10 shows the printed circuit board (PCB) layout examples as done on the evaluation module (EVM) for the CDC6Cx-Q1.

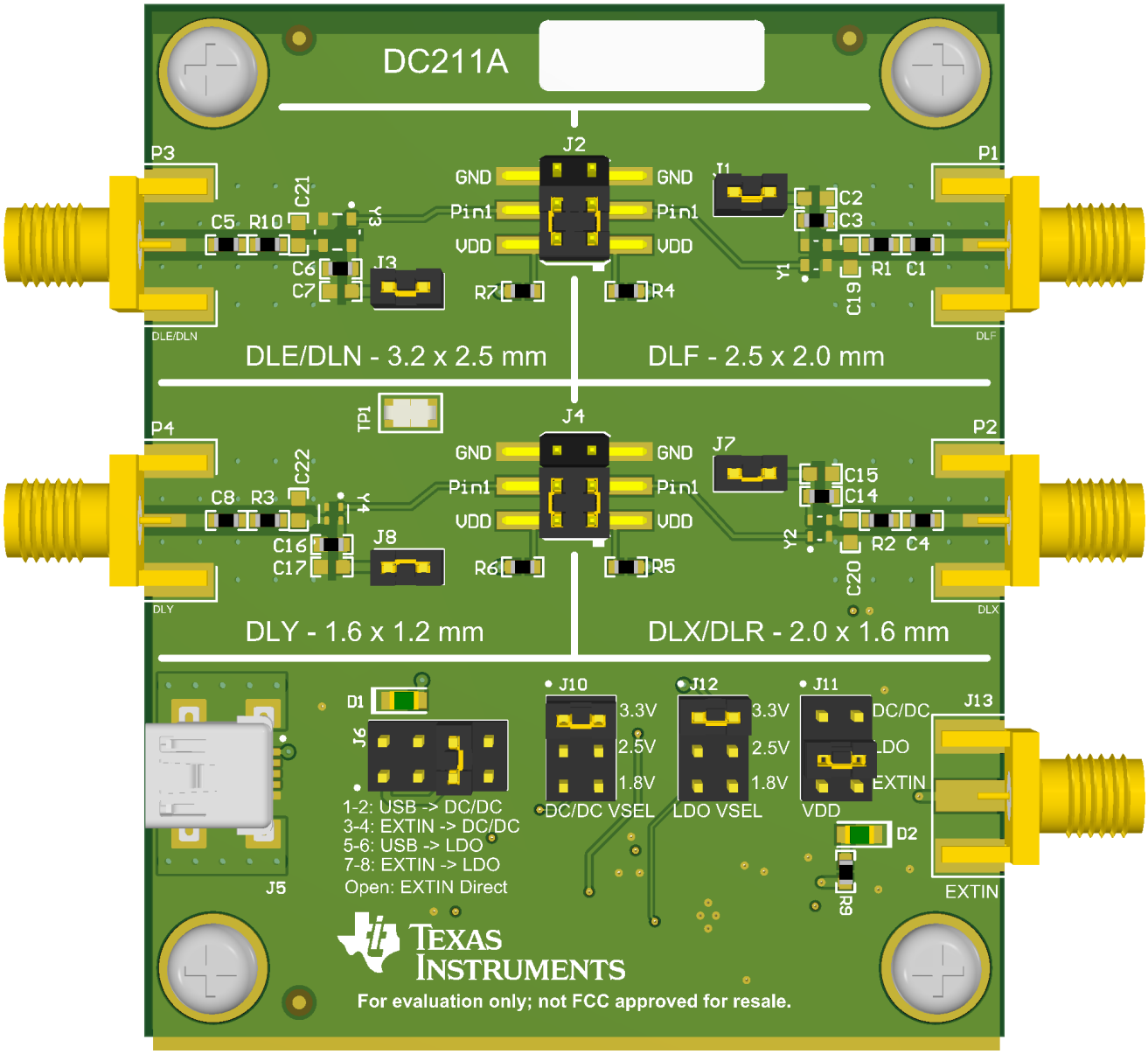

Figure 9-10. PCB Layout Example From CDC6 EVM

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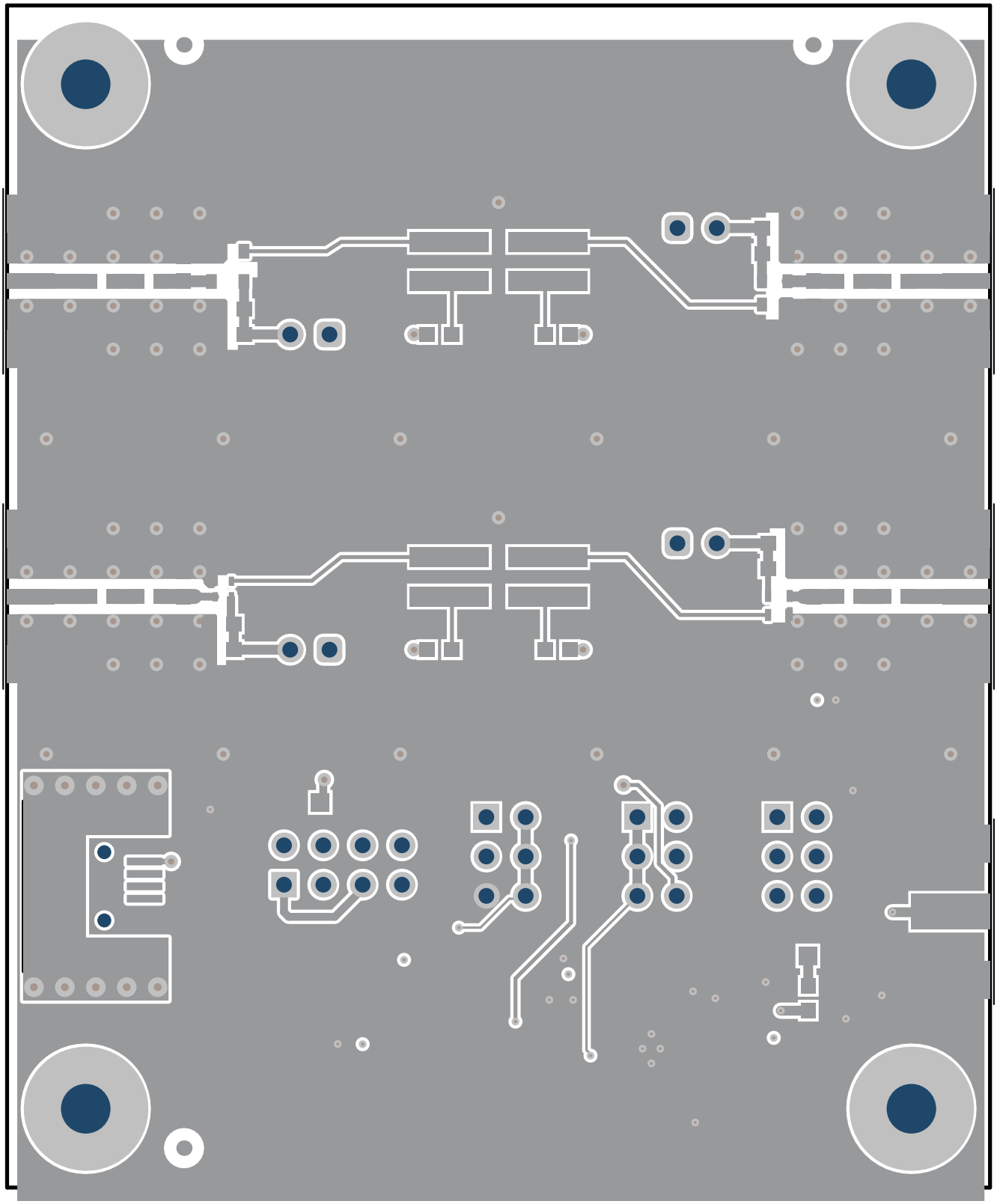

Figure 9-11. PCB Layout Example From CDC6 EVM - Top Layer

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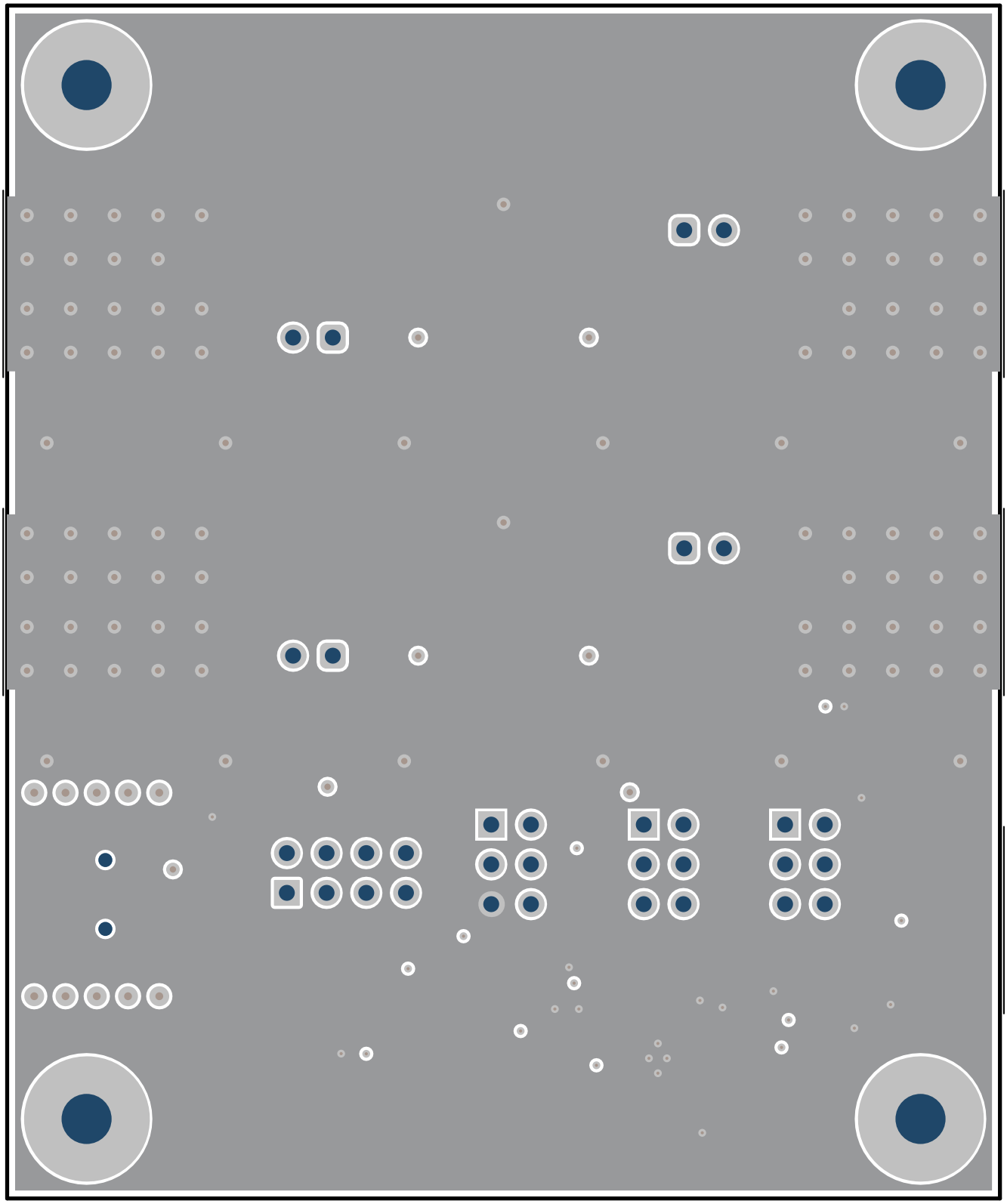

Figure 9-12. PCB Layout Example From CDC6 EVM - GND Layer

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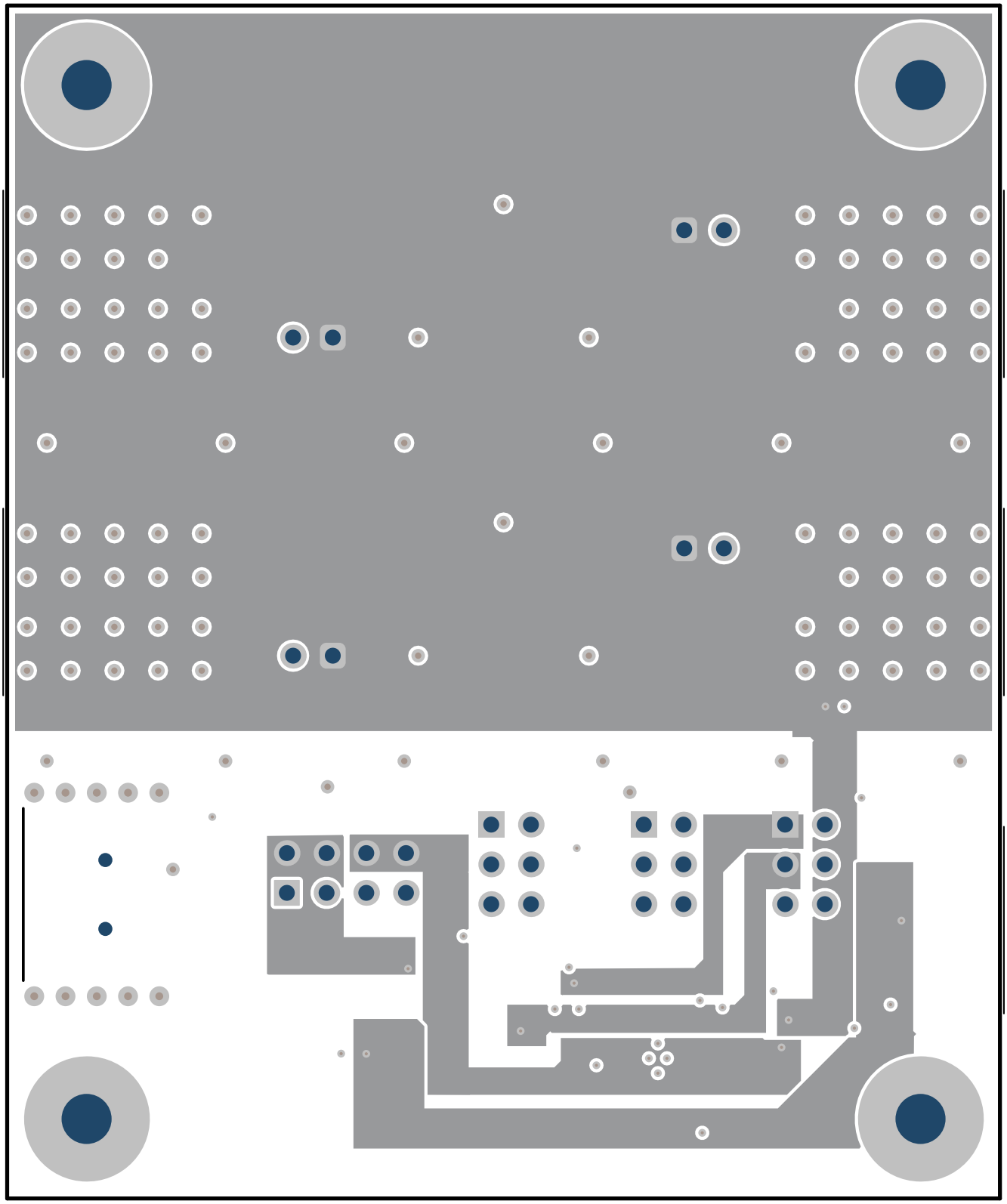

Figure 9-13. PCB Layout Example From CDC6 EVM - Power Layer

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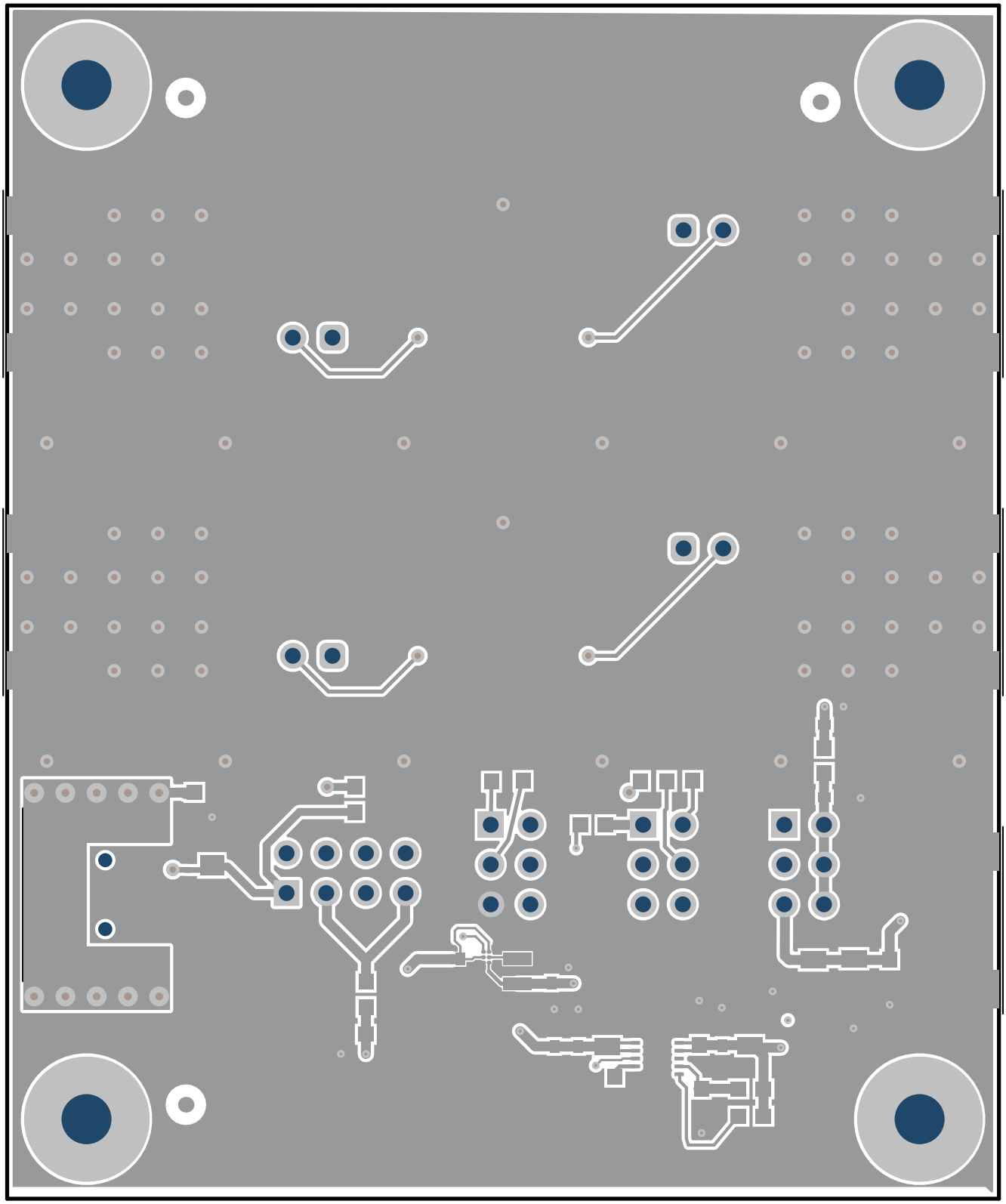

Figure 9-14. PCB Layout Example From CDC6 EVM - Bottom Layer

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CDC6CEVM User's Guide*
- Texas Instruments, *CDC6C OPN Decoder* application note
- Texas Instruments, *CDC6C-Q1 Functional Safety FIT Rate, FMD and Pin FMA*
- Texas Instruments, *Standalone BAW Oscillators Advantages Over Quartz Oscillators* application note
- Texas Instruments, *Driving Multiple Loads With a Single LVCMOS Oscillator* application note
- Texas Instruments, *CDC6Cx-Q1 CISPR25 Radiated Emission Performance Report*
- Texas Instruments, *BAW Oscillator Designs for Building Automation* application note
- Texas Instruments, *BAW Oscillator Designs for Factory Automation* application note
- Texas Instruments, *BAW Oscillator Designs for Grid Infrastructure* application note
- Texas Instruments, *BAW Oscillator Designs for Optical Modules* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2025) to Revision C (July 2026)	Page
• Added comment to contact TI for -EP option	3

Changes from Revision A (October 2025) to Revision B (November 2025) **Page**

- Added legend to explain color assignment for the *Pin Functions* table....4
- Removed minimum and maximum values for output impedance....6
- Updated inout current to match recent design findings....6
- Removed integration bandwidth for RMS period jitter....6
- Updated *Phase Noise Curve at 25MHz, 25ºC, and 3.3V Supply* to include frequency offsets through 20MHz....10
- Updated the *Detailed Design Procedure* to specify output frequency of 25MHz and corrected rise and fall times to match the *Electrical Characteristics* table....19
- Changed Figure 9-3 and Figure 9-4 to include frequency offsets through 20MHz....21
- Updated the *Mechanical, Packaging, and Orderable Information* section....33

Changes from Revision * (March 2025) to Revision A (October 2025) **Page**

- Added corrections to specifications on the first page to match specifications table and added comment about universal land patterns....1
- Changed the device status from *Advanced* to *Production Data* 1
- Added reference to *EMI Reduction and Slow Mode Options* to explain slow mode orderable options....3
- Added output frequency used for all output rise and fall time data and increased rise and fall times maximum values....6
- Decreased maximum rise or fall time for slow mode 2, 3, and 4....6
- Added 10% to 90% rise and fall time typical values....6
- Lowered input low voltage for function pins and specified maximum value per VDD....6
- Added diagram to describe standby and output enable pin power-on characteristics....8
- Updated Figure 6-8 and Figure 6-9 with new, updated data....10
- Changed the order of HIGH and LOW functions for structural consistency and added all OPN letters to the *Function Pin Descriptions* table....13
- Moved Section 8.3.5 and Section 8.3.5.1 to separate, independent sections under the *Feature Description* 14
- Added Section 8.3.7 15
- Added the *Wettable Flanks* section....18
- Removed V_{DD} power-up ramp time requirements, no specific power-up requirements are no longer needed 24

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC6C002000BDLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	MB
CDC6C004000BDLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	BB
CDC6C004096BDLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	HB
CDC6C008000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	OA
CDC6C008192ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	QA
CDC6C008192BDLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	IB
CDC6C012000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AB
CDC6C012288ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	EA
CDC6C019200ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	GA
CDC6C020000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	DA
CDC6C020000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	DA
CDC6C023430ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	JB
CDC6C023430EDLYRQ1	Active	Production	VSON (DLY) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	LB
CDC6C024000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	CA
CDC6C024000HDLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	7A
CDC6C024000HDLYRQ1	Active	Production	VSON (DLY) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	7A
CDC6C025000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AA
CDC6C025000ADLNRQ1	Active	Production	VSON (DLN) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AA
CDC6C025000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AA
CDC6C025000ADLYRQ1	Active	Production	VSON (DLY) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AA
CDC6C025000BDLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	4A
CDC6C025000EDLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	SA
CDC6C025000EDLYRQ1	Active	Production	VSON (DLY) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	SA
CDC6C027000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	HA
CDC6C027000ADLNRQ1	Active	Production	VSON (DLN) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	HA
CDC6C027000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	HA
CDC6C033333ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	MA
CDC6C033333ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	MA
CDC6C040000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	FA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC6C040000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	FA
CDC6C042000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	KB
CDC6C048000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	IA
CDC6C050000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	BA
CDC6C050000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	BA
CDC6C100000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	JA
CDC6C100000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	JA
CDC6C125000ADLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	LA
CDC6C125000ADLRRQ1	Active	Production	VSON (DLR) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	LA
CDC6C125000IDLFRQ1	Active	Production	VSON (DLF) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	6A
CDC6C125000IDLYRQ1	Active	Production	VSON (DLY) | 4	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	6A
PCDC6C02500ADLRTQ1	Active	Preproduction	VSON (DLR) | 4	3000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
PCDC6C02500ADLRTQ1.A	Active	Preproduction	VSON (DLR) | 4	3000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
PCDC6C02700ADLRTQ1	Active	Preproduction	VSON (DLR) | 4	3000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
PCDC6C02700ADLRTQ1.A	Active	Preproduction	VSON (DLR) | 4	3000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF CDC6C-Q1 :

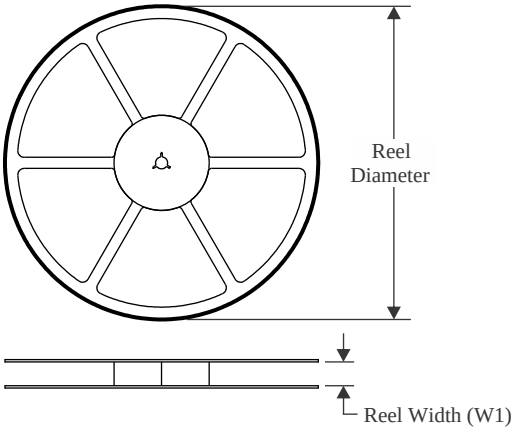
- Catalog : CDC6C

NOTE: Qualified Version Definitions:

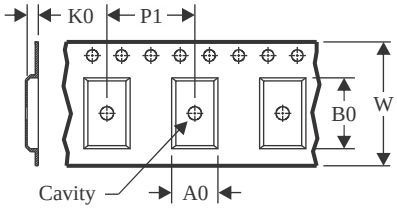
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

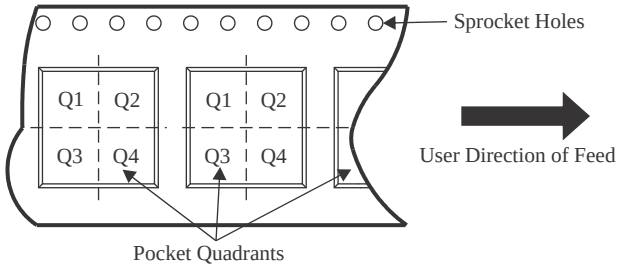


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

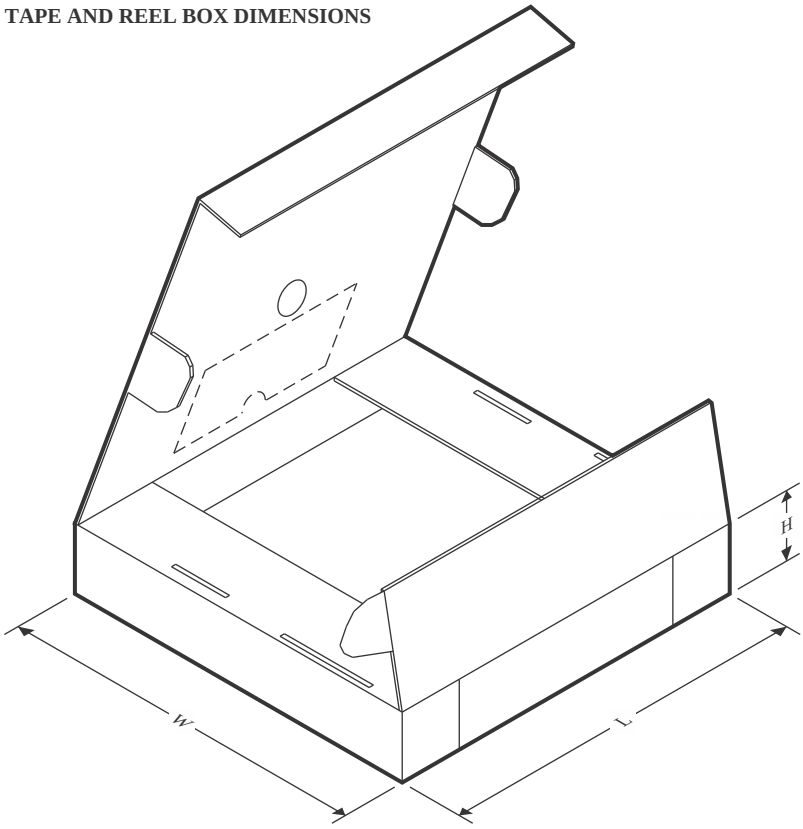


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC6C002000BDLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C004000BDLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C004096BDLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C008000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C008192ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C008192BDLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C012000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C012288ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C019200ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C020000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C020000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C023430ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C023430EDLYRQ1	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1
CDC6C024000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C024000HDLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C024000HDLYRQ1	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC6C025000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C025000ADLNRQ1	VSON	DLN	4	3000	330.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1
CDC6C025000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C025000ADLYRQ1	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1
CDC6C025000BDLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C025000EDLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C025000EDLYRQ1	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1
CDC6C027000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C027000ADLNRQ1	VSON	DLN	4	3000	330.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1
CDC6C027000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C033333ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C033333ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C040000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C040000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C042000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C048000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C050000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C050000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C100000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C100000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C125000ADLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C125000ADLRRQ1	VSON	DLR	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1
CDC6C125000IDLFRQ1	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6C125000IDLYRQ1	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC6C002000BDLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C004000BDLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C004096BDLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C008000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C008192ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C008192BDLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C012000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C012288ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C019200ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C020000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C020000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C023430ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C023430EDLYRQ1	VSON	DLY	4	3000	182.0	182.0	20.0
CDC6C024000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C024000HDLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C024000HDLYRQ1	VSON	DLY	4	3000	182.0	182.0	20.0
CDC6C025000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C025000ADLNRQ1	VSON	DLN	4	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC6C025000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C025000ADLYRQ1	VSON	DLY	4	3000	182.0	182.0	20.0
CDC6C025000BDLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C025000EDLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C025000EDLYRQ1	VSON	DLY	4	3000	182.0	182.0	20.0
CDC6C027000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C027000ADLNRQ1	VSON	DLN	4	3000	367.0	367.0	35.0
CDC6C027000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C033333ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C033333ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C040000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C040000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C042000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C048000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C050000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C050000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C100000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C100000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C125000ADLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C125000ADLRRQ1	VSON	DLR	4	3000	182.0	182.0	20.0
CDC6C125000IDLFRQ1	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6C125000IDLYRQ1	VSON	DLY	4	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

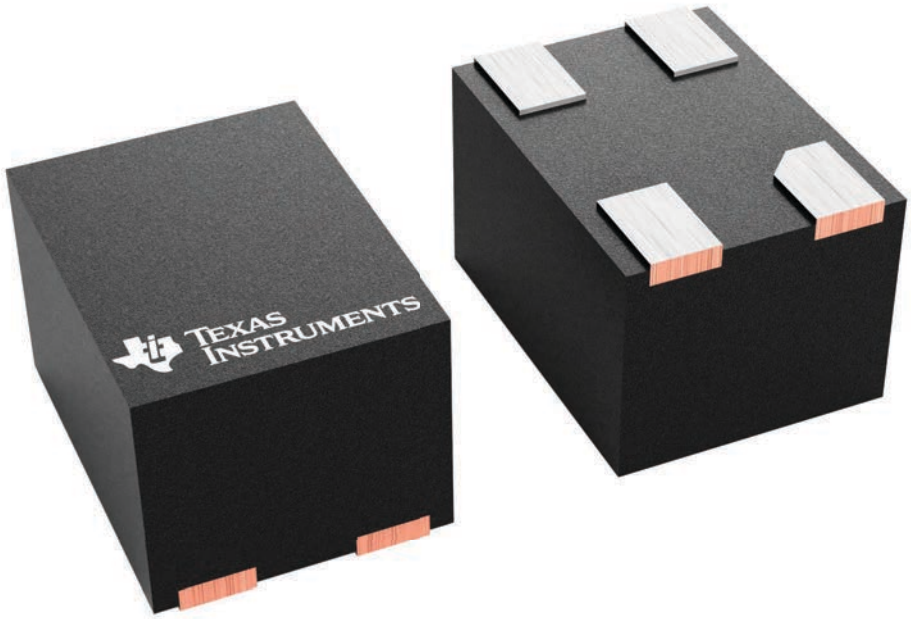
DLY 4

VSON - 1 mm max height

1.6 x 1.2, 0.7 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229365/A

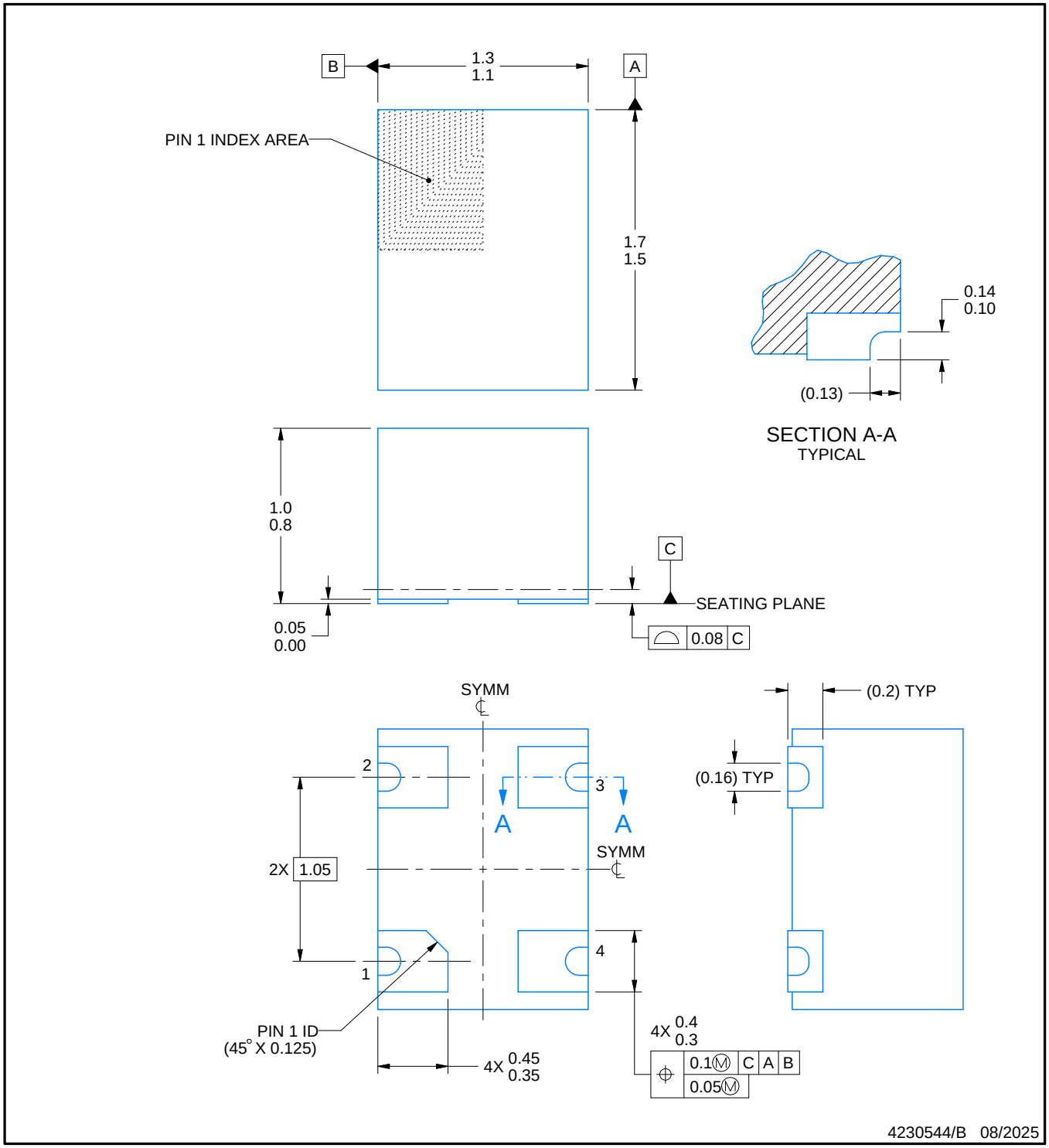
DLY0004D



PACKAGE OUTLINE

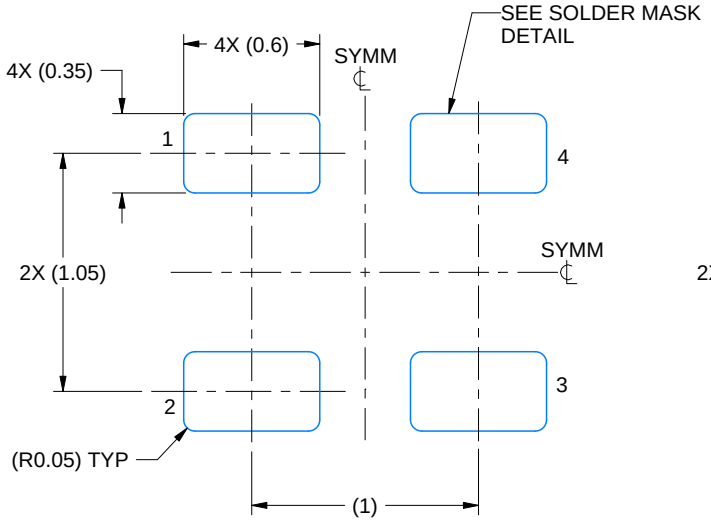
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

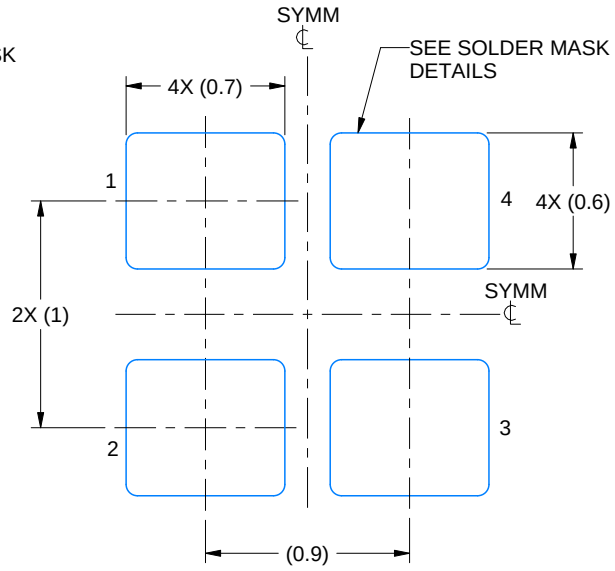


NOTES:

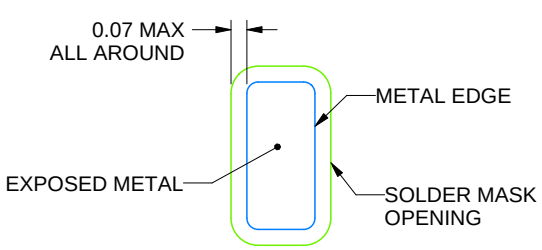
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



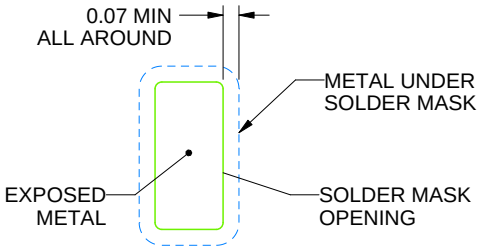
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK
DEFINED
(PREFERRED)



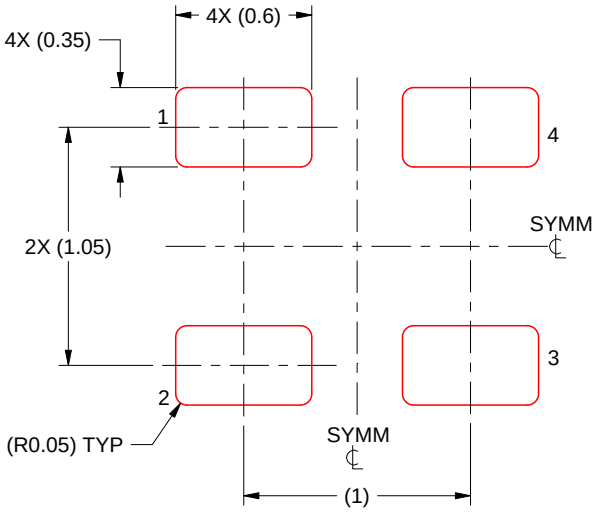
SOLDER MASK DEFINED

SOLDER MASK DETAILS

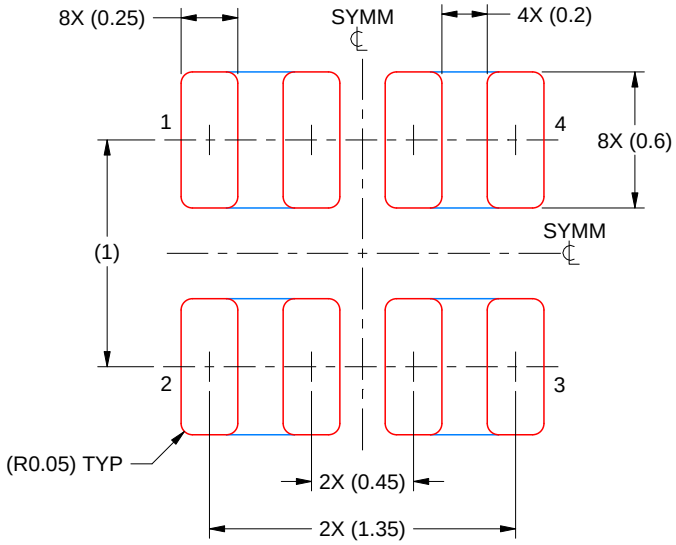
4230544/B 08/2025

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 71%

4230544/B 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

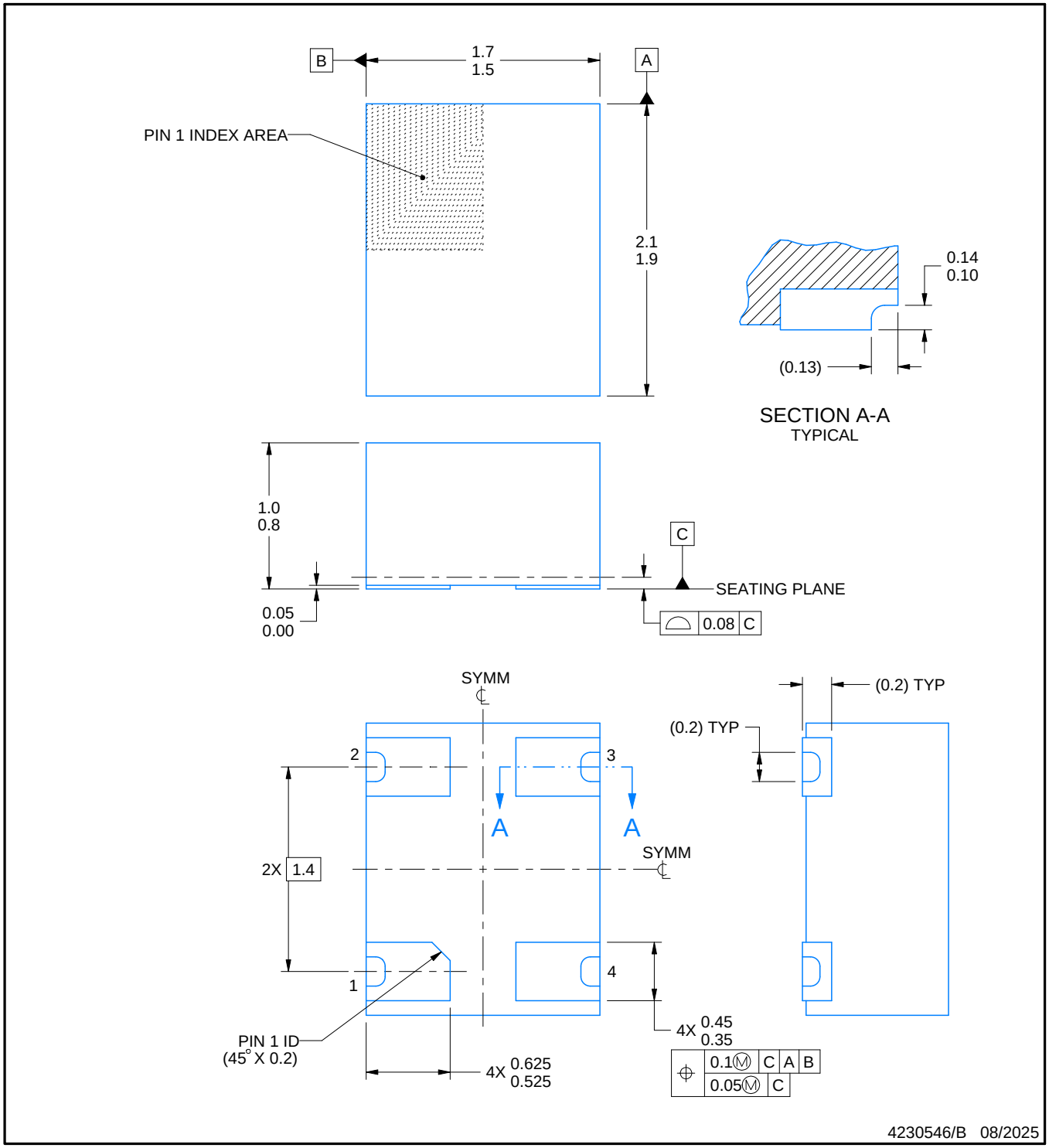
DLR0004A



PACKAGE OUTLINE

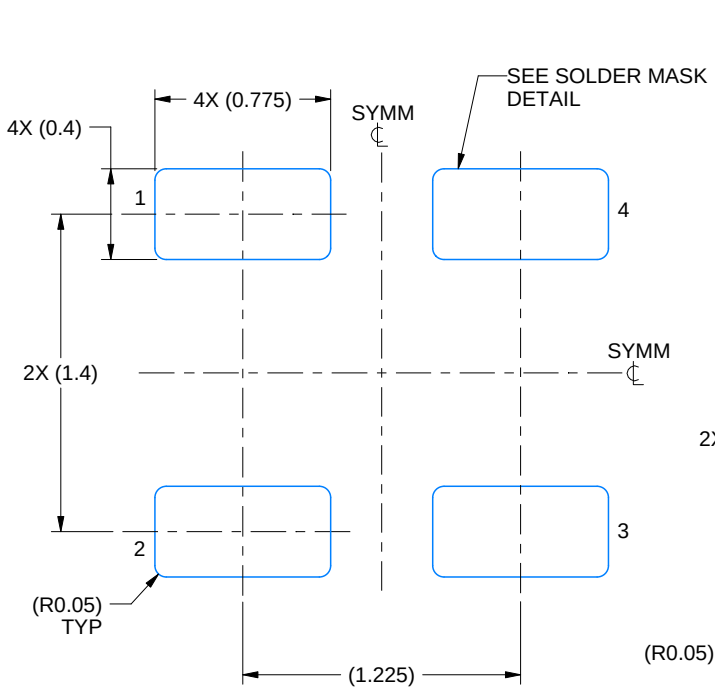
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

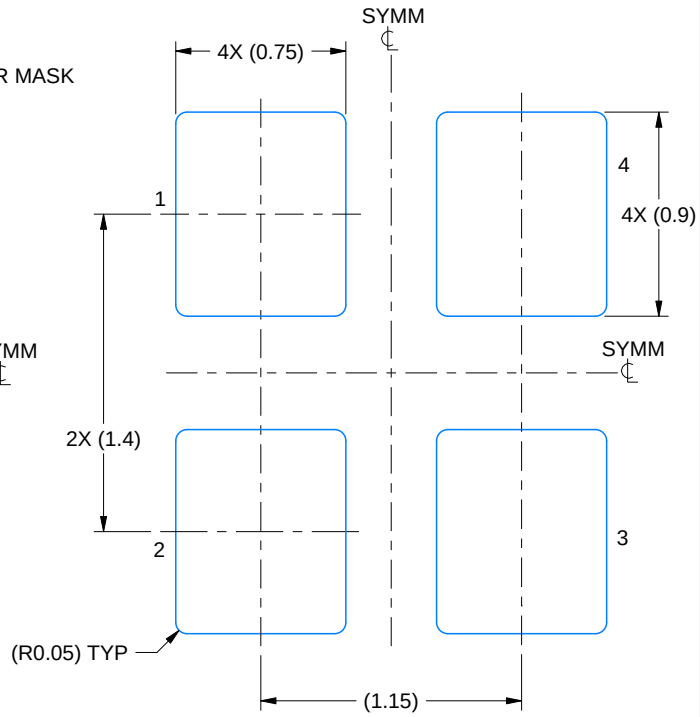


NOTES:

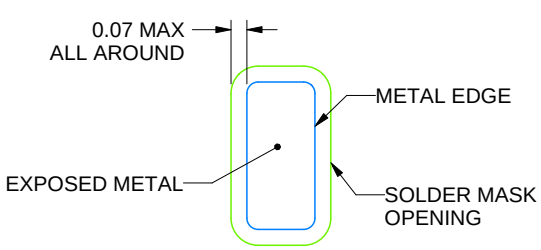
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



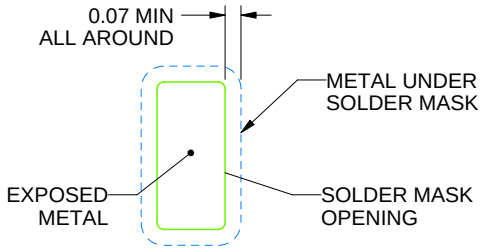
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK DEFINED
(PREFERRED)



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4230546/B 08/2025

NOTES: (continued)

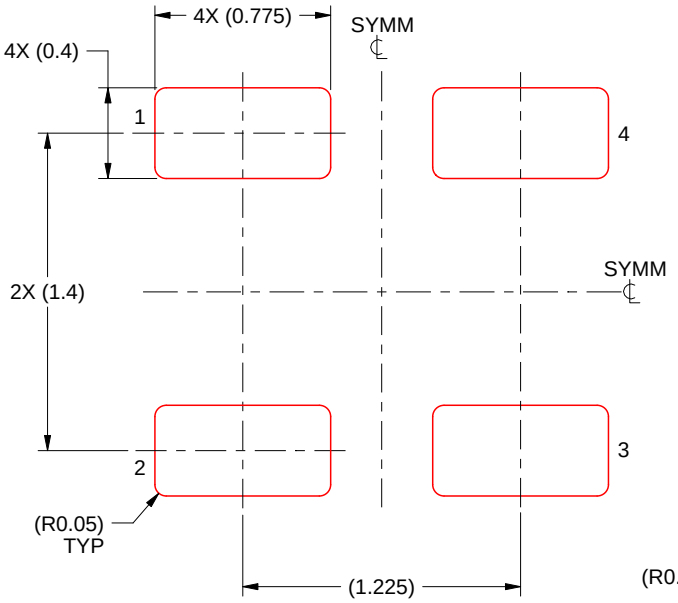
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

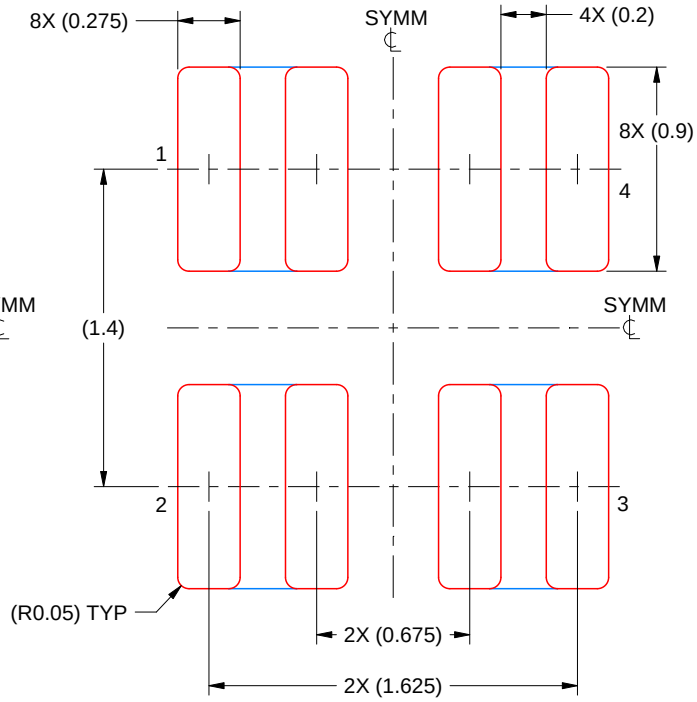
DLR0004A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 73%

4230546/B 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DLF 4

VSON - 1 mm max height

2 x 2.5, 1.65 mm pitch

PLASTIC QUAD FLAT PACK-NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



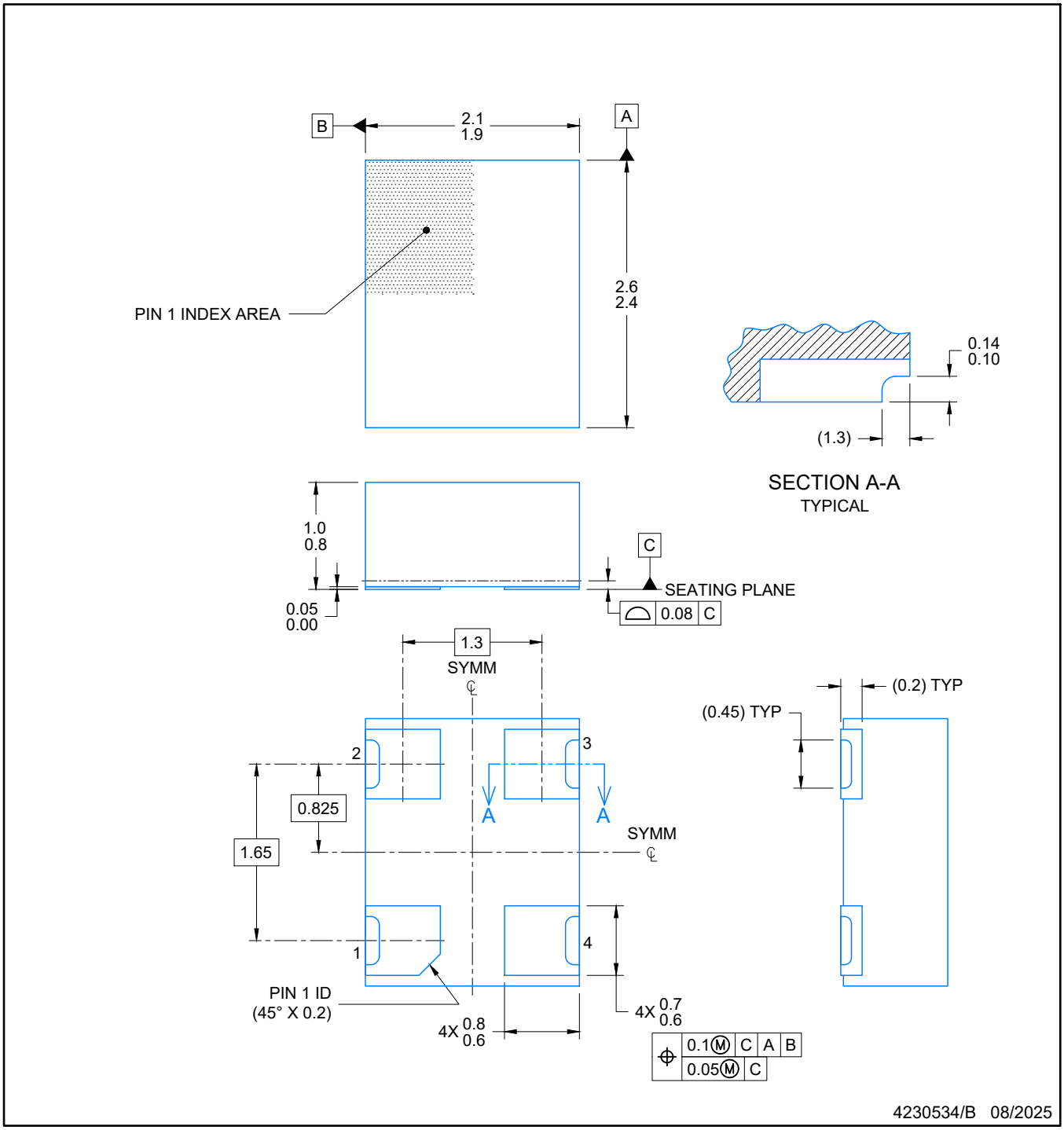
4231598/A

PACKAGE OUTLINE

DLF0004B

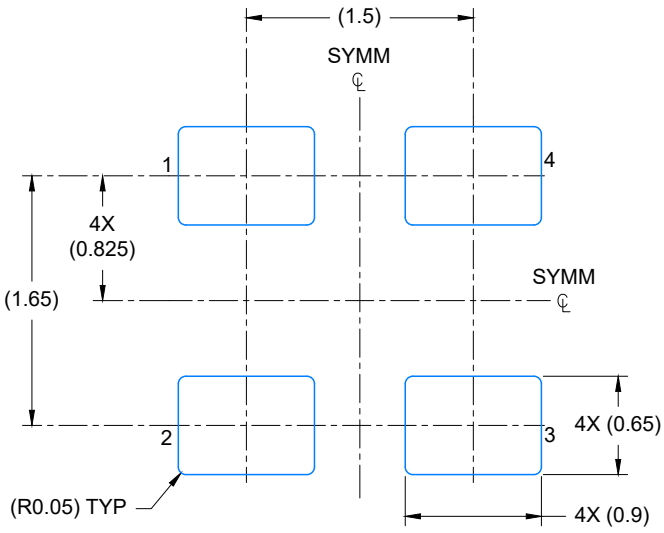
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

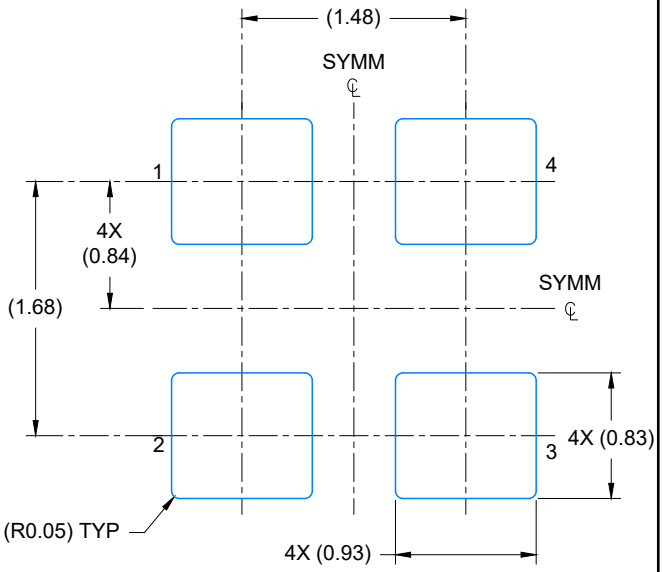


NOTES:

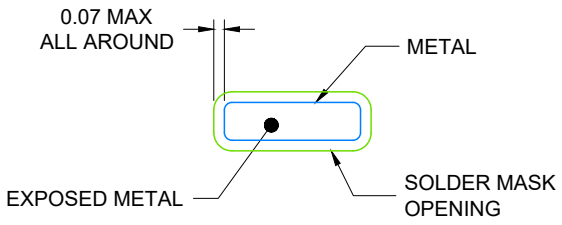
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



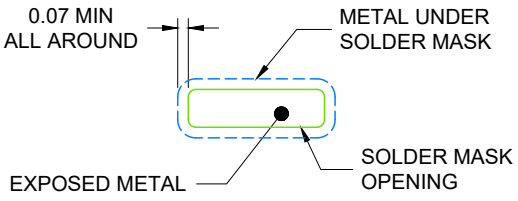
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)



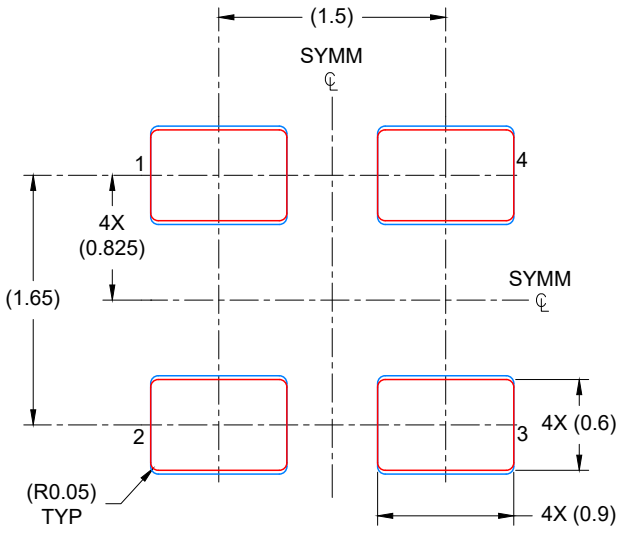
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4230534/B 08/2025

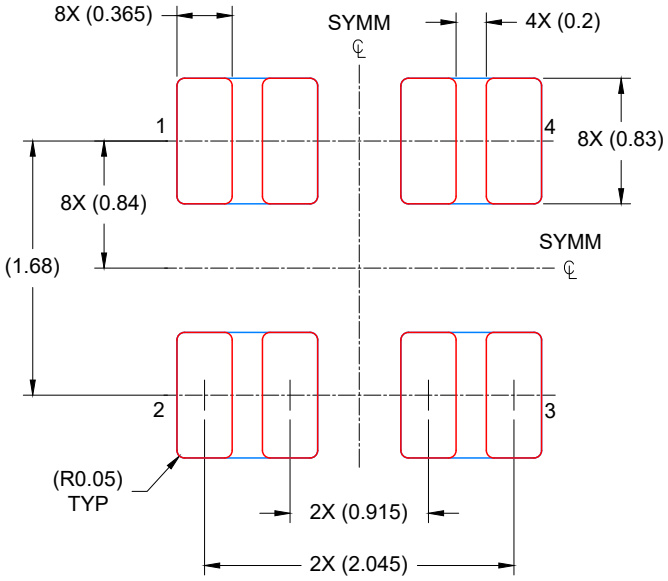
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 92%
SCALE: 20X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

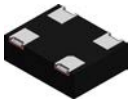
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 83%
SCALE: 20X

4230534/B 08/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

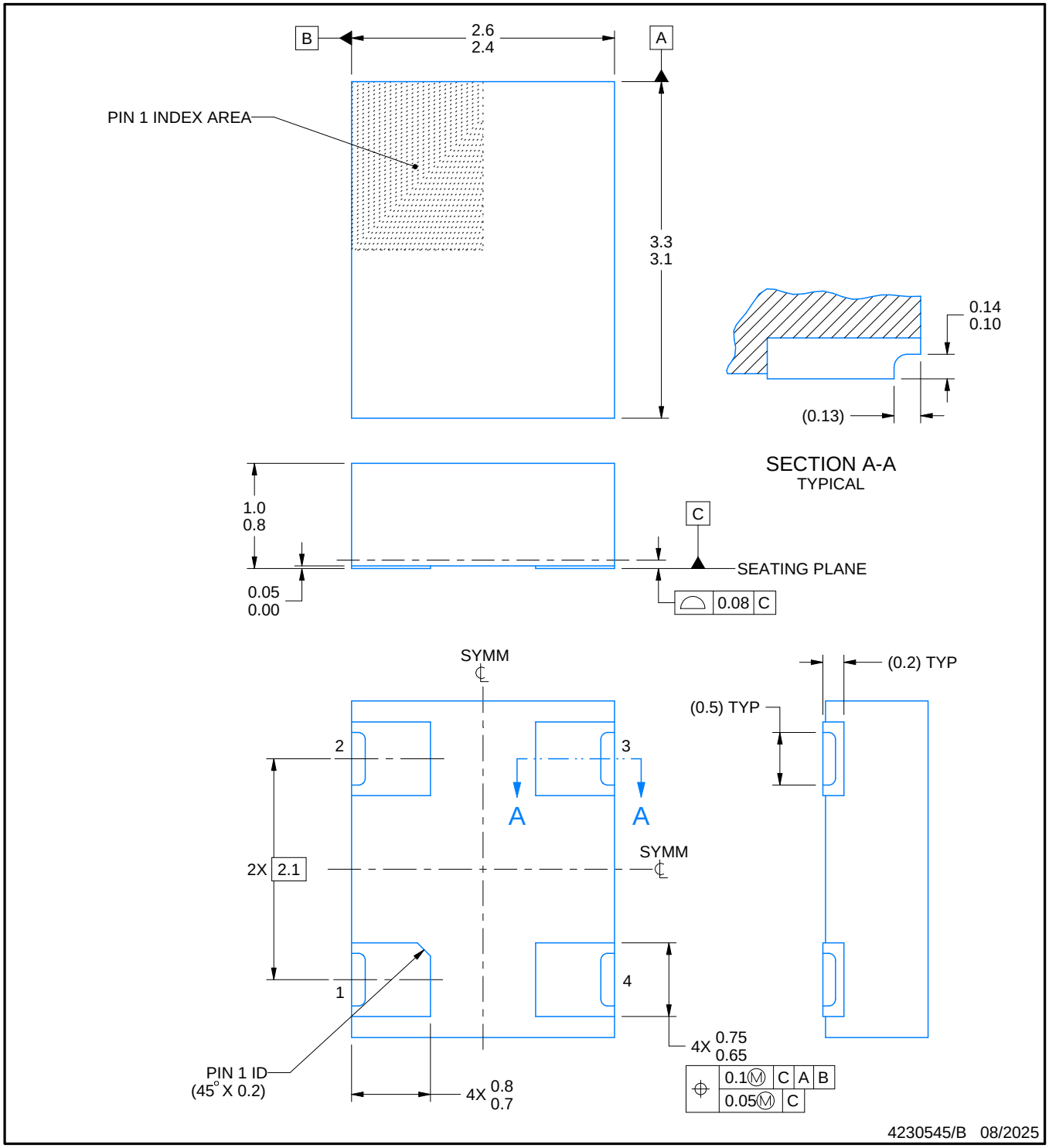
DLN0004A



PACKAGE OUTLINE

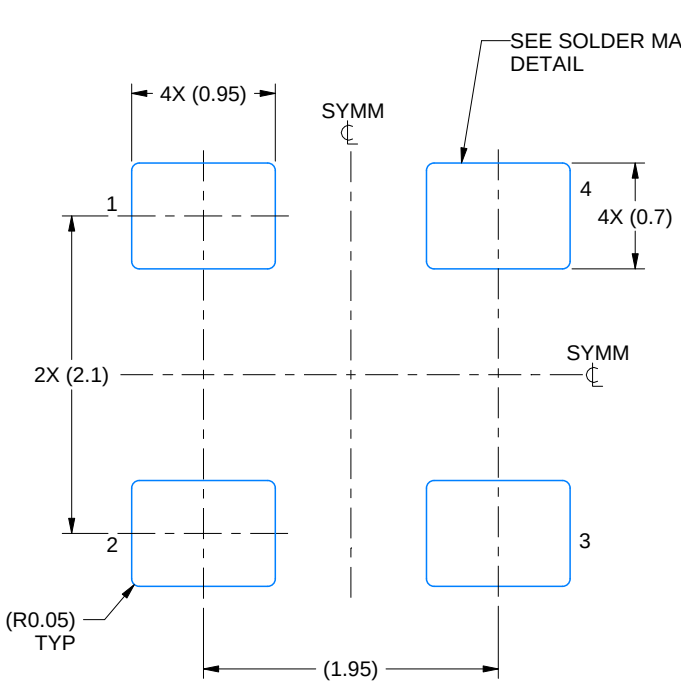
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

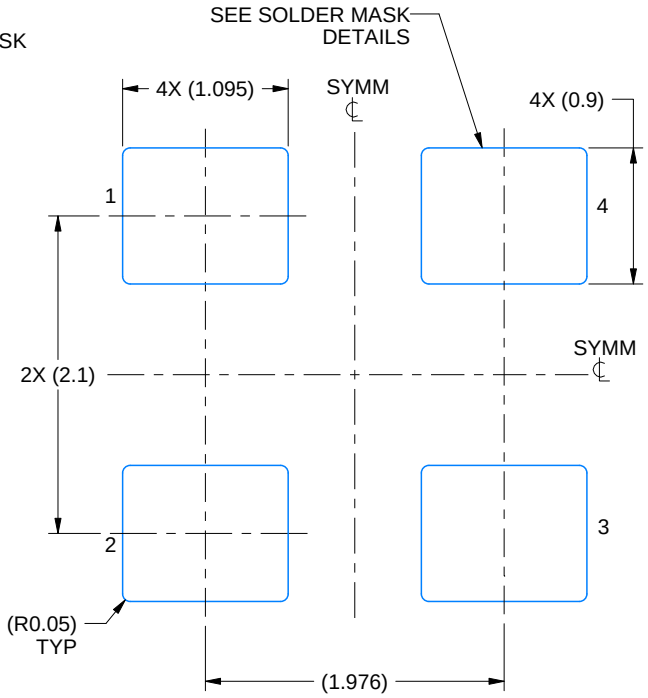


NOTES:

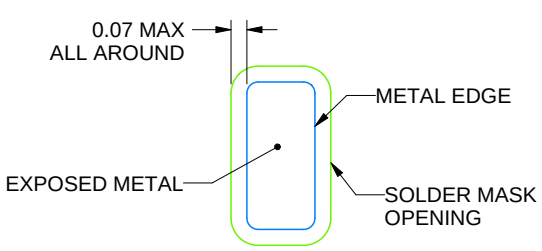
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



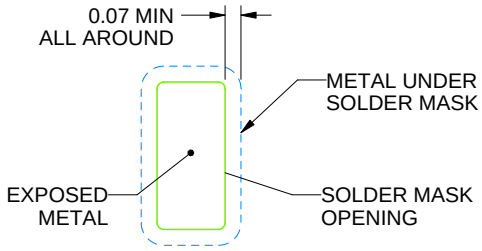
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4230545/B 08/2025

NOTES: (continued)

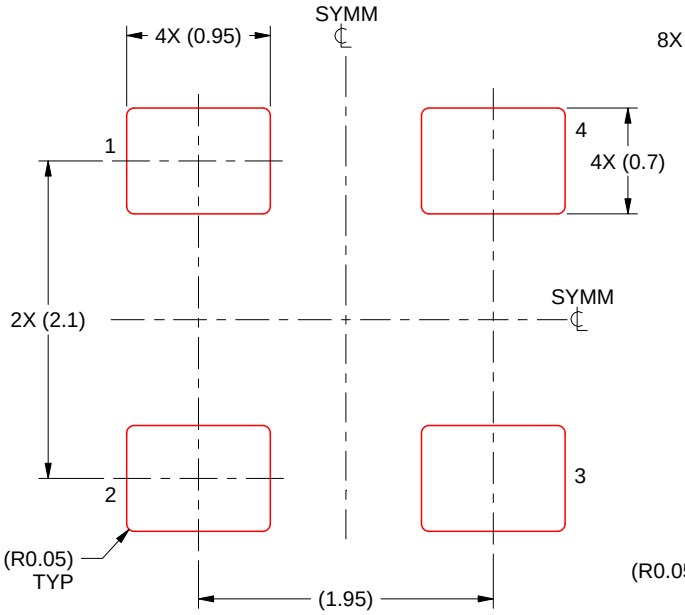
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

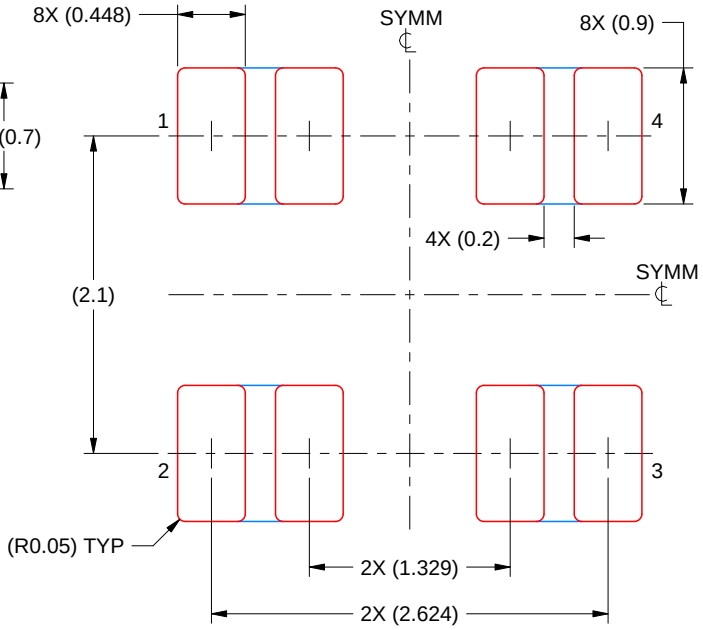
DLN0004A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 81%

4230545/B 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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