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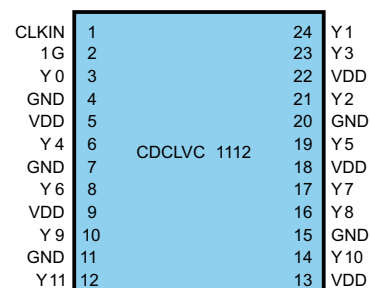
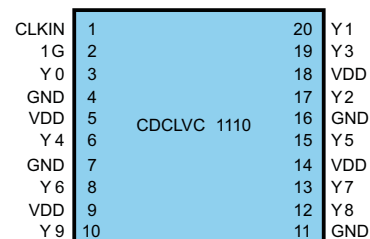
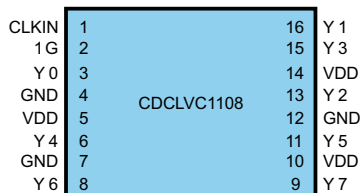
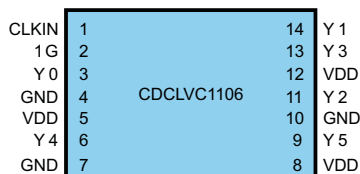
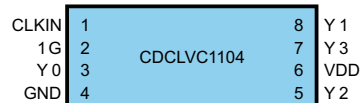
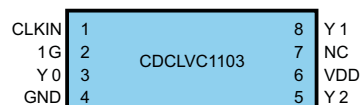
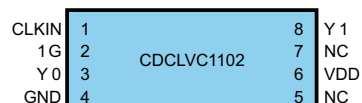
4 Revision History

Changes from Revision A (October 2014) to Revision B	Page
• Changed Packaging name from <i>TTSOP</i> to <i>TSSOP</i> in <i>Device Information Table</i>	1
• Changed CDCLVC1110 Y8 pin number from: 10 to: 12	3
• Changed CDCLVC1110 Y9 pin number from: — to: 10.....	3
• Moved T_{stg} from <i>ESD Ratings</i> to <i>Absolute Maximum Ratings</i>	5
• Added <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections.....	15

Changes from Original (May 2010) to Revision A	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Pin Configuration and Functions

PW Package
8-, 14-, 16-, 20, 24-Pin TSSOP
Top View



Pin Functions

PIN								TYPE	DESCRIPTION
NAME	CDCLVC 1102	CDCLVC 1103	CDCLVC 1104	CDCLVC 1106	CDCLVC 1108	CDCLVC 1110	CDCLVC 1112		
LVCMOS CLOCK INPUT									
CLKIN	1	1	1	1	1	1	1	Input	Input Pin
CLOCK OUTPUT ENABLE									
1G	2	2	2	2	2	2	2	Input	Output Enable
LVCMOS CLOCK OUTPUT									
Y0	3	3	3	3	3	3	3	Output	LVCMOS output. Unused outputs can be left floating.
Y1	8	8	8	14	16	20	24		
Y2	—	5	5	11	13	17	21		
Y3	—	—	7	13	15	19	23		
Y4	—	—	—	6	6	6	6		
Y5	—	—	—	9	11	15	19		
Y6	—	—	—	—	8	8	8		
Y7	—	—	—	—	9	13	17		
Y8	—	—	—	—	—	12	16		
Y9	—	—	—	—	—	10	10		
Y10	—	—	—	—	—	—	14		
Y11	—	—	—	—	—	—	12		
SUPPLY VOLTAGE									
V _{DD}	6	6	6	5	5	5	5	Power	2.5-V or device supply
						9			
				9	13				
				8	10	14	18		
				12	14	18	22		
GROUND									

Pin Functions (continued)

NAME	PIN							TYPE	DESCRIPTION
	CDCLVC 1102	CDCLVC 1103	CDCLVC 1104	CDCLVC 1106	CDCLVC 1108	CDCLVC 1110	CDCLVC 1112		
GND	4	4	4	4	4	4	4	GND	Device ground
							7		
				7	7	11	11		
				10	12	16	15		
							20		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	–0.5	4.6	V
V _{IN}	Input voltage ⁽²⁾	–0.5	V _{DD} + 0.5	V
V _O	Output voltage ⁽²⁾	–0.5	V _{DD} + 0.5	V
I _{IN}	Input current	–20	20	mA
I _O	Continuous output current	–50	50	mA
T _J	Maximum junction temperature		125	°C
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	3.3-V supply	3.0	3.3	V
		2.5-V supply	2.3	2.5	
V _{IL}	Low-level input voltage	V _{DD} = 3.0 V to 3.6 V	V _{DD} /2 – 600		mV
		V _{DD} = 2.3 V to 2.7 V	V _{DD} /2 – 400		
V _{IH}	High-level input voltage	V _{DD} = 3.0 V to 3.6 V	V _{DD} /2 + 600		mV
		V _{DD} = 2.3 V to 2.7 V	V _{DD} /2 + 400		
V _{th}	Input threshold voltage	V _{DD} = 2.3 V to 3.6 V	V _{DD} /2		mV
t _r / t _f	Input slew rate		1	4	V/ns
t _w	Minimum pulse width at CLKIN	V _{DD} = 3.0 V to 3.6 V	1.8		ns
		V _{DD} = 2.3 V to 2.7 V	2.75		
f _{CLK}	LVCMOS clock Input Frequency	V _{DD} = 3.0 V to 3.6 V	DC	250	MHz
		V _{DD} = 2.3 V to 2.7 V	DC	180	
T _A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CDCLVC1102 CDCLVC1103 CDCLVC1104	CDCLVC1106	CDCLVC1108	CDCLVC11010	CDCLVC1112	UNIT
		PW (TSSOP)					
		8 PINS	14 PINS	16 PINS	20 PINS	24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	149.4	112.6	108.4	83.0	87.9	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance ⁽³⁾	69.4	48.0	33.6	32.3	26.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I _{DD}	Static device current ⁽²⁾	1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V		6	10	mA
		1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 2.7 V		3	6	
I _{PD}	Power-down current	1G = 0 V; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V or 2.7 V			60	μA
C _{PD}	Power dissipation capacitance per output ⁽³⁾	V _{DD} = 3.3 V; f = 10 MHz		6		pF
		V _{DD} = 2.5 V; f = 10 MHz		4.5		
I _I	Input leakage current at 1G	V _I = 0 V or V _{DD} ; V _{DD} = 3.6 V or 2.7 V		8	8	μA
	Input leakage current at CLKIN			25	25	
R _{OUT}	Output impedance	V _{DD} = 3.3 V		45		Ω
		V _{DD} = 2.5 V		60		
f _{OUT}	Output frequency	V _{DD} = 3 V to 3.6 V		DC	250	MHz
		V _{DD} = 2.3 V to 2.7 V		DC	180	
OUTPUT PARAMETERS FOR V _{DD} = 3.3 V ± 0.3 V						
V _{OH}	High-level output voltage	V _{DD} = 3 V, I _{OH} = −0.1 mA		2.9		V
		V _{DD} = 3 V, I _{OH} = −8 mA		2.5		
		V _{DD} = 3 V, I _{OH} = −12 mA		2.2		
V _{OL}	Low-level output voltage	V _{DD} = 3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DD} = 3 V, I _{OL} = 8 mA			0.5	
		V _{DD} = 3 V, I _{OL} = 12 mA			0.8	
OUTPUT PARAMETERS FOR V _{DD} = 2.5 V ± 0.2 V						
V _{OH}	High-level output voltage	V _{DD} = 2.3 V, I _{OH} = −0.1 mA		2.2		V
		V _{DD} = 2.3 V, I _{OH} = −8 mA		1.7		
V _{OL}	Low-level output voltage	V _{DD} = 2.3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DD} = 2.3 V, I _{OL} = 8 mA			0.5	

- (1) All typical values are at respective nominal V_{DD}. For switching characteristics, outputs are terminated to 50 Ω to V_{DD}/2 (see [Figure 3](#)).
- (2) For dynamic I_{DD} over frequency see and [Figure 1](#).
- (3) This is the formula for the power dissipation calculation (see and the [Power Considerations](#) section).

$$P_{\text{tot}} = P_{\text{stat}} + P_{\text{dyn}} + P_{\text{Cload}} \text{ [W]}$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} \text{ [W]}$$

$$P_{\text{dyn}} = C_{\text{PD}} \times V_{\text{DD}}^2 \times f \text{ [W]}$$

$$P_{\text{Cload}} = C_{\text{load}} \times V_{\text{DD}}^2 \times f \times n \text{ [W]}$$
 n = Number of switching output pins

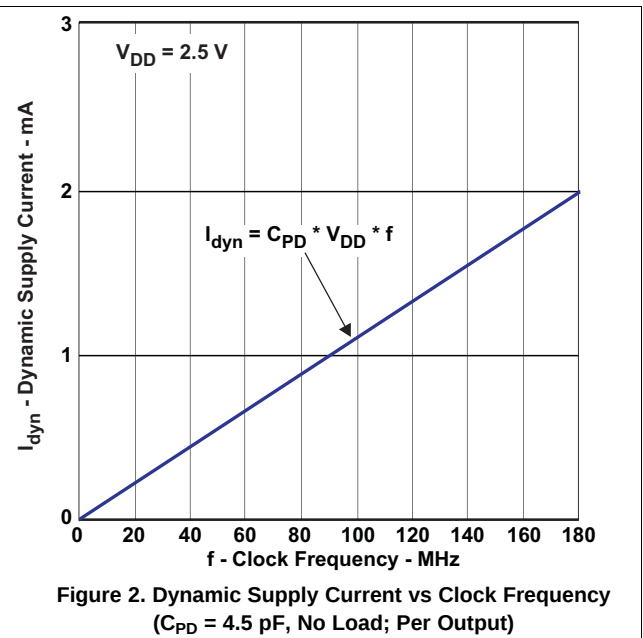
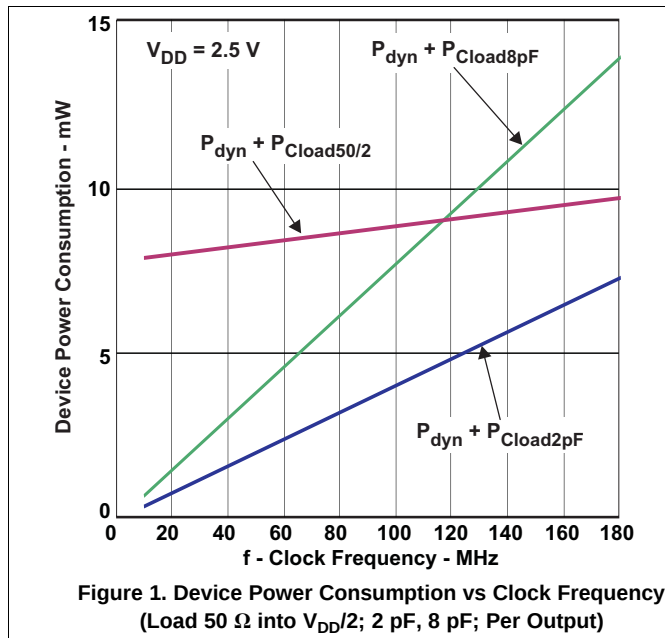
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT PARAMETERS FOR $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$					
t_{PLH} , t_{PHL} Propagation delay	CLKIN to Yn	0.8		2.0	ns
$t_{sk(o)}$ Output skew	Equal load of each output			50	ps
t_r/t_f Rise and fall time	20%–80% ($V_{OH} - V_{OL}$)	0.3		0.8	ns
t_{DIS} Output disable time	1G to Yn			6	ns
t_{EN} Output enable time	1G to Yn			6	ns
$t_{sk(p)}$ Pulse skew ; $t_{PLH(Yn)} - t_{PHL(Yn)}$ ⁽¹⁾	To be measured with input duty cycle of 50%			180	ps
$t_{sk(pp)}$ Part-to-part skew	Under equal operating conditions for two parts			0.5	ns
t_{jitter} Additive jitter rms ⁽²⁾	12 kHz to 20 MHz, $f_{OUT} = 250\text{ MHz}$			100	fs
OUTPUT PARAMETERS FOR $V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$					
t_{PLH} , t_{PHL} Propagation delay	CLKIN to Yn	1		2.6	ns
$t_{sk(o)}$ Output skew	Equal load of each output			50	ps
t_r/t_f Rise and fall time	20%–80% reference point	0.3		1.2	ns
t_{DIS} Output disable time	1G to Yn			10	ns
t_{EN} Output enable time	1G to Yn			10	ns
$t_{sk(p)}$ Pulse skew ; $t_{PLH(Yn)} - t_{PHL(Yn)}$ ⁽¹⁾	To be measured with input duty cycle of 50%			220	ps
$t_{sk(pp)}$ Part-to-part skew	Under equal operating conditions for two parts			1.2	ns
t_{jitter} Additive jitter rms ⁽²⁾	12 kHz to 20 MHz, $f_{OUT} = 180\text{ MHz}$			350	fs

- (1) $t_{sk(p)}$ depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$; $t_{w(OUT)}$ is pulse-width of output waveform and t_{period} is $1/f_{OUT}$.
(2) Parameter is specified by characterization. Not tested in production.

6.7 Typical Characteristics



7 Parameter Measurement Information

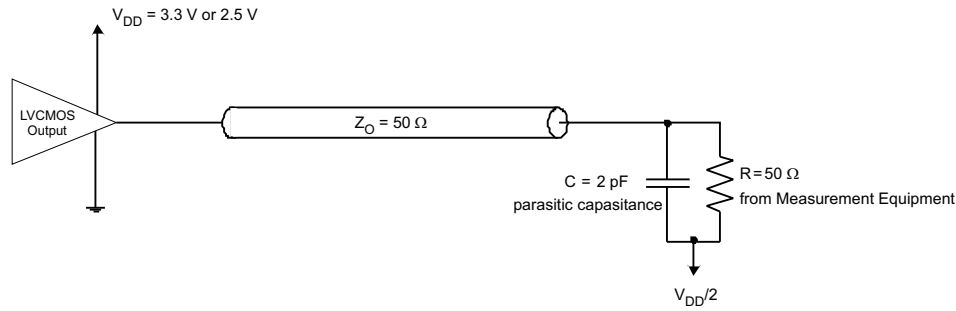


Figure 3. Test Load Circuit

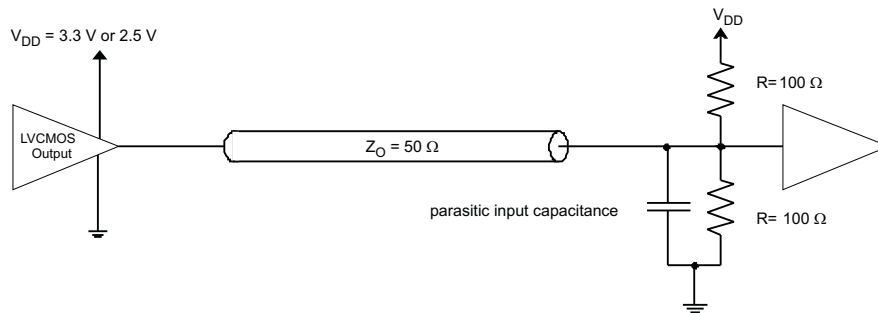


Figure 4. Application Load With 50-ohm Line Termination

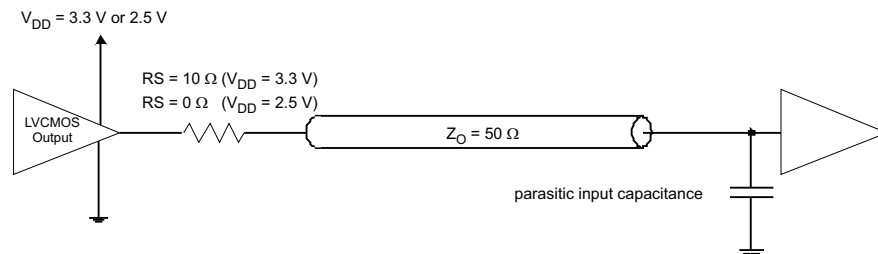


Figure 5. Application Load With Series Line Termination

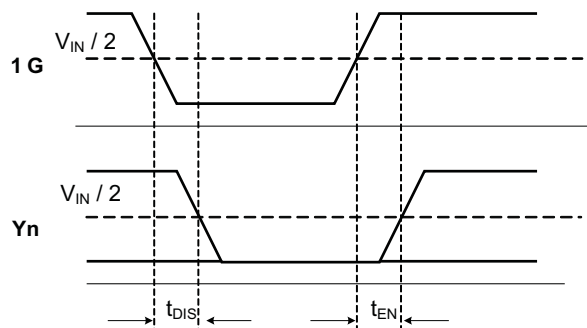


Figure 6. t_{DIS} and t_{EN} for Disable Low

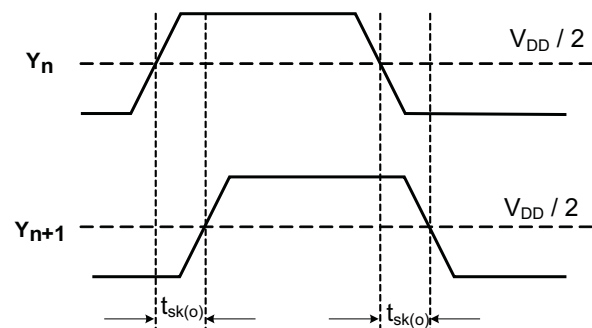
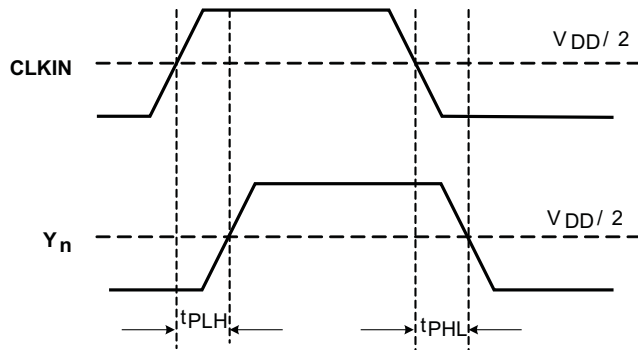


Figure 7. Output Skew $t_{sk(o)}$

Parameter Measurement Information (continued)



Note: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 8. Pulse Skew $t_{sk(p)}$ and Propagation Delay t_{PLH}/t_{PHL}

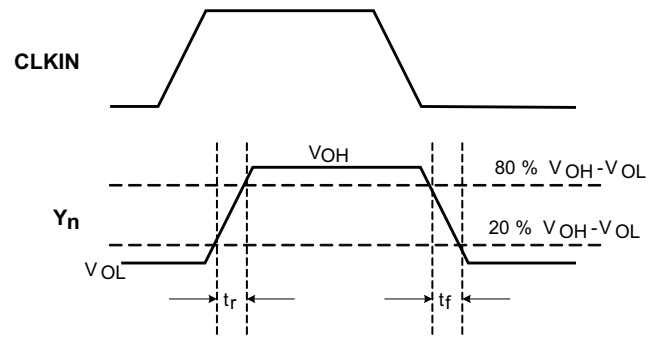


Figure 9. Rise/Fall Times t_r/t_f

8 Detailed Description

8.1 Overview

The CDCLVC11xx family of devices is a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the CDCLVC11xx's output driver with that of the transmission line. [Figure 5](#) and [Figure 6](#) show the proper configuration per configuration for both $V_{DD} = 3.3\text{ V}$ and $V_{DD} = 2.5\text{ V}$. TI recommends placing the series resistor close to the driver to minimize signal reflection.

8.2 Functional Block Diagram

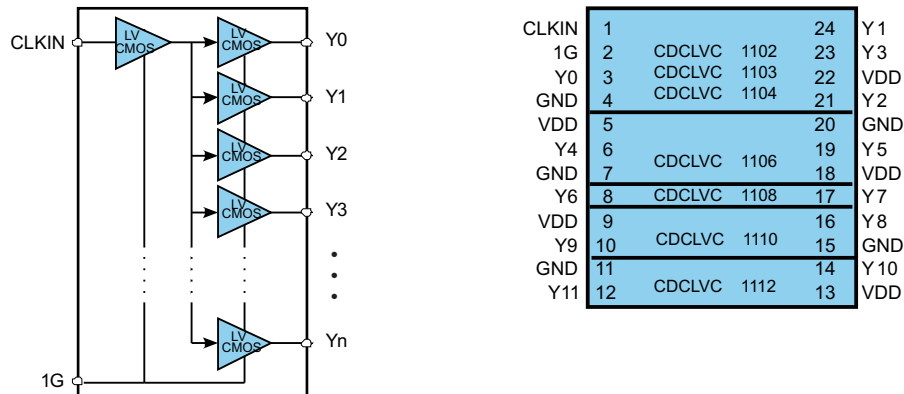


Table 1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

8.3 Feature Description

The outputs of the CDCLVC11xx can be disabled by driving the asynchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. All supply and ground pins must be connected to V_{DD} and GND, respectively.

8.4 Device Functional Modes

The CDCLVC11xx operates from supplies between 2.5 V and 3.3 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCLVC11xx family is a low additive jitter LVCMOS buffer solution that can operate up to 250 MHz at and 180 MHz at $V_{DD} = 2.5$ V. Low output skew as well as the ability for asynchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

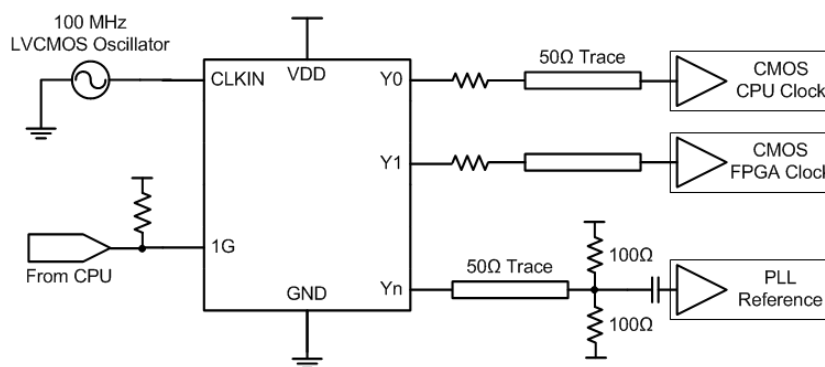


Figure 10. Example System Configuration

9.2.1 Design Requirements

The CDCLVC11xx shown in [Figure 10](#) is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the CDCLVC11xx to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the CDCLVC11xx.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

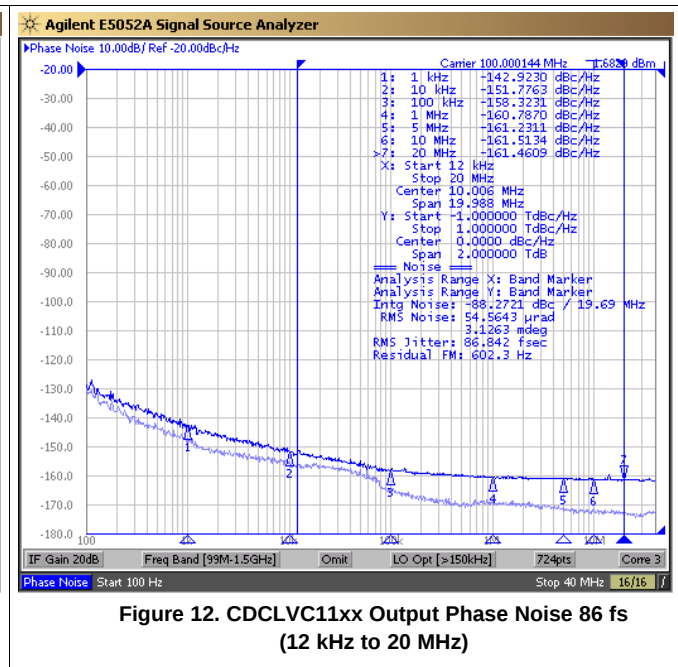
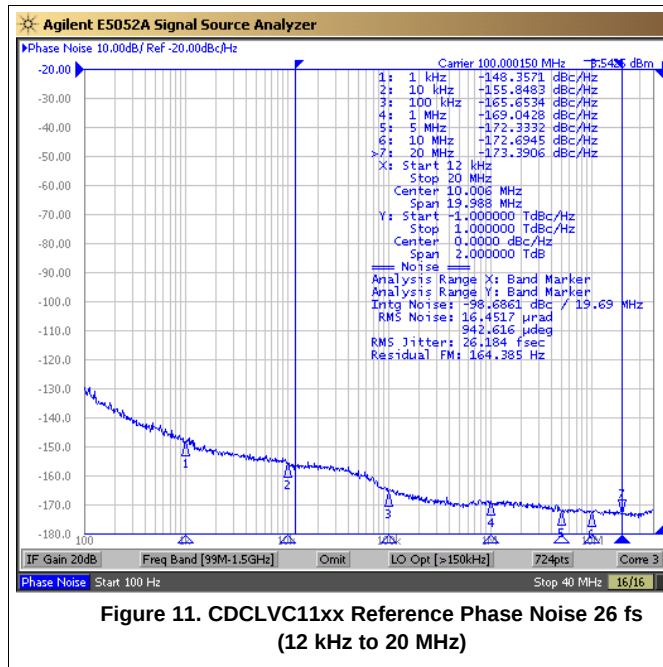
9.2.2 Detailed Design Procedure

Refer to [Figure 5](#) and the [Electrical Characteristics](#) table to determine the appropriate series resistance needed for matching the output impedance of the CDCLVC11xx to that of the characteristic impedance of the transmission line.

Unused outputs can be left floating. See the [Power Supply Recommendations](#) section for recommended filtering techniques.

Typical Application (continued)

9.2.3 Application Curves



The low additive jitter of the CDCLVC11xx can be shown in the previous application example. The low-noise 100-MHz XO with 26-fs RMS jitter drives the CDCLVC11xx, resulting in 86-fs RMS jitter when integrated from 12 kHz to 20 MHz. The resultant additive jitter is a low 82-fs RMS for this configuration.

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 13 shows this recommended power supply decoupling method.

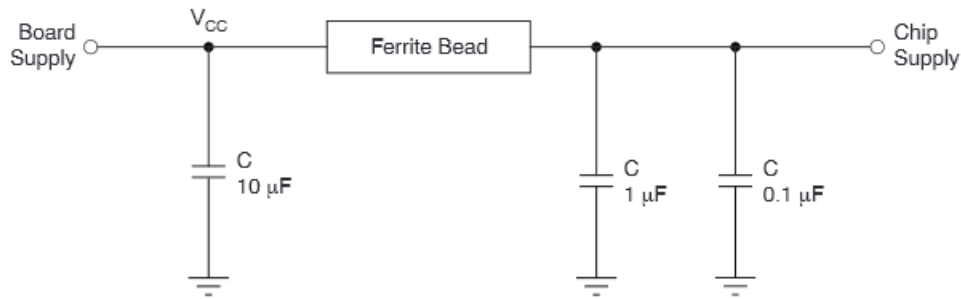


Figure 13. Power Supply Decoupling

10.1 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states.
- Power required to charge any output load.

The output load can be capacitive only or capacitive and resistive. The following formula and the power graphs in and Figure 1 can be used to obtain the power consumption of the device:

$$P_{\text{dev}} = P_{\text{stat}} + n (P_{\text{dyn}} + P_{\text{Cload}})$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}}$$

$$P_{\text{dyn}} + P_{\text{Cload}} = \text{see and Figure 1}$$

where:

V_{DD} = Supply voltage (or 2.5 V)

I_{DD} = Static device current (typical 6 mA for $V_{\text{DD}} = 3.3$ V; typical 3 mA for $V_{\text{DD}} = 2.5$ V)

n = Number of switching output pins

Example for device power consumption for CDCLVC1104: four outputs are switching, $f = 120$ MHz, $V_{\text{DD}} = 3.3$ V, and $C_{\text{load}} = 2$ pF per output:

$$P_{\text{dev}} = P_{\text{stat}} + n (P_{\text{dyn}} + P_{\text{Cload}}) = 19.8 \text{ mW} + 40 \text{ mW} = 59.8 \text{ mW}$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} = 6 \text{ mA} \times 3.3 \text{ V} = 19.8 \text{ mW}$$

$$n (P_{\text{dyn}} + P_{\text{Cload}}) = 4 \times 10 \text{ mW} = 40 \text{ mW}$$

NOTE

For dimensioning the power supply, the total power consumption must be considered. The total power consumption is the sum of the device power consumption and the power consumption of the load.

11 Layout

11.1 Layout Guidelines

Figure 14 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example

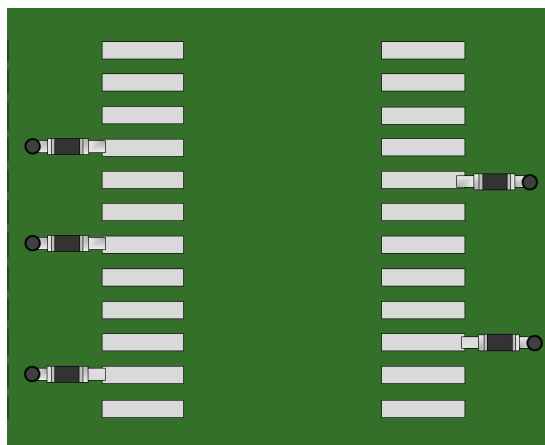


Figure 14. PCB Conceptual Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CDCLVC1102	Click here	Click here	Click here	Click here	Click here
CDCLVC1103	Click here	Click here	Click here	Click here	Click here
CDCLVC1104	Click here	Click here	Click here	Click here	Click here
CDCLVC1106	Click here	Click here	Click here	Click here	Click here
CDCLVC1108	Click here	Click here	Click here	Click here	Click here
CDCLVC1110	Click here	Click here	Click here	Click here	Click here
CDCLVC1112	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCLVC1102PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1102PW.B	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1102PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1102PWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1102PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1102PWRG4.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C2
CDCLVC1103PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1103PW.B	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1103PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1103PWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1103PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1103PWRG4.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C3
CDCLVC1104PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1104PW.B	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1104PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1104PWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1104PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1104PWRG4.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C4
CDCLVC1106PW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1106PW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1106PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1106PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1106PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1106PWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C6
CDCLVC1108PW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8
CDCLVC1108PW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8
CDCLVC1108PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8
CDCLVC1108PWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8
CDCLVC1108PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCLVC1108PWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9C8
CDCLVC1110PW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1110PW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1110PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1110PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1110PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1110PWRG4.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CA
CDCLVC1112PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC
CDCLVC1112PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC
CDCLVC1112PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC
CDCLVC1112PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC
CDCLVC1112PWRG4	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC
CDCLVC1112PWRG4.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C9CC

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

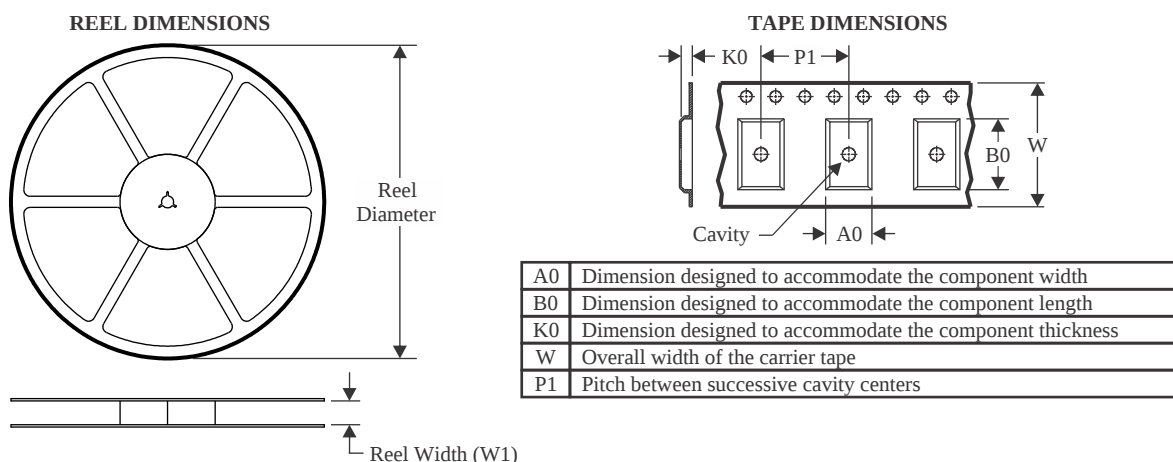
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

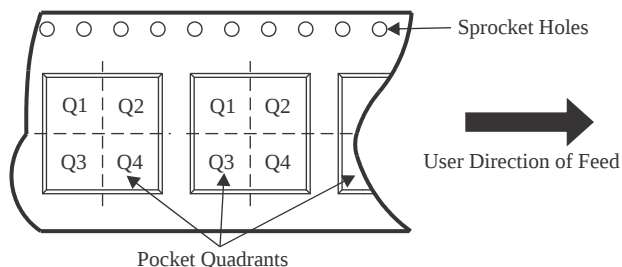
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVC1102PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1102PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1103PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1103PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1104PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1104PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1106PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1106PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1108PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1108PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1110PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CDCLVC1110PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CDCLVC1112PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CDCLVC1112PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

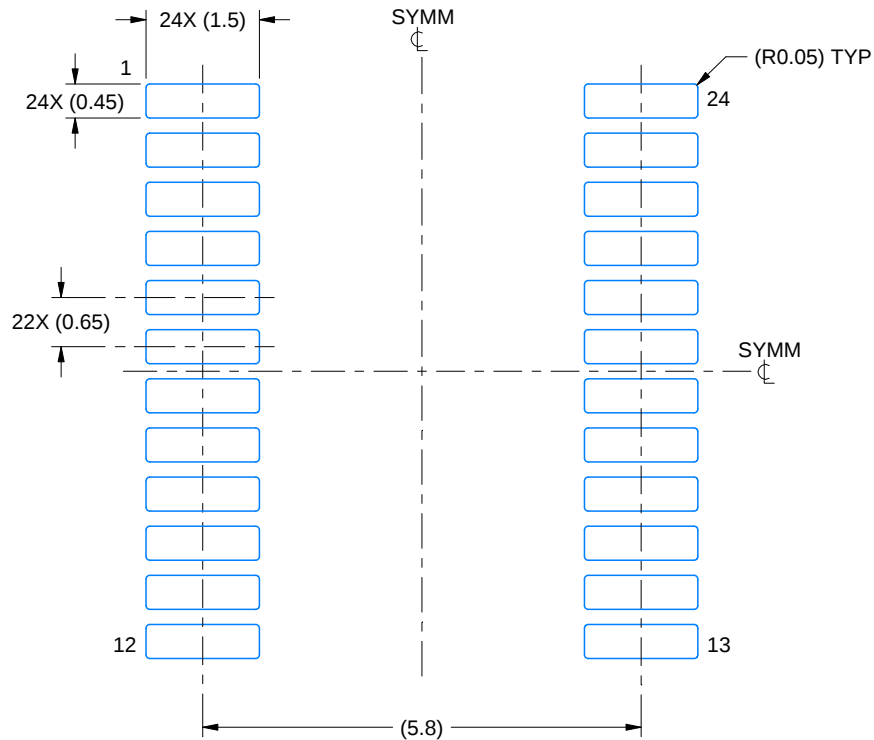
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVC1102PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1102PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1103PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1103PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1104PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1104PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
CDCLVC1106PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
CDCLVC1106PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
CDCLVC1108PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CDCLVC1108PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
CDCLVC1110PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
CDCLVC1110PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
CDCLVC1112PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
CDCLVC1112PWRG4	TSSOP	PW	24	2000	353.0	353.0	32.0

EXAMPLE BOARD LAYOUT

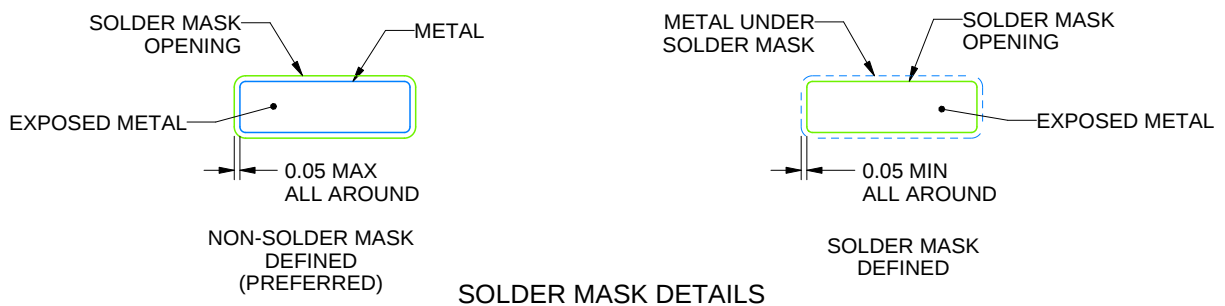
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

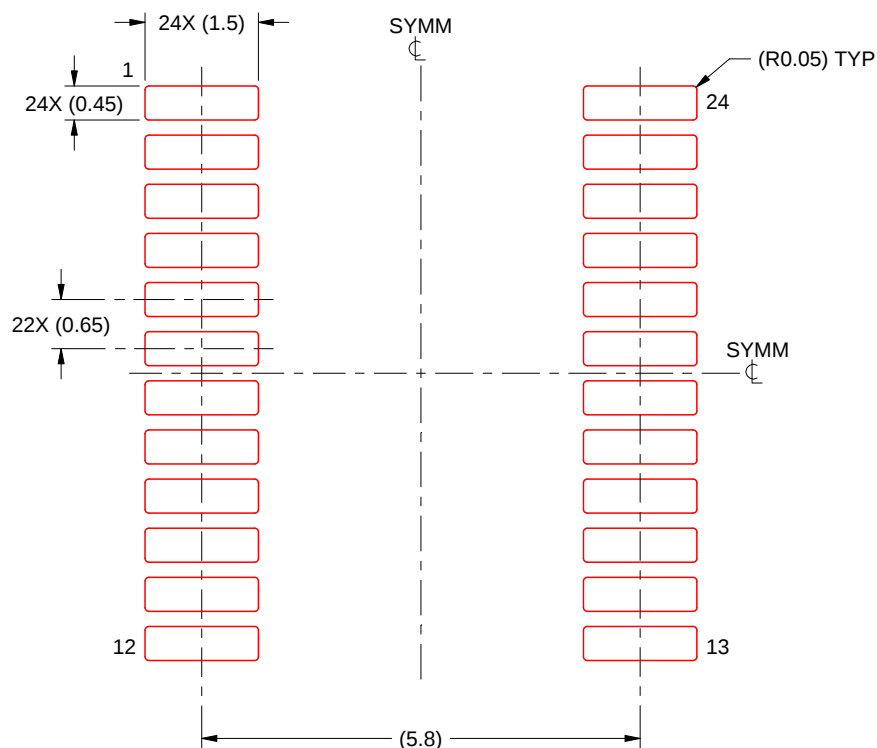
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

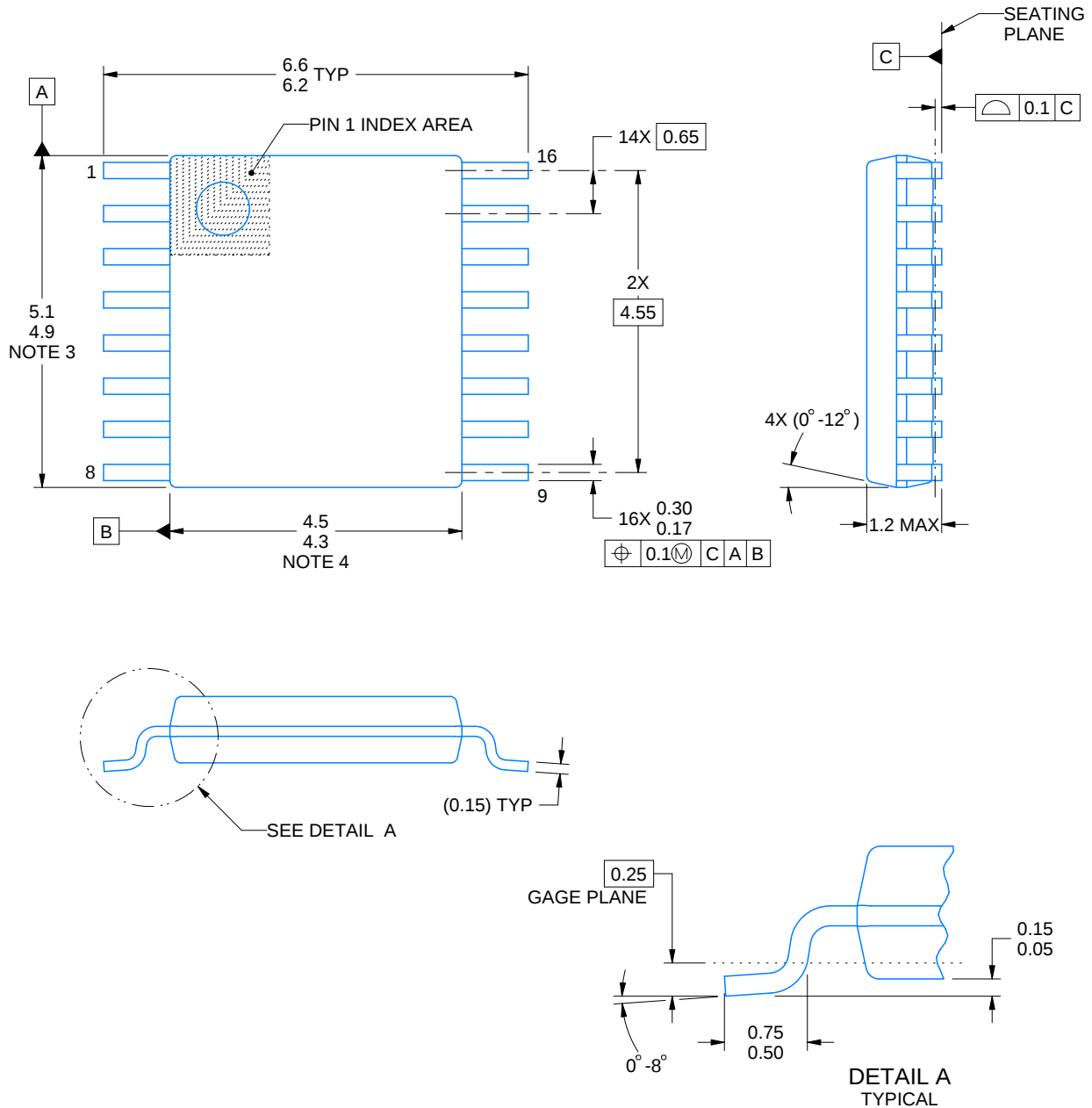


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

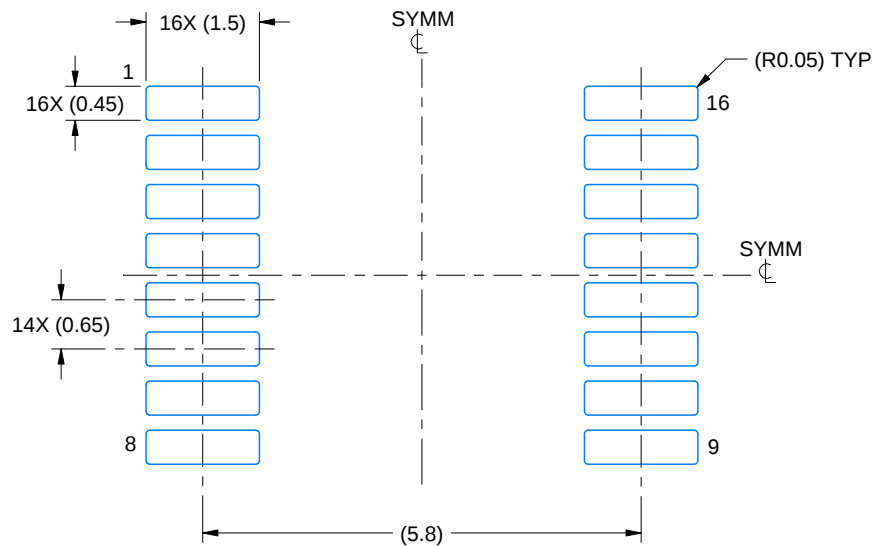
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

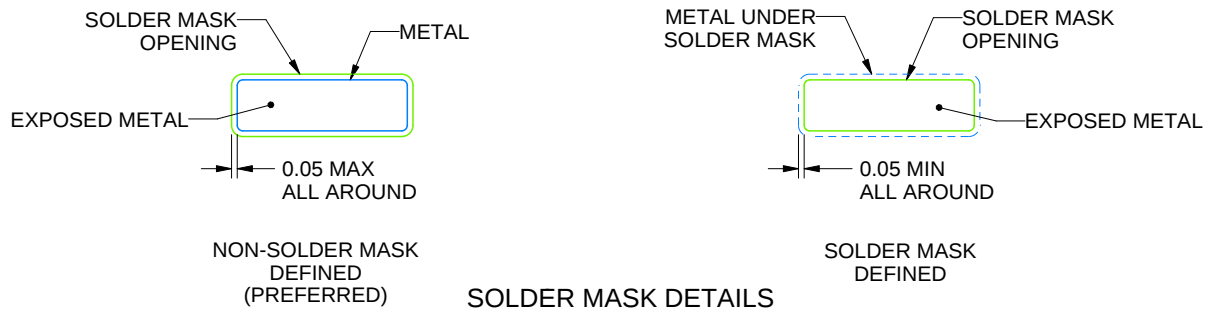
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

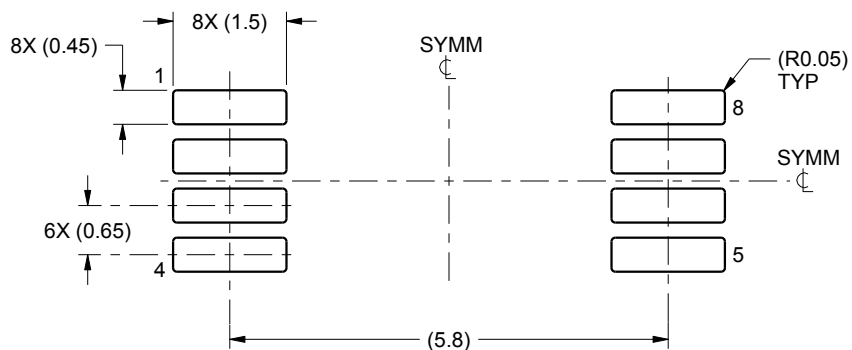
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

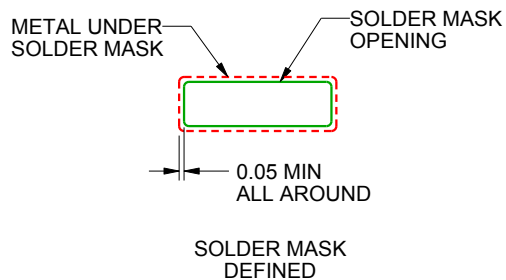
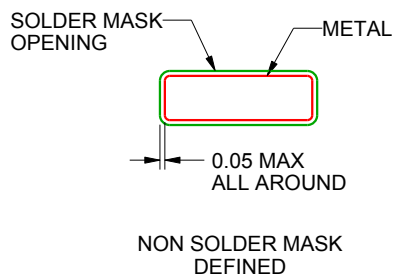
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

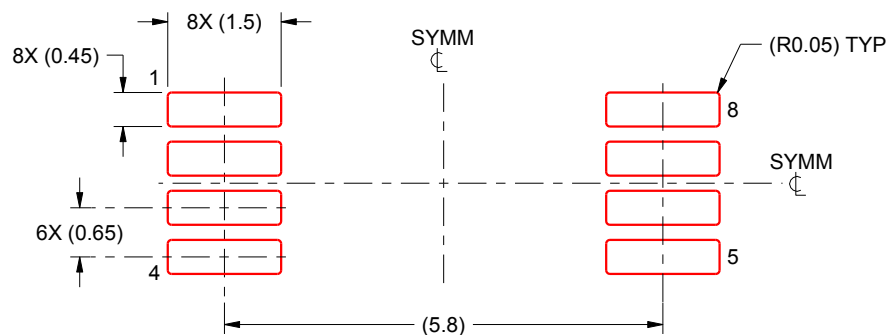
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

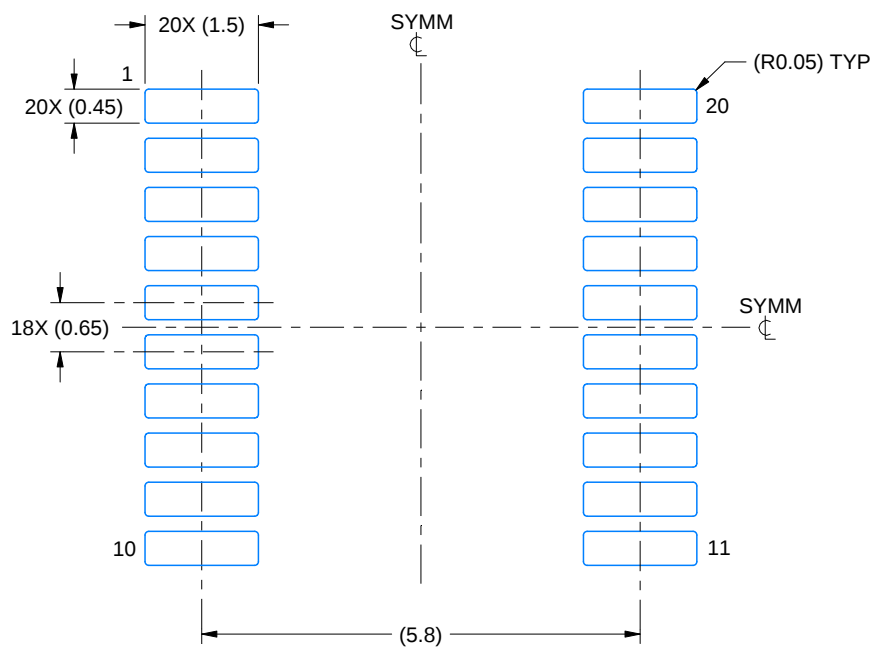
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

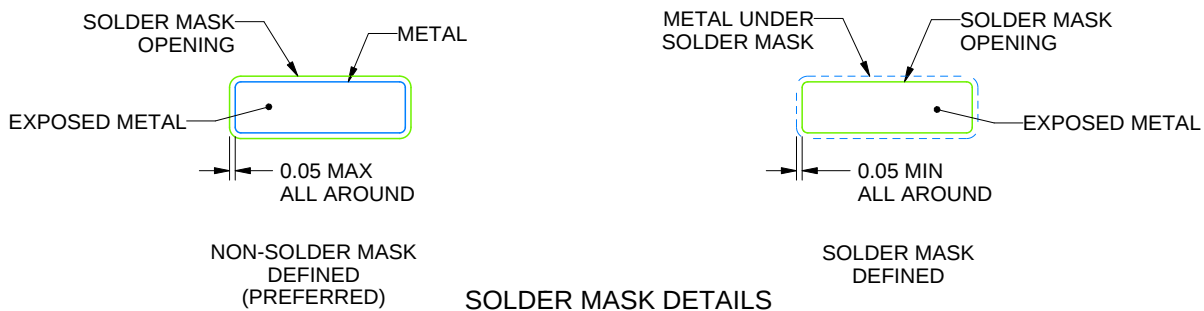
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

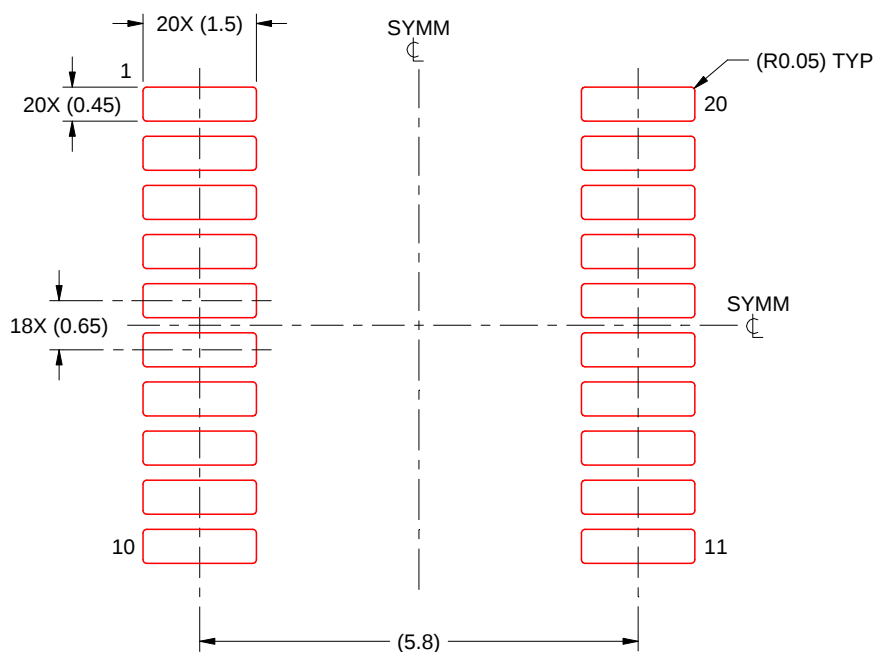
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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