# CDCS504-Q1 Clock Buffer and Clock Multiplier

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Part of a Family of Easy-to-Use Clock Generator Devices
- Clock Multiplier With Selectable Output Frequency
- Frequency Multiplication Selectable Between x1 or x4 With One External Control Pin
- Output Disable Through Control Pin
- Single 3.3-V Device Power Supply
- Wide Temperature Range: –40°C to 105°C
- Low Space Consumption 8-Pin TSSOP Package
- Create a Custom Design Using the CDCS504-Q1 With the WEBENCH® Power Designer

## 2 Applications

Automotive Applications Requiring Clock Multiplication

## 3 Description

The CDCS504-Q1 device is a LVCMOS input clock buffer with selectable frequency multiplication.

The CDCS504-Q1 has an output enable pin.

The device accepts a 3.3-V LVCMOS signal at the input.

The input signal is processed by a phased-locked loop (PLL), whose output frequency is either equal to the input frequency or multiplied by the factor of four.

By this, the device can generate output frequencies between 2 MHz and 108 MHz.

A separate control pin can be used to enable or disable the output. The CDCS504-Q1 device operates in a 3.3-V environment.

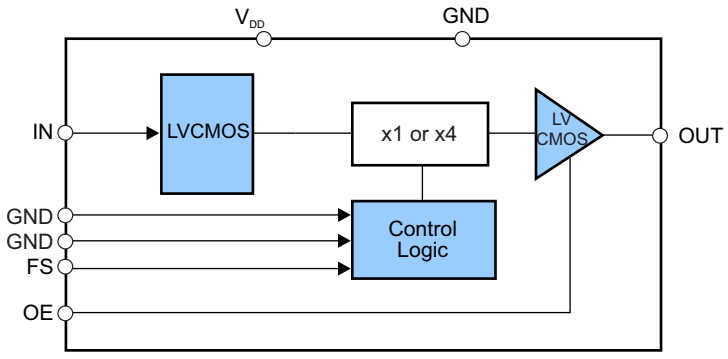
It is characterized for operation from –40°C to 105°C and is available in an 8-pin TSSOP package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| CDCS504-Q1 | TSSOP (8) | 3.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Block Diagram**



## Table of Contents



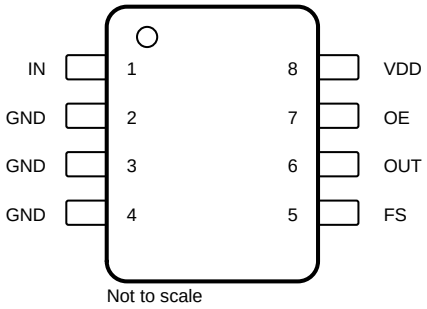
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| April 2017 | * | Initial release. |

# 5 Pin Configuration and Functions

**PW Package**
**8-Pin TSSOP**
**Top View**




Not to scale

**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| FS | 5 | I | Frequency multiplication selection, internal pullup |
| GND | 2, 3, 4 | Ground | Ground |
| IN | 1 | I | LVCMOS clock input |
| OE | 7 | I | Output enable, internal pullup |
| OUT | 6 | O | LVCMOS clock output |
| VDD | 8 | Power | 3.3-V power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 4.6 | V |
| $V_{IN}$ | Input voltage | –0.5 | 4.6 | V |
| $V_{out}$ | Output voltage | –0.5 | 4.6 | V |
| $I_{IN}$ | Input current ($V_I < 0$, $V_I > V_{DD}$) | | 20 | mA |
| $I_{out}$ | Continuous output current | | 50 | mA |
| $T_J$ | Maximum junction temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±1500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3 | | 3.6 | V |
| $f_{IN}$ | Input frequency | FS = 0 | 2 | | 27 | MHz |
| | | FS = 1 | 2 | | 27 | |
| $V_{IL}$ | Low-level input voltage LVCMOS | | | | 0.3 × $V_{DD}$ | V |
| $V_{IH}$ | High-level input voltage LVCMOS | | 0.7 × $V_{DD}$ | | | V |
| $V_I$ | Input voltage threshold LVCMOS | | | 0.5 × $V_{DD}$ | | V |
| $C_L$ | Output load test LVCMOS | | | | 15 | pF |
| $I_{OH}/I_{OL}$ | Output current | | | | ±12 | mA |
| $T_A$ | Operating free-air temperature | | –40 | | 105 | °C |

## 6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)(1)

| THERMAL METRIC(2) | | | | CDCS504-Q1 PW (TSSOP) 8 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | 179.9 | °C/W |
| | | High K | Thermal Airflow (CFM) 0 | 149 | |
| | | | Thermal Airflow (CFM) 150 | 142 | |
| | | | Thermal Airflow (CFM) 250 | 138 | |
| | | | Thermal Airflow (CFM) 500 | 132 | |
| | | Low K | Thermal Airflow (CFM) 0 | 230 | |
| | | | Thermal Airflow (CFM) 150 | 185 | |
| | | | Thermal Airflow (CFM) 250 | 170 | |
| | | | Thermal Airflow (CFM) 500 | 150 | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | | 64.9 | °C/W |
| | | High K | | 65 | |
| | | Low K | | 69 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | | 108.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | | | 9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | | | 107 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | | | n/a | °C/W |

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics – Device Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Device supply current | $f_{in}$ = 3.072 MHz; FS = 1 | | 24 | | mA |
| $f_{OUT}$ | Output frequency | FS = 0 | 2 | | 27 | MHz |
| | | FS = 1 | 8 | | 108 | |
| $I_{IH}$ | LVCMOS input current | $V_I = V_{DD}$; $V_{DD}$ = 3.6 V | | | 10 | µA |
| $I_{IL}$ | LVCMOS input current | $V_I$ = 0 V; $V_{DD}$ = 3.6 V | | | –10 | µA |
| $V_{OH}$ | LVCMOS high-level output voltage | $I_{OH}$ = -–0.1 mA | 2.9 | | | V |
| | | $I_{OH}$ = -–8 mA | 2.4 | | | |
| | | $I_{OH}$ = -–12 mA | 2.2 | | | |

## Electrical Characteristics – Device Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | LVCMOS low-level output voltage | $I_{OL}$ = 0.1 mA | | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | 0.5 | |
| | | $I_{OL}$ = 12 mA | | | 0.8 | |
| $I_{OZ}$ | High-impedance-state output current | OE = Low | –2 | | 2 | µA |
| $t_{JIT(C-C)}$ | Cycle to cycle jitter(1) | $f_{out}$ = 11.264 MHz; FS = 1, 10000 Cycles | | 144 | | ps |
| $t_r$ | Rise time(1) | 20%–80% | | 0.65 | | ns |
| $t_f$ | Fall time(1) | 20%–80% | | 0.55 | | ns |
| $O_{dc}$ | Output duty cycle(2) | | 45% | | 55% | |

(1) Measured with Test Load, see Figure 4.
(2) Not production tested.

## 6.6 Typical Characteristics

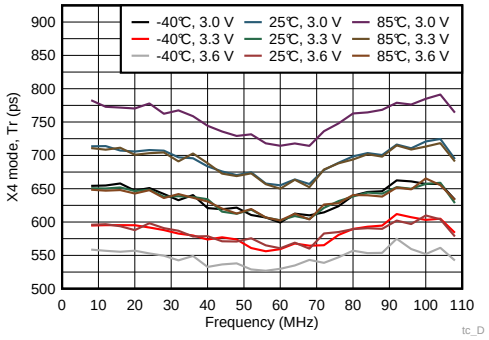



**Figure 1. Typical Tr vs Output Frequency, VDD, Temperature in X4 Mode**

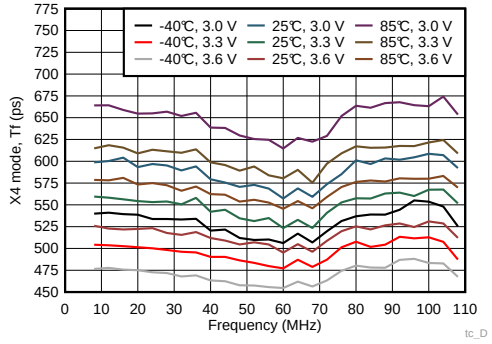
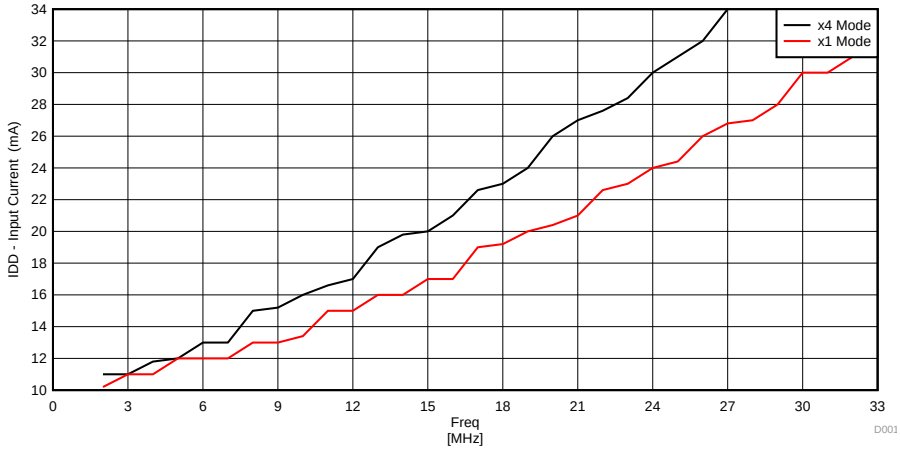



**Figure 2. Typical Tf vs Output Frequency, VDD, Temperature in X4 Mode**




$V_{CC}$ = 3.3 V, output loaded with test load

**Figure 3. $I_{DD}$ vs Input Frequency**

# 7 Parameter Measurement Information

## 7.1 Measurement Circuits

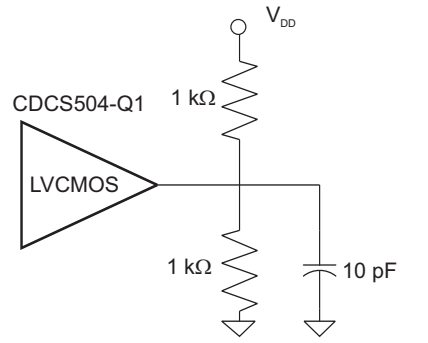





**Figure 4. Test Load**

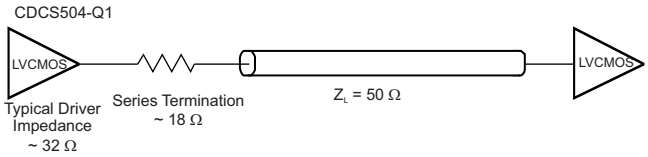




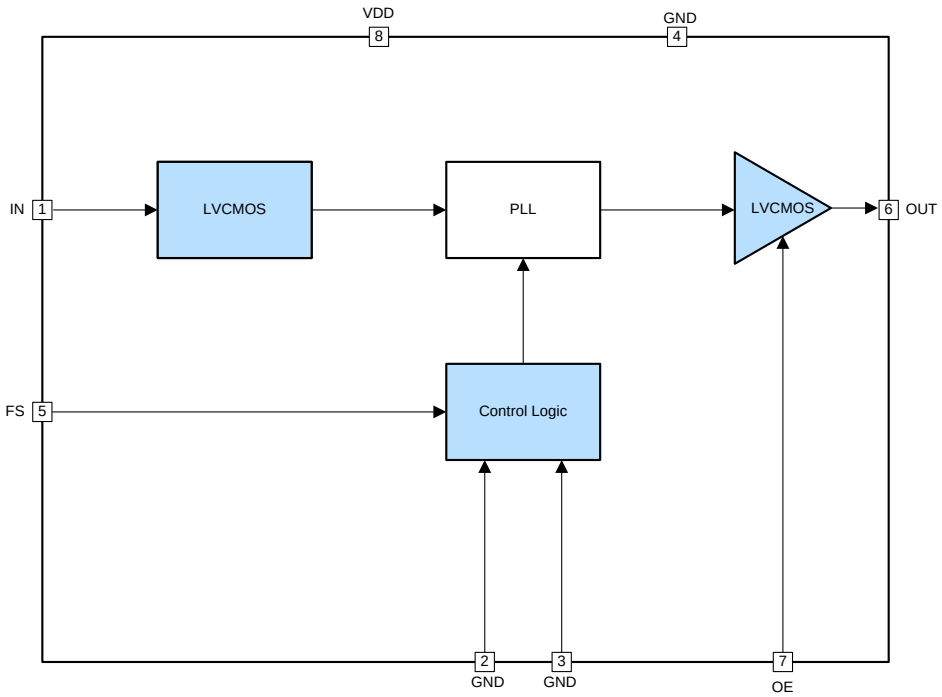

**Figure 5. Load for 50-Ω Board Environment**

# 8 Detailed Description

## 8.1 Overview

The CDCS504-Q1 is a LVCMOS clock buffer (x1 mode) or quadrupler (x4 mode). It integrates an internal PLL and generates a LVCMOS clock frequency range from 2 MHz to 108 MHz.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

The CDCS504-Q1 is qualified for automotive applications with AEC-Q100 test, which could support wide temperature range from –40°C to 105°C. The device is easy to use, only need single 3.3-V power supply. The output enable or disable mode, along with frequency multiplication, could be controlled by external controls pins.

## 8.4 Device Functional Modes

When pin 7 OE is in low, the CDCS504-Q1 outputs 3-state. When pin 7 OE is set in high, the device would output clocks, output frequency depends on pin 5 FS status. FS = high enables frequency ×4 mode. FS= low makes output frequency equal to input frequency. If no input clock is provided, it is recommended to set OE=low in order to avoid random clock pulses from the internal PLL at the outputs.

**Table 1. Function Table**

| OE | FS | $f_{OUT}/f_{IN}$ | $f_{OUT}$ at $f_{in}$ = 27 MHz |
|---|---|---|---|
| 0 | x | x | 3-state |
| 1 | 0 | 1 | 27 MHz |
| 1 | 1 | 4 | 108 MHz |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The CDCS504-Q1 is a clock buffer or multiplier for automotive amplifiers and infotainment. It is fit for the TAS6424-Q1, a four-channel, class-D, digital-input audio-amplifier, when the applications are without available MCLK. See Figure 6 for more details.

## 9.2 Typical Application

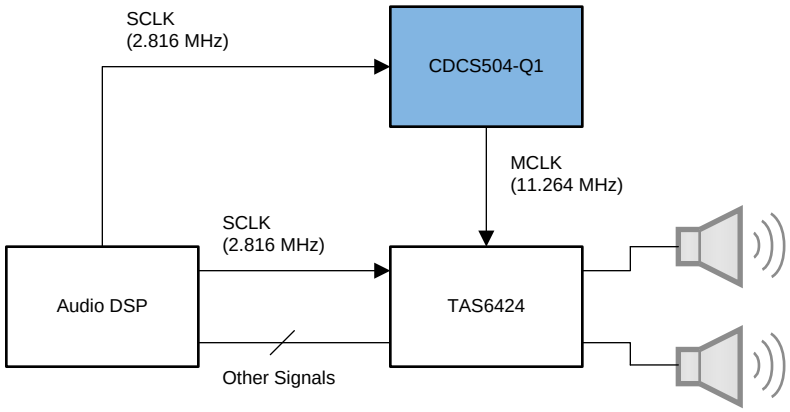





**Figure 6. Clock for Automotive Amplifiers**

### 9.2.1 Design Requirements

The CDCS504-Q1 is supplied with a single-power 3.3 V. The device supports minimum input frequency to 2 MHz. For maximum input frequency, it is 32 MHz in ×1 mode, and 27 MHz in ×4 mode. The input clock is LVCMOS type and should satisfy requirements in the *Recommended Operating Conditions*.

### 9.2.2 Detailed Design Procedure

In some applications, the clock input for CDCS504-Q1 is not always presented. In case there is an unexpected clock output without clock input, TI recommends setting OE pin to low. When it gets clock input ready, set OE pin to high to get expected clock output. If the other application presents continuous clock input for CDCS504-Q1, the OE pin could be floated, internal pullup brings output enable, or an external pullup circuits could be used fixedly.

#### *9.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the CDCS504-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

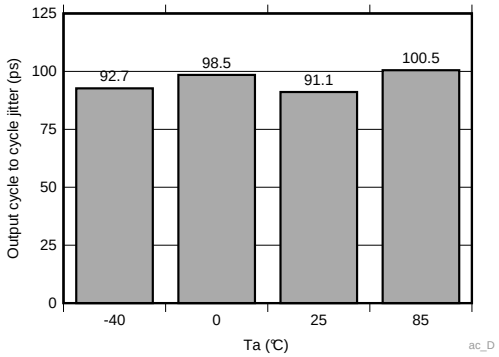
## Typical Application (continued)

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

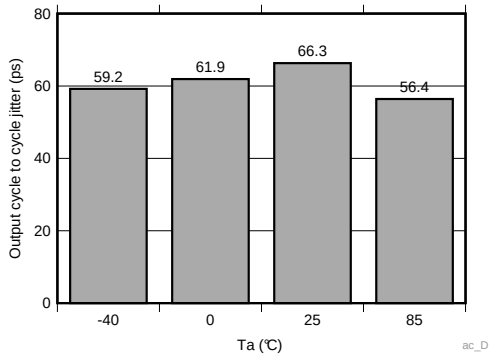
Get more information about WEBENCH tools at www.ti.com/WEBENCH.

### 9.2.3 Application Curves




X1 mode, 8-MHz input, 8-MHz output, VDD = 3.3 V

**Figure 7. Typical Cycle-to-Cycle Jitter vs Temperature**




X4 mode, 27.5-MHz input, 110-MHz output, VDD = 3.3 V

**Figure 8. Typical Cycle-to-Cycle Jitter vs Temperature**

## 10 Power Supply Recommendations

The CDCS504-Q1 requires a 3.3-V supply.

## 11 Layout

### 11.1 Layout Guidelines

The CDCS504-Q1 only has typical 20-mA supply current, so there is no thermal design challenge. A 0.01-µF capacitor may be placed close to VDD pin as a bypass capacitor.

### 11.2 Layout Example

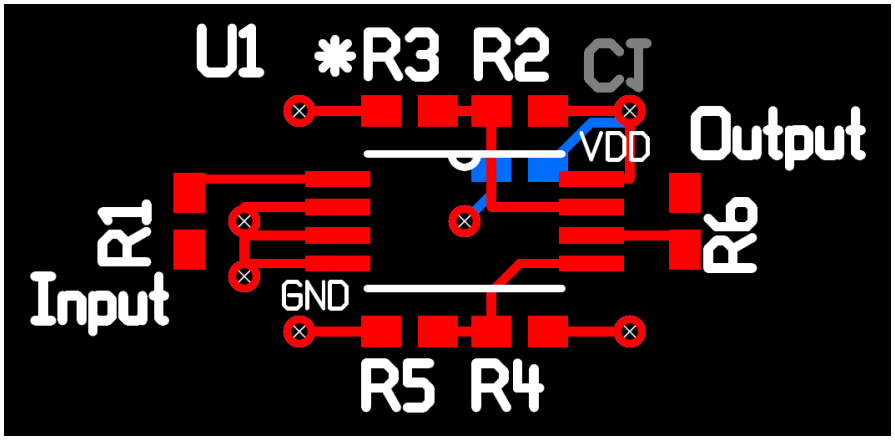



**Figure 9. Layout Example**

# 12 Device And Documentation Support

## 12.1 Device Support

### 12.1.1 Development Support

#### *12.1.1.1 Custom Design With WEBENCH® Tools*

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CDCS504TPWRQ1 | Active | Production | TSSOP (PW) \| 8 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CS504Q |
| CDCS504TPWRQ1.B | Active | Production | TSSOP (PW) \| 8 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CS504Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

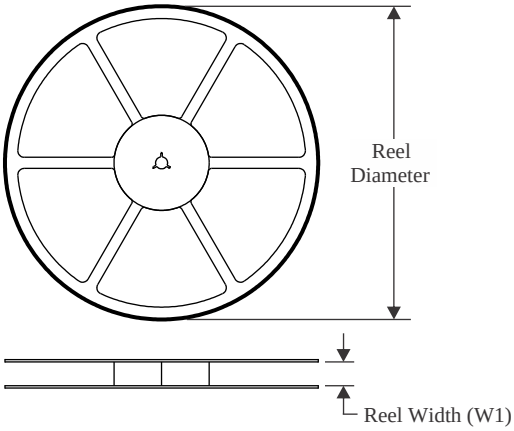
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

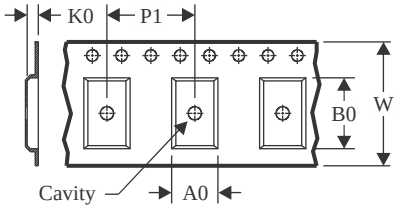
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

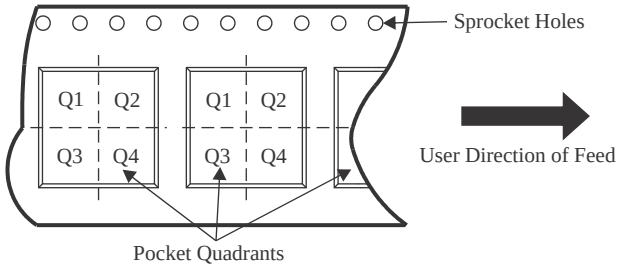



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

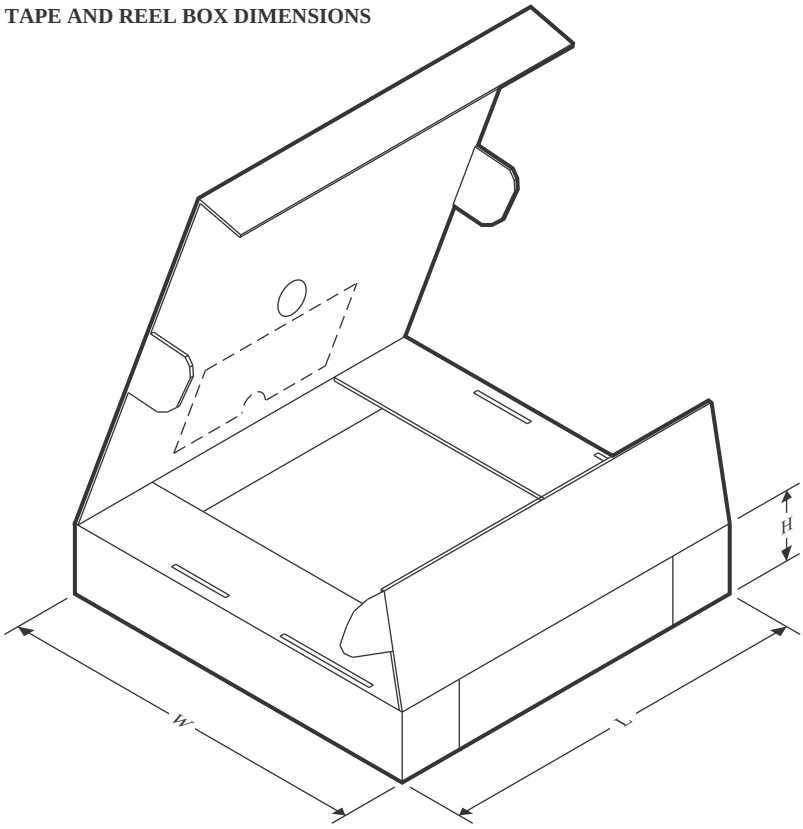
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCS504TPWRQ1 | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

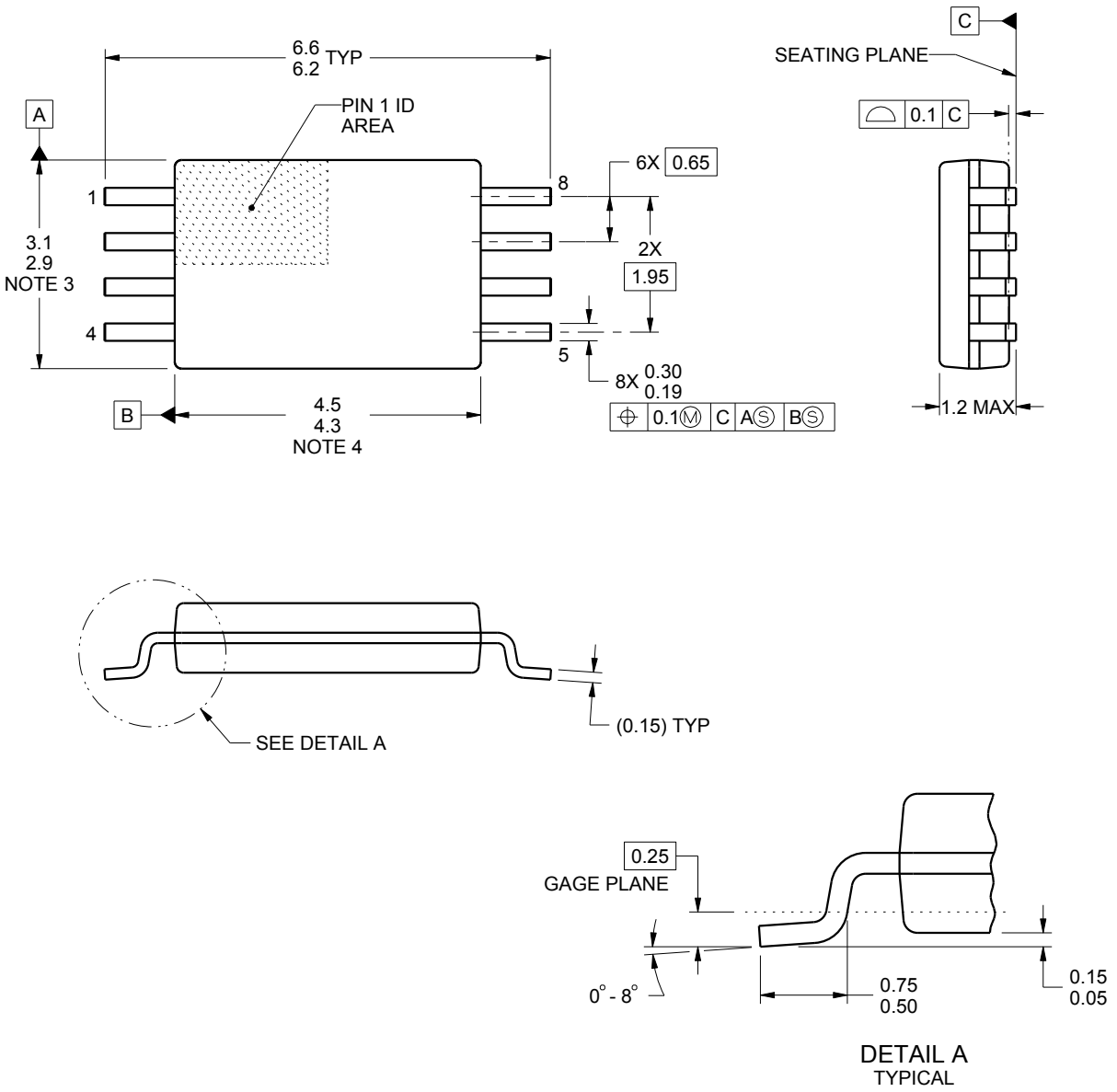
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCS504TPWRQ1 | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0008A

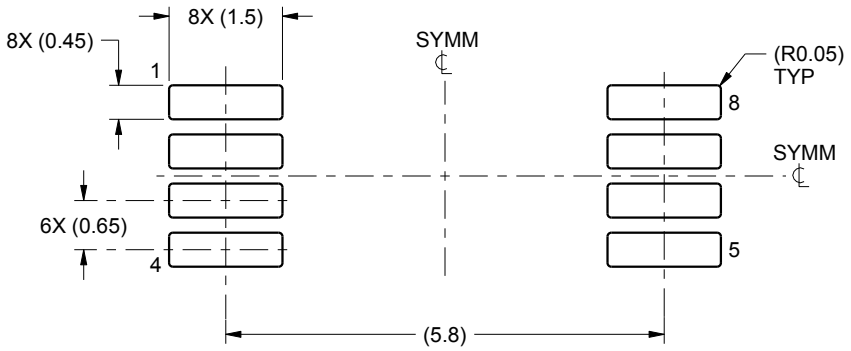
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

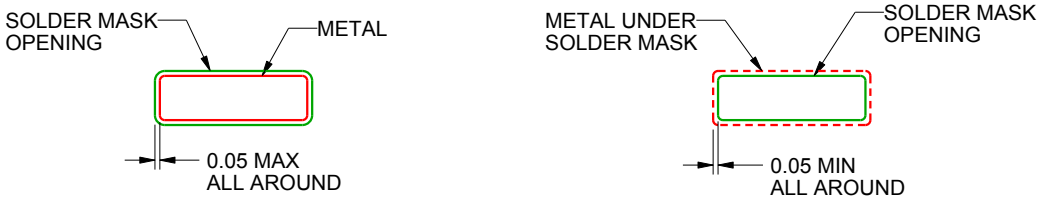



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
NOT TO SCALE

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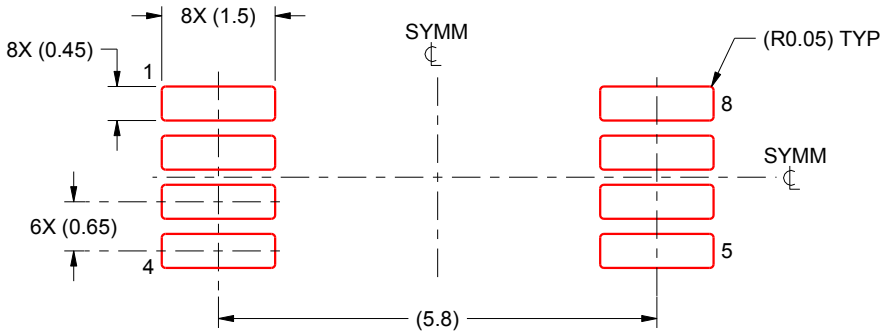
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025