CDCVF25084
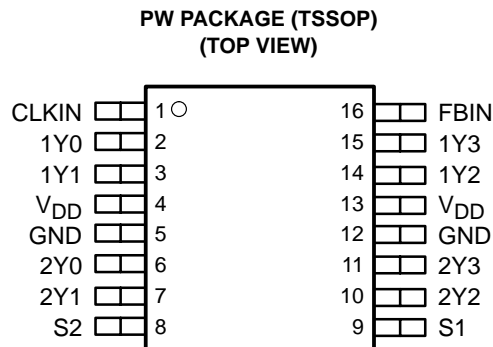# 3.3-V 1:8 ZERO DELAY (PLL) x4 CLOCK MULTIPLIER

SCAS690A – APRIL 2003 – REVISED MAY 2003

- **Phase-Locked Loop-Based Multiplier by Four**
- **Input Frequency Range: 2.5 MHz to 45 MHz**
- **Output Frequency Range: 10 MHz to 180 MHz**
- **LVCMOS/LVTTL I/O Compatible**
- **Low Jitter (Cycle-Cycle): ±120 ps Over the Range 75 MHz to 180 MHz**
- **Distributes One Clock Input to Two Banks of Four Outputs**
- **Auto Frequency Detection to Disable Device (Power-Down Mode)**
- **Operates From Single 3.3-V Supply**
- **Industrial Temperature Range –40°C to 85°C**
- **25-Ω On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Spread Spectrum Clock Compatible (SSC)**
- **Available in 16-Pin TSSOP Package**

PW PACKAGE (TSSOP)
(TOP VIEW)

CLKIN	1		16	FBIN
1Y0	2		15	1Y3
1Y1	3		14	1Y2
V_{DD}	4		13	V_{DD}
GND	5		12	GND
2Y0	6		11	2Y3
2Y1	7		10	2Y2
S2	8		9	S1

description

The CDCVF25084 is a high-performance, low-skew, low-jitter, phase-lock loop clock multiplier. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal including a multiplication factor of four. The CDCVF25084 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKIN x four. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. The device automatically goes into power-down mode when no input signal is applied to CLKIN and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25084 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25084 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKIN and any following changes to the PLL reference.

The CDCVF25084 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	1Y0–1Y3	2Y0–2Y3	OUTPUT SOURCE	PLL SHUTDOWN
0	0	Hi-Z	Hi-Z	N/A	Yes
0	1	Active	Hi-Z	PLL†	No
1	0	Active	Active	Input clock (PLL bypass)	Yes
1	1	Active	Active	PLL†	No

† A CLK input frequency < 2 MHz switches the outputs to low level.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Terminal Functions

| TERMINAL		TYPE	DESCRIPTION
NAME	PIN NO.		
1Y[0:3]	2, 3, 14, 15	O	Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
2Y[0:3]	6, 7, 10, 11	O	Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25084 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.
FBIN	16	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.
GND	5, 12	Ground	Ground
S1, S2	9, 8	I	Select pins to determine mode of operation. See the *FUNCTION TABLE* for mode selection options.
V$_{DD}$	4, 13	Power	Supply voltage. The supply voltage range is 3 V to 3.6 V

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functional block diagram
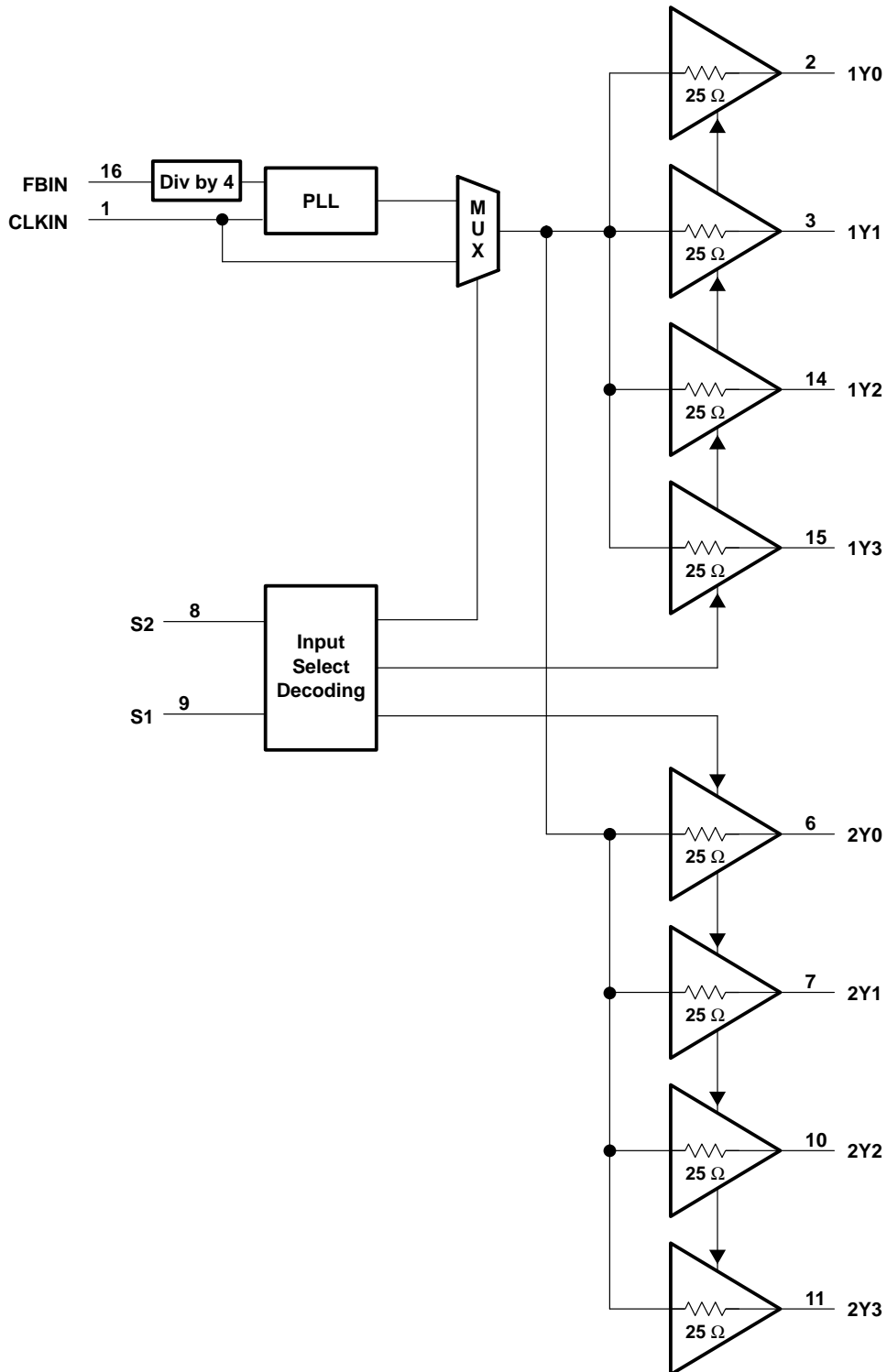
CDCVF25084
3.3-V 1:8 ZERO DELAY (PLL) x4 CLOCK MULTIPLIER

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Notes 1 and 2) .... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD}) .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package .... 147°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Low level input voltage, V_{IL}			0.8	V
High level input voltage, V_{IH}	2			V
Input voltage, V_I	0		3.6	V
High-level output current, I_{OH}			–12	mA
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	–40		85	°C

timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

		MIN	NOM	MAX	UNIT
Input clock frequency, f_{CLKIN}		2.5		45	MHz
Input clock duty cycle		40%		60%	
Clock frequency, f_{clkout}	C_L = 15 pF	10		180	MHz

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = −18 mA			−1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	μA
I_{PD}	Power-down current	f_{CLKIN} = 0 MHz,	V_{DD} = 3.3 V			100	μA
I_{DD}‡	Dynamic current	f_{out} = 80 MHz,	C_L = 15 pF		60	80	mA
I_{OZ}	Output 3-state	V_O = 0 V or V_{DD},	V_{DD} = 3.6 V			±5	μA
C_I	Input capacitance at FBIN, CLKIN	V_I = 0 V or V_{DD}			4		pF
C_I	Input capacitance at S1, S2	V_I = 0 V or V_{DD}			2.2		pF
C_O	Output capacitance	V_I = 0 V or V_{DD}			3		pF
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = −100 μA	V_{DD} − 0.2			V
		V_{DD} = 3 V,	I_{OH} = −12 mA	2.1			
		V_{DD} = 3 V,	I_{OH} = −6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 μA			0.2	V
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.8	
		V_{DD} = 3 V,	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	−24			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		−30		
		V_{DD} = 3.6 V,	V_O = 3.135 V			-15	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	26			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		33		
		V_{DD} = 3.6 V,	V_O = 0.4 V			14	

† All typical values are at respective nominal V_{DD}.
‡ All outputs are switching; for I_{DD} over frequency see Figure 9.

![TEXAS INSTRUMENTS logo]

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(lock)}$	PLL lock time	f_{out} = 100 MHz		2		μs
$t_{(phoffset)}$	Phase offset (CLKIN to FBIN), (see Note 5)	f_{out} = 40 MHz to 75 MHz, Vth = $V_{DD}/2$			±200	ps
		f_{out} = 75 MHz to 180 MHz, Vth = $V_{DD}/2$			±100	
t_{PLH}, t_{PHL}	Propagation delay	S2 = High, S1 = Low (PLL bypass mode)	2.3		4.5	ns
$t_{sk(o)}$	Output skew (Yn to Yn) (see Note 4)	See Figure 3		75	150	ps
$t_{sk(pp)}$	Part-to-part skew (low-to-high transition)	PLL bypass mode			900	ps
		PLL mode, f_{out} = 40 MHz to 75 MHz			350	
		PLL mode, f_{out} = 75 MHz to 180 MHz			300	
$t_{jit(cc)}$	Jitter (cycle-to-cycle)	f_{out} = 40 MHz to 75 MHz			±220	ps
		f_{out} = 75 MHz to 180 MHz			±120	ps
$t_{jit(per)}$	Period jitter	f_{out} = 40 MHz to 75 MHz			260	ps
		f_{out} = 75 MHz to 180 MHz			140	ps
$t_{jit(\theta)}$	Phase jitter	f_{out} = 75 MHz to 180 MHz, peak-to-peak (see Note 6)			±110	ps
		f_{out} = 75 MHz to 180 MHz, RMS (see Note 6)			26	ps
odc	Output duty cycle	f_{out} = 10 MHz to 180 MHz	45%		55%	
$t_{sk(p)}$	Pulse skew	S2 = High, S1 = low (PLL bypass mode)			0.3	ns
t_r, t_f	Rise / fall time rate	See Figure 4	1		3	V/ns

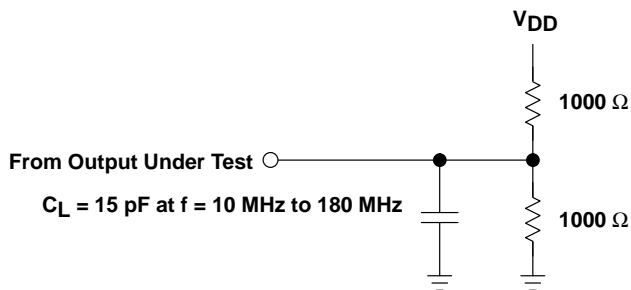† All typical values are at respective nominal V_{DD}.

NOTES: 4. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
      5. Similar waveform at CLKIN and FBIN are required. Output 1Y3 is used as a feedback to FBIN loaded with 11 pF and all other outputs have 15 pF. For phase displacement between CLKIN and Y-outputs, see Figure 5.
      6. Input phase jitter < ±50 ps; output sample size is 20000 cycles.

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PARAMETER MEASUREMENT INFORMATION

V$_{DD}$

1000 Ω

From Output Under Test

C$_L$ = 15 pF at f = 10 MHz to 180 MHz

1000 Ω

NOTES: A. C$_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: Z$_O$ = 50 Ω, t$_r$ < 1.2 ns, t$_f$ < 1.2 ns
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Test Load Circuit

V$_{OH}$

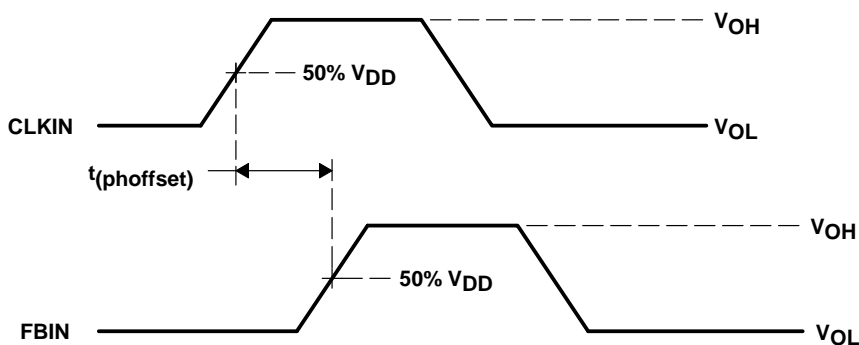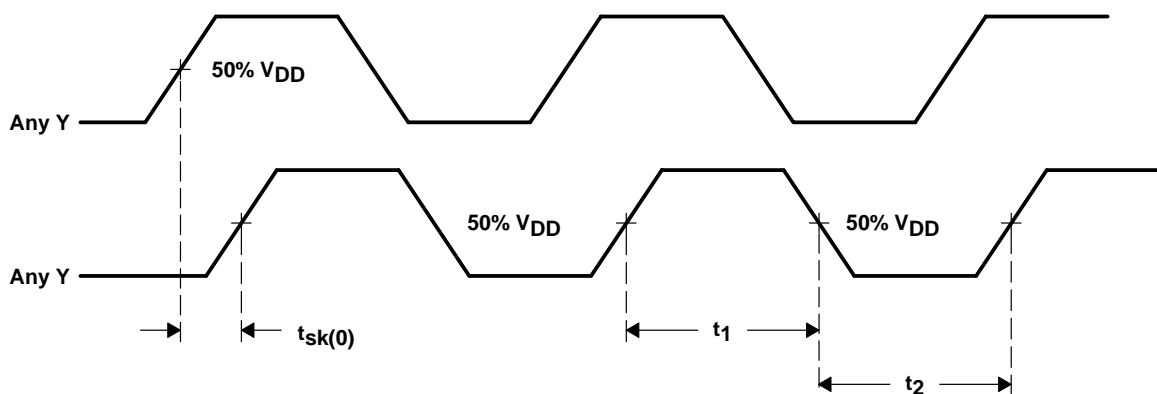50% V$_{DD}$

CLKIN

V$_{OL}$

t$_{(phoffset)}$

V$_{OH}$

50% V$_{DD}$

FBIN

V$_{OL}$

Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)

50% V$_{DD}$

Any Y

50% V$_{DD}$

50% V$_{DD}$

Any Y

t$_{sk(0)}$

t$_1$

t$_2$

NOTE: odc = t$_1$/(t$_1$ + t$_2$) x 100%

Figure 3. Output Skew and Output Duty Cycle (PLL Mode)

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PARAMETER MEASUREMENT INFORMATION
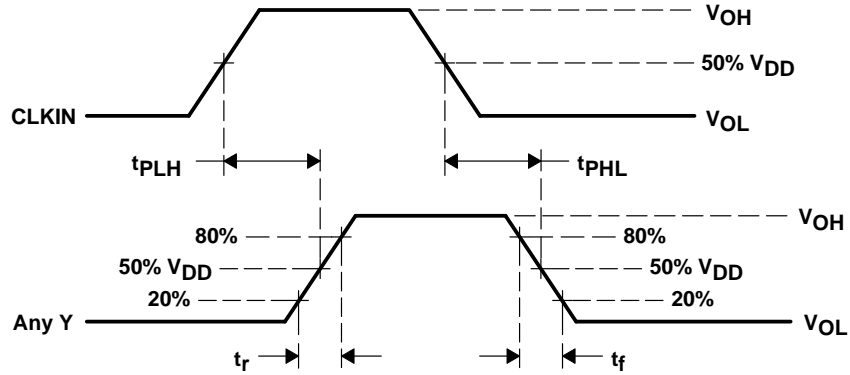
NOTE: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

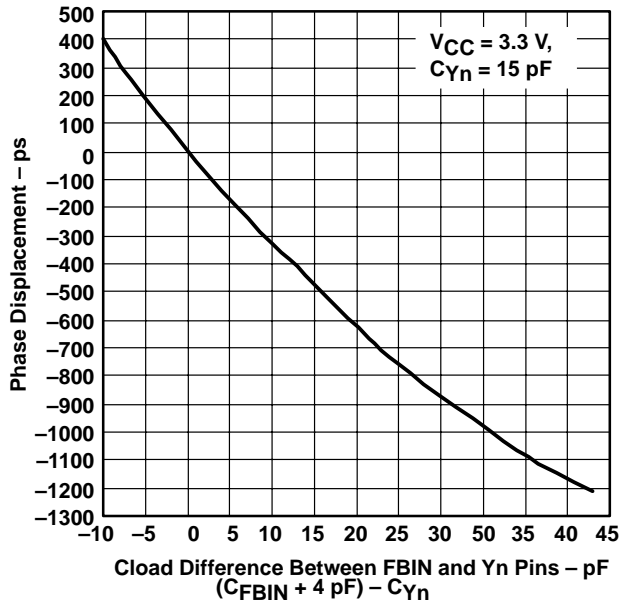**Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)**

PHASE DISPLACEMENT
vs
CLOAD

V_{CC} = 3.3 V,
C_{Yn} = 15 pF

Figure 5

PHASE OFFSET
vs
FREQUENCY

$C_{L(Yn)}$ = 15 pF,
$C_{L(FBIN)}$ = 11 pF

Figure 6

TEXAS
INSTRUMENTS
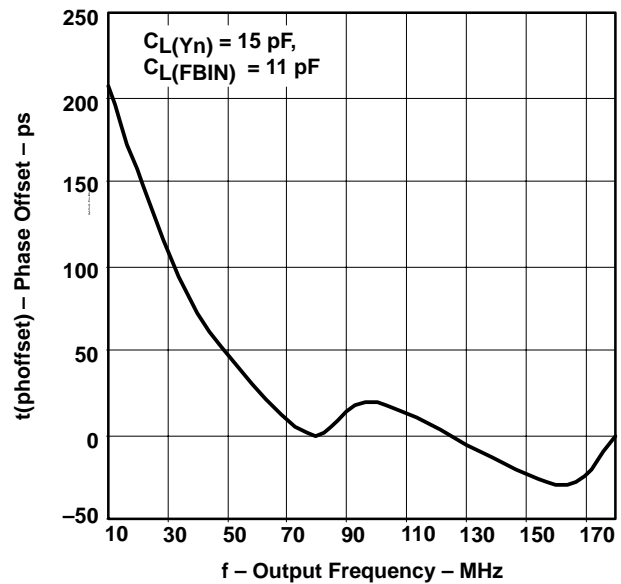POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

**CYCLE-TO-CYCLE / PERIOD JITTER
vs
FREQUENCY**
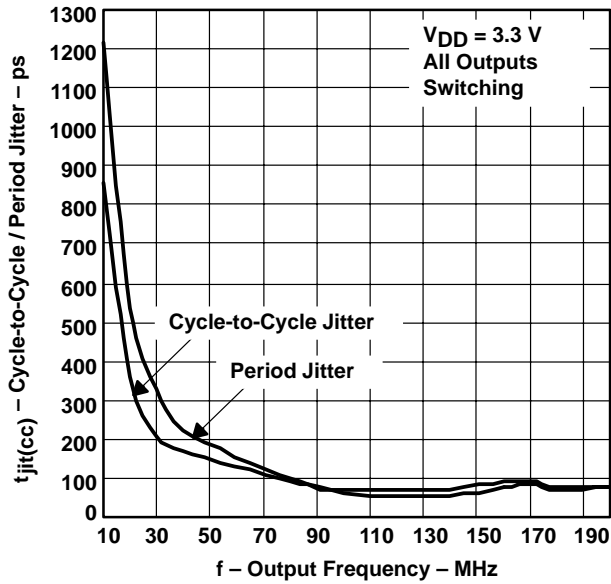
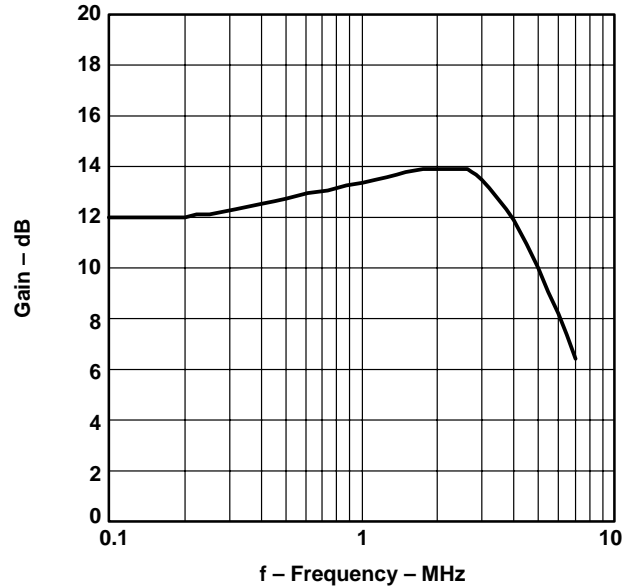**Figure 7**

TRANSFER CHARACTERISTIC FROM CLKIN TO Yn
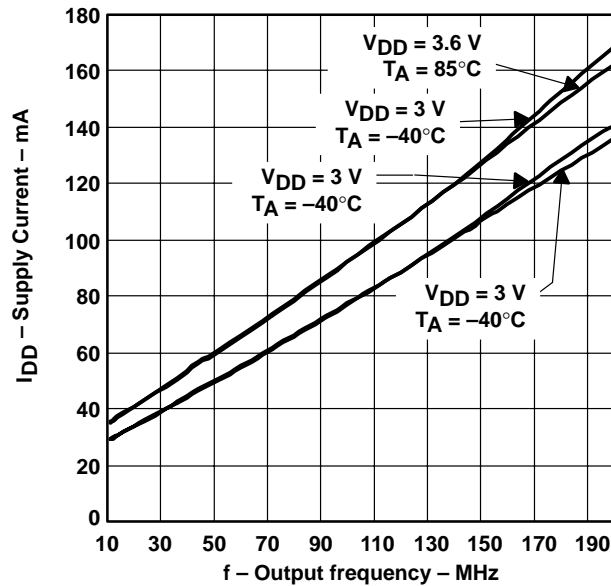

Figure 8

**SUPPLY CURRENT
vs
FREQUENCY**

Figure 9

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCVF25084PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK084
CDCVF25084PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK084
CDCVF25084PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK084

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF25084PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF25084PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDCVF25084PW	PW	TSSOP	16	90	530	10.2	3600	3.5

PIN 1 INDEX AREA

6.6
6.2 TYP

14X 0.65

2X
4.55

5.1
4.9
NOTE 3

4.5
4.3
NOTE 4

16X 0.30
0.17

⊕ 0.1Ⓜ C A B

SEATING PLANE

C

⌒ 0.1 C

4X (0°-12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0°-8°

DETAIL A
TYPICAL
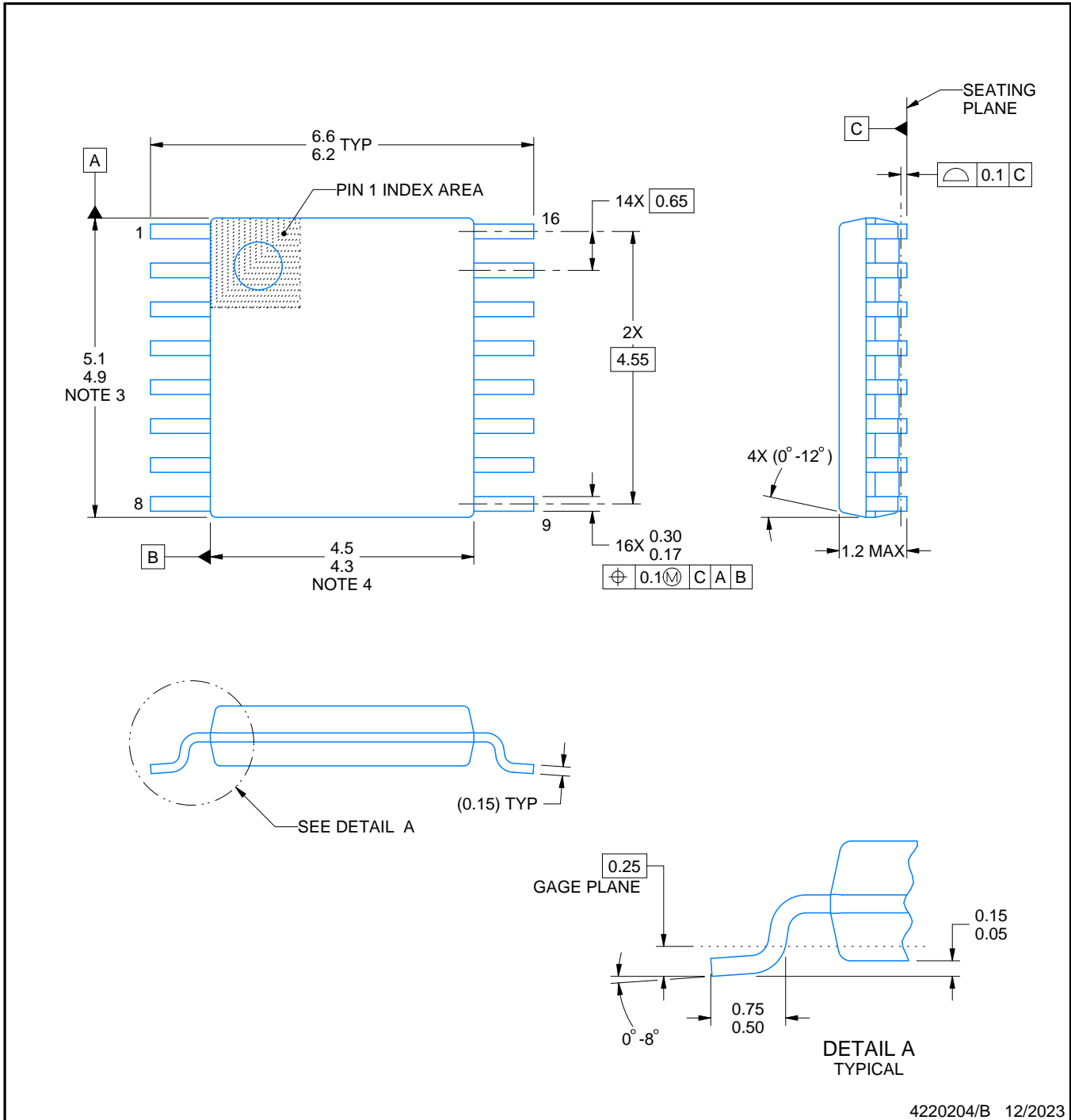
4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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