

CSD17483F4 30-V N-Channel FemtoFET™ MOSFET

1 Features

- Low on-resistance
- Low Q_g and Q_{gd}
- Low-threshold voltage
- Ultra-small footprint (0402 case Size)
 - 1.0 mm × 0.6 mm
- Ultra-low profile
 - 0.36-mm height
- Integrated ESD protection diode
 - Rated > 4-kV HBM
 - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 200-mΩ, 30-V N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

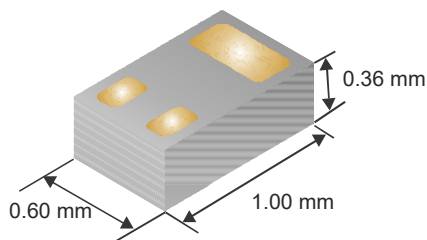


Figure 3-1. Typical Part Dimensions

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
Q_g	Gate Charge Total (4.5 V)	1010	pC
Q_{gd}	Gate Charge Gate-to-Drain	130	pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 1.8\text{ V}$	370
		$V_{GS} = 2.5\text{ V}$	240
		$V_{GS} = 4.5\text{ V}$	200
$V_{GS(th)}$	Threshold Voltage	0.85	V

Device Information

DEVICE ⁽¹⁾	QTY	MEDIA	PACKAGE	SHIP
CSD17483F4	3000	7-Inch Reel	Femto(0402)	Tape and Reel
CSD17483F4T	250		1.00 mm × 0.60 mm SMD Lead Less	

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	12	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}$ ⁽¹⁾	1.5	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	5	A
I_G	Continuous Gate Clamp Current	35	mA
	Pulsed Gate Clamp Current ⁽²⁾	350	
P_D	Power Dissipation ⁽¹⁾	500	mW
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
T_J , T_{stg}	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 7.4\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	2.7	mJ

- (1) Typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

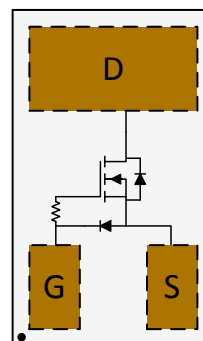


Figure 3-2. Top View



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4 Revision History

Changes from Revision E (April 2018) to Revision F (February 2022) Page

• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

Changes from Revision D (December 2016) to Revision E (April 2018) Page

• Raised I_{DSS} Test Condition Voltage.....	3
• Raised I_{GSS} Test Condition Voltage.....	3

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = 250 μA	30			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 24 V	100			nA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 10 V	50			nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.65	0.85	1.10	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 1.8 V, I _{DS} =0.5 A	370			mΩ
		V _{GS} = 2.5 V, I _{DS} =0.5 A	240			
		V _{GS} = 4.5 V, I _{DS} = 0.5 A	200			
		V _{GS} = 8 V, I _{DS} = 0.5 A	185			
g _{fs}	Transconductance	V _{DS} = 15 V, I _{DS} = 0.5 A	2.4			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz	145			pF
C _{oss}	Output capacitance		42			pF
C _{rss}	Reverse transfer capacitance		2			pF
R _G	Series gate resistance		23			Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 15 V, I _{DS} = 0.5 A	1010			pC
Q _{gd}	Gate charge gate-to-drain		130			pC
Q _{gs}	Gate charge gate-to-source		220			pC
Q _{g(th)}	Gate charge at V _{th}		145			pC
Q _{oss}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V	1095			pC
t _{d(on)}	Turnon delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 0.5 A,R _G = 2 Ω	3.3			ns
t _r	Rise time		1.3			ns
t _{d(off)}	Turnoff delay time		10.6			ns
t _f	Fall time		3.4			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 0.5 A, V _{GS} = 0 V	0.73			V
Q _{rr}	Reverse recovery charge	V _{DS} = 15 V, I _F = 0.5 A, di/dt = 300 A/μs	1475			pC
t _{rr}	Reverse recovery time		5.5			ns

5.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	90	$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance ⁽²⁾	250	

(1) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

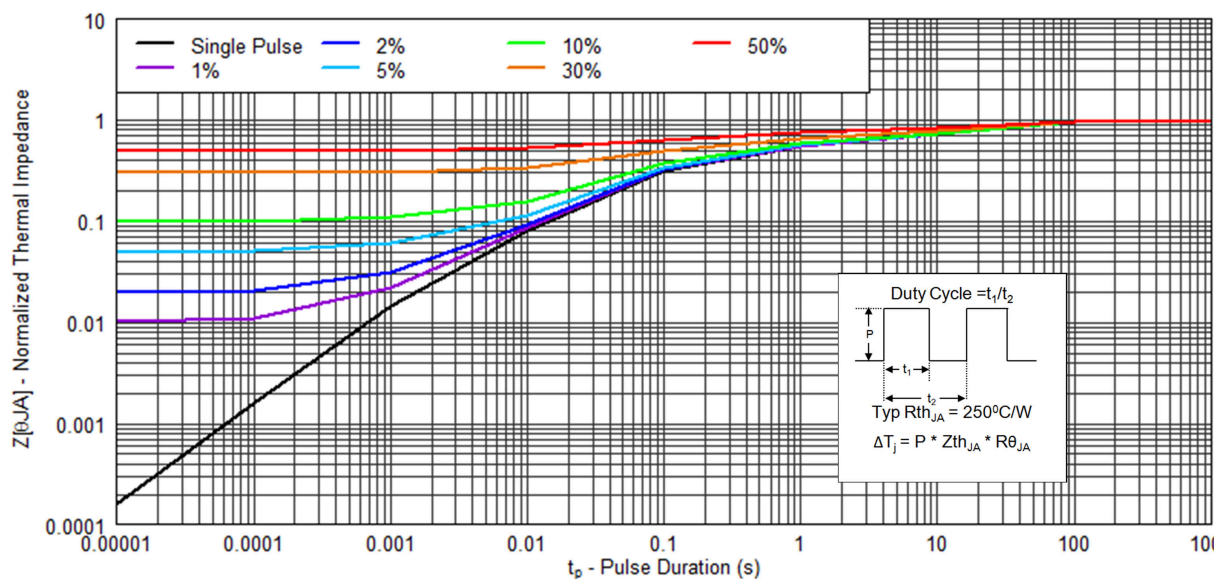


Figure 5-1. Transient Thermal Impedance

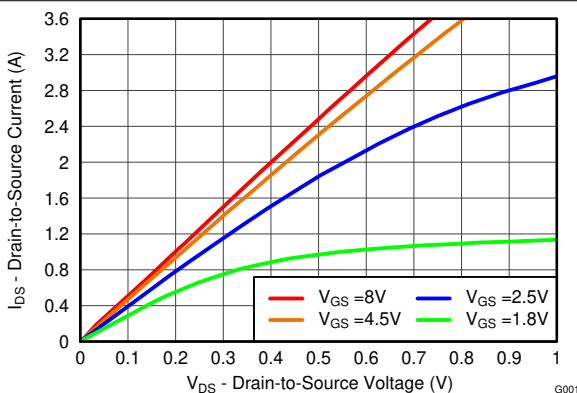


Figure 5-2. Saturation Characteristics

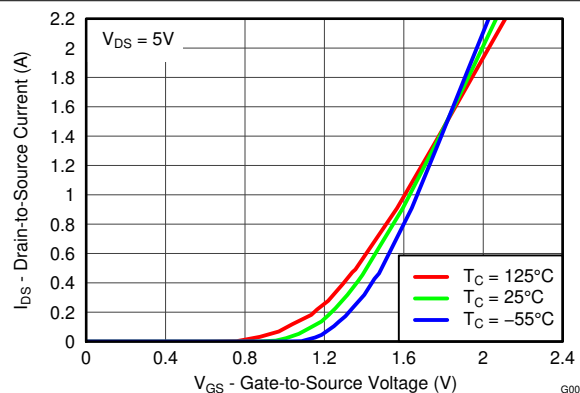


Figure 5-3. Transfer Characteristics

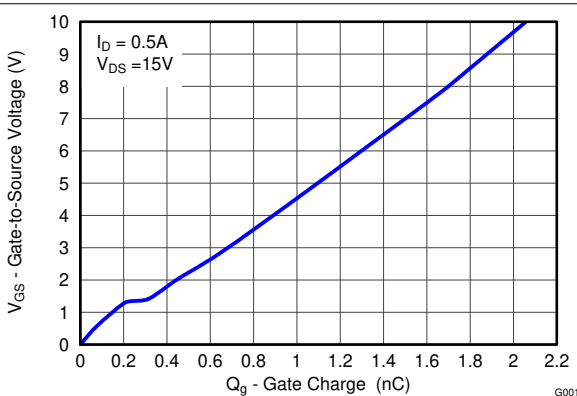


Figure 5-4. Gate Charge

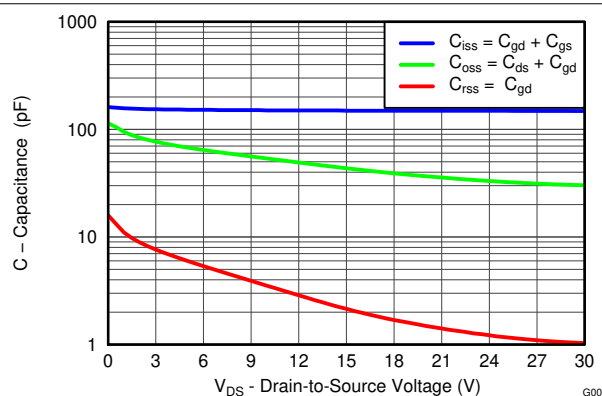


Figure 5-5. Capacitance

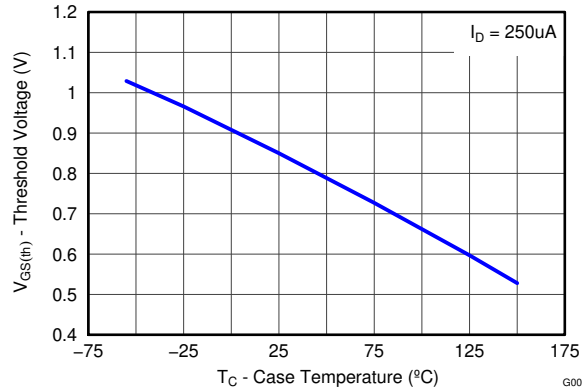


Figure 5-6. Threshold Voltage vs Temperature

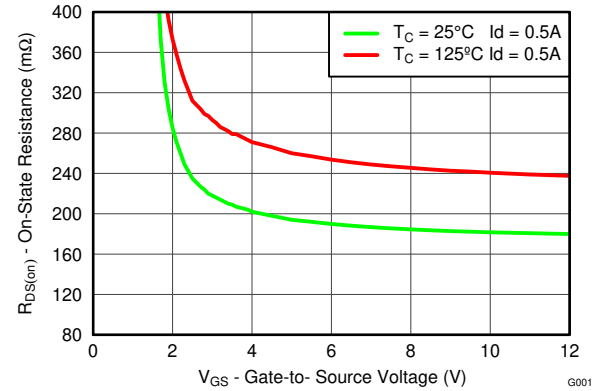


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

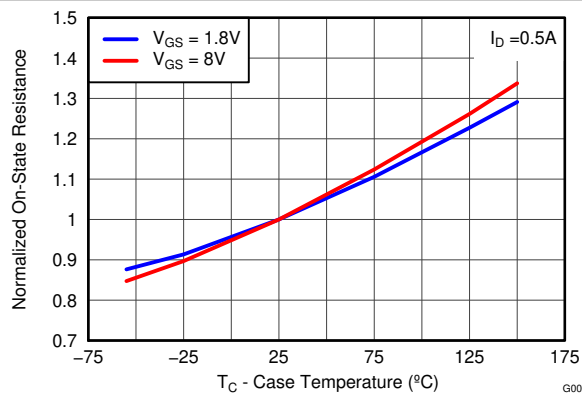


Figure 5-8. Normalized On-State Resistance vs Temperature

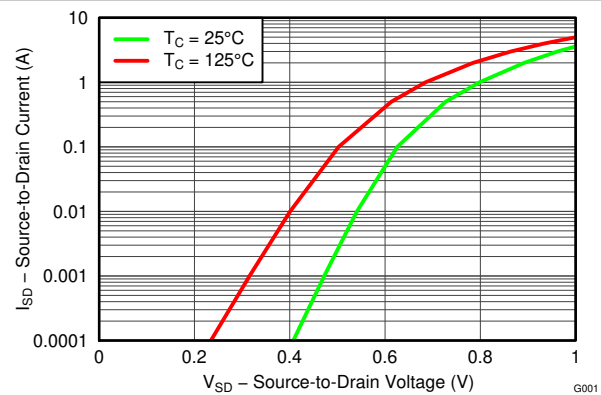


Figure 5-9. Typical Diode Forward Voltage

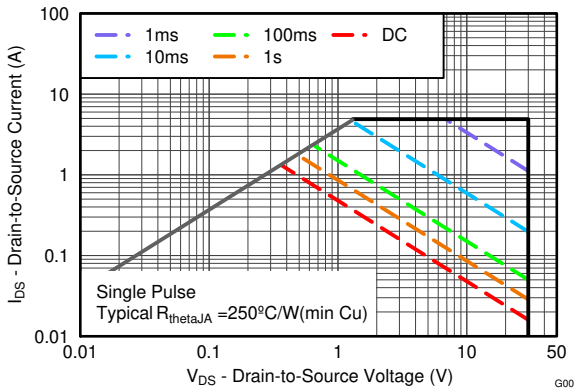


Figure 5-10. Maximum Safe Operating Area

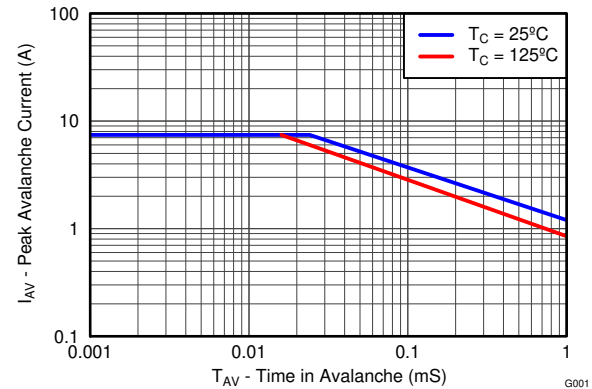
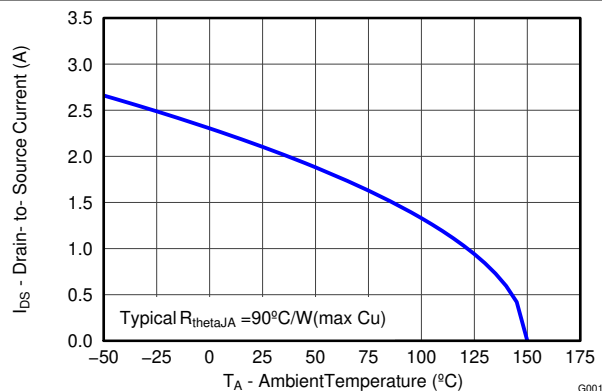


Figure 5-11. Single Pulse Unclamped Inductive Switching

**Figure 5-12. Maximum Drain Current vs Temperature**

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.4 Glossary

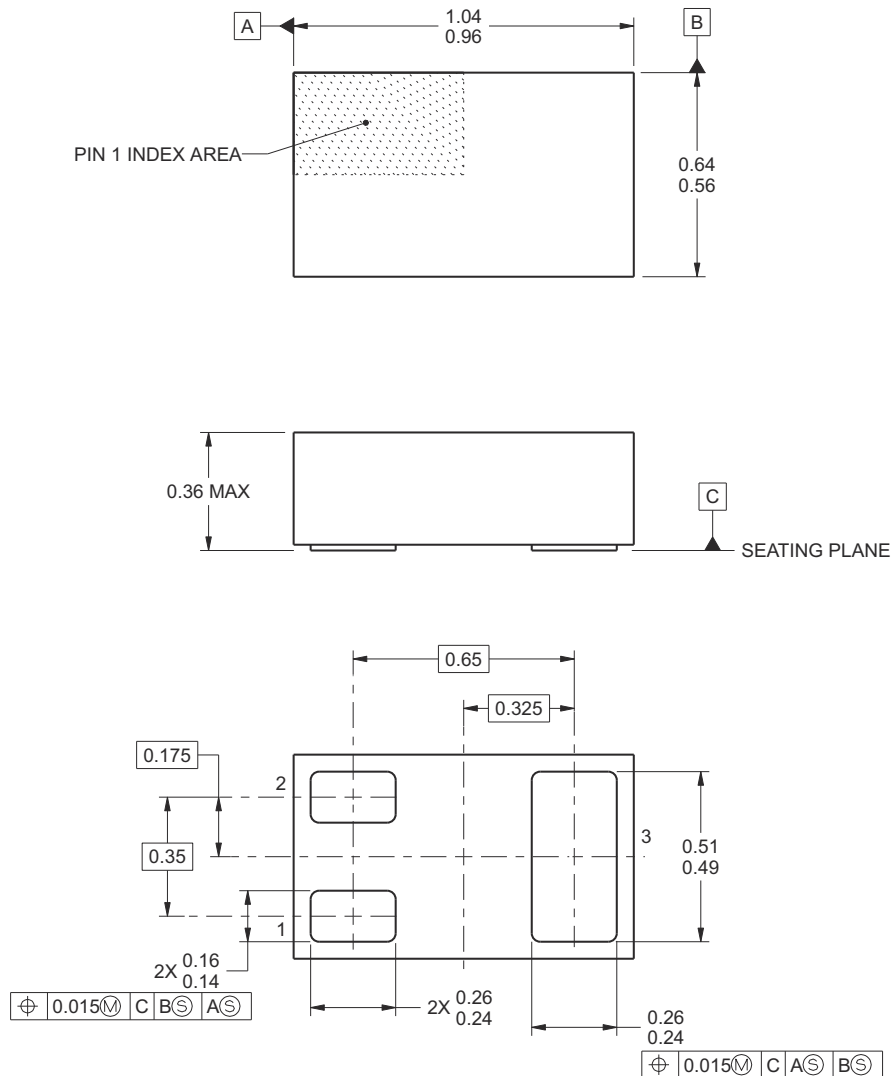
[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

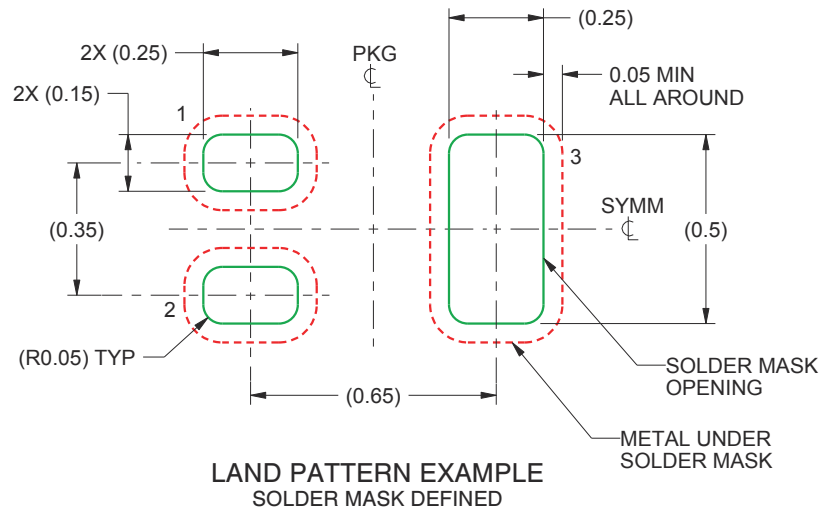
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



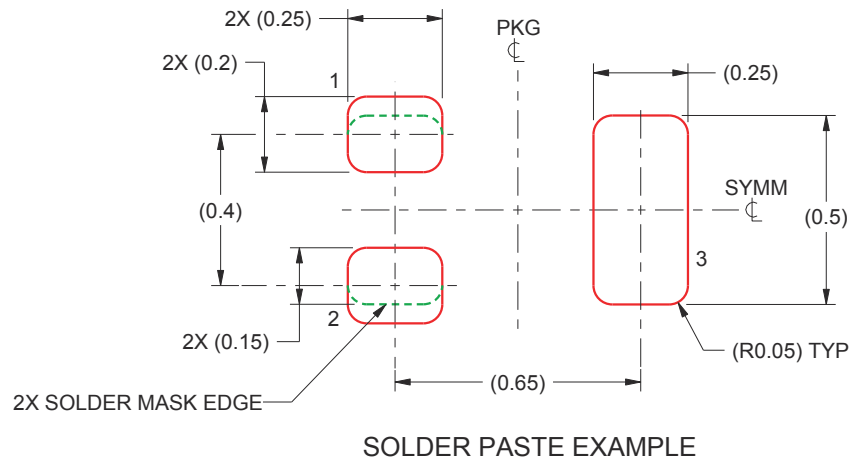
- A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- B. This drawing is subject to change without notice.
- C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.
- B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17483F4	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DP
CSD17483F4.B	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DP
CSD17483F4T	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DP
CSD17483F4T.B	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17483F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD17483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

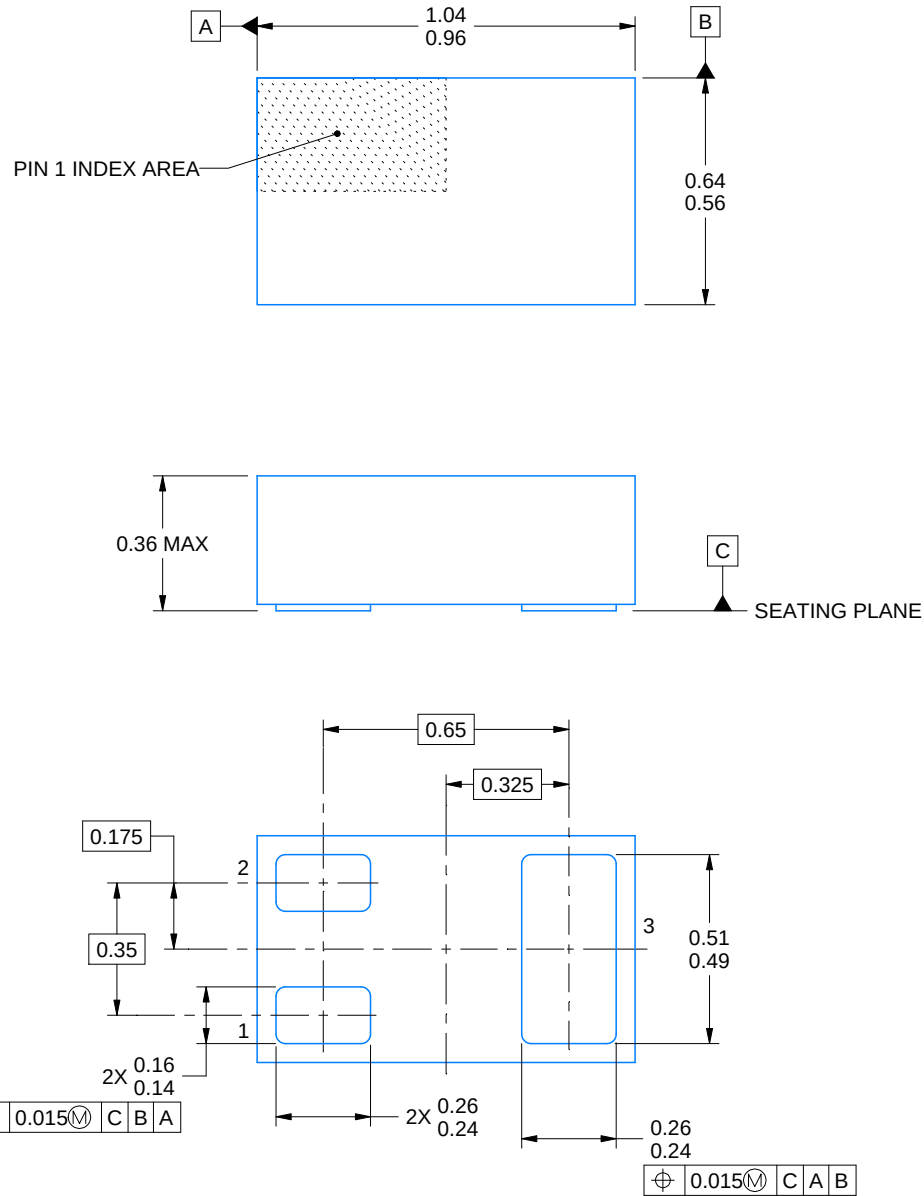


PACKAGE OUTLINE

YJC0003A

PicoStar™ - 0.36 mm max height

PicoStar™



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PicoStar is a trademark of Texas Instruments.

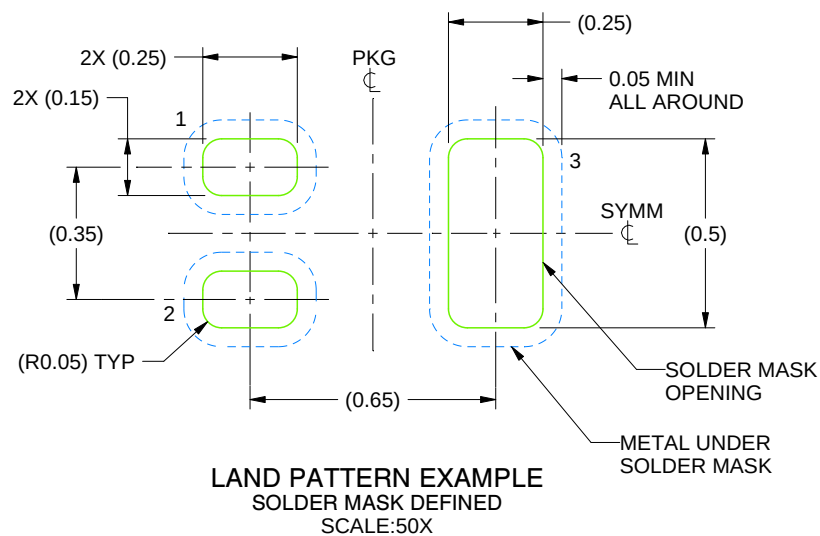
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

YJC0003A

PicoStar™ - 0.36 mm max height

PicoStar™



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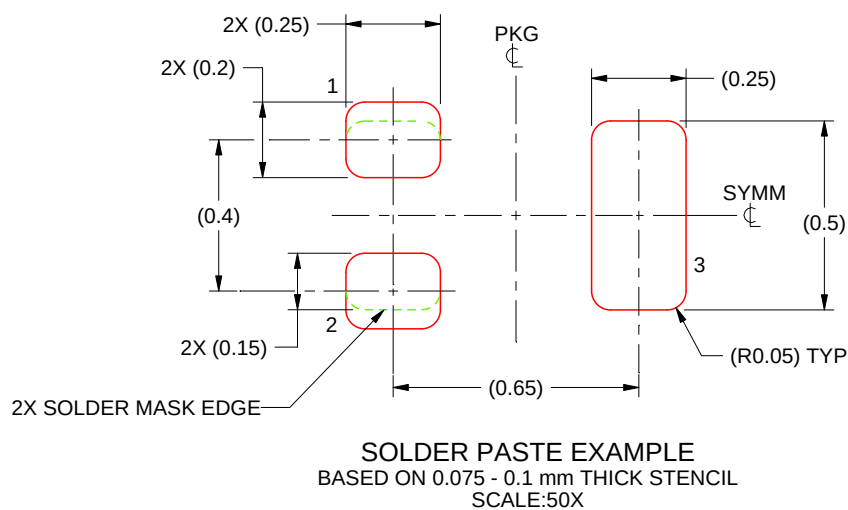
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

YJC0003A

PicoStar™ - 0.36 mm max height

PicoStar™



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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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