CSD25211W1015, P-Channel NexFET™ Power MOSFET

1 Features

- Ultra-low on resistance
- Ultra-low Q_g and Q_{gd}
- Small footprint 1.0 mm × 1.5 mm
- Low profile 0.62 mm height
- Pb Free
- Gate-source voltage clamp
- Gate ESD protection – 3 kV
- RoHS compliant
- Halogen free

2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

The device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile.

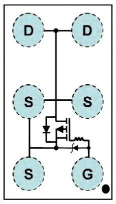


Figure 3-1. Top View

Product Summary

T_A = 25°C unless otherwise stated		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5V)	3.4		nC
Q_{gd}	Gate Charge Gate to Drain	0.2		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –2.5 V	36	mΩ
		V_{GS} = –4.5 V	27	mΩ
$V_{GS(th)}$	Voltage Threshold	–0.8		V

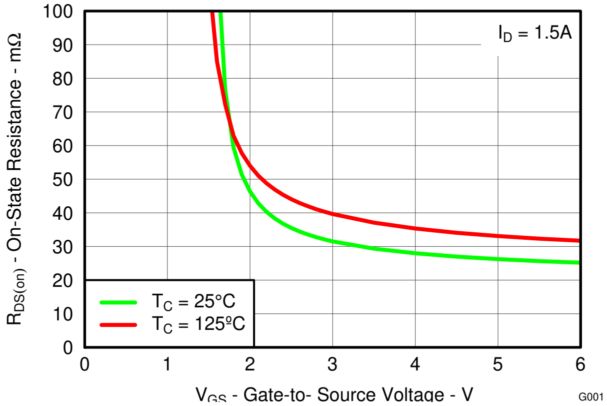
Ordering Information

Device	Package	Media	Qty	Ship
CSD25211W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

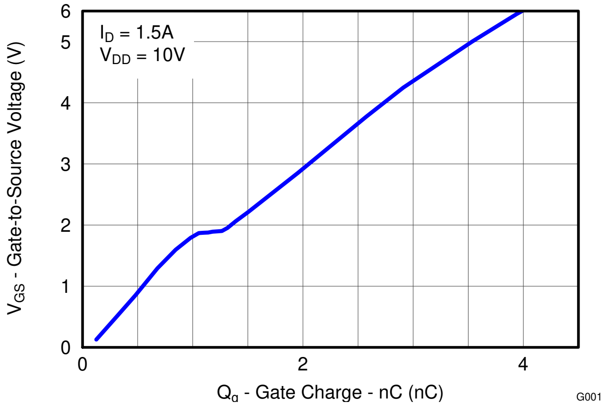
Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	-6	V
I_D	Continuous Drain Current, T_A = 25°C[1]	-3.2	A
I_{DM}	Pulsed Drain Current, T_A = 25°C[2]	-9.5	A
I_G	Continuous Gate Current, T_A = 25°C	-0.5	A
	Pulsed Gate Current	-7	A
P_D	Power Dissipation[1]	1	W
T_{STG}	Storage Temperature Range	–55 to 150	°C
T_J	Operating Junction Temperature Range		

(1) Typical $R_{\theta JA}$ = 119°C/W on 1 $inch^2$ of 2 oz. Cu on 0.06-inch thick FR4 PCB.
(2) Pulse width ≤ 10 µs, duty cycle ≤ 2%



$R_{DS(ON)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2014) to Revision B (September 2022) **Page**

- In the Absolute Maximum Ratings table Continuous Drain Current was changed to Continuous Gate Current. 1
- In the Absolute Maximum Ratings table Pulsed Drain Current was changed to Pulsed Gate Current....... 1

5 Electrical Characteristics

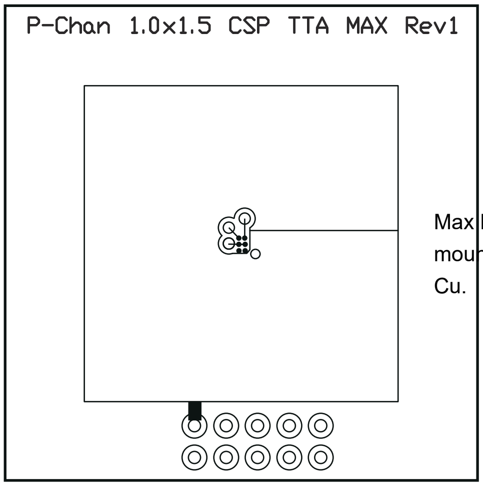
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 µA	–6.1		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –2.5 V, I_D = –1.5 A		36	44	mΩ
		V_{GS} = –4.5 V, I_D = –1.5 A		27	33	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_D = –1.5 A		12		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		475	570	pF
C_{OSS}	Output Capacitance			234	281	pF
C_{RSS}	Reverse Transfer Capacitance			10.5	13.1	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_D = –1.5 A		3.4	4.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.2		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		3.8		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –1.5 A R_G = 4 Ω		13.6		ns
t_r	Rise Time			8.8		ns
$t_{d(off)}$	Turn Off Delay Time			36.9		ns
t_f	Fall Time			14.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –1.5 A, V_{GS} = 0 V		–0.8	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd}= –10 V, I_F = –1.5 A, di/dt = 200 A/µs		6.9		nC
t_{rr}	Reverse Recovery Time			11.6		ns

6 Thermal Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			230	°C/W
	Thermal Resistance Junction to Ambient (1 in^2 Cu area)			149	°C/W



Max $R_{\theta JA}$ = 149°C/W when mounted on 1 $inch^2$ of 2 oz. Cu.

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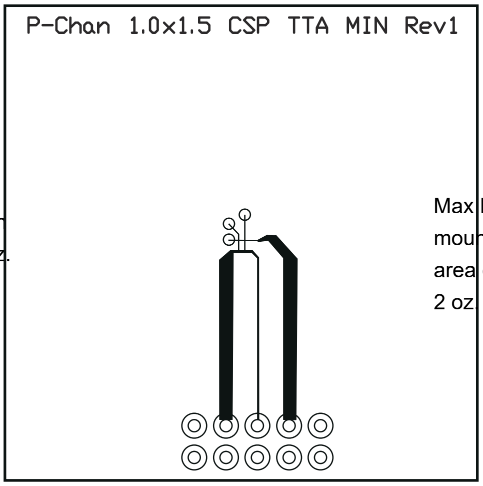

Max $R_{\theta JA}$ = 230°C/W when mounted on minimum pad area of 2 oz. Cu.

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7 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

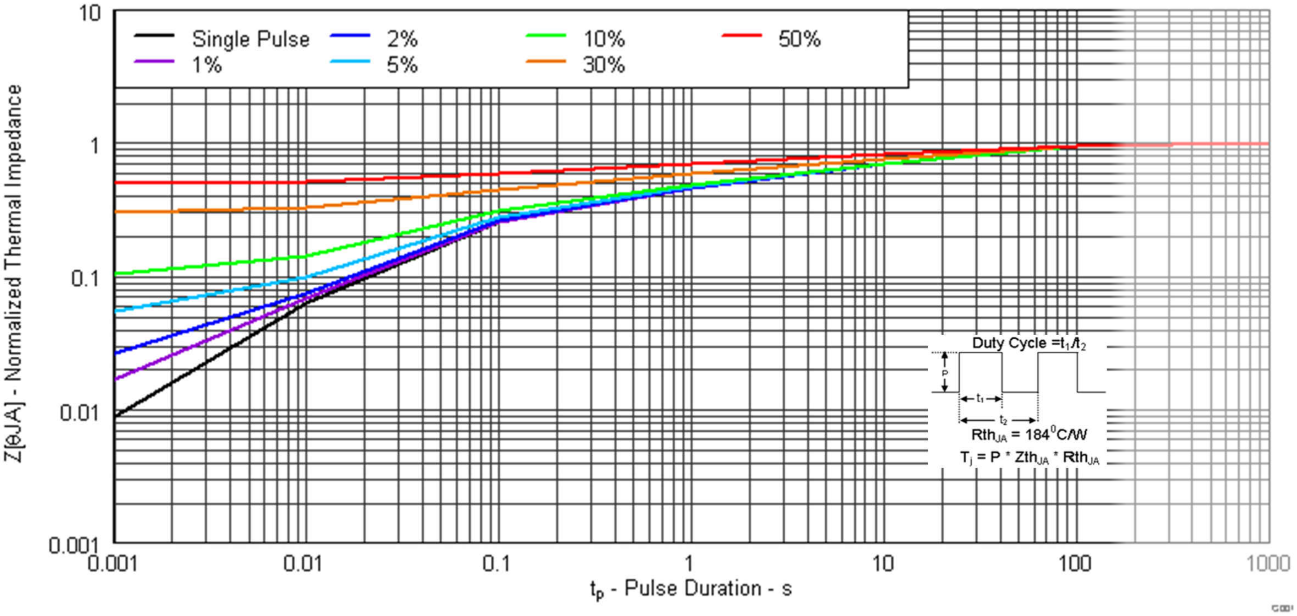


Figure 7-1. Transient Thermal Impedance

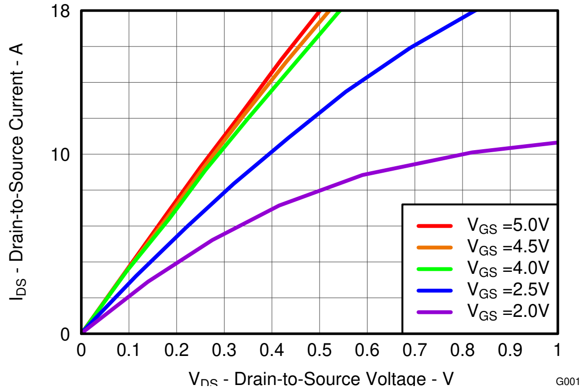


Figure 7-2. Saturation Characteristics

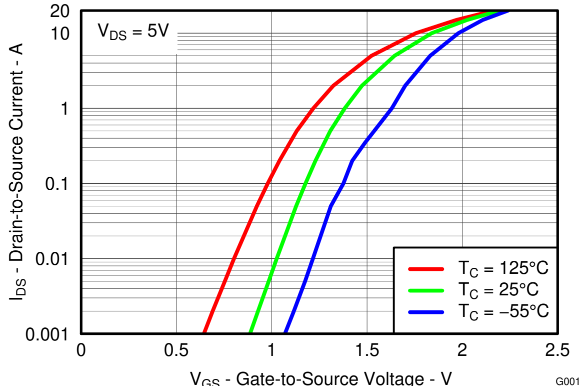


Figure 7-3. Transfer Characteristics

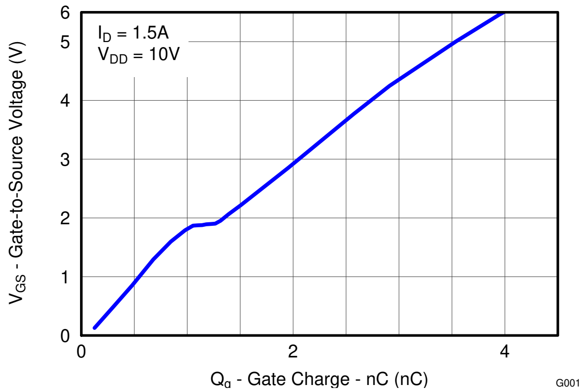


Figure 7-4. Gate Charge

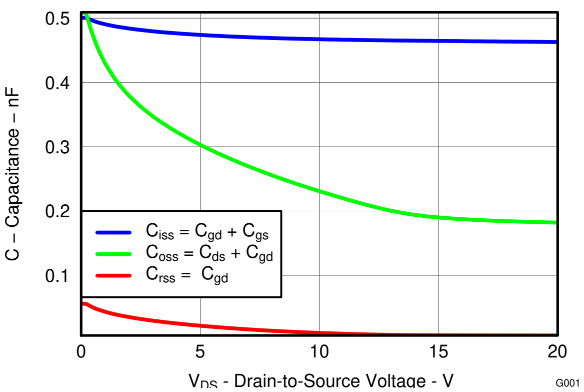


Figure 7-5. Capacitance

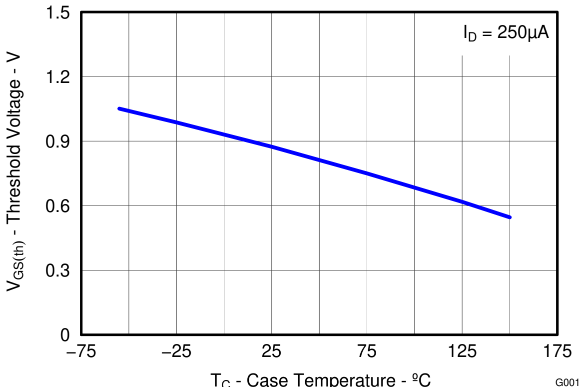


Figure 7-6. Threshold Voltage vs Temperature

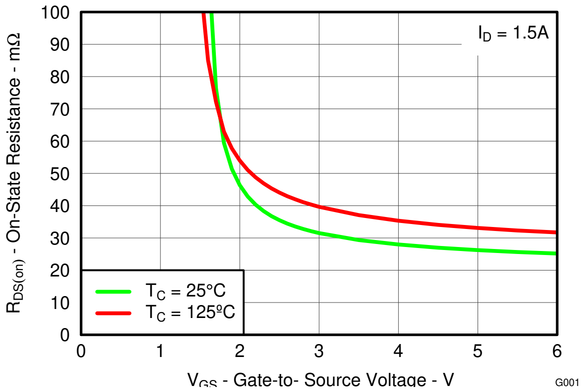


Figure 7-7. On Resistance vs Gate Voltage

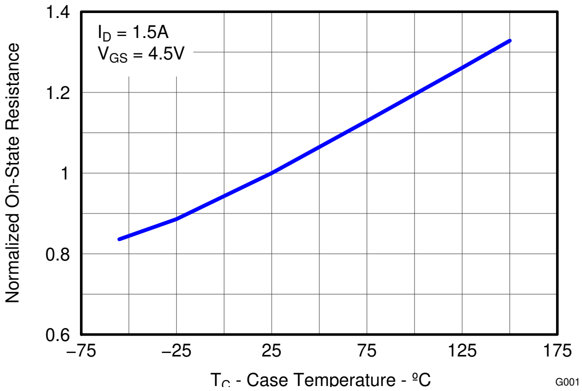


Figure 7-8. Normalized On Resistance vs Temperature

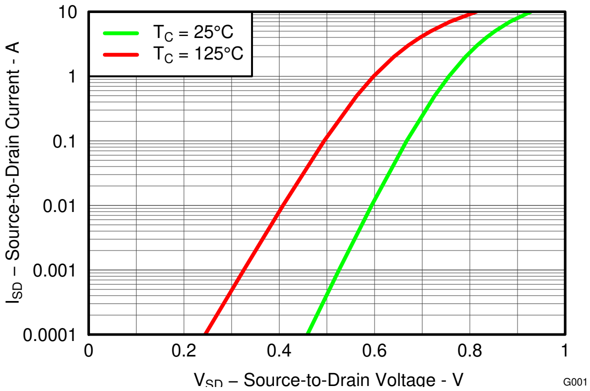


Figure 7-9. Typical Diode Forward Voltage

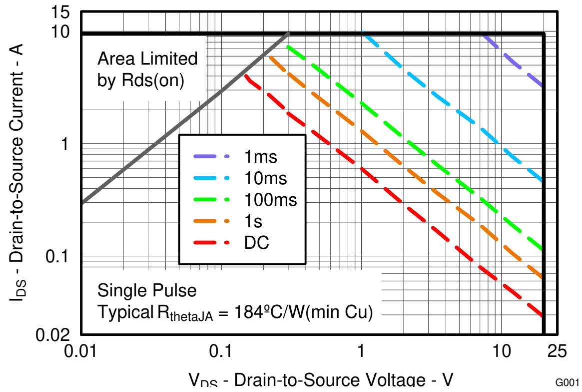


Figure 7-10. Maximum Safe Operating Area

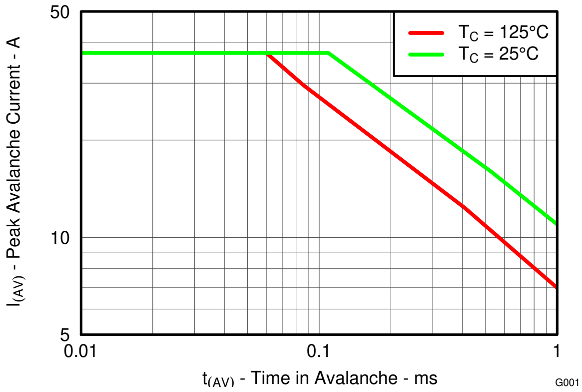


Figure 7-11. Single Pulse Unclamped Inductive Switching

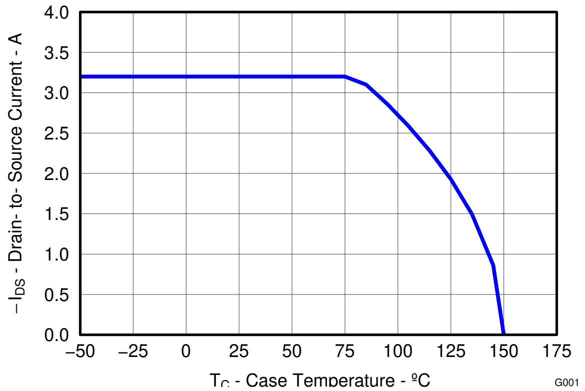
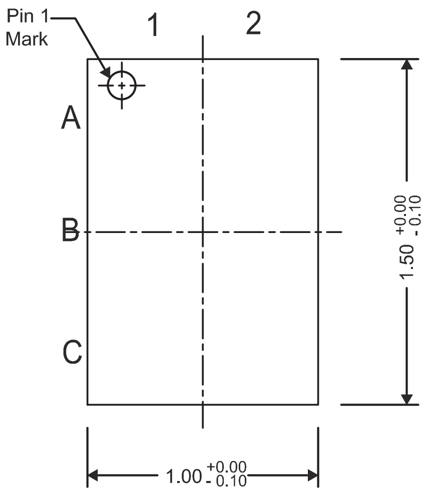


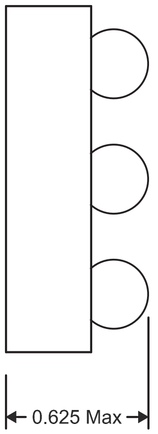
Figure 7-12. Maximum Drain Current vs Temperature

8 Mechanical Data

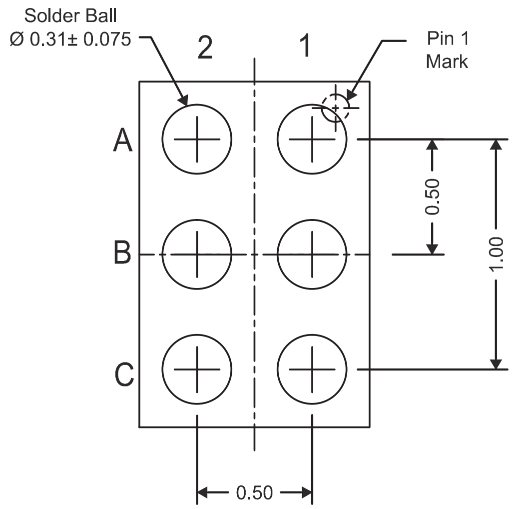
8.1 CSD25211W1015 Package Dimensions



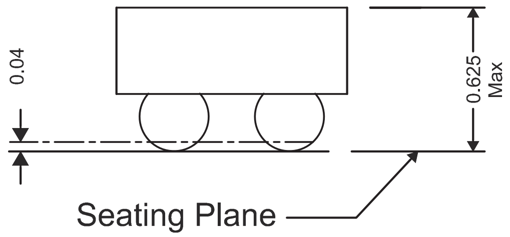
Top View



Side View



Bottom View



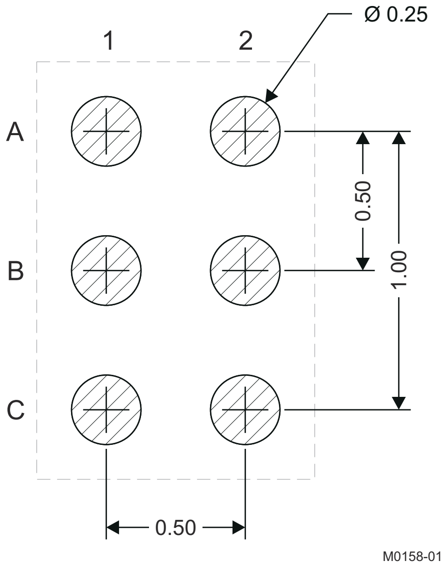
Front View

All dimensions are in mm (unless otherwise specified)

Pinout

POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source

8.2 Land Pattern Recommendation



All dimensions are in mm (unless otherwise specified)

9 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25211W1015	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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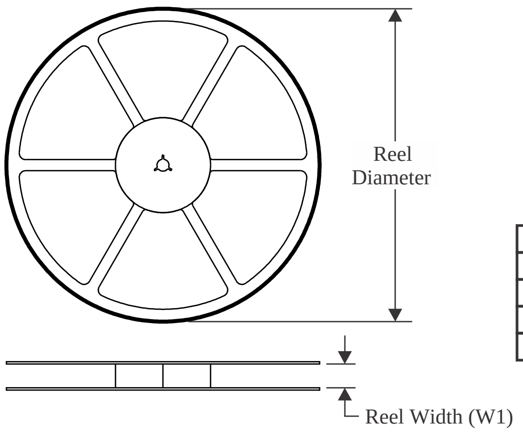
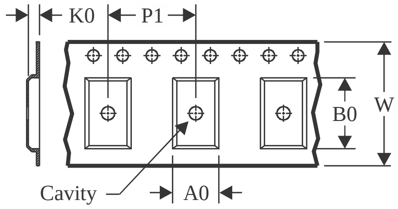
TAPE AND REEL INFORMATION

REEL DIMENSIONS

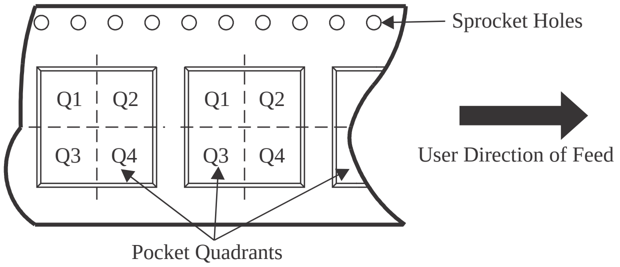


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

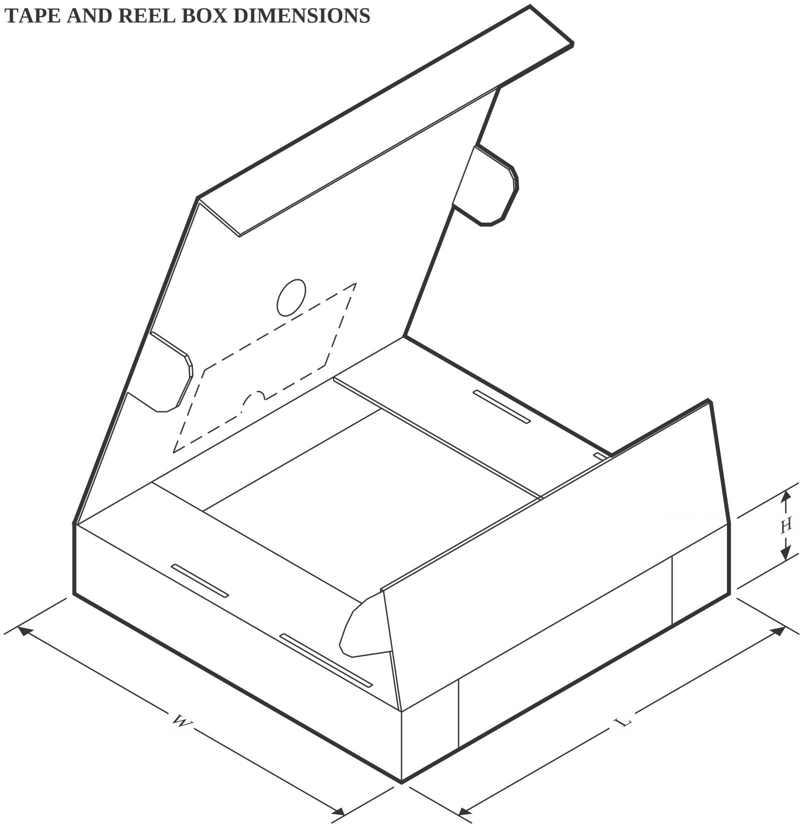
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25211W1015	DSBGA	YZC	6	3000	180.0	8.4	1.09	1.56	0.65	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25211W1015	DSBGA	YZC	6	3000	182.0	182.0	20.0

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