DF1704



SBAS099A – MARCH 2001

SoundPLUS™ Stereo, 24-Bit, 96kHz 8X Oversampling Digital Interpolation Filter

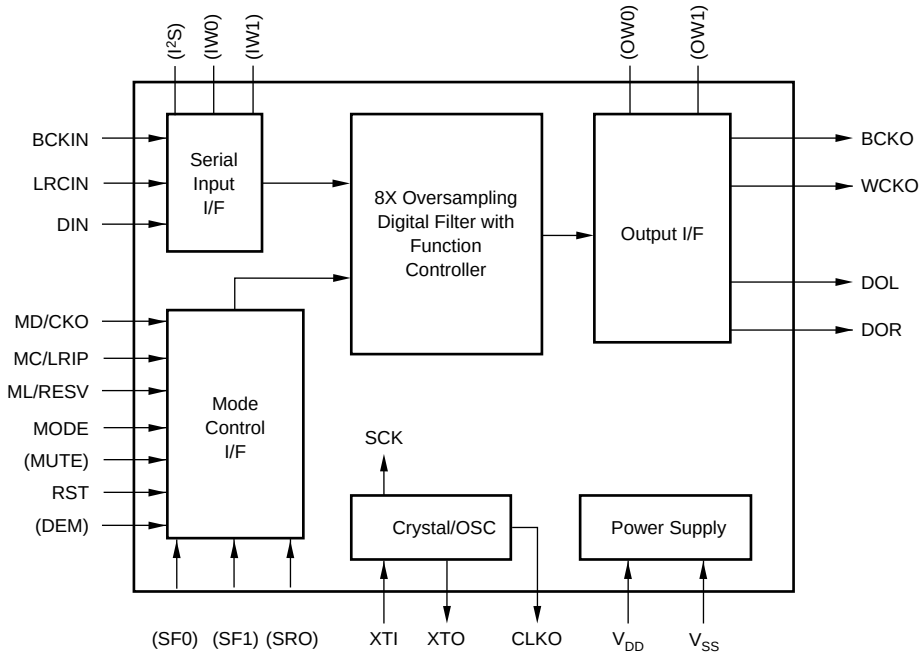
FEATURES

- **COMPANION DIGITAL FILTER FOR THE PCM1704 24-BIT AUDIO DAC**
- **HIGH PERFORMANCE FILTER:**
  Stopband Attenuation: –115dB
  Passband Ripple: ±0.00005dB
- **AUDIO INTERFACE:**
  Input Data Formats: Standard, Left-Justified, and I²S
  Input Word Length: 16, 20, or 24 Bits
  Output Word Length: 16, 18, 20, or 24 Bits
  Sampling Frequency: 32kHz to 96kHz
- **PROGRAMMABLE FUNCTIONS:**
  Hardware or Software Control Modes
  Sharp or Slow Roll-Off Filter Response
  Soft Mute
  Digital De-Emphasis
  Independent Left/Right Digital Attenuation
- **SYSTEM CLOCK: $256f_S$, $384f_S$, $512f_S$, $768f_S$**
- **ON-CHIP CRYSTAL OSCILLATOR**
- **+5V SINGLE-SUPPLY OPERATION**
- **SMALL SSOP-28 PACKAGE**

DESCRIPTION

The DF1704 is a high-performance, stereo, 8X oversampling digital interpolation filter designed for high-end consumer and professional audio applications. The DF1704 supports 24-bit, 96kHz operation and features user-programmable functions, including selectable filter response, de-emphasis, attenuation, and input/output data formats.

The DF1704 is the ideal companion for Texas Instruments' PCM1704 24-bit audio digital-to-analog converter. This combination allows for construction of very high-performance audio systems and components.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DF1704E	SSOP-28	324	–25°C to +85°C	DF1704E	DF1704E	Rails

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} , $V_{CC}1$, $V_{CC}2R$, $V_{CC}2L$) ..... +6.5V
Supply Voltage Differences ..... ±0.1
GND Voltage Differences ..... ±0.1V
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Input Current (any pins except power supplies) ..... ±10mA
Power Dissipation 300mW
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature ..... –55°C to +125°C
Lead Temperature (soldering, 5s) ..... +260°C
Package Temperature (reflow, 10s) ..... +235°C

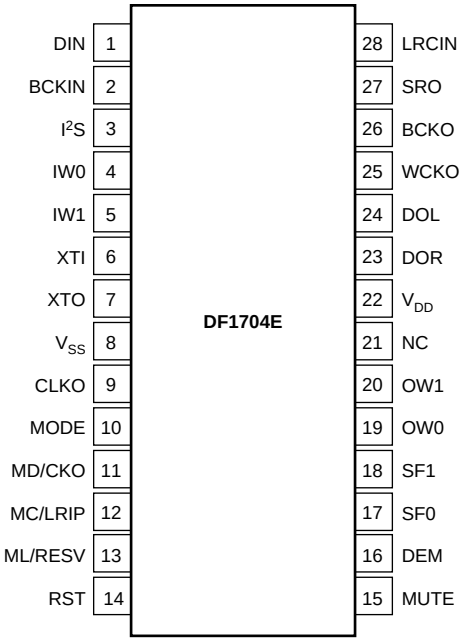
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

TOP VIEW SSOP



NC: No Connection

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	DIN	IN	Serial Audio Data Input(3)
2	BCKIN	IN	Bit Clock Input for Serial Audio Data(3)
3	I^2S	IN	Input Audio Data Format Selection(2, 4)
4	IW0	IN	Input Audio Data Word Selection(2, 4)
5	IW1	IN	Input Audio Data Word Selection(2, 4)
6	XTI	IN	Oscillator Input / External Clock Input
7	XTO	OUT	Oscillator Output
8	V_{SS}	—	Digital Ground
9	CLKO	OUT	Buffered System Clock Output
10	MODE	IN	Mode Control Selection (H: Software, L: Hardware)(1)
11	MD/CKO	IN	Control Data Input/Clock Output Frequency Select(1, 5)
12	MC/LRIP	IN	Control Data Clock/Polarity of LRCK Select(1, 5)
13	ML/RESV	IN	Control Data Latch/Reserved(1, 5)
14	RST	IN	Reset. When this pin is LOW, the digital filter is held in reset.(1)
15	MUTE	IN	Mute Control(1, 4)
16	DEM	IN	De-Emphasis Control(2, 4)
17	SF0	IN	Sampling Rate Select for De-emphasis(2, 4)
18	SF1	IN	Sampling Rate Select for De-emphasis(2, 4)
19	OW0	IN	Output Audio Data Word and Format Select(2, 4)
20	OW1	IN	Output Audio Data Word and Format Select(2, 4)
21	NC	—	No Connection
22	V_{DD}	—	Digital Power, +5V
23	DOR	OUT	Rch, Serial Audio Data Output
24	DOL	OUT	Lch, Serial Audio Data Output
25	WCKO	OUT	Word Clock for Serial Audio Data Output
26	BCKO	OUT	Bit Clock for Serial Audio Data Output
27	SRO	IN	Filter Response Select(2, 4)
28	LRCIN	IN	L/R Clock Input (f_S) for Serial Audio Data(3)

NOTES: (1) Pins 10-15; Schmitt-Trigger input with pull-up resistor. (2) Pins 3-5, 16-20, 27; Schmitt-Trigger input with pull-down resister. (3) Pins 1, 2, 28; Schmitt-Trigger input. (4) Pins 3-5, 15-20, 27; these pins are invalid when MODE (pin 10) is HIGH. (5) Pins 11-13; these pins have different functions corresponding to MODE (pin 10), (HIGH/LOW).

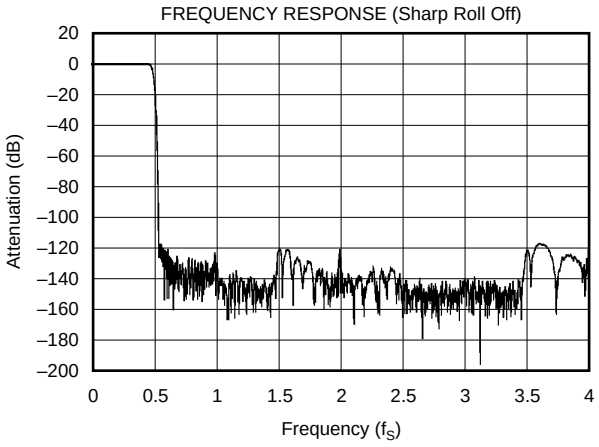
ELECTRICAL CHARACTERISTICS

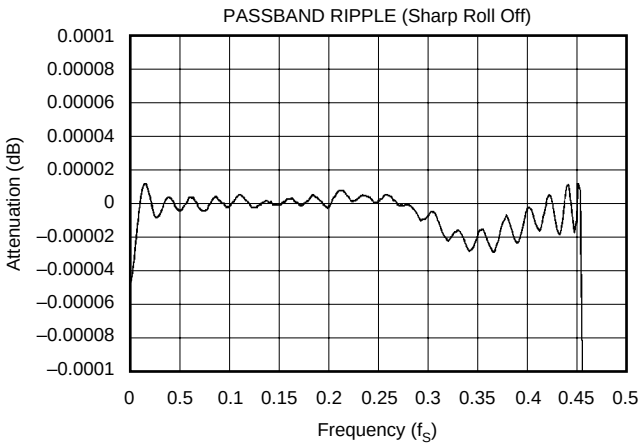
All specifications at +25°C, V_{DD} = +5V, unless otherwise noted.

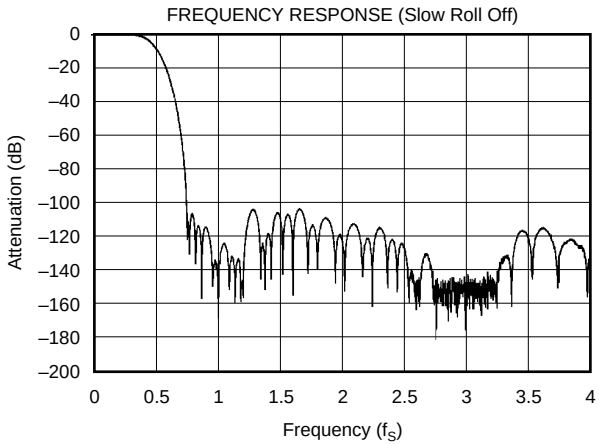
PARAMETER	CONDITIONS	DF1704E MIN	DF1704E TYP	DF1704E MAX	UNITS
RESOLUTION			24		Bits
INPUT DATA FORMAT					
Audio Data Interface Format			Standard / Left-Justified / I^2S		
Audio Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB-First, Two's Binary Comp		
Sampling Frequency (f_S)		32		96	kHz
System Clock Frequency			$256/384/512/768f_S$		
OUTPUT DATA FORMAT					
Audio Data Interface Format			Right-Justified		
Audio Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB-First, Binary Two's Complement		
DIGITAL INPUT/OUTPUT					
Input Logic Level: V_{IH}		2.0			V
V_{IL}				0.8	V
Output Logic Level: V_{OH}	I_{OH} = 2mA	4.5			V
V_{OL}	I_{OL} = 4mA			0.5	V
CLKO AC CHARACTERISTICS					
Rise Time (t_R)	20% to 80% V_{DD}, 10pF		4		ns
Fall Time (t_F)	80% to 20% V_{DD}, 10pF		3		ns
Duty Cycle	10pF Load		37		%
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1 (Sharp Roll-Off)					
Passband	±0.00005dB			$0.454f_S$	
	–3dB			$0.493f_S$	
Stopband		$0.546f_S$			
Passband Ripple				±0.00005	dB
Stopband Attenuation	Stopband = $0.546f_S$	–115			dB
Filter Characteristics 2 (Sharp Roll-Off)					
Passband Ripple	±0.0001dB			$0.254f_S$	
	–3dB			$0.460f_S$	
Stopband		$0.732f_S$			
Passband Ripple				±0.0001	dB
Stopband Attenuation	Stopband = $0.748f_S$	–100			dB
Delay Time			$45.125/f_S$		sec
De-Emphasis Error				±0.003	dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}	4.5	5	5.5	VDC
Supply Current: I_{DD}			20	30	mA
Power Dissipation			100	150	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

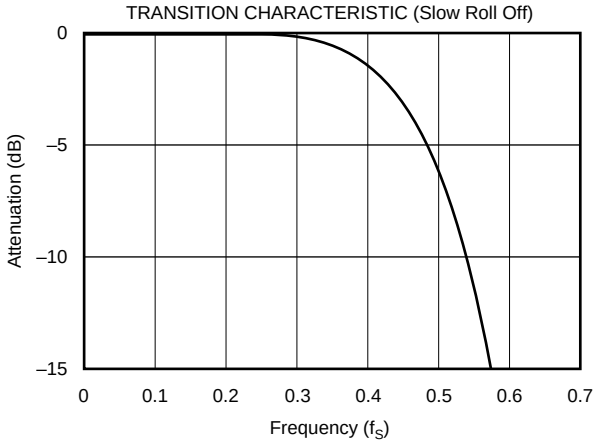
TYPICAL CHARACTERISTICS OF INTERNAL FILTER

DIGITAL FILTER (DE-EMPHASIS OFF, f_S = 44.1kHz)

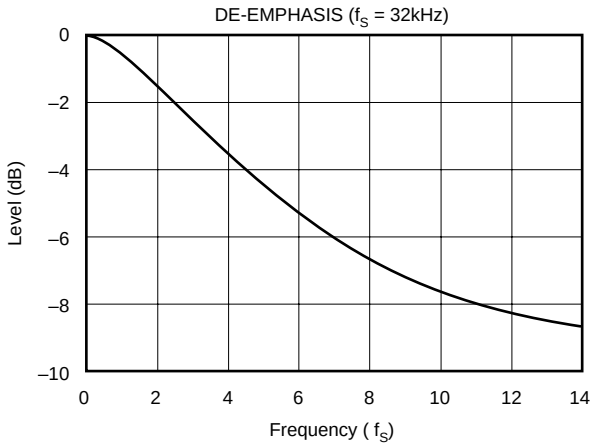


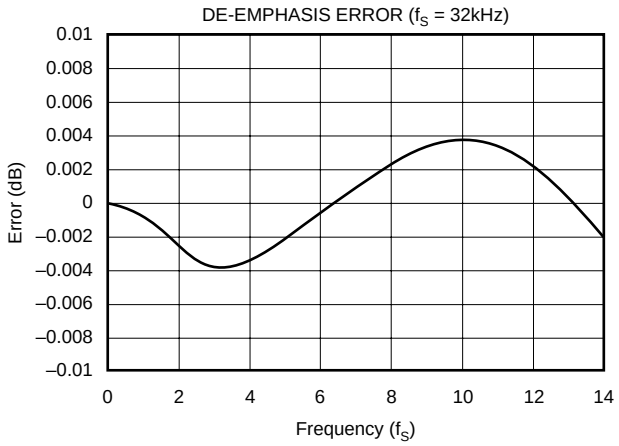




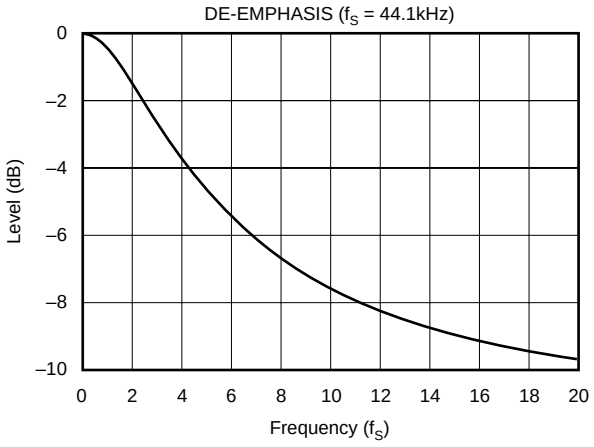


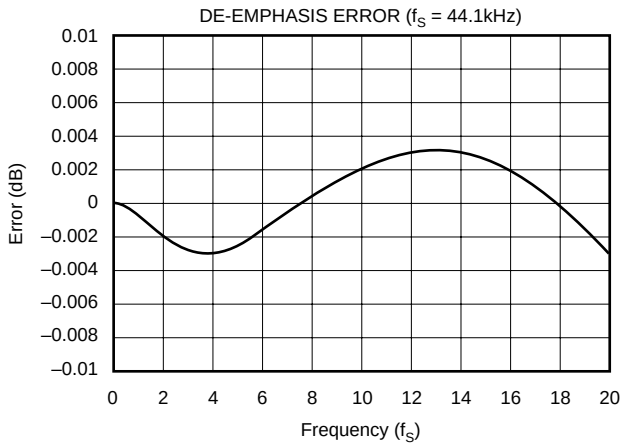
DE-EMPHASIS AND DE-EMPHASIS ERROR

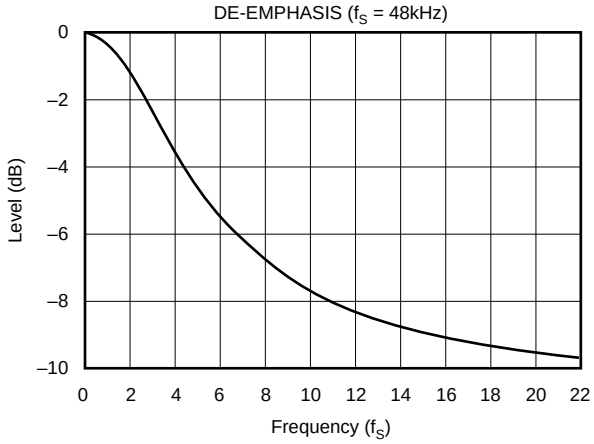


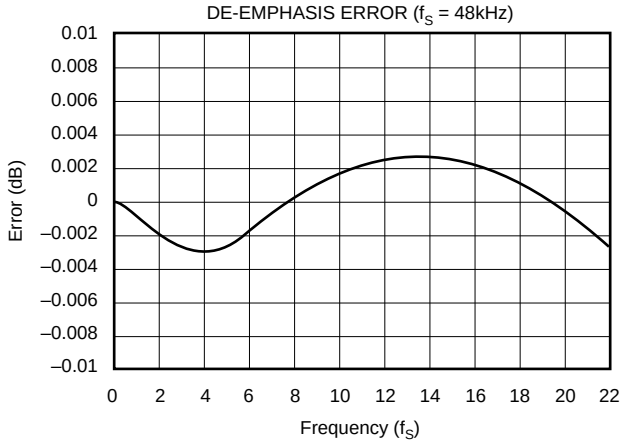


TYPICAL CHARACTERISTICS OF INTERNAL FILTER (Cont.)









SYSTEM CLOCK REQUIREMENTS

The system clock of the DF1704 can be supplied by either an external clock signal at XTI (pin 6), or by the on-chip crystal oscillator. The system clock rate must run at $256f_S$, $384f_S$, $512f_S$, or $768f_S$, where f_S is the audio sampling rate.

It should be noted that a $768f_S$ system clock cannot be used when f_S = 96kHz. In addition, the on-chip crystal oscillator is limited to a maximum frequency of 24.576MHz. Table I shows the typical system clock frequencies for selected sample rates.

The DF1704 includes a system clock detection circuit that determines the system clock rate in use. The circuit compares the system clock input (XTI) frequency with the LRCIN input rate to determine the system clock multiplier. Ideally, LRCIN and BCKIN should be derived from the system clock to ensure proper synchronization. If the phase difference between the system clock and LRCIN is larger than ±6 bit clock (BCKIN) periods, the synchronization of the system and LRCIN clocks will be performed automatically by the DF1704.

Timing requirements for the system clock input are shown in Figure 1.

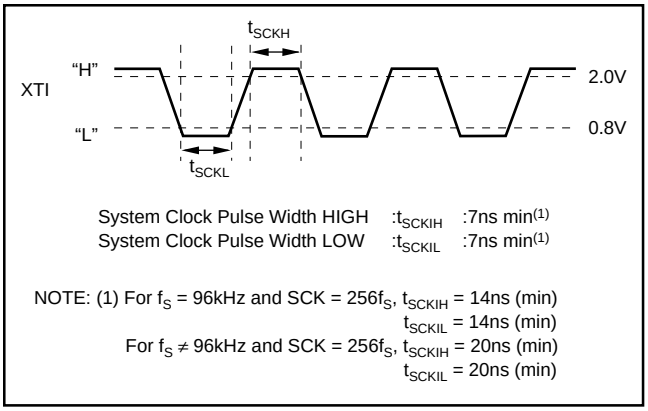


FIGURE 1. System Clock Timing.

RESET

The DF1704 has both an internal power-on reset circuit and a reset pin, $\overline{RST}$ (pin 14), for providing an external reset signal. The internal power-on reset is performed automatically when power is applied to the DF1704, as shown in Figure 2. The $\overline{RST}$ pin can be used to synchronize the DF1704 with a system reset signal, as shown in Figure 3.

During the power-on reset period (1024 system clocks), the DF1704 outputs are forced LOW. For an external forced reset, the outputs are forced LOW during the initialization period (1024 system clocks), which occurs after the LOW-to-HIGH transition of the $\overline{RST}$ pin as shown in Figure 3.

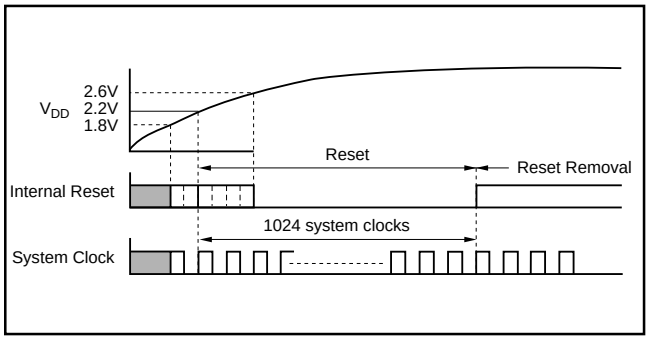


FIGURE 2. Internal Power-On Reset Timing.

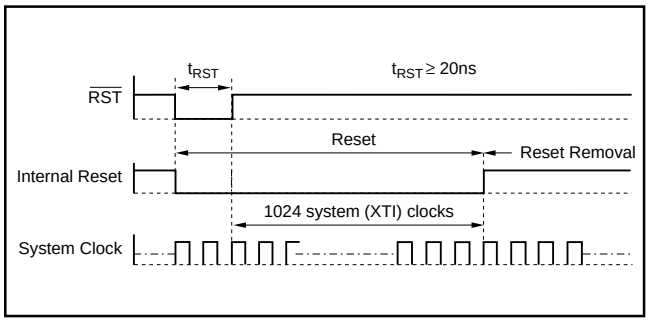


FIGURE 3. External Forces Reset Timing.

AUDIO INPUT INTERFACE

The audio input interface is comprised of BCKIN (pin 2), LRCIN (pin 28), and DIN (pin 1).

BCKIN is the input bit clock, which is used to clock data applied at DIN into the DF1704's input serial interface. Input data at DIN is clocked into the DF1704 on the rising edge of BCKIN. The left/right clock, LRCIN, is used as a word latch for the audio input data.

BCKIN can run at $32f_S$, $48f_S$, or $64f_S$, where f_S is the audio sample frequency. LRCIN is run at the f_S rate. Figures 4 (a) through 4 (c) show the input data formats, which are selected by hardware or software controls. Figure 5 shows the audio input interface timing requirements.

SAMPLING RATE FREQUENCY (f_S)	SYSTEM CLOCK FREQUENCY (MHz)			
	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	8.1920	12.2880	16.3840	24.5760
44.1kHz	11.2896	16.9340	22.5792	33.8688(1)
48kHz	12.2880	18.4320	24.5760	36.8640(1)
96kHz	24.5760(3)	36.8640(1)	49.1520(1)	See Notes 1, 2

NOTES: (1) Maximum crystal oscillator frequency is 24.576MHz and cannot be used for these combinations. (2) $768f_S$ system clock cannot be used with 96kHz sampling rate. (3) Use external system clock applied at XTI.

TABLE I. Typical System Clock Frequencies.

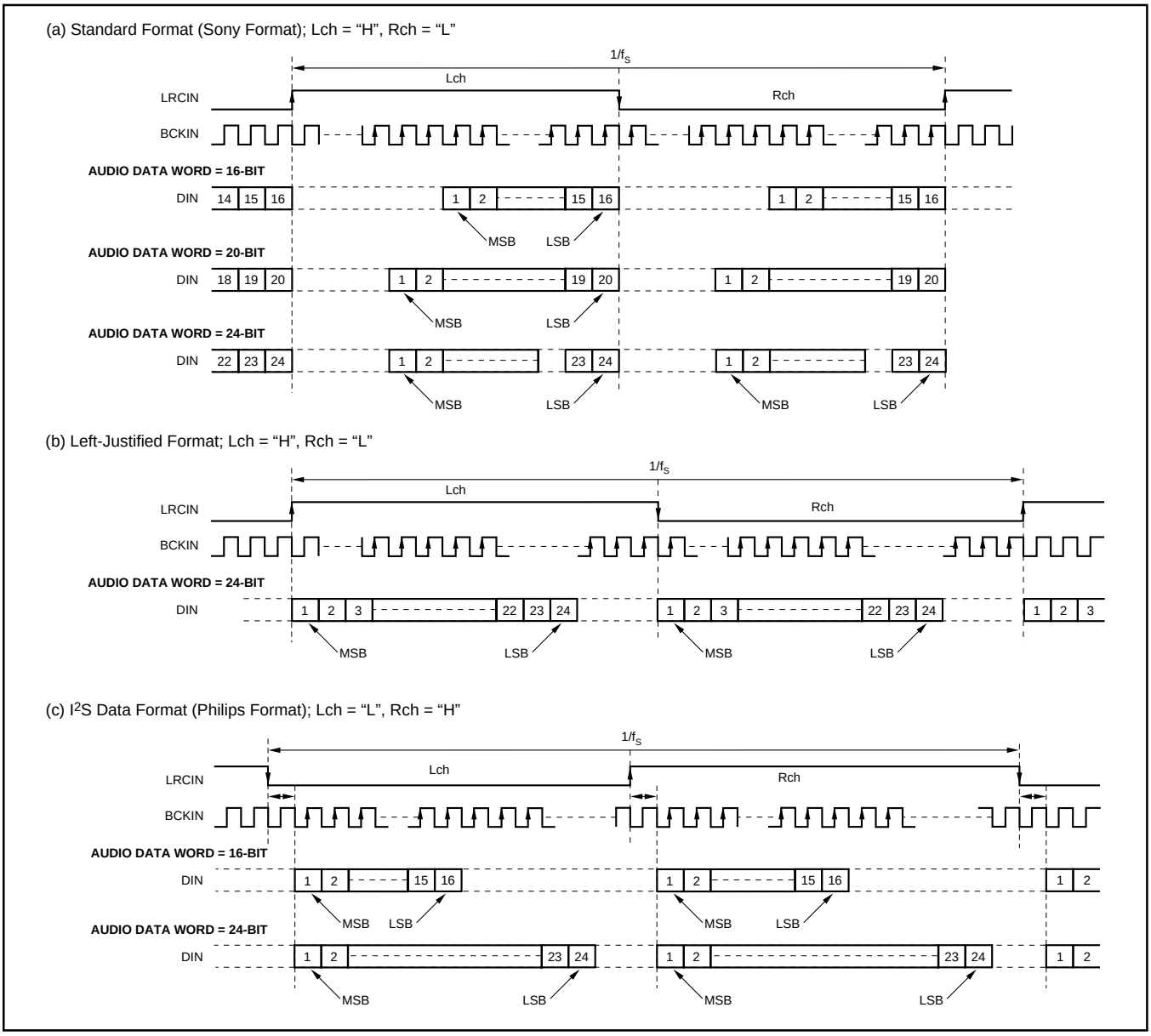
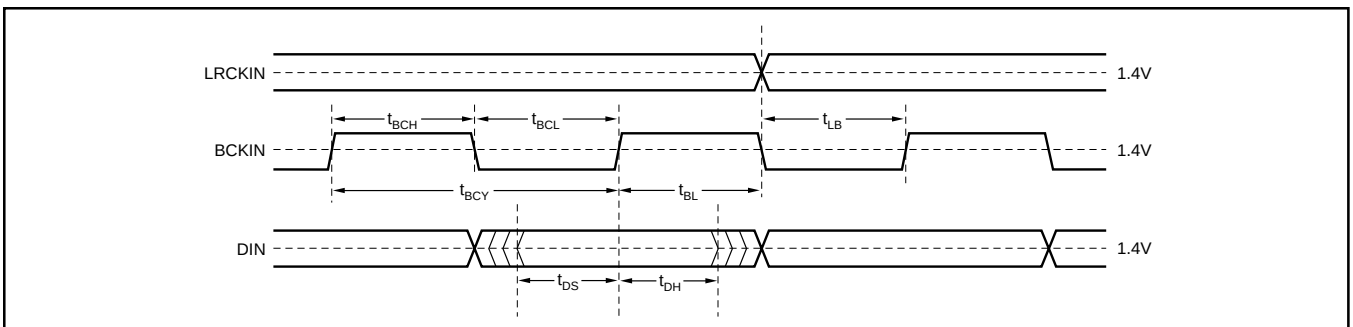


FIGURE 4. Audio Data Input Formats.



BCKIN Pulse Cycle Time	t_{BCY}	100ns (min)
BCKIN Pulse Width HIGH	t_{BCH}	50ns (min)
BCKIN Pulse Width LOW	t_{BCL}	50ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	30ns (min)
LRCIN Edge to BCKIN Rising Edge	t_{LB}	30ns (min)
DIN Set-up Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)

FIGURE 5. Audio Input Interface Timing.

AUDIO OUTPUT INTERFACE

The audio output interface includes BCKO (pin 26), WCKO (pin 25), DOL (pin 24), and DOR (pin 23).

BCKO is the output bit clock and is used to clock data into an audio Digital-to-Analog Converter (DAC), such as the PCM1704. DOL and DOR are the left and right audio data outputs. WCKO is the output word clock and is used to latch audio data words into an audio DAC.

WCKO runs at a fixed rate of $8f_S$ (8X oversampling) for all system clock rates.

BCKO is fixed at $256f_S$ for system clock rates of $256f_S$ or $512f_S$.

BCKO is fixed at $192f_S$ for system clock rates of $384f_S$ or $768f_S$.

The output data format used by the DF1704 for DOL and DOR is Binary Two's Complement, MSB-first, right-justified audio data. Figures 6(a) and 6(b) show the output data formats for the DF1704. Figure 7 shows the audio output timing.

MODE CONTROL

The DF1704 may be configured using either software or hardware control. The selection is made using the MODE input (pin 10).

MODE SETTING	MODE CONTROL SELECTION
MODE = H	Software Mode
MODE = L	Hardware Mode

TABLE II. MODE Selection.

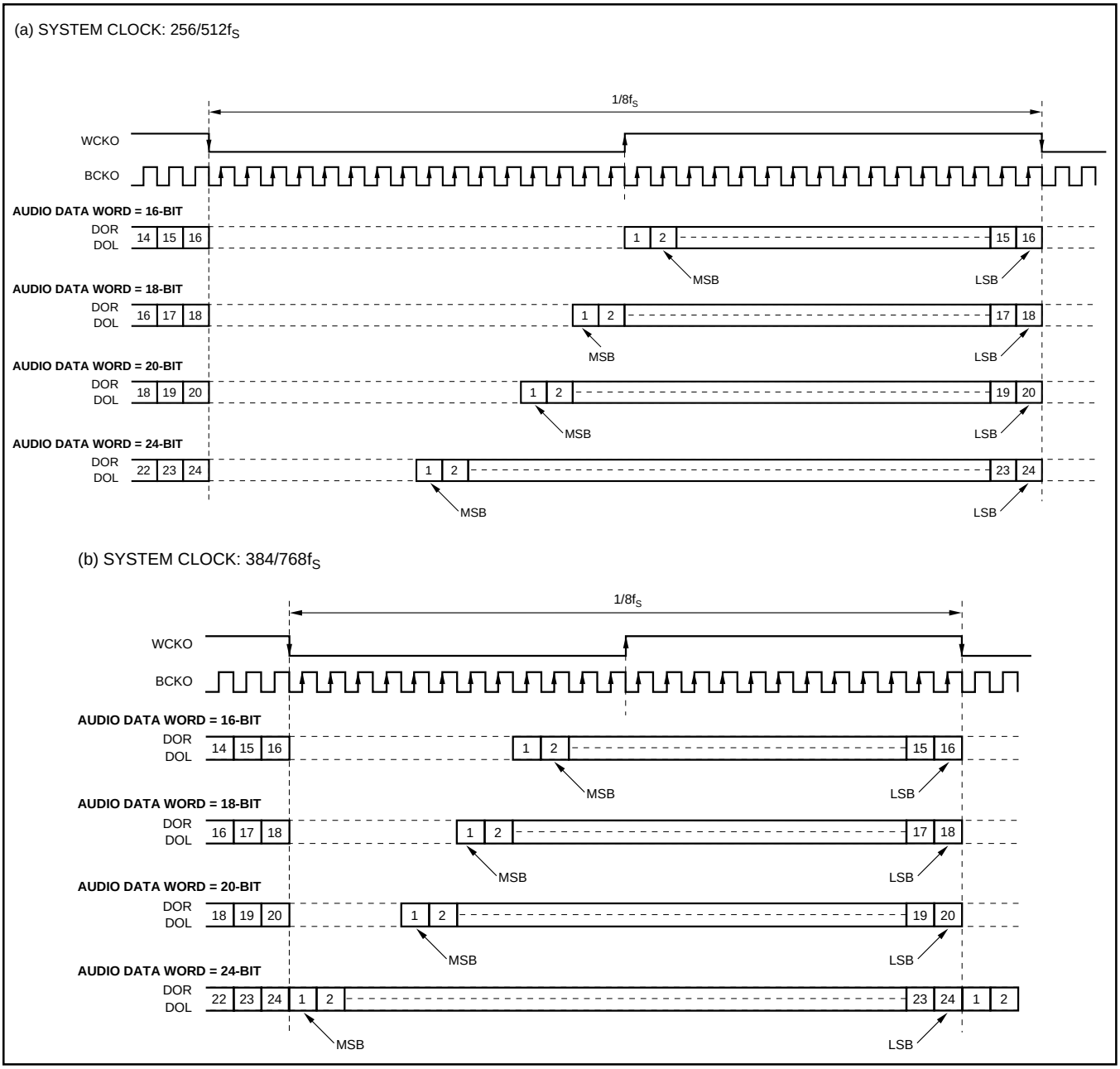
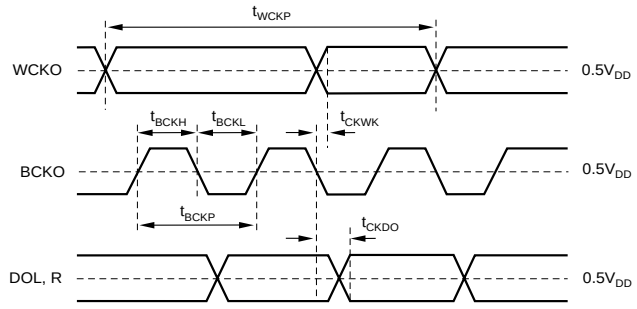


FIGURE 6. Audio Output Data Format.



		min	typ	max
BCKO Period	t_{BCKP}	1/256 f_S or 1/192 f_S		
BCKO Pulse Width High(4)	t_{BCKH}	20ns		100ns
BCKO Pulse Width Low(4)	t_{BCKL}	20ns		100ns
Delay Time BCKO Falling Edge to WCKO Valid	t_{CKWK}	–5ns		5ns
WCKO Period	t_{WCKP}		1/8 f_S	
Delay Time BCKO Falling Edge to DOL, R Valid	t_{CKDO}	–5ns		5ns
Rising Time of All Signals	t_R			7ns
Falling Time of All Signals	t_F			7ns

NOTES: (1) Timing measurement reference level is (V_{IH}/V_{IL})/2. (2) Rising and falling time is measured from 10% to 90% of IN/OUT signals' swing. (3) Load capacitance of all signals are 20pF. (4) Exceptions: f_S = 96kHz and SCK = 256f_S, t_{BCKH} = 14ns (min) t_{BCKL} = 14ns (min)

FIGURE 7. Audio Output Data Format.

Programmable Functions

The DF1704 includes a number of programmable features, with most being accessible from either Hardware or Software mode. Table III summarizes the user programmable functions for both modes of operation.

FUNCTION	SOFTWARE (MODE = H)	HARDWARE (MODE = L)	RESET DEFAULT (Software Mode)
Input Data Format Selection	0	0	Standard Format
Input Word Length Selection	0	0	16 Bits
Output Word Length Selection	0	0	16 Bits
LRCIN Polarity Selection	0	0	Left/Right = High/Low
Digital De-Emphasis	0	0	OFF
Soft Mute	0	0	OFF
Digital Attenuation	0	X	0dB, Independent L/R
Sample Rate for De-Emphasis Function	0	0	44.1 kHz
Filter Roll-Off Selection	0	0	Sharp Roll-Off Selected
CLKO Output Frequency Selection	0	0	Same As XTI Input

Legend: 0 = User Programmable, X = Not Available.

TABLE III. User-Programmable Functions for Software and Hardware Mode.

Hardware Mode Controls

With MODE = L, the DF1704 may be configured by utilizing several user-programmable pins. The following is a brief summary of the pin functions. Table IV provides more details on setting the hardware mode controls.

Pins I^2S, IW0, and IW1 are used to select the audio data input format and word length.

Pins OW0 and OW1 are used to select the output data word length.

The DEM pin is used to enable and disable the digital de-emphasis function. De-emphasis is only available for 32kHz, 44.1kHz, and 48kHz sample rates.

Pins SF0 and SF1 are used to select the sample rate for the de-emphasis function.

The SRO pin is used to select the digital filter response, either sharp or slow roll-off.

The MUTE pin is used to enable or disable the soft mute function.

The CKO pin is used to select the clock frequency seen at the CLKO pin, either XTI or XTI ÷ 2.

The LRIP pin is used to select the polarity used for the audio input left/right clock, LRCIN.

Finally, the RESV pin is not used by the current DF1704 design, but is reserved for future use.

Software Mode Controls

With MODE = H, the DF1704 may be configured by programming four internal registers in software mode. ML (pin 13), MC (pin 12), and MD (pin 11) make up the 3-wire software control port, and may be controlled using DSP or microcontroller general purpose I/O pins, or a serial port. Table V provides an overview of the internal registers, labeled MODE0 through MODE3.

PIN NAME	PIN NUMBER	DESCRIPTION
RESV	13	Reserved, Not Used
LRIP	12	LRCIN Polarity LRIP = L: LRCIN= H = Left Channel, LRCIN= L = Right Channel LRIP = H: LRCIN= L = Left Channel, LRCIN = H = Right Channel
CKO	11	CLKO Output Frequency CKO = H: CLKO Frequency = XTI/2 CKO = L: CLKO Frequency = XTI
MUTE	15	Soft Mute Control: H = Mute Off, L = Mute On
I^2S IW0 IW1	3 4 5	Input Data Format Controls **I^2S IW1 IW0 INPUT FORMAT** L L L 16-Bit, Standard, MSB-First, Right-Justified L L H 20-Bit, Standard, MSB-First, Right-Justified L H L 24-Bit, Standard, MSB-First, Right-Justified L H H 24-Bit, MSB-First, Left-Justified H L L 16-Bit, I^2S H L H 24-Bit, I^2S
SRO	27	Digital Filter Roll-Off: H = Slow, L = Sharp
OW0 OW1	19 20	Output Data Word Length Controls **OW1 OW0 OUTPUT FORMAT** L L 16-Bit, MSB-First L H 18-Bit, MSB-First H L 20-Bit, MSB-First H H 24-Bit, MSB-First
SF0 SF1	17 18	Sample Rate Selection for the Digital De-Emphasis Control **SF1 SF0 SAMPLING RATE** L L 44.1kHz L H Reserved, Not Used H L 48kHz H H 32kHz
DEM	16	Digital De-Emphasis: H = On, L = Off

TABLE IV. Hardware Mode Controls.

Figures 8 through 10 show more details regarding the control port data format and timing requirements. The data format for the control port is 16-bit, MSB-first, with Bit B15 being the MSB.

REGISTER NAME	BIT NAME	DESCRIPTION
MODE0	AL[7:0] LDL A[1:0] res	Attenuation Data for the Left Channel Attenuation Load Control for the Left Channel Register Address Reserved
MODE1	AR[7:0] LDL A[1:0] res	Attenuation Data for the Right Channel Attenuation Load Control for the Right Channel Register Address Reserved
MODE2	MUT DEM IW[1:0] OW[1:0] A[1:0] res	Soft Mute Control Digital De-Emphasis Control Input Data Format and Word Length Output Data Word Length Register Address Reserved
MODE3	I^2S LRP ATC SRO CKO SF[1:0] A[1:0] res	Input Data Format (I^2S or Standard/Left-Justified) LRCIN Polarity Attenuator Control, Dependent or Independent Digital Filter Roll-Off Selection (sharp or slow) CLKO Frequency Selection (XTI or XTI ÷ 2) Sample Rate Selection for De-Emphasis Function Register Address Reserved

NOTE: All reserved bits should be programmed to 0.

TABLE V. Internal Register Mapping.

Register Addressing

A[1:0], bits B10 and B9 of the 16-bit control data word, are used to indicate the register address to be written to by the current control port write cycle. Table VI shows how to address the internal registers using bits A[1:0] of registers MODE0 through MODE3.

A1	A0	REGISTER SELECTED
0	0	MODE0
0	1	MODE1
1	0	MODE2
1	1	MODE3

TABLE VI. Internal Register Addressing.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	res	res	OW1	OW0	IW1	IW0	res	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	res	SF1	SF0	CKO	res	SRO	ATC	LRP	I^2S

FIGURE 8. Internal Mode Control Registers.

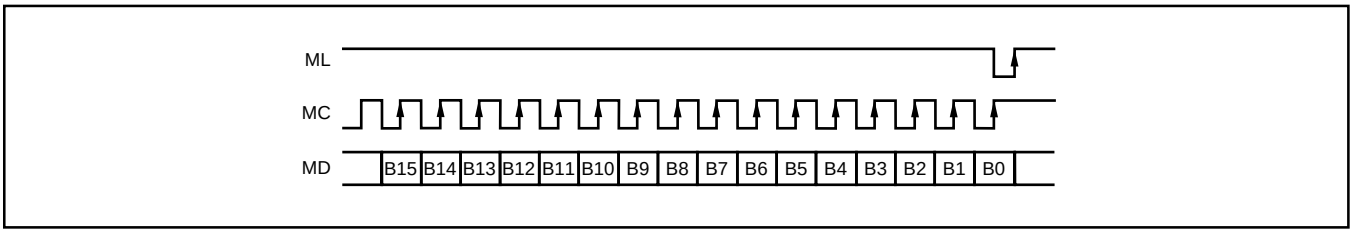
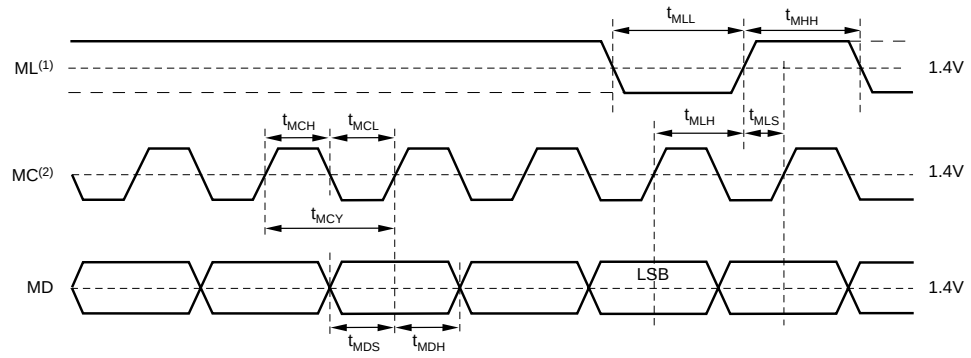


FIGURE 9. Software Interface Format.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
MD Set-Up Time	t_{MDS}	40ns (min)
ML Low Level Time	t_{MLL}	40ns + 1SYSCLK(3) (min)
ML High Level Time	t_{MHH}	40ns + 1SYSCLK(3) (min)
ML Hold Time(2)	t_{MLH}	40ns (min)
ML Set-Up Time(3)	t_{MLS}	40ns (min)

NOTES: (1) ML rising edge to the next MC rising edge. (2) MC rising edge for LSB to ML rising edge. (3) SYSCK: System Clock Cycle.

FIGURE 10. Software Interface Timing Requirements.

MODE0 Register

The MODE0 register is used to set the attenuation data for the Left output channel, or DOL (pin 24).

When ATC = 1 (Bit B2 of Register MODE3 = 1), the Left channel attenuation data AL[7:0] is used for both the Left and Right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), Left channel attenuation data is taken from AL[7:0] of register MODE0, and Right channel attenuation data is taken from AR[7:0] of register MODE1.

AL[7:0] Left Channel Attenuator Data, where AL7 is the MSB and AL0 is the LSB.
Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255)dB

For DATA = FFh, ATTEN = –0dB
For DATA = FEh, ATTEN = –0.5dB
For DATA = 01h, ATTEN = –127.5dB
For DATA = 00h, ATTEN = infinity = Mute

LDL Left Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the Left and Right channels.

When LDL = 1, the Left channel output level is set by the data in AL[7:0]. The Right channel output level is set by the data in AL[7:0], or the most recently programmed data in bits AR[7:0] of register MODE1.

When LDL = 0, the Left channel output data remains at its previously programmed level.

MODE1 Register

The MODE1 register is used to set the attenuation data for the Right output channel, or DOR (pin 23).

When ATC = 1 (Bit B2 of Register MODE3 = 1), the Left channel attenuation data AL[7:0] of register MODE0 is used for both the Left and Right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), Left channel attenuation data is taken from AL[7:0] of register MODE0, and Right channel attenuation data is taken from AR[7:0] of register MODE1.

AR[7:0] Right Channel Attenuator Data, where AR7 is the MSB and AR0 is the LSB. Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255)dB

For DATA = FFh, ATTEN = –0dB
For DATA = FEh, ATTEN = –0.5dB
For DATA = 01h, ATTEN = –127.5dB
For DATA = 00h, ATTEN = infinity = Mute

LDR Right Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the Left and Right channels.

When LDR = 1, the Right channel output level is set by the data in AR[7:0], or by the data in bits AL[7:0] of register MODE0. The Left channel output level is set to the most recently programmed data in bits AL[7:0] of register MODE0.

When LDR = 0, the Right channel output data remains at its previously programmed level.

MODE2 Register

The MODE2 register is used to program various functions:

MUT Soft Mute Function.

When MUT = 0, Soft Mute is ON for both Left and Right channels.
When MUT = 1, Soft Mute is OFF for both Left and Right channels.

DEM Digital De-Emphasis Function.

When DEM = 0, de-emphasis is OFF.
When DEM = 1, de-emphasis is ON.

IW[1:0] Input Data Format and Word Length.

I^2S	IW1	IW0	Description
0	0	0	16-Bit Data, Standard Format (MSB-First, Right-Justified)
0	0	1	20-Bit Data, Standard Format
0	1	0	24-Bit Data, Standard Format
0	1	1	24-Bit Data, MSB-First, Left-Justified
1	0	0	16-Bit Data, I^2S Format
1	0	1	24-Bit Data, I^2S format
1	1	0	Reserved
1	1	1	Reserved

OW[1:0] Output Data Word Length.

OW1	OW0	Description
0	0	16-Bit Data, MSB-First
0	1	18-Bit Data, MSB-First
1	0	20-Bit Data, MSB-First
1	1	24-Bit Data, MSB-First

MODE3 Register

The MODE3 register is used to program various functions.

I^2S Input Data Format.

When I^2S = 0, standard or left-justified formats are enabled.

When I^2S = 1, the I^2S formats are enabled.

LRP LRCIN Polarity Selection.

When LRP = 0, Left channel is HIGH and Right channel is LOW.

When LRP = 1, Left channel is LOW and Right channel is HIGH.

ATC Attenuator Control.
This bit is used to determine whether the Left and Right channel attenuators operate with independent data, or use common data (the Left channel data in bits AL[7:0] of register MODE0).

When ATC = 0, the Left and Right channel attenuator data is independent.

When ATC = 1, the Left and Right channel attenuators use common data.

SRO Digital Filter Roll-Off Selection.

When SRO = 0, sharp roll-off is selected.
When SRO = 1, slow roll-off is selected.

CKO CLKO Output Frequency Selection.

When CKO = 0, the CLKO frequency is the same as the clock at the XTI input.
When CKO =1, the CLKO frequency is half of the XTI input clock frequency.

SF[1:0] Sampling Frequency Selection for the De-Emphasis Function.

SF1	SF0	Description
0	0	44.1 kHz
0	1	Reserved
1	0	48 kHz
1	1	32 kHz

APPLICATIONS INFORMATION

PCB LAYOUT GUIDELINES

In order to obtain the specified performance from the DF1704 and its associated DACs, proper printed circuit board layout is essential. Figure 11 shows two approaches for obtaining the best audio performance.

Figure 11(a) shows a standard, mixed signal layout scheme. The board is divided into digital and analog sections, each with its own ground. The ground areas should be put on a split-plane, separate from the routing and power layers. The DF1704 and all digital circuitry should be placed over the digital section, while the audio DACs and analog circuitry should be located over the analog section of the board. A common connection between the digital and analog grounds is required and is done at a single point as shown.

For Figure 11(a), digital signals should be routed from the DF1704 to the audio DACs using short, direct connections to reduce the amount of radiated high-frequency energy. If necessary, series resistors may be placed in the clock and data signal paths to reduce or eliminate any overshoot or undershoot present on these signals. A value of 50Ω to 100Ω is recommended as a starting point, but the designer should experiment with the resistor values in order to obtain the best results.

Figure 11(b) shows an improved method for high performance, mixed signal board layout. This method adds digital isolation between the DF1704 and the audio DACs, and provides complete isolation between the digital and analog sections of the board. Texas Instrument's ISO150 dual digital coupler provides excellent isolation, and operates at speeds up to 80Mbps.

POWER SUPPLIES AND BYPASSING

The DF1704 requires a single +5V power supply for operation. The power supply should be bypassed by a 10μF and 0.1μF parallel capacitor combination. The capacitors should be placed as close as possible to V_{DD} (pin 22). Aluminum electrolytics or tantalum capacitors can be used for the 10μF value, while ceramics may be used for the 0.1μF value.

BASIC CIRCUIT CONNECTIONS

Figures 12 and 13 show basic circuit connections for the DF1704. Figure 12 shows connections for Hardware mode controls, while Figure 13 shows connections for Software mode controls. Notice the placement of C_1 and C_2 in both figures, as they are physically close to the DF1704.

TYPICAL APPLICATIONS

The DF1704 will typically be used in high-performance audio equipment, in conjunction with high-performance audio DACs. Figure 14 shows a typical application circuit example, employing the DF1704, a digital audio receiver, and two PCM1704 24-bit, 96kHz audio DACs.

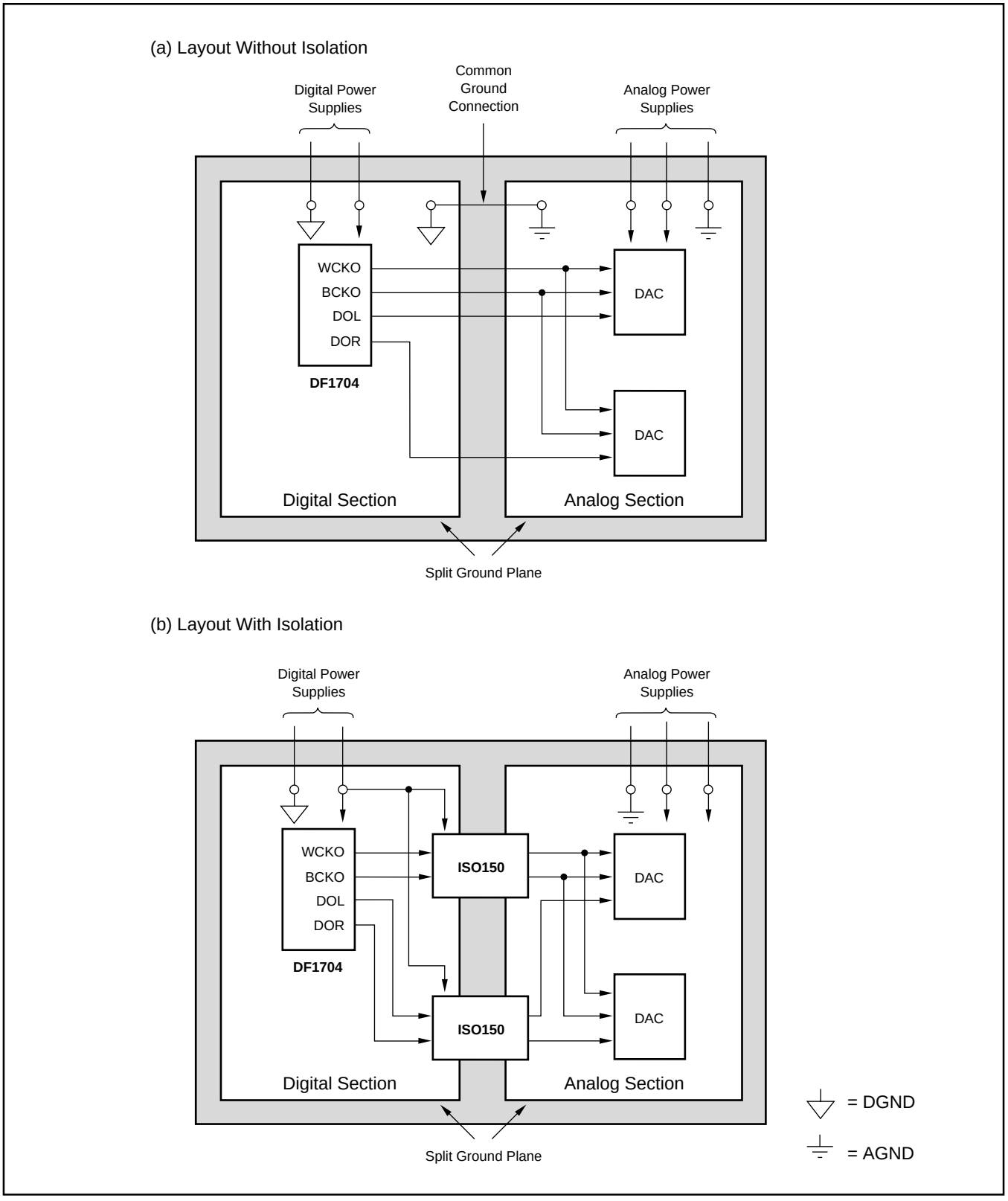


FIGURE 11. PCB Layout Model.

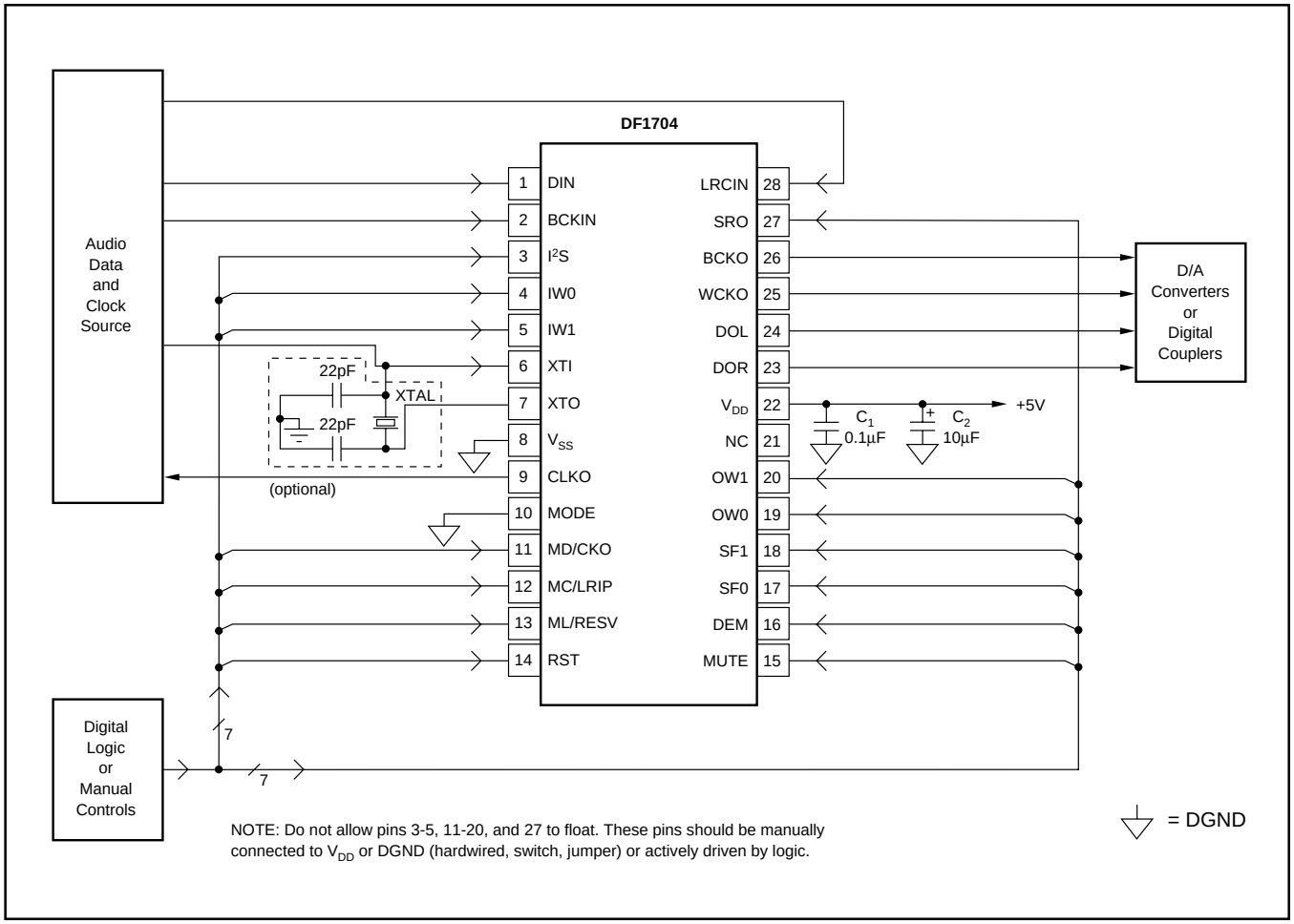


FIGURE 12. Basic Circuit Connections, Hardware Control.

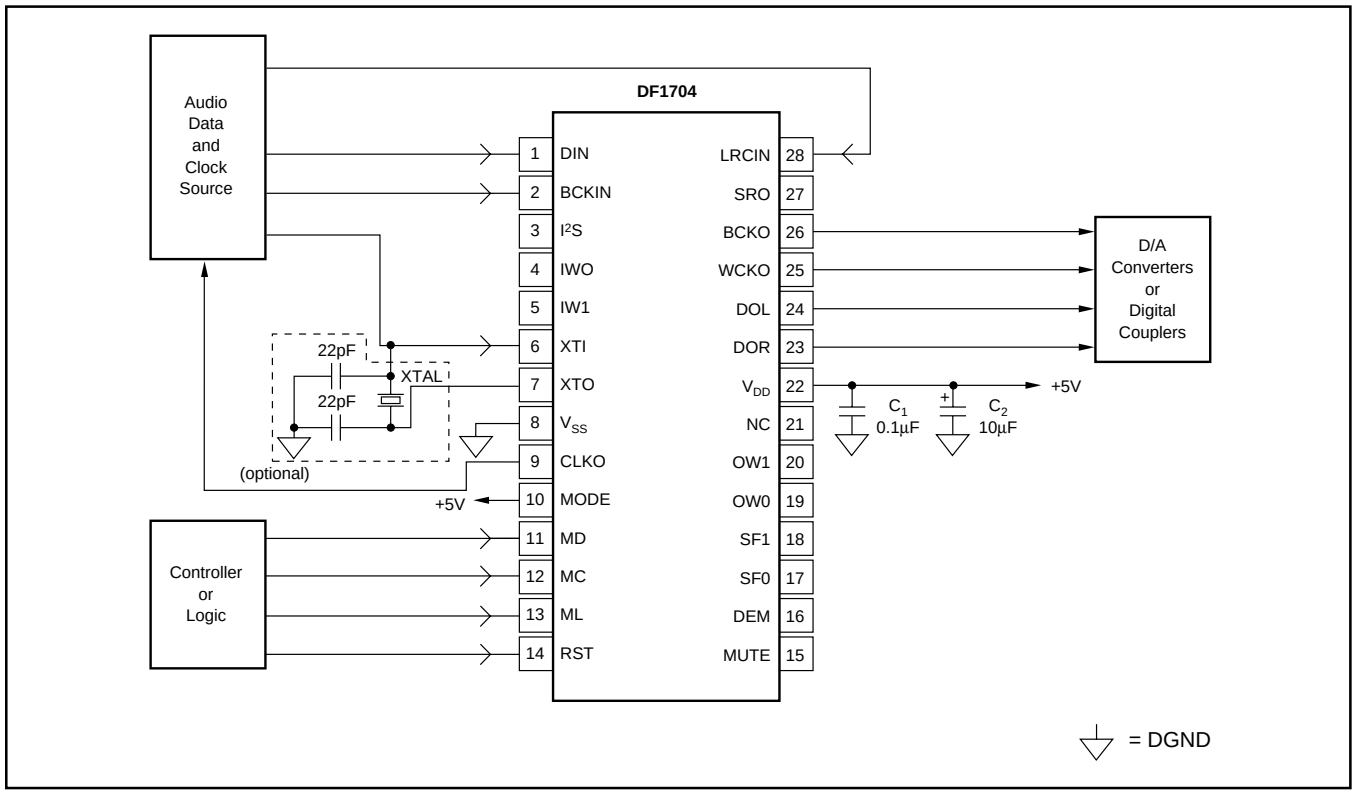


FIGURE 13. Basic Circuit Connection, Software Control.

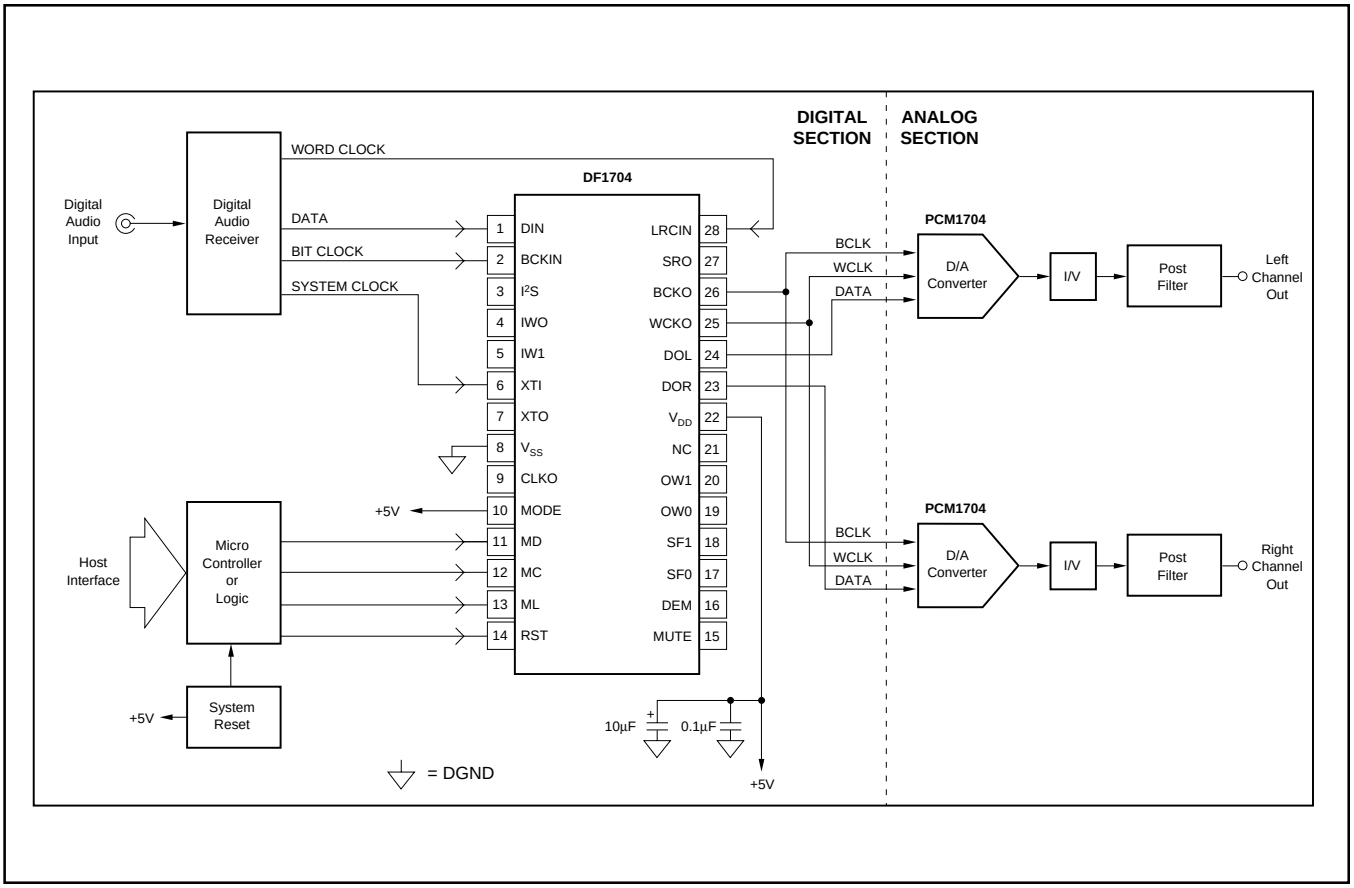


FIGURE 14. DF1704 Typical Application Circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DF1704E	Last Time Buy	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	DF1704E
DF1704E.B	Last Time Buy	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See DF1704E	DF1704E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

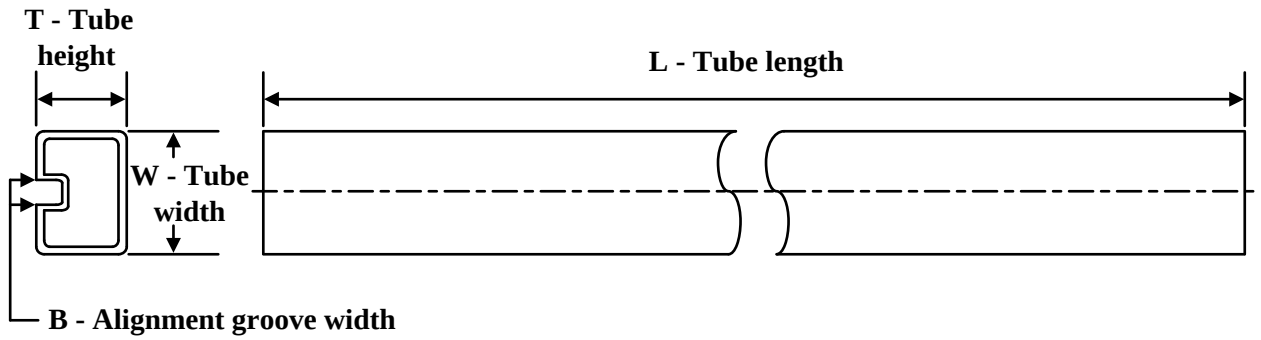
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DF1704E	DB	SSOP	28	47	500	10.6	500	9.6
DF1704E.B	DB	SSOP	28	47	500	10.6	500	9.6

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