

SBVS070B − JUNE 2006 − REVISED MAY 2009

Sensor Signal Conditioning IC for Closed-Loop Magnetic Current Sensor

FEATURES

- DESIGNED FOR SENSORS FROM VACUUMSCHMELZE (VAC)
- SINGLE SUPPLY: 5V
- POWER OUTPUT: H-Bridge
- DESIGNED FOR DRIVING INDUCTIVE LOADS
- EXCELLENT DC PRECISION
- WIDE SYSTEM BANDWIDTH
- HIGH-RESOLUTION, LOW-TEMPERATURE DRIFT
- BUILT-IN DEGAUSS SYSTEM
- EXTENSIVE FAULT DETECTION
- EXTERNAL HIGH-POWER DRIVER OPTION

APPLICATIONS

- GENERATOR/ALTERNATOR MONITORING AND CONTROL
- FREQUENCY AND VOLTAGE INVERTERS
- MOTOR DRIVE CONTROLLERS
- SYSTEM POWER CONSUMPTION
- PHOTOVOLTAIC SYSTEMS

DESCRIPTION

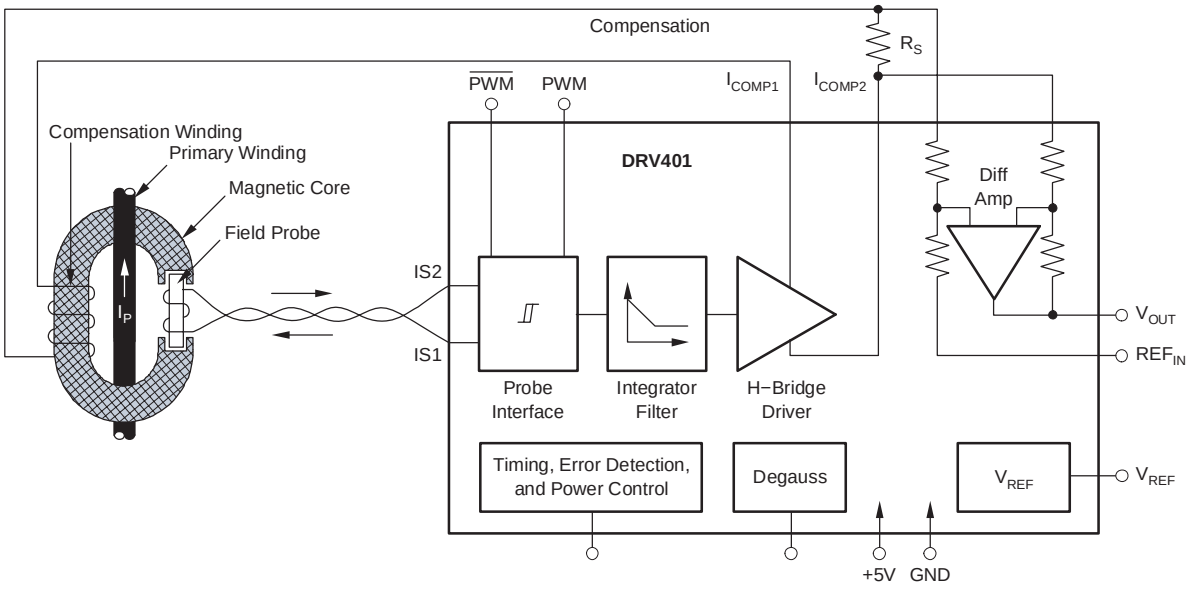
The DRV401 is designed to control and process signals from specific magnetic current sensors made by Vacuumschmelze GmbH & Co. KG (VAC). A variety of current ranges and mechanical configurations are available. Combined with a VAC sensor, the DRV401 monitors both ac and dc currents to high accuracy.

Provided functions include: probe excitation, signal conditioning of the probe signal, signal loop amplifier, an H-bridge driver for the compensation coil, and an analog signal output stage that provides an output voltage proportional to the primary current. It offers overload and fault detection, as well as transient noise suppression.

The DRV401 can directly drive the compensation coil, or connect to external power drivers. Therefore, the DRV401 combines with sensors to measure small to very large currents.

To maintain the highest accuracy, the DRV401 can demagnetize (degauss) the sensor at power-up and on demand.

Patents Pending.



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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7V
Signal Input Terminals:	
Voltage(2)	−0.5V to V_{DD} + 0.5V
Differential Amplifier(3)	−10V to +10V
Current at IS1 and IS2	±75mA
Current (pins other than IS1 and IS2)(2)	±25mA
I_{COMP} Short Circuit(4)	+250mA
Operating Junction Temperature	−50°C to +150°C
Storage Temperature	−55°C to +150°C
ESD Rating:	
Human Body Model (HBM)	
Pins IA_{IN1} and IA_{IN2} Only	1kV
All Other Pins	4kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited, except for the differential amplifier input pins.

(3) These inputs are not internally protected against over voltage. The differential amplifier input pins must be limited to 5mA, max or ±10V, max.

(4) Power-limited; observe maximum junction temperature.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
DRV401	QFN-20 (5mm x 5mm)	RGW	HAAQ
DRV401	SO-20	DWP	DRV401A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range: **T_J = −40°C to +125°C.**

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, and zero output current I_{COMP}, unless otherwise noted.

PARAMETER		CONDITIONS	DRV401 MIN	DRV401 TYP	DRV401 MAX	UNITS
DIFFERENTIAL AMPLIFIER		R_L = 10kΩ to 2.5V, V_{REFIN} = 2.5V				
OFFSET VOLTAGE						
Offset Voltage, RTO(1)(2)	V_{OS}	Gain 4V/V		±0.01	±0.1	mV
Drift, RTO(2)	**dV_{OS}/dT**			**±0.1**	**±1(3)**	**µV/°C**
vs Common-Mode, RTO	CMRR	−1V to +6V, V_{REF} = 2.5V		±50	±250	µV/V
vs Power-Supply, RTO	PSRR	V_{REF} not included		±4	±50	µV/V
SIGNAL INPUT						
Common-Mode Voltage Range			−1		(V_{DD}) + 1	V
SIGNAL OUTPUT						
Signal Over-Range Indication (OVER-RANGE), Delay(2)		**V_{IN} = 1V Step, See Notes 2 and 3**		**2.5 to 3.5**		**µs**
Voltage Output Swing From Negative Rail(2), OVER-RANGE Trip Level		I = +2.5mA, CMP Trip Level		+48	+85	mV
Voltage Output Swing From Positive Rail(2), OVER-RANGE Trip Level		I = −2.5mA, CMP Trip Level	V_{DD} − 85	V_{DD} − 48		mV
Short-Circuit Current(2)	I_{SC}	V_{OUT} Connected To GND		−18		mA
		V_{OUT} Connected To V_{DD}		+20		mA
Gain, V_{OUT}/V_{IN_DIFF}				**4**		**V/V**
Gain Error				±0.02	±0.3	%
Gain Error Drift				**±0.1**		**ppm/°C**
Linearity Error		R_L = 1kΩ		10		ppm
FREQUENCY RESPONSE						
Bandwidth(2)	BW_{-3dB}			2		MHz
Slew Rate(2)	SR	CMVR = −1V to = +4V		6.5		V/µs
Settling Time, Large-Signal(2)		dV ± 2V to 1%, No External Filter		0.9		µs
Settling Time(2)		dV ± 0.4V to 0.01%		14		µs
INPUT RESISTANCE						
Differential			16.5	20	23.5	kΩ
Common-Mode			41	50	59	kΩ
External Reference Input			41	50	59	kΩ
NOISE						
Output Voltage Noise Density, f = 1kHz, RTO(2)	e_n	Compensation Loop Disabled		170		$nV/\sqrt{Hz}$

COMPENSATION LOOP						
DC STABILITY		Probe f = 250kHz, R_{LOAD} = 20Ω				
Offset Error(4)		Deviation from 50% PWM, Pin Gain = L		0.03		%
Offset Error Drift(2)		**Deviation from 50% PWM, Pin Gain = L**		**7.5**		**ppm/°C**
Gain, Pin Gain = L(2)		$\lvert V_{ICOMP1}\rvert - \lvert V_{ICOMP2}\rvert$	−200	25	200	ppm/V
Power-Supply Rejection Ratio	PSRR	Probe Loop f = 250kHz		500		ppm/V
FREQUENCY RESPONSE						
Open-Loop Gain, Two Modes, 7.8kHz		Pin Gain H/L		24/32		dB
PROBE COIL LOOP						
Input Voltage Clamp Range		Field Probe Current < 50mA		−0.7 to V_{DD} + 0.7		V
Internal Resistor, IS1 or IS2 to V_{DD1}(2)	R_{HIGH}		47	59	71	Ω
Internal Resistor, IS1 or IS2 to GND1(2)	R_{LOW}		60	75	90	Ω
Resistance Mismatch Between IS1 and IS2(2)		ppm of R_{HIGH} + R_{LOW}		300	1500	ppm
Total Input Resistance(3)				**134**	**200**	Ω
Comparator Threshold Current(3)			22	28	34	mA
Minimum Probe Loop Half-Cycle(2)			250	280	310	ns
Probe Loop Minimum Frequency			250			kHz
No Oscillation Detect (Error) Suppression				35		µs
COMPENSATION COIL DRIVER, H-BRIDGE						
Peak Current(2)		**V_{ICOMP1} − V_{ICOMP2} = 4.0V_{PP}**		**250**		**mA**
Voltage Swing		20Ω Load	4.2			V_{PP}
Output Common-Mode Voltage				V_{DD2}/2		V
Wire Break Detect, Threshold Current(5)		I_{COMP1} and I_{COMP2} Railed		33	57	mA

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_J = −40°C to +125°C, with zero output current I_{COMP}.**

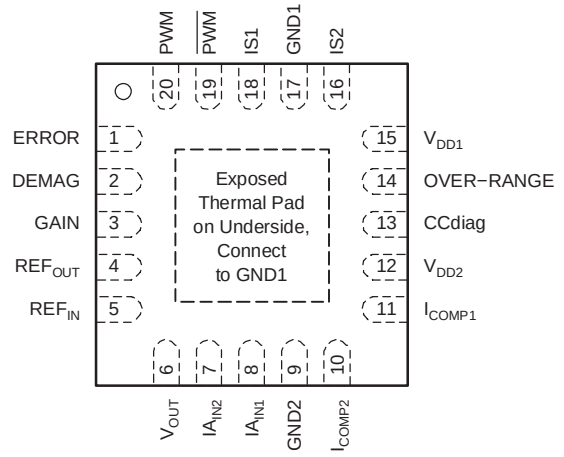
At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

PARAMETER		CONDITIONS	DRV401 MIN	DRV401 TYP	DRV401 MAX	UNITS
VOLTAGE REFERENCE						
Voltage(2)		No Load	2.495	2.5	2.505	V
Drift(2)		**No Load**		**±5**	**±50**	**ppm/°C**
PSRR(2)				±15	±200	µV/V
Load Regulation(2)		Load to GND/V_{DD}, dI = 0mA to 5mA		0.15		mV/mA
Short-Circuit Current	I_{SC}	REF_{OUT} Connected to V_{DD}		+20		mA
		REF_{OUT} Connected to GND		−18		mA
DEMAGNETIZATION						
Duration		See Timing Diagram		**106**	**130(3)**	**ms**
DIGITAL I/O						
LOGIC INPUTS (DEMAG, GAIN, and CCdiag Pins)		**CMOS Type Levels**				
Pull-Up High Current (CCdiag)		3.5 < V_{IN} < V_{DD}		160		µA
Pull-Up Low Current (CCdiag)		0 < V_{IN} < 1.5		5		µA
Logic Input Leakage Current		0 < V_{IN} < V_{DD}		0.01	5	µA
Logic Level, Input: L/H				2.1/2.8		V
Hysteresis				0.7		V
OUTPUTS (ERROR AND OVER-RANGE Pins)						
Logic Level, Output: L		4mA Sink		0.3		V
Logic Level, Output: H				No Internal Pull-Up		
OUTPUTS (PWM and $\overline{PWM}$ Pins)		Push-Pull Type				
Logic Level L		4mA Sink		0.2		V
Logic Level H		4mA Source		(V_{DD}) − 0.4		V
POWER SUPPLY						
Specified Voltage Range	**V_{DD}**		**4.5**	**5**	**5.5**	**V**
Power-On Reset Threshold	V_{RST}			1.8		V
Quiescent Current [I(V_{DD1}) + I(V_{DD2})]	I_Q	I_{COMP} = 0mA, Sensor Not Connected			6.8	mA
Brownout Voltage Level(2)				4		V
Brownout Indication Delay				135		µs
TEMPERATURE RANGE						
Specified Range	T_J		−40		+125	°C
Operating Range	T_J		−50		+150	°C
Package Thermal Resistance						
QFN Surface-Mount	θ_{JA}	See Note 6		40		°C/W
SO PowerPAD Surface-Mount	θ_{JA}	See Note 6		27		°C/W

(1) Parameter value referred to output (RTO).
(2) See Typical Characteristic curves.
(3) Total input resistance and comparator threshold current are inversely related. See Figure 2a.
(4) For VAC sensors, 0.2% of PWM offset approximately corresponds to 10mA primary current offset per winding.
(5) See *Compensation Driver* section in Applications Information.
(6) See *Applications Information* section for information on power dissipation, layout considerations, and proper PCB soldering and heat-sinking technique.

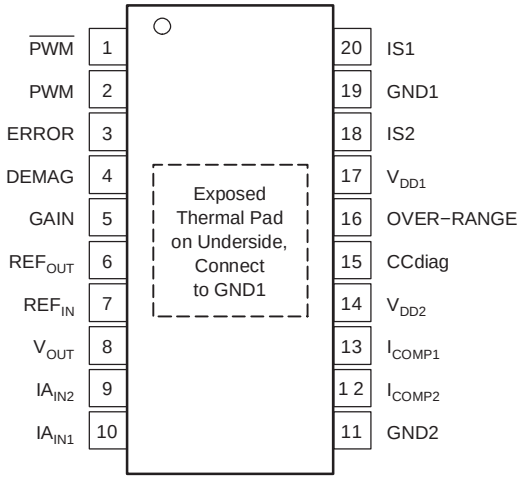
PIN CONFIGURATIONS

Top View **RGW**



QFN−20 (5mm x 5mm)

Top View **DWP**



Wide−Body SO−20

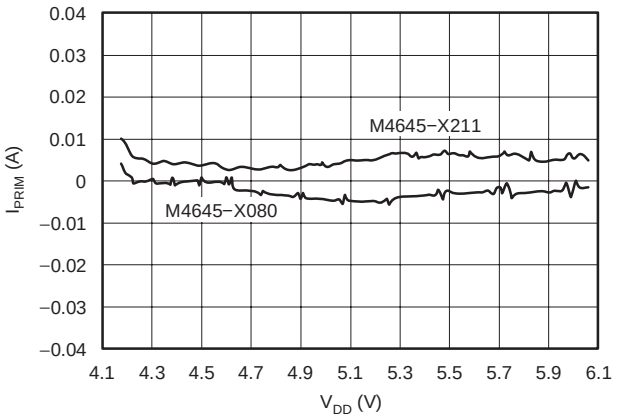
PIN ASSIGNMENTS

NAME	RGW	DWP	DESCRIPTION
ERROR	1	3	Error flag: open-drain output, see the *Error Conditions* section.
DEMAG	2	4	Control input, see the *Demagnetization* section.
GAIN	3	5	Control input for open-loop gain: low = normal, high = −8dB.
REF_{OUT}	4	6	Output for internal 2.5V reference voltage.
REF_{IN}	5	7	Input for zero reference to differential amplifier.
V_{OUT}	6	8	Output for differential amplifier.
IA_{IN2}	7	9	Noninverting input of differential amplifier.
IA_{IN1}	8	10	Inverting input of differential amplifier.
GND2	9	11	Ground connection. Connect to GND1.
I_{COMP2}	10	12	Output 2 of compensation coil driver.
I_{COMP1}	11	13	Output 1 of compensation coil driver.
V_{DD2}	12	14	Supply voltage. Connect to V_{DD1}.
CCdiag	13	15	Control input for wire-break detection: high = enable.
OVER−RANGE	14	16	Open-drain output for over-range indication: low = over-range.
V_{DD1}	15	17	Supply voltage.
IS2	16	18	Probe connection 2.
GND1	17	19	Ground connection.
IS1	18	20	Probe connection 1.
$\overline{PWM}$	19	1	PWM output from probe circuit (inverted).
PWM	20	2	PWM output from probe circuit.
Exposed Thermal Pad	—	—	Connect to GND1.

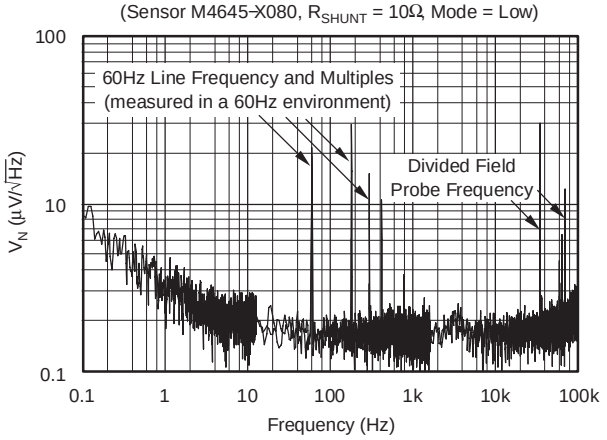
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

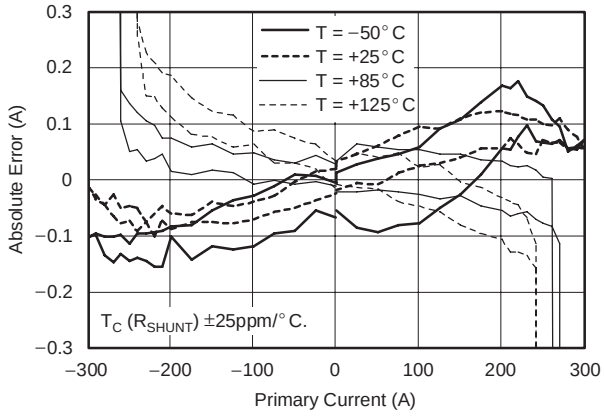
DRV401 AND SENSOR:
OFFSET vs SUPPLY VOLTAGE



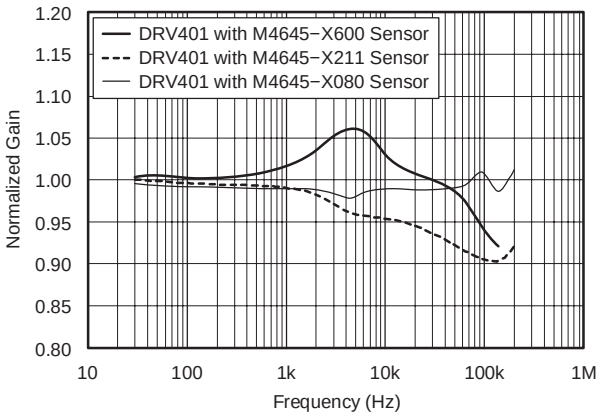
DRV401 AND SENSOR:
OUTPUT VOLTAGE NOISE DENSITY
(Sensor M4645−X080, R_{SHUNT} = 10Ω, Mode = Low)



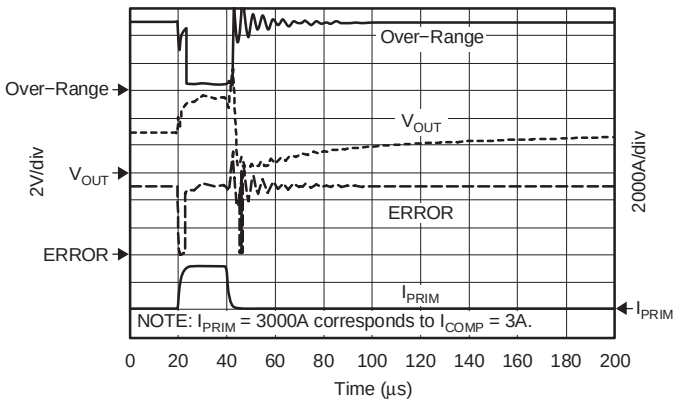
DRV401 AND SENSOR: ABSOLUTE ERROR
(Soldered DWP−20 with 1 Square−Inch Copper Pad)
(Measurements by Vacuumschmelza GmbH)



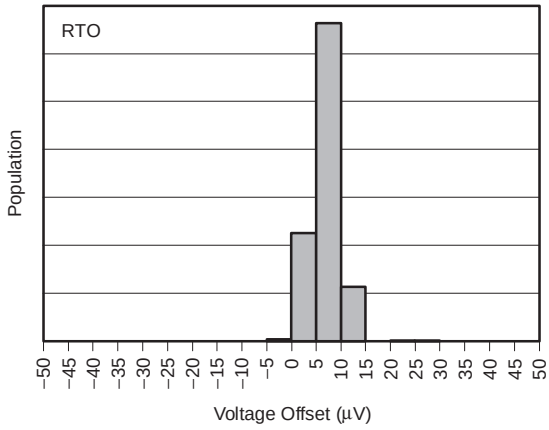
GAIN FLATNESS vs FREQUENCY
(Measurements by Vacuumschmelze GmbH)



3A I_{COMP} OVERLOAD RECOVERY
(Measurements by Vacuumschmelze GmbH)



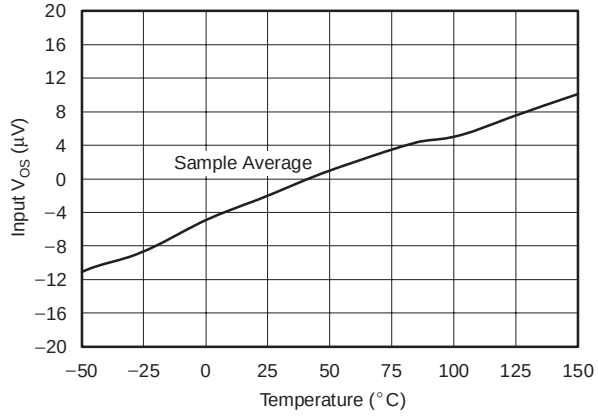
DIFFERENTIAL AMPLIFIER:
VOLTAGE OFFSET PRODUCTION DISTRIBUTION



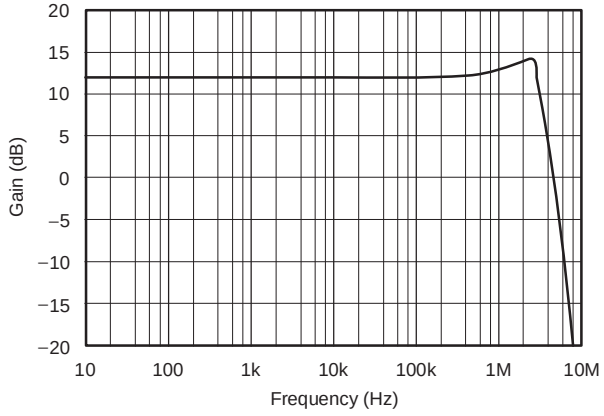
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

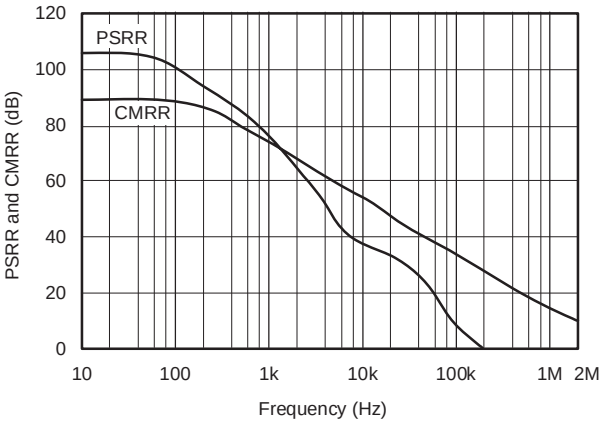
DIFFERENTIAL AMPLIFIER:
OFFSET VOLTAGE vs TEMPERATURE, RTO



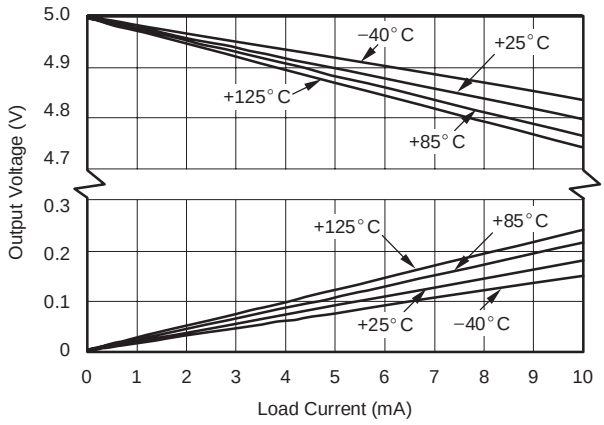
DIFFERENTIAL AMPLIFIER:
GAIN vs FREQUENCY



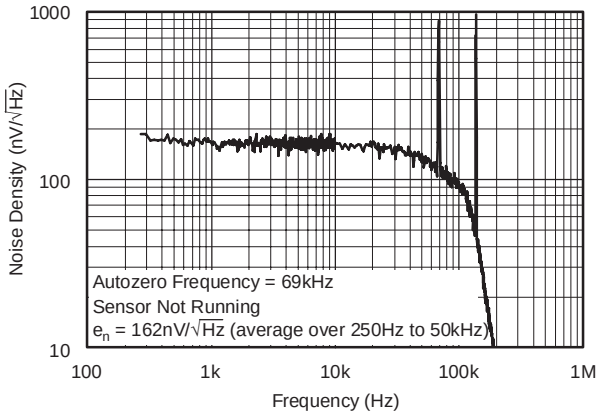
DIFFERENTIAL AMPLIFIER:
PSRR AND CMRR vs FREQUENCY



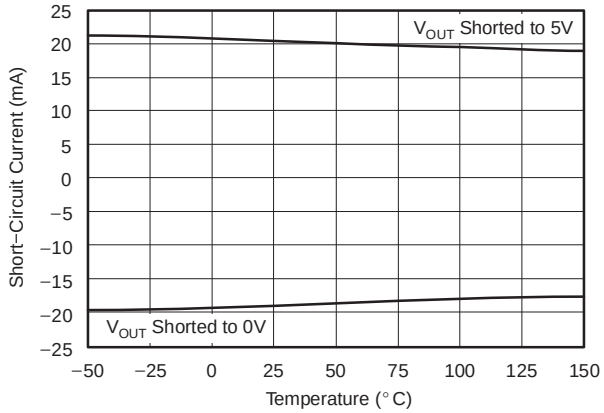
DIFFERENTIAL AMPLIFIER:
OUTPUT VOLTAGE vs OUTPUT CURRENT



DIFFERENTIAL AMPLIFIER:
OUTPUT NOISE DENSITY



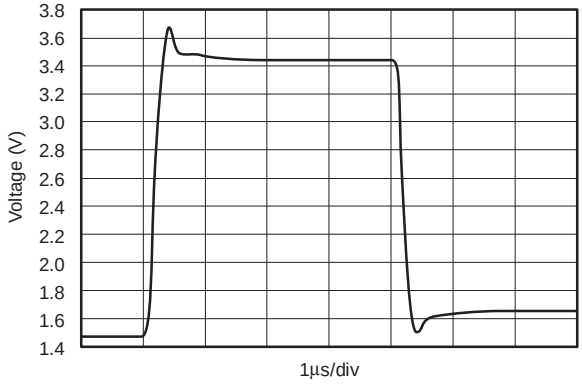
DIFFERENTIAL AMPLIFIER:
SHORT−CIRCUIT CURRENT vs TEMPERATURE



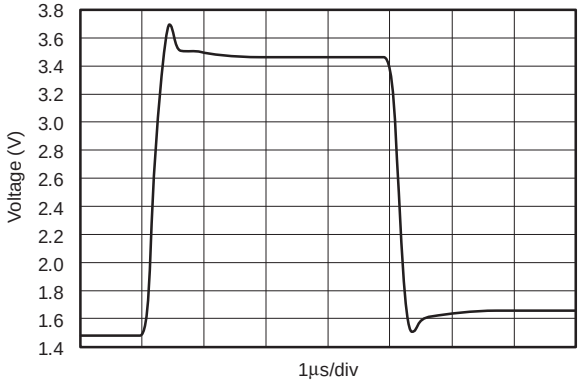
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

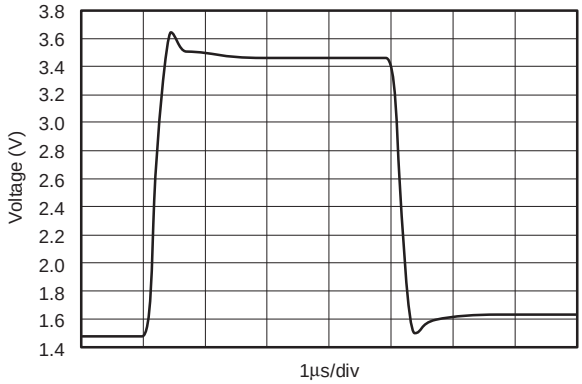
DIFFERENTIAL AMPLIFIER:
T_A = −50°C LARGE−SIGNAL STEP RESPONSE



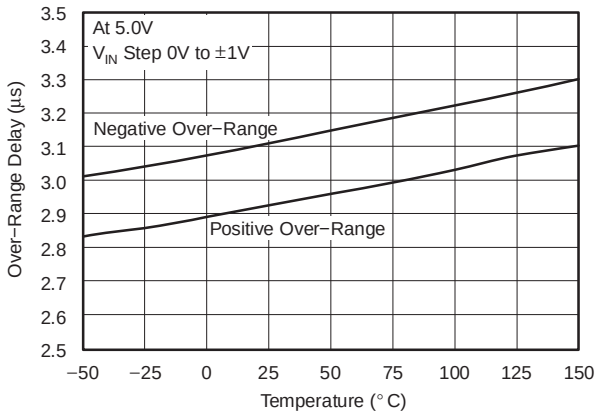
DIFFERENTIAL AMPLIFIER:
T_A = +25°C LARGE−SIGNAL STEP RESPONSE



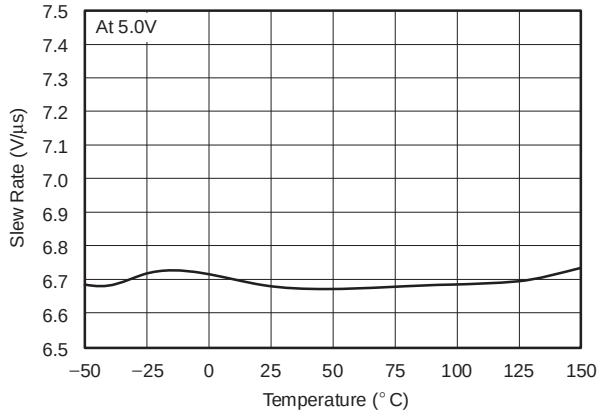
DIFFERENTIAL AMPLIFIER:
T_A = +150°C LARGE−SIGNAL STEP RESPONSE



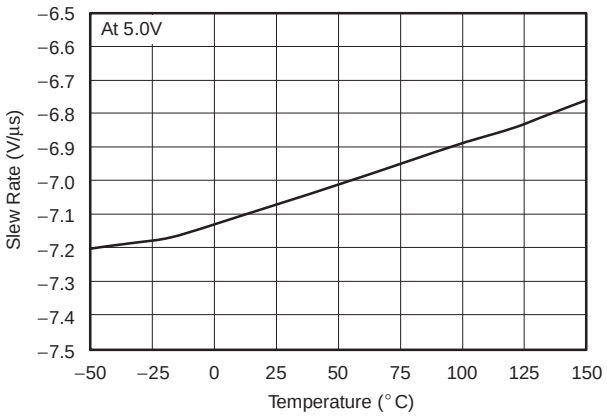
DIFFERENTIAL AMPLIFIER:
OVER−RANGE DELAY vs TEMPERATURE



DIFFERENTIAL AMPLIFIER:
POSITIVE SLEW RATE vs TEMPERATURE



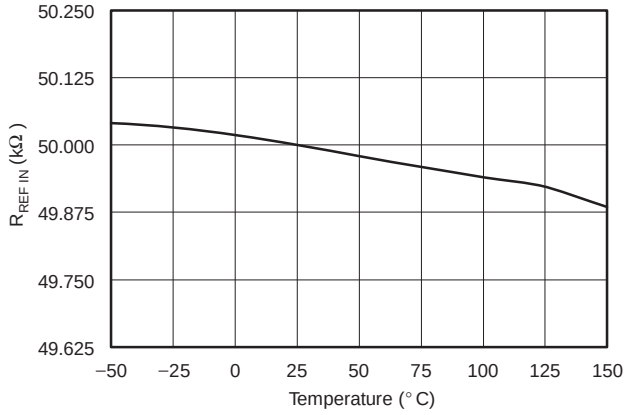
DIFFERENTIAL AMPLIFIER:
NEGATIVE SLEW RATE vs TEMPERATURE



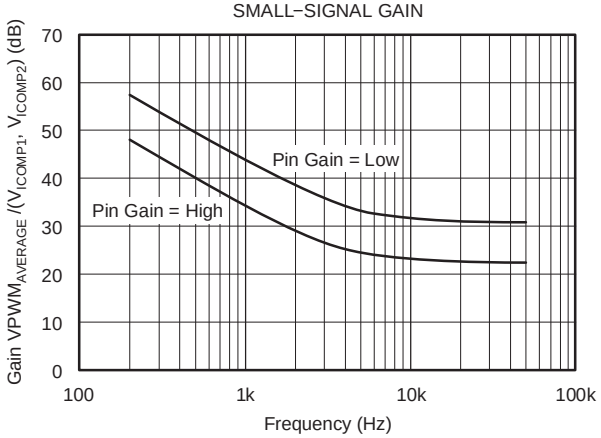
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

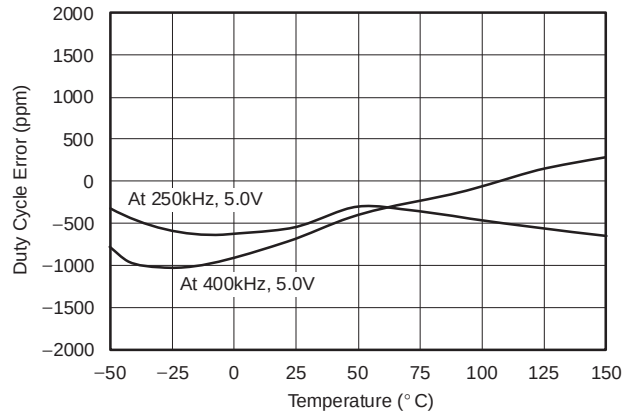
DIFFERENTIAL AMPLIFIER:
REF_{IN} RESISTANCE vs TEMPERATURE



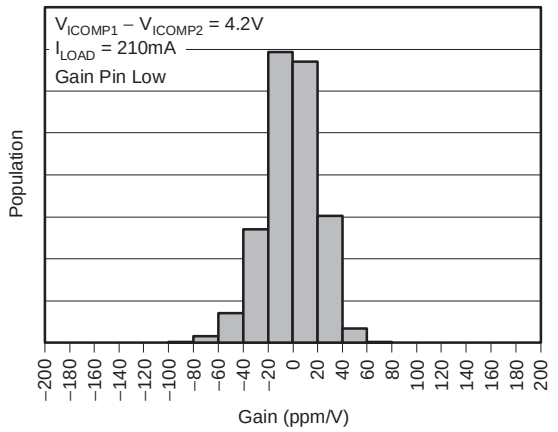
COMPENSATION LOOP:
SMALL−SIGNAL GAIN



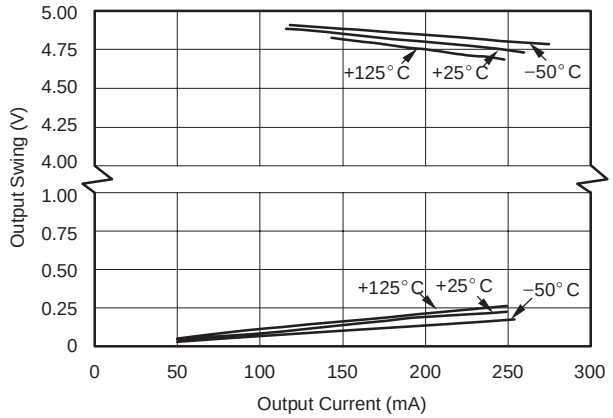
COMPENSATION LOOP:
DUTY CYCLE ERROR vs TEMPERATURE



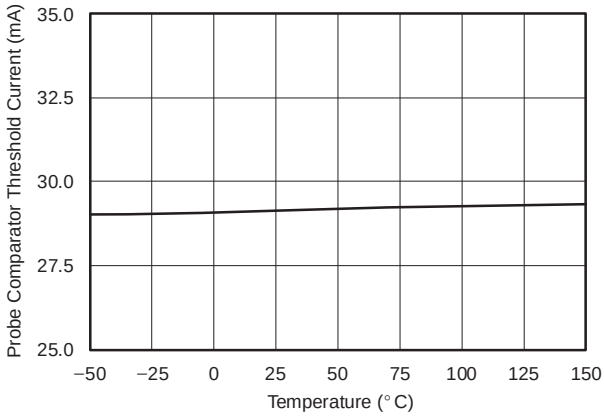
COMPENSATION LOOP:
DC GAIN: DUTY CYCLE ERROR CHANGE



I_{COMP} OUTPUT SWING TO RAIL
vs OUTPUT CURRENT



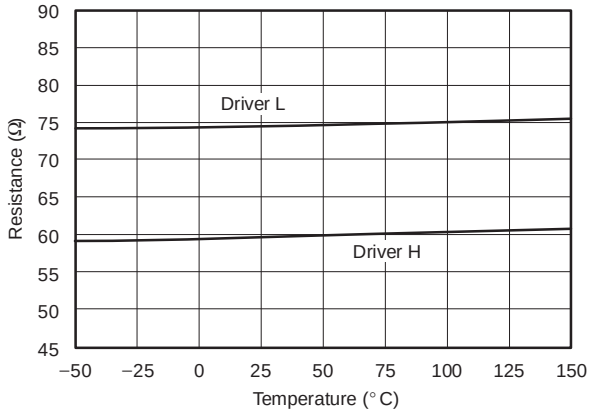
PROBE COMPARATOR THRESHOLD
CURRENT vs TEMPERATURE



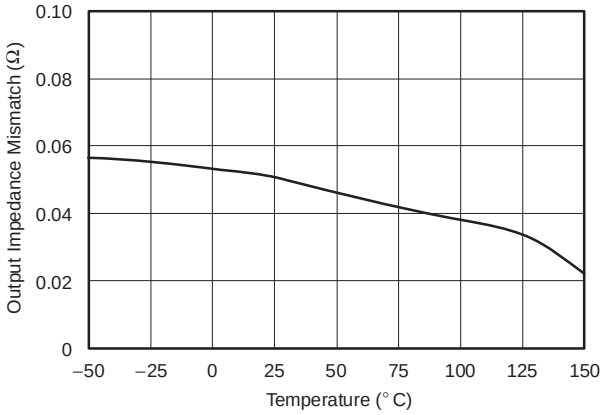
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

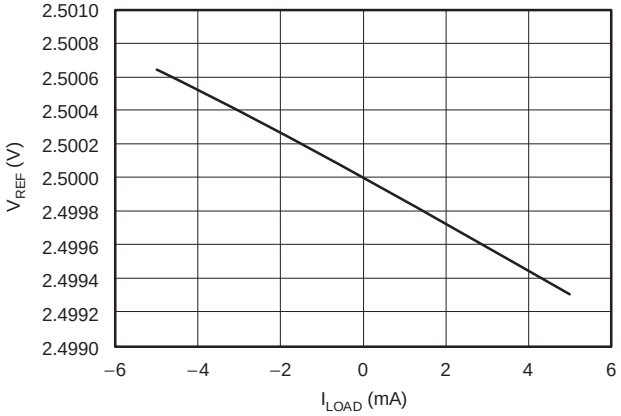
PROBE DRIVER:
INTERNAL RESISTOR vs TEMPERATURE



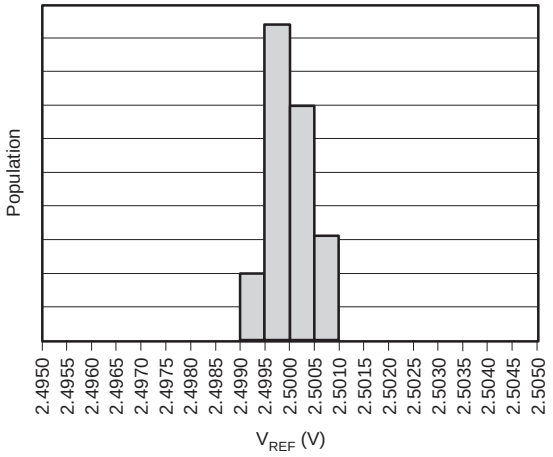
OUTPUT IMPEDANCE MISMATCH OF IS1 AND IS2
vs TEMPERATURE



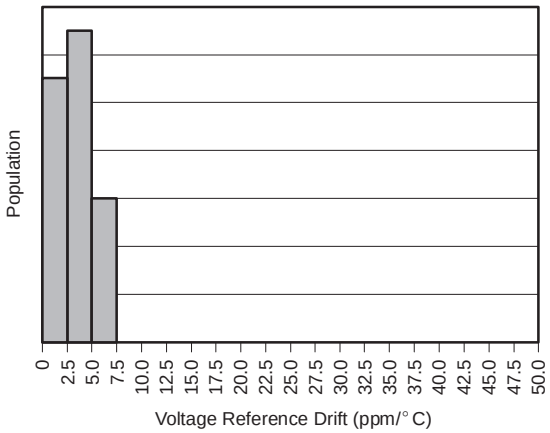
VOLTAGE REFERENCE vs LOAD CURRENT



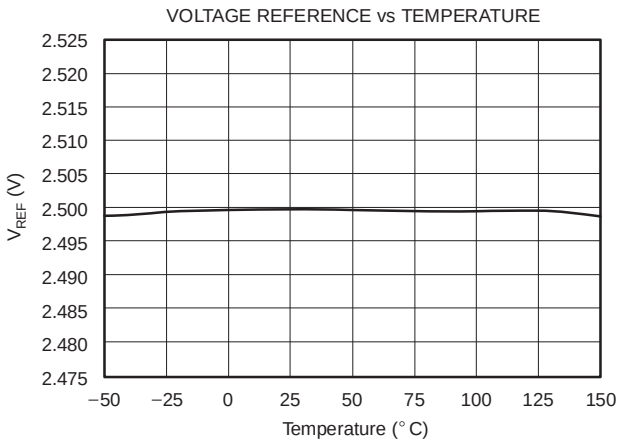
VOLTAGE REFERENCE PRODUCTION DISTRIBUTION



VOLTAGE REFERENCE DRIFT
PRODUCTION DISTRIBUTION



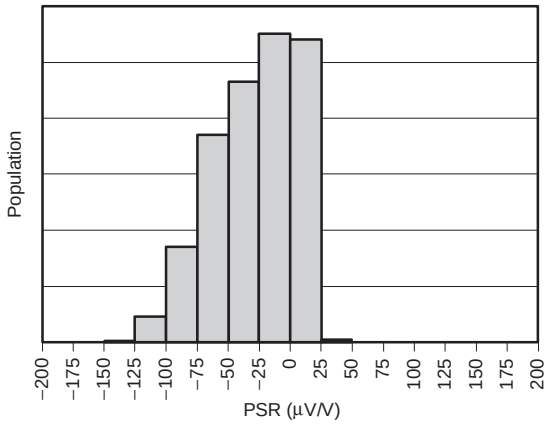
VOLTAGE REFERENCE vs TEMPERATURE



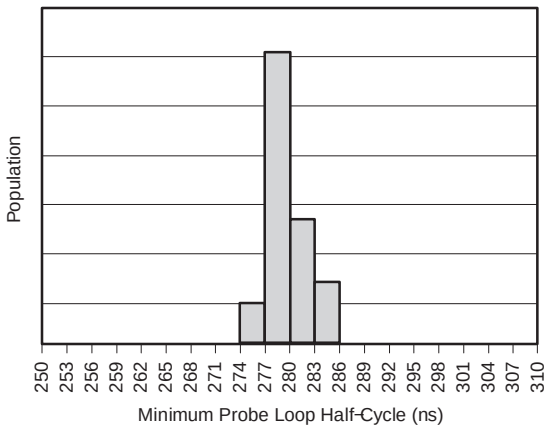
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and V_{DD1} = V_{DD2} = +5V with external 100kHz filter BW, unless otherwise noted.

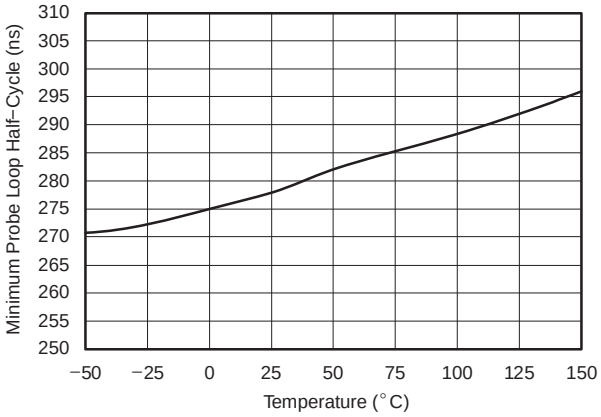
VOLTAGE REFERENCE POWER−SUPPLY REJECTION PRODUCTION DISTRIBUTION



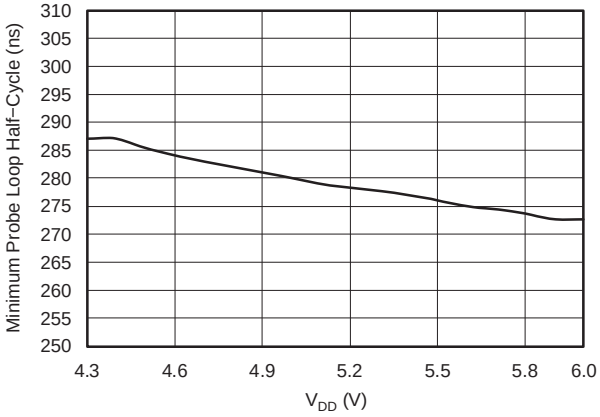
OSCILLATOR PRODUCTION DISTRIBUTION



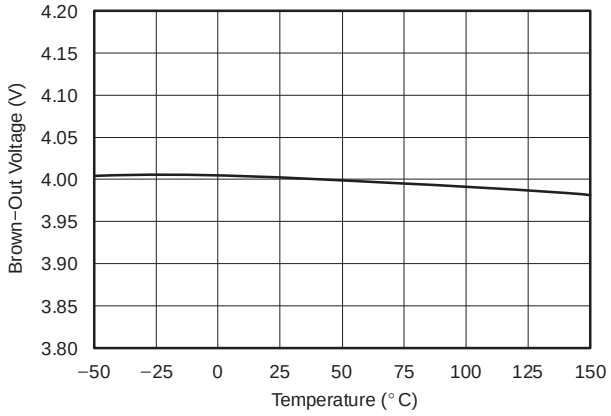
OSCILLATOR vs TEMPERATURE



OSCILLATOR vs SUPPLY VOLTAGE



BROWN−OUT VOLTAGE vs TEMPERATURE



APPLICATIONS INFORMATION

FUNCTIONAL PRINCIPLE OF CLOSED-LOOP CURRENT SENSORS WITH MAGNETIC PROBE USING THE DRV401

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method as well as excellent galvanic isolation performance combined with high resolution, accuracy, and reliability.

At dc and in low-frequency ranges, the magnetic field induced from the current in the primary winding is compensated by a current flowing through a compensation winding. A magnetic field probe, located in the magnetic core loop, detects the magnetic flux. This probe delivers the signal to the amplifier that drives the current through the compensation coil, bringing the magnetic flux back to zero. This compensation current is proportional to the primary current, relative to the winding ratio.

In higher frequency ranges, the compensation winding acts as the secondary winding in the current transformer, while the H-bridge compensation driver is rolled off and provides low output impedance.

A difference amplifier senses the voltage across a small shunt resistor that is connected to the compensation loop. This difference amplifier generates the output voltage that is referenced to REF_{IN} and is proportional to the primary current. Figure 1 shows the DRV401 used as a compensation current sensor.

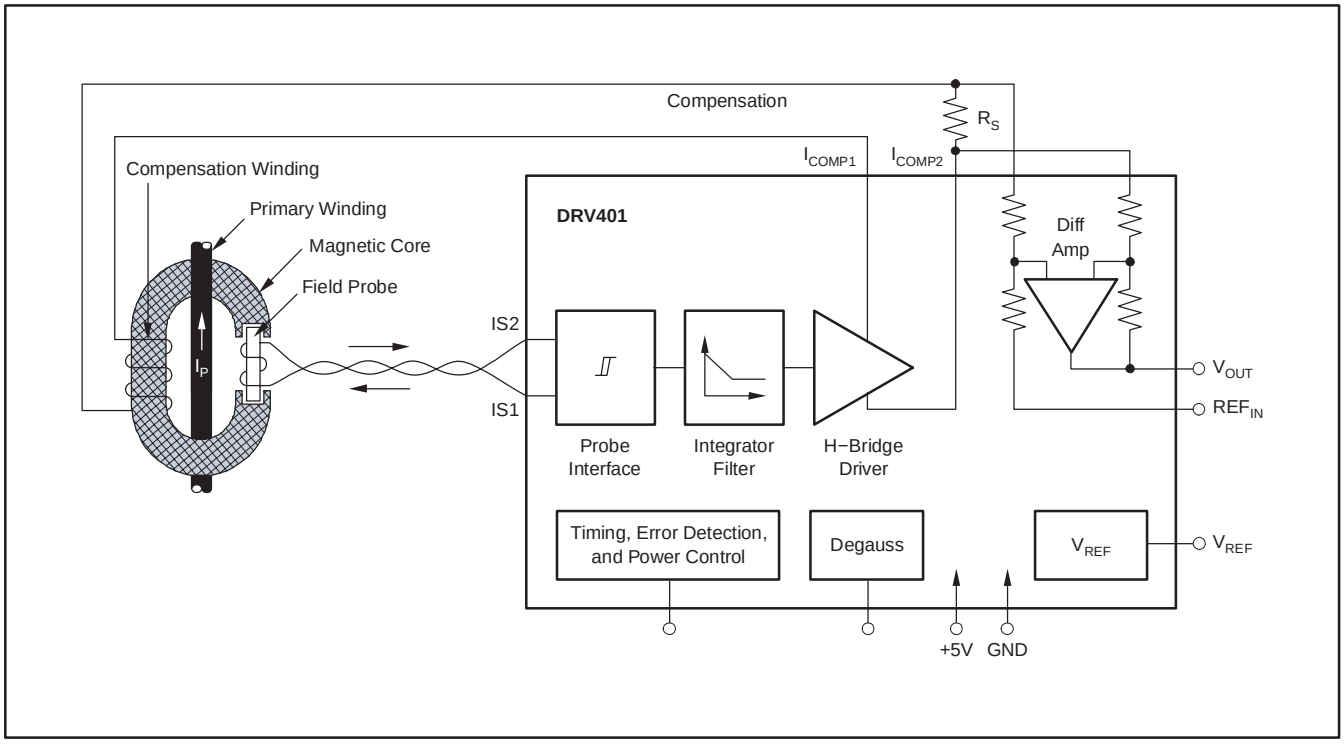


Figure 1. Principle of Compensation Current Sensor with the DRV401

FUNCTIONAL DESCRIPTION

The DRV401 operates from a single +5V supply. It is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation. The DRV401 provides magnetic field probe excitation, signal conditioning, and compensation coil driver amplification. In addition, it detects error conditions and handles overload situations. A precise differential amplifier allows translation of the compensation current into an output voltage using a small shunt resistor. A buffered voltage reference can be used for comparator, analog-to-digital converter (ADC), or bipolar zero reference voltages.

Dynamic error correction ensures high dc precision over temperature and long-term accuracy. The DRV401 uses analog signal conditioning; the internal loop filter and integrator are switched capacitor-based circuits. Therefore, the DRV401 allows combination with high-precision sensors for exceptional accuracy and resolution. The typical characteristic curve, *DRV401 and Sensor Linearity*, shows an example of the linearity and temperature stability achieved by the device.

A demagnetization cycle can be initiated on demand or on power-up. This cycle reduces offset and restores high performance after a strong overload condition. An internal clock and counter logic generate the degauss function. The same clock controls power-up, overload detection and recovery, error, and time-out conditions.

The DRV401 is built on a highly reliable CMOS process. Unique protection cells at critical connections enable the design to handle inductive energy.

MAGNETIC PROBE (SENSOR) INTERFACE

The magnetic field probe consists of an inductor wound on a soft magnetic core. The probe is connected between pins IS1 and IS2 of the probe driver that applies approximately +5V (the supply voltage) through resistors across the probe coil (see Figure 2a).

The probe core reaches saturation at a current of typically 28mA (see Figure 2a). The comparator is connected to V_{REF} by approximately 0.5V. A current comparator detects the saturation and inverts the excitation voltage polarity, causing the probe circuit to oscillate in a frequency range of 250kHz to 550kHz. The oscillating frequency is a function of the magnetic properties of the probe core and its coil.

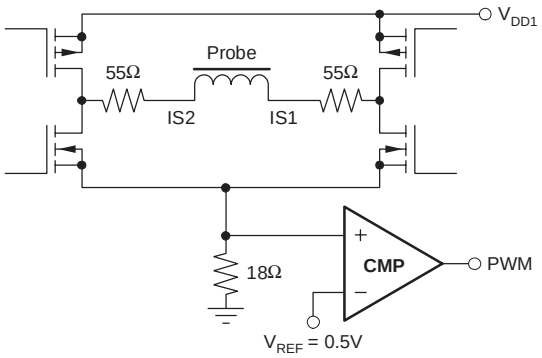
The current rise rate is a function of the coil inductance: $dI = L \times V \times dT$. However, the inductance of the field probe is low while its core material is in saturation (the horizontal part of the hysteresis curve) and is high at the vertical part of the hysteresis curve. The resulting inductance and the series resistance determine the output voltage and current versus time performance characteristic.

Without external magnetic influence, the duty cycle is exactly 50% because of the inherent symmetry of the magnetic hysteresis; the probe inductor is driven from −B saturation through the high inductance range to +B saturation and back again in a time-symmetric manner (see Figure 2b).

If the core material is magnetized in one direction, a long and a short charge time result because the probe current through the inductors generates a field that either subtracts or adds to the flux in the probe core, either driving the probe core out of saturation or further into saturation (see Figure 2c). The current into the probe is limited by the voltage drops across the probe driver resistors.

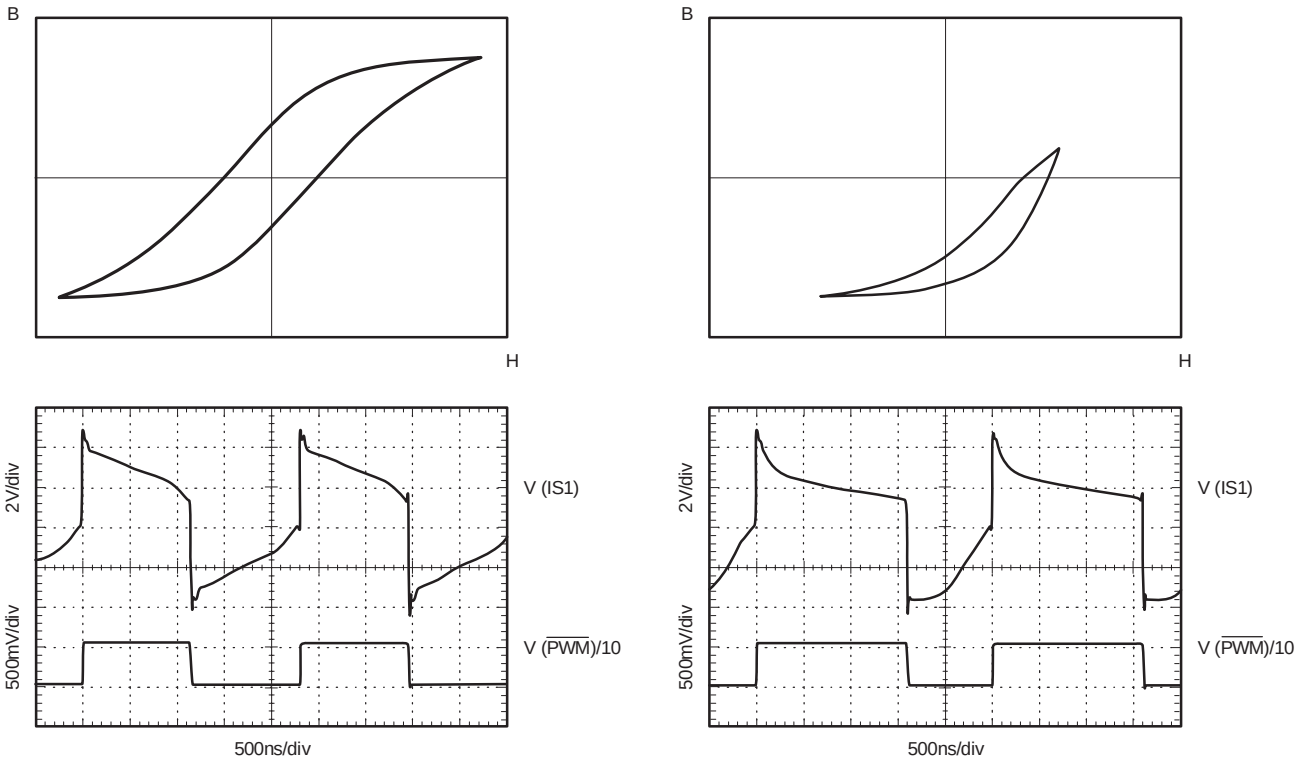
The DRV401 continuously monitors the logic magnetic flux polarity state. In the case of distortion noise and excessive overload that could fully saturate the probe, the overload control circuit recovers the probe loop. During an overload condition, the probe oscillation frequency increases to approximately 1.6MHz until limited by the internal timing control.

In an overload condition, the compensation current (I_{COMP}) driver cannot deliver enough current into the sensor secondary winding, and the magnetic flux in the sensor main core becomes uncompensated.



NOTE: MOS components function as switches only.

a) Simplified probe interface circuit.
The probe is connected between S1 and S2.



b) Without an external magnetic field, the hysteresis curve is symmetrical and the probe loop generates 50% duty cycle.

c) An external magnetic flux (H) generated from the primary current (I_{PRIM}) shifts the hysteresis curve of the magnetic field probe in the H-axis and the probe loop generates a nonsymmetrical duty cycle.

Figure 2. Magnetic Probe, Hysteresis, and Duty Cycle

The transition from normal operation to overload happens relatively slowly, because the inherent sensor transformer characteristics induce the initial primary current step, as shown in Figure 3. As the transformer-induced secondary current starts to decay, the compensation feedback driver increases its output voltage to maintain the sensor core flux compensation at zero.

When the system compensation loop reaches its driving limit, the rising magnetic flux causes one of the probe PWM half-periods to become shorter. The minimum half-period of the probe oscillation is limited by the internal timing to 280ns, based on the properties of the VAC magnetic sensors. After three consecutive cycles of the same half-period being shorter than 280ns, the DRV401 goes into overload-latch mode. The device stores the I_{COMP} driver output signal polarity and continues producing the skewed-duty cycle PWM signal. This action prevents the loss of compensation signal polarity information during very strong overloads. In this case, both PWM half-periods are short and approximately equal, because the field probe stays completely in one of the saturated regions.

The overload-latch condition is removed after the primary current goes low enough for the I_{COMP} driver to compensate, and both half-periods of the probe driver oscillation become longer than 280ns (the field probe comes out of the saturated region).

Peak voltages and currents can be generated during normal operations as well as overload conditions. Therefore, both probe connection pins are internally protected against coupled energy from the magnetic core. Wiring between probe and IC inputs should be short and guarded against interference; see *Layout Considerations*.

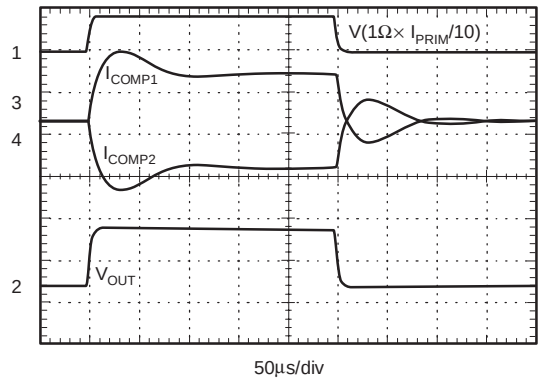
For reliable operation, error detection circuits monitor the probe operation:

1. If the probe driver comparator (CMP) output stays low longer than 32µs, the ERROR flag asserts active, and the compensation current (I_{COMP}) is set to zero.
2. If the probe driver period is less than 275ns on three consecutive pulses, the ERROR flag asserts active.

See the *Error Conditions* section for more details.

PWM PROCESSING

The outputs PWM and $\overline{PWM}$ represent the probe output signal as a differential PWM signal. It can drive external circuitry or be used for synchronous ripple reduction. The PWM signal from the probe excitation and sense stage is internally connected to a high-performance, switched-capacitor integrator followed by an integrating-differentiating filter. This filter converts the PWM signal into a filtered delta signal and prepares it for driving the analog compensation coil driver. The gain roll-off frequency of the filter stage is set to provide high dc gain and loop stability. If additional gain is added from external circuitry, the internal gain can be reduced by 8dB, asserting the GAIN pin high (see the *External Compensation Coil Driver* section).



A current pulse of 0A to 18A (Ch 1) generates the two I_{COMP} signals (Ch 3 and Ch 4). Ch 2 shows the resulting output signal, V_{OUT}. This test uses the M4645-X030 sensor, no bandwidth limitation, but a 20-sample average.

Figure 3. Primary Current Step Response

COMPENSATION DRIVER

The compensation coil driver provides the driving current for the compensation coil. A fully differential driver stage offers high signal voltages to overcome the wire resistance of the coil with only +5V supply. The compensation coil is connected between I_{COMP1} and I_{COMP2}, both generating an analog voltage across the coil (see Figure 3) that turns into current from the wire resistance (and eventually from the inductance). The compensation current represents the primary current transformed by the turns ratio. A shunt resistor is connected in this loop and the high-precision difference amplifier translates the voltage from this shunt to an output voltage.

Both compensation driver outputs provide low impedance over a wide frequency range to insure smooth transitions between the closed-loop compensation frequency range and the high-frequency range, where the primary winding directly couples the primary current into the compensation coil at a rate set by the winding ratio.

The two compensation driver outputs are designed with protection circuitry to handle inductive energy. However, additional external protection diodes might be necessary for high current sensors.

For reliable operation, a wire break in the compensation circuit can be detected. If the feedback loop is broken, the integrating filter drives the outputs I_{COMP1} and I_{COMP2} to the opposite rails. With one of these pins coming within 300mV to ground, a comparator tests for a minimum current flowing between I_{COMP1} and I_{COMP2}. If this current stays below the threshold current level for at least 100µs, the ERROR pin is asserted active (low). The threshold current level for this test is less than 57mA at 25°C and 65mA at −40°C, if the I_{COMP} pins are fully railed (see the Typical Characteristics).

For sensors with high winding resistance (compensation coil resistance + R_{SHUNT}) or connected to an external compensation driver, this function should be disabled by pulling the CCdiag pin low.

$$R_{MAX} = \frac{V_{OUT}}{65mA} \quad (1)$$

Where:

V_{OUT} equals the peak voltage between I_{COMP1} and I_{COMP2} at a 65mA drive current.

R_{MAX} equals the sum of the coil and the shunt resistance.

EXTERNAL COMPENSATION COIL DRIVER

An external driver for the compensation coil can be connected to the I_{COMP1} and I_{COMP2} outputs. To prevent a wire break indication, CCdiag has to be asserted low.

An external driver can provide both a higher drive voltage and more drive current. It also moves the power dissipation to the external transistors, thereby allowing a higher winding resistance in the compensation coil and more current. Figure 4 shows a block diagram of an external compensation coil driver. To drive the buffer, either one or both I_{COMP} outputs can be used. Note, however, that the additional voltage gain could cause instability of the loop. Therefore, the internal gain can be reduced by approximately 8dB by asserting the GAIN pin high. R_{SHUNT} is connected to GND to allow for a single-ended external compensation driver. The differential amplifier can continue to sense the voltage, and used for the gain and over-range comparator or ERROR flag.

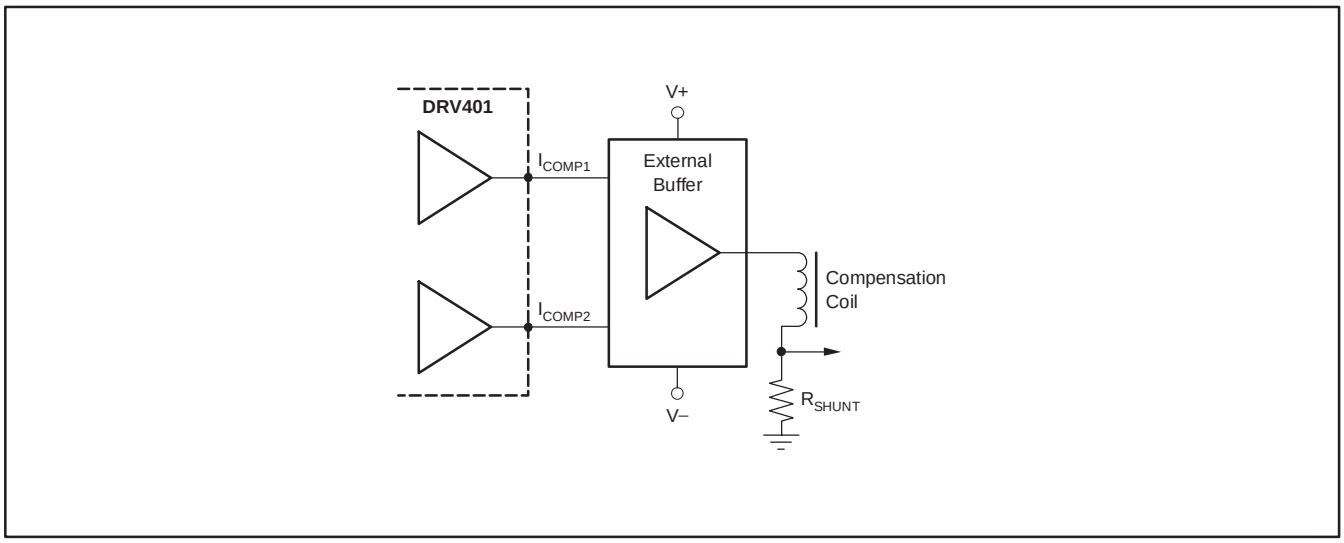


Figure 4. DRV401 with External Compensation Coil Driver and R_{SHUNT} Connected to GND

SHUNT SENSE AMPLIFIER

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4V/V, set by precisely matched and stable internal SiCr resistors.

Both inputs of the differential amplifier are normally connected to the current shunt resistor. This resistor adds to the internal (10kΩ) resistor, slightly reducing the gain in this leg. For best common-mode rejection (CMR), a dummy shunt resistor (R_5) is placed in series with the REF_{IN} pin to restore matching of both resistor dividers, as shown in Figure 5a.

For gains of 4V/V:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3} \qquad (2)$$

With $R_2/R_1 = R_4/R_3 = 4$; $R_5 = R_{SHUNT} \times 4$

Typically, the gain error resulting from the resistance of R_{SHUNT} is negligible; for 70dB of common-mode rejection, however, the match of both divider ratios needs to be better than 1/3000.

The amplifier output can drive close to the supply rails, and is designed to drive the input of a SAR-type ADC; adding an RC low-pass filter stage between the DRV401 and the ADC is recommended. This filter not only limits the signal bandwidth but also decouples the high-frequency component of the converter input sampling noise from the amplifier output. For R_F and C_F values, refer to the specific converter recommendations in the specific product data sheet. Empirical evaluation may be necessary to obtain optimum results.

The output can drive 100pF directly and shows 50% overshoot with approximately 1nF capacitance. Adding R_F allows much larger capacitive loads, as shown in Figure 5b and Figure 5c. Note that with R_F of only 20Ω, the load capacitor should be either smaller than 1nF or larger than 33nF to avoid overshoot; with R_F of 50Ω this transient area is avoided.

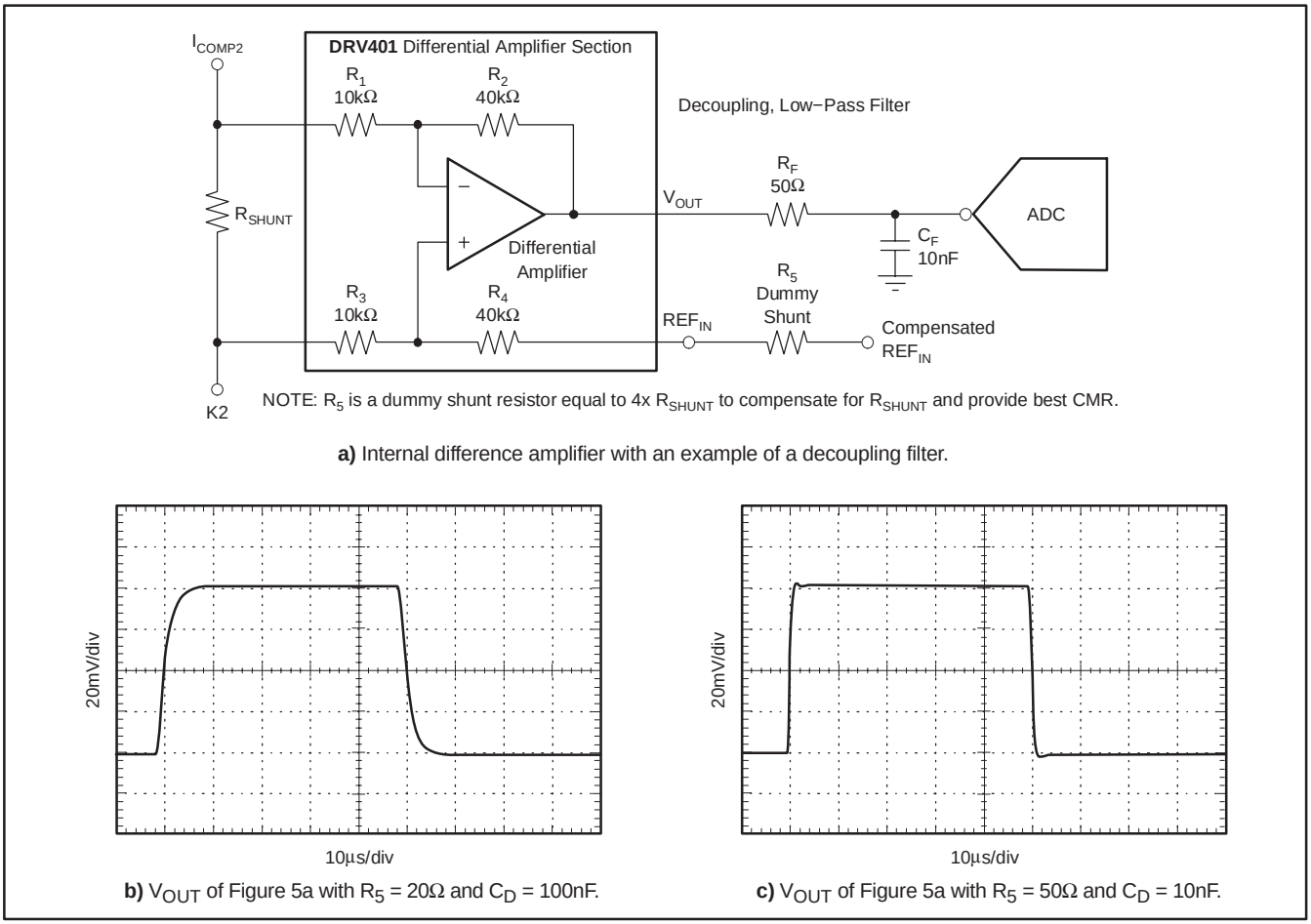


Figure 5. Internal Difference Amplifier with Example of a Decoupling Filter

The reference input (REF_{IN}) is the reference node for the exact output signal (V_{OUT}). Connecting REF_{IN} to the reference output (REF_{OUT}) results in a live zero reference voltage of 2.5V. Using the same reference for REF_{IN} and the ADC avoids mismatch errors that exist between two reference sources.

OVER-RANGE COMPARATOR

High peak current can overload the differential amplifier connected to the shunt. The OVER-RANGE pin, an open-drain output, indicates an over-voltage condition for the differential amplifier by pulling low. The output of this flag is suppressed for 3µs, preventing unwanted triggering from transients and noise. This pin returns to high as soon as the overload condition is removed (external pull-up required to return the pin high).

This ERROR flag not only provides a warning about a signal clipping condition, but is also a window comparator output for actively shutting off circuits in the system. The value of the shunt resistor defines the operating window for the current. It sets the ratio between the nominal signal and the trip level of the Over-Range flag. The trip current of this window comparator is calculated using the following example:

With a 5V supply, the output voltage swing is approximately ±2.45V (load and supply voltage-dependent).

The gain of 4V/V allows an input swing of ±0.6125V.

Thus, the clipping current is $I_{MAX} = 0.6125V/R_{SHUNT}$.

See the differential amplifier curve of the Typical Characteristics, *Output Voltage vs Output Current*.

The over-range condition is internally detected as soon as the amplifier exceeds its linear operating range, not just a set voltage level. Therefore, the error or the over-range comparator level is reliably indicated in fault conditions such as output shorts, low load or low supply conditions. As soon as the output cannot drive the voltage higher, the flag is activated. This configuration is a safety improvement over a voltage level comparator.

NOTE: The internal resistance of the compensation coil may prevent high compensation current from flowing because of I_{COMP} driver overload. Therefore, the differential amplifier may not overload with this current. However, a fast rate of change of the primary current would be transmitted through transformer action and safely trigger the overload flag.

VOLTAGE REFERENCE

The precision 2.5V reference circuit offers low drift (typically 10ppm/K) and is used for internal biasing; it is also connected to the REF_{OUT} pin. The circuit is intended as the reference point of the output signal to allow a bipolar signal around it. This output is buffered for low impedance and tolerates sink and source currents of ±5mA. Capacitive loads can be directly connected, but generate ringing on fast load transients. A small series resistor of a few ohms improves the response, especially for a capacitive load in the range of 1µF. Figure 6 shows the transient load regulation with 1nF direct load.

The reference source is part of the integrated circuit and referenced to GND2. Large current pulses driving the compensation coil can generate a voltage drop in the GND connection that would add on to the reference voltage. Therefore, a low impedance GND layout is critical to handle the currents and the high bandwidth of this IC.

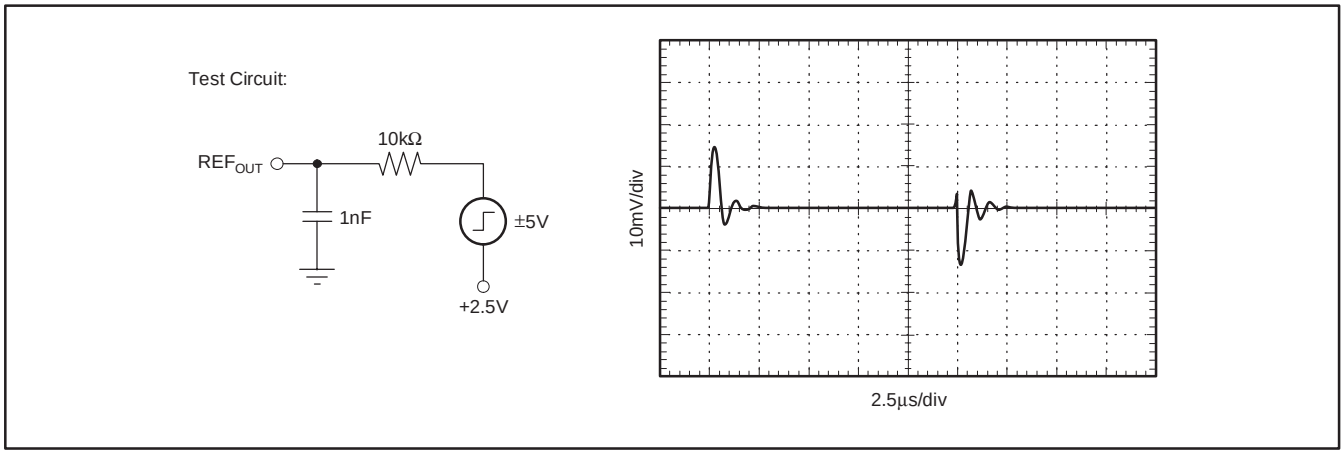


Figure 6. Pulse Response Test Circuit and Scope Shot of Reference

DEMAGNETIZATION

Iron cores are not immune to residual (remanence) magnetism. The residual remanence can produce a signal offset error, especially after strong current overload, which goes along with high magnetic field density. Therefore, the DRV401 includes a signal generator for a demagnetization cycle. The digital control pin, DEMAG, starts this cycle on demand after this pin is held high for at least 25.6µs. Shorter pulses are ignored. The cycle lasts for approximately 110ms. During this time, the Error flag is asserted low to indicate that the output is not valid. When DEMAG is high during power-on, a demagnetization cycle immediately initiates (12µs) after power-on (V_{DD} > 4V). Holding DEMAG low avoids this cycle at power-up (see the *Power-On and Brownout* section).

The probe circuit is in normal operation and oscillates during the demagnetization cycle. The outputs $\overline{PWM}$ and PWM are active accordingly.

A demagnetization cycle can be aborted by pulling DEMAG low, filtered by 25µs to ignore glitches (see Figure 7). In a typical circuit, the DEMAG pin may be connected to the positive supply, which enables a degauss cycle every time the unit is powered on.

The degauss cycle is based on an internal clock and counter logic. The maximum current is limited by the resistance of the connected coil in series with the shunt resistor. The DEMAG logic input requires a +5V CMOS-compatible signal.

POWER-ON AND BROWNOUT

Power-on is detected with the supply voltage going higher than 4V at V_{DD1}. When DEMAG is high, a degauss cycle is started (see Figure 7a). During this time the ERROR flag remains low, indicating the not ready condition. Maintaining DEMAG low prevents this cycle, and the DRV401 starts operation approximately 32µs after power-up. If no probe error conditions are detected within four full cycles (that is, the probe half-periods are shorter than 32µs and longer than 280ns), the compensation driver starts and the ERROR pin indicates the ready condition by going high, typically about 42µs after power-up.

NOTE: an external pull-up resistor is required to pull the ERROR pin high.

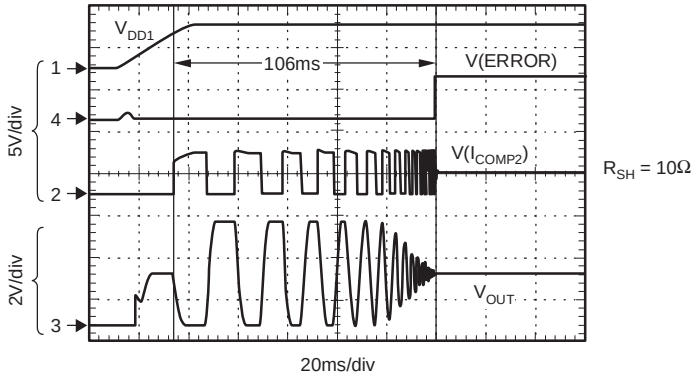
Both supply pins (V_{DD1} and V_{DD2}) should not differ by more than 100mV for proper device operation. They are normally connected together or separately filtered (see *Layout Considerations*).

The DRV401 tests for low supply voltage with a brown-out voltage level of +4V; proper power conditions must be supplied. Good power-supply and low ESR bypass capacitors are required to maintain the supply voltage during the large current pulses that the DRV401 can drive.

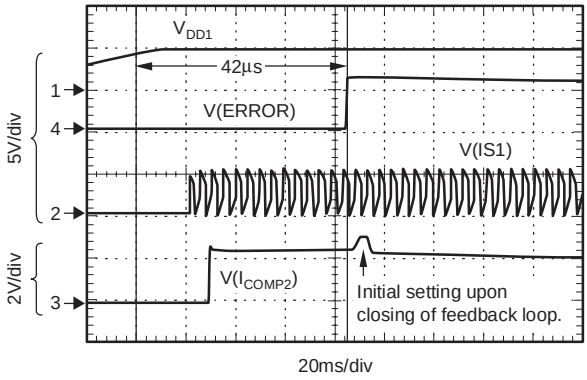
A critical voltage level is derived from the proper operation of the probe driver. The probe interface relies on a peak current flowing through the probe to trip the comparator. The probe resistance plus the internal resistance of the driver (see Electrical Characteristics specification, *Probe Coil Loop, Internal Resistor*) sets the lower limit for the acceptable supply voltage. Voltage drops lasting less than 31µs are ignored. The probe error detection activates the ERROR pin as soon as proper oscillation fails for more than 32µs.

A low supply voltage condition, or brown-out, is detected at +4V. Short and light voltage drops of less than 100µs are ignored, provided the probe circuit continues to operate. If the probe no longer operates, the ERROR pin goes active. Signal overload recovery is only provided if the probe loop was not discontinued.

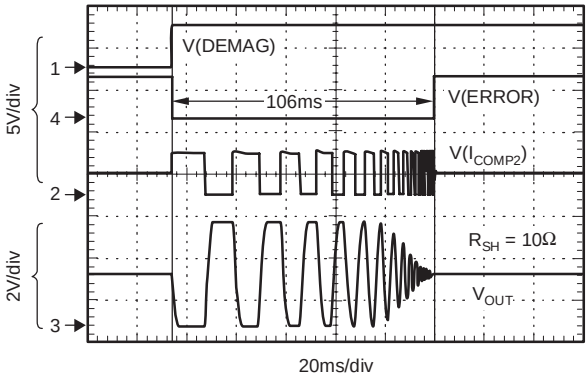
A supply drop lasting longer than 100µs generates power-on reset. A voltage dip down to +1.8V (for V_{DD1}) also initiates a power-on reset.



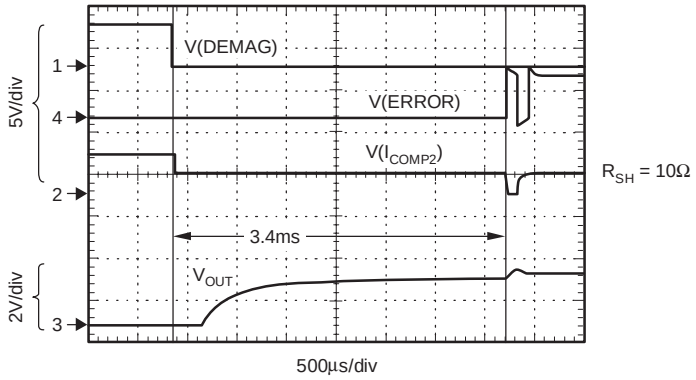
a) Demagnetization cycle on power-up. With power-up, the V_{OUT} across the compensation coil centers around half the supply and then starts the cycle after the 4V threshold is exceeded. The ERROR flag resets to H after the cycle is completed.



b) Power-up without demagnetization. The probe oscillation V(IS1) starts just before ERROR resets—15µs after the supply voltage crosses the 4V threshold.



c) Demagnetization cycle on command.



d) Abort of demagnetization cycle. The ERROR flag resets to H (as shown) and the output settles back to normal operation.

Figure 7. Demagnetization and Power-On Timing

ERROR CONDITIONS

In addition to the Over-Range flag that indicates signal clipping in the output amplifier (differential amplifier), a system error flag is provided. The ERROR flag indicates conditions when the output voltage does not represent the primary current. It is active during a demagnetization cycle, during a power-fail or brown-out. It also goes active with an open or short-circuit in the probe loop. As soon as the error condition is no longer present and the circuit has returned to normal operation, the flag resets.

Both the ERROR and Over-Range flags are open-drain logic outputs. They can be connected together for a wired-OR and require an external pull-up resistor for proper operation.

The following conditions result in ERROR flag activation (ERROR asserts low):

1. The probe comparator stays low for more than 32µs. This condition occurs either if the probe coil connection is open or if the supply voltage dips to the level where the required saturation current cannot be reached. During the 32µs timeout, the I_{COMP} driver remains active but goes inactive thereafter. In case of recovery, ERROR is low and the I_{COMP} driver remains in reset for another 3.3ms.
2. The probe driver pulse-width is less than 280ns for three consecutive periods. This condition indicates either a shorted field probe coil or a fully-saturated sensor at start-up. If this condition persists longer than 25µs and then recovers, the ERROR flag remains low and I_{COMP} is in reset for another 3.3ms. If the condition lasts less than 25µs, the ERROR flag recovers immediately and the I_{COMP} driver is not interrupted.
3. During demagnetization, if the cycle is aborted early by pulling DEMAG low, the ERROR flag stays low for another 3.3ms (I_{COMP} is disabled during this time).
4. An open compensation coil is detected (longer than 100µs). Note: the probe driver, the PWM signal filter and the I_{COMP} driver continue to function in normal mode—only the ERROR flag is asserted in this case. This condition indicates that not enough current is flowing in the I_{COMP} driver output; this condition might be the result of a high-resistance compensation coil or the connection of an external driver. Detection of this condition can be disabled by setting the CCdiag pin low.
5. At power-on after V_{DD1} crosses the +4V threshold, the ERROR flag is low for approximately 42µs.
6. A supply voltage low (brown-out) condition lasts longer than 100µs. Recovery is the same as power-up, either with or without a demag cycle.

PROTECTION RECOMMENDATIONS

The inputs IA_{IN1} and IA_{IN2} require external protection to limit the voltage swing beyond 10V of the supply voltage. The driver outputs I_{COMP1} and I_{COMP2} can handle high current pulses protected by internal clamp circuits to the supply voltage. If repeated over-currents of large magnitudes are expected, connect external Schottky diodes to the supply rails. This external protection prevents current flowing into the die.

The probe connections IS1 and IS2 are protected with diode clamps to the supply rails. In normal applications, no external protection is required. The maximum current must be limited to ±75mA.

All other pins offer standard protection—see the Absolute Maximum Ratings table.

BASIC CONNECTION EXAMPLE

The circuit shown in Figure 8 offers an example of a fully-connected current sensor system.

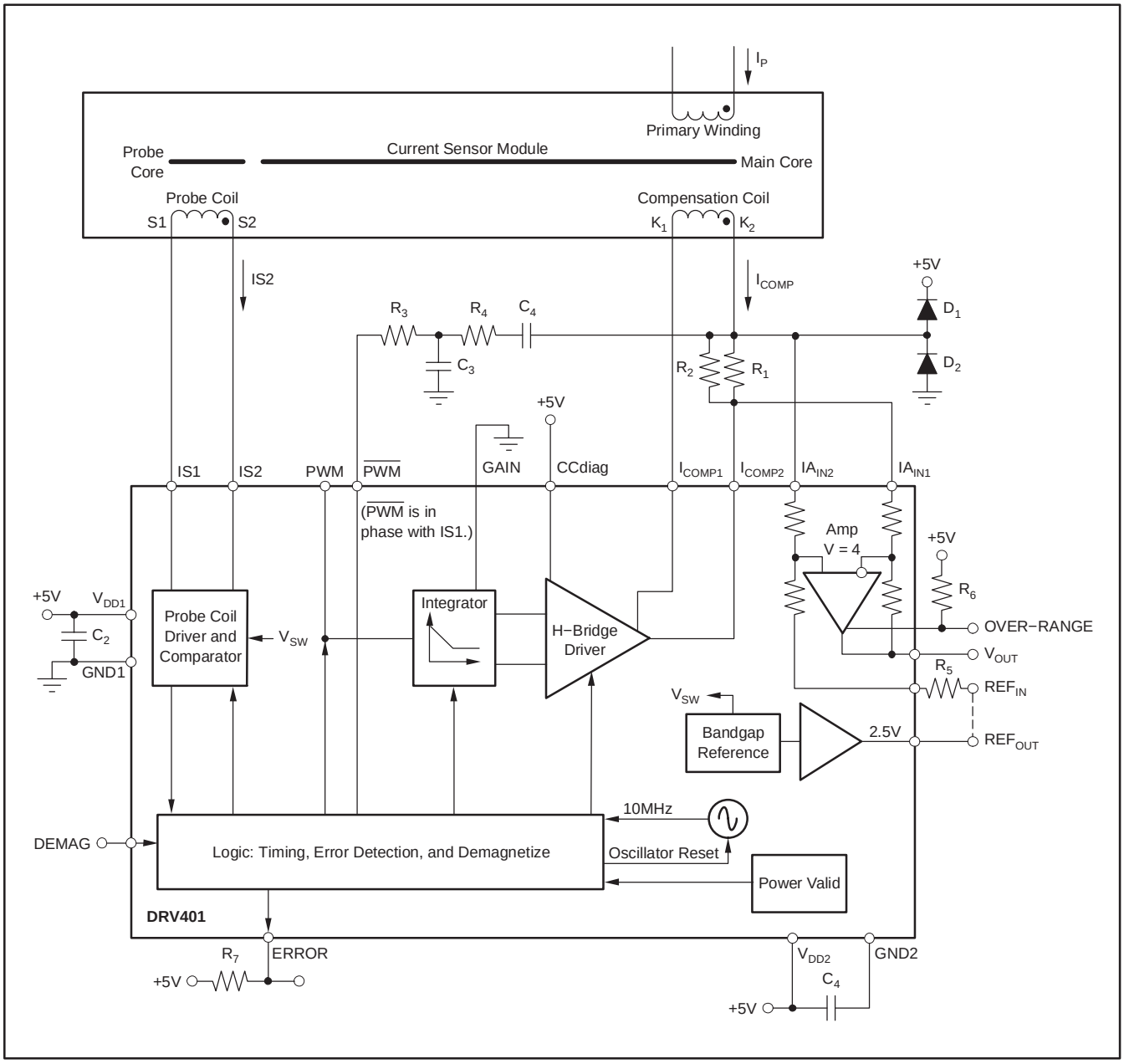


Figure 8. Basic Connection Circuit

The connection example in Figure 8 illustrates the few external components required for optimal performance. Each component is described in the following list:

I_P is the primary current to be measured; **K_1** and **K_2** connect to the compensation coil. **S1** and **S2** connect to the magnetic field probe. The dots indicate the winding direction on the sensor main core.

R_1 and **R_2** form the shunt resistor R_{SHUNT}. This resistance is split into two to allow for adjustments to the required R_{SHUNT} value. The accuracy and temperature stability of these resistors are part of the final system performance.

R_3 and **R_4**, together with **C_3** and **C_4**, form a network that reduces the remaining probe oscillator ripple in the output signal. The component values depend on the sensor type and are tailored for best results. This network is not required for normal operation.

R_5 is the dummy shunt (R_D) resistor used to restore the symmetry of both differential amplifier inputs. $R_5 = 4 \times R_{SHUNT}$, but the accuracy is less important.

R_6 and **R_7** are pull-up resistors connected to the logic outputs.

C_1 and **C_2** are decoupling capacitors. Use low ESR-type capacitors connected close to the pins. Use low impedance printed circuit board (PCB) traces, either avoiding vias (plated-through holes) or using multiple vias. A combination of a large (> 1µF) and a small (< 4.7nF) capacitor are suggested. When selecting capacitors, make sure to consider the large pulse currents handled from the DRV401.

D_1 and **D_2** are protection diodes for the differential amplifier input. They are only needed if the voltage drop at R_{SHUNT} exceeds 10V at the maximum possible peak current.

LAYOUT CONSIDERATIONS

The DRV401 operates with relatively large currents and fast current pulses, and offers wide-bandwidth performance. It is often exposed to large distortion energy from both the primary signal and the operating environment. Therefore, the wiring layout must provide shielding and low-impedance connections between critical points.

Use low ESR capacitors for power-supply decoupling. Use a combination of a small capacitor and a large capacitor of 1µF or larger. Use low-impedance tracks to connect the capacitors to the pins.

Both grounds should be connected to a local ground plane. Both supplies can be connected together; however, best results are achieved with separate decoupling (to the local GND plane) and ferrite beads in series with the main supply. The ferrite beads decouple the DRV401, reducing interaction with other circuits powered from the same supply voltage source.

The reference output is referred to GND2. A low-impedance, star-type connection is required to avoid the driver current and the probe current modulating the voltage drop on the ground track.

The connection wires of the difference amplifier to the shunt must be low resistance and of equal length. For best accuracy, avoid current in this connection. Consider using a *Kelvin Contact*-type connection. The required resistance value can be set using two resistors.

Wires and PCB traces for S1 and S2 should be very close or twisted. I_{COMP1} and I_{COMP2} should also be wired close together. To avoid capacitive coupling, run a ground shield between the S1/S2 and I_{COMP} wire pair or keep them distant from each other.

The compensation driver outputs (I_{COMP}) are low frequency only; however, the primary signal (with high-frequency content present) is coupled into the compensation winding, the shunt, and the difference amplifier. Therefore, careful layout is recommended.

The output of REF_{OUT} and V_{OUT} can drive some capacitive loads, but avoid large direct capacitive loads; these loads increase internal pulse currents. Given the wide bandwidth of the differential amplifier, isolate any large capacitive load with a small series resistor. A small capacitor in the pF range can improve the transient response on a high resistive load.

The exposed thermal pad on the bottom of the package must be soldered to GND because it is internally connected to the substrate, which must be connected to the most negative potential. It is also necessary to solder the exposed pad to the PCB to provide structural integrity and long-term reliability.

POWER DISSIPATION

Using the thermally-enhanced PowerPAD™ SO and QFN packages dramatically reduces the thermal impedance from junction to case. These packages are constructed using a down-set lead frame upon which the die is mounted, as shown in Figure 9a and Figure 9b. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. Figure 9 shows the SO-20 package as an example. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The two outputs I_{COMP1} and I_{COMP2} are linear outputs. Therefore, the power dissipation on each output is proportional to the current multiplied by the internal voltage drop on the active transistor. For I_{COMP1} and I_{COMP2}, this internal voltage drop is the voltage drop to V_{DD2} or GND, according to the current-conducting side of the output.

Output short-circuits are particularly critical for the driver because the full supply voltage can be seen across the conducting transistor, and the current is not limited by anything other than the current density limitation of the FET. Permanent damage to the device can occur.

The DRV401 does not include temperature protection or thermal shut-down.

THERMAL PAD

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. Table 1 shows the thermal resistance (T_{JA}) for the two packages with the exposed thermal pad soldered to a normal PCB, as described in Technical Brief SLMA002, *PowerPAD Thermally-Enhanced Package*. See also EIA/JEDEC Specifications JESD51-0 to 7, *QFN/SON PCB Attachment* (SLUA271), and *Quad Flatpack No-Lead Logic Packages* (SCBA017). These documents are available for download at www.ti.com.

Table 1. $\theta_{JA/JP}$ Estimations According To EIA/JED51-7

	QFN-20	SO-20
θ_{JP}	9	9
θ_{JA} Still Air	40	35
θ_{JA} with Forced Airflow (150lfm)	38	32

θ_{JA} = junction-to-ambient thermal resistance,
θ_{JP} = junction-to-pad thermal resistance,
lfm = linear foot per minute.

NOTE: All thermal models have an accuracy ≈ 20%.

Measuring the temperature as close as possible to the exposed thermal pad is recommended. The relatively low thermal impedance, θ_{JP}, of less than 10°C/W (with some additional °C/W to the temperature test point on the PCB) allows good estimation of the junction temperature in the application.

The thermal pad on the PCB should contain nine or more vias for the QFN package. The same applies for the SO package, where the solder pad on the PCB can be larger than the exposed pad (for example, 6.6mm × 18mm) as recommended in the application literature noted previously.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.

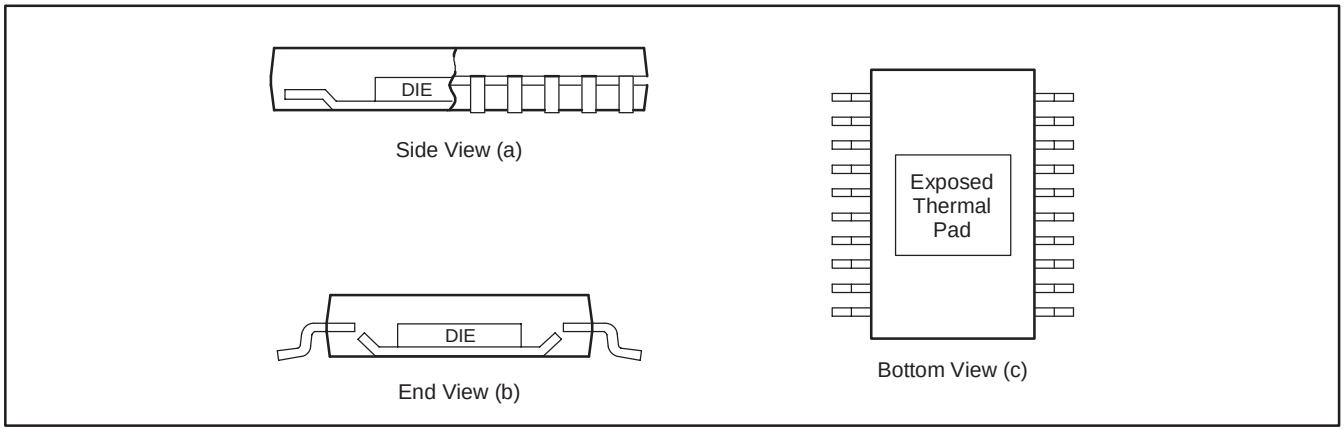


Figure 9. SO-20 Package Example of Thermally-Enhanced PowerPAD

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/09	B	1	Front Page	Updated front page appearance.
		5	Pin Configurations	Added DWP pinout information to the Pin Assignments table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV401AIDWP	Obsolete	Production	SO PowerPAD (DWP) | 20	-	-	Call TI	Call TI	-40 to 125	DRV401A
DRV401AIDWPR	Active	Production	SO PowerPAD (DWP) | 20	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV401A
DRV401AIDWPR.A	Active	Production	SO PowerPAD (DWP) | 20	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV401A
DRV401AIDWPR.B	Active	Production	SO PowerPAD (DWP) | 20	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV401A
DRV401AIRGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HAAQ
DRV401AIRGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HAAQ
DRV401AIRGWR.B	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HAAQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DRV401 :

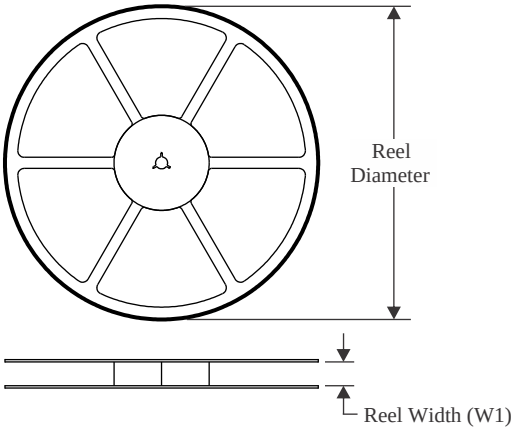
- Automotive : DRV401-Q1
- Enhanced Product : DRV401-EP

NOTE: Qualified Version Definitions:

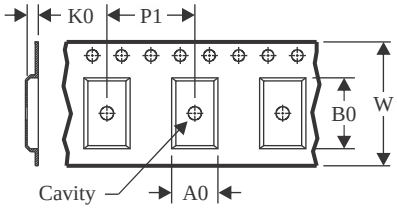
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

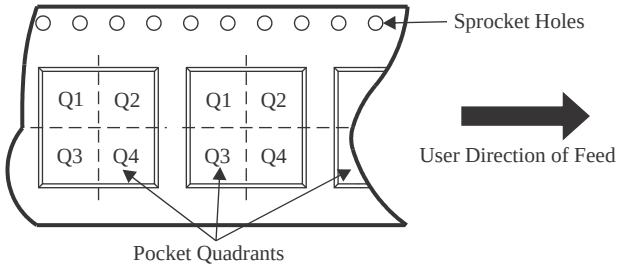


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

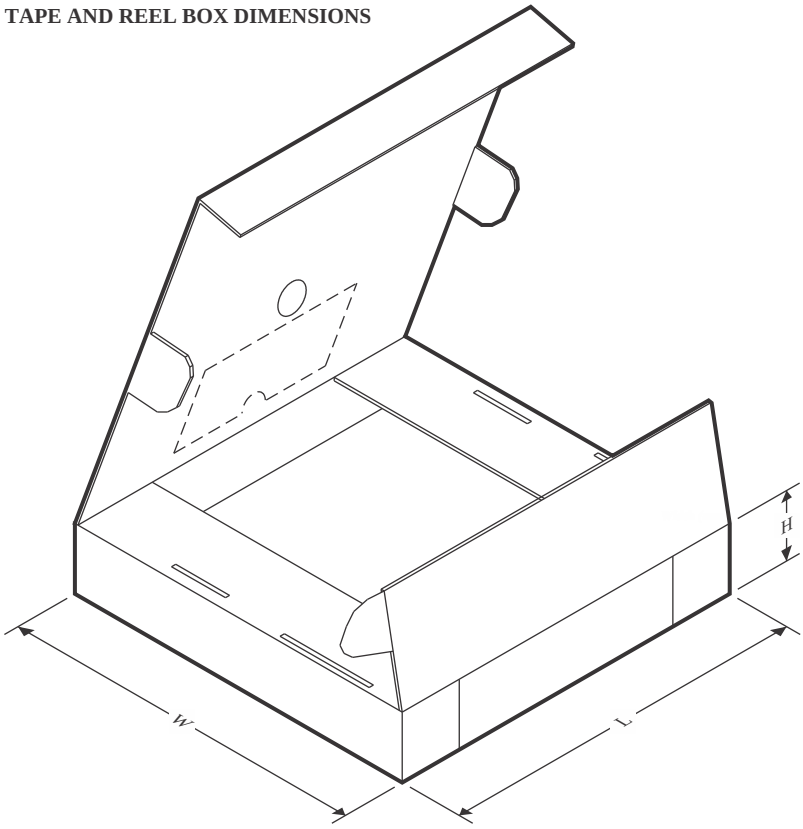
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV401AIDWPR	SO PowerPAD	DWP	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV401AIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV401AIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV401AIDWPR	SO PowerPAD	DWP	20	1000	356.0	356.0	45.0
DRV401AIRGWR	VQFN	RGW	20	3000	360.0	360.0	36.0
DRV401AIRGWR	VQFN	RGW	20	3000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

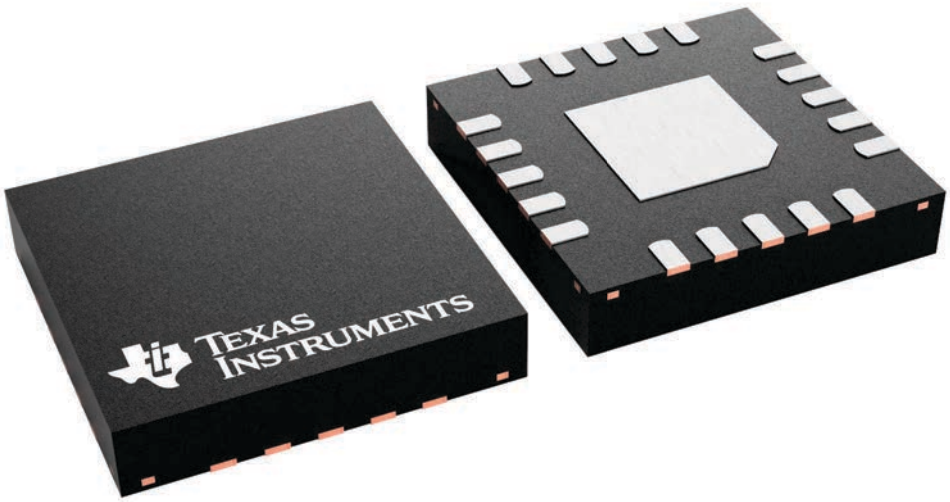
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



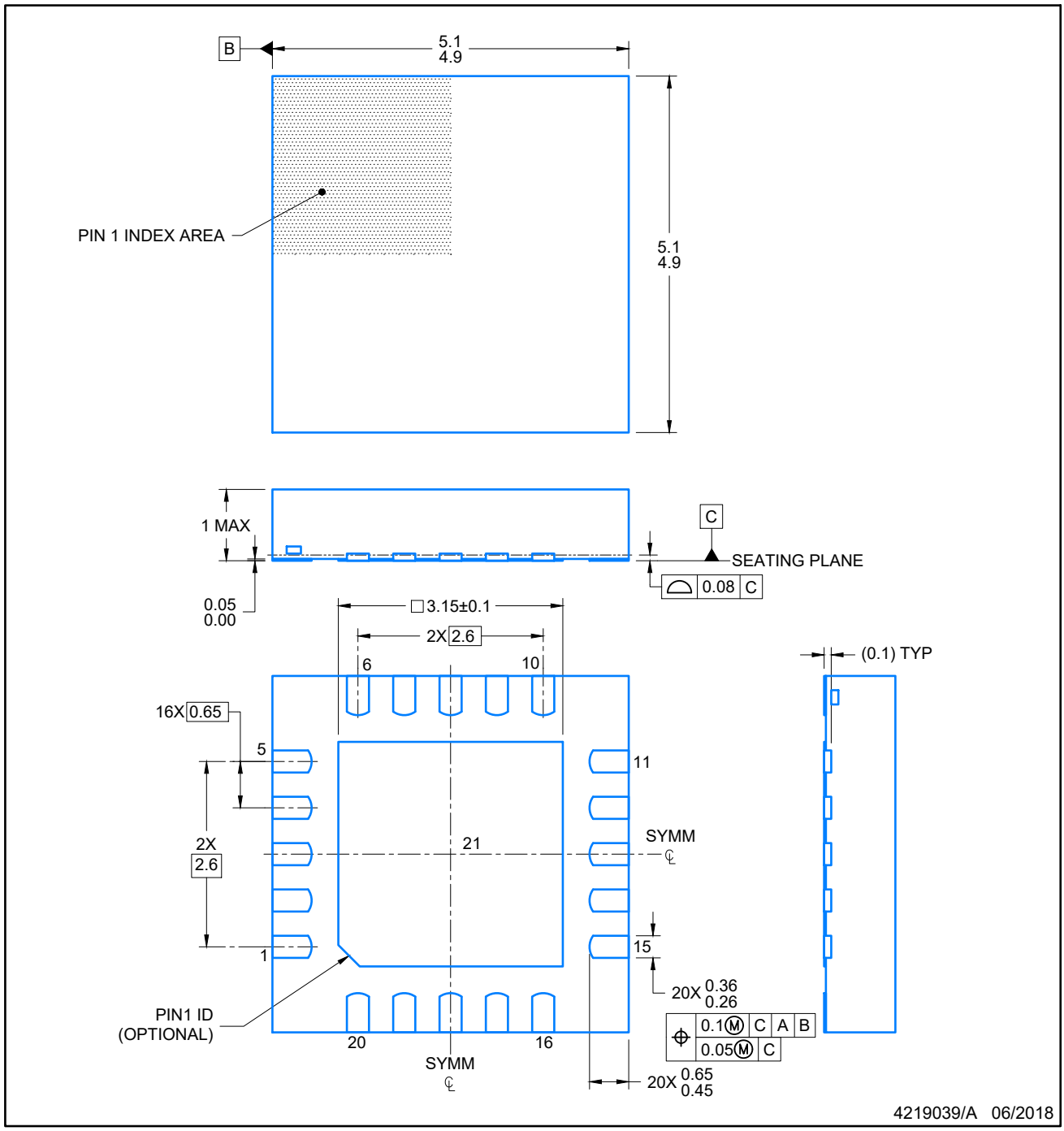
4227157/A

PACKAGE OUTLINE

RGW0020A

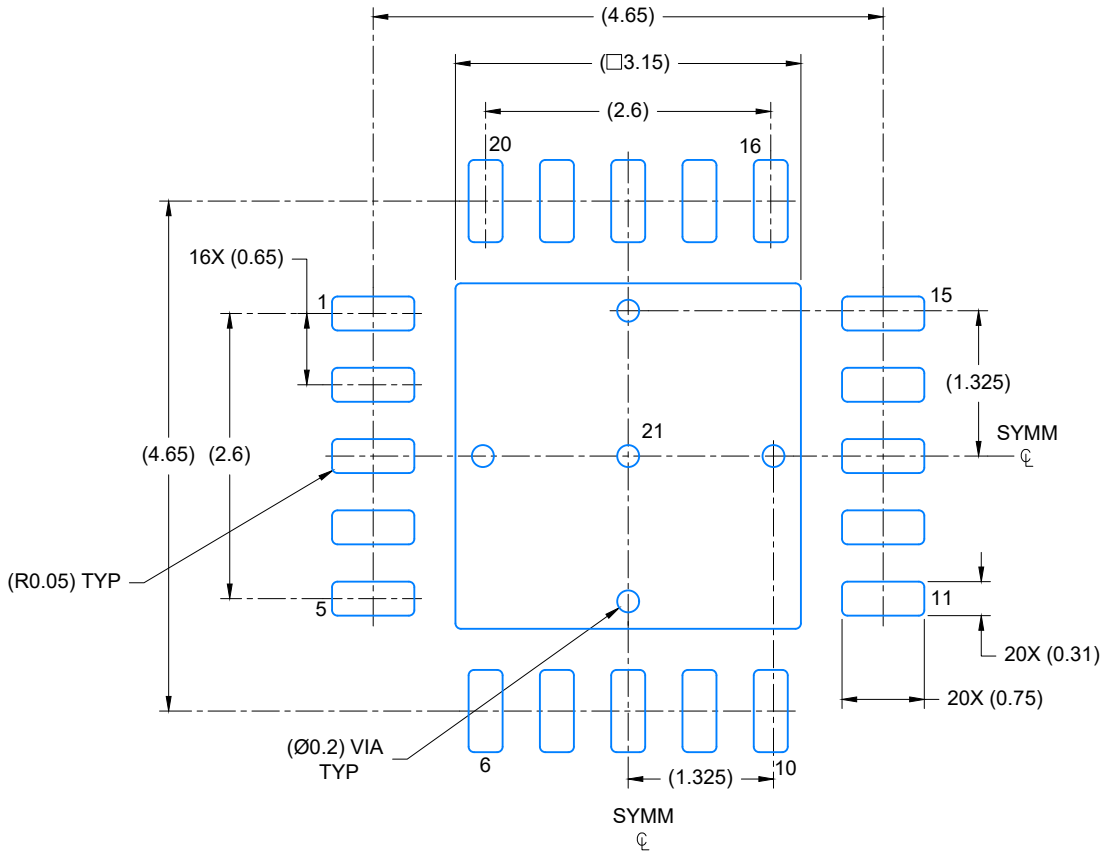
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



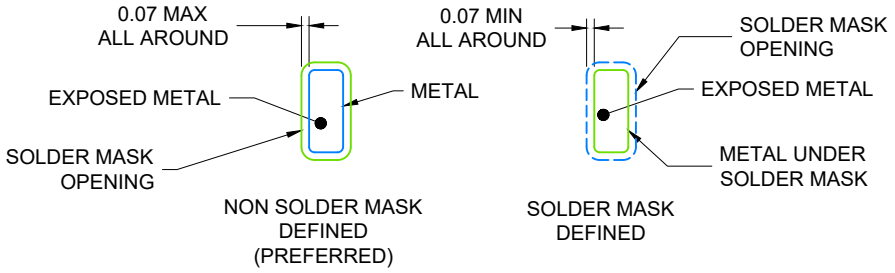
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

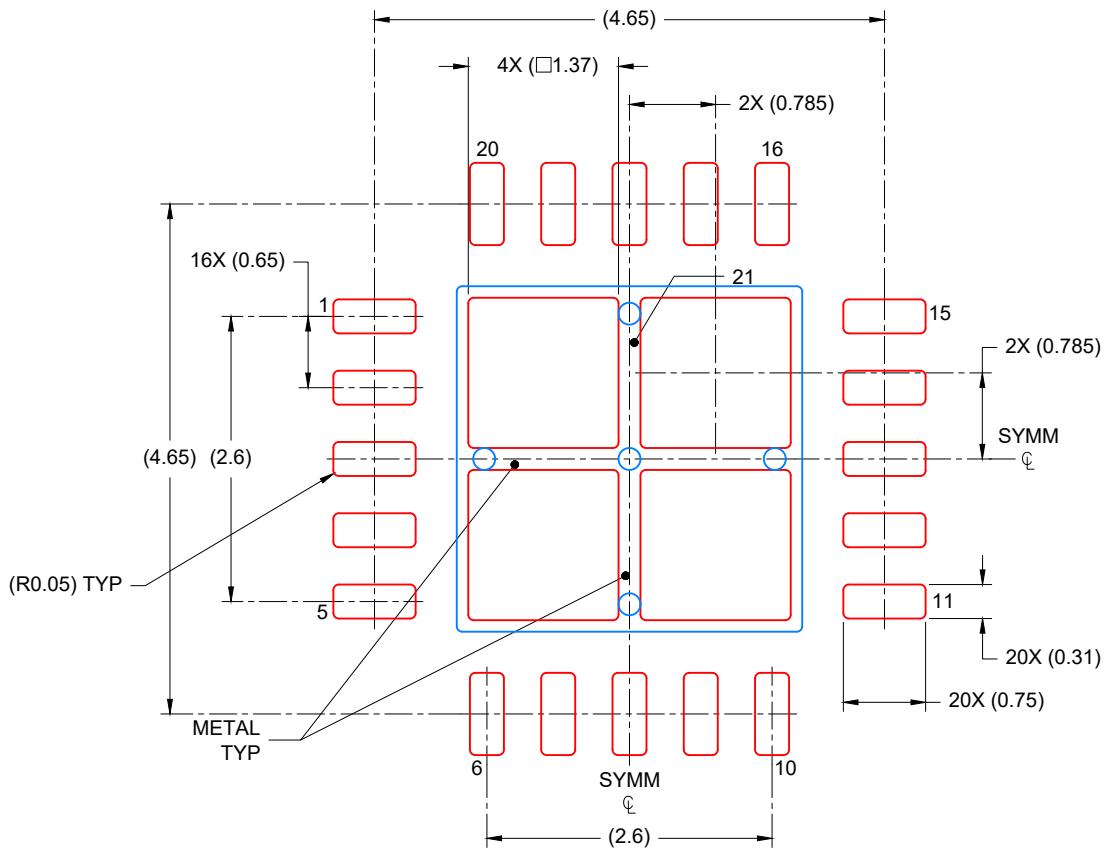


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

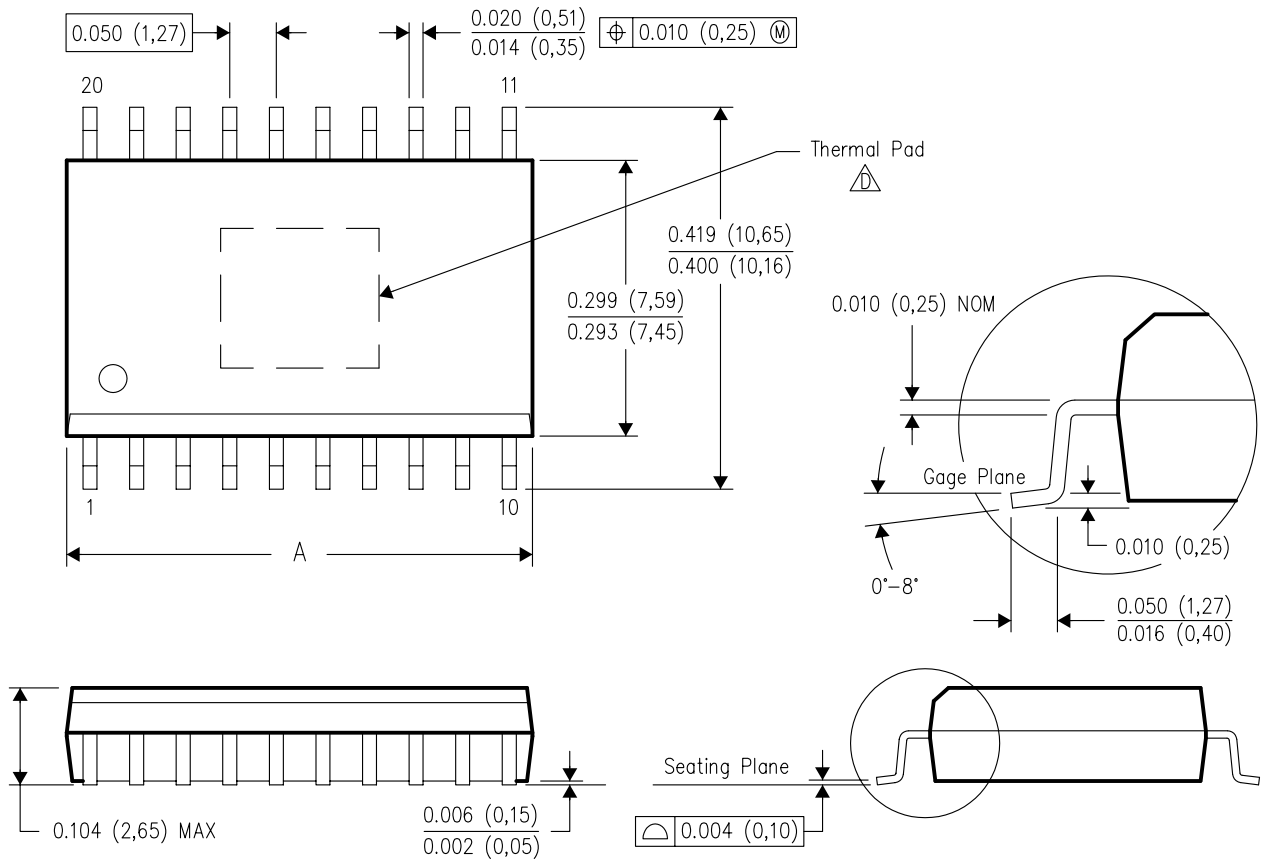
4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

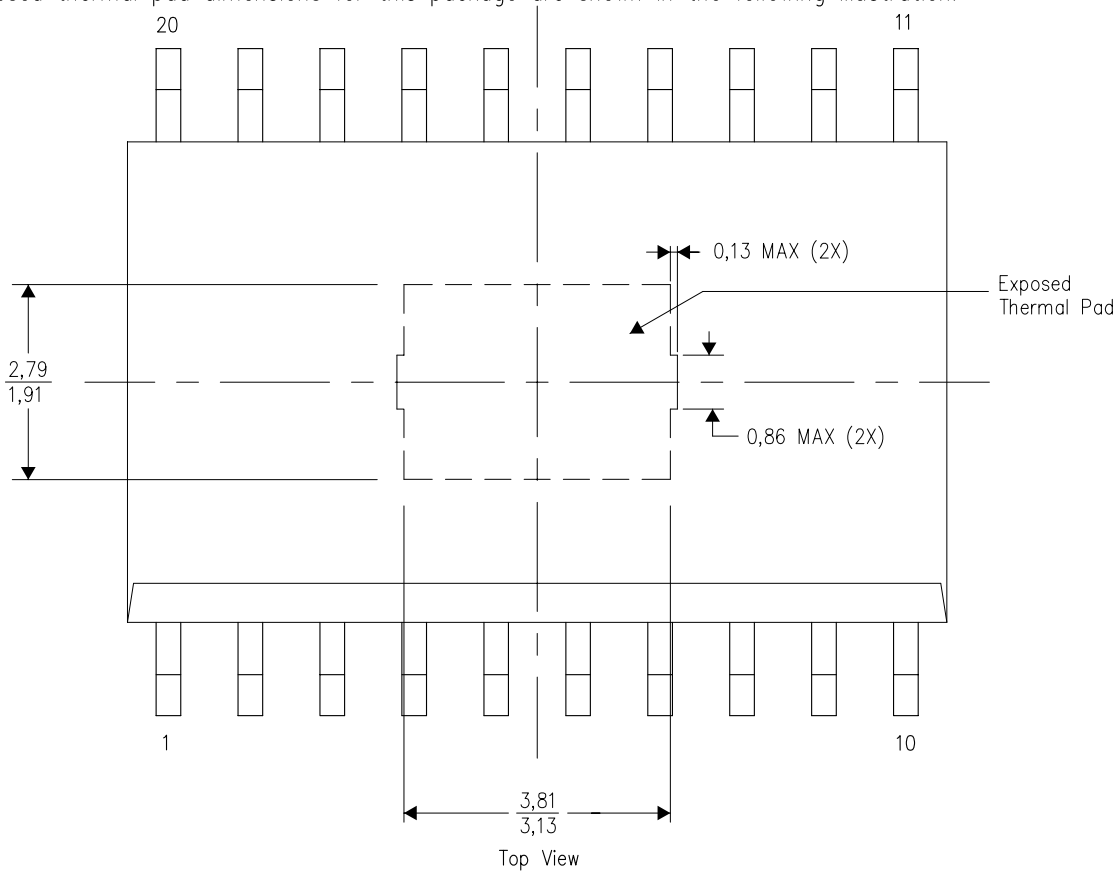
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

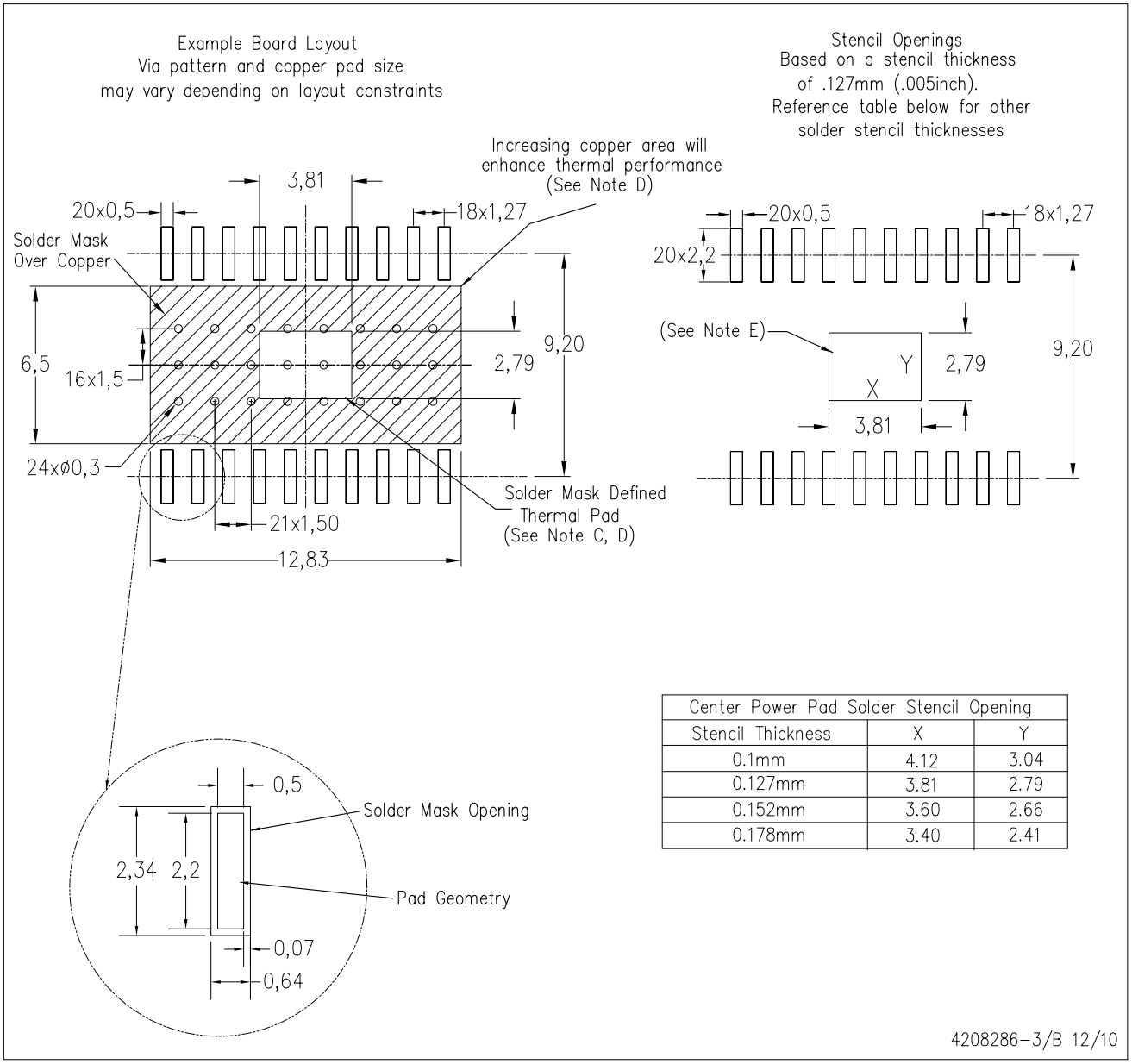


Exposed Thermal Pad Dimensions

4206325–4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.12	3.04
0.127mm	3.81	2.79
0.152mm	3.60	2.66
0.178mm	3.40	2.41

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

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Last updated 10/2025