DRV81315/A-Q1 Protected Low-Side Switch

1 Features

- Single Channel Protected Low side switch
  - **100mΩ $R_{DS(ON)}$** at 25°C
  - Output Stage upto **40V operating tolerance**
- AEC-Q100 Qualified (Upto Grade 1)
- Fully Protected
  - **Internal current limit**
  - **Independent Overtemperature** protection
    - Dynamic and absolute overtemperature protection
  - **Integrated Overvoltage clamp** for Inductive load discharge
- **Diagnostic feedback**
  - MCU Fault interrupt signal (STATUS)
  - Off state **open load detect** (DRV81315A only)
- **2.6V to 5.5V input** supply voltage range
  - Supports **3p3V, 5V MCU** I/O control
- Thermally Enhanced Surface mount packages **(DDA-8 , DRL-6)**

2 Applications

- Engine and Transmission
- Lighting
- Braking and Suspension
- Body Electronics and Zonal modules
- Battery management system

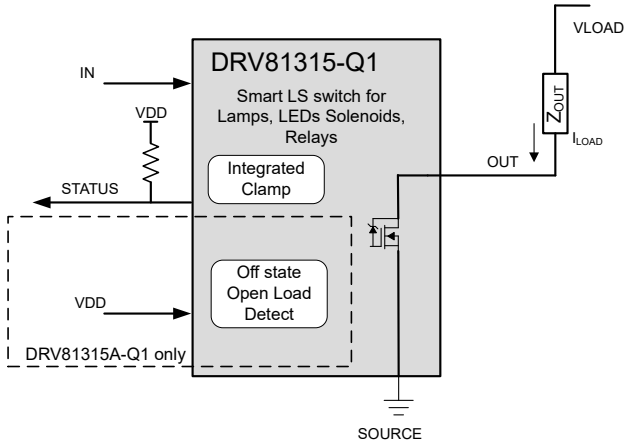
3 Description

The DRV81315/A-Q1 integrates single protected low side switch with a low $R_{DS(ON)}$ of 100mΩ. The device can be controlled by means of a GPIO interface. The switch is protected against over current by means of an internal fixed threshold current limit. The switch is protected against overtemperature by integrated overtemperature sensor. The switch integrates an output overvoltage protection for inductive load demagnetization. Faults report is available as an open drain STATUS output. The DRV81315A also supports open-load/short to GND detection diagnostic in the off state, reported on the STATUS pin. The DRV81315/A are available in 6-pin DRL(SOT-563) package and 8-pin HSOIC(DDA) thermally enhanced package (Eco-friendly: RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV81315DDA	HSOIC (8)	4.90 mm × 3.90 mm
DRV81315ADDA	HSOIC (8)	4.90 mm × 3.90 mm
DRV81315ADRL	SOT-563(6)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Pin Configuration and Functions

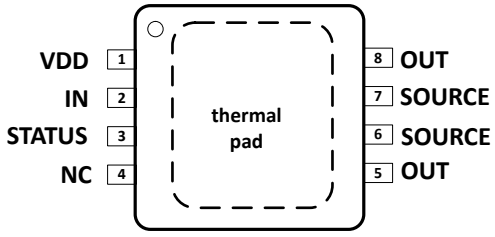


Figure 4-1. DRV81315A DDA Package8-Pin HSOICTop View

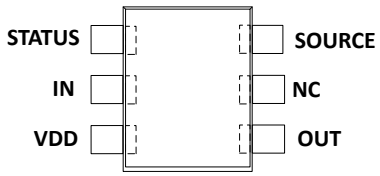


Figure 4-2. DRV81315A DRL Package6-Pin SOT-563 (with Immersion Sn)Top View

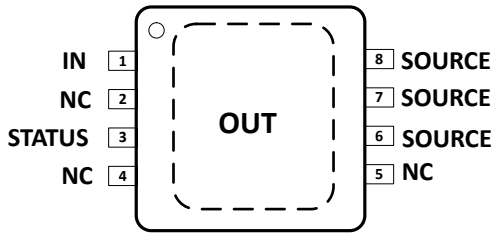


Figure 4-3. DRV81315 DDA Package8-Pin HSOICTop View

Pin Functions

PIN				Type	DESCRIPTION
NAME	DRV81315A		DRV81315		
	DDA8	DRL6	DDA8		
IN	2	2	1	I	GPIO input for control
VDD	1	3	-	P	Supply pin, connect to 3p3V, 5V
STATUS	3	1	3	O	Diagnostic output
NC	4	5	2,4,5	-	
SOURCE	6,7	6	6,7,8	G	Power FET source and ground reference
OUT	5,8	4	EP	O	Power FET Drain

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5 Specification

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
IN	Input Logic voltage	-0.3	5.75	V
VDD	Input Supply Voltage(DRV81315A)		5.75	V
V_{OUT}	Output tolerance	-0.3	Internally limited	V
V_{OUT_SC}	Output voltage fault short circuit tolerance		28	V
$E_{AS_sp_DDA}$	Single pulse Energy capability for DDA T_J = 150 C ,R_L=17Ω, L = 100mH, V_{LOAD}=14V		50	mJ
$E_{AS_sp_DRL}$	Single pulse Energy capability for DRL T_J = 150 C ,R_L=50Ω, L = 300mH, V_{LOAD}=24V		50	mJ
$E_{AS_rep_p_DDA}$	Inductive clamp energy for 2M cycles, DDA package. T_J = 125C ,R_L=24Ω, L = 100mH, V_{LOAD}=14V		20	mJ
$E_{AS_rep_p_+DRL}$	Inductive clamp energy for 2M cycles, DRL package. T_J = 125C ,R_L=50Ω, L = 300mH, V_{LOAD}=14V		10	mJ
STATUS	Digital output pin voltage	-0.5	5.75	V
I_{peak}	Peak motor drive output current	Internally limited		A
P_{dis}	Continuous total power dissipation	See *Section 5.4*		
T_J	Operating virtual junction temperature	-40	150	°C
T_{stg}	Storage temperature	-60	150	°C

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage (DRV81315)		3		5.5	V
V_{VDD}	Input Supply Voltage (DRV81315A)					
V_{LOAD}	Battery voltage during normal operation		6		18	V
T_{AMB}	Operating Ambient temperature		-40		125	°C
T_J	Operating junction temperature		-40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		DDA (HSOIC-8)	DRL (SOT-563)	UNIT
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.4*[1]	137.4*	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.0*	58.8*	°C/W

[1] *Values are initial estimates

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THERMAL METRIC(1)		DDA (HSOIC-8)	DRL (SOT-563)	UNIT
		8 PINS	6 PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	20.3*	29.8*	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4*	1.3*	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.3*	29.4*	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.1*	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note, SPRA953.

5.5 Electrical Characteristics

Typical values are at T_A = 25°C . All limits are over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{q_off}	Supply current in inactive state	IN = 0, DRV81315A	4	10	25	µA
I_{q_on}	Supply current in active state	IN = 1	25	40	65	µA
I_{q_fault}	Supply current in fault state	IN = 1			400	µA
V_{UVLO_rise}	VDD undervoltage rising	DRV81315A	2.5		2.9	V
	IN undervoltage rising	DRV81315				
V_{UVLO_fall}	VDD undervoltage falling	DRV81315A	2.3		2.6	V
	IN undervoltage falling	DRV81315				
STATUS OUTPUT						
V_{STAT_L}	Status output low voltage	I_{STAT}= 1mA			0.4	V
I_{STAT_H}	Status high leakage current	V_{STAT} = 5V			1	µA
TWO-LEVEL LOGIC INPUT (DRV81315A)						
V_{IL}	Low level logic input				0.8	V
I_{IL}	Low level logic input current	V_{IN} = 0V	-1		1	µA
V_{IH}	High level input voltage		2			V
I_{IH}	High level input current	V_{IN} = 5.5			10	µA
V_{I_HYS}	Input voltage hysteresis		0.13			V
OUTPUT STAGE						
$R_{DS(ON)}$	FET on resistance	I_O = 1A , T_J = 25°C , V_{VDD}=3V, IN=1, DRV81315A		125		mΩ
		I_O = 1A , T_J = 25°C, V_{IN}=3V, DRV81315				
		I_O = 1A, T_J = 150°C , V_{VDD}=3V, IN=1, DRV81315A			250	
		I_O = 1A , T_J = 150°C, V_{IN}=3V, DRV81315				
$R_{DS(ON)}$	FET on resistance	I_O = 1A , T_J = 25°C , V_{VDD}=5V, IN=1, DRV81315A		110		
		I_O = 1A , T_J = 25°C, V_{IN}=5V, DRV81315				
		I_O = 1A, T_J = 150°C , V_{VDD}=5V, IN=1, DRV81315A			220	
		I_O = 1A , T_J = 150°C, V_{IN}=5V, DRV81315				
I_{OFF}	Off-state leakage current	V_{OUT} = 18 V, T_J = 150°C			5	µA
V_F	Body diode forward voltage	I_O = -1A		0.8		V
V_{CLTH_LT}	Drain source clamping voltage threshold	I_{OUT} = 10 mA , T_J = -40°C	40			V

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Typical values are at T_A = 25°C . All limits are over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLAMP}	Drain source clamping voltage	I_{OUT} = 1.5 A , T_J = 150°C	41		45	V
OFF STATE DIAGNOSTIC(DRV81315A)						
V_{OL}	Off state open load output detection threshold	IN = 0	0.6	1.2	1.8	V
t_{OL_DG}	Output comparator deglitch			150		µs
SWITCHING						
t_R	Rise time	V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=5V, DRV81315	20	30	40	µs
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=3V, DRV81315	20	30	40	
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=3V, DRV81315A				
t_F	Fall time	V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=5V, DRV81315	15	25	50	µs
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=3V, DRV81315	30	60	120	
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=3V, DRV81315A				
SR_{rise}	Rising slew rate	V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{IN}=5V, DRV81315	0.3	0.5	0.7	V/µs
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{IN}=3V, DRV81315	0.3	0.5	0.7	
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{VDD}=3V, DRV81315A				
SR_{fall}	Falling slew rate	V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{IN}=5V, DRV81315	0.3	0.5	0.7	V/µs
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{IN}=3V, DRV81315	0.1	0.25	0.4	
		V_{LOAD} = 13V; R_L = 13Ω, VOUT = 30% V_{LOAD} to 70% V_{LOAD}, V_{VDD}=3V, DRV81315A				
$t_{PD_L_to_H}$	Propogation Delay , Input Low to Output High	V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=5V, DRV81315	20	33	40	µs
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=3V, DRV81315	20	33	40	
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=3V, DRV81315A				
$t_{PD_H_to_L}$	Propogation Delay, Input High to Output Low	V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=5V, DRV81315	18	25	45	µs
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=5V, DRV81315A				
		V_{LOAD} = 13V; R_L = 13Ω, V_{IN}=3V, DRV81315	18	25	45	
		V_{LOAD} = 13V; R_L = 13Ω, V_{VDD}=3V, DRV81315A				
PROTECTION CIRCUITS						
I_{LIM}	Current limitation value	V_{INX}= 5, T_J = 25°C , DDA package		7.8	10	A
		V_{INX}= 5, T_J = 150°C , DDA package	5.5			A
I_{LIM}	Current limitation value	V_{INX}= 5, T_J = 25°C , DRL package		4.7	6	A
		V_{INX}= 5, T_J = 150°C , DRL package	3			A
T_{TSD}	Thermal shutdown temperature	Die temperature	150	175	200	°C
T_{TSD_hys}	Thermal shutdown temperature hysteresis			7		°C

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Typical values are at T_A = 25°C . All limits are over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{STAT_reset}	Thermal reset of Status		135			°C
ΔT_J	Dynamic temperature			40		K
ΔT_{J_HYS}	Dynamic temperature hysteresis			15		K
t_{STATUS}	Overtemperature deglitch on STATUS pin			20		µs

Output timing diagrams

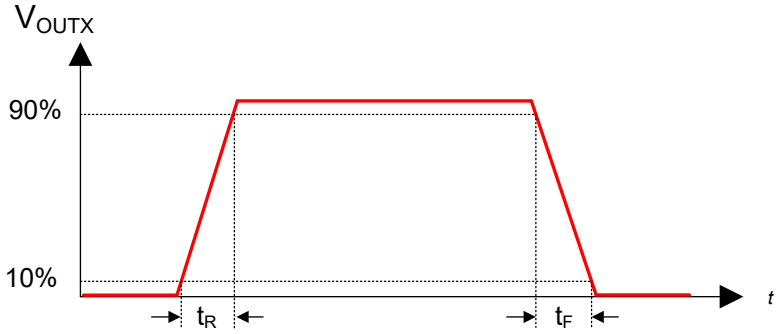


Figure 5-1. Output rise/fall times

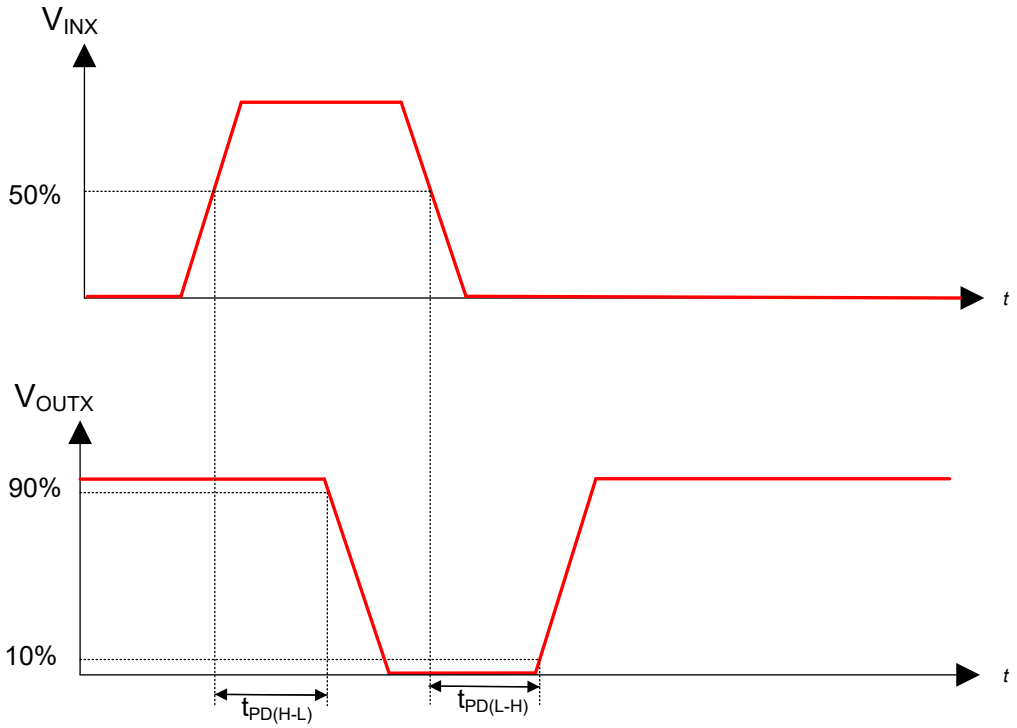


Figure 5-2. Propogation delay

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5.6 Transient thermal impedance and Current capability

*Information based on thermal simulations. Values are Initial estimates***

Table 5-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability

PART NUMBER	PACKAGE	$R_{\theta JA}$ [°C/W](1)				Current [A] (2)			
		0.01 sec	0.1 sec	1 sec	DC	0.01 sec	0.1 sec	1 sec	DC
DRV81315A-Q1	DDA (HSOIC8)	5	12	23	47	8.5	5.5	4	2.8
	DRL (SOT-563)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
DRV81315-Q1	DDA (HSOIC8)	5	12	23	47	8.5	5.5	4	2.8

(1) Based on thermal simulations using 114.3 × 76.2 × 1.6mm, 4 layer PCBSection 7.2.2 – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes with 0.3mm thermal via drill diameter, 0.025mm Cu plating, 1 minimum mm via pitch.
(2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C.

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6 Detailed Description

6.1 Overview

The DRV81315/A is a single channel low side switch driver with each integrated switch of typical Rdson 100mΩ. The switch has integrated overvoltage protection for safe demagnetization of Inductive loads. The DRV81315A variant is powered over the VDD pin, and IN pin serves as logic input to control output. The DRV81315 (non A) variant utilizes IN pin as both power as well as control logic. The switch is protected against over current by means of a fixed integrated current limit. Furthermore, the switch also has overtemperature protection. Diagnostic feedback is available over an open drain output STATUS on the DRV81315. An off state diagnostic is available on the DRV81315A for detection of an open load or STG condition on the output. The DRV81315/A is available in both 8-pin HSOIC(DDA package) and 6-pin SOT-563(DRL package).

Property	DRV81315A	DRV81315
Package	DDA(HSOIC8), DRL(SOT-563)	DDA(HSOIC8)
Off state open load / STG diagnostic	Y	N
Power input	VDD	IN
Logic control for Output	IN	IN

6.2 Functional Block Diagram

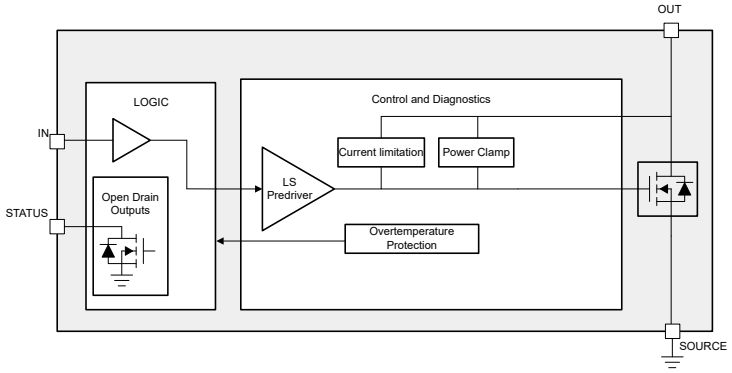


Figure 6-1. DRV81315-Q1

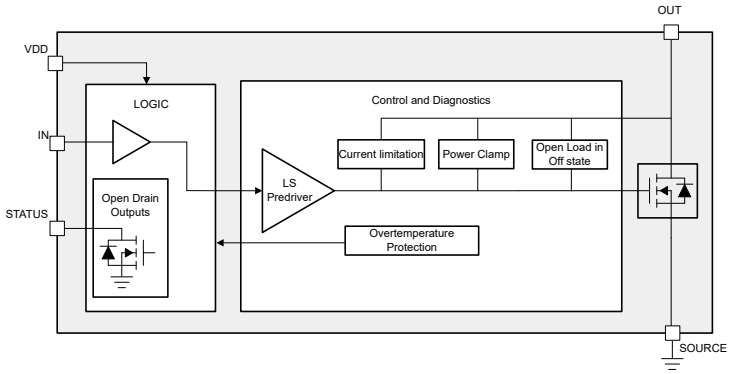


Figure 6-2. DRV81315A-Q1

6.3 Feature Description

6.3.1 Off state diagnostics (OL, STG)

The DRV81315A device features a comparator on the OUT pin which can be used to indicate the output state. When used in conjunction with an external pull down resistor , the comparator can help detect an open load

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condition (OL). The resistor selection is influenced by leakage tolerance of load, capacitance on output and PWM interval of the load.

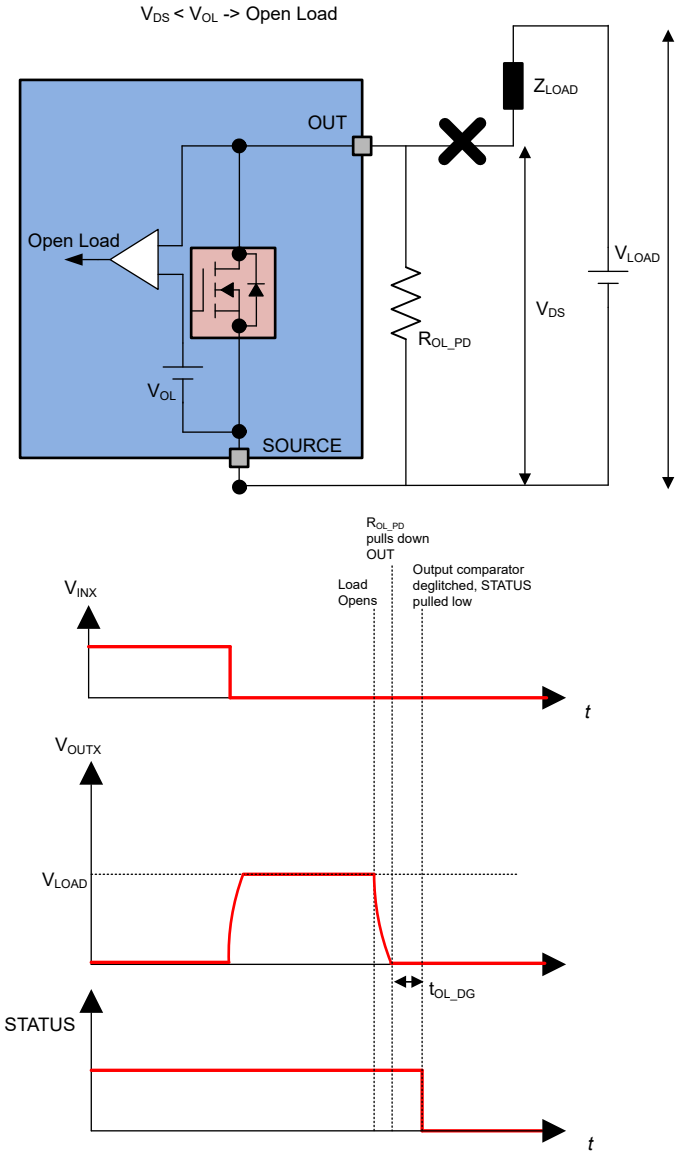


Figure 6-3. Open Load detection

An external resistor (R_{OL_PD}) can be connected to pull the output down to ground if the Load is disconnected.

The comparator output can also be helpful to determine if a short to GND condition (STG) is present on the OUT pin. Following are the values of short the can be detected.

$$R_{short} \leq \frac{V_{OL}(R_{load})}{(V_{load} - V_{OL})} \quad (1)$$

Where R_{short}[2] is the impedance of the short that can be detected, R_{load} is the impedance of the load, V_{load} is the load side supply and V_{OL} is the Output comparator threshold.

[2] This expression neglects a High impedance Pull down recommended for Open load detection R_{OL_PD}

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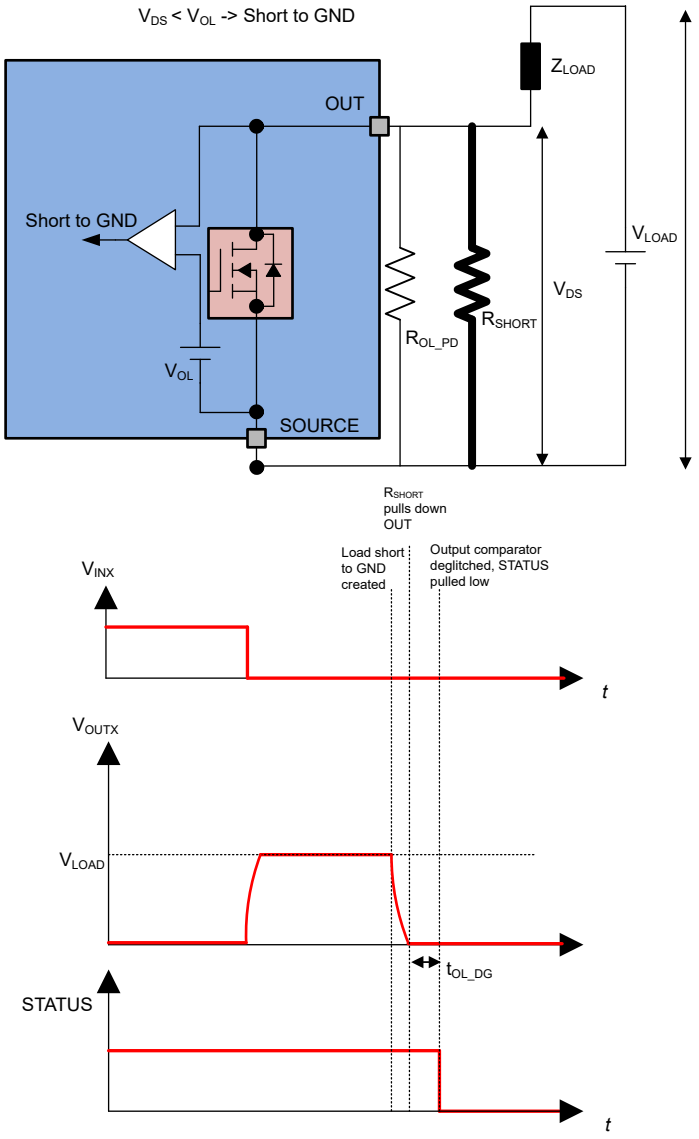


Figure 6-4. Short to GND

User must note that since Open Load as well as Short to Ground result in same output state, distinguishing one from another is not possible.

6.3.2 Control Interface / Power input

The DRV81315-Q1 device does not have a dedicated supply pin. The circuits are powered over the IN pin, which also functions as control input. The DRV81315A-Q1 device does have a VDD pin , separate from IN pin. Here the VDD pin acts as supply and the IN pin acts as pure logic control for the Output low side FET

When logic high voltage is applied to IN pin, the corresponding channel Output low side FET is turned on and output is pulled low.

6.4 Protection Circuits

The DRV81315/A-Q1 is Fully protected in Overcurrent , Overtemperature, FET Overvoltage and Undervoltage scenarios

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6.4.1 Overvoltage clamp

When switching off inductive loads, voltage clamping is necessary to prevent device damage. The active clamping circuit consists of a zener stack connected between the Drain and the Gate. When the kickback voltage exceeds the Zener threshold , the kickback pushes current into the gate, forcing the FET to turn back on slightly in the saturation region. This dissipates the inductive energy directly inside the FET in a controlled manner.

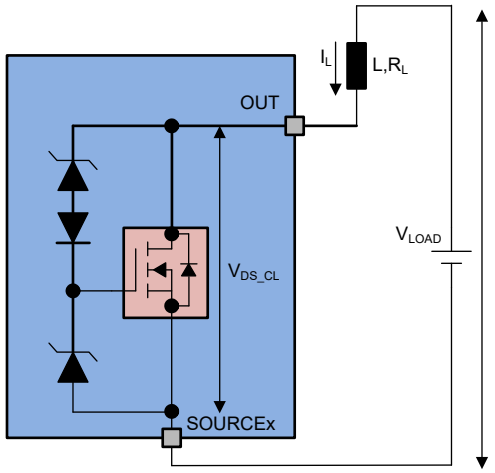


Figure 6-5. Active overvoltage clamp

6.4.1.1 Demagnetization energy capability

During demagnetization of inductive loads, magnetic energy is dissipated in the DRV813xx-Q1 low-side switch. The equation shows how to calculate the energy for low-side switches when the low-side V_{DS} clamp voltage is V_{DS_CL} , when the load (L, R_L) is carrying current I_L and the other end of load is connected to V_{LOAD}:

$$E_{AS} = V_{DS_CL} \times \left[\frac{V_{LOAD} - V_{DS_CL}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{LOAD} - V_{DS_CL}}\right) + I_L\right] \times \frac{L}{R_L} \quad (2)$$

Under the assumption of R_L = 0, this simplifies to

$$E_{AS} = \frac{1}{2} \times L \times {I_L}^2 \times \left(\frac{V_{DS_CL}}{V_{DS_CL} - V_{LOAD}}\right) \quad (3)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AS_sp} value provided in Absolute Maximum Ratings denotes the single pulse energy handling capability per channel, while the $E_{AS_Rep_p}$ value provided in Absolute Maximum Ratings denotes the repetitive pulse energy handling capability per channel.

6.4.1.1.1 Single pulse clamping capability

The maximum energy and corresponding load inductance, load current the device can withstand for one pulse inductive dissipation at 125°C is shown here. The device can withstand 40% of this energy for one million inductive repetitive pulses with a >4-Hz repetitive pulse. If the application parameters exceed this device limit, use a protection device like a freewheeling diode to dissipate the energy stored in the inductor

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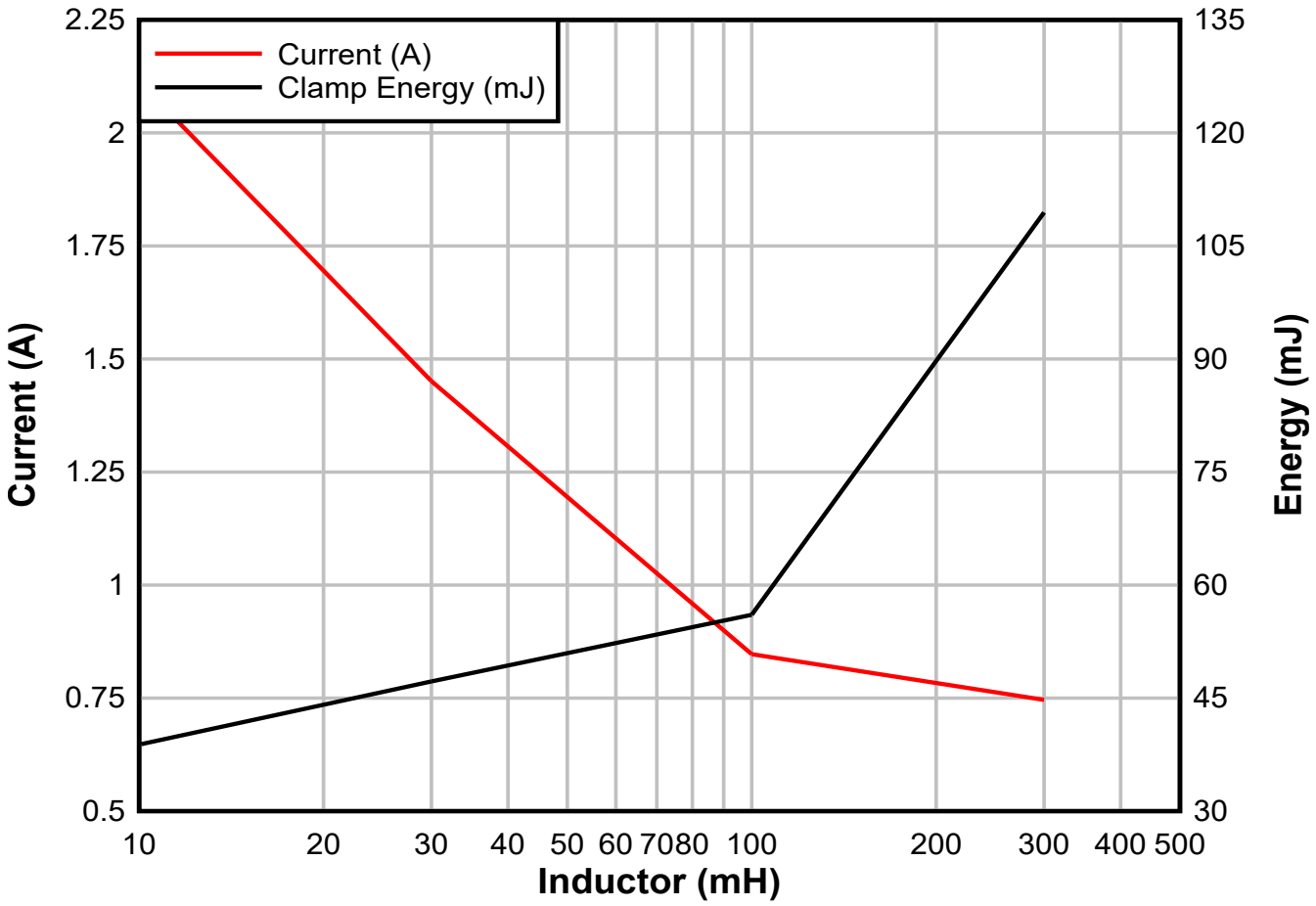


Figure 6-6. Single pulse clamping energy (per channel) at T_J = 150C (DDA package)

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6.4.2 Overcurrent limit

Overcurrent limitation is intended to protect against short circuit conditions while allowing inrush currents typical of loads such as lamps, motors and capacitive loads. When the sensed load current exceeds the limitation level I_{LIM} , the gate drive of the low side FET is continually altered in closed loop to keep output current limited.

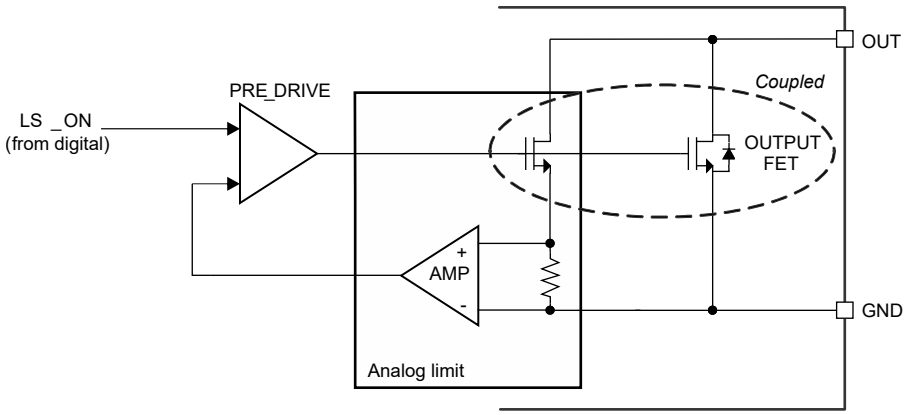


Figure 6-7. Working of Current limit circuit

The effect of this is a possible increase in the FET drain to source voltage and consequently a drastic increase in power dissipated. The FET keeps heating up at I_{LIM} until the either Dynamic Temperature shutdown (ΔT_{DYN})

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or Absolute temperature shut off (T_{TSD}) is reached. These thermal shutdown mechanisms are accompanied by ΔT_{DYN_HYS} or T_{TSD_HYS} hysteresis respectively. Both thermal shutdown events have equal priority and both need to be cleared for the driver to attempt to retry. The channel henceforth behaves as normal auto-restart, current limiting device. The STATUS pin is pulled low only at the event of Absolute Overtemperature T_{TSD} is reached. The STATUS pin is released when both dynamic temperature shutdown hysteresis and absolute temperature STATUS reset conditions are cleared (see Section 6.4.5)

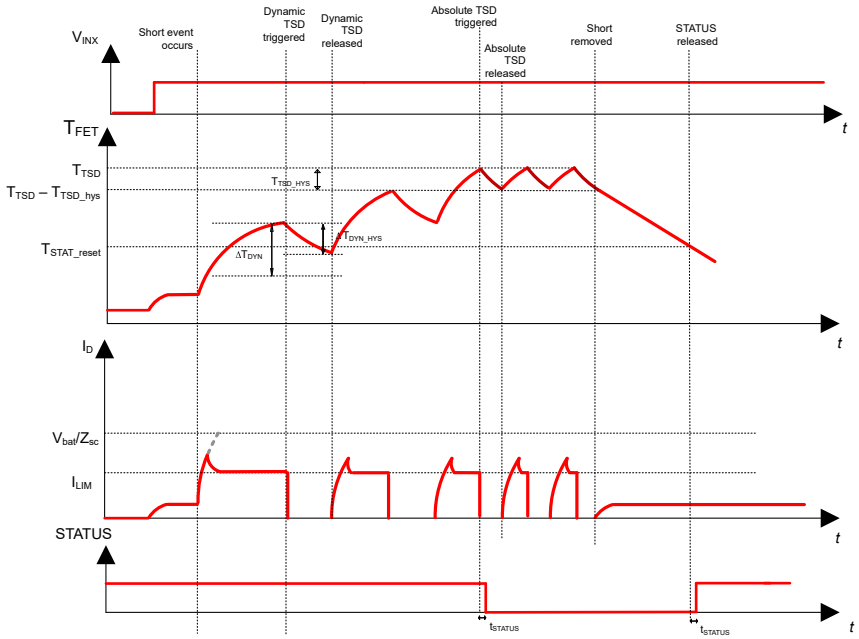


Figure 6-8. Overcurrent limit circuit operation in event of short

6.4.3 Thermal Shutdown (TSD)

To protect power stage from overheat the device incorporates an absolute (T_{TSD}) and a dynamic temperature limitation (ΔT_{DYN}). Triggering one of them causes the output to switch off and retry.

6.4.3.1 Dynamic Overtemperature Stress (ΔT_{DYN})

Thermal overstress can occur when huge temperature gradients happen across two points on the die. The dynamic temperature limitation enables a more controlled increment in FET temperature in high power dissipating events such as current limit by comparing relative temperature delta between FET and cooler parts of die. Dynamic overtemperature events do not result in STATUS going low. However a prevailing dynamic overtemperature condition can gate the recovery of STATUS.

6.4.3.2 Absolute Overtemperature

Aside from the dynamic temperature protection and monitoring, the FET also has an absolute temperature sensor. The triggering of this sensor also results in a channel shut off, followed by the STATUS pulled low. The channel retries once the temperature falls below T_{TSD_hys}.

Note

Only Absolute overtemperature events can cause the STATUS to go low. Recovery of the STATUS pin however can happen only if the Dynamic Overtemperature sensor has fallen below ΔT_{DYN} - ΔT_{DYN_hys} and the FET temperature sensor falls below T_{TSD_reset}

The STATUS pin is pulled low to indicate an absolute overtemperature event. The STATUS pin is released once the temperature falls below T_{TSD_reset}. The STATUS pin is released after the temperature returning to < T_{TSD_RESET} in DRV81315A but stays latched low till IN pin is pulled low in DRV81315.

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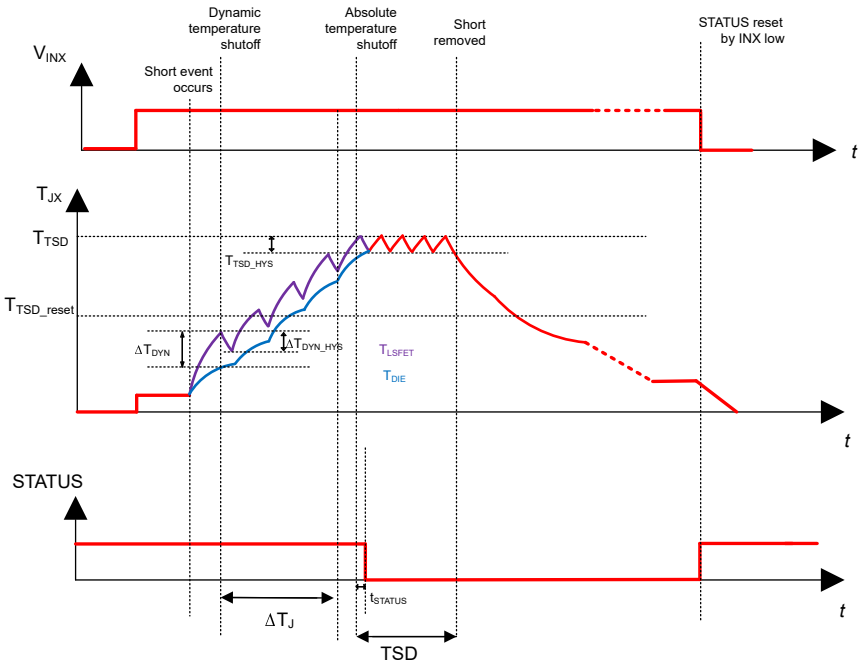


Figure 6-9. Overtemperature Protection(DRV81315)

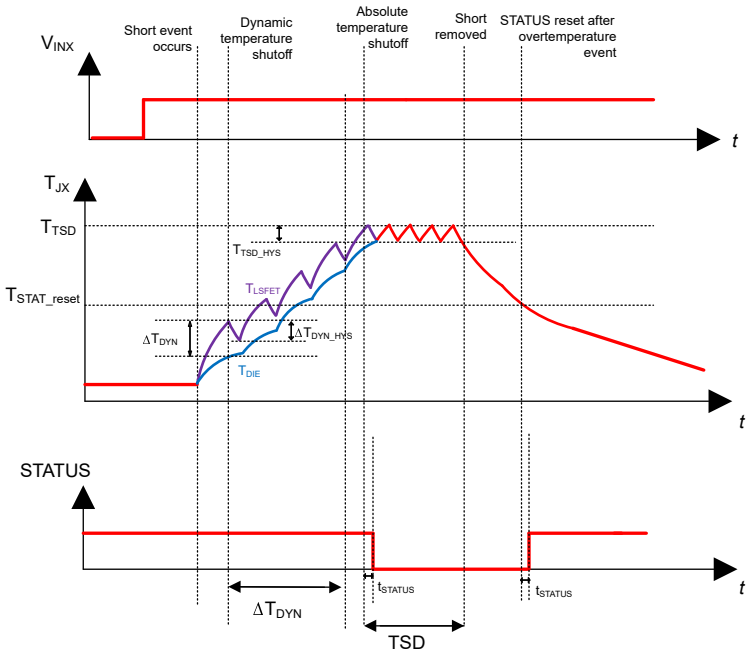


Figure 6-10. Overtemperature Protection(DRV81315A)

6.4.4 Undervoltage Lockout (UVLO)

If at any time the voltage on the supply pin (INx for DRV81315, VDD for DRV81315A) pin falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled, and internal logic is reset. Operation resumes when supply pin rises above the UVLO threshold. There is no indication on the STATUS pin.

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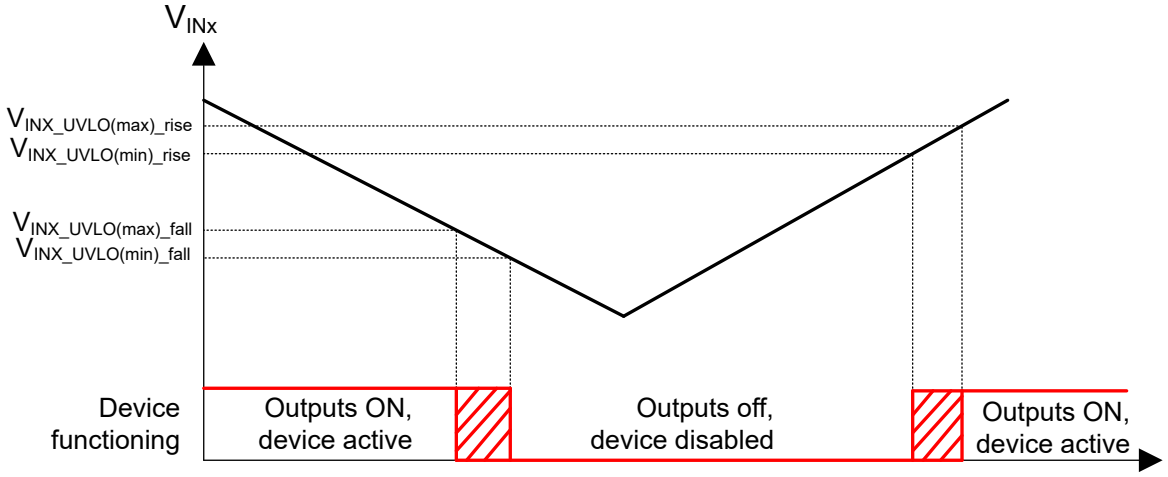


Figure 6-11. DRV81315 UVLO device response

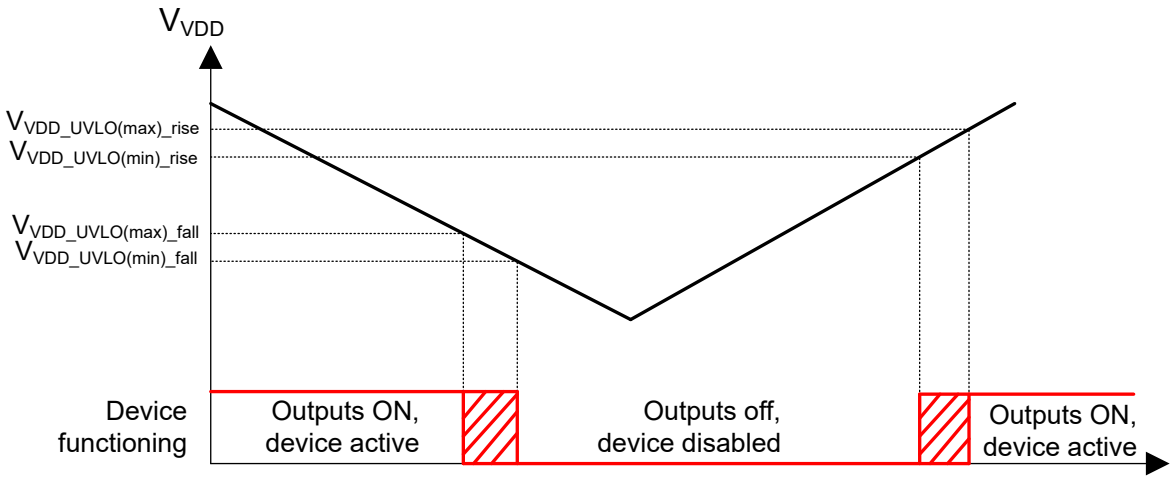


Figure 6-12. DRV81315A UVLO device response

6.4.5 Summary of STATUS pin response

Table 6-1. Summary of STATUS pin response for DRV81315A

T_{FET} (1) > T_{TSD}	T_{STAT_reset} < T_{FET} < T_{TSD} - T_{TSD_hys}	T_{FET} < T_{STAT_reset}	ΔT (2) > ΔT_{DYN}	ΔT < ΔT_{DYN} – ΔT_{DYN_hys}	OUT response	STATUS
✓	✖	✖	✖	✓	Off	Low
✖	✓	✖	✖	✓	On	Low
✖	✖	✓	✖	✓	On	High
✖	✖	✖	✖	✓	On	High
✓	✖	✖	✓	✖	Off	Low
✖	✓	✖	✓	✖	Off	Low
✖	✖	✓	✓	✖	Off	Low
✖	✖	✖	✓	✖	Off	High

(1) T_{FET} denotes FET temperature
(2) $\Delta T = T_{FET} - T_{controller}$

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Table 6-2. Summary of STATUS pin response for DRV81315

T_{FET} (1)> T_{TSD}	T_{STAT_reset} < T_{FET} < T_{TSD} - T_{TSD_hys}	T_{FET} <T_{STAT_reset}	ΔT(2) >ΔT_{DYN}	ΔT < ΔT_{DYN}– ΔT_{DYN_hys}	OUTresponse	STATUS
✓	✖	✖	✖	✓	Off	Low
✖	✓	✖	✖	✓	On	Low
✖	✖	✓	✖	✓	On	Low(3)
✖	✖	✖	✖	✓	On	High
✓	✖	✖	✓	✖	Off	Low
✖	✓	✖	✓	✖	Off	Low
✖	✖	✓	✓	✖	Off	Low
✖	✖	✖	✓	✖	Off	High

(1) T_{FET} denotes FET temperature
(2) $\Delta T = T_{FET} - T_{controller}$
(3) Latched low till IN is toggled

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Typical Application

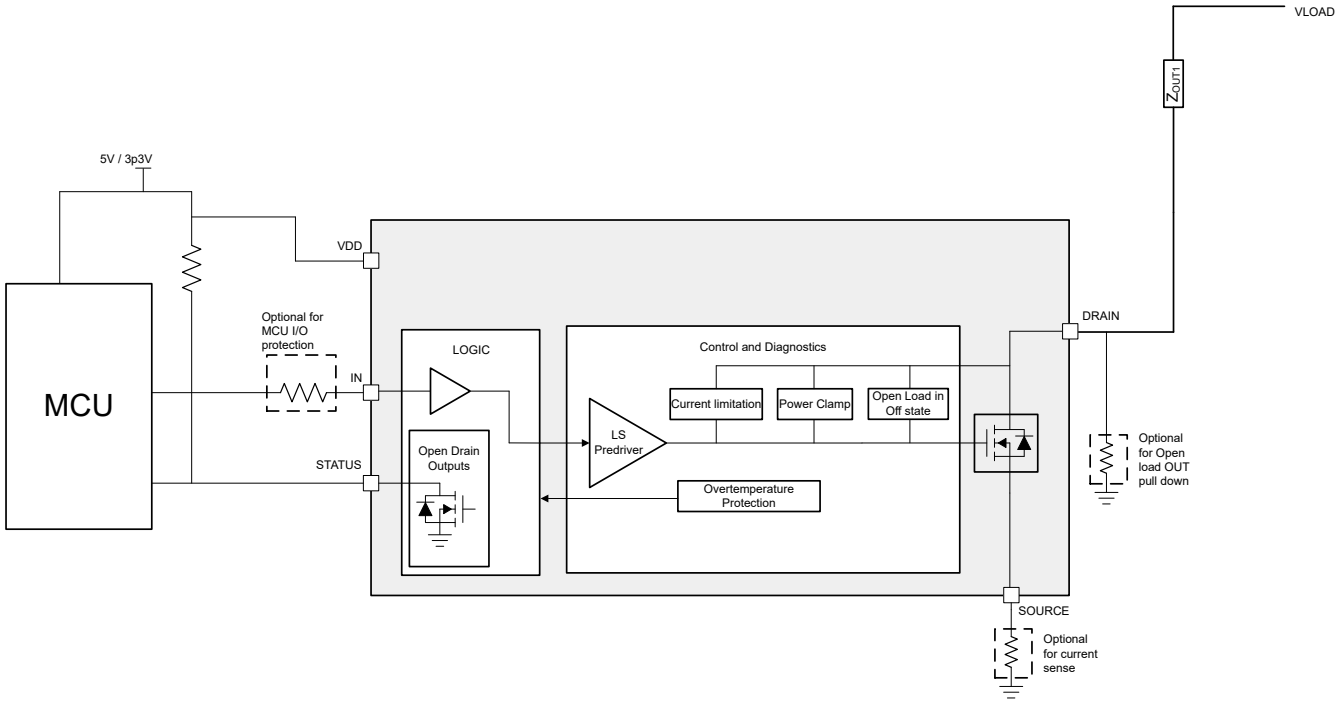


Figure 7-1. Typical Application Schematic of DRV81315A

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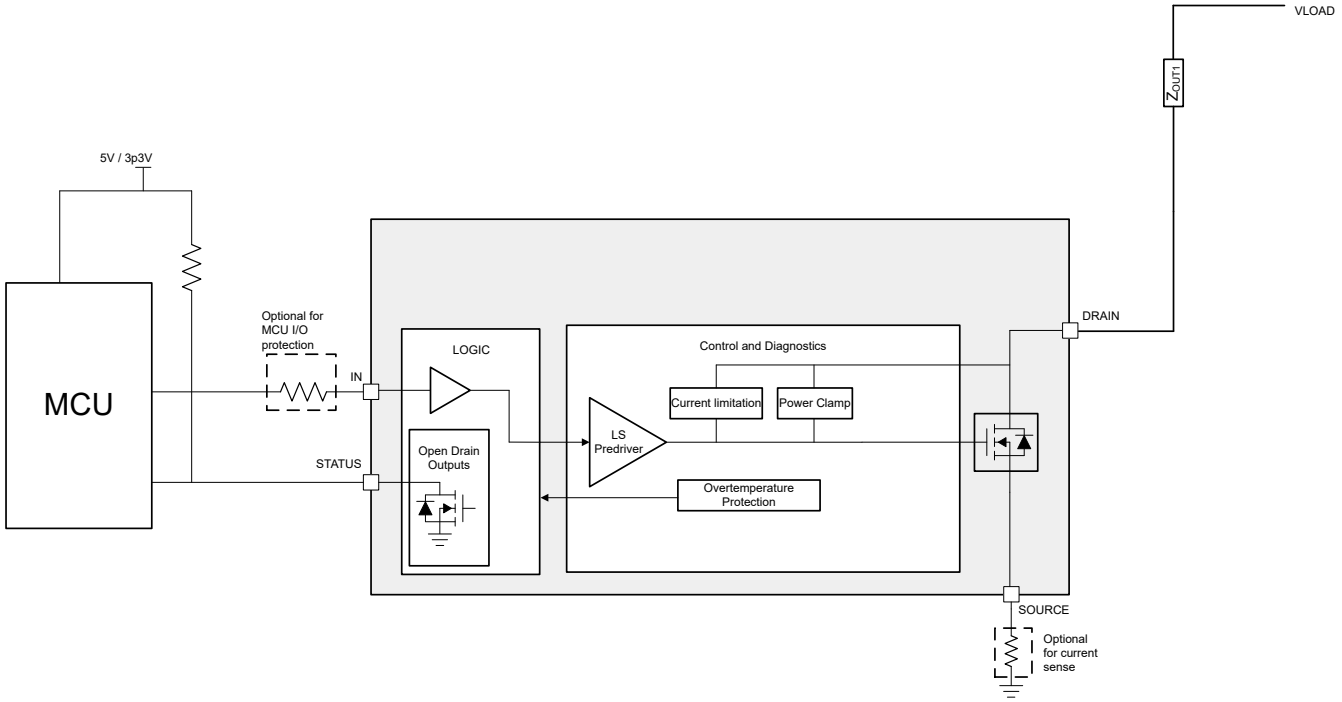


Figure 7-2. Typical Application Schematic of DRV81315

7.1.1 External components

Following table shows recommended external components for the DRV81315/A-Q1

Table 7-1. Required External components

Symbol	Description	Value	Purpose
R_{STATUS}	Pull up resistor on STATUS	10kΩ	Bias the STATUS voltage to high when the pin is not pulled low.

Table 7-2. Optional External components

Symbol	Description	Value	Purpose
C_{OUT}	Capacitor on each OUTx relative to SOURCEx	<10nF	Filtering for system level ESD
R_{SNS}	Shunt sense resistor between SOURCEx and GND	<200mΩ	Optional Resistor at SOURCE pin for sensing of load current
R_{series}	Series resistor to prevent MCU latchup	<500Ω	MCU I/O protection

7.2 Layout

7.2.1 Layout Guidelines

Small-value capacitors must be ceramic, and placed closely to device pins.

The DRV81315/A DDA package uses an HSOIC package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding several vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the

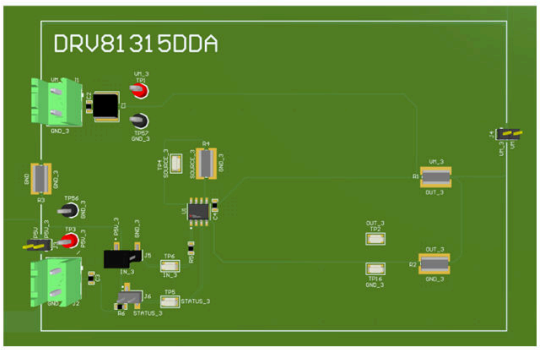
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opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

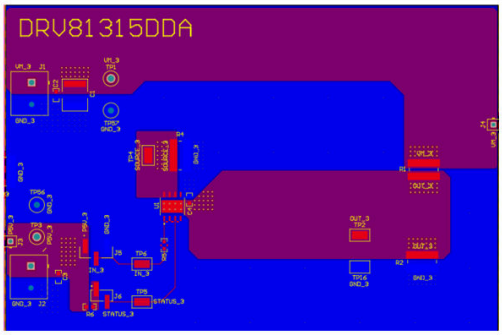
For details about how to design the PCB, see the TI Application note, *PowerPAD Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

The DRV81315ADRL package benefits from a very good junction to top, junction to Board thermal resistance parameter. To achieve good thermal performance, connecting the OUT and SOURCE pins to large copper pour is beneficial. On the top PCB layer, the pour can extend beyond the package dimensions. In addition to this, having a OUT plane on one or more internal PCB layers and/or on the bottom layer is recommended. Vias must connect these planes to the top OUT pour. The SOURCE pin can electrically be connected to the board GND and vias to the GND layer can help improve the performance

7.2.2 Layout Example



Top Signal Layer



Second Layer (GND)

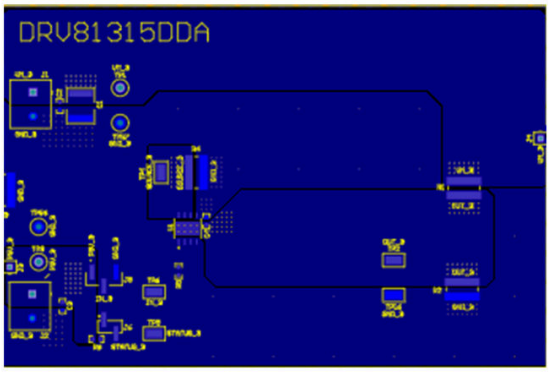


Figure 7-3. DDA package (Power Pad) in 2s2p (only top and second planes shown)

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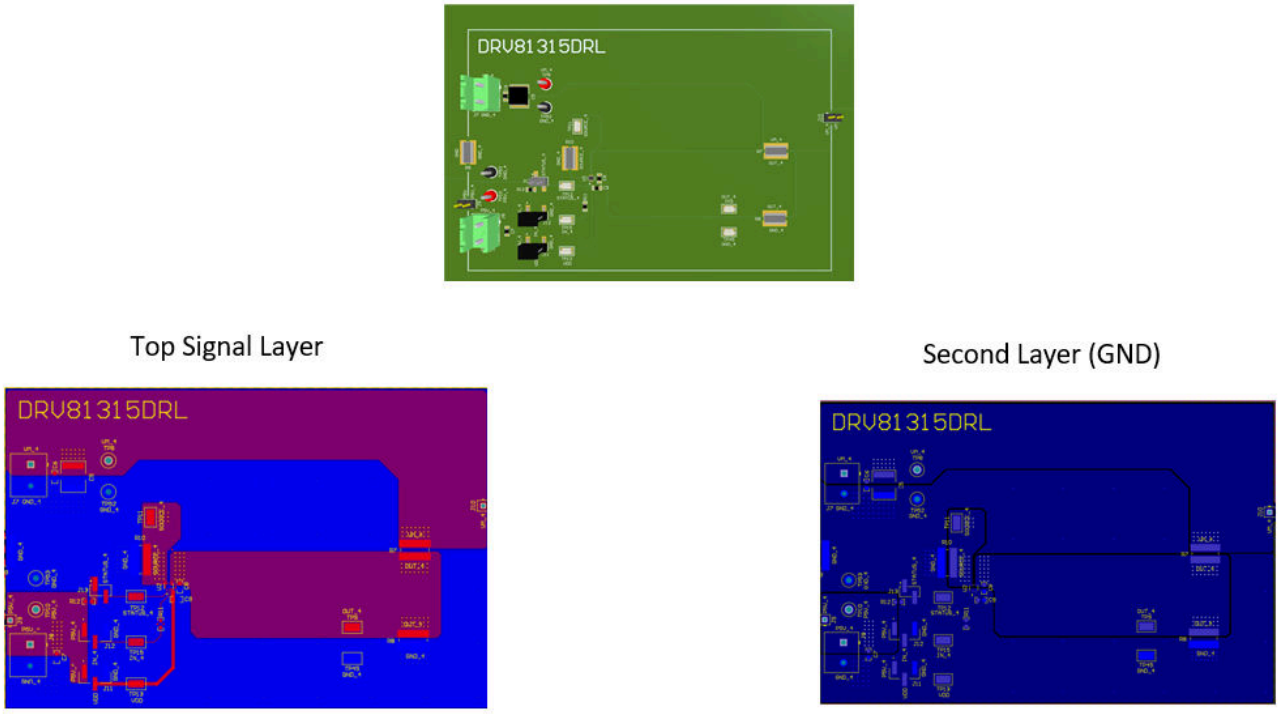


Figure 7-4. DRL package in 2s2p (only top and second planes shown)

7.3 Thermal Consideration

7.3.1 Power Dissipation

Power dissipation in the DRV81315 device has two components

Static power dissipation : Power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 4:

$$P = R_{DS(ON)} \cdot (I_{OUT})^2 \quad (4)$$

Where:

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and the duration.

Switching Power dissipation : Power dissipated in the Output FET when the FET is turned ON/OFF while maintaining a load current (PWM operation). The power dissipated follows the equation below :

$$P_{sw} = P_{sw_reg} + P_{sw_clamp}$$

$$P_{sw_reg} = 0.5 \times V_{load} \times I_{load} \times (tr + tf) \times F_{sw}$$

$$P_{sw_clamp} = E_{AS} * F_{sw}$$

where:

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- P_{sw} is the switching power dissipation of one FET
- V_{load} is the load supply
- I_{load} is the load current
- t_r and t_f denote the rise and fall times at the output
- F_{sw} is the switching frequency
- E_{AS} is the inductive demagnetization energy

Note

The component P_{sw_clamp} is relevant only in case of the integrated output clamp of the DRV813XX being used. An external recirculation path (such as a recirculation diode) being present eliminates the need to consider this component.

When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002.
- *PowerPAD Made Easy*, SLMA004.

8.2 Community Resources

8.3 Trademarks

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV81315AQDRLRQ1	Active	Preproduction	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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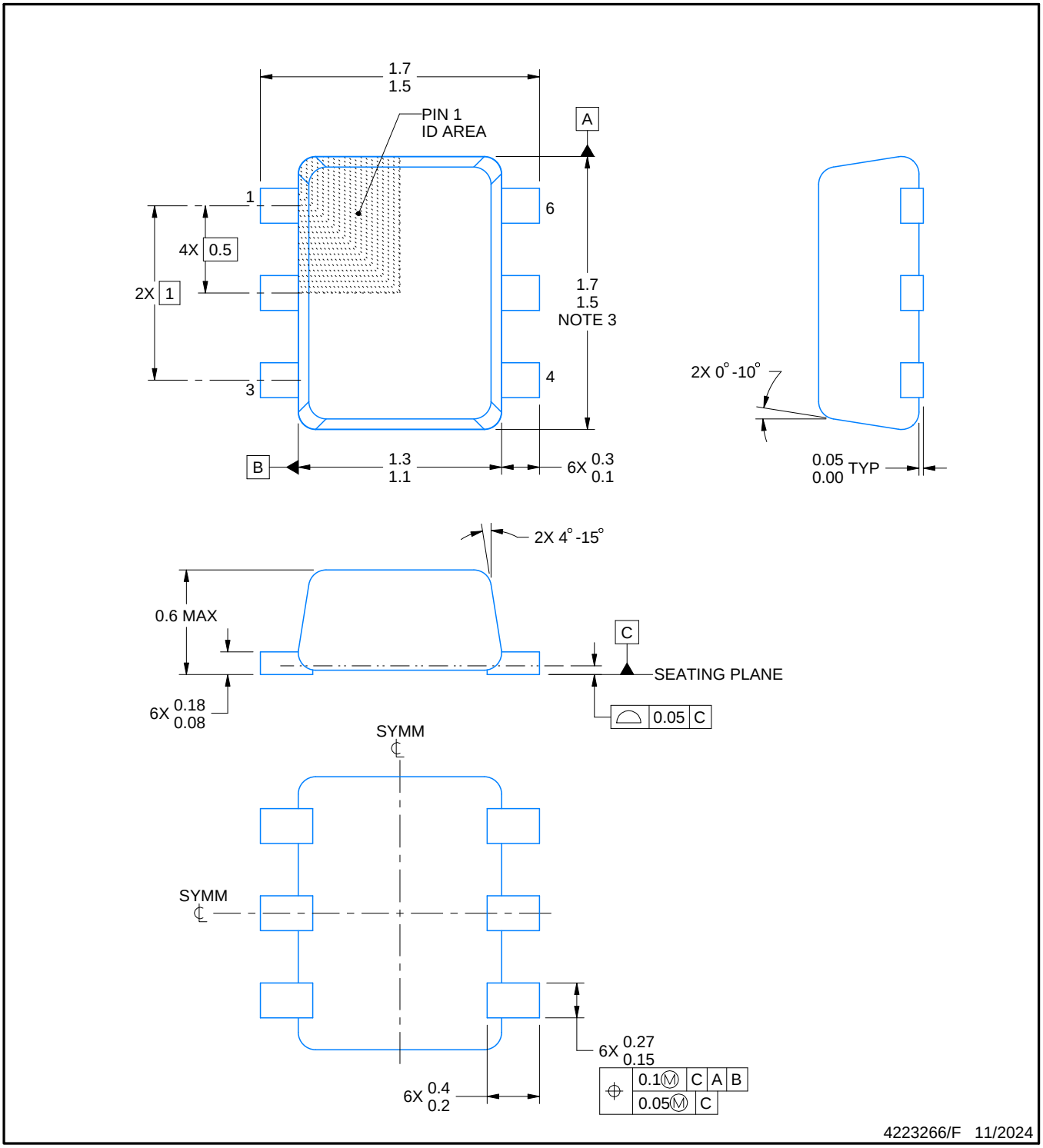


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

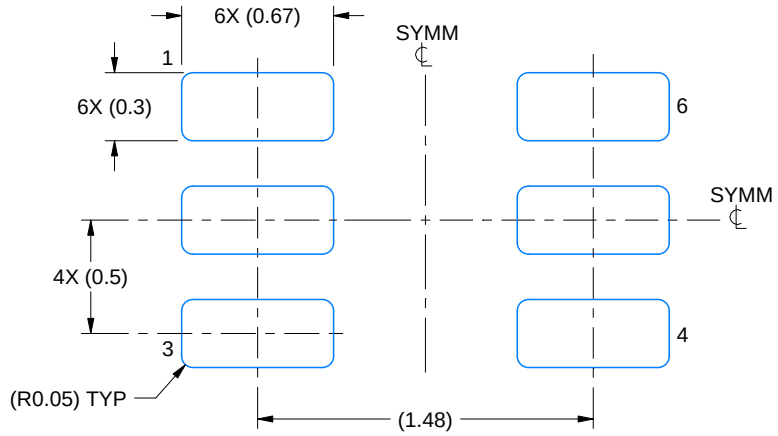
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

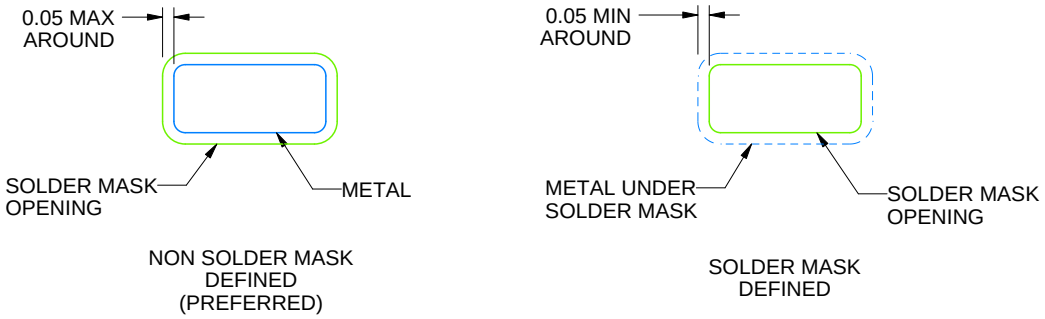
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

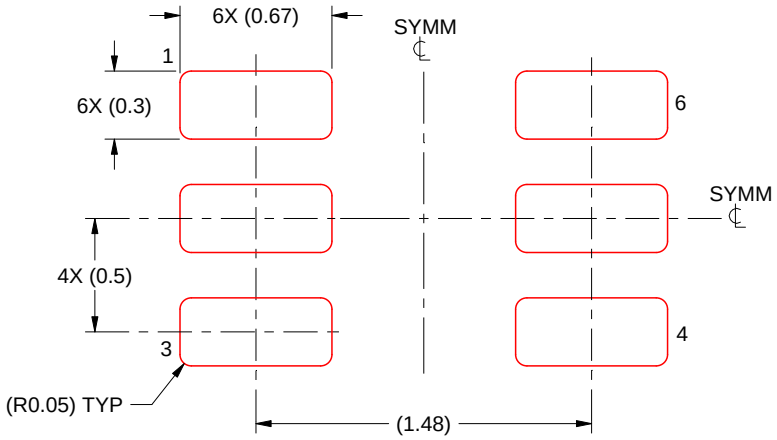
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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