# DRV81325/A -Q1 Dual Channel Protected Low-side Switches

## 1 Features

- Dual Protected Integrated Low Side switches
  - **110mΩ $R_{DS(ON)}$** at 25°C
  - Output Stage upto **40V operating tolerance**
- AEC-Q100 Qualified (up to Grade 1)
- Hardware control interface
- Fully Protected
  - **Internal current limit** for each switch
  - **Independent Overtemperature** protection for each switch
    - Dynamic and absolute overtemperature protection
  - **Integrated Overvoltage clamps** for inductive load discharge
- **Diagnostic feedback** (DRV81325A)
  - MCU Fault interrupt signal (STATUS) available per channel
- **2.6V to 5.5V input** Voltage operating range
  - Supports **3p3V, 5V MCU** I/O control
- Non Thermally Enhanced Surface mount package **(D-SOIC8)** , Thermally Enhanced Surface mount package **(DDA8)**

## 2 Applications

- Engine and Transmission
- Lighting
- Braking and Suspension
- Body Electronics and Zonal modules
- Battery management system

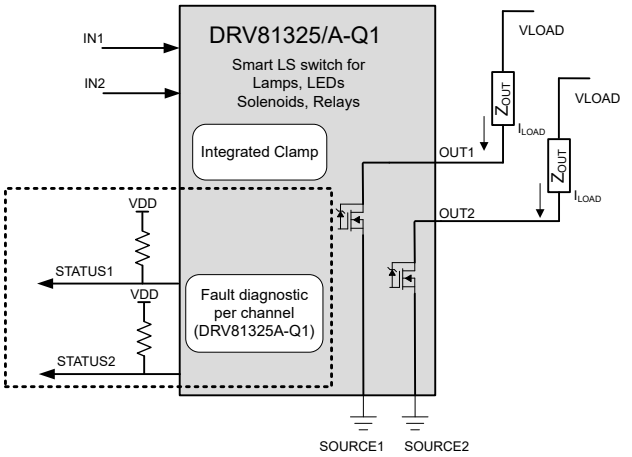
## 3 Description

The DRV81325/A -Q1 integrates two protected low side switches with a low $R_{DS(ON)}$ of 110mΩ. The device can be controlled by means of a GPIO interface. Each channel is protected against over current by means of an internal fixed threshold current limit. Channels are protected against overtemperature by integrated overtemperature sensor. Each channel has integrated output overvoltage protection for inductive load demagnetization. The protection features of each individual channel work independent of other channel. Fault report are available per each channel as an open drain STATUS output (A variant). The DRV81325/A-Q1 is available in 8-pin SOIC(D) package and 8-pin HSOIC(DDA) thermally enhanced package (Eco-friendly: RoHS & no Sb/Br).

**Device Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV81325ADDA(2) | HSOIC (8) | 4.90 mm × 3.90 mm |
| DRV81325AD | SOIC (8) | 4.90 mm × 3.90 mm |
| DRV81325D(2) | SOIC (8) | 4.90 mm × 3.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview Product




**Simplified Schematic**

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# 4 Pin Configuration and Functions

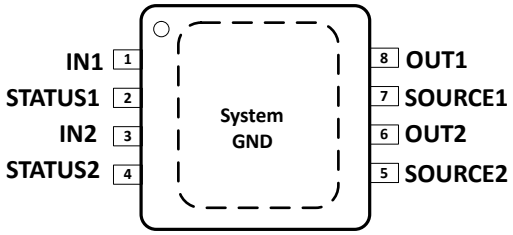


**Figure 4-1. DRV81325A-Q1 DDA Package 8-Pin HSOIC Top View**

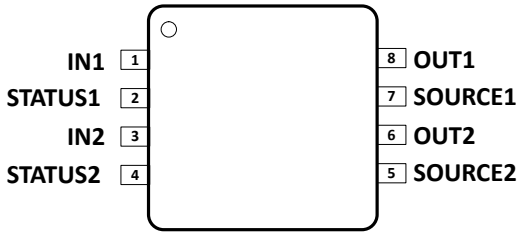


**Figure 4-2. DRV81325A-Q1 D Package 8-Pin SOIC Top View**

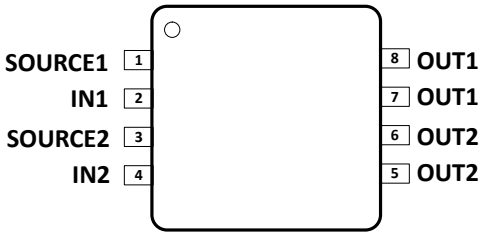


**Figure 4-3. DRV81325-Q1 D Package 8-Pin SOIC Top View**

## Pin Functions

| PIN | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DRV81325A | | DRV81325 | | |
| | DDA(8) | D(8) | D(8) | | |
| IN1 | 1 | 1 | 2 | P/I | Input channel 1 |
| IN2 | 3 | 3 | 4 | P/I | Input channel 2 |
| STATUS1 | 2 | 2 | - | O | Diagnostic output 1 |
| STATUS2 | 4 | 4 | - | O | Diagnostic output 2 |
| OUT1 | 8 | 8 | 7,8 | O | Power FET Drain 1 |
| OUT2 | 6 | 6 | 5,6 | O | Power FET Drain 2 |
| SOURCE1 | 7 | 7 | 1 | G | Power FET source and ground reference for channel 1 |
| SOURCE2 | 5 | 5 | 3 | G | Power FET source and ground reference for channel 2 |

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# 5 Specification

## 5.1 Absolute Maximum Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $IN_X$ | Input Supply/logic Voltage | | 5.75 | V |
| $V_{OUT}$ | Output tolerance | –0.3 | Internally limited | V |
| $V_{SRC1\_SRC2}$ | Potential difference between SOURCE1 and SOURCE2 | -0.5 | 0.5 | V |
| $V_{OUT\_SC}$ | Output Voltage for Short Circuit tolerance | | 28 | V |
| $E_{AS\_sp}$ | Single pulse Energy capability<br>$T_A$ = 125 C ,$R_L$=17Ω, L = 100mH, $V_{LOAD}$=14V | | 50 | mJ |
| $E_{AS\_Rep\_p}$ | Inductive clamp energy<br>for 2M cycles $T_A$ = 105C ,$R_L$=24Ω, L = 100mH, $V_{LOAD}$=14V | | 20 | mJ |
| STATUS | Digital output pin voltage | –0.5 | 5.75 | V |
| $I_{peak}$ | Peak drive output current | Internally limited | | A |
| $P_{dis}$ | Continuous total power dissipation | See *Thermal Information* | | W |
| $T_J$ | Operating virtual junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –60 | 150 | °C |

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{INX}$ | Power supply voltage | | 3 | | 5.5 | V |
| $V_{LOAD}$ | Battery voltage during normal operation | | 6 | | 18 | V |
| $T_{AMB}$ | Operating Ambient temperature | | -40 | | 125 | °C |
| $T_J$ | Operating junction temperature | | -40 | | 150 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | DDA (HSOIC-8) | D (SOIC-8) | UNIT |
|---|---|---|---|---|
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 45.4*[1] | 118.4* | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 58.0* | 54.0* | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 20.3* | 62.5* | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.4* | 13.0* | °C/W |

[1] * Values are initial estimates

| THERMAL METRIC(1) | | DDA (HSOIC-8) | D (SOIC-8) | UNIT |
|---|---|---|---|---|
| | | 8 PINS | 8 PINS | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 20.3* | 61.7* | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.1* | NA | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics

Typical values are at $T_A$ = 25°C , $V_{IN}$ = 5V unless otherwise noted. All limits are over recommended operating conditions, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES(IN1,IN2)** | | | | | | |
| $I_{INx\_norm}$ | Control input current draw in normal operation | INx = 1 | 25 | 40 | 65 | µA |
| $I_{INx\_fault}$ | Control input current draw in abnormal operation (Current limit) | INx = 1 | | | 400 | µA |
| $V_{INx\_uvlo\_rise}$ | IN undervoltage rising | | 2.5 | | 2.9 | V |
| $V_{INx\_uvlo\_fall}$ | IN undervoltage falling | | 2.3 | | 2.6 | V |
| **STATUS OUTPUT(STATUS1, STATUS2)(DRV81325A)** | | | | | | |
| $V_{STAT\_L}$ | Status output low voltage | $I_{STAT}$= 1mA | | | 0.4 | V |
| $I_{STAT\_H}$ | Status high leakage current | $V_{STAT}$ = 5V | | | 1 | µA |
| **OUTPUT STAGE** | | | | | | |
| $R_{DS(ON)}$ | FET on resistance | $I_O$ = 1A , $T_J$ = 25°C , $V_{INx}$=3V, DRV81325A | | 125 | | mΩ |
| | | $I_O$ = 1A , $T_J$ = 25°C, $V_{INx}$=3V, DRV81325 | | | | |
| | | $I_O$ = 1A, $T_J$ = 150°C , $V_{INx}$=3V, DRV81325A | | | 250 | |
| | | $I_O$ = 1A , $T_J$ = 150°C, $V_{INx}$=3V, DRV81325 | | | | |
| $R_{DS(ON)}$ | FET on resistance | $I_O$ = 1A , $T_J$ = 25°C , $V_{INx}$=5V, DRV81325A | | 110 | | |
| | | $I_O$ = 1A , $T_J$ = 25°C, $V_{INx}$=5V, DRV81325 | | | | |
| | | $I_O$ = 1A, $T_J$ = 150°C , $V_{INx}$=5V, DRV81325A | | | 220 | |
| | | $I_O$ = 1A , $T_J$ = 150°C, $V_{INx}$=5V, DRV81325 | | | | |
| $I_{OFF}$ | Off-state leakage current | $V_{OUT}$ = 18 V, $T_J$ = 150°C | | | 5 | µA |
| $V_F$ | Body diode forward voltage | $I_O$ = -1A | | 0.8 | | V |
| $V_{CLTH\_LT}$ | Drain source clamping voltage threshold | $I_{OUT}$ = 10 mA , $T_J$ = -40°C | 40 | | | V |
| $V_{CLAMP}$ | Drain source clamping voltage | $I_{OUT}$ = 1.5 A , $T_J$ = 150°C | 41 | | 45 | V |
| **SWITCHING** | | | | | | |
| $t_R$ | Rise time | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=3V | 20 | 30 | 40 | µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=5V | 20 | 30 | 40 | |
| $t_F$ | Fall time | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=3V | 30 | 60 | 120 | µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=5V | 15 | 25 | 50 | |

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Typical values are at $T_A$ = 25°C , $V_{IN}$ = 5V unless otherwise noted. All limits are over recommended operating conditions, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $SR_{rise}$ | Rising slew rate | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, VOUT = 30% $V_{LOAD}$ to 70% $V_{LOAD}$, $V_{INx}$=3V | 0.3 | 0.5 | 0.7 | V/µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, VOUT = 30% $V_{LOAD}$ to 70% $V_{LOAD}$, $V_{INx}$=5V | 0.3 | 0.5 | 0.7 | |
| $SR_{fall}$ | Falling slew rate | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, VOUT = 30% $V_{LOAD}$ to 70% $V_{LOAD}$, $V_{INx}$=3V | 0.1 | 0.25 | 0.4 | V/µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, VOUT = 30% $V_{LOAD}$ to 70% $V_{LOAD}$, $V_{INx}$=5V | 0.3 | 0.5 | 0.7 | |
| $t_{PD\_L\_to\_H}$ | Propogation Delay , Input Low to Output High | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=3V | 20 | 33 | 40 | µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=5V | 20 | 33 | 40 | |
| $t_{PD\_H\_to\_L}$ | Propogation Delay, Input High to Output Low | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=3V | 18 | 25 | 45 | µs |
| | | $V_{LOAD}$ = 13V; $R_L$ = 13Ω, $V_{INx}$=5V | 18 | 25 | 45 | |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{LIM}$ | Current limitation value | $V_{INx}$= 5, $T_J$ = 25°C , DDA package | | 7.8 | 10 | A |
| | | $V_{INx}$= 5, $T_J$ = 125°C , DDA package | 5.5 | | | A |
| | | $V_{INx}$= 5, $T_J$ = 25°C , D package | | 4.7 | 6 | A |
| | | $V_{INx}$= 5, $T_J$ = 125°C , D package | 3 | | | A |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 175 | 200 | °C |
| $T_{TSD\_hys}$ | Thermal shutdown temperature hysteresis | | | 7 | | °C |
| $T_{STAT\_reset}$ | Thermal reset of Status | DRV81325A | 135 | | | °C |
| $\Delta T_J$ | Dynamic temperature | | | 40 | | °C |
| $\Delta T_{J\_HYS}$ | Dynamic temperature hysteresis | | | 15 | | °C |
| $t_{STATUS}$ | Overtemperature deglitch on STATUS pin | DRV81325A | | 20 | | µs |

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### Output timing diagrams

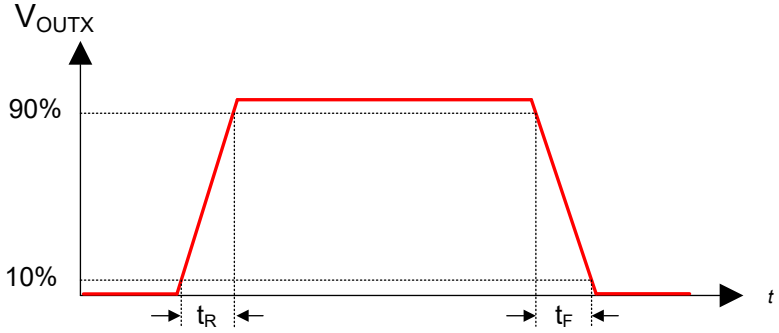


**Figure 5-1. Output rise/fall times**

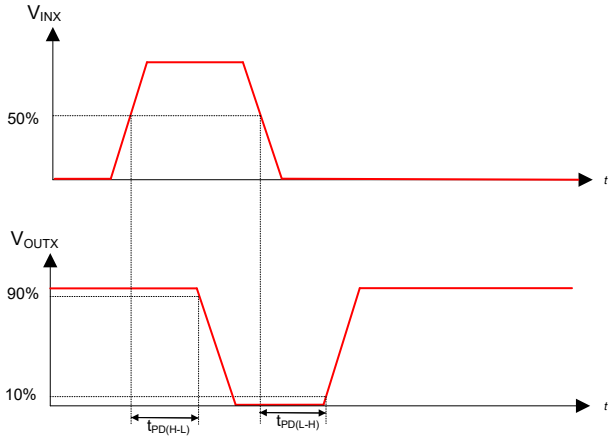


**Figure 5-2. Propogation delay**

## 5.6 Transient Thermal Impedance & Current Capability

*Information based on thermal simulations. Values are Initial estimates***

**Table 5-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability**

| PART NUMBER | PACKAGE | $R_{\theta JA}$ [°C/W](1) | | | | Current [A], only single channel conducting(2) | | | | Current [A], both channels conducting (per channel reported)(3) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 10 msec | 0.1 sec | 1 sec | DC | 0.01 sec | 0.1 sec | 1 sec | DC | 10 msec | 0.1 sec | 1 sec | DC |
| DRV81325A-Q1 | DDA (HSOIC 8) | 5 | 12 | 23 | 47 | 8.5 | 5.5 | 4 | 2.8 | 6.0 | 3.9 | 2.8 | 2.0 |
| | D (SOIC8 ) | 8 | 15 | 40 | 114 | 6.7 | 4.9 | 3.0 | 1.8 | 4.8 | 3.5 | 2.1 | 1.3 |
| DRV81325-Q1 | D (SOIC8 ) | 8 | 15 | 40 | 114 | 6.7 | 4.9 | 3.0 | 1.8 | 4.8 | 3.5 | 2.1 | 1.3 |

1. Based on thermal simulations using 114.3 x 76.2 x 1.6 mm, 4 layer PCB Section 7.4.2 – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 minimum mm via pitch.
2. Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C.
3. In parallel mode usage, this value of load current capability is effectively doubled. For instance if both channel together can conduct 1A each, when the channels are parallled, the paralleled output can support 2A.

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# 6 Detailed Description

## 6.1 Overview

The DRV81325/A -Q1 are dual channel low side switch drivers with each integrated switch of typical $R_{DS(ON)}$ 110mΩ. Each switch has integrated overvoltage protection for safe demagnetization of Inductive loads. The devices are powered over control pins INx per channel. Each channel is protected against over current by means of a fixed integrated current limit. Each channel further also has an overtemperature protection. Diagnostic feedback is available per channel over an open drain output STATUSx on the DRV81325A to alert the user of overtemperature condition on the Output. The DRV81325A is available in 8-pin HSOIC(DDA package) , 8-pin SOIC(D package). The DRV81325 is available in 8-pin SOIC(D package).

| Property | DRV81325A | DRV81325 |
|---|---|---|
| Package | DDA(HSOIC8), D(SOIC8) | D(SOIC8) |
| Diagnostic output (STATUS) | Y | N |

## 6.2 Functional Block Diagram

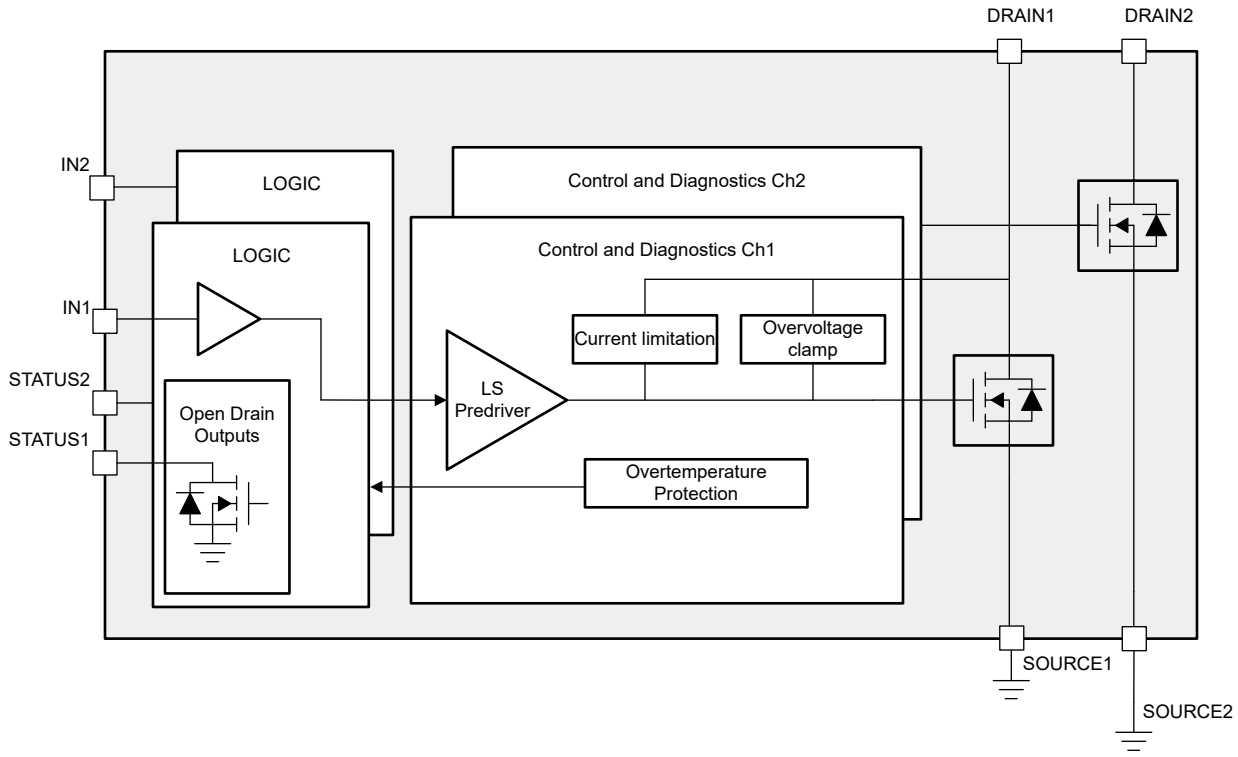


**Figure 6-1. DRV81325A-Q1 Functional Block Diagram**

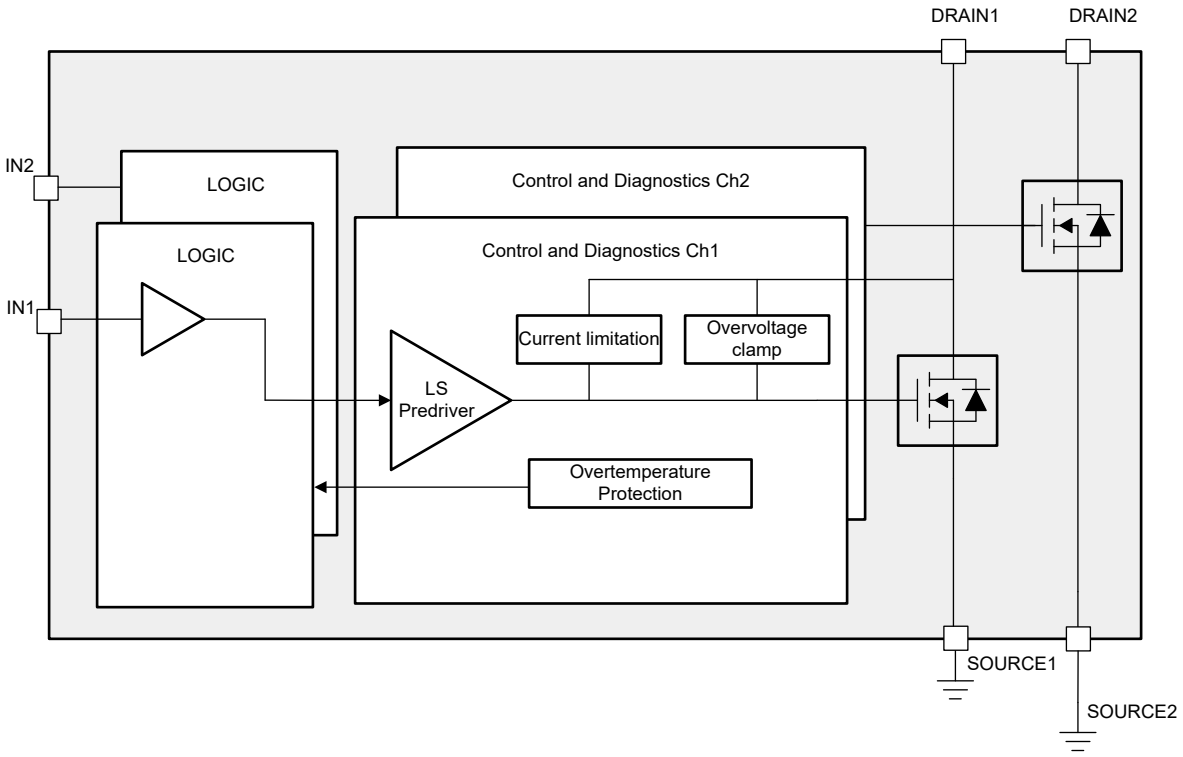


**Figure 6-2. DRV81325-Q1 Functional Block Diagram**

### *6.2.1 Control interface / Power input*

The DRV81325/A device does not have a dedicated supply pin. The circuits of each channel are powered over the corresponding control input. This pin behaves as a supply as well as a control input.

When logic high voltage is applied to this pin, the corresponding channel Output Low side FET is turned on and output is pulled low.

### *6.2.2 Shunt sensing support*

The source terminal of each MOSFET is exposed on the SOURCEx pins. An external sense resistor can be connected between a SOURCE pin and GND to measure the current on that channel as shown in figure

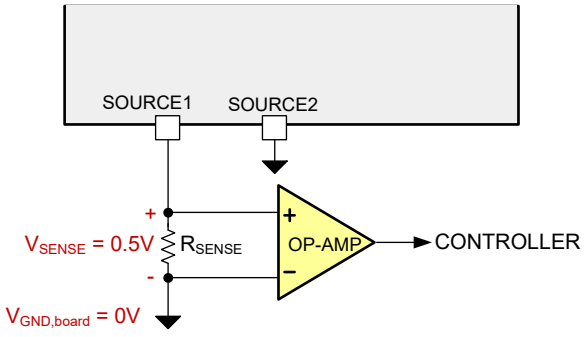


**Figure 6-3. SOURCEx Voltage With Respect to Board Ground Using Current Sense Resistor**

The SOURCEx pins must be connected directly to system GND if external current sensing is not used.

The Absolute Maximum Ratings for the SOURCEx pins set the maximum voltage across the shunt resistor to 0.5V. The shunt resistor must be sized so that at the highest load current the voltage across the sense resistor doesn't exceed 0.5V.

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### 6.2.3 Paralleling of channels

The DRV81325/DRV81325A-Q1 channels can be paralleled to support higher drive currents. The ON resistance of the paralleled output is effectively approximately 0.5*$R_{DS(ON)}$. The paralleling must be done at the board level by shorting the outputs and inputs. For the DRV81325A-Q1, TI recommends to also short the STATUS1 and STATUS2 pins.

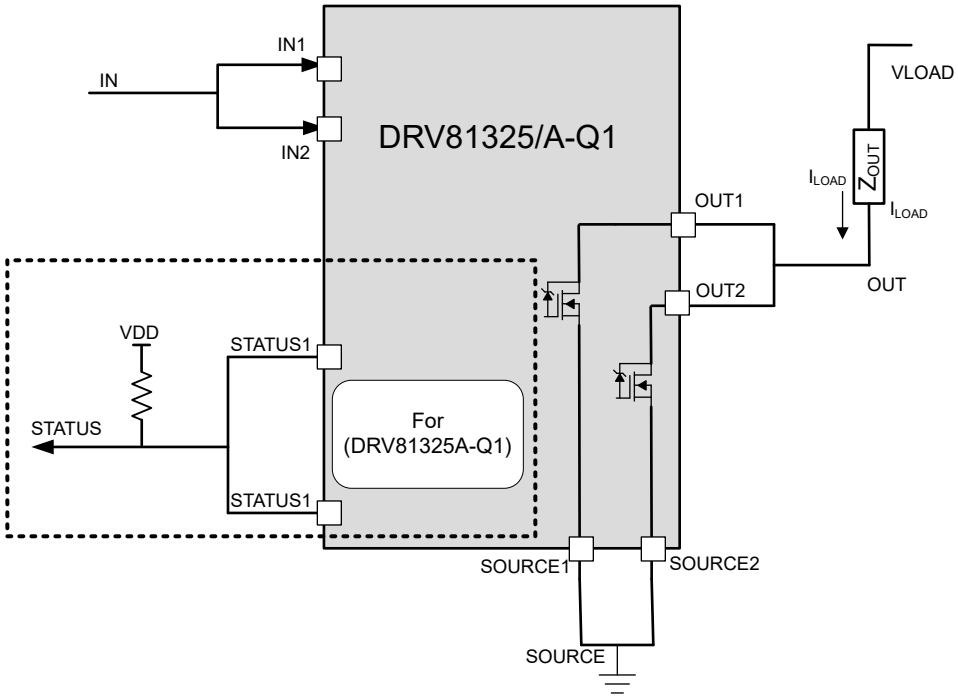


**Figure 6-4. Paralleling channels of DRV81325/DRV81325A-Q1**

## 6.3 Protection Circuits

The DRV81325/A -Q1 is Fully protected in Overcurrent , Overtemperature, FET Overvoltage and Undervoltage scenarios

### 6.3.1 Overvoltage clamp

When switching off inductive loads, voltage clamping is necessary to prevent device damage. The active clamping circuit consists of a zener stack connected between the Drain and the Gate. When the kickback voltage exceeds the Zener threshold , the kickback pushes current into the gate, forcing the FET to turn back on slightly in the saturation region. This dissipates the inductive energy directly inside the FET in a controlled manner.

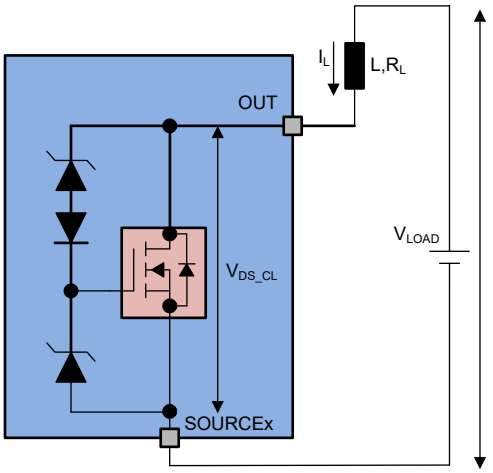


**Figure 6-5. Active overvoltage clamp**

#### 6.3.1.1 Demagnetization energy capability

During demagnetization of inductive loads, magnetic energy is dissipated in the DRV813xx-Q1 low-side switch. The equation shows how to calculate the energy for low-side switches when the low-side $V_{DS}$ clamp voltage is $V_{DS\_CL}$ , when the load (L, $R_L$ ) is carrying current $I_L$ and the other end of load is connected to $V_{LOAD}$:

$$E_{AS} = V_{DS\_CL} \times \left[ \frac{V_{LOAD} - V_{DS\_CL}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{LOAD} - V_{DS\_CL}}\right) + I_L \right] \times \frac{L}{R_L} \quad (1)$$

Under the assumption of $R_L$ = 0, this simplifies to

$$E_{AS} = \frac{1}{2} \times L \times {I_L}^2 \times \left(\frac{V_{DS\_CL}}{V_{DS\_CL} - V_{LOAD}}\right) \quad (2)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The $E_{AS\_sp}$ value provided in Section 5.1 denotes the single pulse energy handling capability per channel, while the $E_{AS\_Rep\_p}$ value provided in Section 5.1 denotes the repetitive pulse energy handling capability per channel.

### *6.3.2 Single pulse clamping capability*

The maximum energy and corresponding load inductance, load current the device can withstand for one pulse inductive dissipation at 125°C is shown here. The device can withstand 40% of this energy for one million inductive repetitive pulses with a lesser than 4-Hz repetitive pulse. If the application parameters exceed this device limit, use an external protection device like a freewheeling diode to dissipate the energy stored in the inductor

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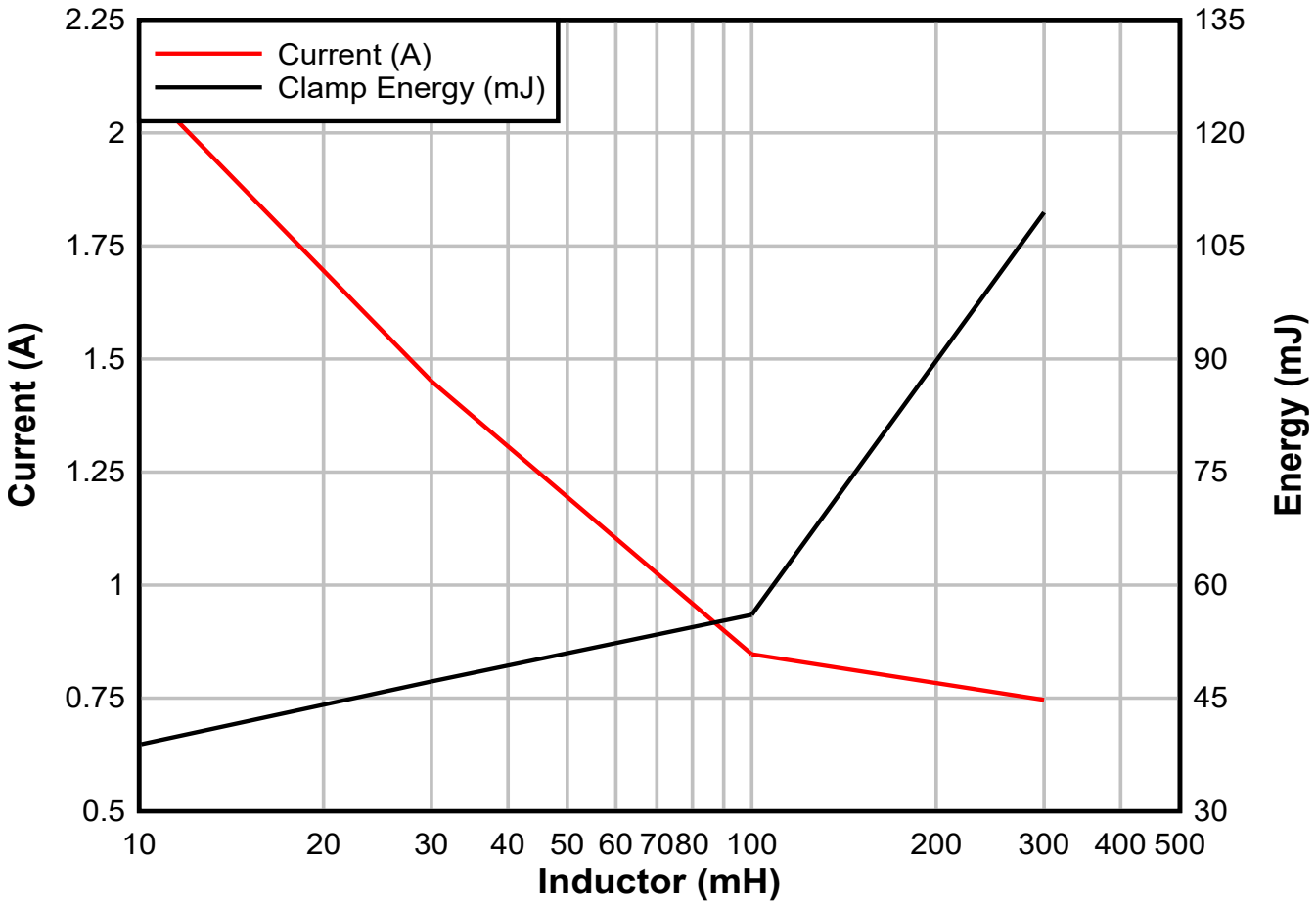


**Figure 6-6. Single pulse clamping energy (per channel) at 125C. $V_{LOAD}$ = 14V and $R_{LOAD}$ = $V_{LOAD}$ / Current(A)**

### *6.3.3 Overcurrent limit*

Overcurrent limitation is intended to protect against short circuit conditions while allowing inrush currents typical of loads such as lamps, motors and capacitive loads. When the sensed load current exceeds the limitation level $I_{LIM}$ , the gate drive of the low side FET is continually altered in closed loop to keep output current limited.

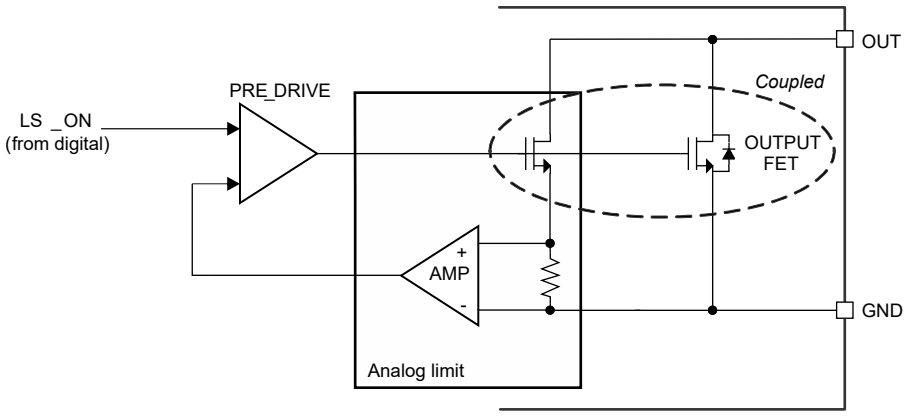


**Figure 6-7. Working of Current limit circuit**

The effect of this is a possible increase in the FET drain to source voltage and consequently a drastic increase in power dissipated. The FET keeps heating up at $I_{LIM}$ until the either Dynamic Temperature shutdown ($\Delta T_{DYN}$) or Absolute temperature shut off ($T_{TSD}$) is reached. These thermal shutdown mechanisms are accompanied by $\Delta T_{DYN\_HYS}$ or $T_{TSD\_HYS}$ hysteresis respectively. Both thermal shutdown events have equal priority and both need to be cleared for the driver to attempt to retry. The channel henceforth behaves as normal auto-restart, current limiting device. The STATUS pin is pulled low only at the event of Absolute Overtemperature $T_{TSD}$ is reached. The STATUS pin is released when both dynamic temperature shutdown hysteresis and absolute temperature STATUS reset conditions are cleared (see STATUS pin handling)

The current limit condition on one channel does not affect other channel, unless there is an event such as common over temperature (die level)

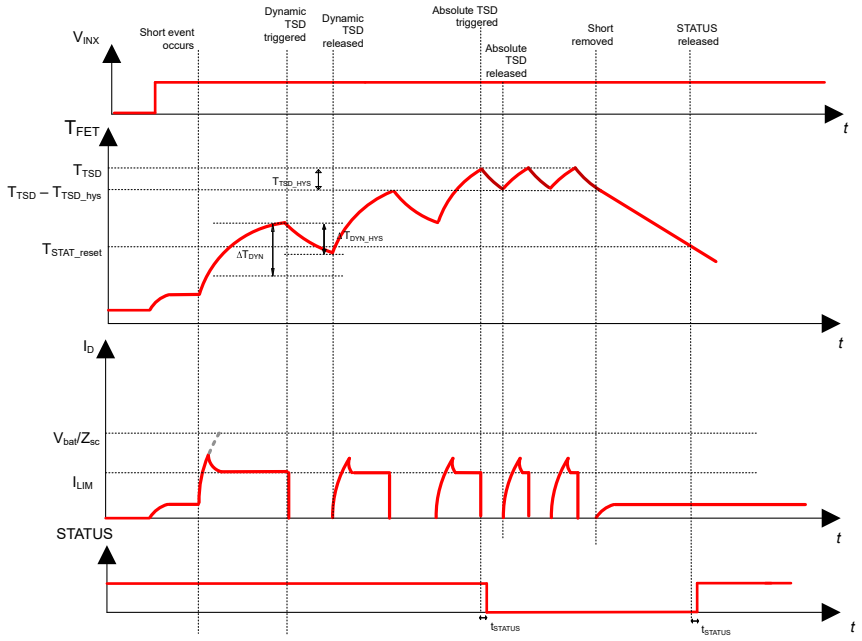


**Figure 6-8. Overcurrent limit circuit operation in event of short**

#### 6.3.3.1 Current limiting when channels paralleled

When the DRV81325/DRV81325A-Q1 channels are paralleled , there is no internal circuit that synchronizes the operation of the two individual channels. As a result when thermally stressful events such as current limit/inrush occur, there can be asymmetric heating and cooling of the two channels, the effect of which is a gradual skewing in time of the thermal shut off and retry behaviors. The user must therefore expect an effective steady state current limiting occurring at $1xI_{LIM}$.

The benefit of paralleling the two channels however does manifest as an effectively higher activation threshold for the current limiting behavior. This is due to the current splitting between the two channels when the channels are paralleled, which translates to a total of $2xI_{LIM}$, required to trip the individual current limits of either channel.

Figure 6-9 illustrates how the effective paralleled output current can look due to the skewing of thermal shut off and retry events of the individual channels

ADVANCE INFORMATION

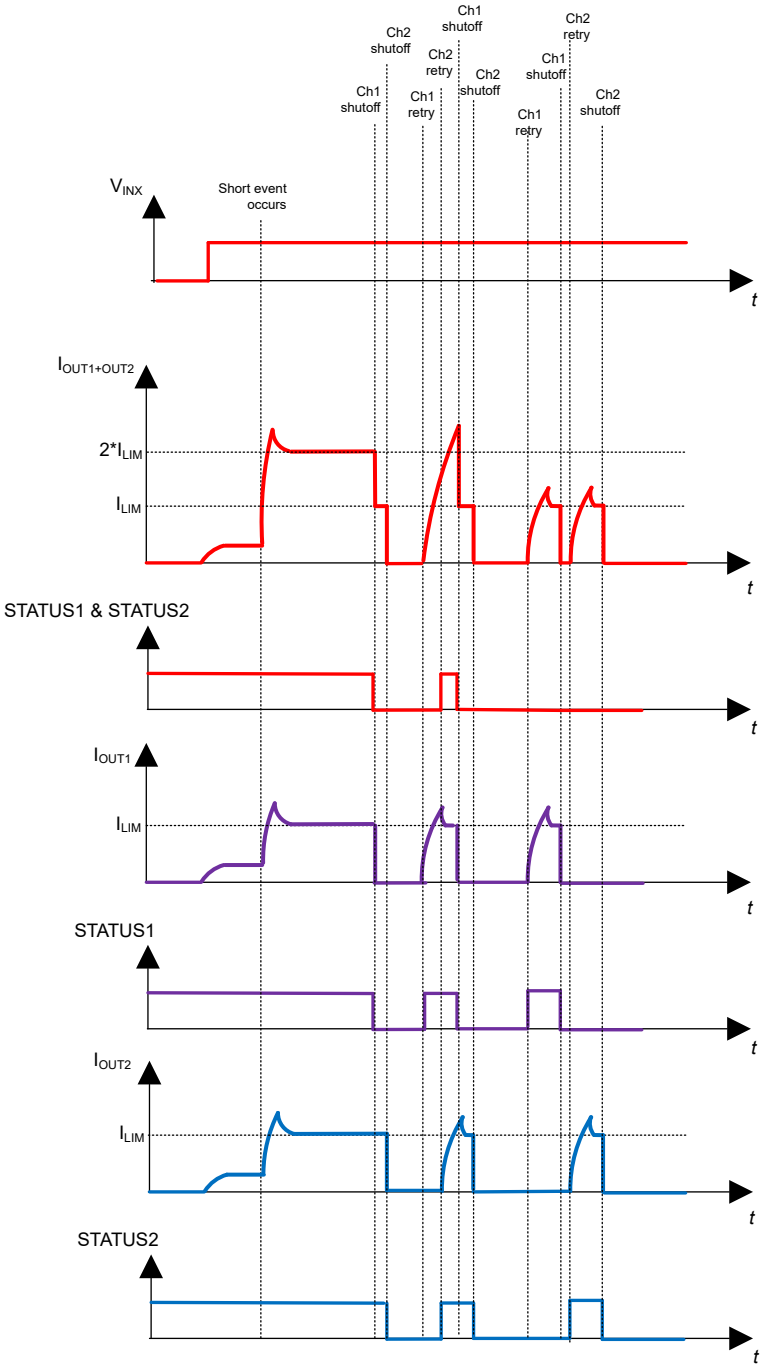


**Figure 6-9. Limited current in the paralleled output over time**

### *6.3.4 Thermal Shutdown (TSD)*

To protect power stage from overheat the device incorporates an absolute ($T_{TSD}$) and a dynamic temperature limitation ($\Delta T_{DYN}$). Triggering one of them causes the output to switch off and retry.

The thermal protection of both output power stages is independent

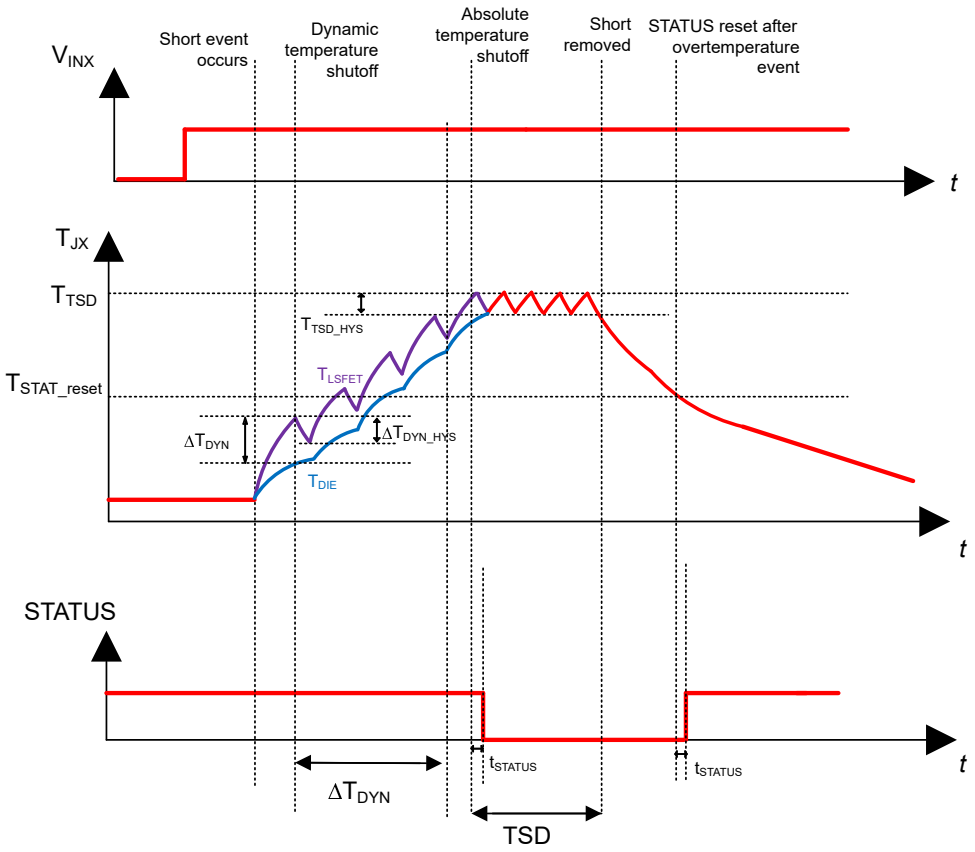


**Figure 6-10. Overtemperature Protection**

#### 6.3.4.1 Dynamic Overtemperature Stress ($\Delta T_{DYN}$)

Thermal overstress can occur when huge temperature gradients happen across two points on the die. The dynamic temperature limitation enables a more controlled increment in FET temperature in high power dissipating events such as current limit by comparing relative temperature delta between FET and cooler parts of die. Dynamic overtemperature events do not result in STATUS going low. However a prevailing dynamic overtemperature condition can gate the recovery of STATUS.

#### 6.3.4.2 Absolute Overtemperature (TSD)

Aside from the dynamic temperature protection and monitoring, the FET also has a absolute temperature sensor. Triggering this sensor results in a channel shut off, followed by the STATUS pulled low. The channel retries once the temperature falls below $T_{TSD\_hys}$.

**Note**

Only Absolute overtemperature events can cause the STATUS to go low. Recovery of the STATUS pin however can happen only if the Dynamic Overtemperature sensor has fallen below $\Delta T_{DYN} - \Delta T_{DYN\_hys}$ and the FET temperature sensor falls below $T_{TSD\_reset}$

### *6.3.5 Undervoltage Lockout (UVLO)*

If at any time the voltage on the INx pin falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled, and internal logic is reset. Operation resumes when INx rises above the UVLO threshold. There is no indication on the STATUS pin.

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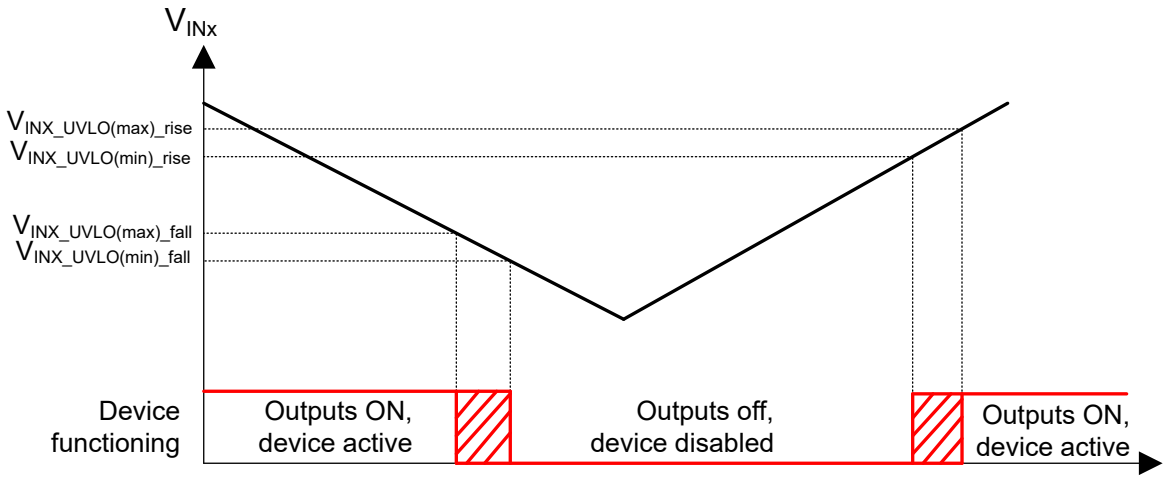


**Figure 6-11. $V_{INX}$ UVLO device response**

### *6.3.6 Summary of STATUS pin response*

| $T_{FET}$ (1)> $T_{TSD}$ | $T_{STAT\_reset}$ < $T_{FET}$ < $T_{TSD}$ - $T_{TSD\_hys}$ | $T_{FET}$ <$T_{STAT\_reset}$ | ΔT(2) >$ΔT_{DYN}$ | ΔT < $ΔT_{DYN}$– $ΔT_{DYN\_hys}$ | OUT response | STATUS |
|---|---|---|---|---|---|---|
| ✓ | ✖ | ✖ | ✖ | ✓ | Off | Low |
| ✖ | ✓ | ✖ | ✖ | ✓ | On | Low |
| ✖ | ✖ | ✓ | ✖ | ✓ | On | High |
| ✖ | ✖ | ✖ | ✖ | ✓ | On | High |
| ✓ | ✖ | ✖ | ✓ | ✖ | Off | Low |
| ✖ | ✓ | ✖ | ✓ | ✖ | Off | Low |
| ✖ | ✖ | ✓ | ✓ | ✖ | Off | Low |
| ✖ | ✖ | ✖ | ✓ | ✖ | Off | High |

1. $T_{FET}$ denotes FET temperature
2. ΔT= $T_{FET}$ - $T_{controller}$

ADVANCE INFORMATION

# Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 1 Application Information

DRV81325/A -Q1 can be used in the following configuration with optional sense resistors on SOURCE pins or current sense.

## 2 Typical Application

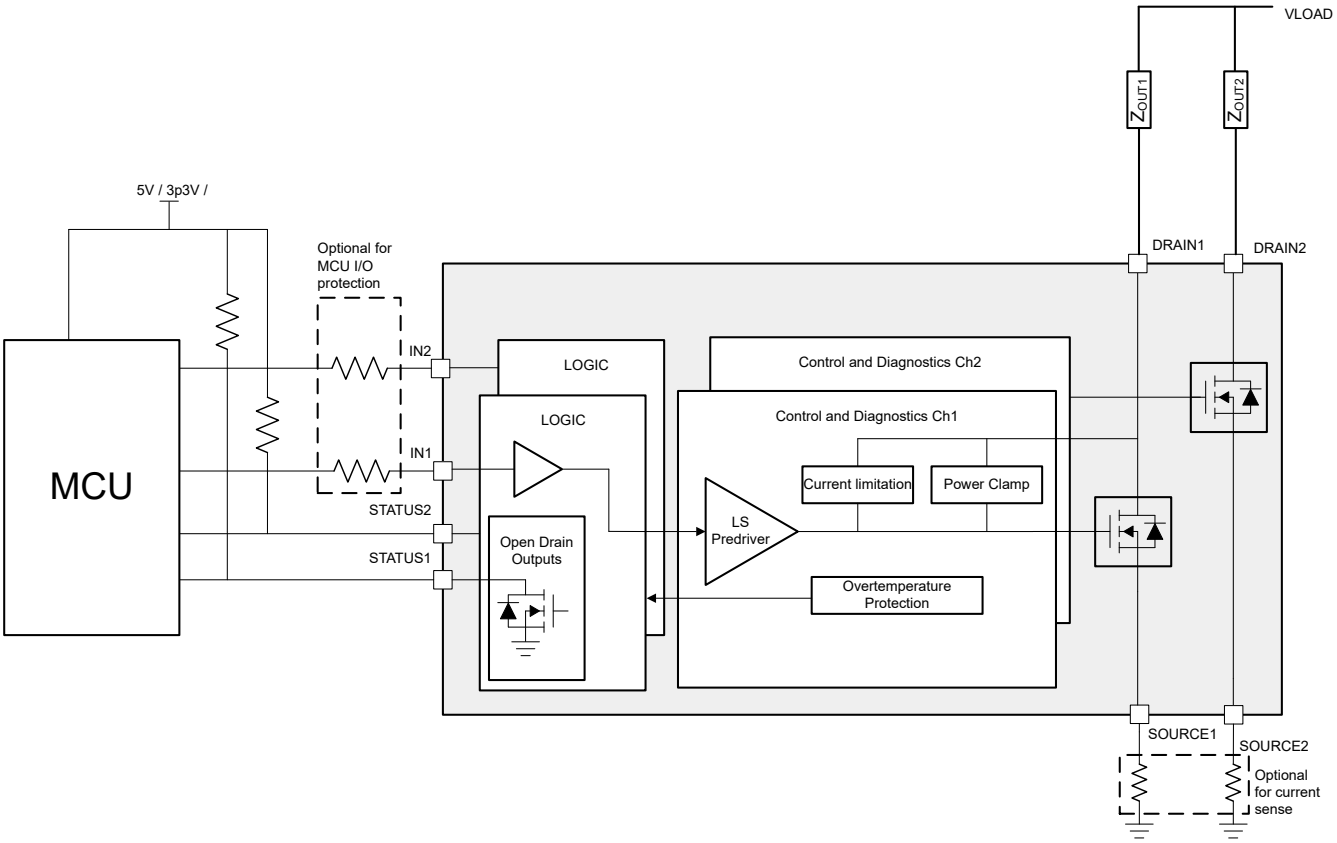


**Figure 7-1. Typical Application Schematic of DRV81325A**

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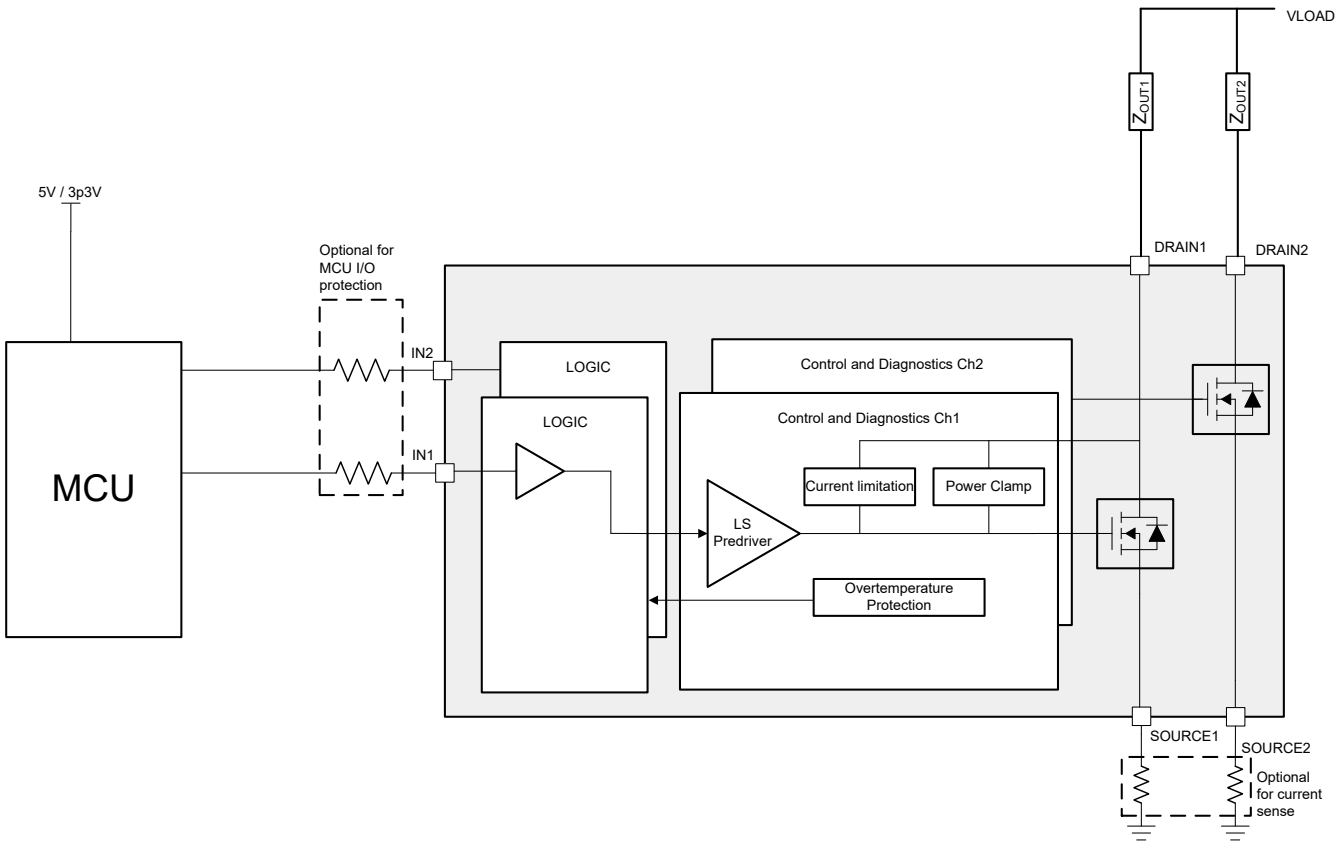



**Figure 7-2. Typical Application Schematic of DRV81325**

### *2.1 External Components*

Following table shows recommended external components for the DRV81325/A-Q1

**Table 7-1. Required External components**

| Symbol | Description | Value | Purpose |
|---|---|---|---|
| $R_{STATUS}$ | Pull up resistor on STATUS | 10kΩ | Bias the STATUS voltage to high when the pin is not pulled low. **For DRV81325A-Q1** |

**Table 7-2. Optional External components**

| Symbol | Description | Value | Purpose |
|---|---|---|---|
| $C_{OUT}$ | Capacitor on each OUTx relative to SOURCEx | <10nF | Filtering for system level ESD |
| $R_{SNS}$ | Shunt sense resistor between SOURCEx and GND | <200mΩ | Optional Resistor at SOURCEx pin for sensing of load current |
| $R_{series}$ | Series resistor to prevent MCU latchup | <500Ω | MCU I/O protection |

## 3 Transient thermal performance

| Figure 7-3. 1(1s0p) Layer PCB with increasing copper area - D package | Figure 7-4. 1(1s0p) Layer PCB with increasing copper area - DDA package |
|---|---|

| Figure 7-5. 4(2s2p) Layer PCB with increasing copper area - D package | Figure 7-6. 4(2s2p) Layer PCB with increasing copper area - D package |
|---|---|

# 4 Layout

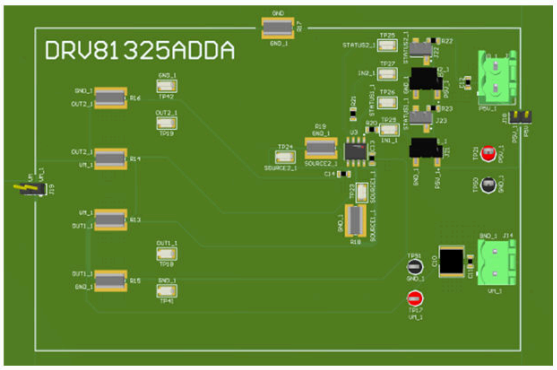
## *4.1 Layout Guidelines*

Small-value capacitors must be ceramic, and placed closely to device pins.

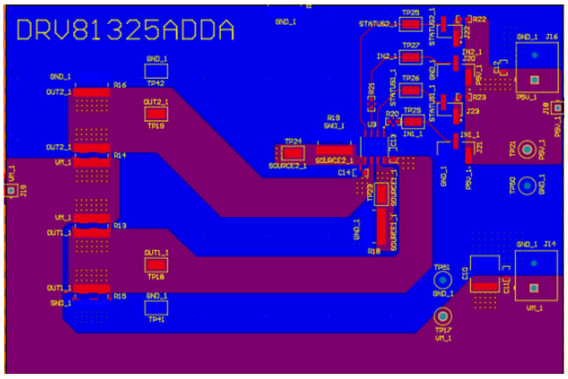
The high-current device outputs must use wide metal traces.

The device thermal pad must be soldered to the PCB top-layer ground plane. Multiple vias must be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

## *4.2 Layout Example*




Top Signal Layer




Second Layer (GND)

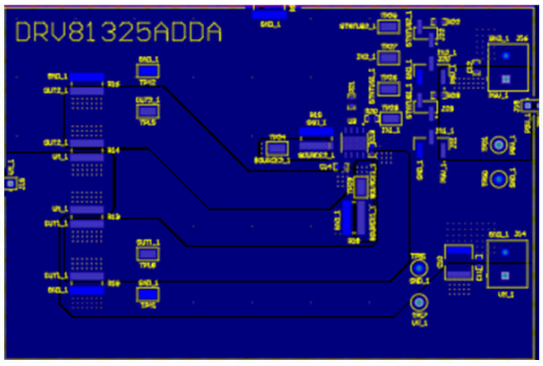
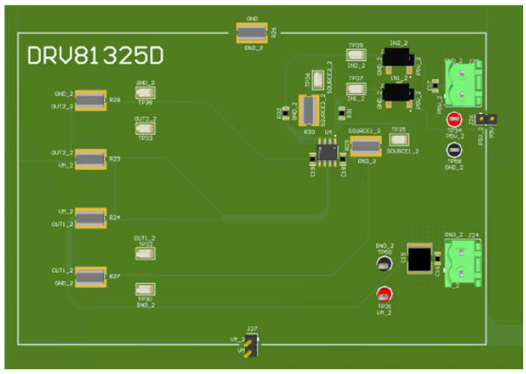
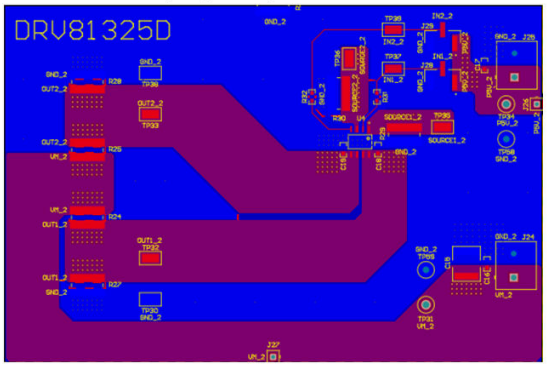



**Figure 7-7. DDA package (Power Pad) in 2s2p (only top and second planes shown)**

ADVANCE INFORMATION




Top Signal Layer




Second Layer (GND)

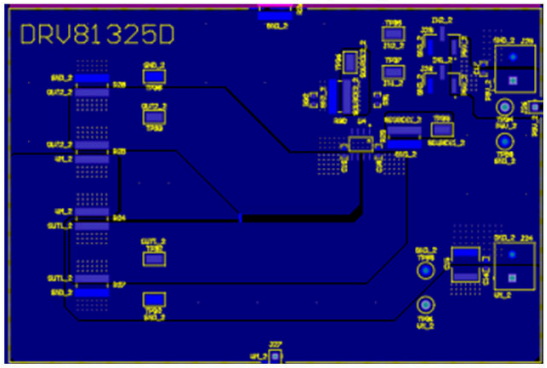



**Figure 7-8. D package in 2s2p (only top and second planes shown)**

## 5 Thermal Consideration

### *5.1 Power Dissipation*

Power dissipation in the DRV81325 device has two components

**Static power dissipation :** Power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 3:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \quad (3)$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT}$ is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and the duration.

**Switching Power dissipation :** Power dissipated in the Output FET when the FET is turned ON/OFF while maintaining a load current (PWM operation). The power dissipated follows the equation below :

$$P_{sw} = P_{sw\_reg} + P_{sw\_clamp}$$

$$P_{sw\_reg} = 0.5 \times V_{load} \times I_{load} \times (tr + tf) \times F_{sw}$$

$$P_{sw\_clamp} = E_{AS} * F_{sw}$$

where:

- $P_{sw}$ is the switching power dissipation of one FET
- $V_{load}$ is the load supply
- $I_{load}$ is the load current
- $t_r$ and $t_f$ denote the rise and fall times at the output
- $F_{sw}$ is the switching frequency
- $E_{AS}$ is the inductive demagnetization energy

**Note**

The component $P_{sw\_clamp}$ is relevant only in case of the integrated output clamp of the DRV813XX being used. An external recirculation path (such as a recirculation diode) being present eliminates the need to consider this component.

When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### *5.2 Heatsinking*

The DRV81325DDA package uses an HSOIC package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI Application Report, *PowerPAD Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

ADVANCE INFORMATION

# 7 Device and Documentation Support

## 7.1 Documentation Support

### *7.1.1 Related Documentation*

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002.
- *PowerPAD Made Easy*, SLMA004.

## 7.2 Community Resources

## 7.3 Trademarks

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# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PDRV81325AQDRQ1 | Active | Preproduction | SOIC (D) \| 8 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

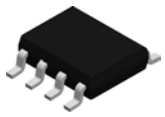
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

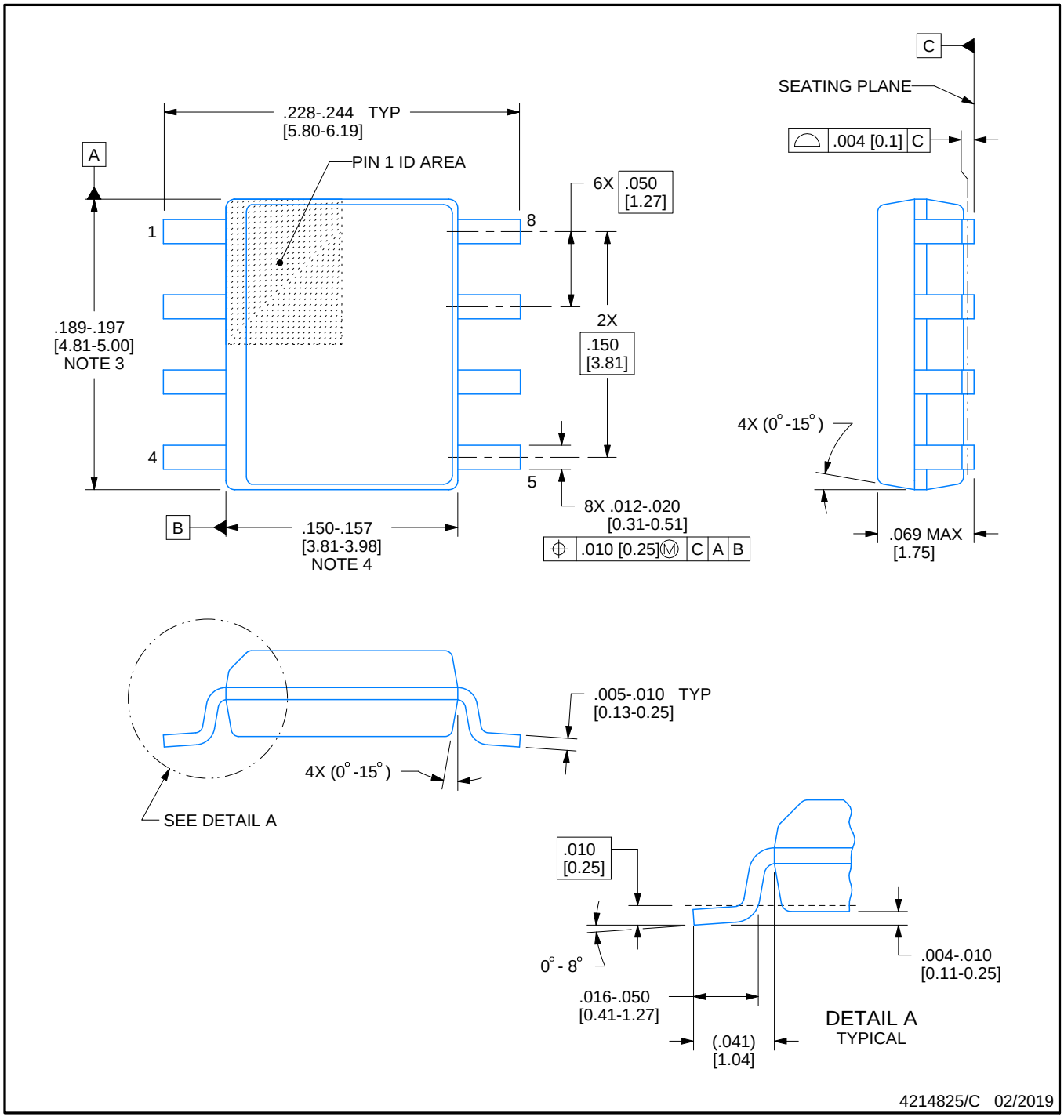


# PACKAGE OUTLINE

## D0008A

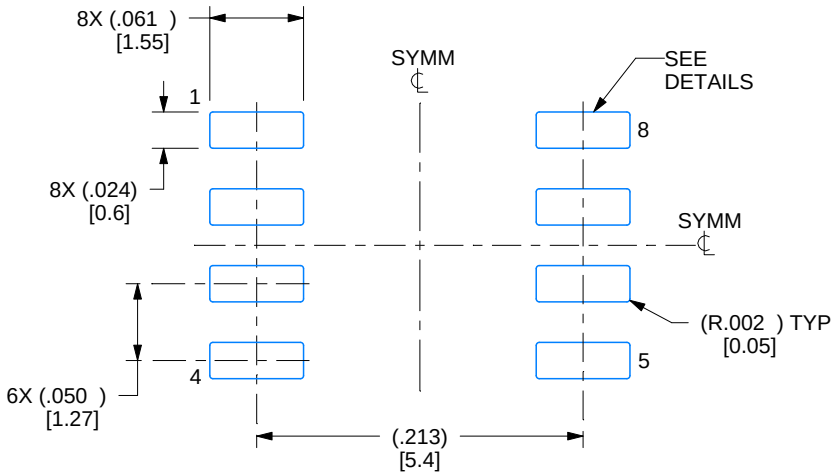
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

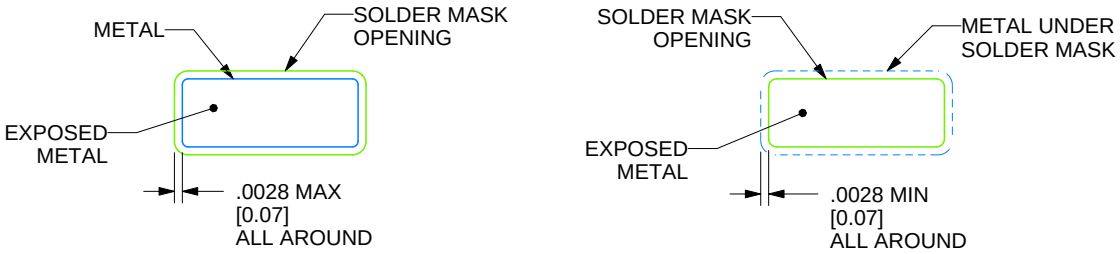



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

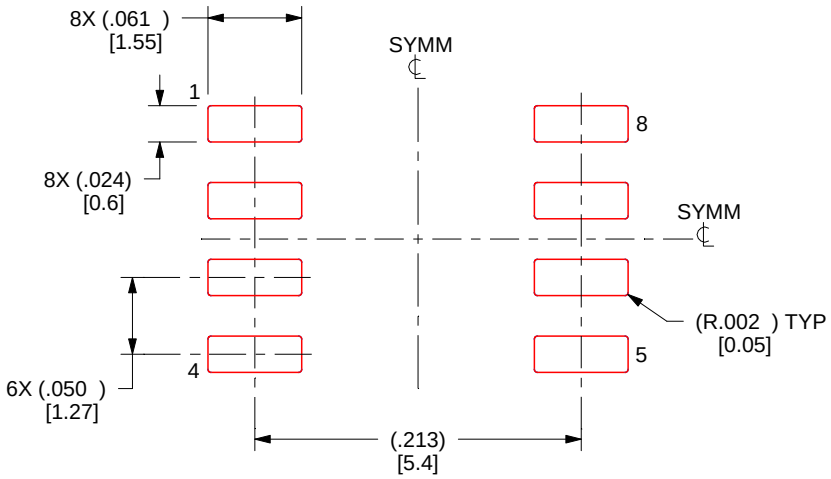
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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