TEXAS INSTRUMENTS

DRV8301-Q1

SLOS842A – SEPTEMBER 2013 – REVISED JUNE 2015

DRV8301-Q1 Automotive Three-Phase Gate Driver With Dual Current Shunt Amplifiers and Buck Regulator

Not Recommended for New Designs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Tested With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4A
- Operating Supply Voltage 6 to 60 V
- 2.3-A Sink and 1.7-A Source Gate Drive Current Capability
- Integrated Dual Shunt Current Amplifiers With Adjustable Gain and Offset
- Integrated Buck Converter to Support up to 1.5-A External Load
- Independent Control of 3 or 6 PWM Inputs
- Bootstrap Gate Driver With 100% Duty Cycle Support
- Programmable Dead Time to Protect External FETs from Shoot-Through
- Slew Rate Control for EMI Reduction
- Programmable Overcurrent Protection of External MOSFETs
- Support Both 3.3-V and 5-V Digital Interface
- SPI Interface
- Thermally Enhanced 56-Pin HTSSOP Pad-Down DCA Package

2 Applications

- Automotive 3-Phase Brushless DC Motor and Permanent Magnet Synchronous Motor
- Water, Oil, Fuel Pumps

3 Description

The DRV8301-Q1 device is an automotive gate driver IC for three phase motor drive applications. The device provides three half bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low side. The device supports up to 2.3-A sink and 1.7-A source peak current capability and only needs a single power supply with a wide range from 6 to 60 V. The DRV8301-Q1 device uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high-side FET or low-side FET is switching to prevent current shoot through. V_{DS} of FETs is sensed to protect external power stage during overcurrent conditions.

The DRV8301-Q1 device includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3 V.

The DRV8301-Q1 device also has an integrated switching mode buck converter with adjustable output and switching frequency to support MCU or additional system power needs. The buck is capable to drive up to 1.5-A load.

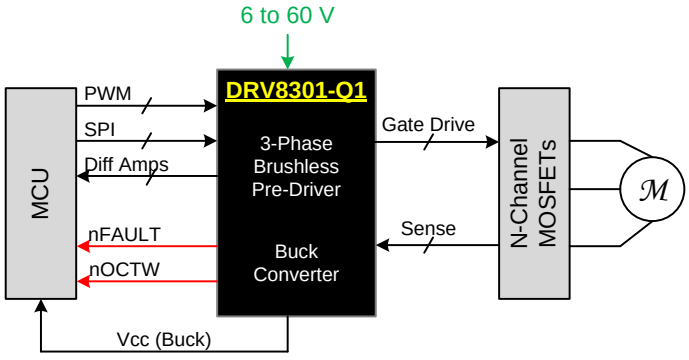
The SPI interface provides detailed fault reporting and flexible parameter settings such as gain options for current shunt amplifier, slew rate control of gate driver, and other settings.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8301-Q1	HTSSOP (56)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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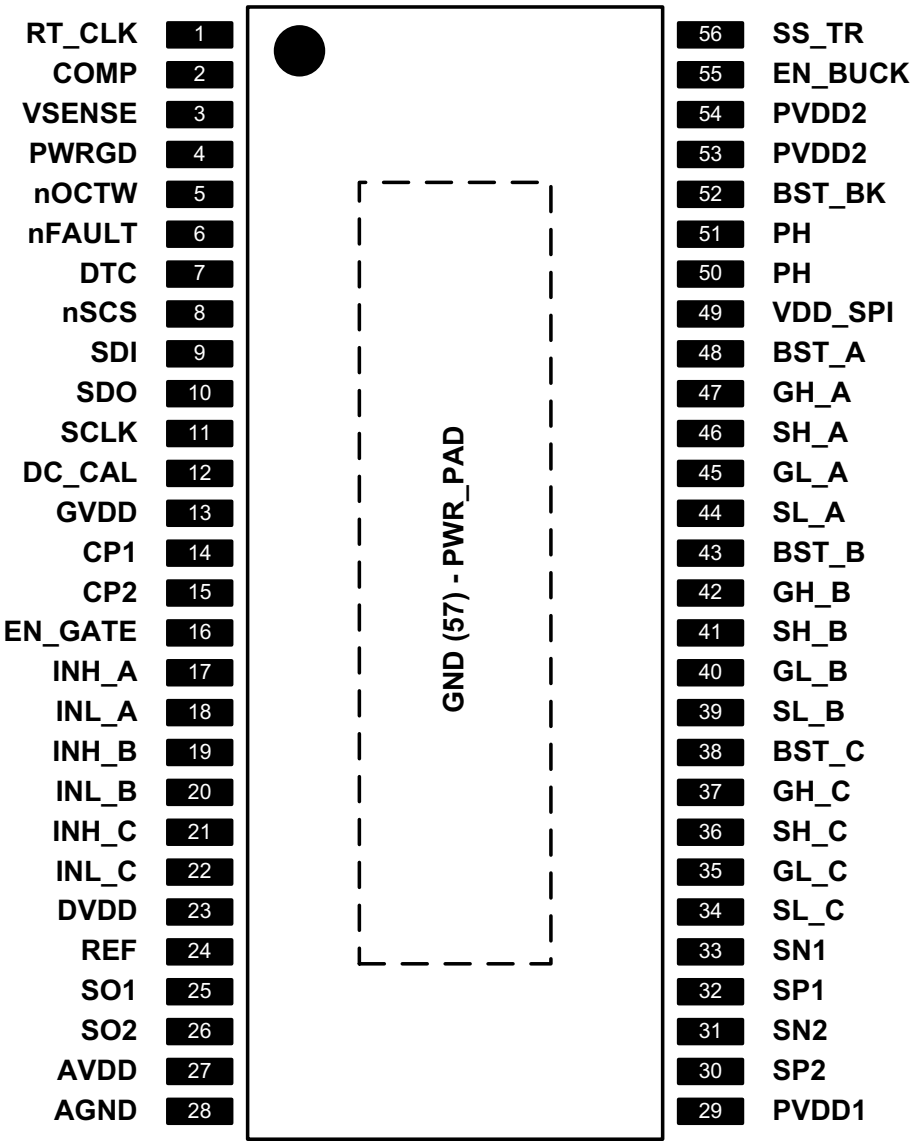
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2013) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• PVDD absolute max voltage rating reduced from 70 V to 65 V	6
• Clarification made on how the OCP status bits report in *Overcurrent Protection and Reporting (OCP)*	18
• Update to PVDD1 undervoltage protection in *Undervoltage Protection (PVDD_UV and GVDD_UV)* describing specific transient brownout issue.	18
• Update to EN_GATE pin functional description in *EN_GATE* clarifying proper EN_GATE reset pulse lengths.	21
• Added *Gate Driver Start-up Issue Errata*	25

5 Pin Configuration and Functions

DCA Package
56-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	28	P	Analog ground pin
AVDD	27	P	Internal 6-V supply voltage, AVDD cap should always be installed and connected to AGND. This is an output, but not specified to drive external circuitry.
BST_A	48	P	Bootstrap capacitor pin for half-bridge A
BST_B	43	P	Bootstrap capacitor pin for half-bridge B
BST_BK	52	P	Bootstrap capacitor pin for buck converter
BST_C	38	P	Bootstrap capacitor pin for half-bridge C
COMP	2	O	Buck error amplifier output and input to the output switch current comparator.
CP1	14	P	Charge pump pin 1, ceramic capacitor should be used between CP1 and CP2
CP2	15	P	Charge pump pin 2, ceramic capacitor should be used between CP1 and CP2
DC_CAL	12	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can occur through external microcontroller.
DTC	7	I	Dead-time adjustment with external resistor to GND
DVDD	23	P	Internal 3.3-V supply voltage. DVDD capacitor should connect to AGND. This is an output, but not specified to drive external circuitry.
EN_BUCK	55	I	Enable buck converter. Internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors
EN_GATE	16	I	Enable gate driver and current shunt amplifiers. Control buck through EN_BUCK pin.
nFAULT	6	O	Fault report indicator. This output is open drain with external pullup resistor required.
GH_A	47	O	Gate drive output for high-side MOSFET, half-bridge A
GH_B	42	O	Gate drive output for high-side MOSFET, half-bridge B
GH_C	37	O	Gate drive output for high-side MOSFET, half-bridge C
GL_A	45	O	Gate drive output for low-side MOSFET, half-bridge A
GL_B	40	O	Gate drive output for low-side MOSFET, half-bridge B
GL_C	35	O	Gate drive output for low-side MOSFET, half-bridge C
GVDD	13	P	Internal gate driver voltage regulator. GVDD capacitor should connect to GND
INH_A	17	I	PWM Input signal (high-side), half-bridge A
INH_B	19	I	PWM Input signal (high-side), half-bridge B
INH_C	21	I	PWM Input signal (high-side), half-bridge C
INL_A	18	I	PWM Input signal (low-side), half-bridge A
INL_B	20	I	PWM Input signal (low-side), half-bridge B
INL_C	22	I	PWM Input signal (low-side), half-bridge C
nOCTW	5	O	Overcurrent and over temperature warning indicator. This output is open drain with external pullup resistor required. Programmable output mode through SPI registers.
PH	50	O	The source of the internal high-side MOSFET of buck converter
	51		
PVDD1	29	P	Power supply pin for gate driver, current shunt amplifier, and SPI communication. PVDD1 is independent of buck power supply, PVDD2. PVDD1 capacitor should connect to GND
PVDD2	53	P	Power supply pin for buck converter, PVDD2 capacitor should connect to GND.
	54		
PWRGD	4	I	An open-drain output with external pullup resistor required. Asserts low if buck output voltage is low because of thermal shutdown, dropout, overvoltage, or EN_BUCK shut down
REF	24	I	Reference voltage to set output of shunt amplfiiers with a bias voltage which equals to half of the voltage set on this pin. Connect to ADC reference in microcontroller.
RT_CLK	1	I	Resistor timing and external clock for buck regulator. Resistor should connect to GND (PowerPAD) with very short trace to reduce the potential clock jitter due to noise.
SCLK	11	I	SPI clock signal
nSCS	8	I	SPI chip select

(1) KEY: I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
SDI	9	I	SPI input
SDO	10	O	SPI output
SH_A	46	I	High-Side MOSFET source connection, half-bridge A. High-side V_{DS} measured between this pin and PVDD1.
SH_B	41	I	High-Side MOSFET source connection, half-bridge B. High-side V_{DS} measured between this pin and PVDD1.
SH_C	36	I	High-Side MOSFET source connection, half-bridge C. High-side V_{DS} measured between this pin and PVDD1.
SL_A	44	I	Low-Side MOSFET source connection, half-bridge A. Low-side V_{DS} measured between this pin and SH_A.
SL_B	39	I	Low-Side MOSFET source connection, half-bridge B. Low-side V_{DS} measured between this pin and SH_B.
SL_C	34	I	Low-Side MOSFET source connection, half-bridge C. Low-side V_{DS} measured between this pin and SH_C.
SN1	33	I	Input of current amplifier 1 (connecting to negative input of amplifier).
SN2	31	I	Input of current amplifier 2 (connecting to negative input of amplifier).
SO1	25	O	Output of current amplifier 1
SO2	26	O	Output of current amplifier 2
SP1	32	I	Input of current amplifier 1 (connecting to positive input of amplifier). Recommended to connect to ground side of the sense resistor for the best common-mode rejection.
SP2	30	I	Input of current amplifier 2 (connecting to positive input of amplifier). Recommended to connect to ground side of the sense resistor for the best common-mode rejection.
SS_TR	56	I	Buck soft-start and tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. Cap should connect to GND
VDD_SPI	49	I	SPI supply pin to support 3.3-V or 5-V logic. Connect to either 3.3 V or 5 V.
VSENSE	3	I	Buck output voltage sense pin. Inverting node of error amplifier.
GND (PWR_PAD)	57	P	GND pin. The exposed PowerPAD must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage including transient, PVDD	Relative to PGND	–0.3	65	V
Maximum supply-voltage ramp rate, $PVDD_{RAMP}$	Voltage rising up to $PVDD_{MAX}$		1	V/µs
Voltage, V_{OPA_IN}	SPx and SNx	–0.6	0.6	V
Input voltage for logic and digital pins, V_{LOGIC}	INH_A, INL_A, INH_B, INL_B, INH_C, INL_C, EN_GATE, SCLK, SDI, SCS, DC_CAL	–0.3	7	V
Maximum voltage	Between PGND and GND (V_{PGND})	–0.3	0.3	V
	GVDD (V_{GVDD})		13.2	
	AVDD (V_{AVDD})		8	
	DVDD (V_{DVDD})		3.6	
	VDD_SPI (V_{VDD_SPI})		7	
	SDO (V_{SDO})		VDD_SPI +0.3	
Maximum reference voltage, V_{REF}	Current amplifier		7	V
Maximum current, I_{IN_MAX}	All digital and analog input pins except FAULT and OCTW pins	–1	1	mA
Maximum sinking current, $I_{IN\_OD\_MAX}$	For open-drain pins (nFault and nOCTW Pins)		7	mA
Maximum current, I_{REF}	REF		100	µA
Maximum operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 28, 56, and 29)	±500	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{PVDD1}	DC supply voltage PVDD1 for normal operation	Relative to PGND	6		60	V
V_{PVDD2}	DC supply voltage PVDD2 for buck converter		3.5		60	V
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{DIN}	Maximum capacitance on digital input pin				10	pF
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor range. Time range is 50 ns (-GND) to 500 ns (150 kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	$\overline{FAULT}$ pin sink current. Open drain	V = 0.4 V			2	mA
I_{OCTW}	$\overline{OCTW}$ pin sink current. Open drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	Qg(TOT) = 25 nC or total 30-mA gate drive average current			200	kHz
I_{gate}	Total average gate drive current				30	mA
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV8301-Q1 DCA (HTSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

PVDD = 6 to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PINS: INH_X, INL_X, nSCS, SDI, SCLK, EN_GATE, DC_CAL						
V_{IH}	High input threshold		2			V
V_{IL}	Low input threshold				0.8	V
RPULL_DOWN – INTERNAL PULLDOWN RESISTOR FOR GATE DRIVER INPUTS						
R_{EN_GATE}	Internal pulldown resistor for EN_GATE			100		kΩ
R_{INH_X}	Internal pulldown resistor for high-side PWMs (INH_A, INH_B, and INH_C)	EN_GATE high		100		kΩ
R_{INH_X}	Internal pulldown resistor for low-side PWMs (INL_A, INL_B, and INL_C)	EN_GATE high		100		kΩ
R_{nSCS}	Internal pulldown resistor for $\overline{SCS}$	EN_GATE high		100		kΩ
R_{SDI}	Internal pulldown resistor for SDI	EN_GATE high		100		kΩ
R_{DC_CAL}	Internal pulldown resistor for DC_CAL	EN_GATE high		100		kΩ
R_{SCLK}	Internal pulldown resistor for SCLK	EN_GATE high		100		kΩ
OUTPUT PINS: nFAULT AND nOCTW						
V_{OL}	Low output threshold	I_O = 2 mA			0.4	V
V_{OH}	High-output threshold	External 47 kΩ pullup resistor connected to 3-5.5 V	2.4			V
I_{OH}	Leakage Current on Open-Drain Pins When Logic High $\overline{FAULT}$ and $\overline{OCTW}$)				1	µA
GATE DRIVE OUTPUT: GH_A, GH_B, GH_C, GL_A, GL_B, GL_C						
V_{GX_NORM}	Gate driver Vgs voltage	PVDD = 8 to 60 V, I_{gate} = 30 mA, C_{CP} = 22 nF	9.5		11.5	V
		PVDD = 8 to 60 V, I_{gate} = 30 mA, C_{CP} = 220 nF	9.5		11.5	
V_{GX_MIN}	Gate driver Vgs voltage	PVDD = 6 to 8 V, I_{gate} = 15 mA, C_{CP} = 22 nF	8.8			V
		PVDD = 6 to 8 V, I_{gate} = 30 mA, C_{CP} = 220 nF	8.3			
I_{oso1}	Maximum source current setting 1, peak	Vgs of FET equals to 2 V. REG 0x02		1.7		A
I_{osi1}	Maximum sink current setting 1, peak	Vgs of FET equals to 8 V. REG 0x02		2.3		A
I_{oso2}	Source current setting 2, peak	Vgs of FET equals to 2 V. REG 0x02		0.7		A
I_{osi2}	Sink current setting 2, peak	Vgs of FET equals to 8 V. REG 0x02		1		A
I_{oso3}	Source current setting 3, peak	Vgs of FET equals to 2 V. REG 0x02		0.25		A
I_{osi3}	Sink current setting 3, peak	Vgs of FET equals to 8 V. REG 0x02		0.5		A
R_{gate_off}	Gate output impedence during standby mode when EN_GATE low (pins GH_x, GL_x)		1.6		2.4	kΩ
SUPPLY CURRENTS						
I_{PVDD1_STB}	PVDD1 supply current, standby	EN_GATE is low. PVDD1 = 8 V.		20	50	µA
I_{PVDD1_OP}	PVDD1 supply current, operating	EN_GATE is high, no load on gate drive output, switching at 10 kHz, 100-nC gate charge		15		mA
I_{PVDD1_HIZ}	PVDD1 Supply current, Hi-Z	EN_GATE is high, gate not switching	2	5	10	mA
INTERNAL REGULATOR VOLTAGE						
A_{VDD}	AVDD voltage	PVDD = 8 to 60 V	6	6.5	7	V
		PVDD = 6 to 60 V	5.5		6	
D_{VDD}	DVDD voltage		3	3.3	3.6	V
VOLTAGE PROTECTION						
V_{PVDD_UV}	Undervoltage protection limit, PVDD	PVDD falling			5.9	V
		PVDD rising			6	
V_{GVDD_UV}	Undervoltage protection limit, GVDD	GVDD falling			7.5	V

Electrical Characteristics (continued)

PVDD = 6 to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GVDD_OV}	Overvoltage protection limit, GVDD			16		V
CURRENT PROTECTION, (VDS SENSING)						
V_{DS_OC}	Drain-source voltage protection limit	PVDD = 8 to 60 V	0.125		2.4	V
		PVDD = 6 to 8 V (1)	0.125		1.491	
T_{oc}	OC sensing response time			1.5		µs
T_{OC_PULSE}	$\overline{OCTW}$ pin reporting pulse stretch length for OC event			64		µs

(1) Reduced A_{VDD} voltage range results in limitations on settings for overcurrent protection. See Table 11.

6.6 Buck Converter Characteristics

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
$I_{SD(PVDD2)}$	Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 60 V		1.3	4	µA
$I_{NON\_SW(PVDD2)}$	Operating: nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V		116	136	µA
V_{EN_BUCK}	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
R_{DS_ON}	On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
I_{LIM}	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
F_{sw}	Switching frequency	RT = 200 kΩ	450	581	720	kHz
PWRGD	VSENSE threshold	VSENSE falling		92%		
		VSENSE rising		94%		
		VSENSE rising		109%		
		VSENSE falling		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω

6.7 Current Shunt Amplifier Characteristics

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G1	Gain option 1	Tc = –40°C to 125°C	9.5	10	10.5	V/V
G2	Gain option 2	Tc = –40°C to 125°C	18	20	21	V/V
G3	Gain Option 3	Tc = –40°C to 125°C	38	40	42	V/V
G4	Gain Option 4	Tc = –40°C to 125°C	75	80	85	V/V
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 10, Vstep = 2 V		300		ns
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 20, Vstep = 2 V		600		ns
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 40, Vstep = 2 V		1.2		µs
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 80, Vstep = 2 V		2.4		µs
Vswing	Output swing linear range		0.3		5.7	V
Slew Rate		G = 10		10		V/µs
DC_offset	Offset error RTI	G = 10 with input shorted			4	mV
Drift_offset	Offset drift RTI			10		µV/C
Ibias	Input bias current				100	µA
Vin_com	Common input mode range		–0.15		0.15	V
Vin_dif	Differential input range		–0.3		0.3	V
Vo_bias	Output bias	With zero input current, V_{REF} up to 6 V	–0.5%	0.5 × V_{REF}	0.5%	V
CMRR_OV	Overall CMRR with gain resistor mismatch	CMRR at DC, gain = 10	70	85		dB

6.8 Gate Timing and Protection Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING, OUTPUT PINS						
$t_{pd,lf-O}$	Positive input falling to GH_x falling	C_L = 1 nF, 50% to 50%		45		ns
$t_{pd,lr-O}$	Positive input rising to GL_x falling	C_L = 1 nF, 50% to 50%		45		ns
T_{d_min}	Minimum dead time after hand shaking (1)				50	ns
T_{dtp}	Dead Time	With R_{DTC} set to different values	50		500	ns
t_{GDr}	Rise time, gate drive output	C_L = 1 nF, 10% to 90%		25		ns
t_{GDF}	Fall time, gate drive output	C_L = 1 nF, 90% to 10%		25		ns
T_{ON_MIN}	Minimum on pulse	Not including handshake communication. Hi-z to on state, output of gate driver			50	ns
T_{pd_match}	Propagation delay matching between high-side and low-side				5	ns
T_{dt_match}	Deadtime matching				5	ns
TIMING, PROTECTION AND CONTROL						
$t_{pd,R\_GATE-OP}$	Start-up time, from EN_GATE active high to device ready for normal operation	PVDD is up before start-up, all charge pump caps and regulator caps as in recommended condition		5	10	ms
$t_{pd,R\_GATE-Quick}$	If EN_GATE goes from high to low and back to high state within quick reset time, it will only reset all faults and gate driver without powering down charge pump, current amp, and related internal voltage regulators.	Maximum low pulse time			10	µs
$t_{pd,E-L}$	Delay, error event to all gates low			200		ns
$t_{pd,E-FAULT}$	Delay, error event to $\overline{\text{FAULT}}$ low			200		ns
OTW_CLR	Junction temperature for resetting over temperature warning			115		°C

(1) Dead time programming definition: Adjustable delay from GH_x falling edge to GL_X rising edge, and GL_X falling edge to GH_X rising edge. This is a minimum dead-time insertion. It is not added to the value set by the microcontroller externally.

Gate Timing and Protection Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTW_SET/OTSD_CLR	Junction temperature for over temperature warning and resetting over temperature shut down			130		°C
OTSD_SET	Junction temperature for over temperature shut down		150			°C

6.9 SPI Timing Requirements (Slave Mode Only)

See Figure 1 and Figure 2.

			MIN	NOM	MAX	UNIT
t_{SPI_READY}	SPI ready after EN_GATE transitions to HIGH	PVDD > 6 V		5	10	ms
t_{CLK}	Minimum SPI clock period		100			ns
t_{CLKH}	Clock high time		40			ns
t_{CLKL}	Clock low time		40			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{HD_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			20	ns
t_{HD_SDO}	SDO output data hold time		40			ns
t_{SU_SCS}	SCS setup time		50			ns
t_{HD_SCS}	SCS hold time		50			ns
t_{HI_SCS}	SCS minimum high time before SCS active low		40			ns
t_{ACC}	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{DIS}	SCS disable time, SCS high to SDO high impedance			10		ns

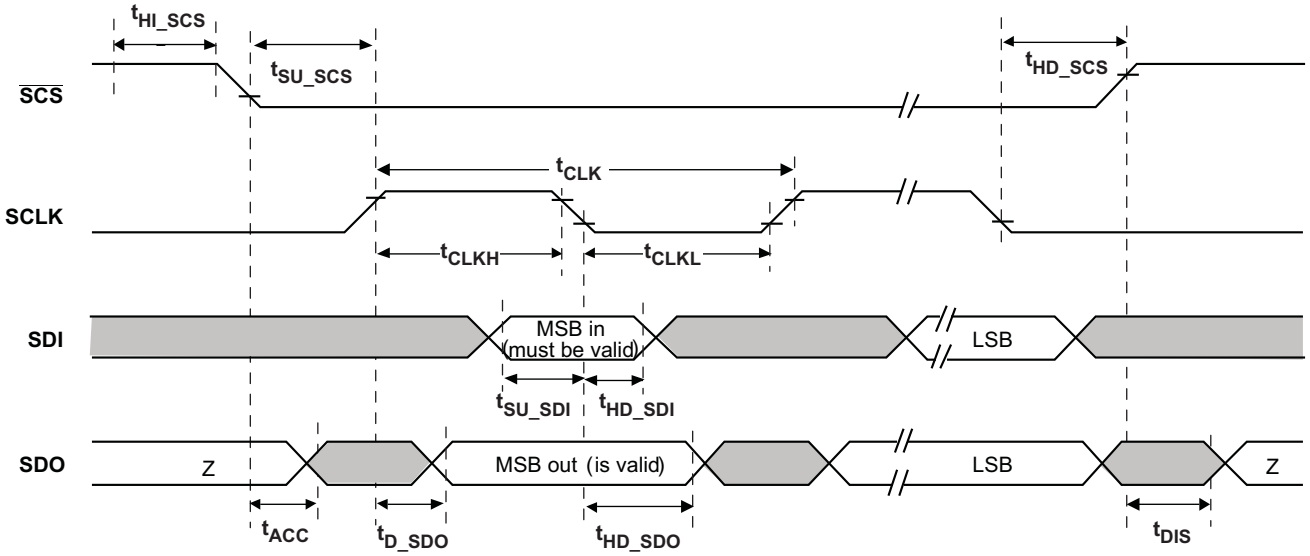


Figure 1. SPI Slave Mode Timing Definition

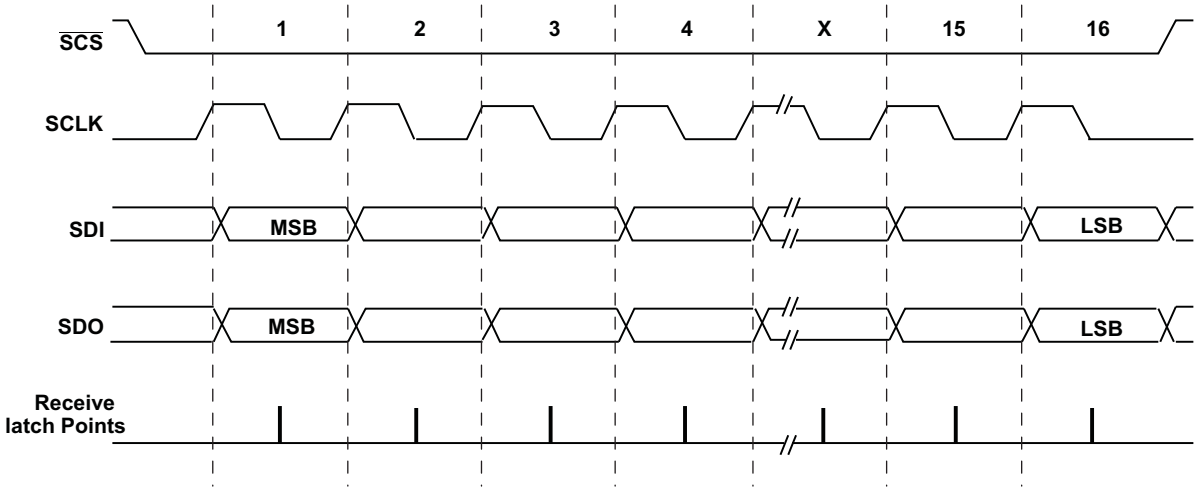


Figure 2. SPI Slave Mode Timing Diagram

6.10 Typical Characteristics

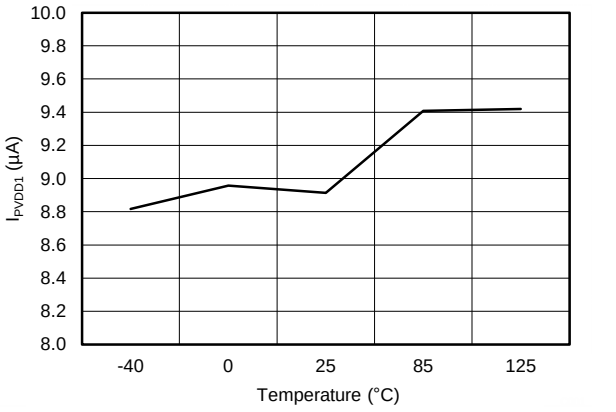


Figure 3. I_{PVDD1} vs Temperature (PVDD1 = 8 V, EN_GATE = LOW)

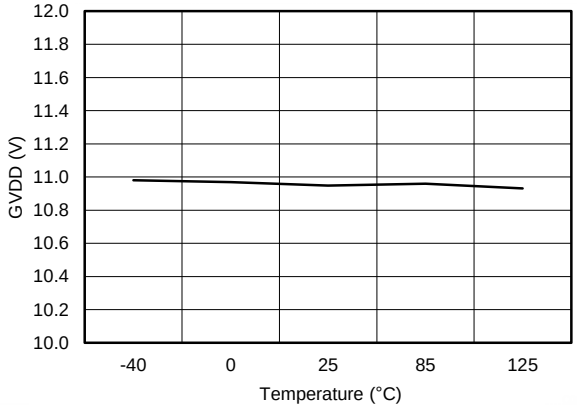


Figure 4. GVDD vs Temperature (PVDD1 = 8 V, EN_GATE = HIGH)

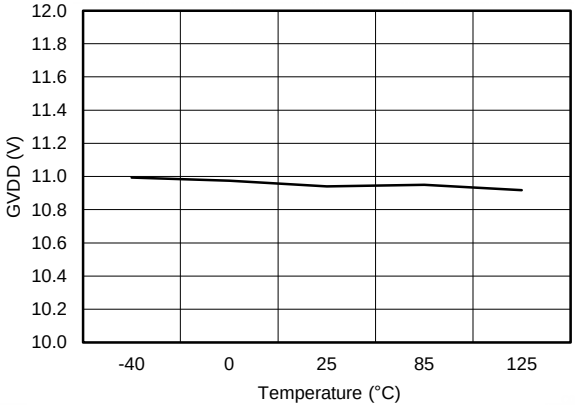


Figure 5. GVDD vs Temperature (PVDD1 = 60 V, EN_GATE = HIGH)

7 Detailed Description

7.1 Overview

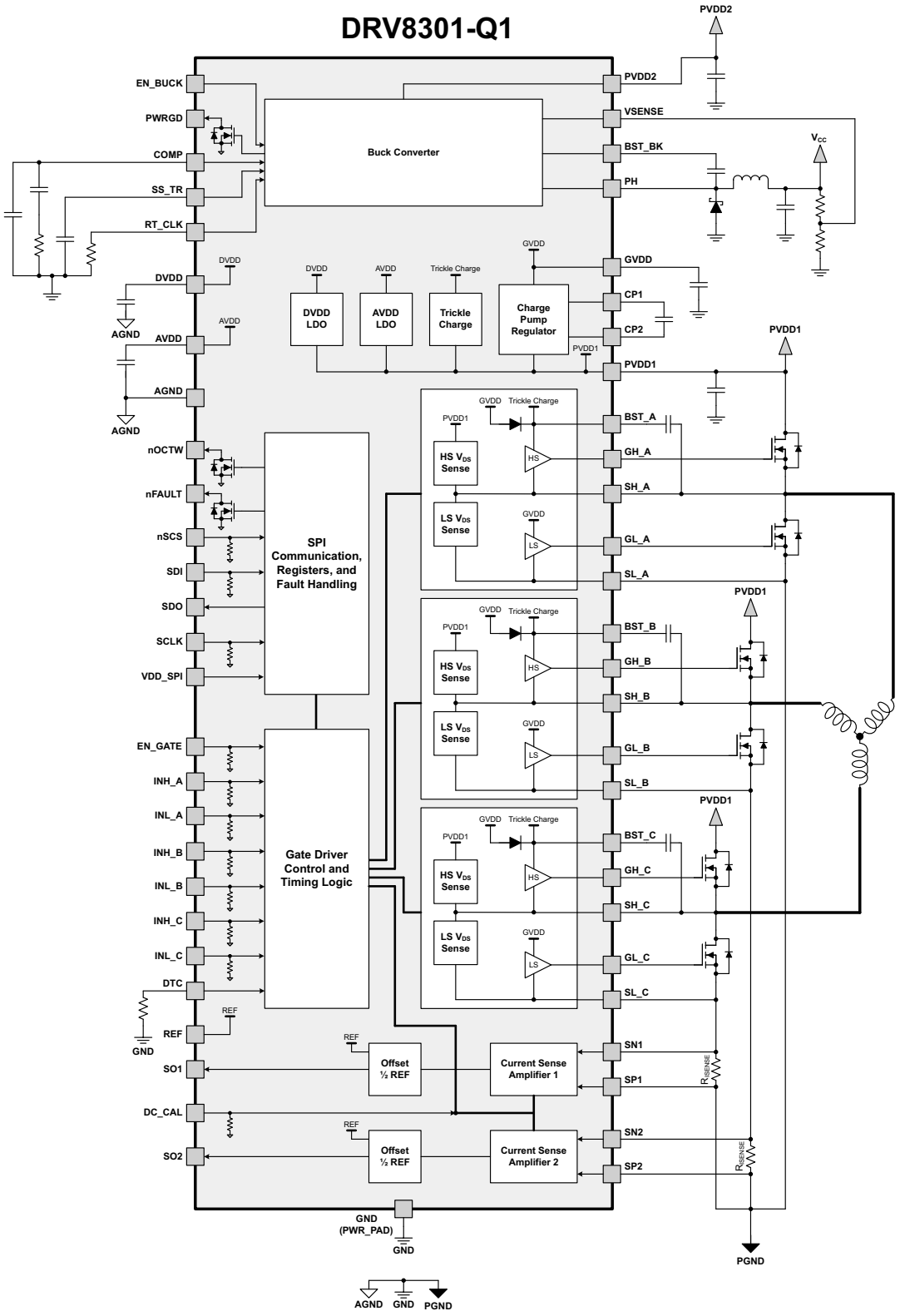
The DRV8301-Q1 is a 6-V to 60-V gate driver IC for three-phase motor drive applications. This device reduces external component count by integrating three half-bridge drivers, two current shunt amplifiers, and a switching buck converter. The DRV8301-Q1 provides overcurrent, overtemperature, and undervoltage protection. Fault conditions are indicated through the nFAULT and nOCTW pins in addition to the SPI registers.

Adjustable dead time control and peak gate drive current allows for finely tuning the switching of the external MOSFETs. Internal hand-shaking is used to prevent flow of current.

VDS sensing of the external MOSFETs allows for the DRV8301-Q1 to detect overcurrent conditions and respond appropriately. Individual MOSFET overcurrent conditions are reported through the SPI status registers.

The highly configurable buck converter can support a wide range of output options. This allows the DRV8301-Q1 to provide a power supply rail for the controller and lower voltage components.

7.2 Function Block Diagram



7.3 Feature Description

7.3.1 Three-Phase Gate Driver

The half-bridge drivers use a bootstrap configuration with a trickle charge pump to support 100% duty cycle operation. Each half-bridge is configured to drive two N-channel MOSFETs, one for the high-side and one for the low-side. The half-bridge drivers can be used in combination to drive a 3-phase motor or separately to drive various other loads.

The peak gate drive current and internal dead times are adjustable to accommodate a variety of external MOSFETs and applications. The peak gate drive current is set through a register setting and the dead time is adjusted with an external resistor on the DTC pin. Shorting the DTC pin to ground will provide the minimum dead time (50 ns). There is an internal hand shake between the high side and low side MOSFETs during switching transitions to prevent current shoot through.

The three-phase gate driver can provide up to 30 mA of average gate drive current. This will support switching frequencies up to 200 kHz when the MOSFET Qg = 25 nC.

Each MOSFET gate driver has a VDS sensing circuit for overcurrent protection. The sense circuit measures the voltage from the drain to the source of the external MOSFETs while the MOSFET is enabled. This voltage is compared against the programmed trip point to determine if an overcurrent event has occurred. The high-side sense is between the PVDD1 and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines will help provide accurate VDS sensing.

The DRV8301-Q1 allows for both 6-PWM and 3-PWM control through a register setting.

Table 1. 6-PWM Mode

INL_X	INH_X	GL_X	GH_X
0	0	L	L
0	1	L	H
1	0	H	L
1	1	L	L

Table 2. 3-PWM Mode

INL_X	INH_X	GL_X	GH_X
X	0	H	L
X	1	L	H

7.3.2 Current Shunt Amplifiers

The DRV8301-Q1 includes two high-performance current shunt amplifiers to accurate low-side, inline current measurement.

The current shunt amplifiers have four programmable GAIN settings through the SPI registers. These are 10, 20, 40, and 80 V/V.

The current shunt amplifiers provide output offset up to 3 V to support bidirectional current sensing. The offset is set to half the voltage on the reference pin (REF).

To minimize DC offset and drift overtemperature, a calibration method is provided through either the DC_CAL pin or SPI register. When DC calibration is enabled, the device will short the input of the current shunt amplifier and disconnect the load. DC calibration can be done at any time, even during MOSFET switching, because the load is disconnected. For the best results, perform the DC calibration during the switching OFF period, when no load is present, to reduce the potential noise impact to the amplifier.

The output of the current shunt amplifier can be calculated as:

$$V_O = \frac{V_{REF}}{2} - G \times (SN_X - SP_X) \quad (1)$$

where

- V_{REF} is the reference voltage (REF pin)
- G is the gain of the amplifier (10, 20, 40, or 80 V/V)
- SN_X and SP_X are the inputs of channel x. SP_X should connect to the ground side of the sense resistor for the best common-mode rejection.

Figure 6 shows the current shunt amplifier simplified block diagram.

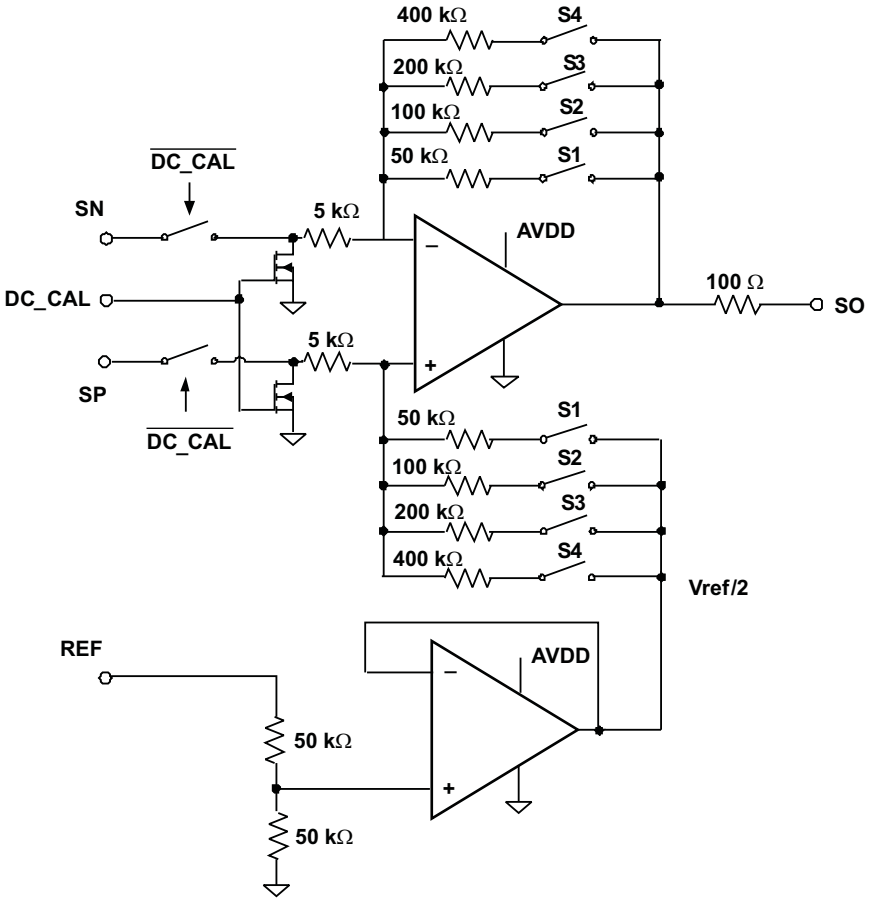


Figure 6. Current Shunt Amplifier Simplified Block Diagram

7.3.3 Buck Converter

The DRV8301-Q1 uses an integrated TPS54160 1.5 A, 60 V, step-down DC-DC converter. Although integrated in the same device, the buck converter is designed completely independent of the rest of the gate driver circuitry. Because the buck converter will support external MCU or other external power need, the independency of buck operation is very critical for a reliable system; this will give the buck converter minimum impact from gate driver operations. Some examples are: when gate driver shuts down due to any failure, buck will still operate unless the fault is coming from buck itself. The buck keeps operating at much lower PVDD of 3.5 V, this will assure the system to have a smooth power-up and power-down sequence when gate driver is not able to operate due to a low PVDD.

For proper selection of the buck converter external components, see *TPS54160 1.5-A, 60-V, Step-Down DC/DC Converter with Eco-mode™* (SLVSB56).

The buck has an integrated high-side N-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The wide switching frequency of 300 kHz to 2200 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT_CLK pin. The device has an internal phase lock loop (PLL) on the RT_CLK pin that is used to synchronize the power switch turnon to a falling edge of an external system clock.

The buck converter has a default start-up voltage of approximately 2.5 V. The EN_BUCK pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. When the EN_BUCK pin is floating the device will operate. The operating current is 116 µA when not switching and under no load. When the device is disabled, the supply current is 1.3 µA.

The integrated 200-mΩ high-side MOSFET allows for high–efficiency power supply designs capable of delivering 1.5 A of continuous current to a load. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The buck can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8-V reference.

The BUCK has a power good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open-drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pullup resistor is used.

The BUCK minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power good comparator. When the OV comparator is activated, the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS_TR (slow start and tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS_TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault,

The BUCK, also, discharges the slow-start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit will slow-start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help control the inductor current.

7.3.4 Protection Features

7.3.4.1 Overcurrent Protection and Reporting (OCP)

To protect the power stage from damage due to excessive currents, V_{DS} sensing circuitry is implemented in the DRV8301-Q1. Based on the $R_{DS(on)}$ of the external MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be determined to trigger the overcurrent protection features when exceeded. The voltage threshold is programmed through the SPI registers. Overcurrent protection should be used as a protection scheme only; it is not intended as a precise current regulation scheme. There can be up to a 20% tolerance across channels for the V_{DS} trip point.

$$V_{DS} = I_{DS} \times R_{DS(on)} \quad (2)$$

The V_{DS} sense circuit measures the voltage from the drain to the source of the external MOSFET while the MOSFET is enabled. The high-side sense is between the PVDD1 and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines will help provide accurate VDS sensing.

Four different overcurrent modes (OC_MODE) can be set through the SPI registers. The OC status bits operate in latched mode. When an overcurrent condition occurs the corresponding OC status bit will latch in the DRV8301-Q1 registers until the fault is reset. After the reset the OC status bit will clear from the register until another overcurrent condition occurs.

1. Current Limit Mode

   In current limit mode the device uses current limiting instead of device shutdown during an overcurrent event. In this mode the device reports overcurrent events through the nOCTW pin. The nOCTW pin will be held low for a maximum 64-µs period (internal timer) or until the next PWM cycle. If another overcurrent event is triggered from another MOSFET, during a previous overcurrent event, the reporting will continue for another 64-µs period (internal timer will restart) or until both PWM signals cycle. The associated status bit will be asserted for the MOSFET in which the overcurrent was detected.

   There are two current control settings in current limit mode. These are set by one bit in the SPI registers. The default mode is cycle by cycle (CBC).
   – Cycle-By-Cycle Mode (CBC): In CBC mode, the MOSFET on which overcurrent has been detected on will shut off until the next PWM cycle.
   – Off-Time Control Mode: In Off-Time mode, the MOSFET in which overcurrent has been detected is disabled for a 64-µs period (set by internal timer). If overcurrent is detected in another MOSFET, the timer will be reset for another 64-µs period and both MOSFETs will be disabled for the duration. During this period, normal operation can be restored for a specific MOSFET with a corresponding PWM cycle.
2. OC Latch Shutdown Mode

   When an overcurrent event occurs, both the high-side and low-side MOSFETs will be disabled in the corresponding half-bridge. The nFAULT pin and nFAULT status bits will be asserted along with the associated status bit for the MOSFET in which the overcurrent was detected. The nFAULT pin, nFAULT status bit, and OC status bit will latch until a reset is received through the GATE_RESET bit or a quick EN_GATE reset pulse.
3. Report Only Mode

   No protective action will be taken in this mode when an overcurrent event occurs. The overcurrent event will be reported through the nOCTW pin (64-µs pulse) and SPI status register. The external MCU should take action based on its own control algorithm.
4. OC Disabled Mode

   The device will ignore and not report all overcurrent detections.

7.3.4.2 Undervoltage Protection (PVDD_UV and GVDD_UV)

To protect the power output stage during start-up, shutdown, and other possible undervoltage conditions, the DRV8301-Q1 provides undervoltage protection by driving the gate drive outputs (GH_X, GL_X) low whenever PVDD or GVDD are below their undervoltage thresholds (PVDD_UV/GVDD_UV). This will put the external MOSFETs in a high impedance state. When the device is in PVDD_UV it will not respond to SPI commands and the SPI registers will revert to their default settings.

A specific PVDD1 undervoltage transient brownout from 13 to 15 µs can cause the DRV8301-Q1 to become unresponsive to external inputs until a full power cycle. The transient condition consists of having PVDD1 greater than the PVDD_UV level and then PVDD1 dropping below the PVDD_UV level for a specific period of 13 to 15 µs. Transients shorter or longer than 13 to 15 µs will not affect the normal operation of the undervoltage protection. Additional bulk capacitance can be added to PVDD1 to reduce undervoltage transients.

7.3.4.3 Overvoltage Protection (GVDD_OV)

The device will shut down both the gate driver and charge pump if the GVDD voltage exceeds the GVDD_OV threshold to prevent potential issues related to the GVDD pin or the charge pump (for example, short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a reset transition on the EN_GATE pin.

7.3.4.4 Overtemperature Protection

A two-level overtemperature detection circuit is implemented:

- Level 1: Over Temperature Warning (OTW)
  OTW is reported through the nOCTW pin (overcurrent and/or overtemperature warning) for default settings. OCTW pin can be set to report OTW or OCW only through the SPI registers. See *SPI Communication*.
- Level 2: Over Temperature Latched Shutdown of Gate Driver and Charge Pump (OTSD_GATE)
  OTSD_GATE is reported through the nFAULT pin. This is a latched shutdown, so the gate driver will not recover automatically, even if the overtemperature condition is not present anymore. An EN_GATE reset or SPI (RESET_GATE) is required to recover the gate driver to normal operation after the temperature goes below a preset value, t_{OTSD_CLR}.

SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD1 is within the defined operation range.

7.3.4.5 Fault and Protection Handling

The nFAULT pin indicates when a shutdown event has occurred. These events include overcurrent, overtemperature, overvoltage, or undervoltage. nFAULT is an open-drain signal. nFAULT will go high when the gate driver is ready for PWM inputs during start-up.

The nOCTW pin indicates when a overcurrent event or overtemperature event has occurred. These events are not necessary related to a shutdown.

Table 3 provides a summary of all the protection features and their reporting structure.

Table 3. Fault and Warning Reporting and Handling

EVENT	ACTION	LATCH	REPORTING ON nFAULT PIN	REPORTING ON nOCTW PIN	REPORTING IN SPI STATUS REGISTER
PVDD undervoltage	External FETs Hi-Z; Weak pulldown of all gate driver output	N	Y	N	Y
DVDD undervoltage	External FETs Hi-Z; Weak pulldown of all gate driver output; When recovering, reset all status registers	N	Y	N	N
GVDD undervoltage	External FETs Hi-Z; Weak pulldown of all gate driver output	N	Y	N	Y
GVDD overvoltage	External FETs Hi-Z; Weak pulldown of all gate driver output Shutdown the charge pump Won't recover and reset through SPI reset command or quick EN_GATE toggling	Y	Y	N	Y
OTW	None	N	N	Y (in default setting)	Y
OTSD_GATE	Gate driver latched shutdown. Weak pulldown of all gate driver output to force external FETs Hi-Z Shut down the charge pump	Y	Y	Y	Y
OTSD_BUCK	OTSD of Buck	Y	N	N	N
Buck output undervoltage	UVLO_BUCK: auto-restart	N	Y (PWRGD pin)	N	N
Buck overload	Buck current limiting (Hi-Z high side until current reaches zero and then auto-recovering)	N	N	N	N
External FET overload – current limit mode	External FETs current limiting (only OC detected FET)	N	N	Y	Y
External FET overload – Latch mode	Weak pulldown of gate driver output and PWM logic "0" of LS and HS in the same phase. External FETs Hi-Z	Y	Y	Y	Y
External FET overload – reporting only mode	Reporting only	N	N	Y	Y

7.3.5 Start-up and Shutdown Sequence Control

During power up all gate drive outputs are held low. Normal operation of gate driver and current shunt amplifiers can be initiated by toggling EN_GATE from a low state to a high state. If no errors are present, the DRV8301-Q1 is ready to accept PWM inputs. Gate driver always has control of the power FETs even in gate disable mode as long as PVDD is within functional region.

There is an internal diode from SDO to VDD_SPI, so VDD_SPI is required to be powered to the same power level as other SPI devices (if there is any SDO signal from other devices) all the time. VDD_SPI supply should be powered up first before any signal appears at SDO pin and powered down after completing all communications at SDO pin.

7.4 Device Functional Modes

7.4.1 EN_GATE

EN_GATE low is used to put gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low-power consumption mode to save energy. SPI communication is not supported during this state and the SPI registers will revert to their default settings after a full EN_GATE reset. The device will put the MOSFET output stage to high-impedance mode as long as PVDD is still present.

When the EN_GATE pin goes low to high, it will go through a power-up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, and so forth and reset all latched faults related to gate driver block. The EN_GATE will also reset status registers in the SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present.

When EN_GATE goes from high to low, it will shut down gate driver block immediately, so gate output can put external FETs in high impedance mode. It will then wait for 10 µs before completely shutting down the rest of the blocks. A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10 µs). This will prevent the device from shutting down the other functional blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode. To perform a full reset, EN_GATE should be toggled for longer than 20 µs. This allows for all of the blocks to completely shut down and reach known states.

An EN_GATE reset pulse (high → low → high) from 10 to 20 µs should not be applied to the EN_GATE pin. The DRV8301-Q1 has a transition area from the quick to full reset modes that can cause the device to become unresponsive to external inputs until a full power cycle. An RC filter can be added externally to the pin if reset pulses with this period are expected to occur on the EN_GATE pin.

The other way to reset all of the faults is to use SPI command (RESET_GATE), which will only reset gate driver block and all the SPI status registers without shutting down the other functional blocks.

One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset will not work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 20 µs is required to reset GVDD_OV fault. TI highly recommends to inspect the system and board when GVDD_OV occurs.

7.4.2 DTC

Dead time can be programmed through DTC pin. A resistor should be connected from DTC to ground to control the dead time. Dead time control range is from 50 ns to 500 ns. Short DTC pin to ground will provide minimum dead time (50 ns). Resistor range is 0 to 150 kΩ. Dead time is linearly set over this resistor range.

Current shoot-through prevention protection will be enabled in the device all time independent of dead time setting and input mode setting.

7.4.3 VDD_SPI

VDD_SPI is the power supply to power SDO pin. It has to be connected to the same power supply (3.3 V or 5 V) that MCU uses for its SPI operation.

During power-up or power-down transient, VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at SDO pin from any other devices in the system because it causes a parasitic diode in the DRV8301-Q1 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

7.5 Programming

7.5.1 SPI Communication

7.5.1.1 SPI

The DRV8301-Q1 SPI operates as a slave. The SPI input (SDI) data format consists of a 16 bit word with 1 read/write bit, 4 address bits, and 11 data bits. The SPI output (SDO) data format consists of a 16 bit word with 1 frame fault bit, 4 address bits, and 11 data bits. When a frame is not valid, frame fault bit will set to 1 and the remaining bits will shift out as 0.

A valid frame must meet following conditions:

- Clock must be low when nSCS goes low.
- Should have 16 full clock cycles.
- Clock must be low when nSCS goes high.

When nSCS is asserted high, any signals at the SCLK and SDI pins are ignored and SDO is forced into a high impedance state. When nSCS transitions from HIGH to LOW, SDO is enabled and the SDO response word loads into the shift register based on the previous SPI input word.

The SCLK pin must be low when nSCS transitions low. While nSCS is low, at each rising edge of the clock the response word is serially shifted out on the SDO pin with the MSB shifted out first.

While SCS is low, at each falling edge of the clock the new input word is sampled on the SDI pin. The SPI input word is decoded to determine the register address and access type (read or write). The MSB will be shifted in first. Any amount of time may pass between bits, as long as nSCS stays active low. This allows two 8-bit words to be used. If the input word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in the next SDO response word will then report 1. After the 16th clock cycle or when nSCS transitions from LOW to HIGH, the SDI shift register data is transferred into a latch where the input word is decoded.

For a READ command (Nth cycle) sent to SDI, SDO will respond with the data at the specified address in the next cycle. (N+1)

For a WRITE command (Nth cycle) sent to SDI, SDO will respond with the data in Status Register 1 (0x00) in the next cycle (N+1). This feature is intended to maximize SPI communication efficiency when having multiple write commands.

7.5.1.2 SPI Format

The SDI input data word is 16 bits long and consists of:

- 1 read/write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

The SDO output data word is 16 bits long and consists of:

- 1 fault frame bit F [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

The SDO output word (Nth cycle) is in response to the previous SDI input word (N-1 cycle).

Therefore each SPI Query/Response pair requires two full 16 bit shift cycles to complete.

Table 4. SPI Input Data Control Word Format

	R/W	ADDRESS				DATA										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SPI Output Data Response Word Format

	R/W	DATA														
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	F0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.6 Register Maps

7.6.1 Read / Write Bit

The MSB bit of the SDI input word (W0) is a read/write bit. When W0 = 0, the input word is a write command. When W0 = 1, input word is a read command.

7.6.2 Address Bits

Table 6. Register Address

REGISTER TYPE	ADDRESS [A3..A0]				REGISTER NAME	DESCRIPTION	READ AND WRITE ACCESS
Status Register	0	0	0	0	Status Register 1	Status register for device faults	R
	0	0	0	1	Status Register 2	Status register for device faults and ID	R
Control Register	0	0	1	0	Control Register 1		R/W
	0	0	1	1	Control Register 2		R/W

7.6.3 SPI Data Bits

7.6.3.1 Status Registers

Table 7. Status Register 1 (Address: 0x00) (All Default Values are Zero)

ADDRESS	REGISTER NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Status Register 1	FAULT	GVDD_UV	PVDD_UV	OTSD	OTW	FETHA_OC	FETLA_OC	FETHB_OC	FETLB_OC	FETHC_OC	FETLC_OC

Table 8. Status Register 2 (Address: 0x01) (All Default Values are Zero)

ADDRESS	REGISTER NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	Status Register 2				GVDD_OV				Device ID [3]	Device ID [2]	Device ID [1]	Device ID [0]

7.6.3.2 Control Registers

Table 9. Control Register 1 for Gate Driver Control (Address: 0x02)(1)

ADDRESS	NAME	DESCRIPTION	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x02	GATE_CURRENT	Gate drive peak current 1.7 A										0(1)	0(1)
		Gate drive peak current 0.7 A										0	1
		Gate drive peak current 0.25 A										1	0
		Reserved										1	1
	GATE_RESET	Normal mode									0(1)		
		Reset gate driver latched faults (reverts to 0)									1		
	PWM_MODE	6 PWM inputs (see Table 1)								0(1)			
		3 PWM inputs (see Table 2)								1			
	OCP_MODE	Current limit						0(1)	0(1)				
		OC latch shut down						0	1				
		Report only						1	0				
		OC disabled						1	1				
	OC_ADJ_SET	See OC_ADJ_SET table	X	X	X	X	X						

(1) Default value

Table 10. Control Register 2 for Current Shunt Amplifiers and Misc Control (Address: 0x03)(1)

ADDRESS	NAME	DESCRIPTION	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x03	OCTW_MODE	Report both OT and OC at nOCTW pin										0(1)	0(1)
		Report OT only										0	1
		Report OC only										1	0
		Report OC only (reserved)										1	1
	GAIN	Gain of shunt amplifier: 10 V/V								0(1)	0(1)		
		Gain of shunt amplifier: 20 V/V								0	1		
		Gain of shunt amplifier: 40 V/V								1	0		
		Gain of shunt amplifier: 80 V/V								1	1		
	DC_CAL_CH1	Shunt amplifier 1 connects to load through input pins							0(1)				
		Shunt amplifier 1 shorts input pins and disconnects from load for external calibration							1				
	DC_CAL_CH2	Shunt amplifier 2 connects to load through input pins						0(1)					
		Shunt amplifier 2 shorts input pins and disconnects from load for external calibration						1					
	OC_TOFF	Cycle by cycle					0(1)						
		Off-time control					1						
	Reserved												

(1) Default value

7.6.3.3 Overcurrent Adjustment

Table 11. OC_ADJ_SET Table

Control Bit (D6–D10) (0xH)	0	1	2	3	4	5	6	7
Vds (V)	0.06	0.068	0.076	0.086	0.097	0.109	0.123	0.138
Control Bit (D6–D10) (0xH)	8	9	10	11	12	13	14	15
Vds (V)	0.155	0.175	0.197	0.222	0.250	0.282	0.317	0.358
Control Bit (D6–D10) (0xH)	**16**	17	18	19	20	21	22	23
Vds (V)	0.403	0.454	0.511	0.576	0.648	0.730	0.822	0.926
Code Number (0xH)	24	25	26	27	28	29	30	31
Vds (V)	1.043	1.175	1.324	1.491	1.679(1)	1.892(1)	2.131(1)	2.400(1)

(1) Do not use settings 28, 29, 30, 31 for V_{DS} sensing if the IC is expected to operate in the 6-V to 8-V range.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8301-Q1 is a gate driver designed to drive a 3-phase BLDC motor in combination with external power MOSFETs. The device provides a high level of integration with three half-bridge gate drivers, two current shunt amplifiers, overcurrent protection, and a step-down buck regulator.

8.1.1 Gate Driver Start-up Issue Errata

The DRV8301-Q1 gate drivers may not correctly power up if a voltage greater than 8.5 V is present on any SH_X pin when EN_GATE is first brought logic high (device first enabled) after PVDD1 power is applied. This situation should be avoided by ensuring the voltage levels on the SH_X pins are less than 8.5 V when the DRV8301-Q1 is first enabled. After the first successful enable, EN_GATE can be brought low or high regardless of the SH_X pin voltage with no impact to the device operation.

8.2 Typical Application

The following design is a common application of the DRV8301-Q1.

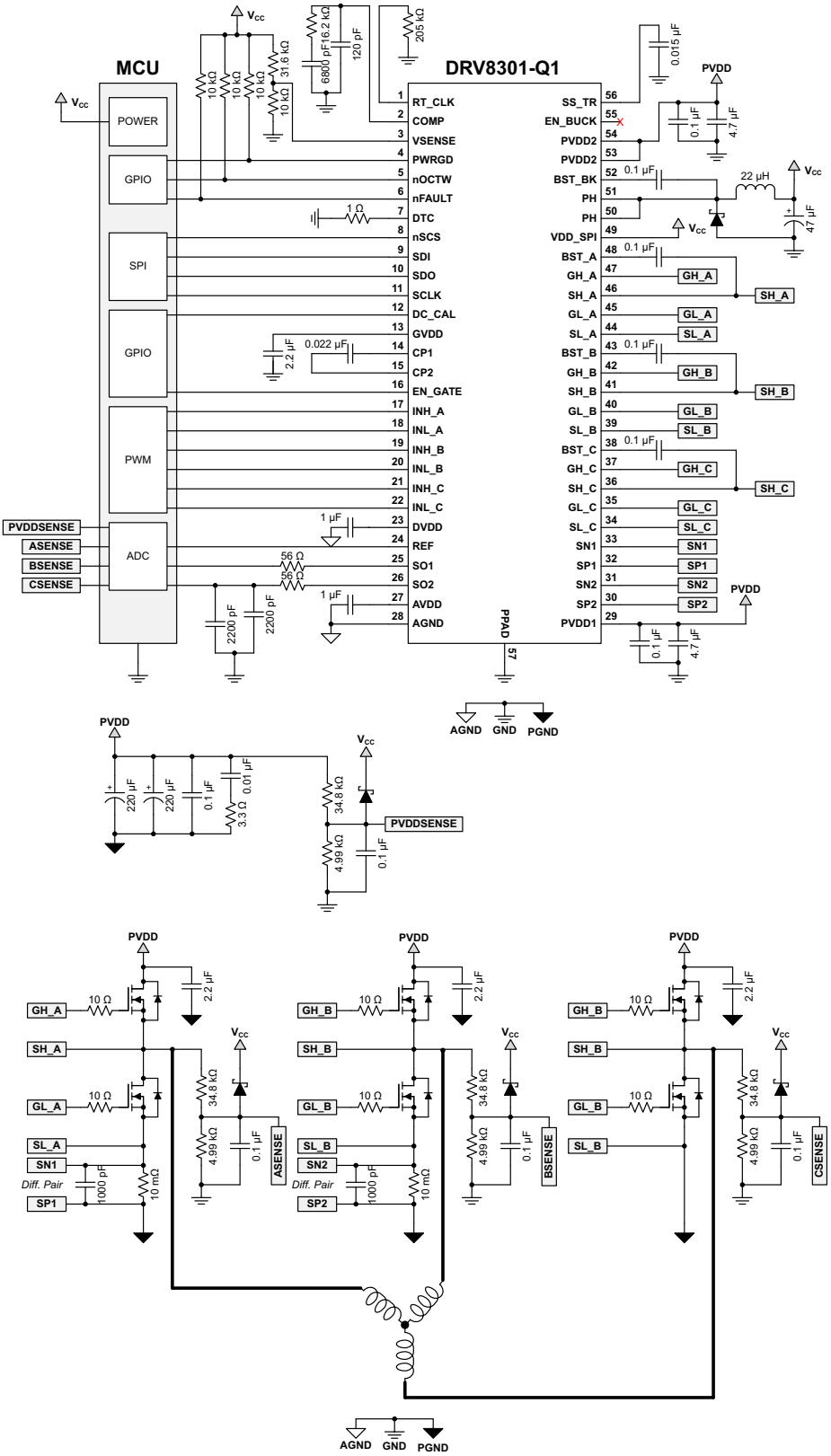


Figure 7. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 12. Design Parameters

DESIGN PARAMETER	REFERENCE	VALUE
Supply voltage	PVDD	24 V
Motor winding resistance	M_R	0.5 Ω
Motor winding inductance	M_L	0.28 mH
Motor poles	M_P	16 poles
Motor rated RPM	M_{RPM}	4000 RPM
Target full-scale current	I_{MAX}	14 A
Sense resistor	R_{SENSE}	0.01 Ω
MOSFET Q_g	Q_g	29 nC
MOSFET RDS(on)	$R_{DS(on)}$	4.7 mΩ
VDS trip level	OC_ADJ_SET	0.123 V
Switching frequency	f_{SW}	45 kHz
Series gate resistance	R_{GATE}	10 Ω
Amplifier reference	V_{REF}	3.3 V
Amplifier gain	Gain	10 V/V

8.2.2 Detailed Design Procedure

Table 13. Gate Driver External Components

NAME	PIN 1	PIN 2	RECOMMENDED
R_{nOCTW}	nOCTW	V_{CC} (1)	≥10 kΩ
R_{nFAULT}	nFAULT	V_{CC} (1)	≥10 kΩ
R_{DTC}	DTC	GND (PowerPAD)	0 to 150 kΩ (50 ns to 500 ns)
C_{GVDD}	GVDD	GND (PowerPAD)	2.2 µF (20%) ceramic, ≥ 16 V
C_{CP}	CP1	CP2	0.022 µF (20%) ceramic, rated for PVDD1
C_{DVDD}	DVDD	AGND	1 µF (20%) ceramic, ≥ 6.3 V
C_{AVDD}	AVDD	AGND	1 µF (20%) ceramic, ≥ 10 V
C_{PVDD1}	PVDD1	GND (PowerPAD)	≥4.7 µF (20%) ceramic, rated for PVDD1
C_{BST_X}	BST_X	SH_X	0.1 µF (20%) ceramic, ≥ 16 V

(1) V_{CC} is the logic supply to the MCU

Table 14. Buck Regulator External Components

NAME	PIN 1	PIN 2	RECOMMENDED
R_{RT_CLK}	RT_CLK	GND (PowerPAD)	See *Buck Converter*
C_{COMP}	COMP	GND (PowerPAD)	See *Buck Converter*
RC_{COMP}	COMP	GND (PowerPAD)	See *Buck Converter*
$R_{VSENSE1}$	PH (Filtered)	VSENSE	See *Buck Converter*
$R_{VSENSE2}$	VSENSE	GND (PowerPAD)	See *Buck Converter*
R_{PWRGD}	PWRGD	V_{CC} (1)	≥ 10 kΩ
L_{PH}	PH	PH (Filtered)	See *Buck Converter*
D_{PH}	PH	GND (PowerPAD)	See *Buck Converter*
C_{PH}	PH (Filtered)	GND (PowerPAD)	See *Buck Converter*
C_{BST_BK}	BST_BK	PH	See *Buck Converter*
C_{PVDD2}	PVDD2	GND (PowerPAD)	≥4.7 µF (20%) ceramic, rated for PVDD2

(1) V_{CC} is the logic supply to the MCU

Table 14. Buck Regulator External Components (continued)

NAME	PIN 1	PIN 2	RECOMMENDED
C_{SS_TR}	SS_TR	GND (PowerPAD)	See *Buck Converter*

8.2.2.1 Gate Drive Average Current Load

The gate drive supply (GVDD) of the DRV8301-Q1 can deliver up to 30 mA (RMS) of current to the external power MOSFETs. Use Equation 3 to determine the approximate RMS load on the gate drive supply:

Gate Drive RMS Current = MOSFET Qg × Number of Switching MOSFETs × Switching Frequency (3)

Example:

7.83 mA = 29 nC × 6 × 45 kHz

This is a rough approximation only.

8.2.2.2 Overcurrent Protection Setup

The DRV8301-Q1 provides overcurrent protection for the external power MOSFETs through the use of V_{DS} monitors for both the high side and low side MOSFETs. These are intended for protecting the MOSFET in overcurrent conditions and not for precise current regulation.

The overcurrent protection works by monitoring the V_{DS} voltage of the external MOSFET and comparing it against the OC_ADJ_SET register value. If the V_{DS} exceeds the OC_ADJ_SET value the DRV8301-Q1 takes action according to the OC_MODE register.

Overcurrent Trip = OC_ADJ_SET / MOSFET $R_{DS(on)}$ (4)

Example:

26.17 A = 0.123 V/ 4.7 mΩ

MOSFET $R_{DS(on)}$ changes with temperature and this will affect the overcurrent trip level.

8.2.2.3 Sense Amplifier Setup

The DRV8301-Q1 provides two bidirectional low-side current shunt amplifiers. These can be used to sense a sum of the three half-bridges, two of the half-bridges individually, or in conjunction with an additional shunt amplifier to sense all three half-bridges individually.

1. Determine the peak current that the motor will demand (I_{MAX}). This will be dependent on the motor parameters and your specific application. $I_{(MAX)}$ in this example is 14 A.
2. Determine the available voltage range for the current shunt amplifier. This will be ± half of the amplifier reference voltage (V_{REF}). In this case the available range is ±1.65 V.
3. Determine the sense resistor value and amplifier gain settings. There are common tradeoffs for both the sense resistor value and amplifier gain. The larger the sense resistor value, the better the resolution of the half-bridge current. This comes at the cost of additional power dissipated from the sense resistor. A larger gain value will allow you to decrease the sense resistor, but at the cost of increased noise in the output signal. This example uses a 0.01-Ω sense resistor and the minimum gain setting of the DRV8301-Q1 (10 V/V). These values allow the current shunt amplifiers to measure ±16.5 A (some additional margin on the 14 A requirement).

8.2.3 Application Curves

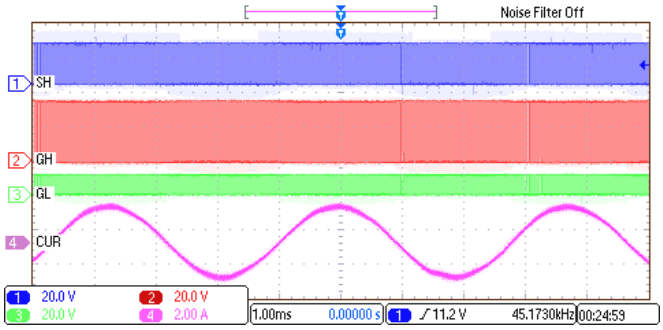


Figure 8. Motor Spinning 2000 RPM

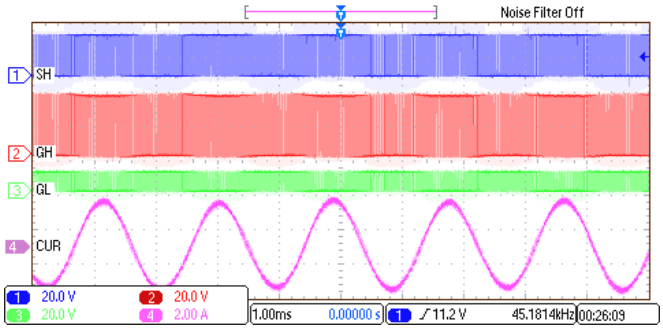


Figure 9. Motor Spinning 4000 RPM

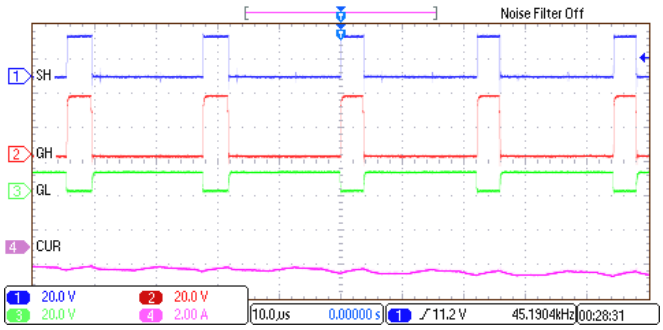


Figure 10. Gate Drive 20% Duty Cycle

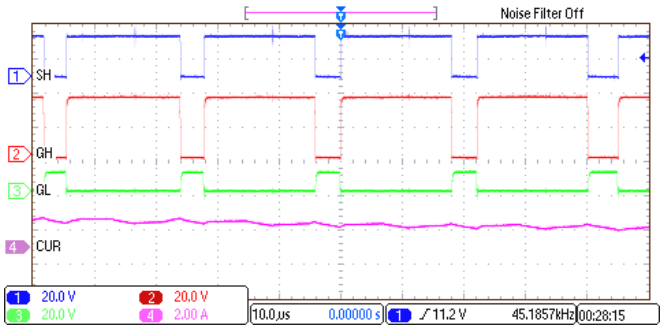


Figure 11. Gate Drive 80% Duty Cycle

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and its ability to source or sink current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

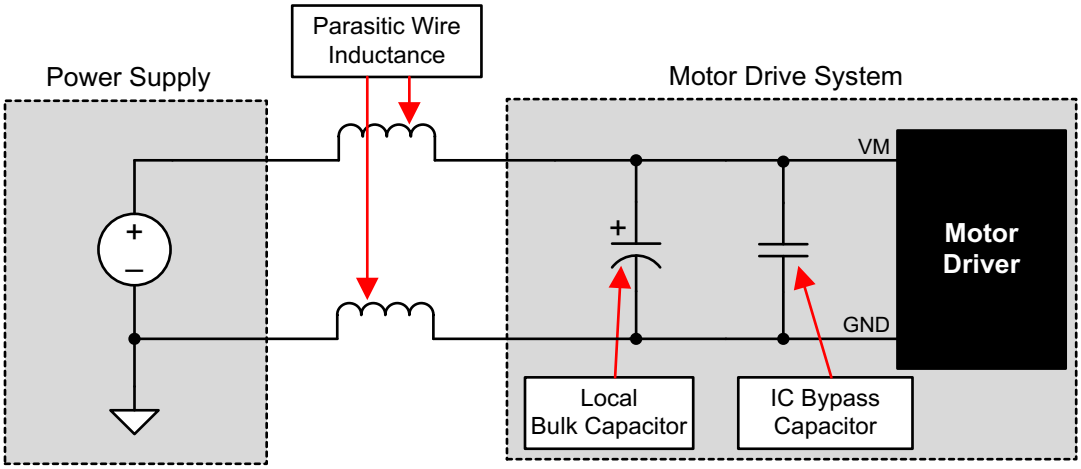


Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

Use these layout recommendations when designing a PCB for the DRV8301-Q1.

- The DRV8301-Q1 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered (See *PowerPAD™ Thermally Enhanced Package* application report, SLMA002).
- PVDD bypass capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD).
- GVDD bypass capacitor should be placed close its corresponding pin with a low impedance path to device GND (PowerPAD).
- AVDD and DVDD bypass capacitors should be placed close to their corresponding pins with a low impedance path to the AGND pin. It is preferable to make this connection on the same layer.
- AGND should be tied to device GND (PowerPAD) through a low impedance trace/copper fill.
- Add stitching vias to reduce the impedance of the GND path from the top to bottom side.
- Try to clear the space around and underneath the DRV8301-Q1 to allow for better heat spreading from the PowerPAD.

10.2 Layout Example

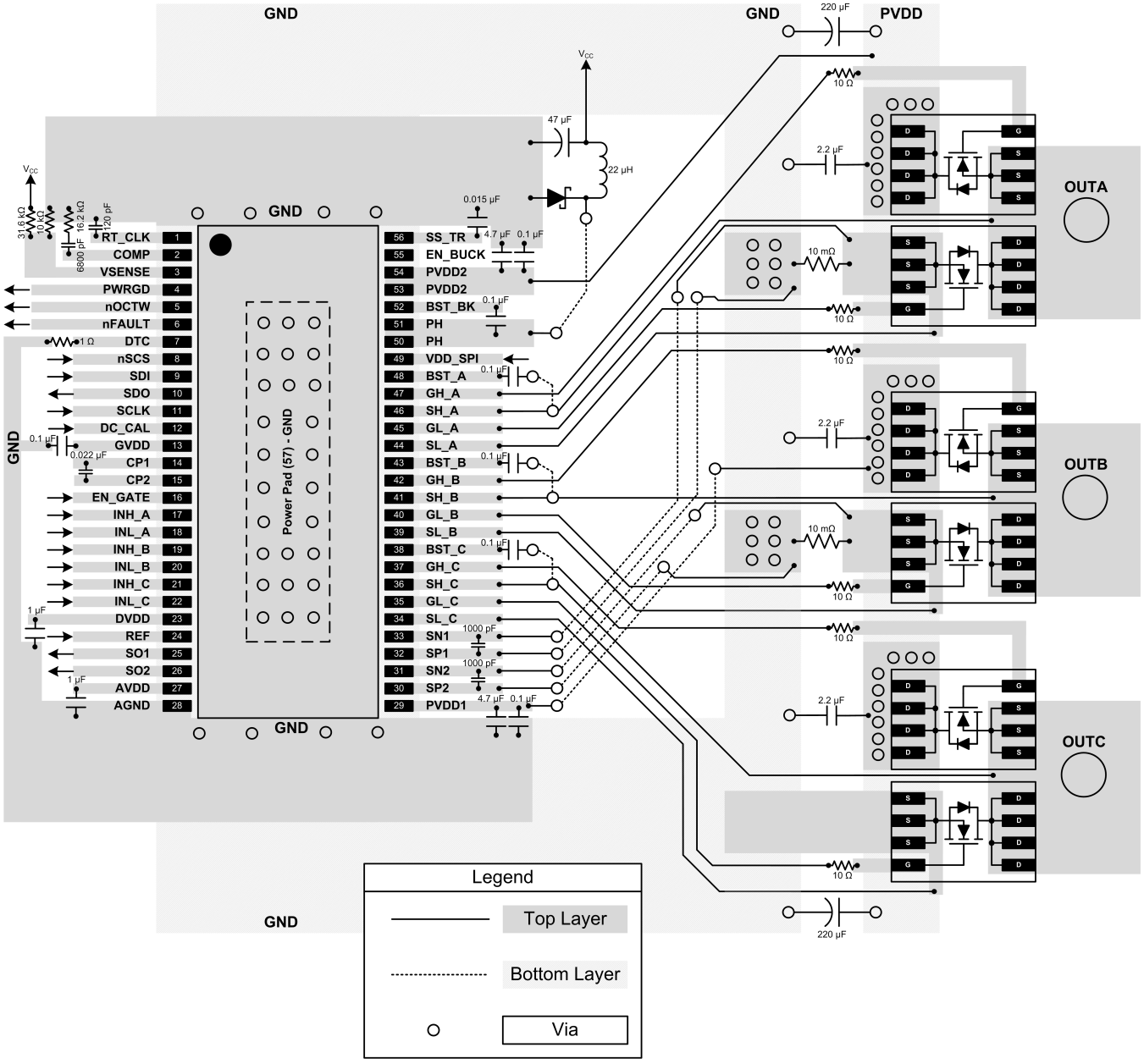


Figure 13. Top and Bottom Layer Layout Schematic

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *TPS54160 1.5-A, 60-V, Step-Down DC/DC Converter with Eco-mode™*, SLVSB56

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8301QDCAQ1	NRND	Production	HTSSOP (DCA) | 56	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q
DRV8301QDCAQ1.A	NRND	Production	HTSSOP (DCA) | 56	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q
DRV8301QDCARQ1	NRND	Production	HTSSOP (DCA) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q
DRV8301QDCARQ1.A	NRND	Production	HTSSOP (DCA) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

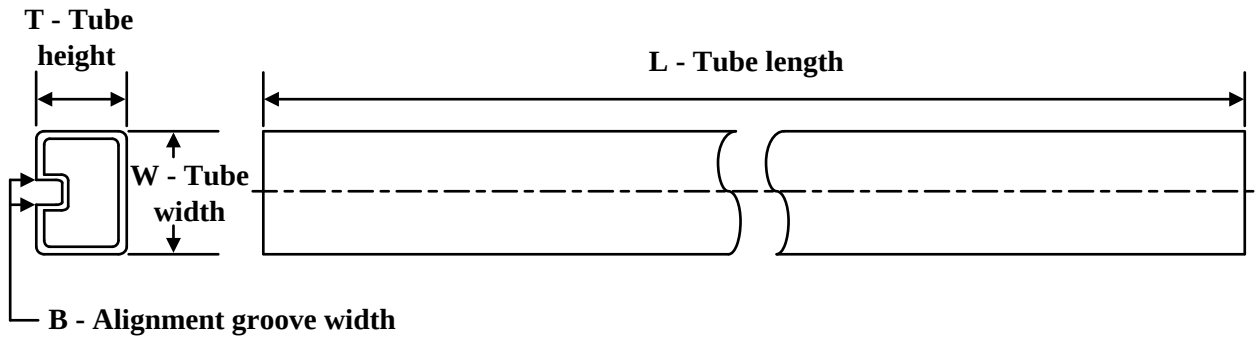
OTHER QUALIFIED VERSIONS OF DRV8301-Q1 :

- Catalog : DRV8301

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8301QDCAQ1	DCA	HTSSOP	56	35	530	11.89	3600	4.9
DRV8301QDCAQ1.A	DCA	HTSSOP	56	35	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

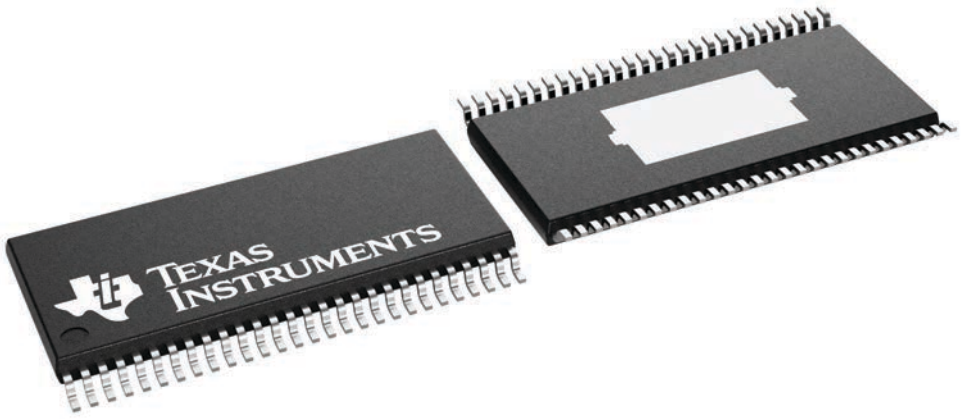
DCA 56

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 14, 0.5 mm pitch

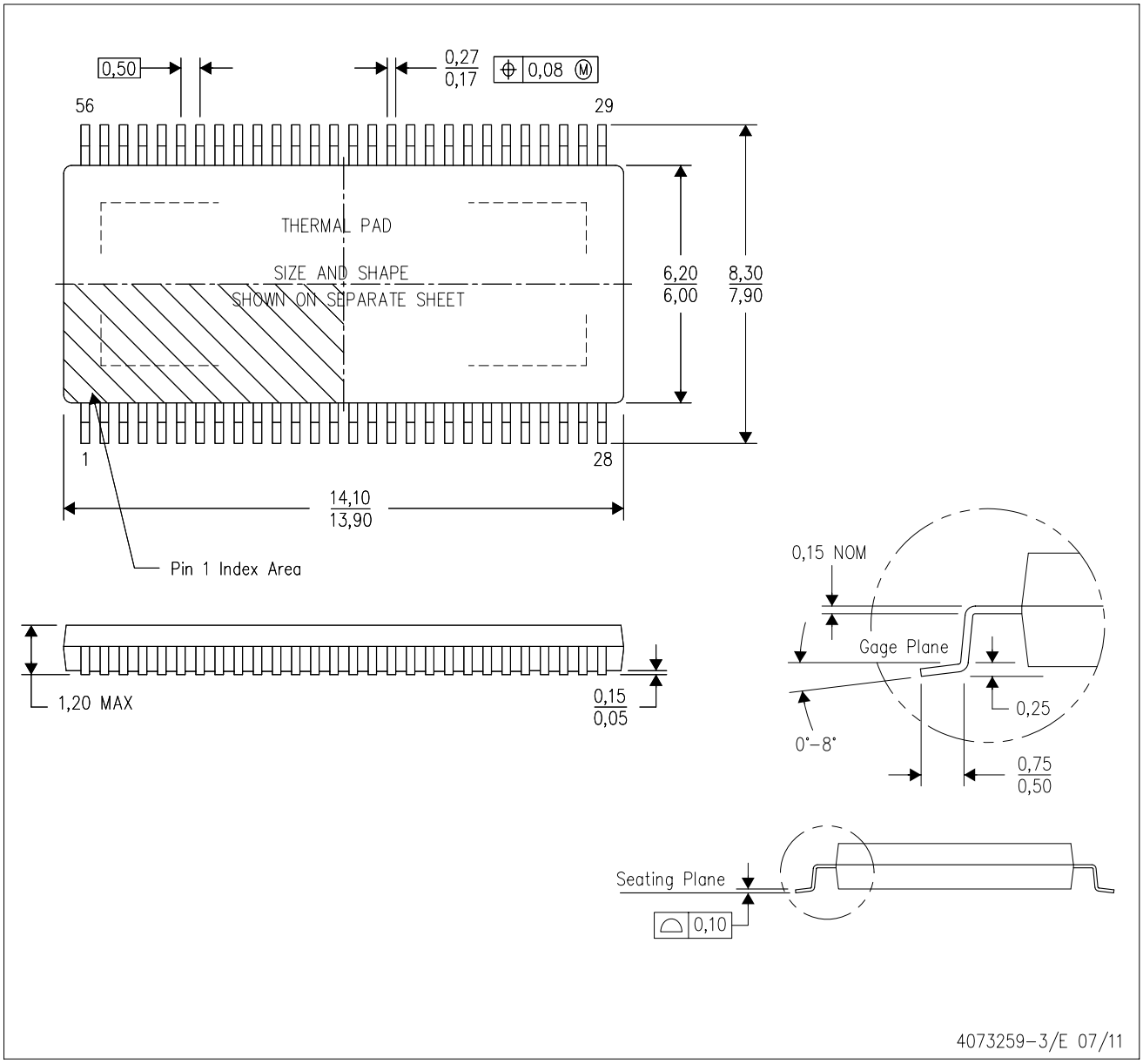
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231600/A

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

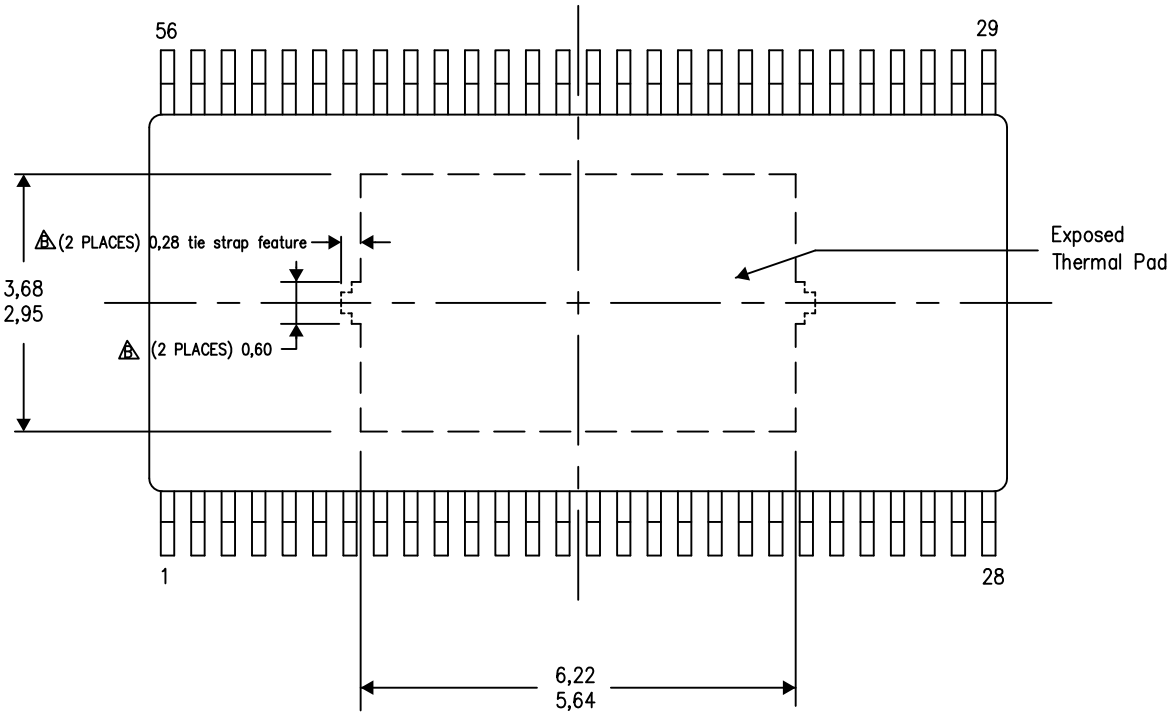
DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

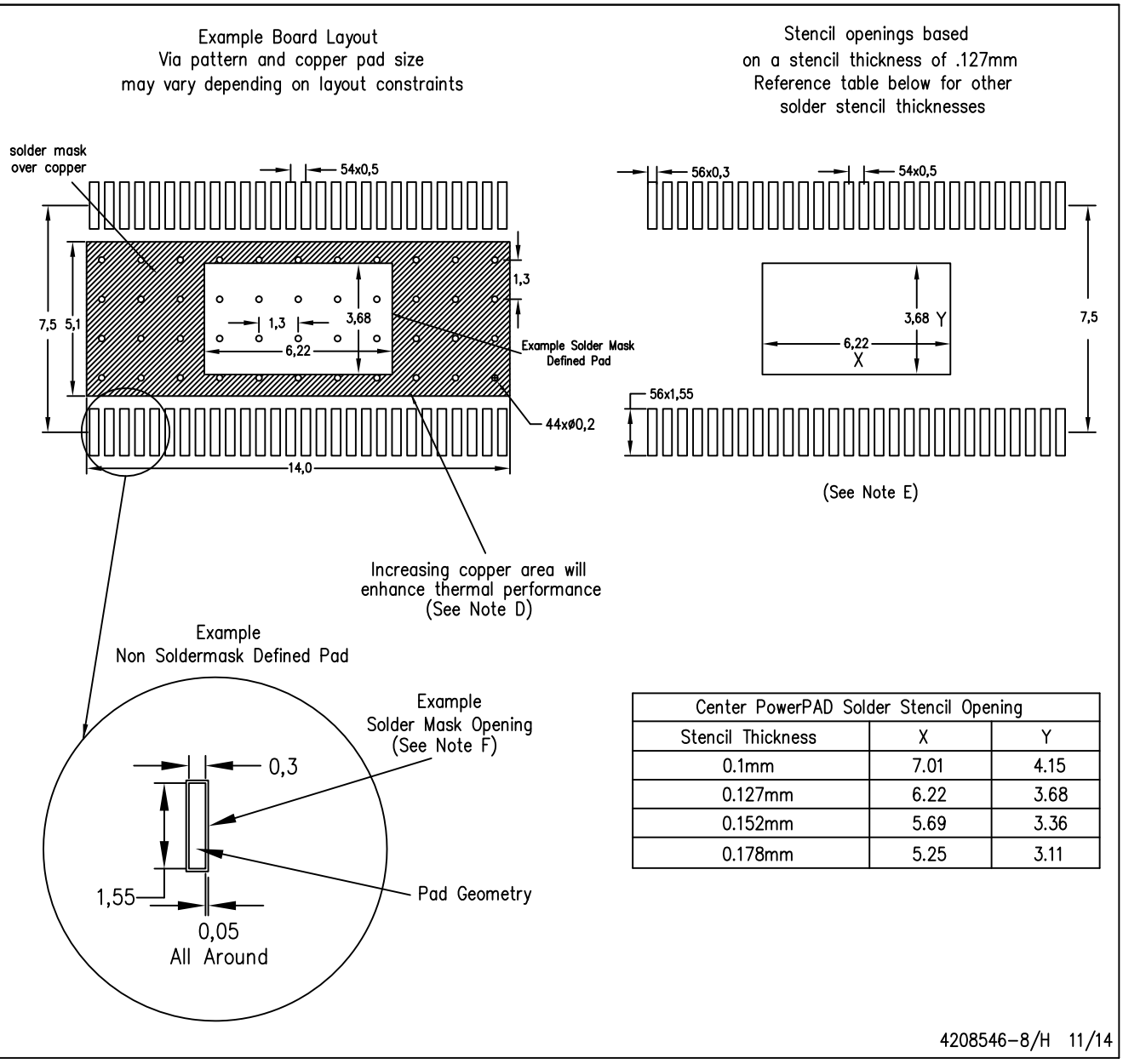
4206320–13/S 11/14

NOTES: A. All linear dimensions are in millimeters

B. Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.01	4.15
0.127mm	6.22	3.68
0.152mm	5.69	3.36
0.178mm	5.25	3.11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Last updated 10/2025