DRV8374-Q1 Three-Phase Integrated FET Motor Driver

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1 Features

- 4.5V to 35V operating voltage (40V abs max)
- High output current capability: 40A Peak
- Low MOSFET on-state resistance
  - 17mΩ $R_{DS(ON)}$ (HS + LS) at T_A = 25°C
- Reduced switching loss with 850V/us slew rate and reverse recovery loss minimization technique
  - Adjustable slew rate options
- Low audible noise and ease of motor control with ultra-low dead time < 100ns, and propagation delay < 100ns
- Low power sleep mode
  - 3.6µA typical at V_{VM} = 24V, T_A = 25°C
- Multiple control interface options
  - 6x PWM control interface
  - 3x PWM control interface
- Supports up to 200kHz PWM frequency
- Does not require external current sense resistors, built-in current sensing
- Flexible device configuration option
  - DRV8374S-Q1: 5MHz 16-bit SPI for device configuration and fault status
  - DRV8374H-Q1: Hardware pin based configuration
- Supports 1.8V, 3.3V, and 5V logic inputs
- Built-in 5V (5%), 30mA LDO regulator (Except for DRV8374G-Q1)
- Integrated protection features
  - Supply under-voltage lockout (UVLO)
  - Charge pump under-voltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal warning and shutdown (OTW/OTSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over SPI

2 Applications

- Brushless-DC (BLDC) Motor Modules
- HVAC motors
- Office automation machines
- Factory automation and robotics
- Automotive HVAC control module

3 Description

The DRV8374-Q1 provides a single-chip power stage device for customers driving 4.5V to 35V brushless-DC motors. The DRV8374 integrates three 1/2-H bridges with 40V absolute maximum capability and a very low $R_{DS(ON)}$ of 17mΩ (high-side plus low-side) to enable high power drive capability. Current is sensed using an integrated current sensing feature which eliminates the need for external sense resistors. Power management features with integrated LDO generate the necessary voltage rails for the device and can be used to power external circuits.

DRV8374-Q1 implements a 6x or 3x PWM control scheme which can be used to implement sensored or sensorless field-oriented control (FOC), sinusoidal control, or trapezoid control using an external microcontroler. The DRV8374 is capable of driving a PWM frequency up to 200kHz. The control scheme is highly configurable through hardware pins or register settings ranging from motor current limiting behavior to fault response.

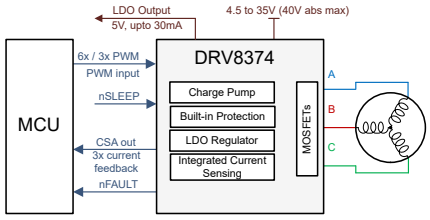
There are a large number of protection features integrated into , intended to protect the device, motor, and system against fault events. Refer Section 10.1 for design consideration and recommendation on device usage.

There are a large number of protection features integrated into DRV8374, intended to protect the device, motor, and system against fault events. Refer Section 10.1 for design consideration and recommendation on device usage.

Device Information

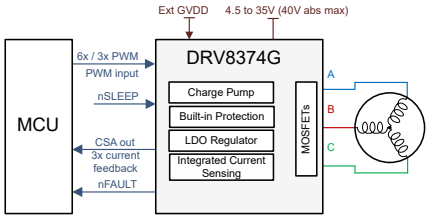
PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
PDRV8374HQVERRQ1(2)	VQFN (23)	6.00mm x 4.00mm
PDRV8374HQVEORQ1(2)	VQFN (29)	7.00mm x 5.00mm
PDRV8374SQVEORQ1	VQFN (29)	7.00mm x 5.00mm
PDRV8374GSQVEORQ1(2)	VQFN (29)	7.00mm x 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Device available for preview only.



Simplified Schematics for DRV8374H/S

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.



Simplified Schematic for DRV8374G

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4 Revision History

DATE	REVISION	NOTES
August 2026	*	Initial release.

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5 Device Comparison Table

DEVICE	PACKAGES	INTERFACE
DRV8374H-Q1	23-pin VQFN (6x4 mm)	Hardware, Internal GVDD supply
DRV8374S-Q1	29-pin VQFN (7x5 mm)	SPI, Internal GVDD supply
DRV8374H-Q1		Hardware, Internal GVDD supply

Table 5-1. DRV8374S-Q1 (29 pin SPI variant) vs. DRV8374H-Q1 (29 pin Hardware variant) vs.DRV8374GS-Q1 (29 pin SPI variant, Extrenal GVDD) configuration comparison

Parameters	DRV8374S-Q1 (SPI variant 29 pin)	DRV8374H-Q1 (Hardware variant 29 pin)	DRV8374GS-Q1 (SPI variant 29 pin External GVDD)
PWM mode settings	PWM_MODE (4 settings)	MODE_SR pin (4 settings)	PWM_MODE (4 settings)
Slew rate settings	SLEW_RATE (4 settings)	SLEW pin (4 settings)	SLEW_RATE (4 settings)
CSA gain settings	CSA_GAIN (4 settings)	GAIN pin (4 settings)	CSA_GAIN (4 settings)
SDO pin configuration: mode, voltage	SDO_ODEN (2 settings), SDO_MD (2 settings)	NA	SDO_ODEN (2 settings), SDO_MD (2 settings)
Current Limit configuration: Mode, reporting on nFAULT, Blanking time, 100% duty PWM frequency	ILIMFLT_MODE (2 settings),ILIM_MODE (2 settings), ILIM_BLANK_SEL (4 settings), PWM_100_FREQ_SEL (4 settings)	Current limit reporting on nFAULT is enabled, fixed to coast mode, blanking time set to 5.6µs for slew rate of 50V/µs and 1.8µs for all other slew rates, the 100% duty input PWM cycle is fixed to 20kHz	ILIMFLT_MODE (2 settings),ILIM_MODE (2 settings), ILIM_BLANK_SEL (4 settings), PWM_100_FREQ_SEL (4 settings)
Over voltage protection mode	OVP_MODE (2 settings), OVP_SEL (2 settings)	Over voltage protection is disabled	OVP_MODE (2 settings), OVP_SEL (2 settings)
OCP configuration: Mode, level, deglitch	OCP_MODE (4 settings), OCP_LVL (2 settings),OCP_DEG (4 settings) and OCP_TRETRY (2 settings)	Enabled with automatic retry mode, level is fixed to 50A with 1.2µs deglitch time, 5ms retry time	OCP_MODE (4 settings), OCP_LVL (2 settings),OCP_DEG (4 settings) and OCP_TRETRY (2 settings)
Active demagnetization: Enable, comparator threshold, comparator mask time, behaviour during fault	EN_ASR (2 settings), EN_AAR (2 settings), AD_COMP_TH_HS & AD_COMP_TH_LS	MODE_SR (2 settings), active demag comparator threshold set to 500mA, comparator mask time set to 5.6µs for slew rate of 50V/µs and 1.8µs for all other slew rates. ADMAG_TMARGIN set to 1.6µs, active demag is disabled during OCP.	EN_ASR (2 settings), EN_AAR (2 settings), AD_COMP_TH_HS & AD_COMP_TH_LS
Over temperature warning	OTW_MODE (2 settings)	Reported on nFAULT	OTW_MODE (2 settings)

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6 Pin Configuration and Functions

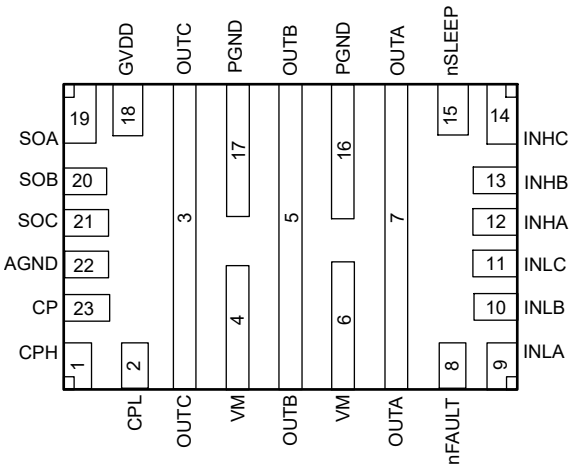


Figure 6-1. DRV8374-Q1 23-Pin VQFN Top View

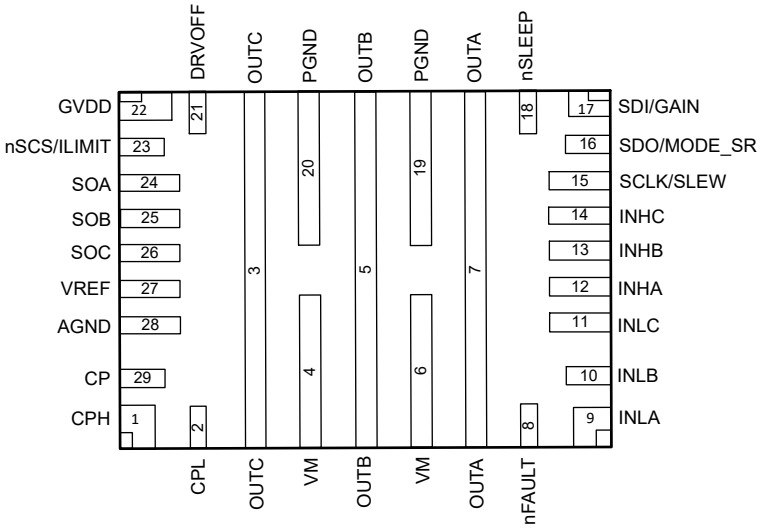


Figure 6-2. DRV8374-Q1 29-Pin VQFN Top View

Table 6-1. DRV8374-Q1 Pin Functions

PIN	23-pin VQFN Package	29-pin VQFN Package			TYPE[1]	DESCRIPTION
NAME	DRV8374H	DRV8374H	DRV8374S	DRV8374G		
AGND	22	28	28	28	GND	Device analog ground. Refer Section 10.3.1 for connections recommendation.
CP	23	29	29	29	PWR O	Charge pump output. Connect a X5R or X7R, 1µF, 16V ceramic capacitor between the CP and VM pins.
CPH	1	1	1	1	I	Charge pump switching node. Connect a X5R or X7R, 100nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage CPL rating at least twice the normal operating voltage of the device.
CPL	2	2	2	2	I	
DRVOFF	-	21	21	21	I	When this pin is pulled high the six MOSFETs in the power stage are turned OFF making all outputs Hi-Z.

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Table 6-1. DRV8374-Q1 Pin Functions (continued)

PIN	23-pin VQFN Package	29-pin VQFN Package			TYPE[1]	DESCRIPTION
NAME	DRV8374H	DRV8374H	DRV8374S	DRV8374G		
GAIN	-	17	-	-	I	Current sense amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GVDD	18	22	22	22	PWR I/O	For DRV8374H/S: 5V internal regulator output. Connect an X5R or X7R, 1µF, 10V ceramic capacitor between the GVDD and AGND pins. This regulator can source up to 30mA externally. For DRV8374G: External power supply input for the internal predriver. Connect an X5R or X7R, 1µF, 10V ceramic capacitor between the GVDD and AGND pins.
ILIMIT	-	23	-	-		Sets the threshold for phase current used in cycle by cycle current limit.
INHA	12	12	12	12	I	High-side driver control input for OUTA. This pin controls the output of the high-side MOSFET.
INHB	13	13	13	13	I	High-side driver control input for OUTB. This pin controls the output of the high-side MOSFET.
INHC	14	14	14	14	I	High-side driver control input for OUTC. This pin controls the output of the high-side MOSFET.
INLA	9	9	9	9	I	Low-side driver control input for OUTA. This pin controls the output of the low-side MOSFET.
INLB	10	10	10	10	I	Low-side driver control input for OUTB. This pin controls the output of the low-side MOSFET.
INLC	11	11	11	11	I	Low-side driver control input for OUTC. This pin controls the output of the low-side MOSFET.
MODE_SR	-	16	-	-	I	PWM input mode setting. This pin is a 4-level input pin set by an external resistor.
nFAULT	8	8	8	8	O	Fault indicator. The fault indicator is configured as an open-drain output, pulled logic-low when a fault condition is detected. An external pull-up resistor to a voltage between 1.8V and 5V is required for operation. If an external supply is used for the pull-up, the voltage must be pulled above 2.2V during power-up to prevent the device from being entered into test mode.
nSCS	-	-	23	23	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	15	18	18	18	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 20 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
OUTA	7	7	7	7	PWR O	Half bridge output A
OUTB	5	5	5	5	PWR O	Half bridge output B
OUTC	3	3	3	3	PWR O	Half bridge output C
PGND	16, 17	19, 20	19, 20	19, 20	GND	Device power ground. Refer Section 10.3.1 for connections recommendation.
SCLK	-	-	15	15	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	-	-	17	17	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	-	-	16	16	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SLEW	-	15	-	-	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor.

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Table 6-1. DRV8374-Q1 Pin Functions (continued)

PIN	23-pin VQFN Package	29-pin VQFN Package			TYPE[1]	DESCRIPTION
NAME	DRV8374H	DRV8374H	DRV8374S	DRV8374G		
SOA	19	24	24	24	O	Current sense amplifier output for phase A. For 29-pin variant of DRV8374H/S: The current sense amplifier output is a voltage proportional to the low side FET current. Supports capacitive load or low pass filter (resistor in series and capacitor to GND). For 23-pin variant of DRV8374H: The current sense amplifier output is a current proportional to the low side FET current. Refer Section 8.3.10.1 for more details
SOB	20	25	25	25	O	Current sense amplifier output for phase B. For 29-pin variant of DRV8374H/S: The current sense amplifier output is a voltage proportional to the low side FET current. Supports capacitive load or low pass filter (resistor in series and capacitor to GND). For 23-pin variant of DRV8374H: The current sense amplifier output is a current proportional to the low side FET current.Refer Section 8.3.10.1 for more details
SOC	21	26	26	26	O	Current sense amplifier output for phase C. For 29-pin variant of DRV8374H/S: The current sense amplifier output is a voltage proportional to the low side FET current. Supports capacitive load or low pass filter (resistor in series and capacitor to GND). For 23-pin variant of DRV8374H: The current sense amplifier output is a current proportional to the low side FET current. Refer Section 8.3.10.1 for more details.
VM	4, 6	4, 6	4, 6	4, 6	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with two 0.1µF capacitors (for each pin) plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
VREF	-	27	27	27	PWR I	Current sense amplifier reference. Connect a X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the VREF and AGND pins.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (PGND, AGND)	–0.6	0.6	V
Charge pump voltage (CP, CPH)	–0.3	V_M + 6	V
Charge pump negative switching pin voltage (CPL)	-0.3	V_M + 0.3	V
Analog regulators pin voltage (GVDD)	–0.3	5.75	V
Analog regulators pin voltage (GVDD), External	-0.3	5.75	V
Analog pin input voltage (VREF, ILIMIT)	-0.3	5.75	V
Analog pin output voltage (SOx)	-0.3	5.75	V
Logic pin input voltage (INHx, INLx,nSCS, SCLK, SDI)	–0.3	5.75	V
Logic pin input voltage (nSLEEP, DRVOFF)	-0.3	40	V
Logic pin output voltage (SDO)	–0.3	5.75	V
Logic pin output voltage (nFAULT)	-0.3	40	V
Multi-level pin input voltage (GAIN, MODE_SR, SLEW)	-0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings AUTO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			200	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			40	A
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI	–0.1		5.5	V
V_{IN}	Multilevel input voltage	GAIN, MODE_SR, SLEW	-0.1		GVDD	V
V_{OD}	Open drain pullup voltage	nFAULT, SDO, FG	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	-0.1		GVDD	V
I_{OD}	Open drain output current	nFAULT, SDO, FG			5	mA

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over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VREF}	Voltage reference pin voltage	VREF	2.2		5.5	V
ILIMIT	Voltage reference for current limit	ILIMIT	-0.1		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DRV8374H,DRV8374S		UNIT
		29 Pins	23 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.42	26.23	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.09	4.87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.34	15.51	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.34	0.41	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.35	6.98	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (INTERNAL GVDD)						
I_{VMQ}	VM sleep mode current	V_{VM} > 6V, nSLEEP = 0, T_A = 25 °C		3.6	5.5	µA
		nSLEEP = 0		3.6	6.7	µA
I_{VMS}	VM standby mode current	V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C		2.5	3	mA
		nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF'		2.5	3.4	mA
I_{VM}	VM operating mode current	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 20 kHz		6.5	7.8	mA
		nSLEEP =1, f_{PWM} = 20 kHz		6.5	8	mA
		nSLEEP =1, f_{PWM} =100 kHz		21.5	28.2	mA
V_{GVDD}	Analog regulator voltage	0 mA ≤ I_{GVDD} ≤ 30 mA; (External Load); VM > 6V	4.75	5	5.25	V
V_{GVDD}	Analog regulator voltage	0 mA ≤ I_{GVDD} ≤ 15 mA; (External Load); VM = 4.5V	3.7		4.5	V
I_{GVDD}	External analog regulator load				30	mA
I_{SC_GVDD}	Short circuit current on GVDD	Short GVDD to 4.5 (VM>6V)	50		100	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM (VM > 5V)	4	5	6	V
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM (4.5V < VM < 5V)	3.5	4.5	5	V
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			5.5	ms
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
POWER SUPPLIES (EXTERNAL GVDD - only for DRV8374G)						
I_{VMQ}	VM sleep mode current	V_{VM} > 6V, nSLEEP = 0, T_A = 25 °C		3.5	5.5	µA
I_{VMQ}	VM sleep mode current	nSLEEP = 0		3.5	6.7	µA

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T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VMQ}	VM standby mode current	V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C		0.4	0.8	mA
I_{VMQ}	VM standby mode current	nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF'		0.35	0.9	mA
I_{VMQ}	VM operating mode current	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 20 kHz, T_A = 25 °C		2.9	4.4	mA
I_{VMQ}	VM operating mode current	nSLEEP =1, f_{PWM} = 20 kHz		2.9	4.6	mA
I_{VMQ}	VM operating mode current	nSLEEP =1, f_{PWM} =100 kHz		14.5	20	mA
I_{GVDD}	GVDD sleep mode current	nSLEEP = 0, T_A = 25 °C			100	µA
I_{GVDD}	GVDD sleep mode current	nSLEEP = 0			130	µA
I_{GVDD}	GVDD standby mode current	nSLEEP = 1,INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C		1.9	2.3	mA
I_{GVDD}	GVDD standby mode current	nSLEEP = 1,INHx = INLx = 0, SPI = 'OFF'			2.5	mA
I_{GVDD}	GVDD operating mode current	nSLEEP =1, f_{PWM} = 20 kHz		2.7	3.3	mA
I_{GVDD}	GVDD operating mode current	nSLEEP =1, f_{PWM} = 100 kHz		7.5	9	mA
t_{wake}	Wake up time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			5.5	ms
LOGIC-LEVEL INPUTS (DRVOFF, INHx, INLx, nSLEEP, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	nSLEEP, INLx, DRVOFF	1.6		5.5	V
		Other Pins	1.5		5.5	V
V_{HYS}	Input logic hysteresis	nSLEEP	240	450	570	mV
		Other PIns	180	300	500	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	nSLEEP, DRVOFF, V_{PIN} (Pin Voltage) = 5 V	5		35	µA
I_{IH}	Input logic high current	Other pins, V_{PIN} (Pin Voltage) = 2 V	15		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	300	kΩ
R_{PD}	Input pulldown resistance	DRVOFF	150	200	300	kΩ
t_{FILT}	Filter time constant	DRVOFF	1	2	3	µs
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		180	350	550	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–1		25	µA
R_{PU}	Input pullup resistance		160	200	260	kΩ
C_{ID}	Input capacitance			30		pF
FOUR-LEVEL INPUTS (GAIN, MODE_SR, SLEW)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.2*GVDD	V
V_{L2}	Input mode 2 voltage	Hi-Z	0.27*GVDD	0.5*GVDD	0.55*GVDD	V
V_{L3}	Input mode 3 voltage	94 kΩ +/- 5% tied to GVDD	0.6*GVDD	0.76*GVDD	0.9*GVDD	V

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T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{L4}	Input mode 4 voltage	Tied to GVDD	0.95*GVDD		GVDD	V
R_{PU}	Input pullup resistance	To GVDD	120	200	260	kΩ
R_{PD}	Input pulldown resistance	To AGND	120	200	260	kΩ
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA, push-pull	3.4		5.5	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V,	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		17	21	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		17.5	21.5	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		29	33	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		30	34	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 2 A	430	850	1360	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 2 A	250	480	760	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 95.3 kΩ +/- 5% to GVDD, I_{OUTx} = 2 A	120	250	380	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 2 A	22	45	90	V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 2 A	430	975	1360	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 2 A	250	480	760	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 95.3 kΩ +/- 5% to GVDD, I_{OUTx} = 2 A	120	250	380	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 2 A	22	64	90	V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			0.3	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, HS driver ON to LS driver OFF		65	130	ns
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, HS driver ON to LS driver OFF		100	200	ns
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 95.3 kΩ +/- 5% to GVDD, HS driver ON to LS driver OFF		100	230	ns
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, HS driver ON to LS driver OFF		125	550	ns

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T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24 V, = 1 to OUTx transisition, SLEW = 00b or SLEW pin tied to AGND		26	65	ns
		V_{VM} = 24 V, = 1 to OUTx transisition, SLEW = 01b or SLEW pin to Hi-Z		30	75	ns
		V_{VM} = 24 V, = 1 to OUTx transisition, SLEW = 10b or SLEW pin to 95.3 kΩ +/- 5% to GVDD		60	105	ns
		V_{VM} = 24 V, = 1 to OUTx transisition, SLEW = 11b or SLEW pin tied to GVDD		500	800	ns
t_{MIN_PULSE}	Minimum output pulse width	SLEW = 00b or SLEW pin tied to AGND	100			ns
CURRENT SENSE (23 PIN PACKAGE)						
G_{CSA}	Current sense scaling gain			0.04		mA/A
G_{CSA_ERR}	Current sense scaling gain error	T_J = 25°C, RLOAD < 2.5 kΩ	-3		3	%
G_{CSA_ERR}	Current sense scaling gain error	T_J = 25°C, 2.5 kΩ < RLOAD < 5 kΩ	-6		6	%
G_{CSA_ERR}	Current sense scaling gain error	RLOAD < 2.5 kΩ	-5		5	%
G_{CSA_ERR}	Current sense scaling gain error	2.5 kΩ < RLOAD < 5 kΩ	-7		7	%
I_{MATCH}	Current sense scaling mismatch between phases	T_J = 25°C, RLOAD < 2.5 kΩ	-4.3		4.3	%
I_{MATCH}	Current sense scaling mismatch between phases	T_J = 25°C, 2.5 kΩ < RLOAD < 5 kΩ	-8.5		8.5	%
I_{MATCH}	Current sense scaling mismatch between phases	RLOAD < 2.5 kΩ	-6		6	%
I_{MATCH}	Current sense scaling mismatch between phases	2.5 kΩ < RLOAD < 5 kΩ	-8.5		8.5	%
I_{OS_PH}	Current sense offset (refered to main fet)	LS FET current = 0	-200		200	mA
I_{DRIFT}	Current sense output drift (refered to main FET current)	LS FET current = 0	-1200		1200	µA/°C
V_{FS_CSA}	Current sense output voltage range	LS FET current < 30 A	0.35		GVDD - 0.4	V
t_{SET}	Settling time to ±2%	Step on SOx = 1.2 V, RLOAD < 2.5 kΩ, CLOAD < 30 pF, CSA output pull up Voltage = V_{MID_EXT}			1	µs
t_{SET}	Settling time to ±1%	Step on SOx = 1.2 V, RLOAD < 2.5 kΩ, CLOAD < 30 pF, CSA output pull up Voltage = V_{MID_EXT}		1.2	1.5	µs
t_{SET}	Settling time to ±1%	Step on SOx = 1.2 V, 2.5 kΩ < RLOAD < 5 kΩ, CLOAD < 30 pF, CSA output pull up Voltage = V_{MID_EXT}			3	µs
t_{DELAY}	Delay from INLx turn on to current sense amplifier turn on	SLEW_RATE = 00b			0.5	µs
PSRR	Power Supply Rejection Ratio	VM to SOx, 10 kHz	39			dB
PSRR	Power Supply Rejection Ratio	VM to SOx, 100 kHz	10			dB
R_{MIN}	Minimum equivalent resistance on CSA output		0.65			kΩ
CURRENT SENSE AMPLIFIER (29 PIN PACKAGE)						
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 00		0.04		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 01		0.08		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 02		0.16		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 03		0.32		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin tied to AGND		0.04		V/A

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T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{CSA}	Current sense gain (HW Device)	GAIN pin to Hi-Z		0.08		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin to 95.3 kΩ ± 5% to GVDD		0.16		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin tied to GVDD		0.32		V/A
G_{CSA_ERR}	Current sense gain error	TJ = 25°C, 1A < LS FET CURRRENT < 20A	-4		4	%
G_{CSA_ERR}	Current sense gain error	1A < LS FET CURRRENT < 20A	-5.5		5.5	%
G_{CSA_ERR}	Current sense gain error	TJ = 25°C, LS FET Current < 1A	-4		4	%
I_{MATCH}	Current sense gain error matching between phases A, B and C	T_A = 25°C	-4		4	%
		T_A = -40°C to 125°C	-7		7	%
FS_{POS}	Full scale positive current measurement	Current direction from PGND to OUTx in the LS FET, VREF = 3.3 V	20			A
FS_{NEG}	Full scale negative current measurement	Current direction from OUTx to PGND in the LS FET, VREF = 3.3 V			–40	A
V_{LINEAR}	SOX output voltage linear range	VREF <= VGVDD	0.25		VREF-0.25	V
V_{LINEAR}	SOX output voltage linear range	VREF > VGVDD	0.25		VGVDD - 0.25	V
t_{SET}	Settling time to ±2%, 30 pF	Step on SOX = 1.4 V			1	µs
t_{SET}	Settling time to ±1%, 30 pF	Step on SOX = 1.4 V		1.2	1.5	µs
I_{OFFSET}	Current sense offset (referred to OUTx)	T_J = 25°C, Phase current = 0 A	–150	33	150	mA
I_{DRIFT}	Current Sense Offset Drift (referred to OUTx)	Phase current = 0 A	–1000		1000	µA/°C
$t_{CSA_ON_DELAY}$	Delay from INLx turn on to current sense amplifier turn on	SR = 1000 V/µs or 500 V/µs or 250 V/µs			500	ns
$t_{CSA_ON_DELAY}$	Delay from INLx turn on to current sense amplifier turn on	SR = 50 V/µs			1500	ns
V_{VREF_GOOD}	VREF good voltage				2.2	V
I_{VREF}	VREF input current	VREF = 3.0 V, nSLEEP = 0 or 1			25	µA
PSRR	Power Supply Rejection Ratio	VM to SOx, 10 kHz	39		56	dB
		VM to SOx, 100 kHz	10		22	dB
PULSE-BY-PULSE CURRENT LIMIT						
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range (DRV8374H, MCT8374)		0		50	A
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 00b, HW variant		1.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 01b		2.25		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 10b		2.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 11b		3.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 00b, HW variant		5.5		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 01b		6		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 10b		6.5		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 11b		7.5		µs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.1	4.35	4.5	V
		VM falling	3.9	4.15	4.3	V

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T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	90	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	6	10	µs
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_MODE = 1, OVP_SEL = 0	33	34	35	V
		Supply falling, OVP_MODE = 1, OVP_SEL = 0	32.5	33.5	34.5	V
		Supply rising, OVP_MODE = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_MODE = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 0	0.8	1	1.1	V
		Rising to falling threshold, OVP_SEL = 1	0.6	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time		8.5	14	18	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.1	2.4	3.2	V
		Supply falling	1.8	2.45	2.95	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	200	210	300	mV
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply rising	3.1	3.3	3.7	V
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply falling	2.9	3.1	3.5	V
$V_{GVDD_UV_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	170	190	310	mV
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 00b or 01b	50		115	A
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 10b or 11b	25		60	A
I_{OCP}	Overcurrent protection trip point (HW Device)		50		115	A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.4	0.8	1.4	µs
		OCP_DEG = 01b	0.8	1.45	2	µs
		OCP_DEG = 10b	1.2	1.8	2.7	µs
		OCP_DEG = 11b	1.6	2.2	3.2	µs
	Overcurrent protection deglitch time (HW Device)		0.8	1.45	2	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_TRETRY = 0	4	5	6	ms
		OCP_TRETRY = 1	425	500	575	ms
t_{RETRY}	Overcurrent protection retry time (HW Device)		4	5	6	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	125	135	145	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	165	175	185	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	25	30	35	°C

7.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	500			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	200			ns

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		MIN	NOM	MAX	UNIT
t_{SCLKH}	SCLK minimum high time	100			ns
t_{SCLKL}	SCLK minimum low time	100			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

7.7 SPI Timings

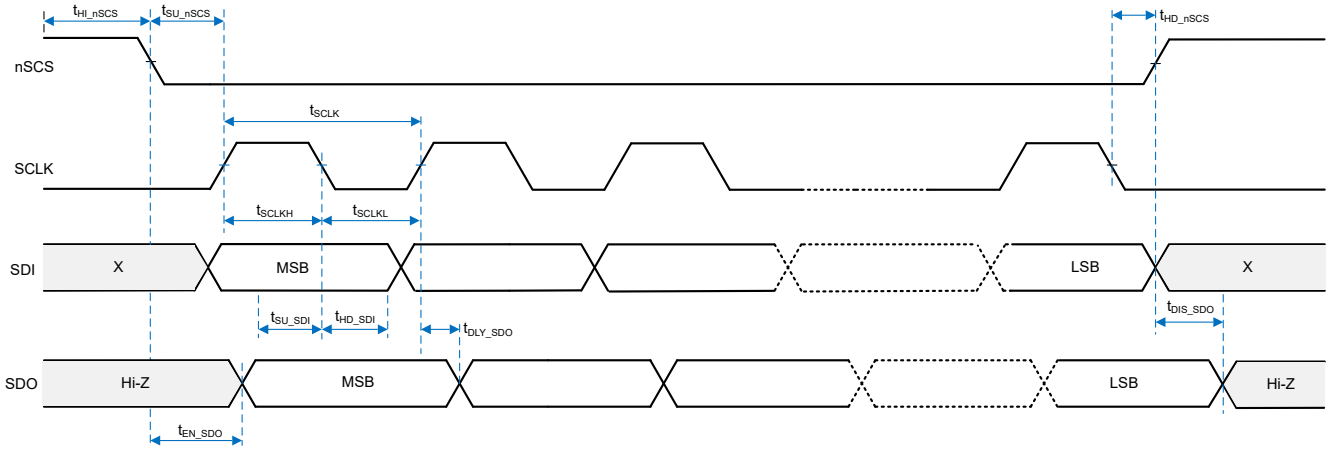


Figure 7-1. SPI Secondary Mode Timings

Note

Above timing diagram applicable for SPI in push-pull mode

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8 Detailed Description

8.1 Overview

The DRV8374-Q1 device is an integrated 17-mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, current sense amplifiers, and linear regulator for the external load. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET.

The DRV8374-Q1 device integrates three, bidirectional current-sense amplifiers for monitoring the current through each of the low side MOSFET using a built-in current sense. The gain setting of the amplifier can be adjusted through the SPI or hardware interface.

In addition to the high level of device integration, the DRV8374-Q1 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), GVDD undervoltage lockout (GVDD_UV) and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV8374-Q1 device in VQFN hotrod surface-mount packages of 6 mm x 4 mm (23-pin) and 7 mm x 5 mm (29-pin).

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8.2 Functional Block Diagram

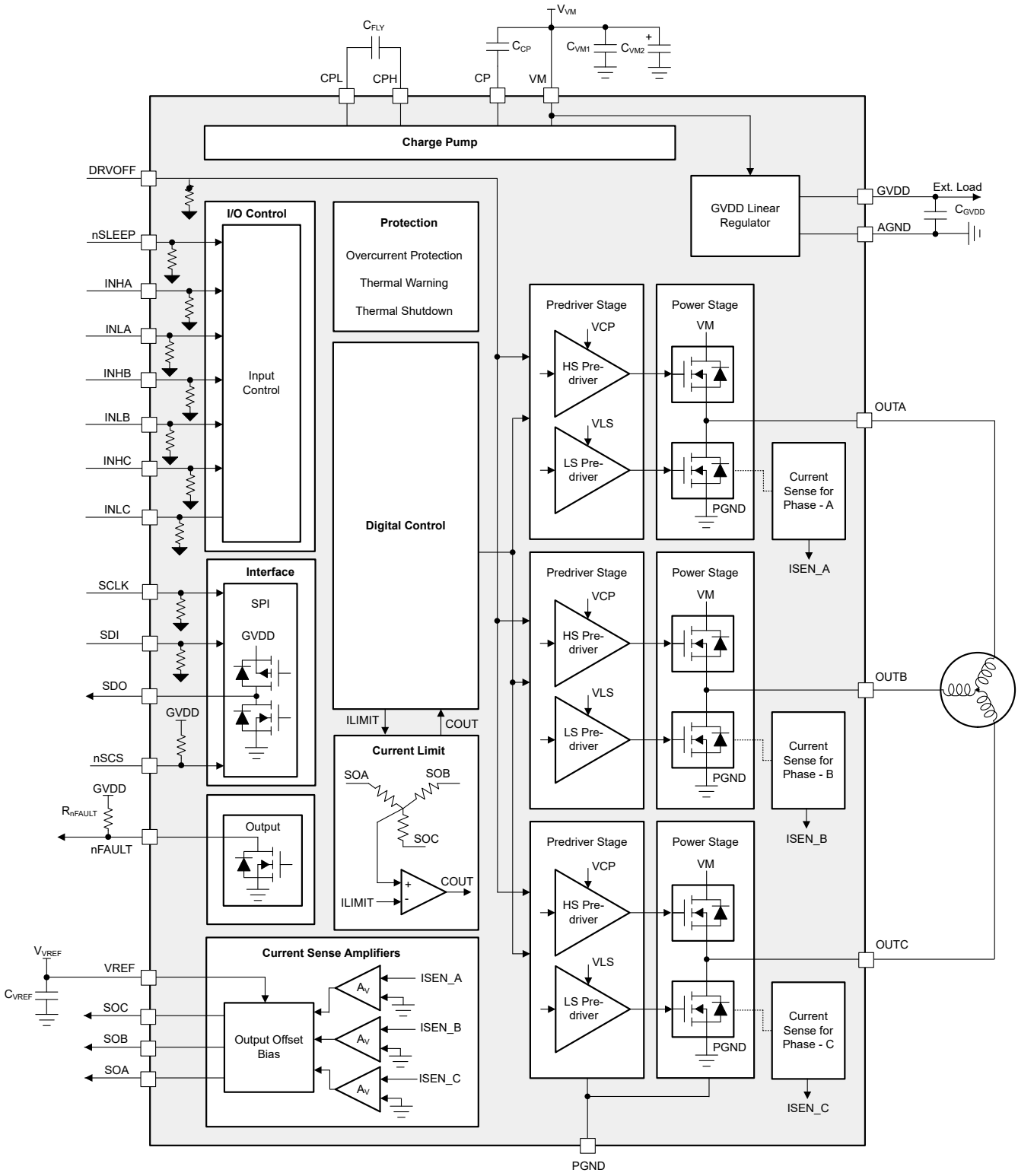


Figure 8-1. DRV8374S Block Diagram

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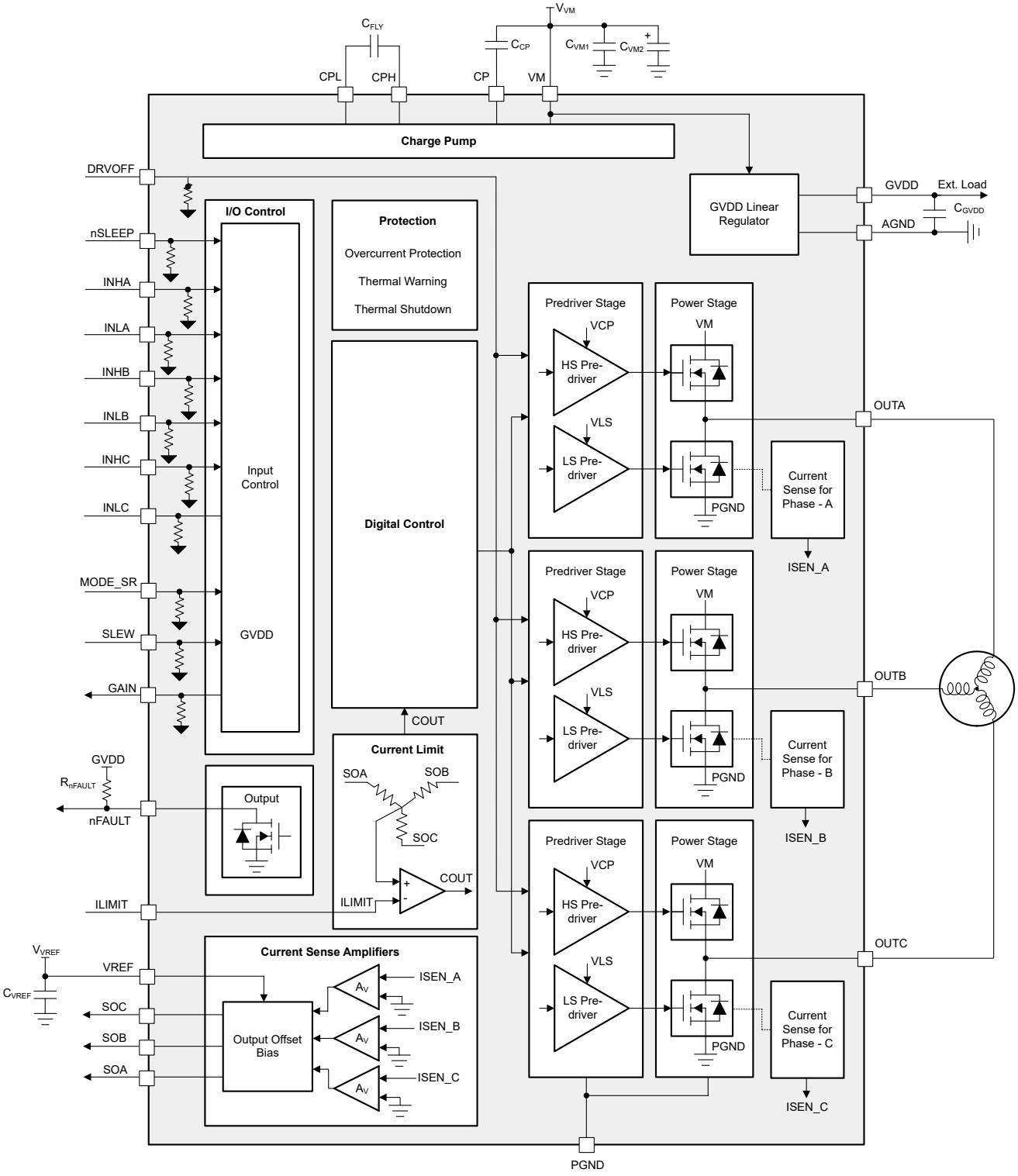


Figure 8-2. DRV8374H Block Diagram

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8.3 Feature Description

lists the recommended values of the external components for the driver.

Note

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable device behaviour.

8.3.1 Output Stage

The DRV8374-Q1 device consists of an integrated 17mΩ (combined high-side and low-side FETs on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

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8.3.2 Control Modes

The family of devices provides four different control modes to support various commutation and control methods. Table 8-1 shows the various modes of the DRV8374-Q1 device.

Table 8-1. PWM Control Modes

MODE Type	MODE_SR Pin (Hardware Variant)	PWM_MODE Bits (SPI Variant)	SR Bits (SPI Variant)	PWM MODE	ASR and AAR Mode
Mode 1	Connected to AGND	PWM_MODE = 0	EN_ASR = 0, EN_AAR = 0	6x Mode	ASR and AAR Disabled
Mode 2	Hi-Z	PWM_MODE = 0	EN_ASR = 1, EN_AAR = 0	6x Mode	ASR Enabled and AAR Disabled
Mode 3	Connected to GVDD with R_{MODE}	PWM_MODE = 1	EN_ASR = 0, EN_AAR = 0	3x Mode	ASR and AAR Disabled
Mode 4	Connected to GVDD	PWM_MODE = 1	EN_ASR = 1, EN_AAR = 0	3x Mode	ASR Enabled and AAR Disabled

Note

The MODE_SR pin is sensed only during power up and the device doesn't support MODE_SR change during operation. TI recommends do not change PWM_MODE during device operation.

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8.3.2.1 3x PWM Mode (PWM_MODE = 10b or 11b or MODE_SR Pin is Connected to GVDD with R_{MODE} or to GVDD)

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 8-2

Table 8-2. 3x PWM Mode Truth Table

INLx	INHx	PHASEx
0	X	Hi-Z
1	0	L
1	1	H

Figure 8-3 shows the application diagram of DRV8374-Q1 configured in 3x PWM mode.

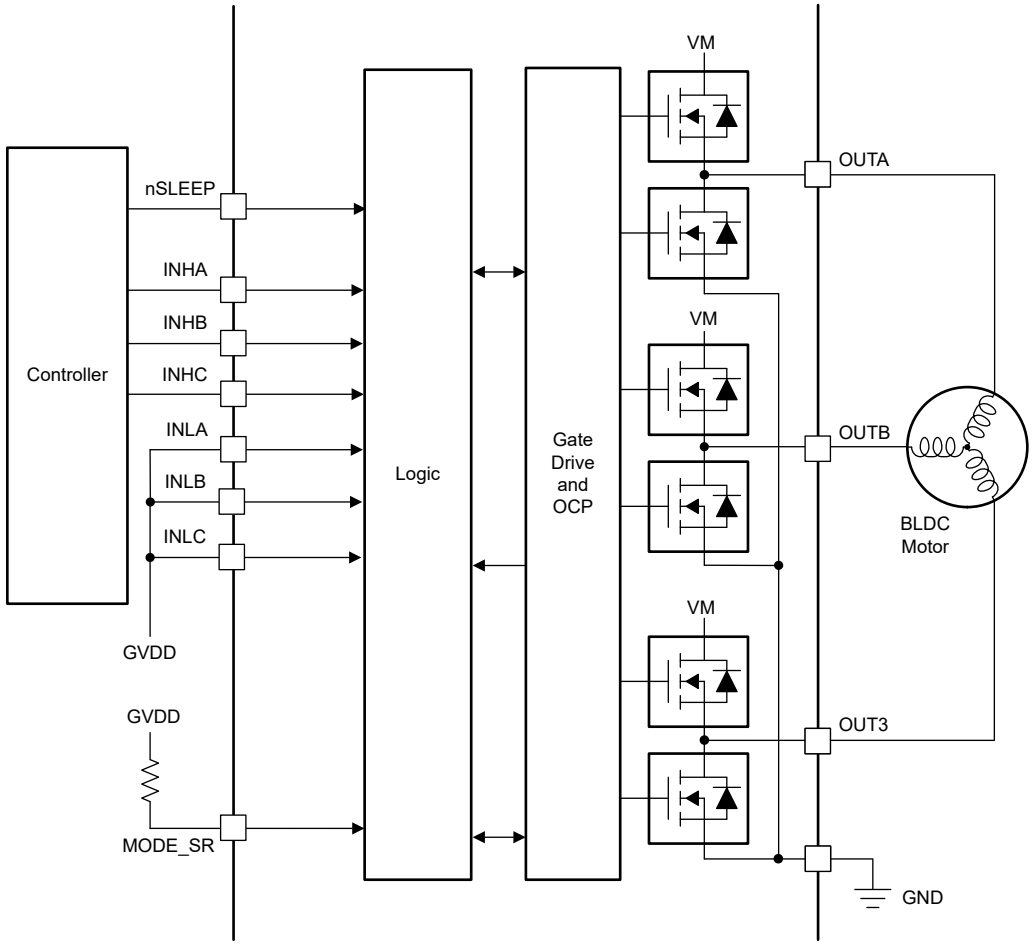


Figure 8-3. 3x PWM Mode

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8.3.3 Device Interface Modes

The DRV8374-Q1 family of devices (29-pin variant) supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design.

8.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the DRV8374-Q1. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin can be configured to either open-drain or push-pull through SDO_MODE.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8374-Q1.

For more information on the SPI, see the *Section 8.5* section.

8.3.3.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are

The hardware interface lets the application designer to configure the most common device settings by tying the pin logic high or logic low, or with a simple pull-up or pull-down resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

For more information on the hardware interface, see the *Section 8.3.9* section.

Note

VCC represents the external pull up voltage. By default SDO pin is open drain

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8.3.4 GVDD Linear Voltage Regulator

A 5V linear regulator is integrated into the family of devices and is available for use by external circuitry. The GVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30 mA). The output of the GVDD regulator should be bypassed near the GVDD pin with a X5R or X7R, 1-µF, 10-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

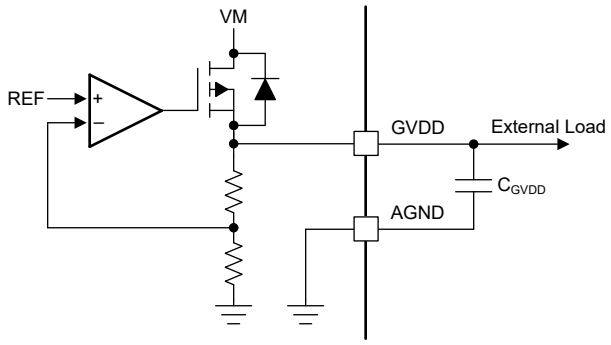


Figure 8-4. GVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the GVDD linear regulator with VM as supply.

$$P = (V_{VM} - V_{GVDD}) \times I_{GVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of GVDD results in an additional power dissipation as shown in Equation 2.

$$P = (24\,V - 5\,V) \times 20\,mA = 380\,mW \quad (2)$$

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8.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram, pin descriptions and see section (Section 8.3) for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low or during an over temperature shutdown.

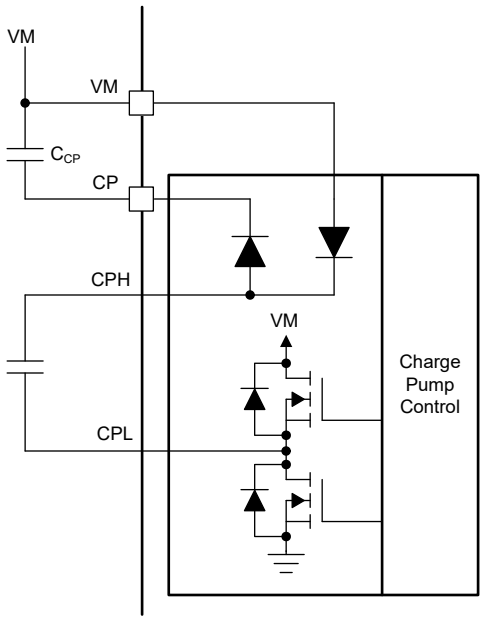


Figure 8-5. Charge Pump

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8.3.6 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in Figure 8-6.

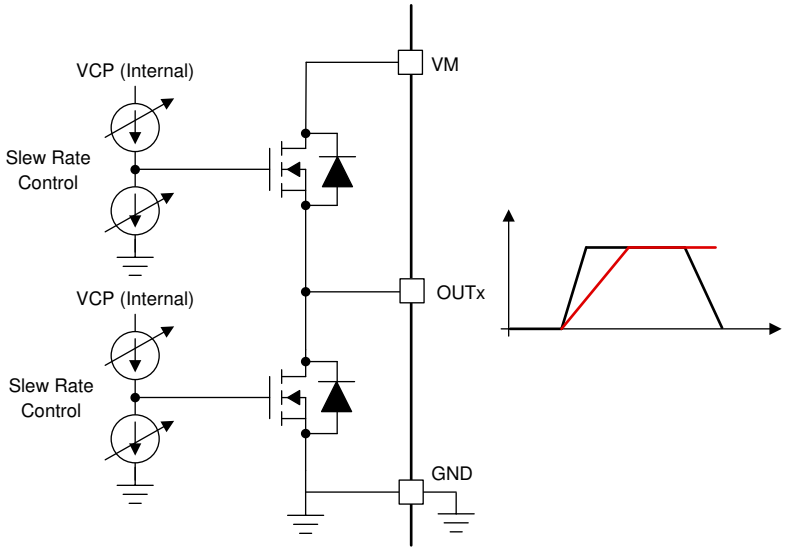


Figure 8-6. Slew Rate Circuit Implementation

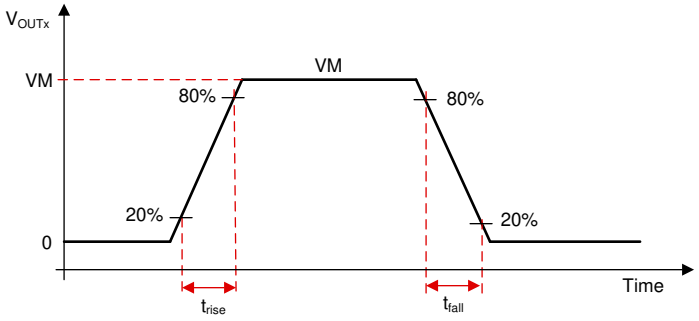


Figure 8-7. Slew Rate Timings

Note

The SLEW pin is sensed only during power up and the device doesn't support slew rate change during operation. TI recommends do not change SLEW_RATE register bits during operation.

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8.3.7 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are maintained to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and maintaining that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in Figure 8-8 and Figure 8-9.

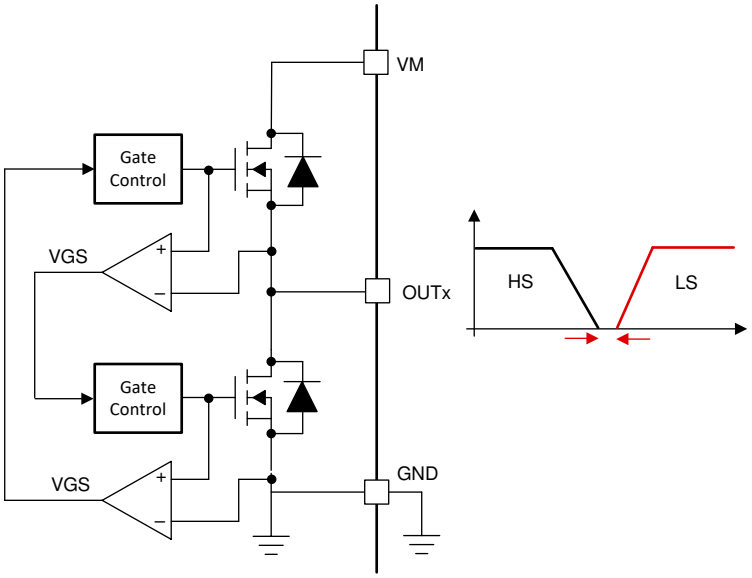


Figure 8-8. Cross Conduction Protection

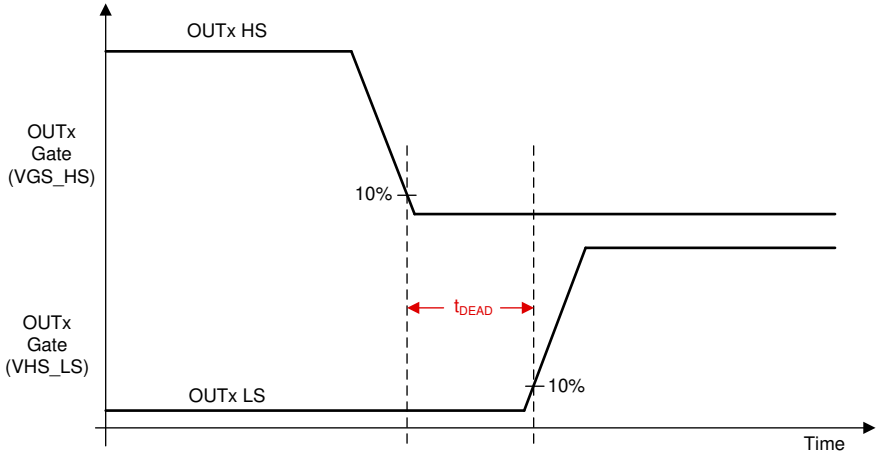


Figure 8-9. Dead Time

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8.3.8 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage.

Note

During current limit mode or active demag mode a small digital delay is added as the input command propagates through the device, and user can see up to 600ns more delay during these modes.

8.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

8.3.9.1 Logic Level Input Pin (Internal Pulldown)

Figure 8-10 shows the input structure for the logic level pins, . The input can be with a voltage or external resistor. TI recommends to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

STATE	CONNECTION
V_{IH}	Tied to GVDD
V_{IL}	Tied to GND

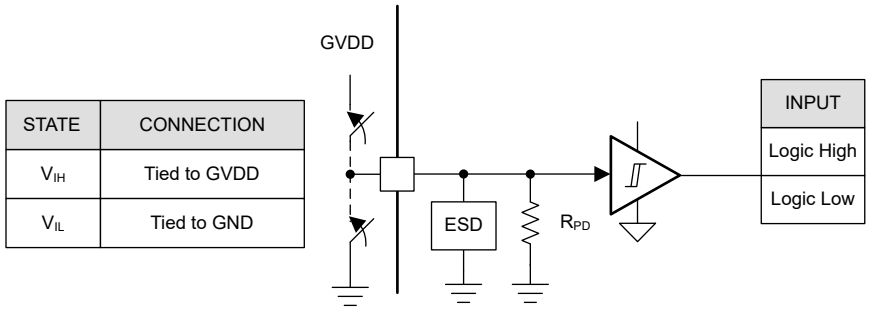


Figure 8-10. Logic-Level Input Pin Structure

8.3.9.2 Logic Level Input Pin (Internal Pullup)

Figure 8-11 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

STATE	CONNECTION
V_{IH}	Tied to GVDD
V_{IL}	Tied to GND

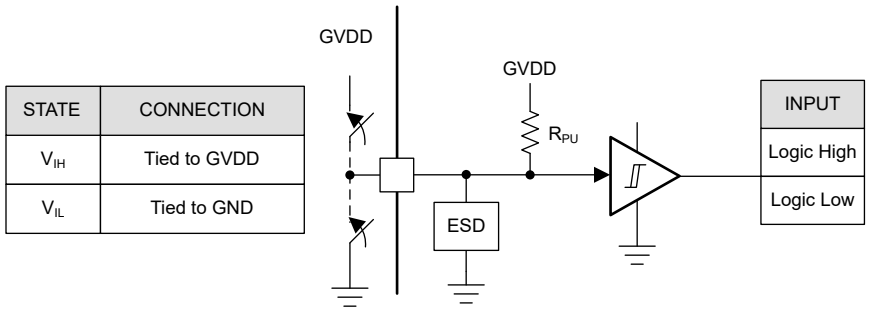


Figure 8-11. Logic nSCS

8.3.9.3 Open Drain Pin

Figure 8-12 shows the structure of the open-drain output and SDO in open drain mode. The open-drain output requires an external pullup resistor to function properly.

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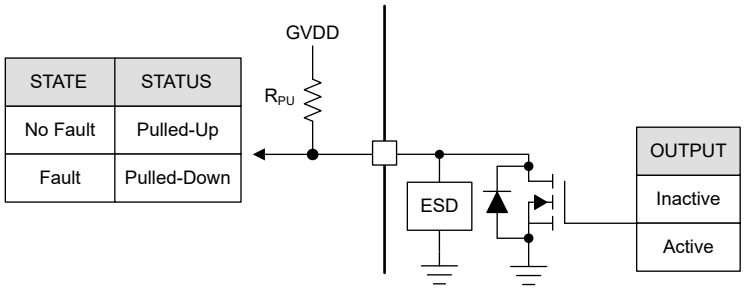


Figure 8-12. Open Drain

8.3.9.4 Push Pull Pin

Figure 8-13 shows the structure of SDO in push-pull mode.

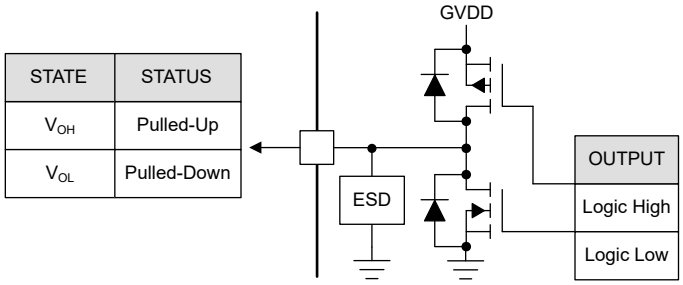


Figure 8-13. Push Pull Pin

8.3.9.5 Four Level Input Pin

Figure 8-14 shows the structure of the four level input pins, on hardware interface devices. The input can be set with an external resistor.

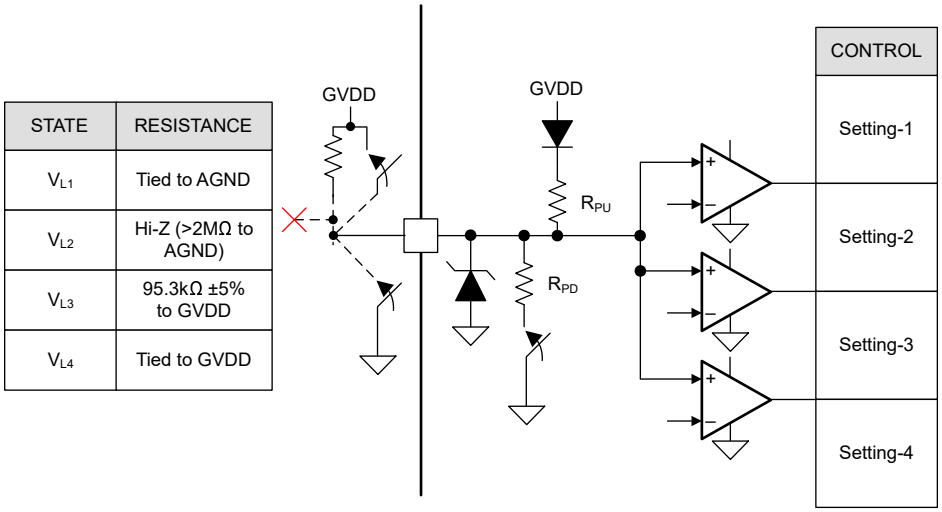


Figure 8-14. Four Level Input Pin Structure

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8.3.10 Current Sense Amplifiers

The DRV8374-Q1 integrates three, high-performance low-side current sense amplifiers for current measurements using built-in current sensing. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless-DC commutation with an external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs (low-side FETs). The current sense amplifier output is a voltage proportional to the LS FET current in 29-pin variant. The current sense amplifier output is a current proportional to the LS FET current in 23-pin variant. The current sense amplifiers in 29-pin variant include features such as programmable gain. An external reference is required to be provided on the voltage reference pin (VREF).

8.3.10.1 Current Sense Amplifier Operation (23-pin variant)

The SOx pin on the DRV8374-Q1 outputs a current proportional to current flowing in the low side FETs multiplied by the gain setting (G_{CSA}). The gain setting is fixed at 0.04mA/A. Figure 8-15 shows the internal architecture of the current sense amplifier for the current outputs. The current sense is implemented with the sense FET on each low-side FET of the DRV8374-Q1 device. This current information is multiplied by the gain setting and available as a current output on the SOx pin. To convert this current into a voltage (for example, input to an A/D converter), a resistor connected to an external reference voltage (EXT_VREF) can act as I/V converter. EXT_VREF can be derived from the A/D converter reference. The value of the resistors R_{PULL_UP} and R_{PULL_DOWN} affects gain error and settling time of the SOx outputs. More details on resistor selection can be found on the Electrical Specification Table.

Output voltage at SOx pin is given as

$$V_{SOX} = \left(V_{EXT_VREF}/2\right) \pm I_{OUT} \times R_T \times GAIN \quad (3)$$

where $R_T = R_{PULL_UP} \,||\, R_{PULL_DOWN}$

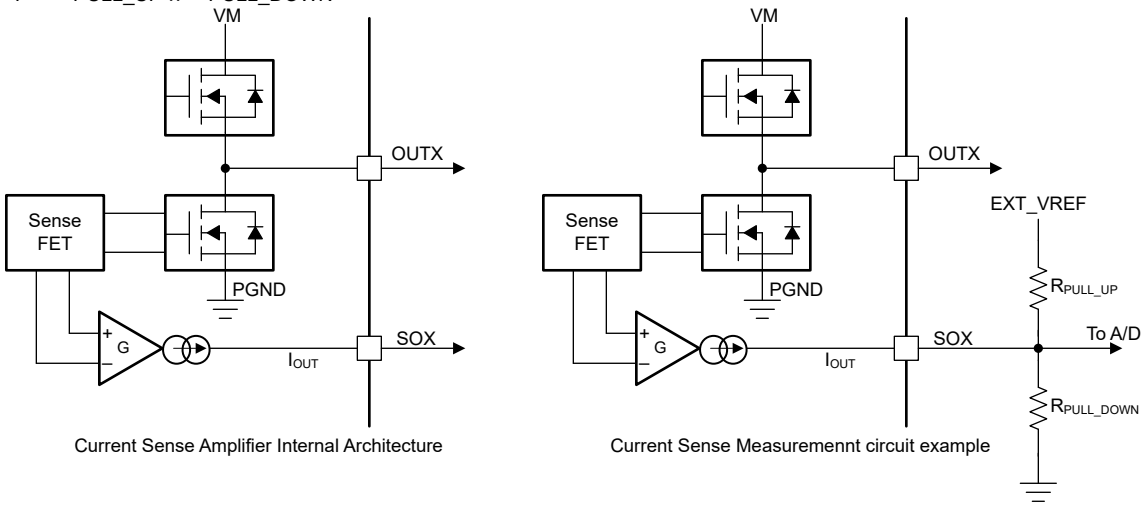


Figure 8-15. Integrated Current Sense Amplifier (23pin Variant)

8.3.10.2 Current Sense Amplifier Operation (29-pin variant)

The SOx pin on the DRV8374-Q1 outputs an analog voltage proportional to current flowing in the low side FETs multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels which can be set by the GAIN pin (in hardware device variant) or the GAIN bits (in SPI device variant).

Figure 8-16 shows the internal architecture of the current sense amplifiers. The current sense is implemented with the sense FET on each low-side FET of the DRV8374-Q1 device. This current information is fed to the internal I/V converter, which generates the CSA output voltage on the SOX pin based on the voltage on VREF pin and the Gain setting. The CSA output voltage can be calculated as :

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$$SOX = \left({V_{REF}}/{2}\right) \pm GAIN \times I_{OUTX} \quad (4)$$

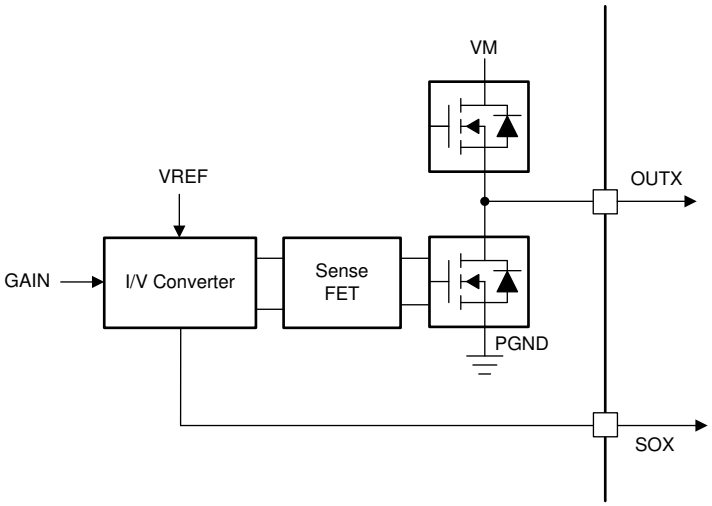


Figure 8-16. Integrated Current Sense Amplifier

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Figure 8-17 and Figure 8-18 show the detail of the amplifier operational range. In bi-directional operation, the amplifier output for 0V input is set at VREF/2. Any change in the differential input results in a corresponding change in the output times the CSA_GAIN factor. The amplifier has a defined linear region in which it can maintain operation.

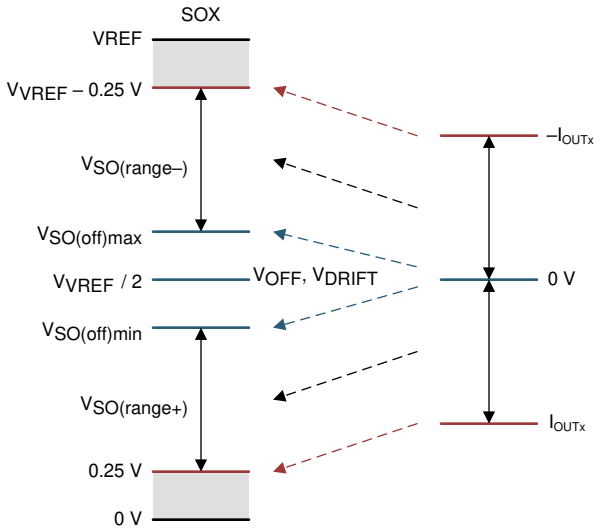


Figure 8-17. Bidirectional Current Sense Output

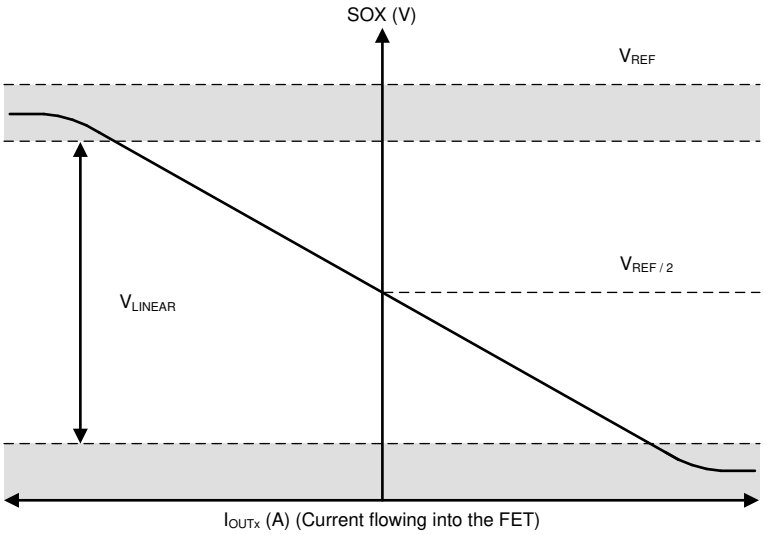


Figure 8-18. Bidirectional Current Sense Regions

Note

The current sense amplifier supports only capacitive load at output. TI recommends connecting low pass filter with resistor and capacitor on output of current sense amplifier.

Note

The current sense amplifier supports dynamic gain change. The GAIN is sampled in every 1ms through pin sensing in HW variant and any GAIN change through SPI write (in SPI variant). After receiving the GAIN change command, the new GAIN is applied to all the three current sense amplifiers on the next falling edge of any INLx signal.

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8.3.11 Active Demagnetization

family of devices has smart rectification features (active demagnetization) which decreases power losses in the device by reducing diode conduction losses. When this feature is enabled, the device automatically turns ON the corresponding MOSFET whenever the device detects diode conduction. This feature can be configured with the pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in sections below.

The device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS comparator compares with the ground (0V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization feature.

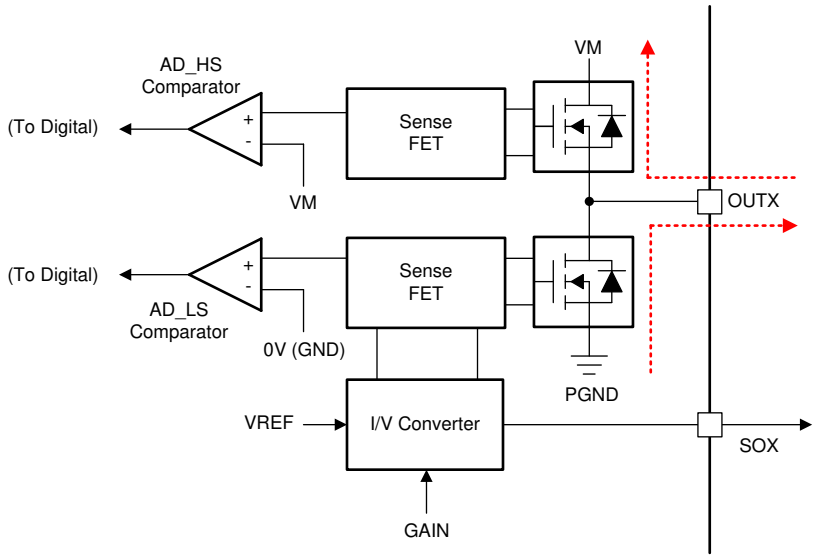


Figure 8-19. Active Demagnetization Operation

Note

Active demagnetization disabled on an OCP event .

Note

A FET that is conducting due to active demagnetization, and if the current through that FET is not decaying to zero when an input command to turn on that FET is given, then the turn on command is not acknowledged, and that FET turns off only when the current reaches to zero independent of the input control signal of that FET.

8.3.11.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

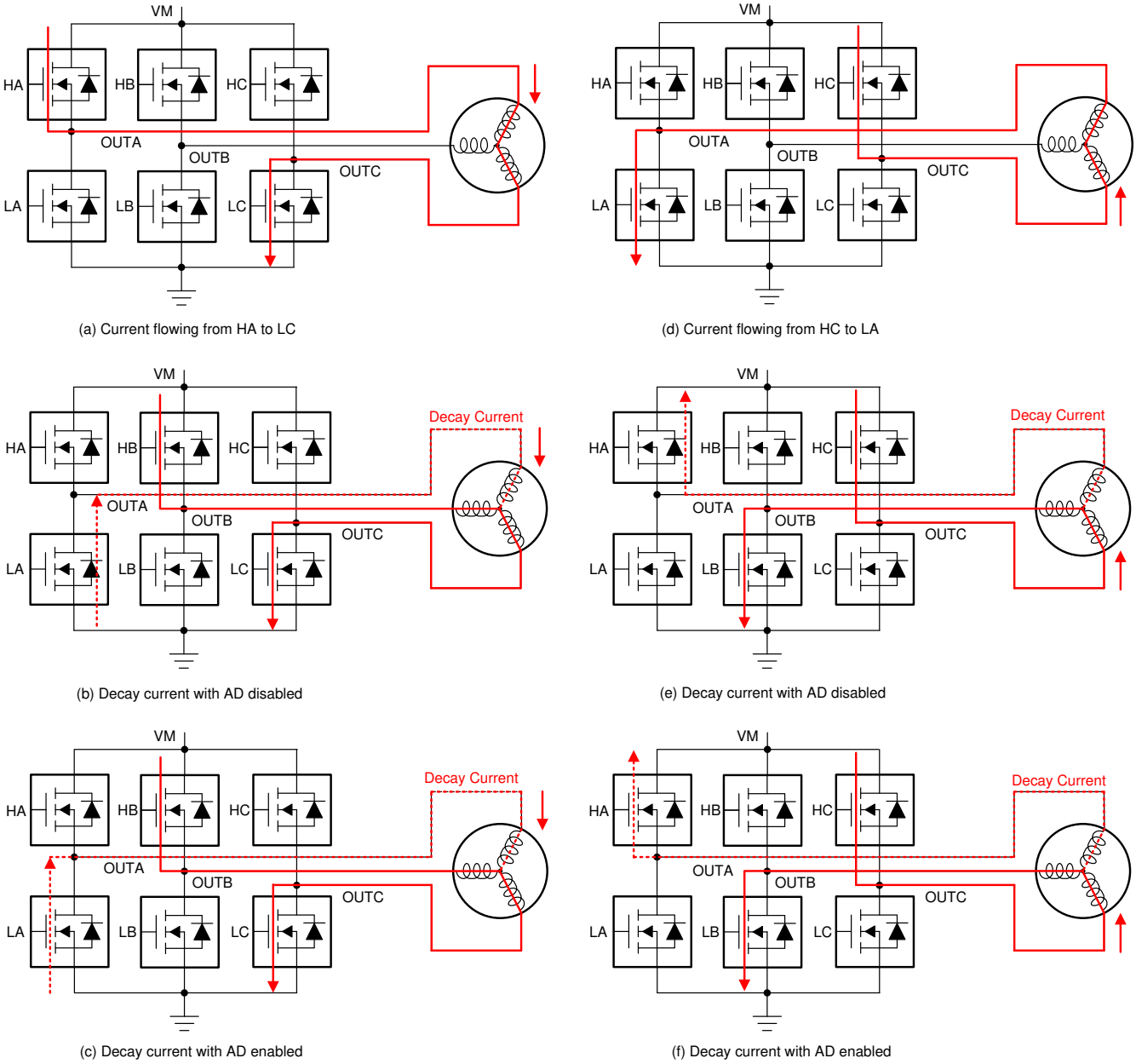
8.3.11.1.1 Automatic Synchronous Rectification in Commutation

Figure 8-20 shows the operation of active demagnetization during the BLDC motor commutation. As shown in Figure 8-20 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in Figure 8-20 (b), the HB switch is turned on, whereas the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in Figure 8-20 (c).

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Similarly the operation of high-side FET is realized in Figure 8-20 (d), (e) and (f).



(a) Current flowing from HA to LC

(d) Current flowing from HC to LA

(b) Decay current with AD disabled

(e) Decay current with AD disabled

(c) Decay current with AD enabled

(f) Decay current with AD enabled

Figure 8-20. ASR in BLDC Motor Commutation

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Figure 8-21 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

Figure 8-21 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demag. comparator threshold and delays.

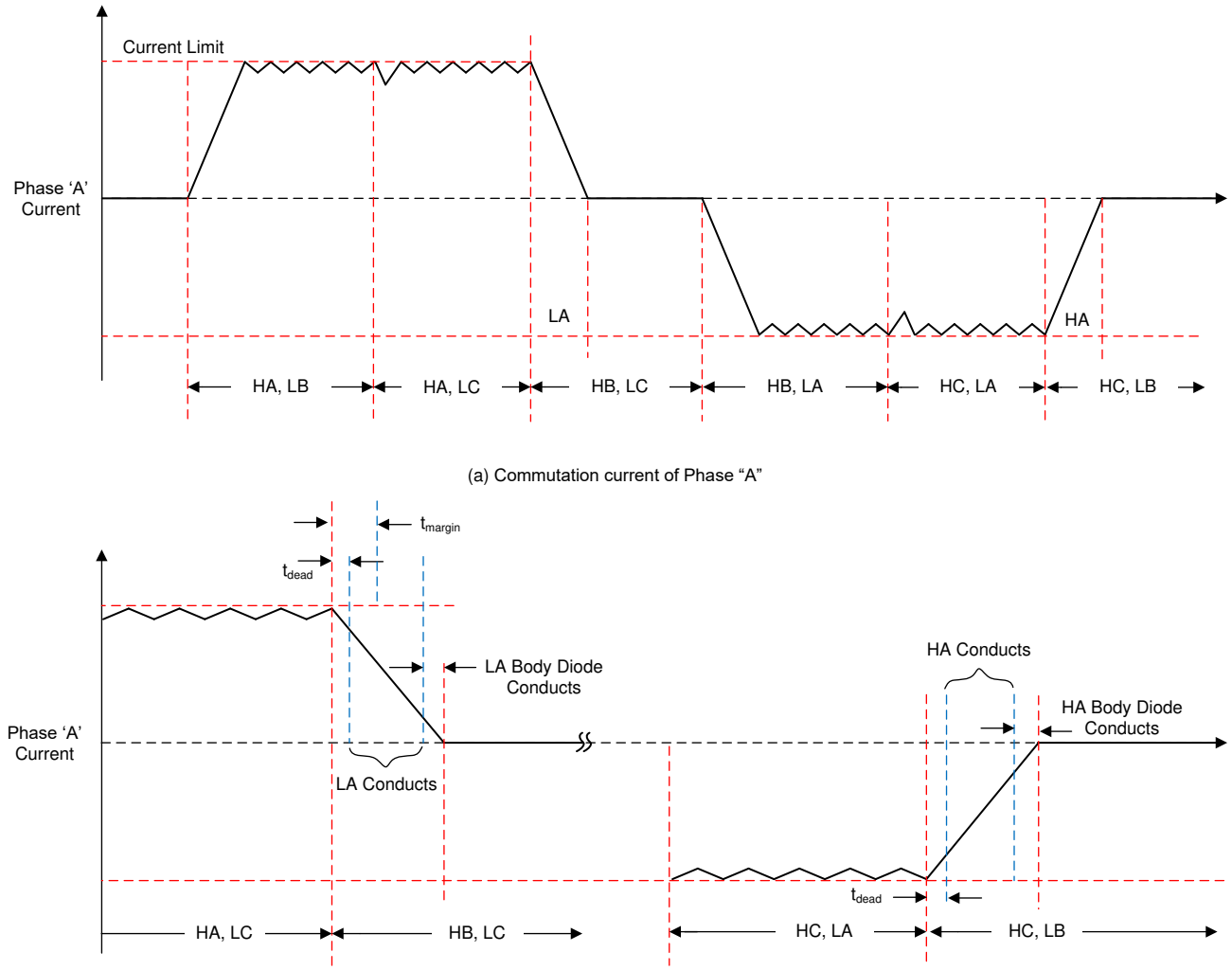


Figure 8-21. Current Waveforms for ASR in BLDC Motor Commutation

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8.3.11.1.2 Automatic Synchronous Rectification in PWM Mode

Figure 8-22 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

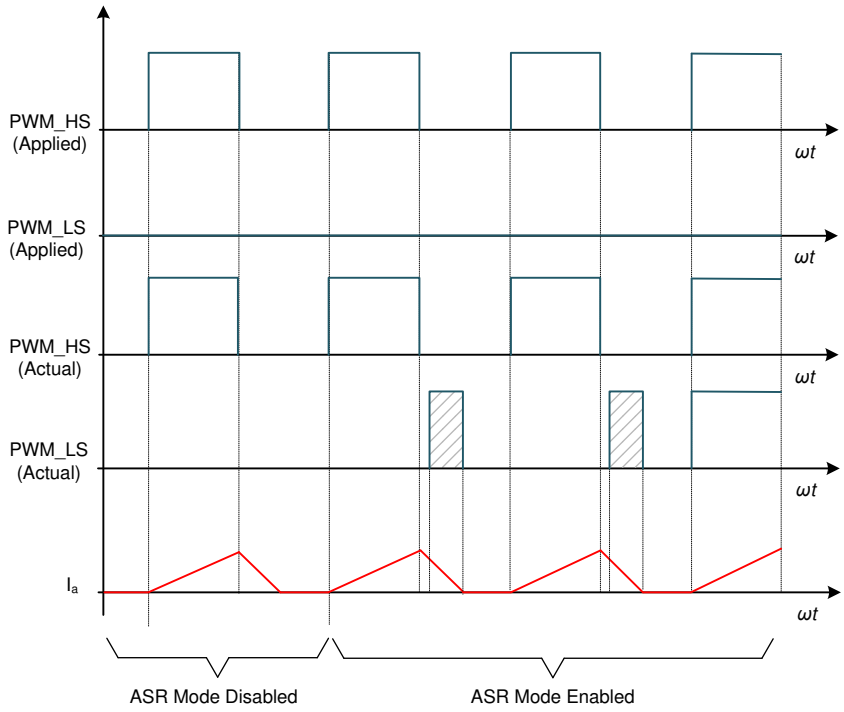


Figure 8-22. ASR in PWM Mode

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8.3.11.2 Automatic Asynchronous Rectification Mode (AAR Mode)

Figure 8-23 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

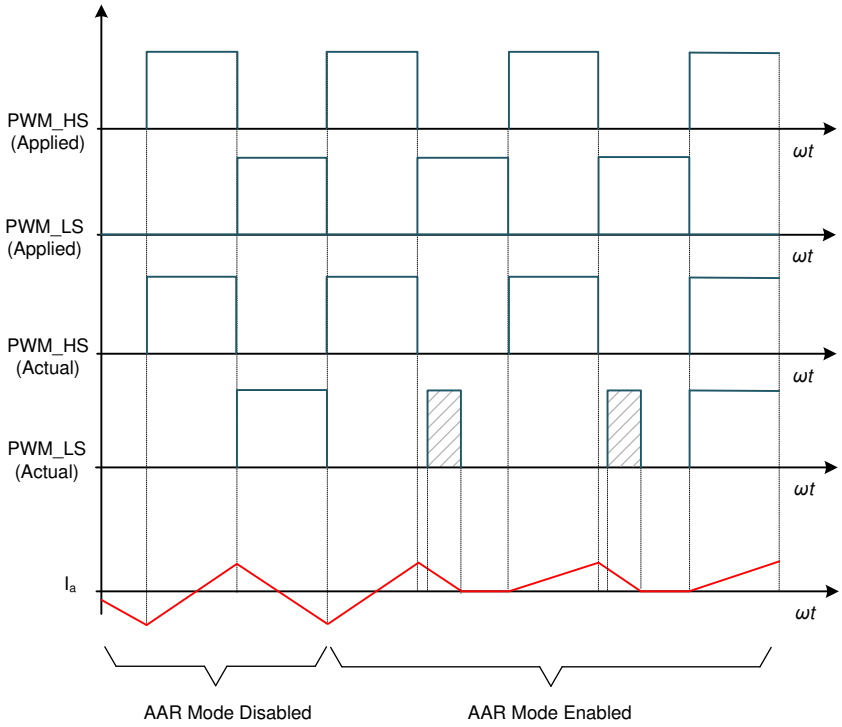


Figure 8-23. AAR in PWM Mode

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8.3.12 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFET exceeds the I_{LIMIT} current. This feature restricts motor current to less than the I_{LIMIT}.

The current-limit circuitry utilizes the current sense amplifier output of the three phases compared with the voltage at ILIMIT pin. shows the implementation of current limit circuitry. As shown in , the output of current sense amplifiers is combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage V_{ILIM} pin to realize the current limit implementation. The relation between current sensed on OUTX pin and V_{MEAS} threshold is given as:

where

- I_{OUTX} is current flowing into the low-side MOSFET
- CSA_GAIN is the current sense amplifier gain

Note

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

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8.3.12.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, DRV8374-Q1 has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant DRV8374-Q1, this internal PWM clock can be configured to either 10kHz or 20kHz or 40kHz through PWM_100_DUTY_SEL. In H/W variant DRV8374-Q1 PWM internal clock is set to 20kHz. The image below shows operation with 100% duty cycle.

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8.3.13 Protections

The DRV8374-Q1 family of devices is protected against VM under voltage, charge pump under voltage, and overcurrent events. Fault Action and Responsesummarizes various faults details.

Table 8-3. Fault Action and Response

nFAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM under-voltage (RESET)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
GVDD under-voltage (RESET)	$V_{VM} > V_{UVLO}$,$V_{GVDD} < V_{GVDD_UVLO}$	External GVDD	—	Hi-Z	Disabled	Automatic: $V_{GVDD} > V_{GVDD_UVLO}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
GVDD under-voltage (RESET)	$V_{GVDD} < V_{GVDD_UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{GVDD} > V_{GVDD_UVLO}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
Charge pump under-voltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
Over-voltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_MODE = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_MODE = 1b	nFAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY} CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 10b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
ILIMIT	$V_{ILIMIT} < V_{SO}$	ILIMFLT_MODE = 0b	None	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
		ILIMFLT_MODE = 1b	nFAULT	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
SPI Error (SPI_FLT)	SCLK, Parity and ADDR fault	SPIFLT_MODE = 0b	None	Active	Active	No action
		SPIFLT_MODE = 1b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, CLR_FLT
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_MODE = 0b	None	Active	Active	No action
		OTW_MODE = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW_HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD)	$T_J > T_{TSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD_HYS}$

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8.3.13.1 VM Supply Undervoltage Lockout (RESET)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in Figure 8-24. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The RESET bit is latched high in the device status register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

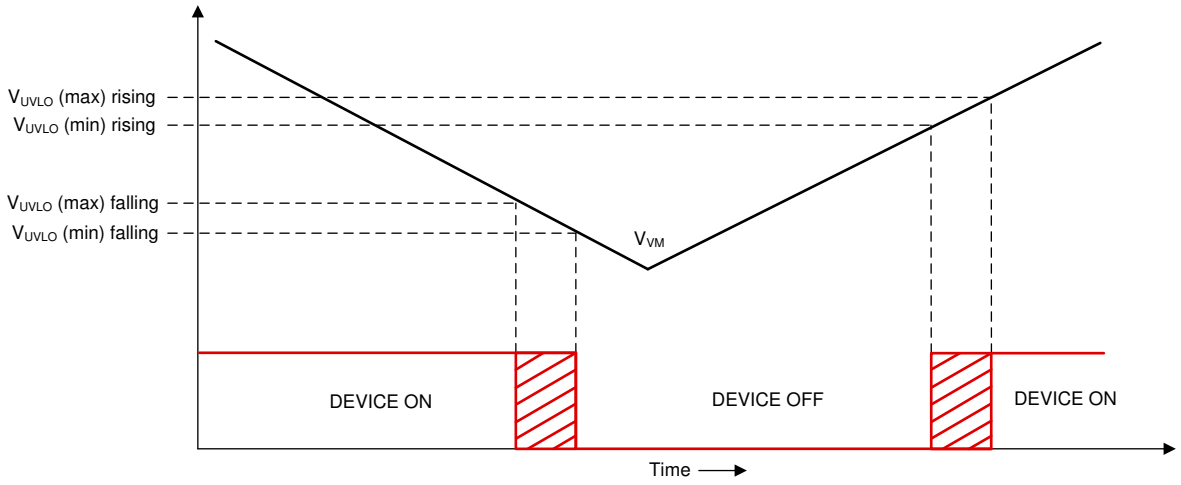


Figure 8-24. VM Supply Undervoltage Lockout

8.3.13.2 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on GVDD pin falls lower than the V_{GVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the GVDD undervoltage condition is removed. The RESET bit is latched high in the device status register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.13.3 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The charge pump undervoltage is reported on nFAULT and CPUV bits. nFAULT bit will be auto-cleared when charge pump undervoltage condition is removed. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device variants.

8.3.13.4 Over Voltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The over-voltage is reported on nFAULT and OVP bits. nFAULT bit will be auto cleared when over voltage condition is removed. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). Setting the OVP_MODE bit high on the SPI devices enables this protection feature. On hardware interface devices, the OVP protection is disabled.

The OVP threshold is also programmable on the SPI device variant. The OVP threshold can be set to 35V or 23V based on the OVP_SEL bit.

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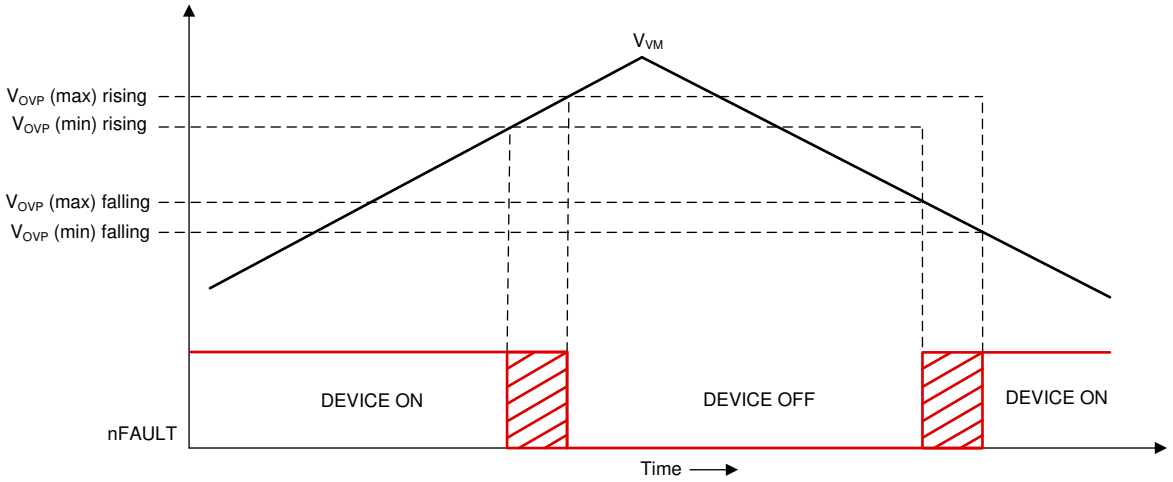


Figure 8-25. Over Voltage Protection

8.3.13.5 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current through a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is fixed at 50A threshold, the t_{OCP_DEG} is fixed at 1.4µs, and the OCP_MODE bit is configured for latched shutdown. On SPI devices, the I_{OCP} threshold is set through the OCP_LVL bits, the t_{OCP_DEG} is set through the OCP_DEG bits.

The OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

8.3.13.5.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The nFAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

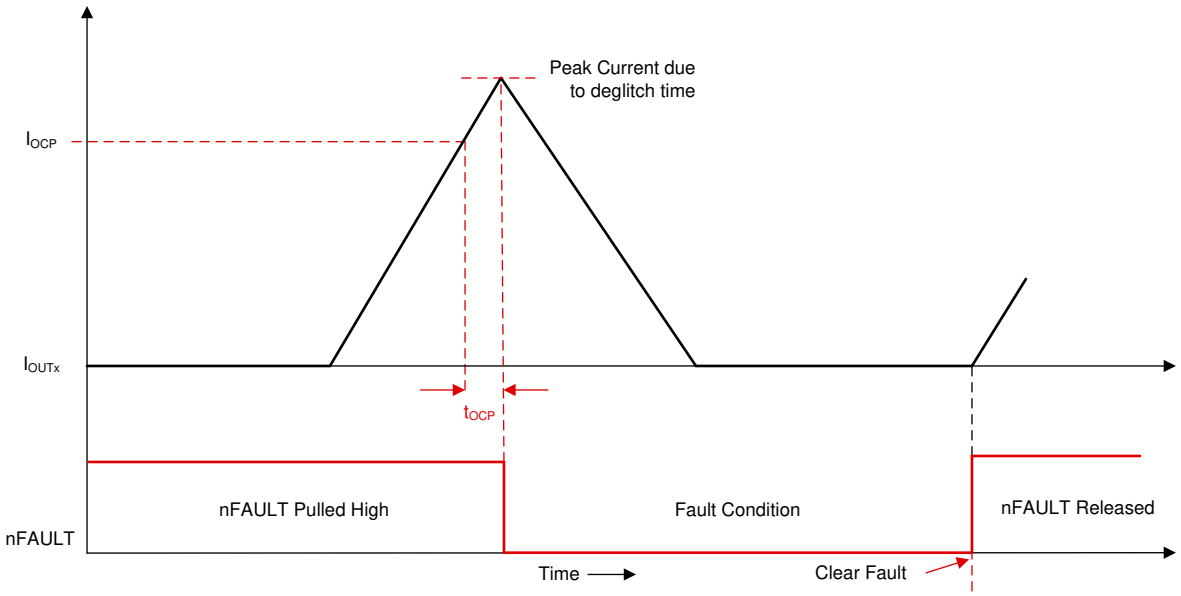


Figure 8-26. Overcurrent Protection - Latched Shutdown Mode

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8.3.13.5.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The nFAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the nFAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

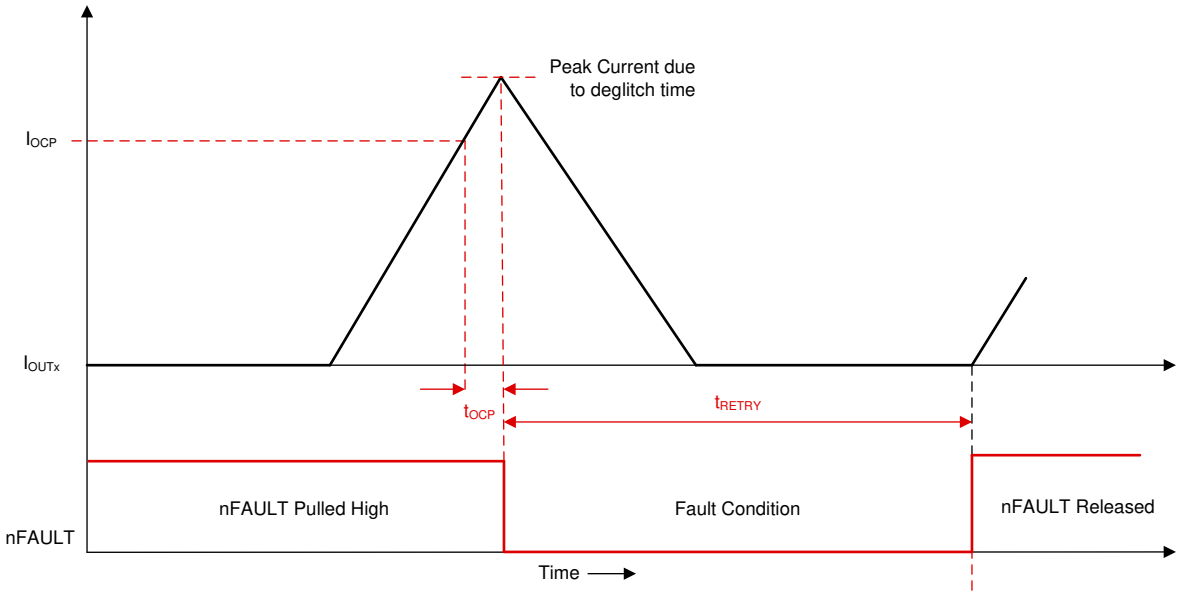


Figure 8-27. Overcurrent Protection - Automatic Retry Mode

8.3.13.5.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the nFAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The DRV8374-Q1 continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.13.5.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

8.3.13.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the OT status (OT_STS) register and OTF bit in the device status register is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_MODE) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}). In hardware variant the over temperature warning is reported on nFAULT pin by default.

8.3.13.7 Thermal Shutdown (OTS)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the nFAULT and OTSD bit in the OT status (OT_STS) register and OTF bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTSD bit

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stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

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8.4 Device Functional Modes

8.4.1 Functional Modes

8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8374-Q1 family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, the charge pump is disabled, the GVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

Note

TI recommends to connect pull up on nFAULT even if pull up is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, maintain that nFAULT is pulled to >2.2V on power up or the device enters internal test mode.

8.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, GVDD regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the DRV8374-Q1 family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence falls within the t_{RST} time window or else the device starts the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

8.4.2 DRVOFF functionality

actively disables the predriver and MOSFETs through the DRVOFF pin, bypassing digital control. Pulling the DRVOFF pin high disables all six MOSFETs. When nSLEEP is high and the DRVOFF pin is high, the charge pump, GVDD regulator, and SPI bus remain active, while driver-related faults, such as OCP, stay inactive. The DRVOFF pin actively disables MOSFETs, halting motor commutation regardless of the INHx and INLx input pins' status.

Note

DRVOFF is applicable only for 29-Pin SPI and Hardware variants.

Note

Since DRVOFF pin independently disables MOSFET, device can trigger fault condition resulting in nFAULT getting pulled low.

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8.5 SPI Communication

8.5.1 Programming

On DRV8374-Q1 SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. DRV8374-Q1 uses SPI mode 0 (Data is sampled on the rising edge and shifted out on the falling edge). Refer to timing diagram Figure 7-1. The SPI operates in secondary mode and connects to a controller. The SPI input data (SDI) word consists of a 24-bit word, with one read or write bit, a parity bit, 6-bit address and 15 bits of data with a parity bit. The SPI output consists of 24 bit word, with a 8 bits of status information (STS register) and 16-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin must be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 24 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and in sleep mode

8.5.1.1 SPI Format

SPI Format - with Parity

The SDI input data word is 24 bits long and consists of the following format:

- 1 read or write bit, W (bit B16)
- 6 address bits, A (bits B22 through B17)
- Parity bit, P (bit B23)
- 15 data bits with 1 parity bit, D (bits B15 through B0)

The SDO output data word is 24 bits long. The most significant bits are status bits and the least significant 16 bits are the data content of the register being accessed.

Table 8-4. SDI Input Data Word Format for SPI

PARITY	ADDRESS							RW	PARITY	DATA													
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
P	A5	A4	A3	A2	A1	A0	W0	P	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 8-5. SDO Output Data Word Format

STATUS								DATA															
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The details of the bits used in SPI frame format are detailed below.

Read/Write Bit (R/W): R/W (W0) bit set to 0b indicates a SPI write transaction. For a SPI read operation, R/W bit needs to be set to 1b.

Address Bits (A): A SPI secondary device takes a 6-bit register address.

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Parity Bit (P): Both header and data fields of a SPI input data frame include a parity bit for single bit error detection - in Table 8-4, B23 is parity bit for the header field, while B15 is the parity bit for the data field. The parity scheme used is even parity - the number of ones in a block of 16-bits (including the parity bit) is even. Data will be written to the internal registers only if the parity check is successful. Parity checks can be enabled or disabled by configuring the SPI_PEN bit of SYS_CTRL register. Parity checks are disabled by default.

Note

Though parity checks are disabled by default, TI recommends enabling parity checks to safeguard against single-bit errors.

9 Register Map

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9.1 CONTROL Registers

Table 9-1 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. CONTROL Registers

Offset	Acronym	Register Name	Section
10h	Fault Mode Register	Fault Mode Register	Section 9.1.1
11h	WATCH_DOG		Section 9.1.2
13h	Drviver Fault Control Register	Drviver Fault Control Register	Section 9.1.3
17h	Fault Clear Register	Fault Clear Register	Section 9.1.4
22h	Predriver control Register	Predriver control Register	Section 9.1.5
23h	CSA Control Register	CSA Control Register	Section 9.1.6
3Fh	System Control Register	System Control Register	Section 9.1.7

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

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9.1.1 Fault Mode Register (Offset = 10h) [Reset = 6011h]

Fault Mode Register is shown in Table 9-3.

Return to the Summary Table.

Table 9-3. Fault Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	VREFEXT_FLT_MODE	R/W	1h	VREF EXTERNAL Fault mode 0h = VREF external uvlo reporting on nFAULT pin is disabled 1h = VREF external uvlo reporting on nFAULT pin is enabled
13	ILIMFLT_MODE	R/W	1h	ILIMIT Fault mode 0h = ILIMIT reporting on nFAULT pin is disabled 1h = ILIMIT reporting on nFAULT pin is enabled
12-11	RESERVED	R/W	0h	Reserved
10	RESERVED	R-0	0h	Reserved
9	OVP_MODE	R/W	0h	Over Voltage Protection Fault mode 0h = Over Voltage protection is disabled 1h = Over Voltage protection is enabled
8	RESERVED	R-0	0h	Reserved
7	SPIFLT_MODE	R/W	0h	SPI Fault mode 0h = SPI fault reporting on nFAULT pin is disabled 1h = SPI fault reporting on nFAULT pin is enabled
6	RESERVED	R-0	0h	Reserved
5-4	OCP_MODE	R/W	1h	Overcurrent Protection Fault mode 0h = Over Current causes a latched fault 1h = Over Current causes an automatic retrying fault 2h = Over Current is report only but no action is taken 3h = Over Current is not reported and no action is taken
3-1	RESERVED	R-0	0h	Reserved
0	OTW_MODE	R/W	1h	Overtemperature Warning Fault mode 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

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9.1.2 WATCH_DOG Register (Offset = 11h) [Reset = 0000h]

WATCH_DOG is shown in Table 9-4.

Return to the Summary Table.

Table 9-4. WATCH_DOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-8	RESERVED	R-0	0h	Reserved
7-0	WATCH_DOG_COUNT	R	0h	Watch dog counter value

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9.1.3 Drviver Fault Control Register (Offset = 13h) [Reset = 0010h]

Drviver Fault Control Register is shown in Table 9-5.

Return to the Summary Table.

Table 9-5. Drviver Fault Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	RESERVED	R-0	0h	Reserved
13-12	RESERVED	R/W	0h	Reserved
11	RESERVED	R-0	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	OVP_SEL	R/W	0h	Overvoltage level setting 0h = VM overvoltage level is 35V 1h = VM overvoltage level is 23V
7-6	RESERVED	R-0	0h	Reserved
5-4	OCP_DEG	R/W	1h	OCP Deglitch time 0h = OCP Deglitch time is 0.6 µs 1h = OCP Deglitch time is 1.2 µs 2h = OCP Deglitch time is 1.6 µs 3h = OCP Deglitch time is 2 µs
3	RESERVED	R-0	0h	Reserved
2	OCP_TRETRY	R/W	0h	OCP Retry Time 0h = 5ms 1h = 500ms
1	RESERVED	R-0	0h	Reserved
0	OCP_LVL	R/W	0h	OCP Level 0h = 50A 1h = 25A

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9.1.4 Fault Clear Register (Offset = 17h) [Reset = 0000h]

Fault Clear Register is shown in Table 9-6.

Return to the Summary Table.

Table 9-6. Fault Clear Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-1	RESERVED	R-0	0h	Reserved
0	FLT_CLR	R-0/W1C	0h	Clear latched faults 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

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9.1.5 Predriver control Register (Offset = 22h) [Reset = 0080h]

Predriver control Register is shown in Table 9-7.

Return to the Summary Table.

Table 9-7. Predriver control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	DIS_ILIMIT	R/W	0h	ILIMIT disable 0h = ILIMIT is enabled 1h = ILIMIT is disabled
13-11	ILIMIT_SEL_CODE	R/W	0h	ILIMIT Selection code for 29 pin, SPI device 0.075(N+1)Vref/gain N is ILIMIT_SEL_CODE in decimal ILIMIT_SEL_CODE = 3'b111, there is No ILIMIT threshold.
10	RESERVED	R-0	0h	
9-8	ILIM_BLANK_SEL	R/W	0h	Current Limit Blanking Time Selection 0h = 5.6us for slew rate of 50 and 1.8us for all other slew rates. 1h = 6.0us for slew rate of 50 and 2.2us for all other slew rates. 2h = 6.6us for slew rate of 50 and 2.8us for all other slew rates. 3h = 7.6us for slew rate of 50 and 3.8us for all other slew rates.
7-4	ADMAG_TMARGIN	R/W	8h	Wait time before determining HiZ N * Clock Cycle period => N*200ns
3	AD_COMP_TH_HS	R/W	0h	Active demag high side comparator threshold 0h = active demag comparator threshold is 500mA 1h = active demag comparator threshold is 600mA
2	AD_COMP_TH_LS	R/W	0h	Active demag low side comparator threshold 0h = active demag comparator threshold is 500mA 1h = active demag comparator threshold is 600mA
1-0	SLEW_RATE	R/W	0h	Slew rate settings 0h = Slew rate is 1100 V/µs 1h = Slew rate is 500 V/µs 2h = Slew rate is 250 V/µs 3h = Slew rate is 50 V/µs

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9.1.6 CSA Control Register (Offset = 23h) [Reset = 0000h]

CSA Control Register is shown in Table 9-8.

Return to the Summary Table.

Table 9-8. CSA Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1-0	CSA_GAIN	R/W	0h	CSA Gain settings 0h = CSA gain is 0.04 V/A 1h = CSA gain is 0.08 V/A 2h = CSA gain is 0.16 V/A 3h = CSA gain is 0.32 V/A

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9.1.7 System Control Register (Offset = 3Fh) [Reset = 0408h]

System Control Register is shown in Table 9-9.

Return to the Summary Table.

Table 9-9. System Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-12	WRITE_KEY	R-0/W	0h	0x5 Write Key Specific to this register.
11	RESERVED	R-0	0h	Reserved
10	SDO_ODEN	R/W	1h	SDO in Open Drain Mode 0h = SDO in Push Pull Mode 1h = SDO in Open Drain Mode
9-8	RESERVED	R-0	0h	Reserved
7	REG_LOCK	R/W	0h	Register Lock Bit 0h = Registers Unlocked 1h = Registers Locked
6	SPI_PEN	R/W	0h	Parity Enable for SPI 0h = Parity Disabled 1h = Parity Enabled
5-4	RESERVED	R/W	0h	Reserved
3	SDO_MD	R/W	1h	SDO Launch Edge Select signal 0h = Launch SDO on Negedge of SCLK 1h = Launch SDO on Posedge of SCLK
2-0	RESERVED	R-0	0h	Reserved

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9.2 STATUS Registers

Table 9-10 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 9-10 should be considered as reserved locations and the register contents should not be modified.

Table 9-10. STATUS Registers

Offset	Acronym	Register Name	Section
0h	Device Status Register	Device Status Register	Section 9.2.1
4h	Over Temperature Status Register	Over Temperature Status Register	Section 9.2.2
5h	Supply Status Register	Supply Status Register	Section 9.2.3
6h	Driver Status Register	Driver Status Register	Section 9.2.4
7h	System Interface Status Register	System Interface Status Register	Section 9.2.5

Complex bit access types are encoded to fit into small table cells. Table 9-11 shows the codes that are used for access types in this section.

Table 9-11. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

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9.2.1 Device Status Register (Offset = 0h) [Reset = 0280h]

Device Status Register is shown in Table 9-12.

Return to the Summary Table.

Table 9-12. Device Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-11	RESERVED	R-0	0h	Reserved
10	RESERVED	R	0h	Reserved
9	DNRDY_STS	R	1h	Device Not Ready Status. Will be cleared automatically after completion of Power Up. 0h = Device is Ready 1h = Device is NOT Ready
8	SYSFLT	R	0h	OTP Read fault occurred. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No OTP read fault is detected 1h = OTP read fault detected
7	RESET	R	1h	Device Reset status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = Cleared by FW after read 1h = Device has undergone power on reset
6	SPIFLT	R	0h	SPI Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No SPI fault is detected 1h = SPI fault is detected
5	OCP	R	0h	Overcurrent Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
4	VREFEXT_UV	R	0h	VREF EXT UVLO status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No VREF External UVLO condition is detected 1h = VREF External UVLO condition is detected
3	OVP	R	0h	Over Voltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No over voltage condition is detected 1h = Over voltage condition is detected
2	UVP	R	0h	Supply Undervoltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No undervoltage voltage condition is detected on CP 1h = Undervoltage voltage condition is detected on CP
1	OTF	R	0h	Overtemperature Fault Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device raw Fault status. 0h = No fault condition is detected 1h = Fault condition is detected

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9.2.2 Over Temperature Status Register (Offset = 4h) [Reset = 0000h]

Over Temperature Status Register is shown in Table 9-13.

Return to the Summary Table.

Table 9-13. Over Temperature Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1	OTW	R	0h	Overtemperature Warning Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
0	OTSD	R	0h	Overtemperature Shutdown Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected

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9.2.3 Supply Status Register (Offset = 5h) [Reset = 0000h]

Supply Status Register is shown in Table 9-14.

Return to the Summary Table.

Table 9-14. Supply Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-7	RESERVED	R-0	0h	Reserved
6	VM_OV	R	0h	Vm Over Voltage Fault Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No Vm over voltage is detected 1h = Vm over voltage is detected
5	VREFEXT_UV	R	0h	VREF EXT UVLO status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No VREF External UVLO condition is detected 1h = VREF External UVLO condition is detected
4	CP_UV	R	0h	Charge Pump Undervoltage fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
3-0	RESERVED	R-0	0h	Reserved

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9.2.4 Driver Status Register (Offset = 6h) [Reset = 0000h]

Driver Status Register is shown in Table 9-15.

Return to the Summary Table.

Table 9-15. Driver Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-13	RESERVED	R-0	0h	Reserved
12	W_LS_GATE_LO	R	0h	W phase low side gate signal status 0h = W phase LS FET is ON 1h = W phase LS FET is OFF
11	V_LS_GATE_LO	R	0h	V phase low side gate signal status 0h = V phase LS FET is ON 1h = V phase LS FET is OFF
10	U_LS_GATE_LO	R	0h	U phase low side gate signal status 0h = U phase LS FET is ON 1h = U phase LS FET is OFF
9	W_HS_GATE_LO	R	0h	W phase high side gate signal status 0h = W phase HS FET is ON 1h = W phase HS FET is OFF
8	V_HS_GATE_LO	R	0h	V phase high side gate signal status 0h = V phase HS FET is ON 1h = V phase HS FET is OFF
7	U_HS_GATE_LO	R	0h	U phase high side gate signal status 0h = U phase HS FET is ON 1h = U phase HS FET is OFF
6	OCPC_HS	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side MOSFET of OUTC 1h = Overcurrent detected on high-side MOSFET of OUTC
5	OCPB_HS	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side MOSFET of OUTB 1h = Overcurrent detected on high-side MOSFET of OUTB
4	OCPA_HS	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side MOSFET of OUTA 1h = Overcurrent detected on high-side MOSFET of OUTA
3	RESERVED	R-0	0h	Reserved
2	OCPC_LS	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side MOSFET of OUTC 1h = Overcurrent detected on low-side MOSFET of OUTC
1	OCPB_LS	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side MOSFET of OUTB 1h = Overcurrent detected on low-side MOSFET of OUTB
0	OCPA_LS	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side MOSFET of OUTA 1h = Overcurrent detected on low-side MOSFET of OUTA

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9.2.5 System Interface Status Register (Offset = 7h) [Reset = 0000h]

System Interface Status Register is shown in Table 9-16.

Return to the Summary Table.

Table 9-16. System Interface Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-5	RESERVED	R-0	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	SPI_PARITY	R	0h	SPI Parity Error 0h = No SPI Parity Error is detected 1h = SPI Parity Error is detected
1	RESERVED	R-0	0h	Reserved
0	FRM_ERR	R	0h	SPI Frame Error 0h = No SPI Frame Error is detected 1h = SPI Frame Error is detected

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The DRV8374-Q1 can be used to drive Brushless-DC motors. The following design procedure can be used to configure the DRV8374-Q1.

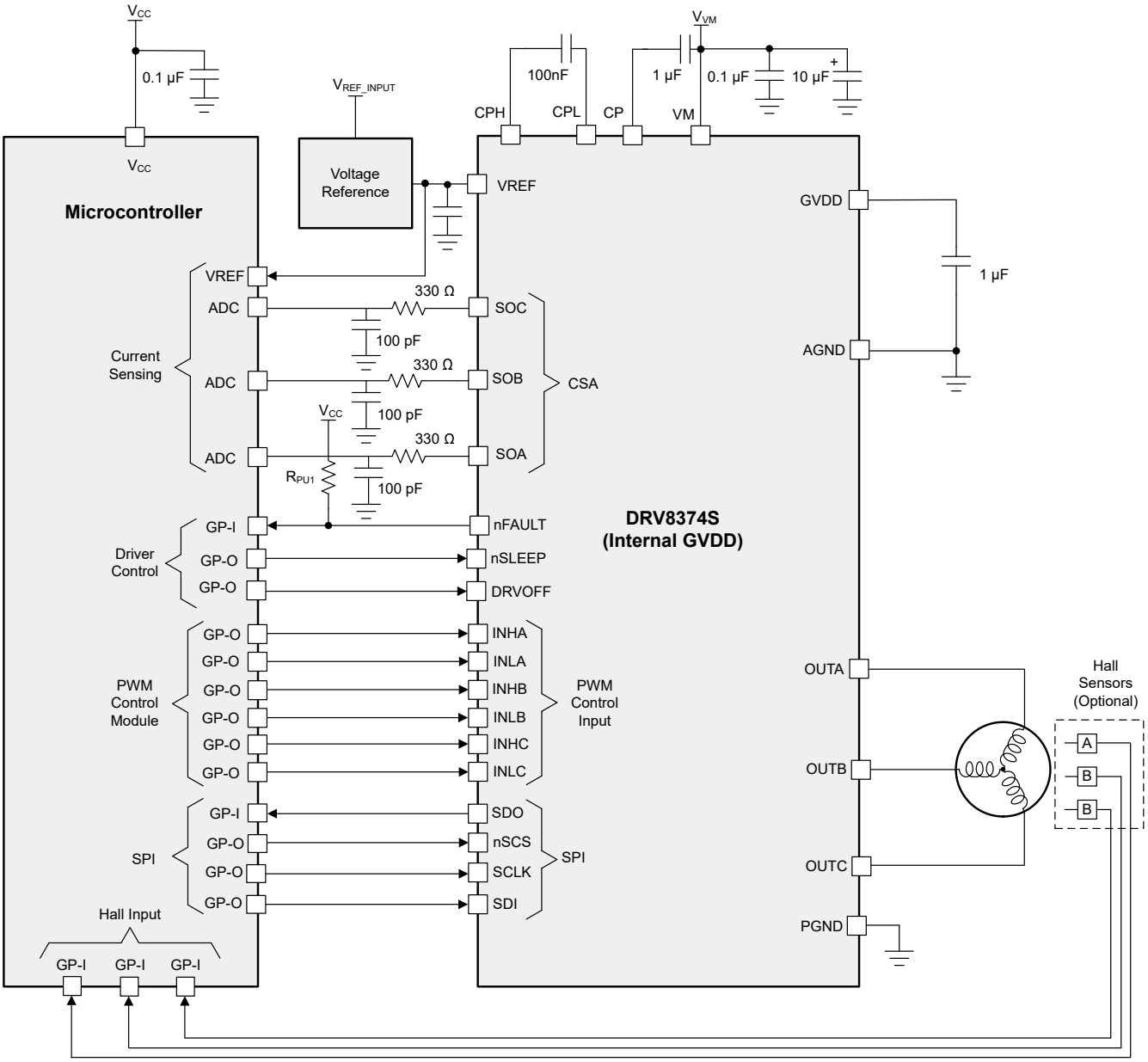


Figure 10-1. Primary Application Schematics 29pin DRV8374 SPI Variant

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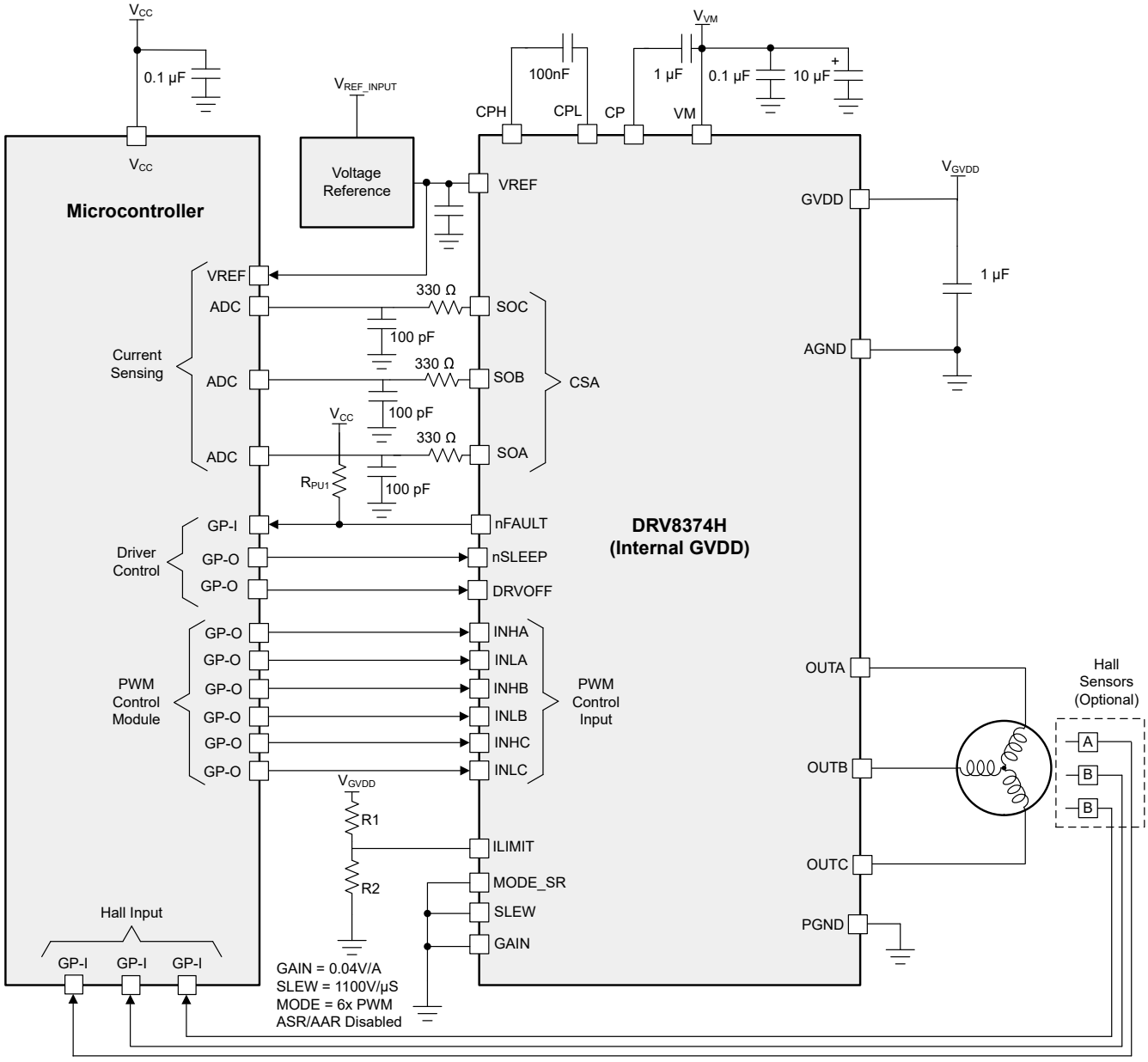


Figure 10-2. Primiary Application Schematics 29pin DRV8374 Hardware Variant

10.2 Power Supply Recommendations

10.2.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally more beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

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The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

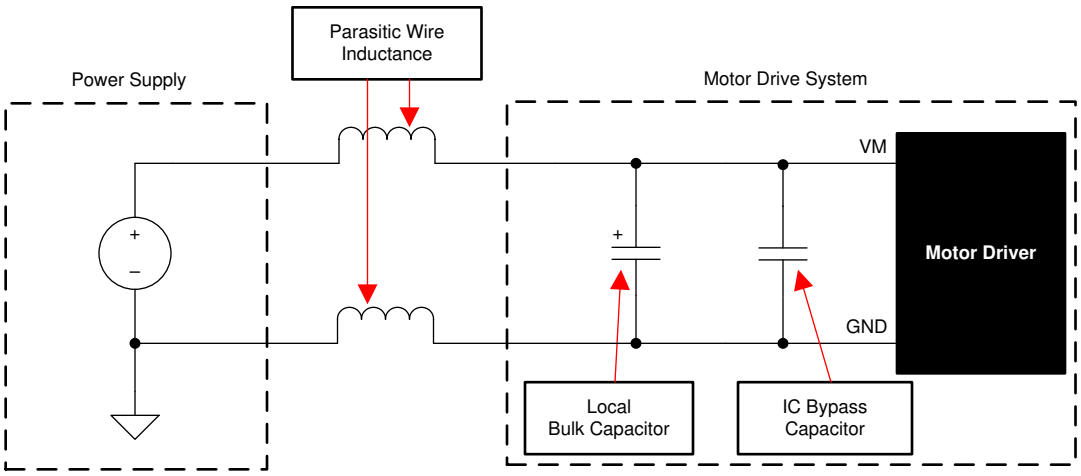


Figure 10-3. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10.3 Layout

10.3.1 Layout Guidelines

The bulk capacitor must be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths must be as wide as possible, and numerous vias must be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current. Small-value capacitors such as the charge pump, GVDD, and VREF capacitors must be ceramic and placed closely to device pins. The high-current device outputs must use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding must be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry to AGND to reduce parasitic effects and improve power dissipation from the device. Maintain grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance. TI recommends to have vias on the PGND pads for better thermal efficiency and run a solid PGND plane underneath the device. Multiple vias must be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

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10.3.2 Layout Example

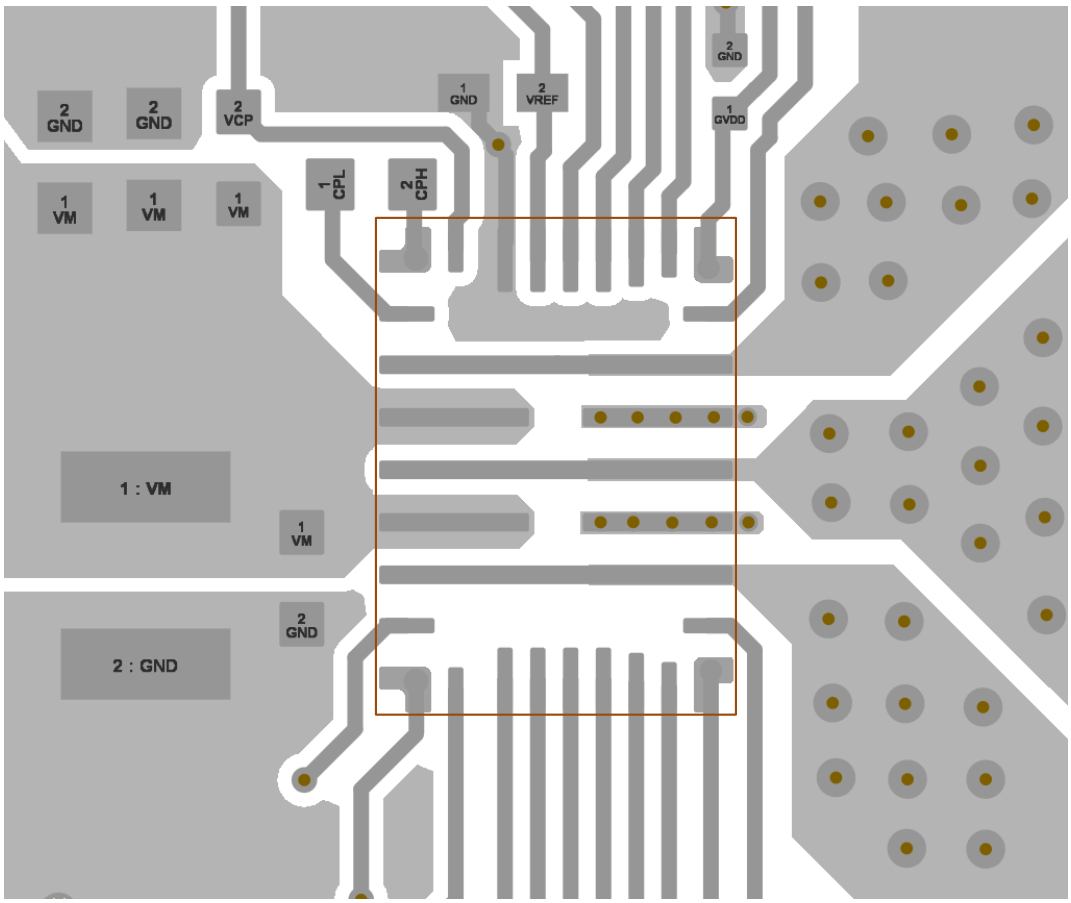


Figure 10-4. Layout example for VQFN 29 pin package

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10.3.3 Thermal Considerations

The DRV8374-Q1 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.3.1 Power Dissipation

The power loss in DRV8374-Q1 include standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in DRV8374-Q1. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and the duration into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that $R_{DS,ON}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

A summary of equations for calculating each loss is shown below for trapezoidal control.

Table 10-1. DRV8374-Q1 Power Losses for Trapezoidal and Field-oriented Control

Loss type	Trapezoidal	Field-oriented control
Power loss due to Quiescent current	$P_{standby} = VM \times I_{VM_TA}$	
LDO	$P_{LDO} = (VM - V_{GVDD}) \times I_{GVDD}$ $P_{LDO} = (VM - V_{AVDD}) \times I_{AVDD}$	
FET conduction	$P_{CON} = 2x\ (I_{PK(trap)})^2 \times R_{ds,on(TA)}$	$P_{CON} = 3x\ (I_{RMS(FOC)})^2 \times R_{ds,on(TA)}$
FET switching	$P_{SW} = I_{PK(trap)} \times V_{PK(trap)} \times t_{rise/fall} \times f_{PWM}$	$P_{SW} = 3x\ I_{RMS(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = 2x\ I_{PK(trap)} \times V_{F(diode)} \times t_{DEADTIME} \times f_{PWM}$	$P_{diode} = 6x\ I_{RMS(FOC)} \times V_{F(diode)} \times t_{DEADTIME} \times f_{PWM}$

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11 Device and Documentation Support

11.1 Documentation Support

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

DATE	REVISION	NOTES
August 2026	*	Initial release.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV8374SQVEORQ1	Active	Preproduction	VQFN-FCRLF (VEO) | 29	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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