DS26LV32AT 3V Enhanced CMOS Quad Differential Line Receiver

Check for Samples: DS26LV32AT

FEATURES

- **Low Power CMOS Design (30 mW typical)**
- **Interoperable with Existing 5V RS-422 Networks**
- **Industrial and Military Temperature Range**
- **Conforms to TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation**
- **3.3V Operation**
- **±7V Common Mode Range @ V_{ID} = 3V**
- **±10V Common Mode Range @ V_{ID} = 0.2V**
- **Receiver OPEN Input Failsafe Feature**
- **Guaranteed AC Parameter:**
  - **Maximum Receiver Skew: 4 ns**
  - **Maximum Transition Time: 10 ns**
- **Pin Compatible with DS26C32AT**
- **32 MHz Toggle Frequency**
- **> 6.5k ESD Tolerance (HBM)**
- **Available in SOIC and CLGA Packaging**
- **Standard Microcircuit Drawing (SMD) 5962-98585**

DESCRIPTION

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV32AT features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The TRI-STATE enables, EN and EN*, allow the device to be active High or active Low. The enables are common to all four receivers.

The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±10V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Connection Diagram

Top View

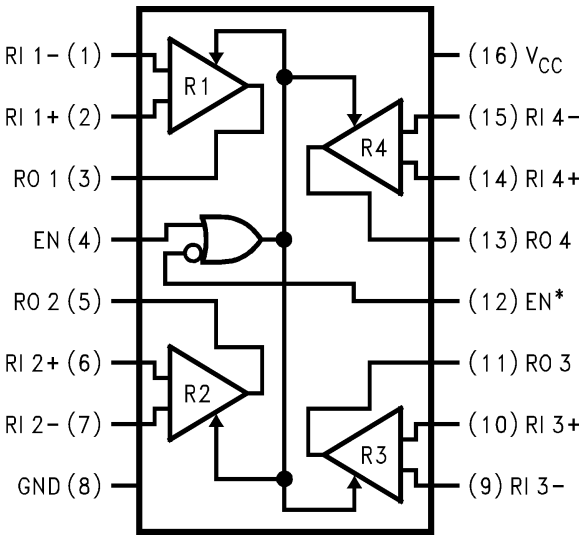


Figure 1.
SOIC Package
See Package Numbers D0016A or NAD0016A

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Truth Table(1)

Enables		Inputs	Output
EN	EN*	RI+–RI−	RO
L	H	X	Z
All other combinations of enable inputs		V_{ID} ≥ +0.2V	H
		V_{ID} ≤ −0.2V	L
		Open(2)	H

(1) L = Logic Low
H = Logic High
X = Irrelevant
Z = TRI-STATE
(2) Open, not terminated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})	−0.5V to +7V
Enable Input Voltage (EN, EN*)	−0.5V to V_{CC} +0.5V
Receiver Input Voltage (V_{ID}: RI+, RI−)	±14V
Receiver Input Voltage (VCM: RI+, RI−)	±14V
Receiver Output Voltage (RO)	−0.5V to V_{CC} +0.5V
Receiver Output Current (RO)	±25 mA Maximum
Maximum Package Power Dissipation @ +25°C	
D0016A Package	1190 mW
NAD0016A Package	1087 mW
Derate D0016A Package 9.8 mW/°C above +25°C	
Derate NAD0016A Package 7.3 mW/°C above +25°C	
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 Sec.)	+260°C
ESD Ratings (HBM, 1.5 kΩ, 100 pF)	
Receiver Inputs and Enables	≥ 6.5 kV
Other Pins	≥ 2 kV

(1) "Absolute Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature Range (T_A)				
DS26LV32AT	−40	+25	+85	°C
DS26LV32AW	−55	+25	+125	°C

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Electrical Characteristics (1) (2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold	$V_{OUT} = V_{OH}$ or V_{OL}	V_{CM} = −7V to +7V, T_A = -40°C to +85°C	RI+, RI−	−200	±17.5	+200	mV
			V_{CM} = −0.5V to +5.5V, T_A = -55°C to +125°C (3)		-200		+200	mV
V_{HY}	Hysteresis	V_{CM} = 1.5V				35		mV
V_{IH}	Minimum High Level Input Voltage			EN, EN*	2.0			V
V_{IL}	Maximum Low Level Input Voltage						0.8	V
R_{IN}	Input Resistance	V_{IN} = −7V, +7V, T_A = -40°C to +85°C (Other Input = GND)		RI+, RI−	5.0	8.5		kΩ
		V_{IN} = −0.5V, +5.5V, T_A = -55°C to +125°C (Other Input = GND) (3)			5.0			kΩ
I_{IN}	Input Current (Other Input = 0V, Power On, or V_{CC} = 0V)	V_{IN} = +10V	T_A = -40°C to +85°C		0	1.1	1.8	mA
		V_{IN} = +3V			0	0.27		mA
		V_{IN} = 0.5V				−0.02		mA
		V_{IN} = −3V			0	−0.43		mA
		V_{IN} = −10V			0	−1.26	−2.2	mA
		V_{IN} = −0.5V	T_A = -55°C to +125°C (3)		0		-1.8	mA
		V_{IN} = 5.5V			0		1.8	mA
I_{EN}	Input Current	V_{IN} = 0V to V_{CC}		EN, EN*			±1	µA
V_{OH}	High Level Output Voltage	I_{OH} = −6 mA, V_{ID} = +1V		RO	2.4	3		V
		I_{OH} = −6 mA, V_{ID} = OPEN						
V_{OH}	High Level Output Voltage	I_{OH} = −100 µA, V_{ID} = +1V				V_{CC} −0.1		V
		I_{OH} = − 100 µA, V_{ID} = OPEN						
V_{OL}	Low Level Output Voltage	I_{OL} = +6 mA, V_{ID} = −1V				0.13	0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{OUT} = V_{CC}$ or GND					±50	µA
		EN = V_{IL}, EN* = V_{IH}						
I_{SC}	Output Short Circuit Current	V_O = 0V, $V_{ID} \geq$ |200 mV| (4)			−10	−35	−70	mA
I_{CC}	Power Supply Current	No Load, All RI+, R1− = OPEN, EN, EN* = V_{CC} or GND	T_A = -40°C to +85°C	V_{CC}		9	15	mA
			T_A = -55°C to +125°C				20	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}.
(2) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(3) This parameter does not meet the TIA/EIA-422-B specification.
(4) Short one output at a time to ground. Do not exceed package.

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Switching Characteristics - Industrial (1) (2)

Over Supply Voltage and -40°C to +85°C Operating Temperature range, unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF, V_{CM} = 1.5V (Figure 2 and Figure 3)	6	17.5	35	ns
t_{PLH}	Propagation Delay Low to High		6	17.8	35	ns
t_r	Rise Time (20% to 80%)			4.1	10	ns
t_f	Fall Time (80% to 20%)			3.3	10	ns
t_{PHZ}	Disable Time	C_L = 50 pF, V_{CM} = 1.5V (Figure 4 and Figure 5)			40	ns
t_{PLZ}	Disable Time				40	ns
t_{PZH}	Enable Time				40	ns
t_{PZL}	Enable Time				40	ns
t_{SK1}	Skew, $\|t_{PHL} - t_{PLH}\|$ (3)	C_L = 15 pF, V_{CM} = 1.5V		0.3	4	ns
t_{SK2}	Skew, Pin to Pin (4)			0.6	4	ns
t_{SK3}	Skew, Part to Part (2)			7	17	ns
f_{MAX}	Maximum Operating Frequency (5)	C_L = 15 pF, V_{CM} = 1.5V	32			MHz

(1) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(2) t_{SK3} is the difference in propagation delay times between any channels of any devices. This specification (maximum limit) applies to devices within V_{CC} ±0.1V of one another, and a Delta T_A = ±5°C (between devices) within the operating temperature range. This parameter is guaranteed by design and characterization.
(3) t_{SK1} is the $|t_{PHL} - t_{PLH}|$ of a channel.
(4) t_{SK2} is the maximum skew between any two channels within a device, either edge.
(5) All channels switching, Output Duty Cycle criteria is 40%/60% measured at 50%. Input = 1V to 2V, 50% Duty Cycle, $t_r/t_f \leq 5$ ns. This parameter is guaranteed by design and characterization.

Switching Characteristics - Military

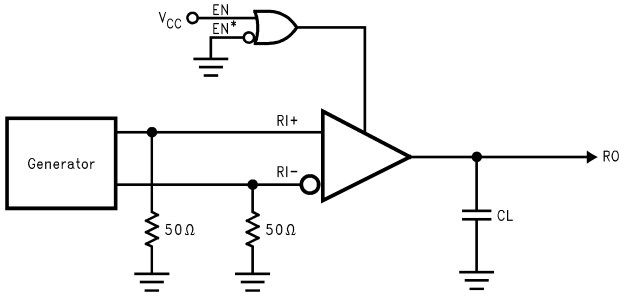
Over Supply Voltage and -55°C to +125°C Operating Temperature range, unless otherwise specified.

Parameter		Test Conditions	Min	Max	Units
t_{PHL}	Propagation Delay High to Low	C_L = 50 pF, V_{CM} = 1.5V (Figure 2 and Figure 3)	6	45	ns
t_{PLH}	Propagation Delay Low to High		6	45	ns
t_{PHZ}	Disable Time	C_L = 50 pF, V_{CM} = 1.5V (Figure 4 and Figure 5)		50	ns
t_{PLZ}	Disable Time			50	ns
t_{PZH}	Enable Time			50	ns
t_{PZL}	Enable Time			50	ns
t_{SK1}	Skew, $\|t_{PHL} - t_{PLH}\|$ (1)	C_L = 50 pF, V_{CM} = 1.5V		6	ns
t_{SK2}	Skew, Pin to Pin (2)			6	ns

(1) t_{SK1} is the $|t_{PHL} - t_{PLH}|$ of a channel.
(2) t_{SK2} is the maximum skew between any two channels within a device, either edge.

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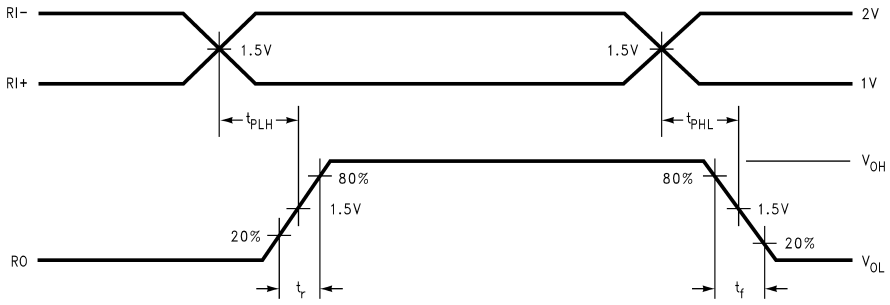
PARAMETER MEASUREMENT INFORMATION



A. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

B. C_L includes probe and jig capacitance.

Figure 2. Receiver Propagation Delay and Transition Time Test Circuit



A. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

B. C_L includes probe and jig capacitance.

C. For military grade product, t_r ≤ 6ns and t_f ≤ 6ns.

D. For military grade product the measure point is 1/2 V_{CC} for t_{PLH}, t_{PHL}, t_{PZL}, and t_{PZH}.

Figure 3. Receiver Propagation Delay and Transition Time Waveform

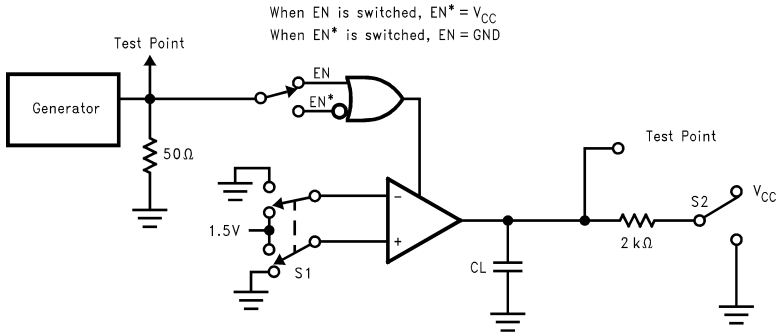
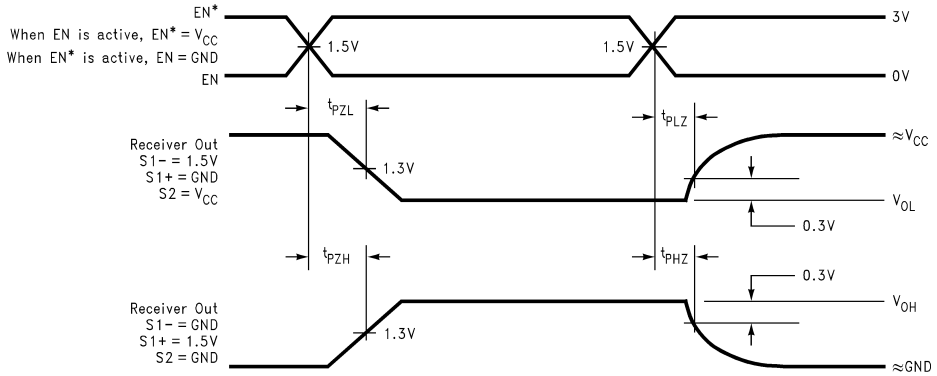


Figure 4. Receiver TRI-STATE Test Circuit



A. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

B. C_L includes probe and jig capacitance.

C. For military grade product, t_r ≤ 6ns and t_f ≤ 6ns.

D. For military grade product the measure point is 1/2 V_{CC} for t_{PLH}, t_{PHL}, t_{PZL}, and t_{PZH}.

Figure 5. Receiver TRI-STATE Output Enable and Disable Waveforms

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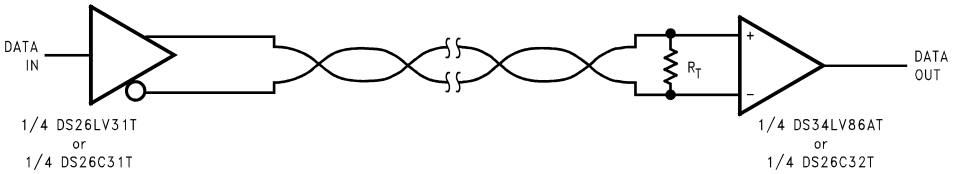
TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- AN-214
- AN-457
- AN-805
- AN-847
- AN-903
- AN-912
- AN-916

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in parallel with 0.01 µF at the power supply pin. A 10 µF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.



R_T is optional although highly recommended to reduce reflection

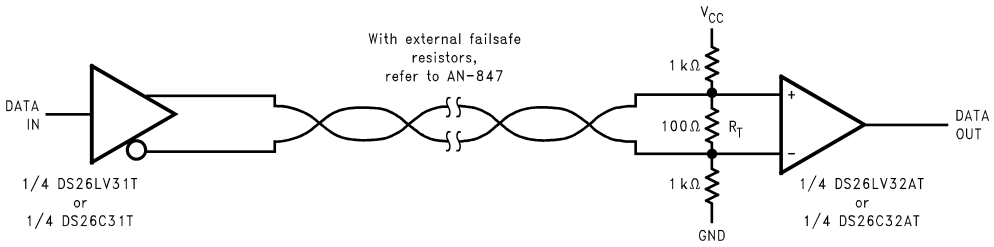


Figure 6. Typical Receiver Connections

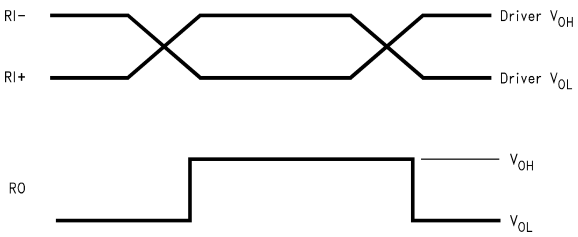


Figure 7. Typical Receiver Output Waveforms

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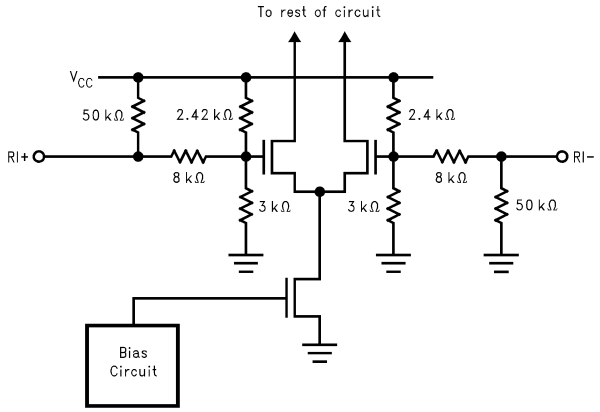


Figure 8. Typical Receiver Input Circuit

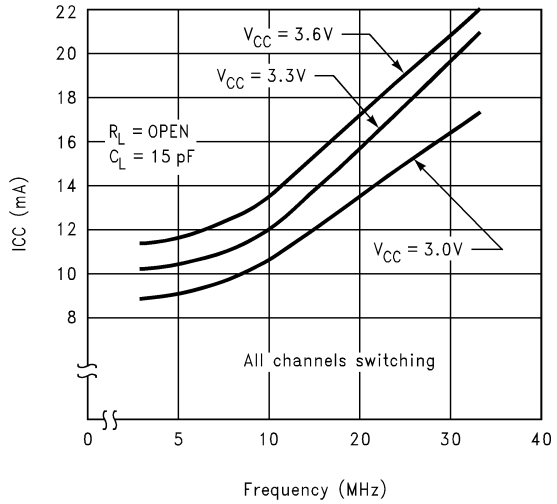


Figure 9. Typical I_{CC} vs Frequency

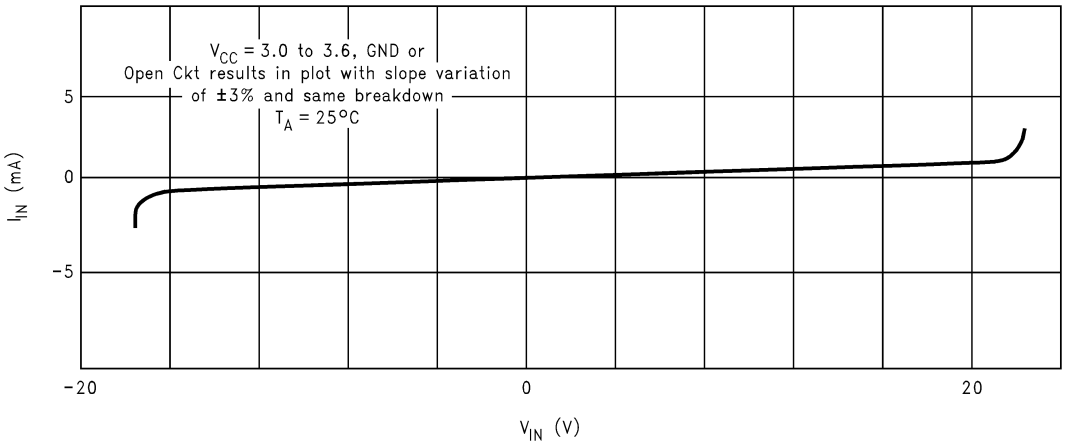


Figure 10. Receiver I_{IN} vs V_{IN} (Power On or Power Off)

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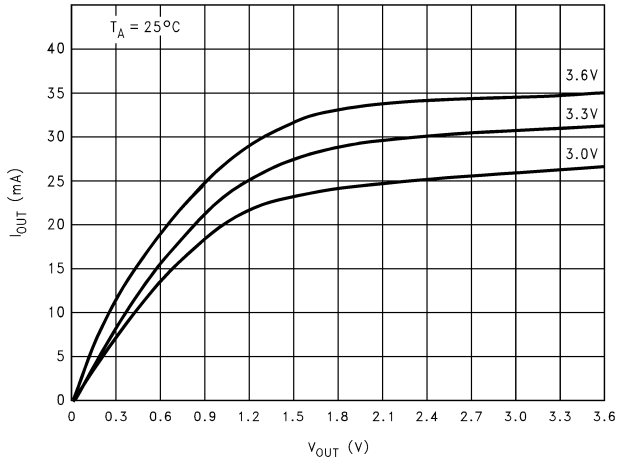


Figure 11. I_{OL} vs V_{OL}

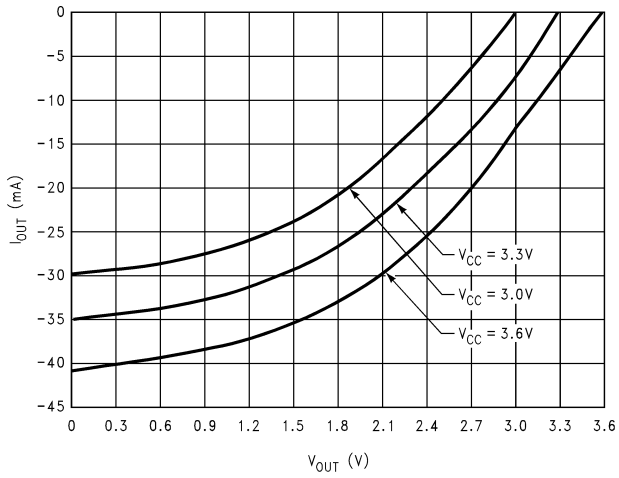


Figure 12. I_{OH} vs V_{OH}

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REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS26LV32ATMX/NOPB.B	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	See DS26LV32ATMX/ NOPB	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

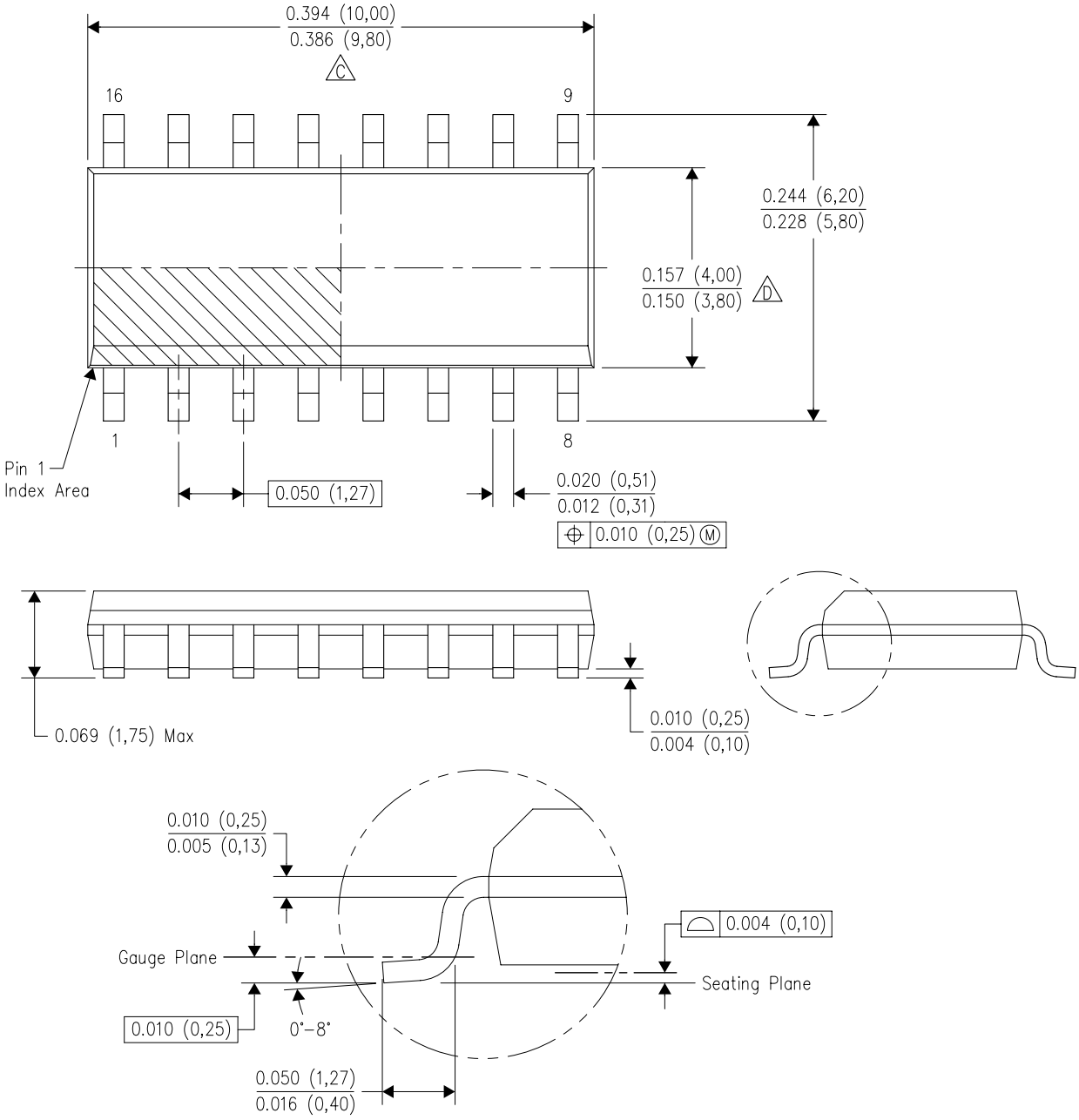
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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