

ESD2CANxx24-Q1 Automotive 24V, 2-Channel ESD Protection Diode for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
 - $\pm 30\text{kV}$, $\pm 25\text{kV}$ or $\pm 20\text{kV}$ contact discharge
 - $\pm 30\text{kV}$, $\pm 25\text{kV}$ or $\pm 20\text{kV}$ air-gap discharge
- ISO 10605 (330pF, 330 Ω) ESD protection:
 - $\pm 27\text{kV}$ or $\pm 20\text{kV}$ contact discharge
 - $\pm 27\text{kV}$ or $\pm 20\text{kV}$ air-gap discharge
- Tested in compliance to IEC 61000-4-5
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD protection with single component
- Low clamping voltage protects downstream components
- AEC-Q101 qualified
- I/O capacitance = 3pF, 2.5pF, or 1.7pF (typical)
- SOT-23 (DBZ) small, standard, common footprint
- SOT-323, SC-70 (DCK) very small, standard, space saving, common footprint
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- **Automotive in-vehicle networks:**
 - Controller area network (CAN)
 - Controlled area network flexible data-rate (CAN-FD)
 - Low, fault tolerant CAN
 - High-speed CAN
- **Industrial control networks:**
 - DeviceNet IEC 62026-3
 - CANopen – CiA 301/302-2 and EN 50325-4

3 Description

The ESD2CANxx24-Q1 is a bidirectional ESD protection diode for Controller Area Network (CAN) interface protection. The ESD2CANxx24-Q1 is rated to dissipate contact ESD strikes beyond the maximum level specified in the ISO 10605 automotive standard ($\pm 27\text{kV}$ Contact, $\pm 27\text{kV}$ Airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as automotive systems require a high level of robustness and reliability for safety applications.

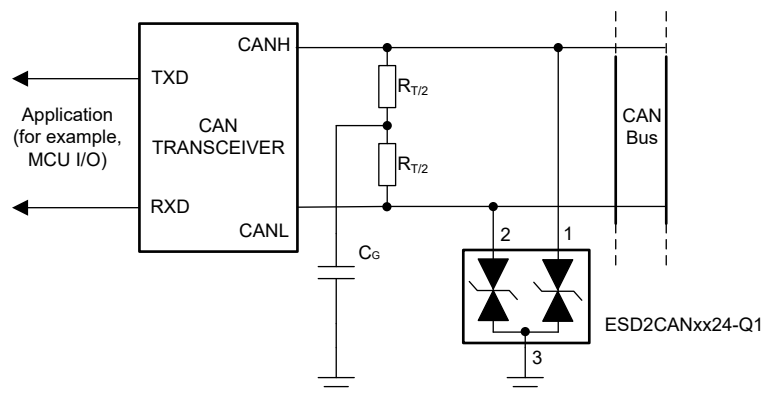
This device features a low IO capacitance per channel and a pin-out to suit two automotive CAN bus lines (CANH and CANL) from the damage caused by ElectroStatic Discharge (ESD) and other transients. Additionally, the 3pF (typical) or less line capacitance of the ESD2CANxx24-Q1 is designed for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10Mbps.

The ESD2CANxx24-Q1 is offered in two leaded packages for easy flow through routing.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ESD2CAN24-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	DCK (SC-70, 3)	2.00mm × 2.10mm
ESD2CANFD24-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm
ESD2CANXL24-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



ESD2CANxx24-Q1 Typical Application



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4 Pin Configuration and Functions

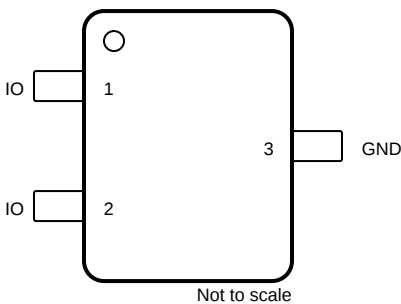


Figure 4-1. DCK or DBZ Package, 3-Pin SC-70 or SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

Parameter		DEVICE	MIN	MAX	UNIT
P _{pp}	IEC 61000-4-5 Power (t _p – 8/20 μs) at 25°C	ESD2CAN24-Q1		210	W
		ESD2CANFD24-Q1		133	
		ESD2CANXL24-Q1		90	
I _{pp}	IEC 61000-4-5 current (t _p – 8/20 μs) at 25°C	ESD2CAN24-Q1		5.7	A
		ESD2CANFD24-Q1		3.5	
		ESD2CANXL24-Q1		2.5	
T _A	Operating free-air temperature		-55	150	°C
T _J	Junction temperature		-55	150	
T _{stg}	Storage temperature		-65	155	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

Parameter		Test Conditions	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 ⁽¹⁾	± 2500	V
		Charged device model (CDM), per AEC Q101-005	± 1000	

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings—IEC Specification

over T_A = 25°C (unless otherwise noted)

Parameter		Test Conditions	DEVICE	VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD2CAN24-Q1	±30000	V
			ESD2CANFD24-Q1	±25000	
			ESD2CANXL24-Q1	±20000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD2CAN24-Q1	±30000	
			ESD2CANFD24-Q1	±25000	
			ESD2CANXL24-Q1	±20000	

5.4 ESD Ratings - ISO Specification

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Parameter			Test Conditions	DEVICE	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Contact discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN24-Q1	±30000	V
				ESD2CANFD24-Q1	±25000	
				ESD2CANXL24-Q1	±20000	
			ISO 10605, 330pF, 330Ω, IO	ESD2CAN24-Q1	±27000	
				ESD2CANFD24-Q1	±20000	
				ESD2CANXL24-Q1	±20000	
		Air-gap discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN24-Q1	±30000	
				ESD2CANFD24-Q1	±25000	
				ESD2CANXL24-Q1	±20000	
			ISO 10605, 330pF, 330Ω, IO	ESD2CAN24-Q1	±27000	
				ESD2CANFD24-Q1	±20000	
				ESD2CANXL24-Q1	±20000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD2CAN24-Q1		ESD2CANFD24-Q1	ESD2CANXL24-Q1	UNIT
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	DBZ (SOT-23)	
		3 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.5	283.0	316.3	325.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.1	164.1	170.7	178.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	131.1	105.1	156.2	165.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.0	67.1	45.9	52.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	130.2	104.4	155.1	164.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.7 Electrical Characteristics

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			-24		24	V
V_{BRF}	Breakdown voltage ⁽²⁾	$I_{IO} = 10\text{mA}$, IO to GND		25.5		35.5	V
V_{BRR}	Breakdown voltage ⁽²⁾	$I_{IO} = -10\text{mA}$, IO to GND		-35.5		-25.5	V
V_{CLAMP}	Clamping voltage ⁽³⁾	$I_{PP} = 5.7\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CAN24-Q1		37		V
		$I_{PP} = 3.5\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CANFD24-Q1		37		
		$I_{PP} = 2.5\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CANXL24-Q1		36		
V_{CLAMP}	Clamping voltage ⁽⁴⁾	$I_{PP} = 16\text{A}$, TLP, IO to GND or GND to IO	ESD2CAN24-Q1		35		V
			ESD2CANFD24-Q1		36		
			ESD2CANXL24-Q1		38		
V_{Hold}	Holding voltage after snapback	TLP	ESD2CAN24-Q1		30		V
			ESD2CANFD24-Q1		30		
			ESD2CANXL24-Q1		30		
I_{LEAK}	Leakage current	$V_{IO} = \pm 24\text{V}$, IO to GND		-50	5	50	nA
R_{DYN}	Dynamic resistance ⁽⁴⁾	IO to GND and GND to IO	ESD2CAN24-Q1		0.35		Ω
			ESD2CANFD24-Q1		0.45		Ω
			ESD2CANXL24-Q1		0.57		Ω
C_L	Line capacitance ⁽⁵⁾	$V_{IO} = 0\text{V}$, $f = 1\text{MHz}$, $V_{pp} = 30\text{mV}$	ESD2CAN24-Q1		3	5	pF
			ESD2CANFD24-Q1		2.5	4.2	
			ESD2CANXL24-Q1		1.7	2.8	

(1) Measurements made on each IO channel

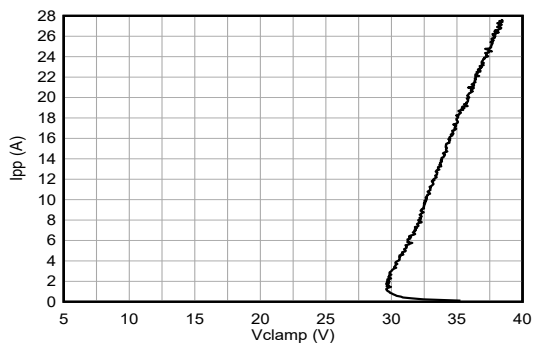
(2) V_{BRF} and V_{BRR} are defined as the voltage when $\pm 10\text{mA}$ is applied in the positive and negative going direction respectively, before the device latches into the snapback state

(3) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5

(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

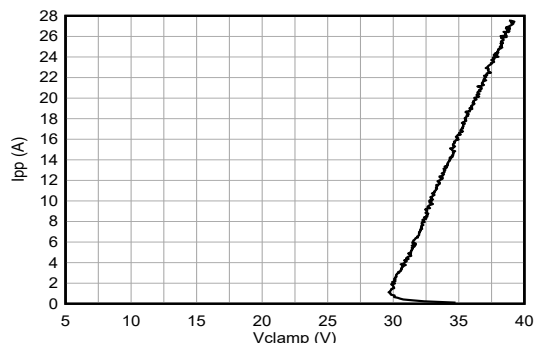
(5) Measured from IO to GND on each channel

5.8 Typical Characteristics – ESD2CAN24-Q1



tp = 100 ns, Transmission Line Pulse (TLP)

Figure 5-1. Positive TLP Curve



tp = 100 ns, Transmission Line Pulse (TLP)

Figure 5-2. Negative TLP Curve

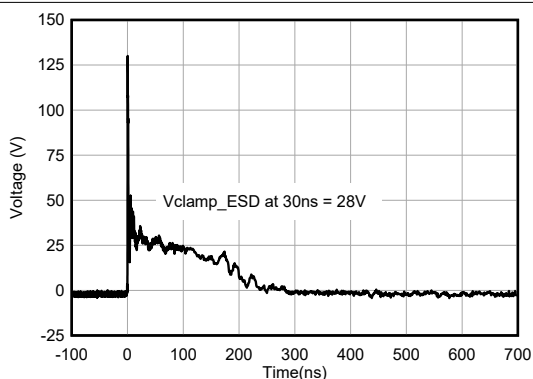


Figure 5-3. +8-kV Clamped IEC Waveform

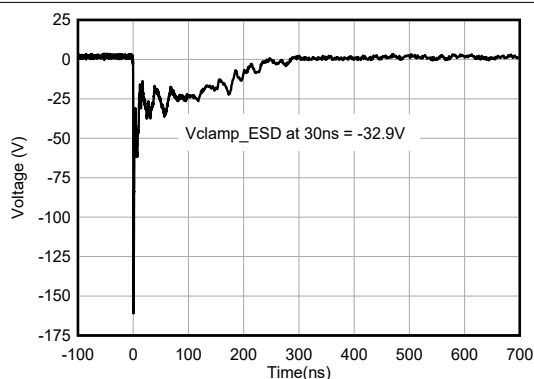


Figure 5-4. -8-kV Clamped IEC Waveform

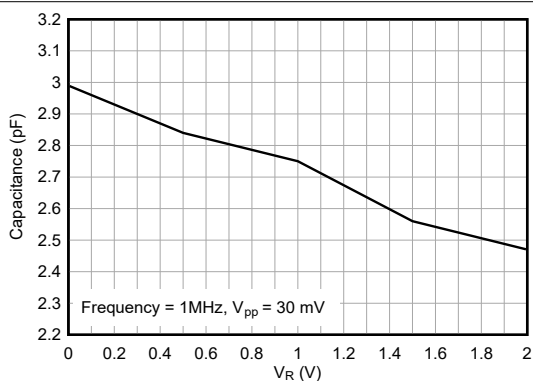


Figure 5-5. Capacitance vs. Bias Voltage

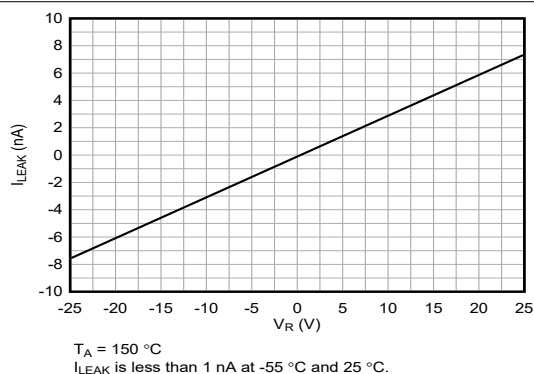


Figure 5-6. Leakage Current vs. Bias Voltage Across Temperature

5.8 Typical Characteristics – ESD2CAN24-Q1 (continued)

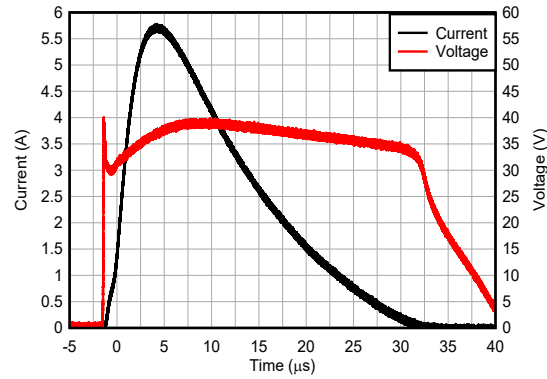
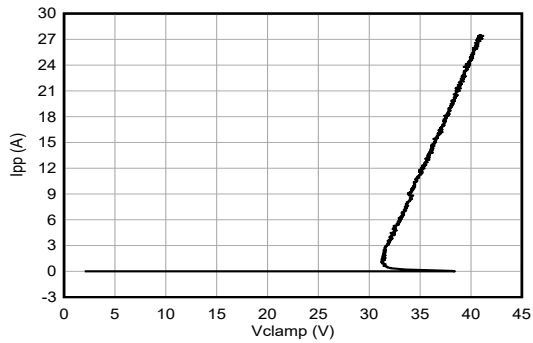


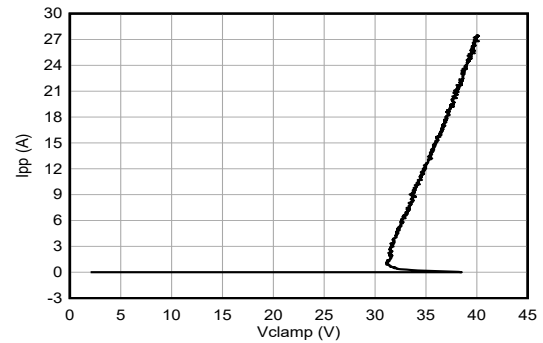
Figure 5-7. 8/20µs Surge Response at 5.7A

5.9 Typical Characteristics – ESD2CANFD24-Q1



tp = 100 ns, Transmission Line Pulse (TLP)

Figure 5-8. Positive TLP Curve



tp = 100 ns, Transmission Line Pulse (TLP)

Figure 5-9. Negative TLP Curve

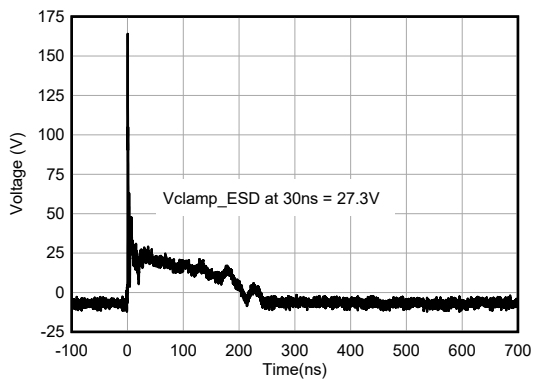


Figure 5-10. +8kV Clamped IEC Waveform

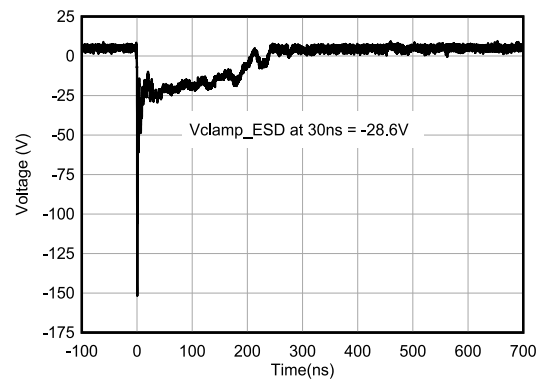


Figure 5-11. -8kV Clamped IEC Waveform

5.9 Typical Characteristics – ESD2CANFD24-Q1 (continued)

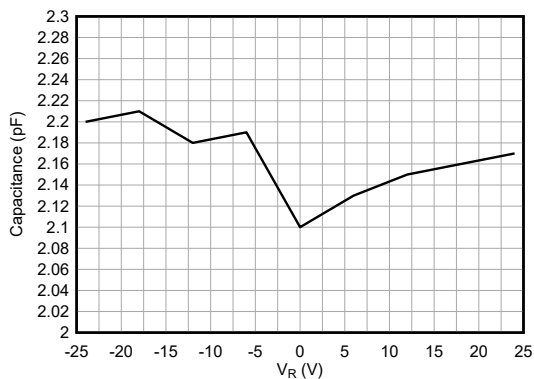


Figure 5-12. Capacitance vs. Bias Voltage

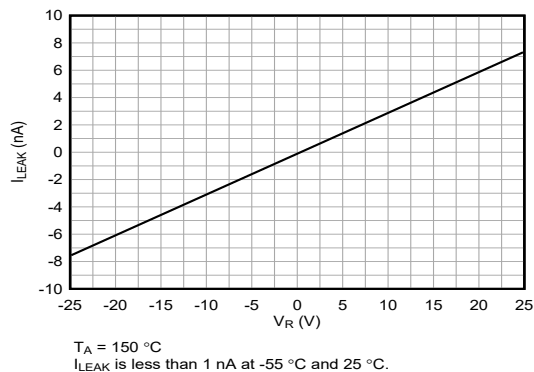


Figure 5-13. Leakage Current vs. Bias Voltage Across Temperature

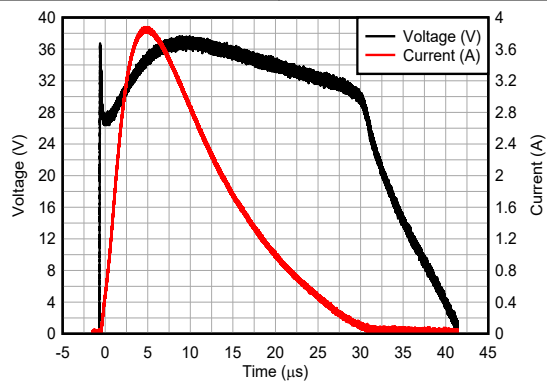


Figure 5-14. 8/20 μs Surge Response at 5.7A

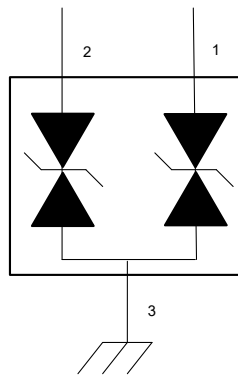
6 Detailed Description

6.1 Overview

The ESD2CANxx24-Q1 is a dual-channel ESD TVS diode in SOT-23 and SC-70 leaded packages which are convenient for automatic optical inspection. This product offers ISO 10605 $\pm 27\text{kV}$ or $\pm 20\text{kV}$ air-gap, $\pm 27\text{kV}$ or $\pm 20\text{kV}$ contact ESD protection, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support. The pF (typical) or less line capacitance of this ESD protection diode is designed for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10Mbps.

A typical application for this product is ESD circuit protection for CAN transceivers used in automotive applications. The ESD2CANxx24-Q1 is a good fit for the ESD protection inside automotive electronic control units (ECUs) for head lights, door modules, climate control, roof control, wipers, cluster, audio, and many other automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

The ESD2CANxx24-Q1 is a bidirectional TVS with a high ESD protection level. This device protects the circuit from ESD strikes up to $\pm 27\text{kV}$ or $\pm 20\text{kV}$ contact and $\pm 27\text{kV}$ or $\pm 20\text{kV}$ air-gap specified in the ISO 10605 automotive standard. The device can also handle up to 5.7A surge current (IEC 61000-4-5 8/20 μs). The I/O capacitance of 3pF (typical) supports a data rate up to 10Mbps. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 37V when the device is taking 5.7A transient surge current. The breakdown is bidirectional so this protection device is a good fit for CAN which is a differential signal. Low leakage allows the diode to conserve power when working below the V_{RWM} . The temperature range of -55°C to $+150^{\circ}\text{C}$ makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 and SC-70 packages are good for applications requiring automatic optical inspection (AOI).

6.3.1 AEC-Q101 Qualified and Temperature Range

This device is qualified to AEC-Q101 standards and is qualified to operate from -55°C to $+150^{\circ}\text{C}$.

6.3.2 ISO 10605 ESD Protection

The I/O pins can withstand ESD events of up to $\pm 27\text{kV}$ contact and $\pm 27\text{kV}$ air-gap in the leaded SOT-23 and SC-70 packages according to the ISO 10605 (330pF and 330 Ω loading condition) standard. An ESD-surge clamp diverts the current to ground.

6.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.7A (8/20 μs waveform). An ESD-surge clamp diverts this current to ground.

6.3.4 IO Capacitance

The capacitance between the I/O pins is 3pF (typical) or less. This capacitance supports data rates for CAN, CANFD, CAN SiC, and CAN-XL up to 10Mbps.

6.3.5 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.57Ω (Pin 1 or Pin 2 to Pin 3) and 0.57Ω (Pin 3 to Pin 1 or Pin 2) or less which prevents system damage during ESD events.

6.3.6 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of $\pm 25.5V$. This protects sensitive equipment from surges above the reverse standoff voltage of $\pm 24V$.

6.3.7 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of $\pm 50nA$ (maximum) with a bias of $\pm 24V$.

6.3.8 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to $37V$ ($I_{PP} = 5.7A$) and $35V$ ($I_{PP} = 16A$ for TLP) for ESD2CAN24-Q1, and $38V$ ($I_{PP} = 3.5A$) and $34V$ ($I_{PP} = 16A$ for TLP) for ESD2CANFD24-Q1, and $36V$ ($I_{PP} = 1.5A$) and $38V$ ($I_{PP} = 16A$ for TLP) for ESD2CANXL24-Q1.

6.3.9 Industry Standard Leaded Packages

This device features industry standard SOT-23 (DBZ) and SC-70 (DCK) leaded packages for automatic optical inspection (AOI).

6.4 Device Functional Modes

The ESD2CANxx24-Q1 is a dual channel passive clamp that has low leakage during normal operation when the voltage between pin 1 or pin 2 and pin 3 is below V_{RWM} , and activates when the voltage between pin 1 or pin 2 and pin 3 goes above V_{BR} . During ISO 10605 ESD events, transient voltages as high as $\pm 27kV$ can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD} , the device reverts back to the low leakage passive state.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD2CANxx24-Q1 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on differential CAN signal lines. The CAN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from an ESD strike passes through the TVS diode, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS diode holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

7.2 Typical Application

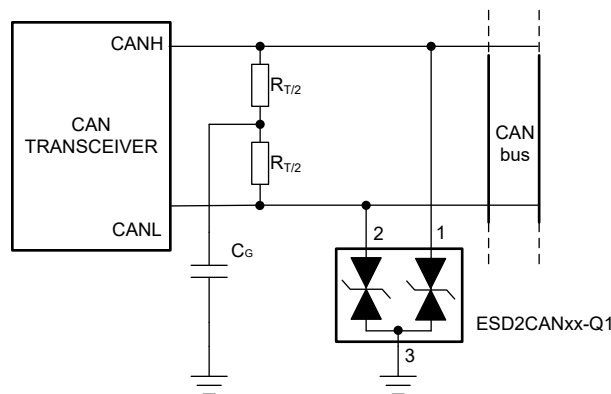


Figure 7-1. ESD2CANxx24-Q1 Typical Application

7.2.1 Design Requirements

For this design example, the ESD2CANxx24-Q1 is used to provide ESD protection for a CAN transceiver. [Table 7-1](#) lists the known design parameters for this application.

Table 7-1. Design Parameters for the ESD2CAN24-Q1 Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} differential signal range	$> \pm 1.5V$
V_{RWM}	$\pm 24V$
Jumpstart short to battery event on V_{IO}	$\pm 24V$
Data rate	Up to 10Mbps
$RT/2$	60Ω

7.2.2 Detailed Design Procedure

The ESD2CANxx24-Q1 has a V_{RWM} of $\pm 24V$ to protect the diode from being damaged during a short to battery event that can occur by reversing the terminal connections during jumpstart. The bidirectional characteristic enables signal integrity across positive and negative signal inputs, as well as accounts for any line faults or miswiring. The low capacitance of 3pF (typical) enables data rates up to 10Mbps, which allows the designer to meet the requirements for CAN, CANFD, CAN SiC, and CAN-XL. The 60Ω split termination improves the

electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that can be present on the differential signal lines.

For additional information, please see the [CAN Bus ESD Protection Application Note](#).

8 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

9 Layout

9.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

9.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.

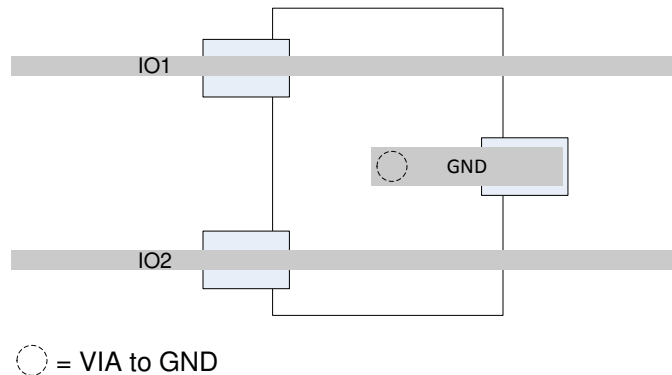


Figure 9-1. Routing with DBZ and DCK Package

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2022) to Revision D (March 2026)	Page
• Updated ISO 330pF/330Ω contact spec from 30kV to 27kV for ESD2CAN24-Q1.....	5
• Updated ISO 330pF/330Ω contact spec from 25kV to 20kV for ESD2CANFD24-Q1.....	5
• Updated ISO 330pF/330Ω air-gap spec from 30kV to 27kV for ESD2CAN24-Q1.....	5
• Updated ISO 330pF/330Ω air-gap spec from 25kV to 20kV for ESD2CANFD24-Q1.....	5

Changes from Revision B (September 2022) to Revision C (November 2022)	Page
• Changed the status of the ESD2CANFD24-Q1 and ESD2CANXL24-Q1 devices from: <i>preview</i> to: <i>active</i>	1

Changes from Revision A (June 2022) to Revision B (September 2022)	Page
• Changed the status of data sheet from: <i>Advanced Information</i> to: <i>Production Data</i>	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD2CAN24DBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1L3
ESD2CAN24DBZRQ1.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1L3
ESD2CAN24DCKRQ1	Active	Production	SC70 (DCK) 3	3000 LARGE T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-55 to 150	1L6
ESD2CAN24DCKRQ1.B	Active	Production	SC70 (DCK) 3	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 150	1L6
ESD2CANFD24DBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2QP8
ESD2CANFD24DBZRQ1.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2QP8
ESD2CANXL24DBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RI8
ESD2CANXL24DBZRQ1.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RI8

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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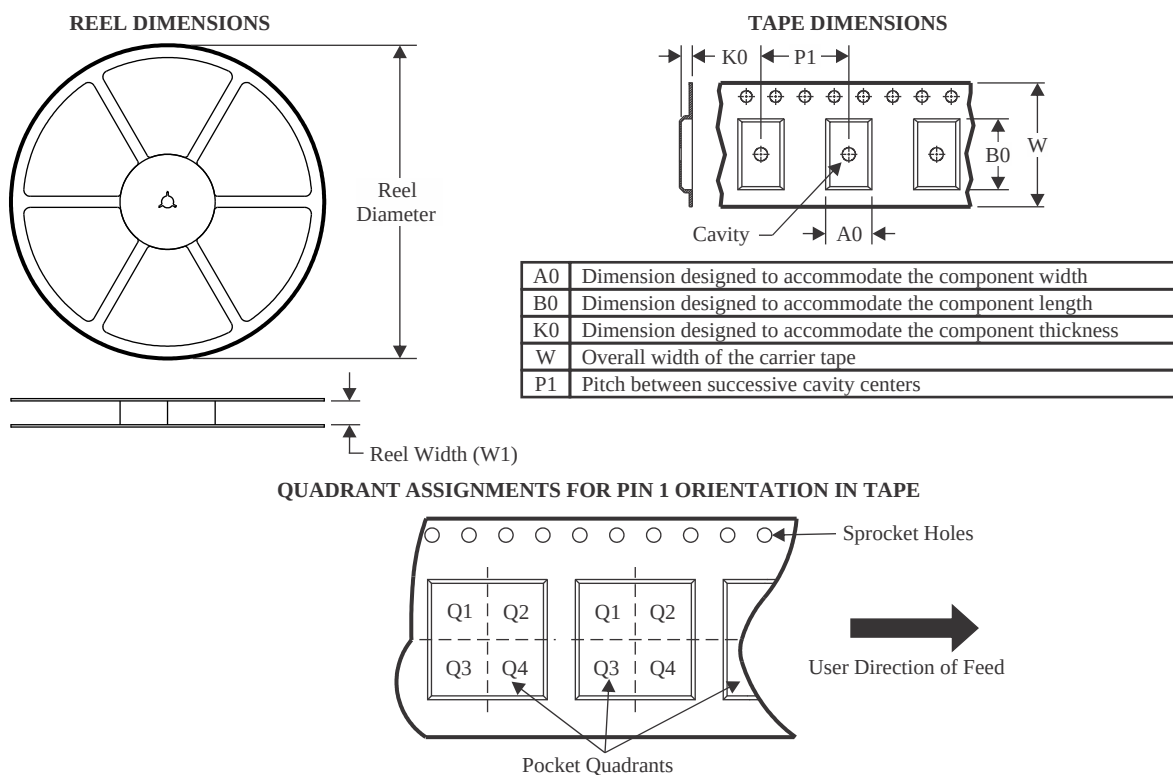
OTHER QUALIFIED VERSIONS OF ESD2CANFD24-Q1 :

- Catalog : [ESD2CANFD24](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

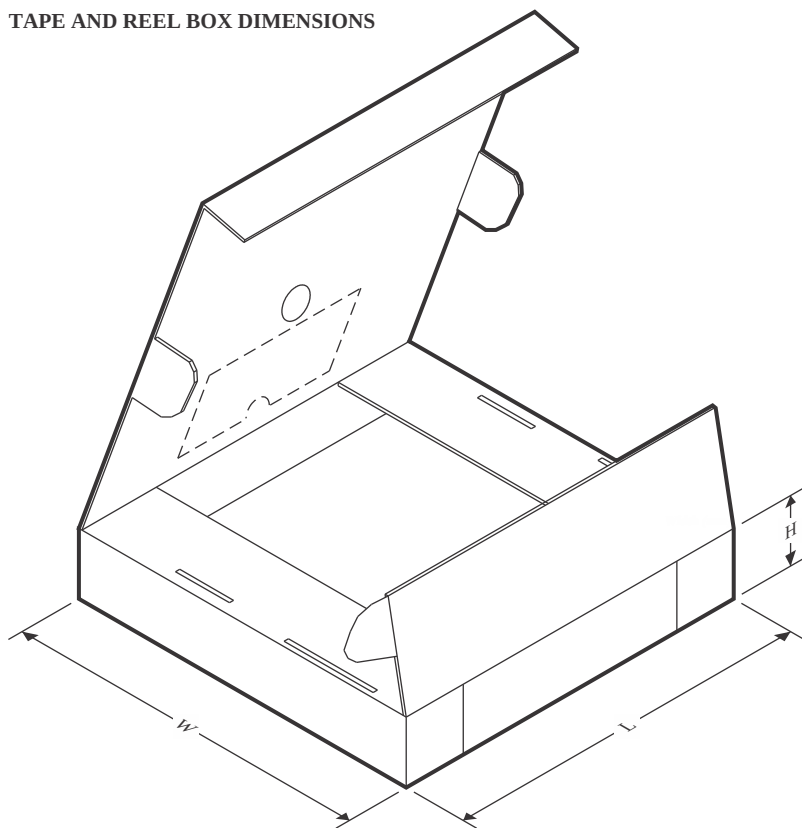
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CAN24DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD2CAN24DCKRQ1	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
ESD2CAN24DCKRQ1	SC70	DCK	3	3000	180.0	8.4	2.3	2.75	1.2	4.0	8.0	Q3
ESD2CANFD24DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD2CANXL24DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

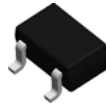
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CAN24DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD2CAN24DCKRQ1	SC70	DCK	3	3000	190.0	190.0	30.0
ESD2CAN24DCKRQ1	SC70	DCK	3	3000	210.0	185.0	35.0
ESD2CANFD24DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD2CANXL24DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

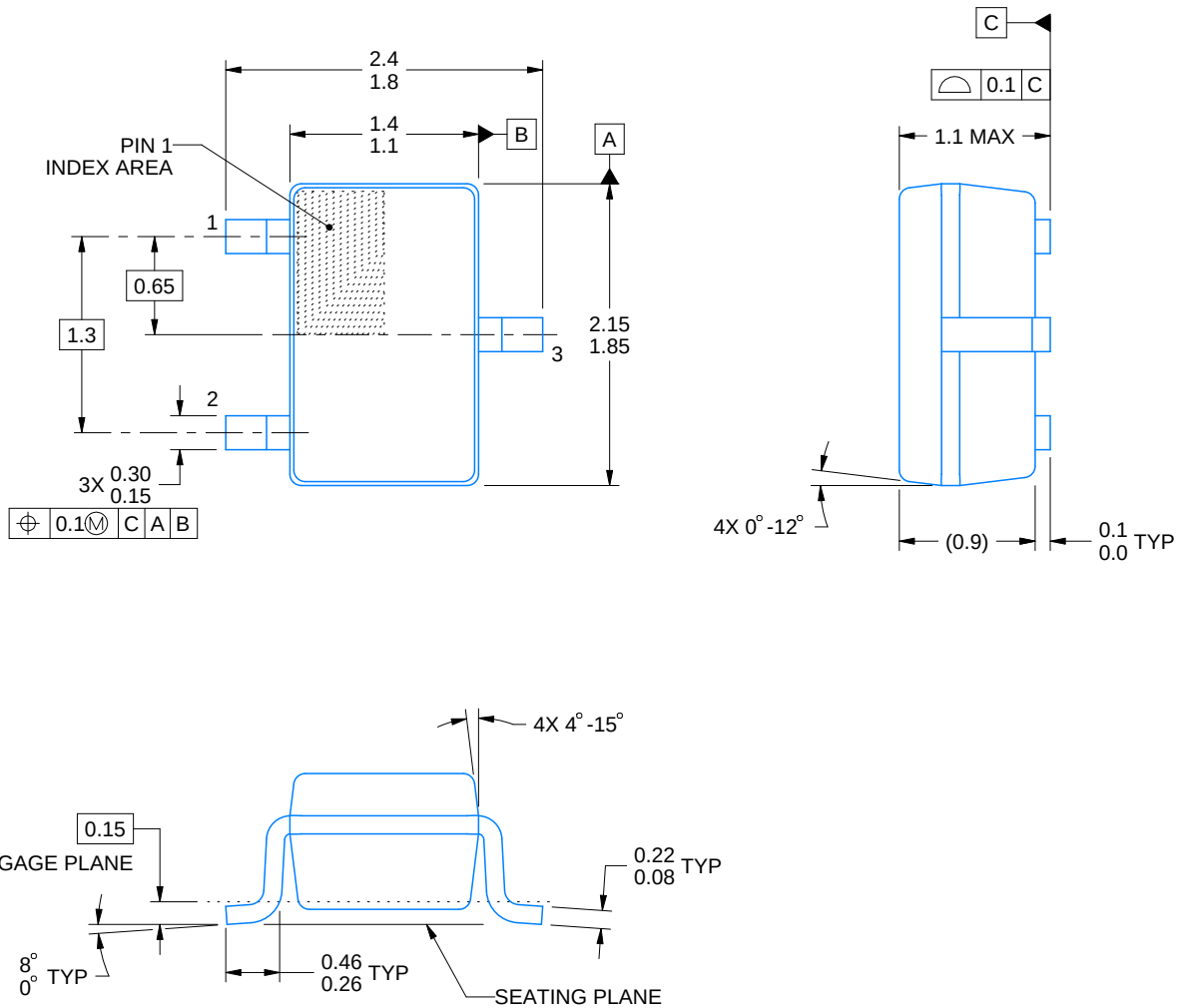
DCK0003A



PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



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NOTES:

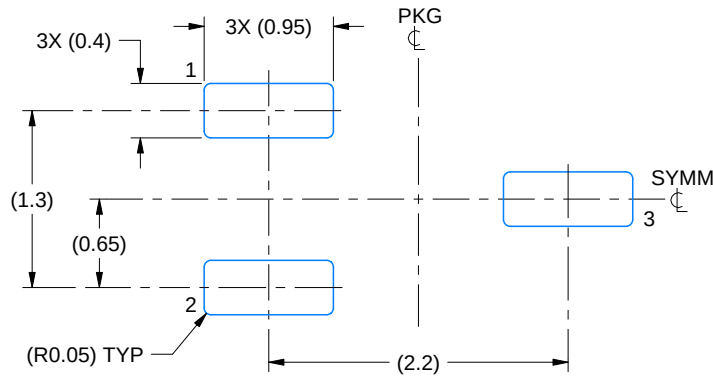
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

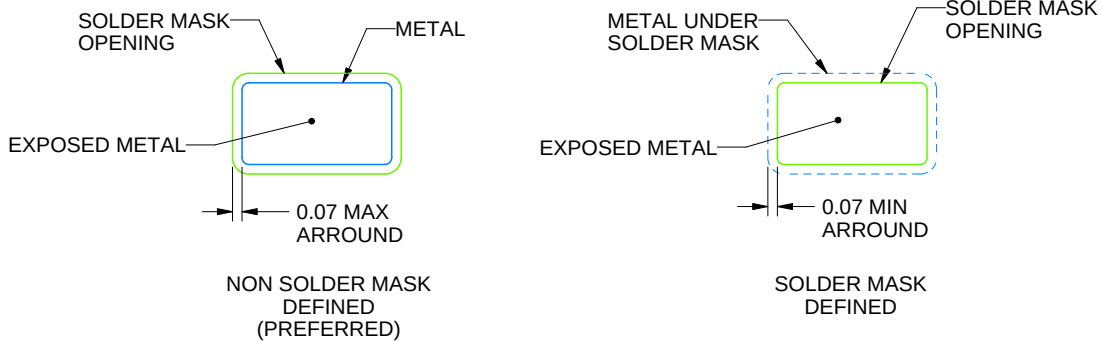
DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

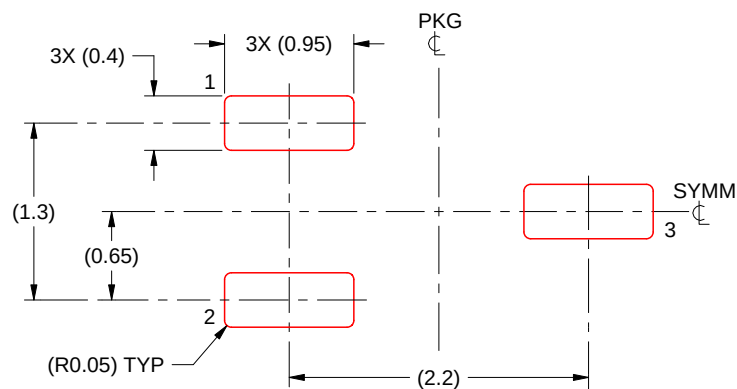
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70

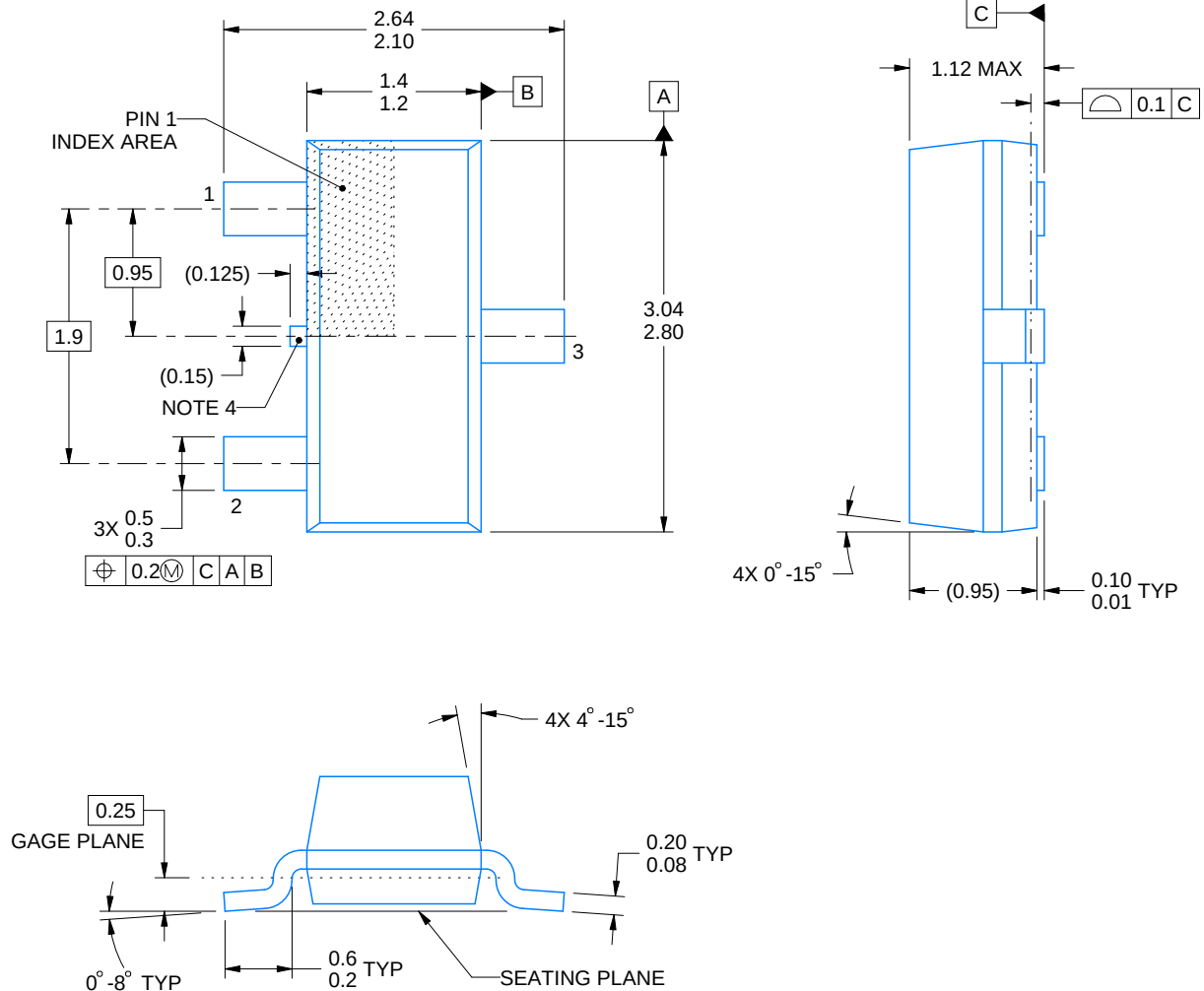


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



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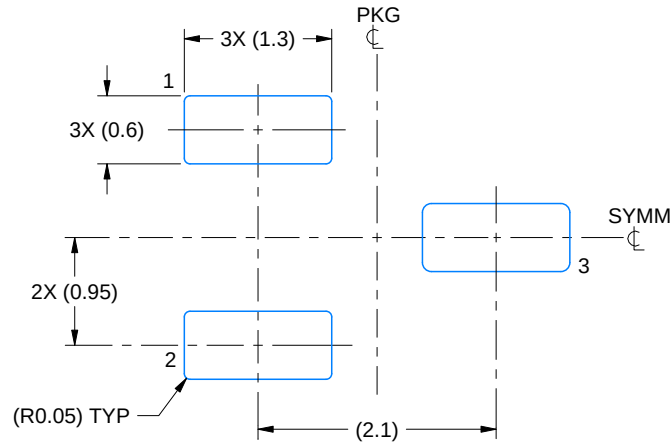
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

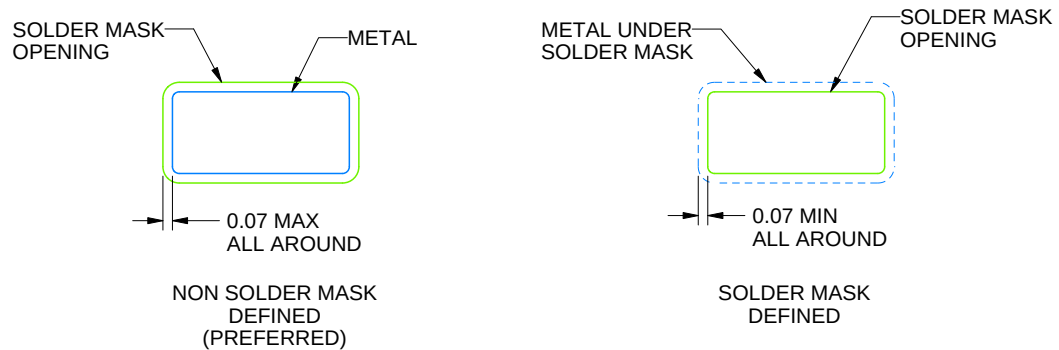
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

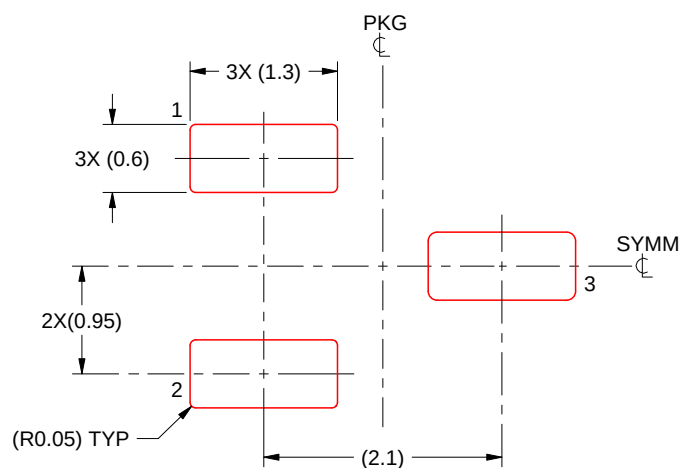
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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