

ESD2CANFD60-Q1 Automotive, 2-Channel, 60V, ESD Protection Diode for In-Vehicle Networks

1 Features

- Working voltage: 60V
- Bidirectional ESD protection
- Low clamping voltage protects downstream components
- Leaded packages to allow for automatic optical inspection (AOI)
- Low capacitance: 2pF (typical)
- AEC-Q101 qualified for automotive applications

2 Applications

- **Automotive in-vehicle networks:**
 - Controller area network (CAN)
 - Controlled area network flexible data-rate (CAN-FD)
 - Low, fault tolerant CAN
 - High-speed CAN

3 Description

The ESD2CANFD60-Q1 is a bidirectional, ESD protection diode for controller area network (CAN) interface protection. The ESD2CANFD60-Q1 is rated to dissipate contact ESD strikes specified in the ISO 10605 automotive standard. The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key, as automotive systems require a high level of robustness and reliability for safety applications.

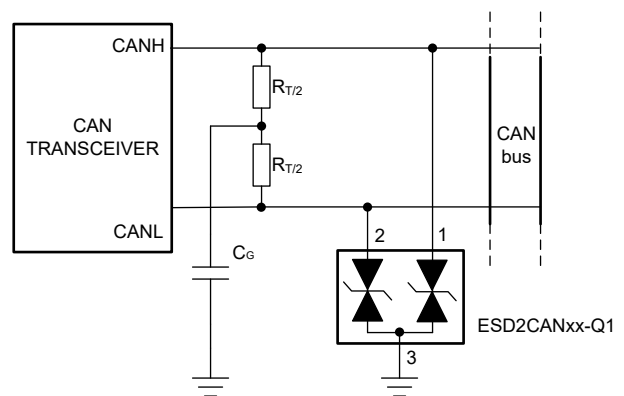
This device features a low IO capacitance per channel and a pinout designed for two automotive CAN bus lines (CANH and CANL) from the damage caused by electrostatic discharge (ESD) and other transients. Additionally, the 2pF (typical) line capacitance of the ESD2CANFD60-Q1 is an excellent choice for CAN, CAN-FD, and CAN SiC applications.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ESD2CANFD60-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For more information, see [Section 9](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



ESD2CANFD60-Q1 Typical Application

ADVANCE INFORMATION



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Pin Configuration and Functions

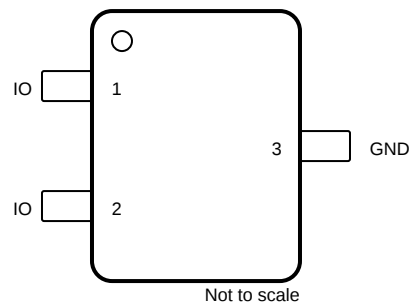


Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground

(1) I/O = Input or Output, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 μ s) at 25°C		500	W
	IEC 61000-4-5 current (t_p - 8/20 μ s) at 25°C		4	A
T_A	Operating free-air temperature	-55	150	°C
T_J	Junction temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001	± 2500	V
		Charged device model (CDM), per AEC Q101-005	± 1000	

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	± 25000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	± 25000	

5.4 ESD Ratings - ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605, C = 150 pF, R = 330 Ω	Contact discharge	± 25000	V
			Air-gap discharge	± 25000	
		ISO 10605, C = 330 pF, R = 330 Ω	Contact discharge	± 24000	
			Air-gap discharge	± 24000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-60		60	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Electrical Characteristics

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	Both Positive and Negative			60	V
V _{BR}	Breakdown voltage	I _{IO} = ±10mA, IO to GND, Both Positive and Negative	63			V
I _{LEAK}	Leakage current, any IO pin to GND	V _{IO} = ±60V, Both Positive and Negative		2	50	nA

5.6 Electrical Characteristics (continued)

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLAMP}	Clamping voltage ⁽¹⁾	$I_{\text{PP}} = 1\text{A}$, $t_p = 8/20\mu\text{s}$, from IO to GND		71		V
V_{CLAMP}	Clamping voltage ⁽¹⁾	$I_{\text{PP}} = 4\text{A}$, $t_p = 8/20\mu\text{s}$, from IO to GND		85		V
V_{CLAMP}	Clamping voltage ⁽²⁾	$I_{\text{PP}} = 16\text{A}$, TLP, from IO to GND		92		V
R_{DYN}	Dynamic resistance ⁽²⁾	IO to GND and GND to IO		0.75		Ω
C_L	Line capacitance, any IO to GND	$V_{\text{IO}} = 0\text{V}$, $f = 1\text{MHz}$, $V_{p-p} = 30\text{mV}$		2		pF

(1) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

(2) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD2CANFD60-Q1 is a dual-channel, TVS diode that provides a path to ground for dissipating ESD events on differential CAN signal lines. The CAN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This voltage is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide application note](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Datasheet user's guide](#)

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

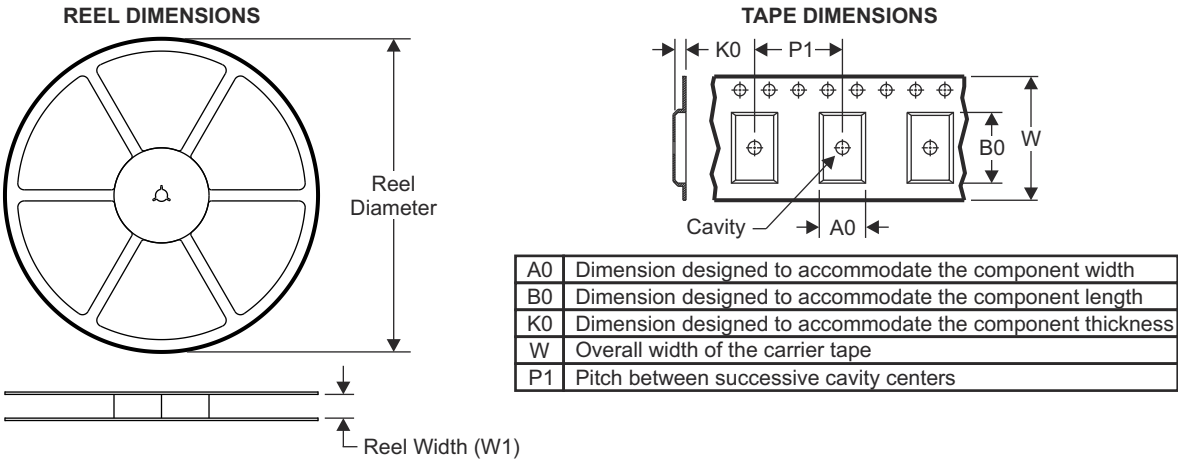
8 Revision History

DATE	REVISION	NOTES
August 2026	*	Initial Release

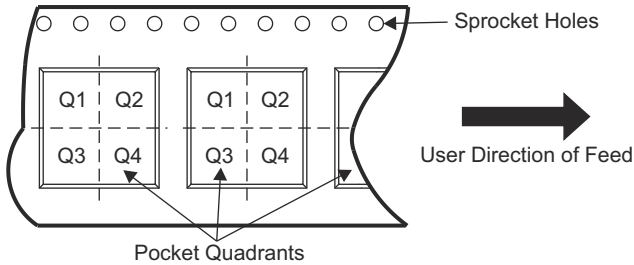
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

9.1 Tape and Reel Information

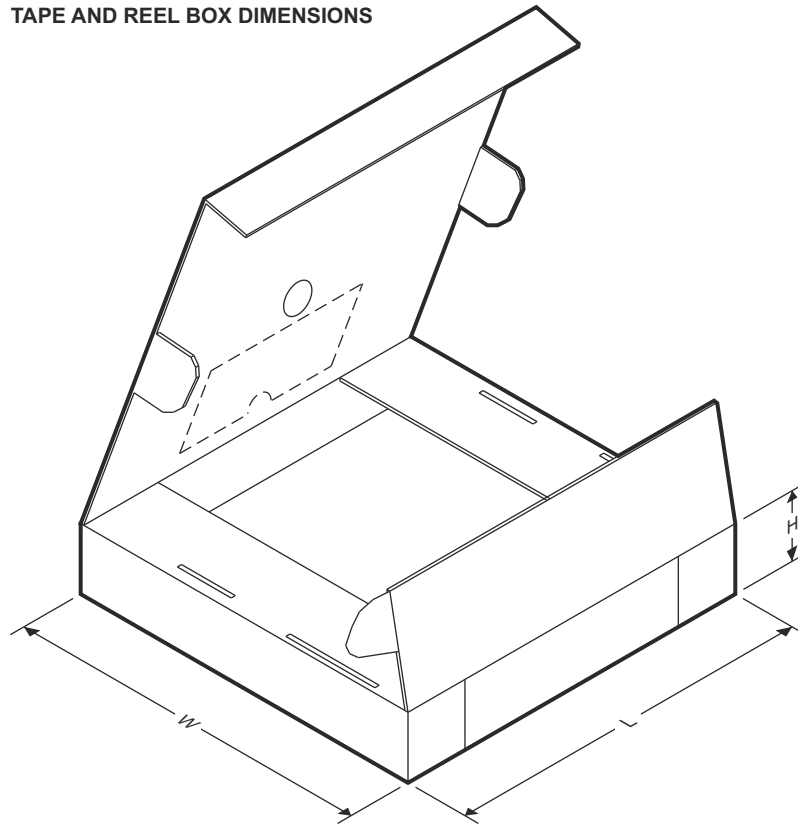


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CANFD60DBZR Q1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

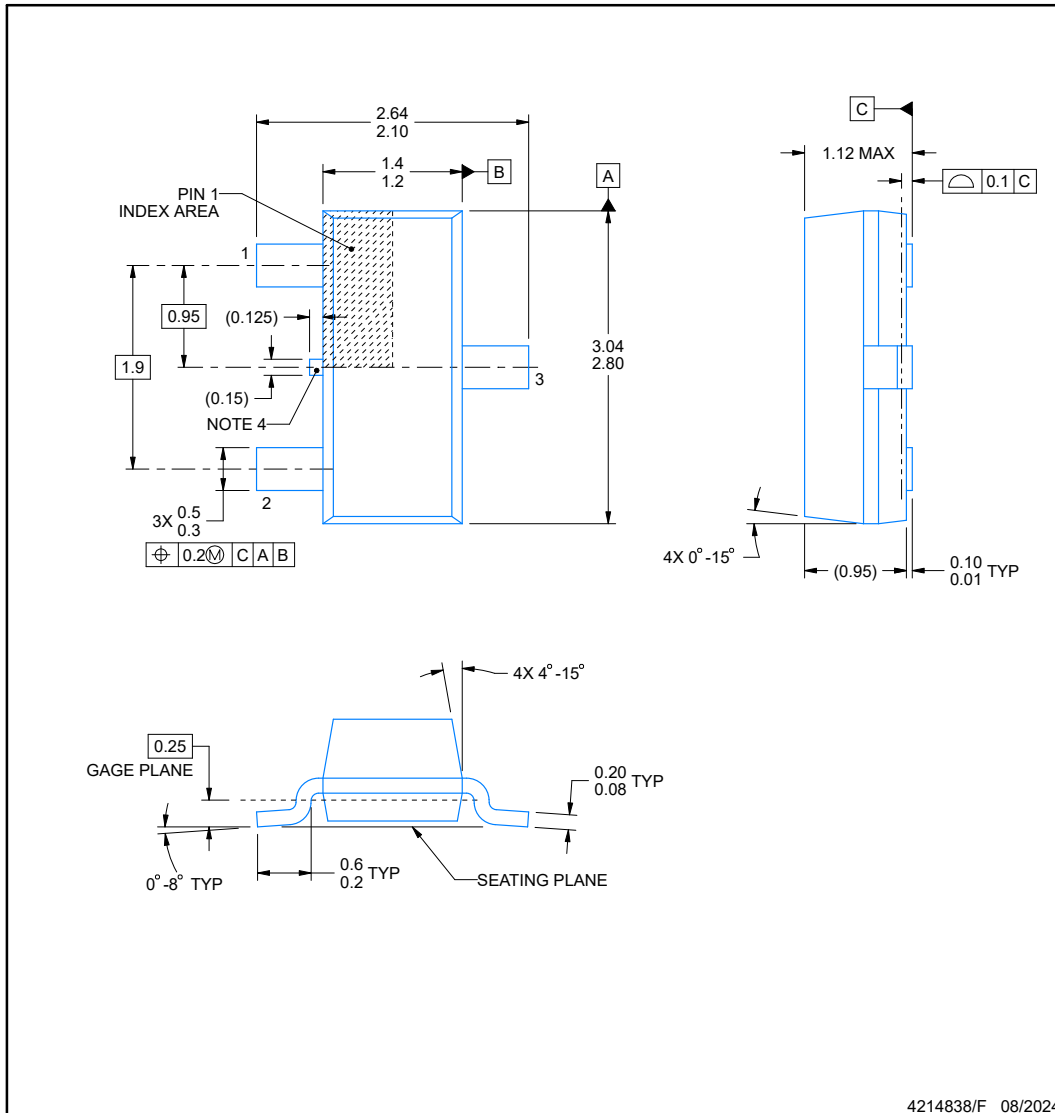


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CANFD60DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

9.2 Mechanical Data

ADVANCE INFORMATION

DBZ0003A **PACKAGE OUTLINE**
SOT-23 - 1.12 mm max height
SMALL OUTLINE TRANSISTOR



NOTES:

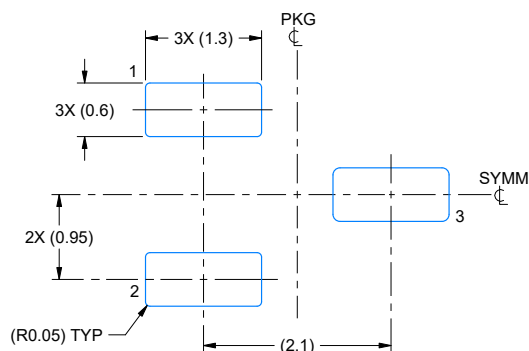
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side.

EXAMPLE BOARD LAYOUT

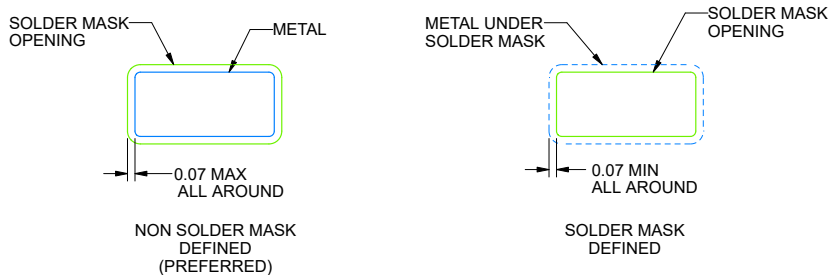
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

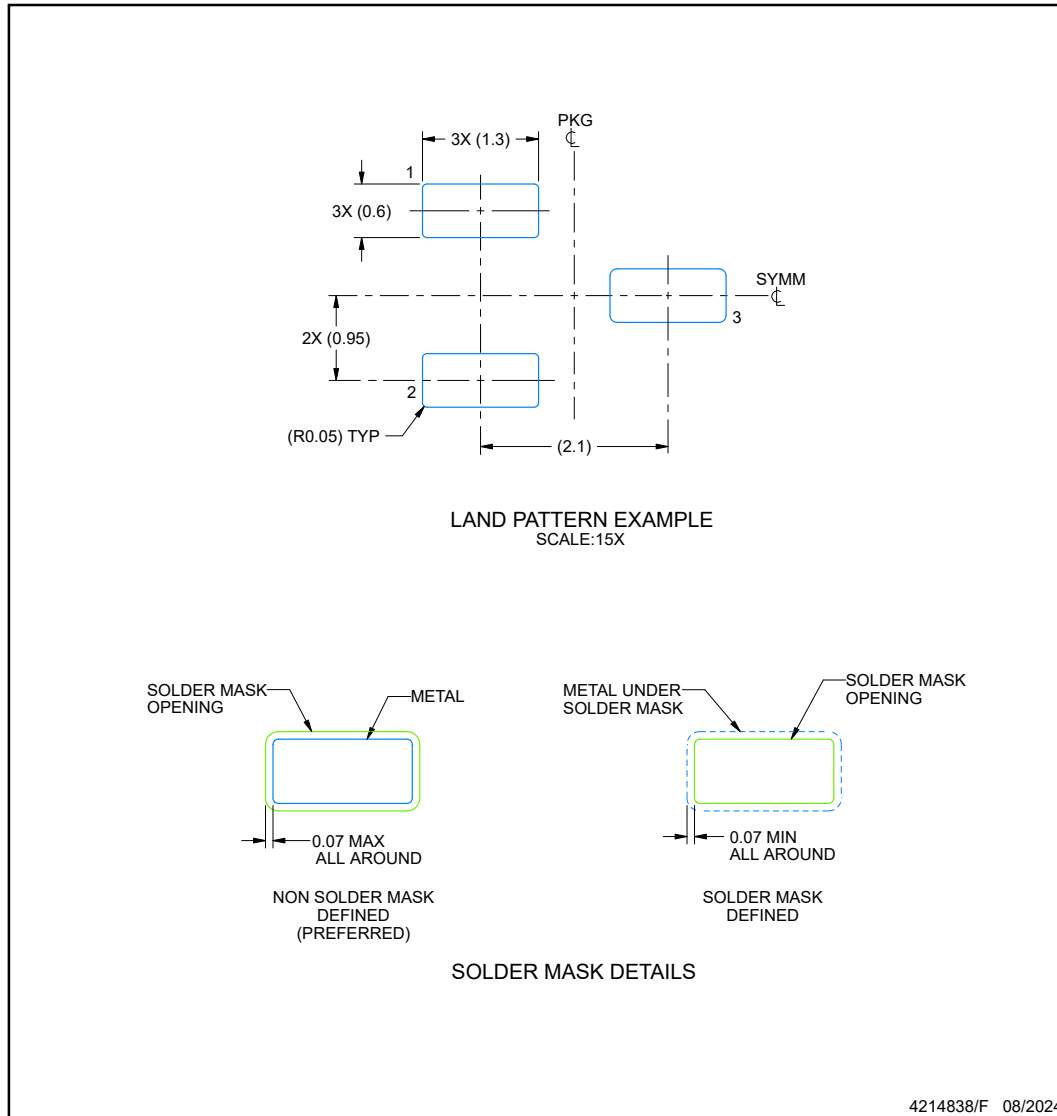
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PESD2CANFD60DBZRQ1	Active	Preproduction	SOT-23 (DBZ) 3	3000 LARGE T&R	-	Call TI	Call TI	-55 to 150	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

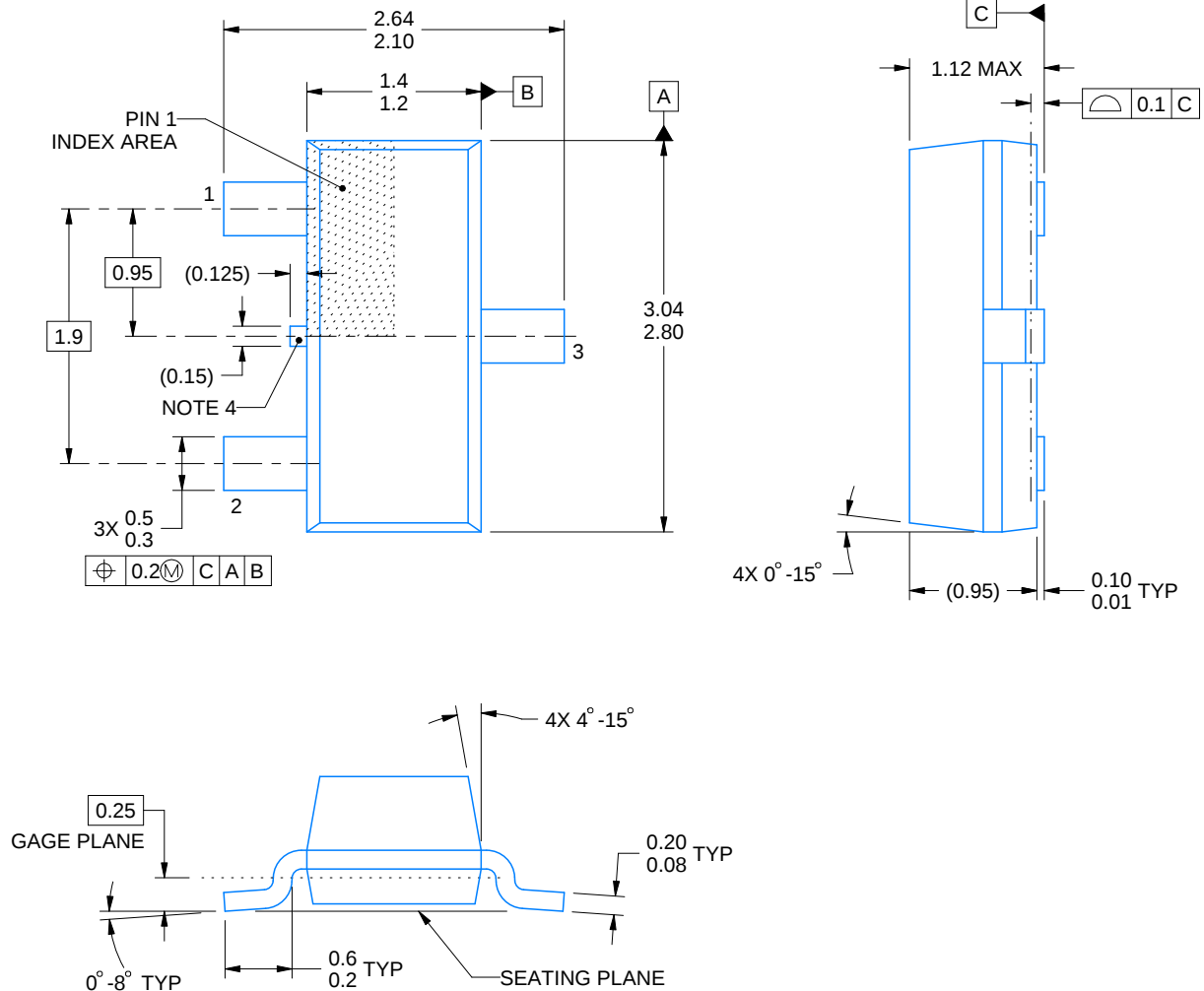
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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DBZ0003A**PACKAGE OUTLINE****SOT-23 - 1.12 mm max height**

SMALL OUTLINE TRANSISTOR



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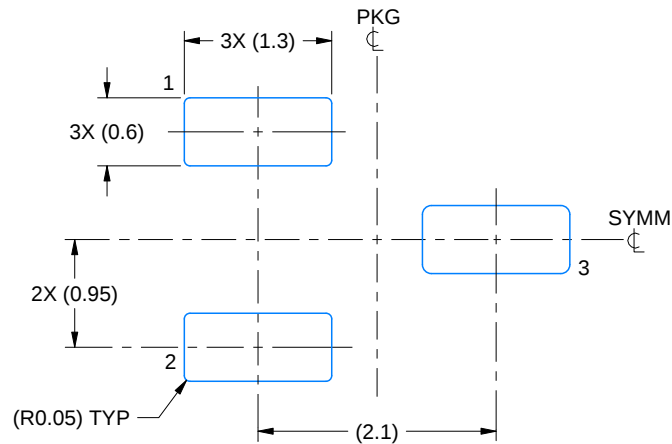
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

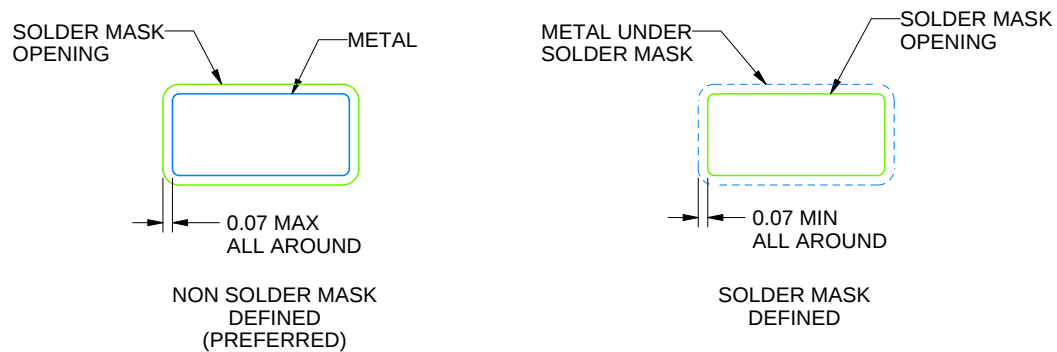
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

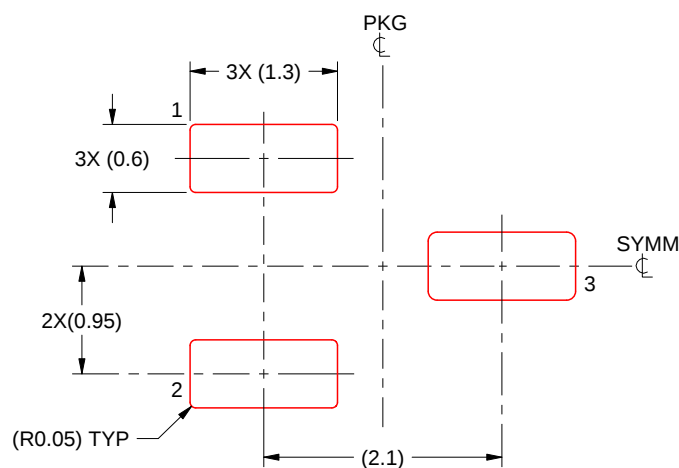
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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