ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 Automotive 24V, 1-Channel ESD Protection Diodes for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±30kV, ±22kV or ±15kV contact discharge
  - ±30kV, ±22kV or ±15kV air-gap discharge
- ISO 10605 (330pF, 330Ω) ESD protection:
  - ±25kV, ±20kV or ±12kV contact discharge
  - ±25kV, ±20kV or ±12kV air-gap discharge
- 24V working voltage
- Bidirectional ESD protection
- Low clamping voltage protects downstream components
- AEC-Q101 qualified
- Temperature range: –55°C to +150°C
- I/O capacitance = 2.3pF, 1.6pF, or 1.1pF (typical)
- Offered in industry standard packages: SOD-323 (DYF), SOD-523 (DYA), and 0402 size leadless package (DPY)
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- Automotive in-vehicle networks:
  - Local interconnect network (LIN)
  - Single line CAN ESD protection
- Industrial control networks:
  - DeviceNet
  - Smart distribution systems

3 Description

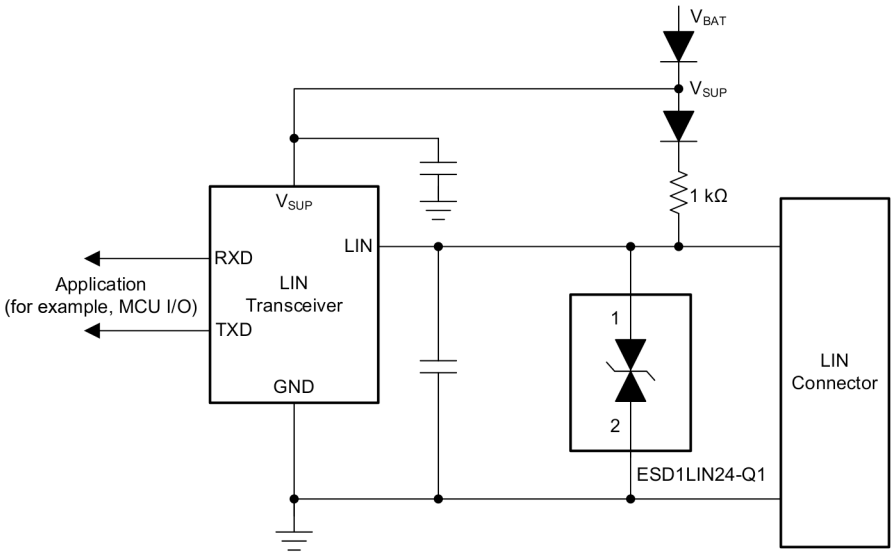
The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single-channel low capacitance bidirectional ESD protection devices for local interconnect network (LIN). These devices are rated to dissipate contact ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard (±30kV Contact, ±30kV Airgap), (±22kV Contact, ±22kV Airgap), and (±15kV Contact, ±15kV Airgap), respectively. The low dynamic resistance and low clamping voltage help protect systems against transient events. This protection is key as automotive systems require a high level of robustness and reliability when they control safety devices.

The ESD1LIN24-Q1 and ESD751-Q1 are both offered in leaded packages for easy flow through routing.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
ESD1LIN24-Q1	DYF (SOD-323, 2)	1.70mm × 1.30mm
ESD751-Q1	DYA (SOD-523, 2)	1.60mm × 0.80mm
ESD761-Q1	DPY (X1SON, 2)	1.00mm × 0.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Pin Configuration and Functions

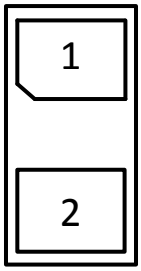


Figure 4-1. DPY Package, 2-Pin X1SON (Top View)

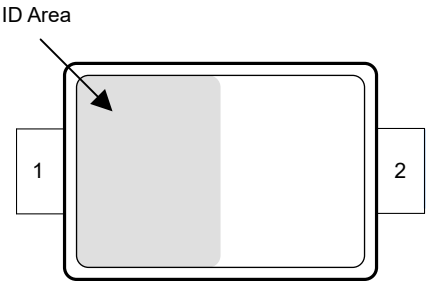


Figure 4-2. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C	ESD1LIN24-Q1		159	W
		ESD751-Q1		102	
		ESD761-Q1		65	
I_{PP}	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C	ESD1LIN24-Q1		4.3	A
		ESD751-Q1		2.8	
		ESD761-Q1		1.8	
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001(1)	± 2500	V
		Charged device model (CDM), per AEC Q101-005	± 1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings—IEC Specification

			DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD1LIN24-Q1	±30000	V
			ESD751-Q1	±22000	
			ESD761-Q1	±15000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD1LIN24-Q1	±30000	
			ESD751-Q1	±22000	
			ESD761-Q1	±15000	

5.4 ESD Ratings - ISO Specification

				DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge	ISO 10605, 150pF, 330Ω, IO	ESD1LIN24-Q1	± 30000	V
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	
			ISO 10605, 330pF, 330Ω, IO	ESD1LIN24-Q1	± 25000	
				ESD751-Q1	± 20000	
				ESD761-Q1	± 12000	
		Air-gap discharge	ISO 10605, 150pF, 330Ω, IO	ESD1LIN24-Q1	± 30000	
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	
			ISO 10605, 330pF, 330Ω, IO	ESD1LIN24-Q1	± 25000	
				ESD751-Q1	± 20000	
				ESD761-Q1	± 12000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC(1)		ESD1LIN24-Q1	ESD751-Q1	ESD761-Q1	UNIT
		DYF (SOD-323)	DYA (SOD-523)	DPY (X1SON)	
		2 PINS	2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	705.4	746.3	282.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	315	301.2	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	561.5	509.6	98.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	145	81.8	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	550.2	503.0	97.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.7 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–24		24	V
V_{BRF}	Breakdown voltage(1)	I_{IO} = 10mA, IO to GND		25.5		35.5	V
V_{BRR}	Breakdown voltage(1)	I_{IO} = –10mA, IO to GND		–35.5		–25.5	V
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 4.3A, t_p = 8/20µs, IO to GND and GND to IO	ESD1LIN24-Q1		37		V
		I_{PP} = 2.8A, t_p = 8/20µs, IO to GND and GND to IO	ESD751-Q1		36.5		
		I_{PP} = 1.8A, t_p = 8/20µs, IO to GND and GND to IO	ESD761-Q1		36.3		
V_{CLAMP}	Clamping voltage(3)	I_{PP} = 16A, TLP, IO to GND and GND to IO	ESD1LIN24-Q1		40		V
			ESD751-Q1		41.5		
			ESD761-Q1		42.5		V
I_{LEAK}	Leakage current	V_{IO} = ±24V, IO to GND		-50	1	50	nA
R_{DYN}	Dynamic resistance(3)		ESD1LIN24-Q1		0.5		Ω
			ESD751-Q1		0.6		
			ESD761-Q1		0.53		
C_L	Line capacitance	V_{IO} = 0V, f = 1MHz, V_{pp} = 30mV, IO to GND	ESD1LIN24-Q1		2.3	3.8	pF
			ESD751-Q1		1.6	2.7	
			ESD761-Q1		1.1	1.8	

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5.8 Typical Characteristics – ESD751

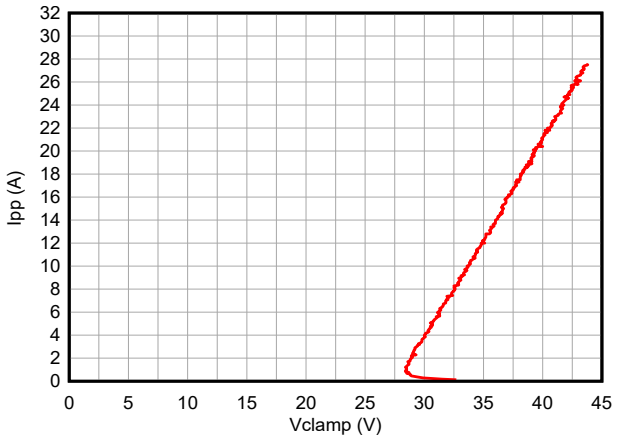


Figure 5-1. Positive TLP Curve

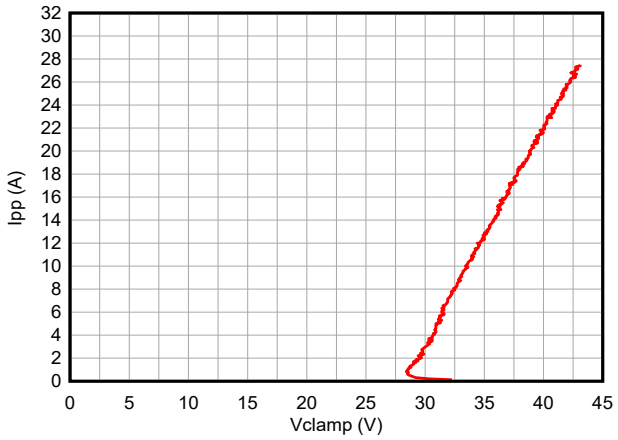


Figure 5-2. Negative TLP Curve

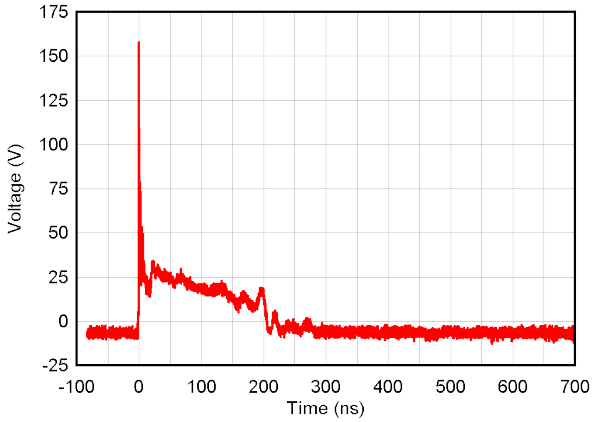


Figure 5-3. +8-kV Clamped IEC Waveform

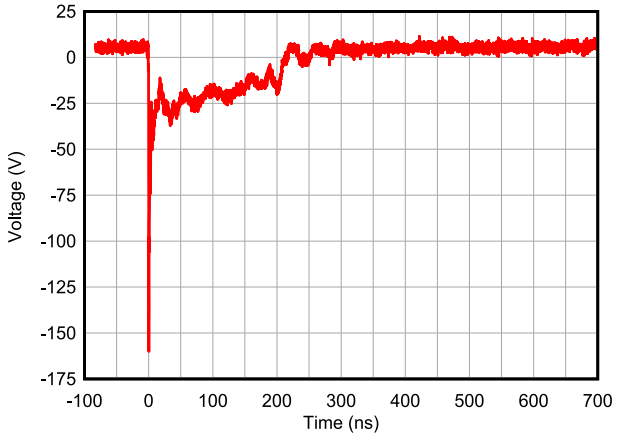


Figure 5-4. -8-kV Clamped IEC Waveform

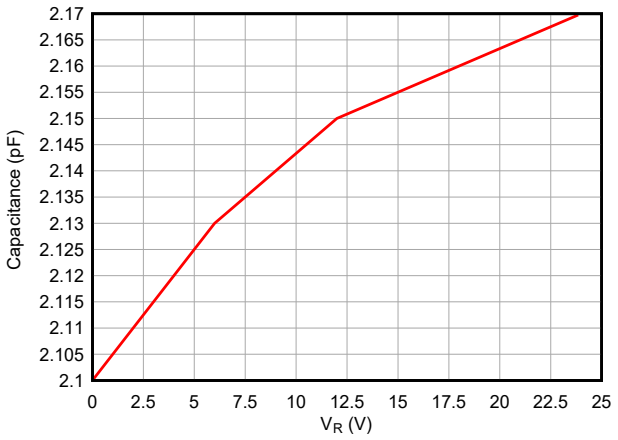


Figure 5-5. Capacitance vs. Bias Voltage

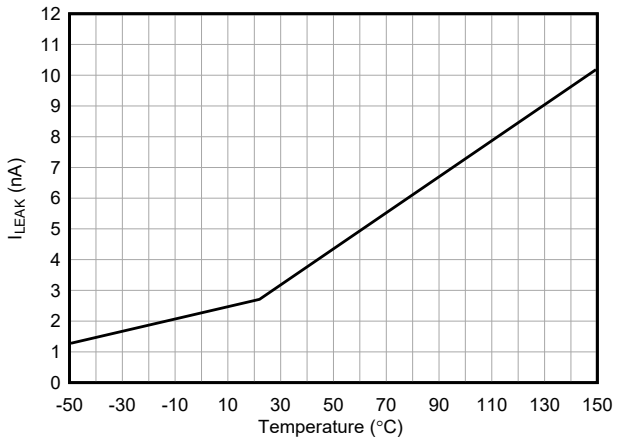


Figure 5-6. Leakage Current vs. Temperature

5.9 Typical Characteristics – ESD1LIN24

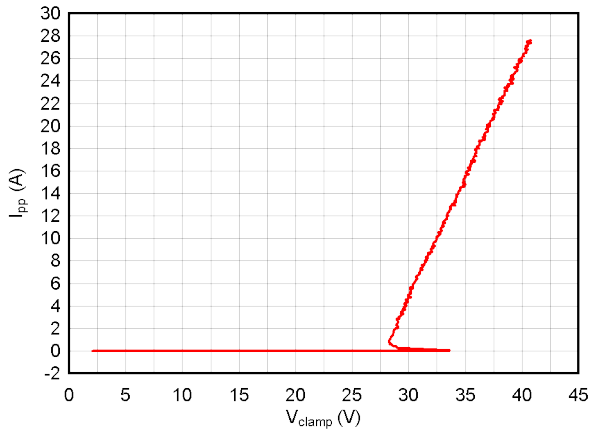


Figure 5-7. Positive TLP Curve

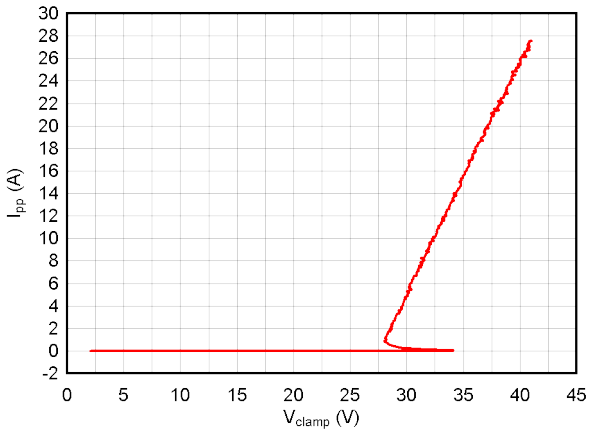


Figure 5-8. Negative TLP Curve

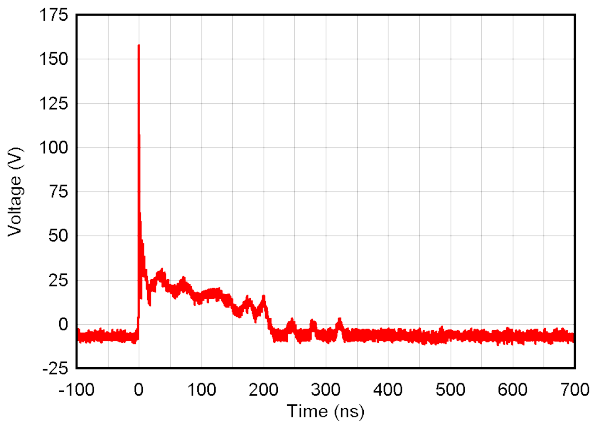


Figure 5-9. +8kV Clamped IEC Waveform

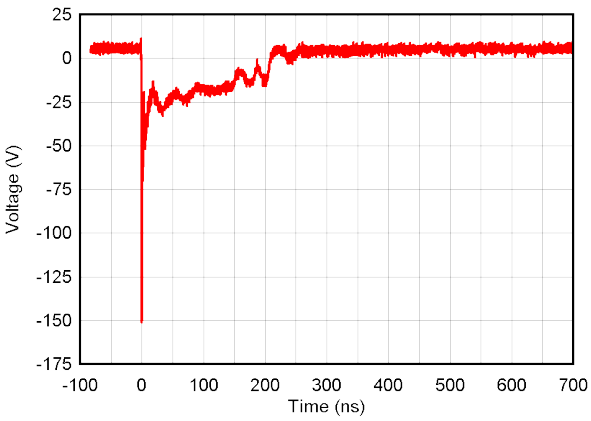


Figure 5-10. −8kV Clamped IEC Waveform

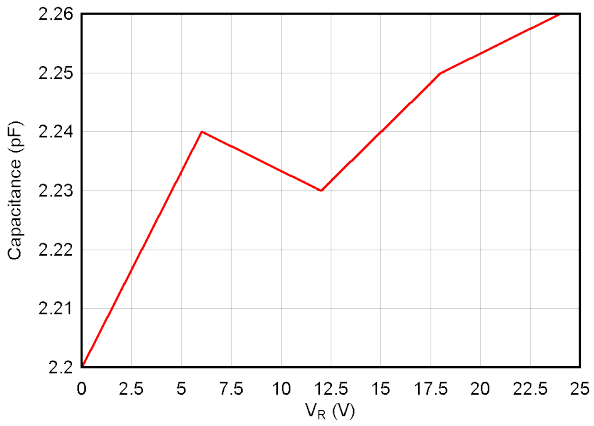


Figure 5-11. Capacitance vs. Bias Voltage

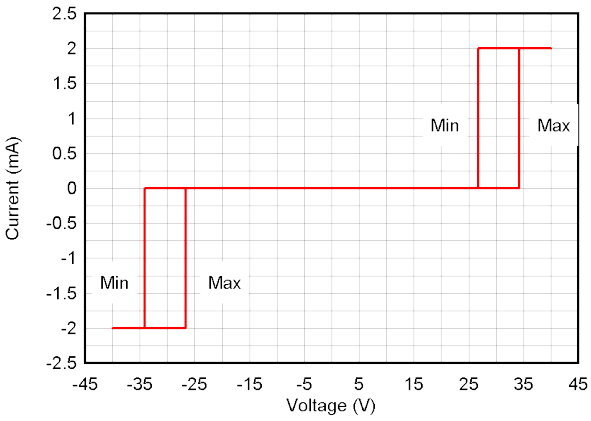


Figure 5-12. DC Voltage Sweep I-V Curve

5.10 Typical Characteristics - ESD761

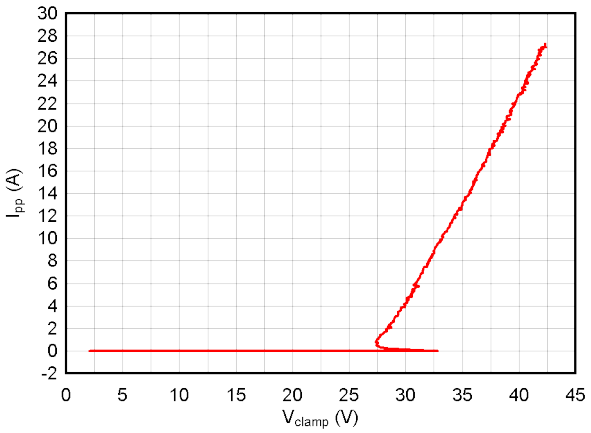


Figure 5-13. Positive TLP Curve

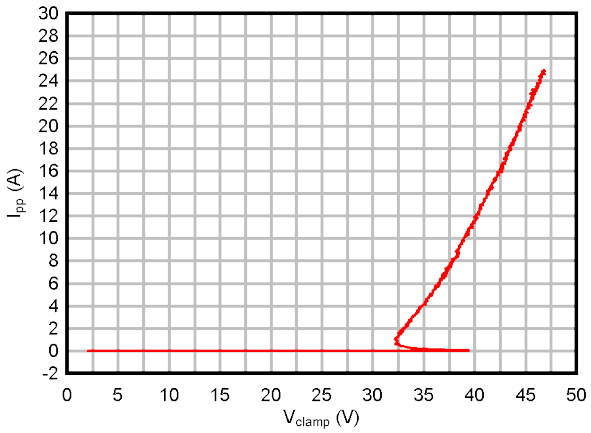


Figure 5-14. Negative TLP Curve

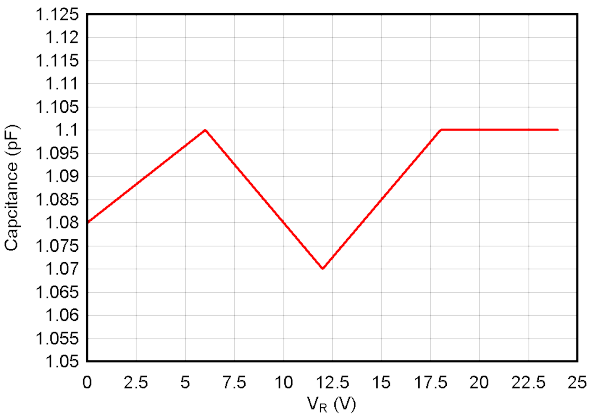


Figure 5-15. Capacitance vs. Bias Voltage

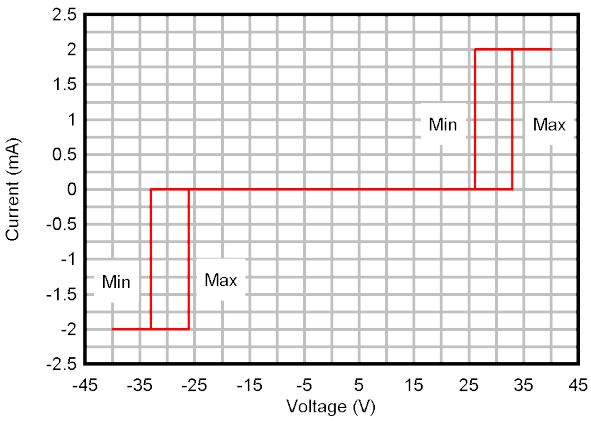


Figure 5-16. DC Voltage Sweep I-V Curve

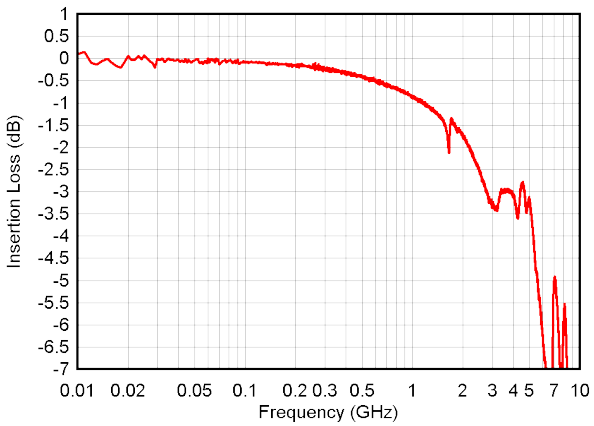


Figure 5-17. Insertion Loss

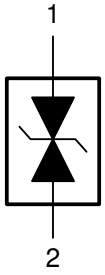
6 Detailed Description

6.1 Overview

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single-channel ESD diodes available in industry standard packages (SOD-323 and SOD-523) which are convenient for automatic optical inspection as well as a smaller leadless package X1SON (DPY). These products offer ISO 10605 ESD ratings of (±25kV Contact, ±25kV Airgap), (±20kV Contact, ±20kV Airgap), and (±12kV Contact, ±12kV Airgap), respectively. The 2.3pF, 1.6pF, and 1.1pF line capacitance of these ESD protection diodes are suitable for LIN applications that support data rates from 20Kbps to 10Mbps.

Typical application of these products is the ESD circuit protection for LIN transceivers used in automotive applications. These devices are commonly used for ESD protection inside automotive electronic control units (ECUs) for head lights, door modules, climate control, roof control, wipers, cluster, audio, and many other automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single-channel bidirectional ESD diodes with a high ESD protection level. These devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. The breakdown is bidirectional so these protection devices can prevent system damage if battery leads are swapped. Low leakage allows the diodes to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes these ESD devices work at extensive temperatures in most environments.

6.3.1 IEC 61000-4-5 Surge Protection

The I/O pins of the ESD1LIN24-Q1, ESD751-Q1, ESD761-Q1 have the following surge ratings (8/20 µs waveform): 4.3A, 2.8A, and 1.8A, respectively. An ESD-surge clamp diverts this current to ground.

6.3.2 IO Capacitance

The capacitance between the I/O pins of the ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 devices are as follows: 2.3pF, 1.6pF, and 1.1pF, respectively. The capacitance of these devices support data rates for LIN up to 10Mbps.

6.3.3 Dynamic Resistance

The I/O pins feature an ESD clamp that have a low R_{DYN} of 0.48Ω for the ESD1LIN24-Q1, 0.6Ω for the ESD751-Q1, and 0.58Ω for the ESD761-Q1.

6.3.4 DC Breakdown Voltage

The DC breakdown voltage between the I/O pins is a minimum of ± 25.5V. This shields sensitive equipment from surges above the reverse standoff voltage of ± 24V.

6.3.5 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 50nA (maximum) with a bias of ± 24V.

6.3.6 Clamping Voltage

The I/O pins of the ESD1LIN24-Q1 feature an ESD clamp that is capable of clamping the voltage to 37V (I_{PP} = 4.3A) and 37.7V (I_{PP} = 16A for TLP). The I/O pins of the ESD751-Q1 feature an ESD clamp that is capable of clamping the voltage to 36.5V (I_{PP} = 2.8A) and 39.7V (I_{PP} = 16A for TLP). The I/O pins of the ESD761-Q1 feature an ESD clamp that is capable of clamping the voltage to 36.3V (I_{PP} = 1.8A) and 39.3V (I_{PP} = 16A for TLP).

6.3.7 Industry Standard Packages

The ESD1LIN24-Q1 and ESD751-Q1 feature industry standard SOD-323 (DYF) and SOD-523 (DYA) leaded packages for automatic optical inspection (AOI). The ESD761-Q1 is offered in the leadless X1SON (DPY) package

6.4 Device Functional Modes

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single channel passive clamps that have low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. During ISO 10605 ESD events, transient voltages from ±25kV to ±12kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single channel TVS diodes which are used to provide a path to ground for dissipating ESD events on LIN signal lines. The LIN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

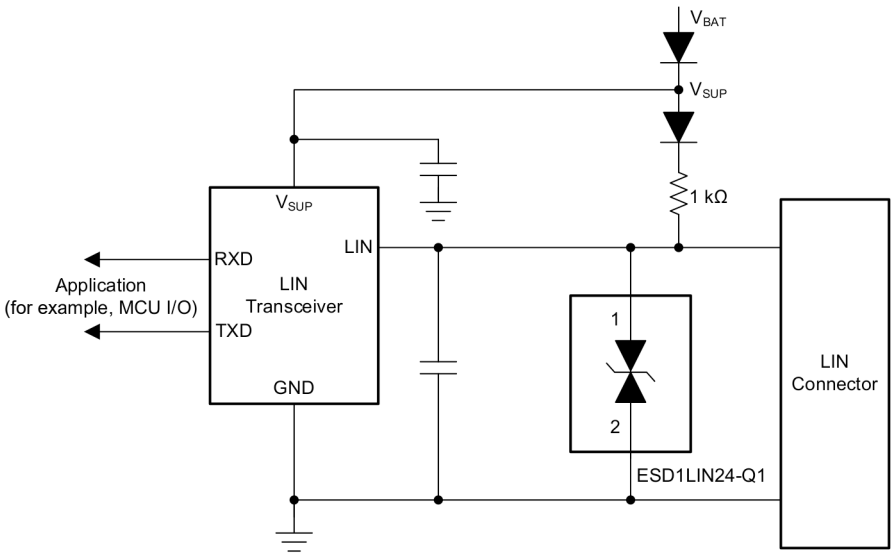


Figure 7-1. Typical Application

7.2.1 Design Requirements

For this design example, the ESD1LIN24-Q1 is used to provide ESD protection to a LIN transceiver. The parameters listed in Table 7-1 are the known design parameters for this application.

Table 7-1. Design Parameters for Typical Applications

DESIGN PARAMETERS	VALUE
Diode configuration	Bidirectional
V_{IO} signal range	Up to 18V
V_{RWM}	±24V
Jumpstart short to battery event on V_{IO}	±2V
Data rate	Up to 10Mbps
Pullup resistor	1kΩ

7.2.2 Detailed Design Procedure

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 have a V_{RWM} of ±24V to protect the diode from being damaged during a short to battery event that can occur by reversing the terminal connections during jumpstart. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 5pF or less permits data rates up to 10Mbps, which allows the designer to meet the requirements for LIN. The 1kΩ and VSUP diode allows the LIN signal to be pulled up to a diode drop below the battery voltage.

7.2.3 Application Curves

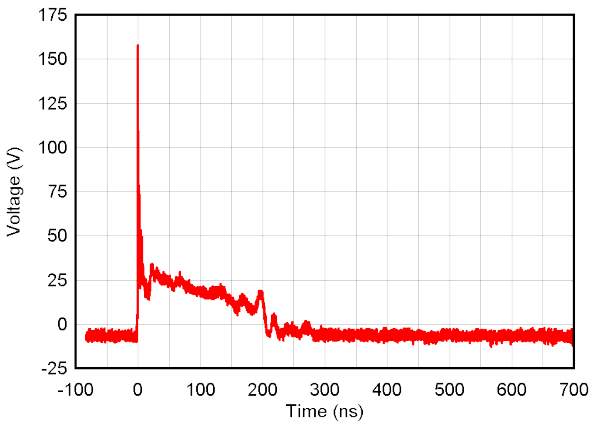


Figure 7-2. +8kV Clamped IEC Waveform

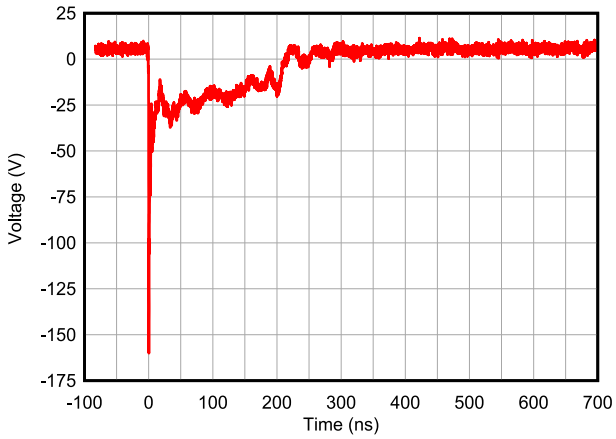


Figure 7-3. −8kV Clamped IEC Waveform

8 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin is not violated.

9 Layout

9.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

9.2 Layout Example

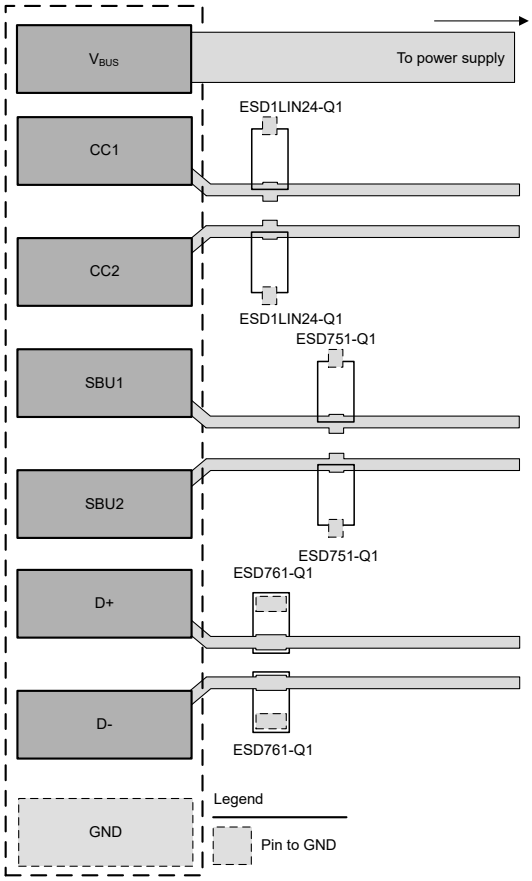


Figure 9-1. Layout Recommendation

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2022) to Revision D (October 2025)	Page
• Updated ISO 330pF/330Ω spec from 30kV to 25kV for ESD1LIN24-Q1	1
• Updated ISO 330pF/330Ω spec from 22kV to 20kV for ESD751-Q1	1
• Updated ISO 330pF/330Ω spec from 15kV to 12kV for ESD761-Q1	1
• Added MSL 1 to ESD1LIN24DYFRQ1	17

Changes from Revision B (November 2022) to Revision C (December 2022)	Page
• Changed the status of the ESD1LIN24-Q1 and ESD761-Q1 device from: *Advanced Information* to: *Production Data*	1
• Updated the Thermal Specifications and Clamping Voltages in the *Thermal Information* and *Electrical Characteristics* table	4

Changes from Revision A (September 2022) to Revision B (November 2022)	Page
• Changed the status of the ESD751-Q1 device from: *Advanced Information* to: *Production Data*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

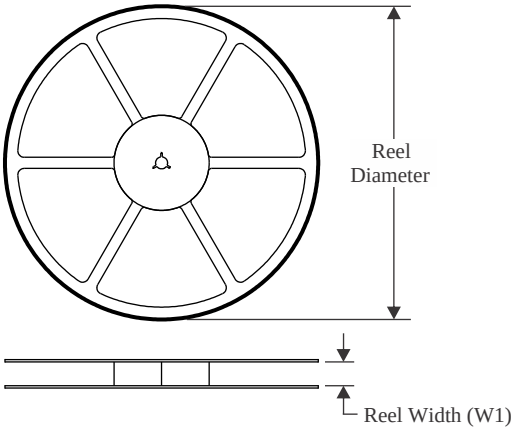
PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

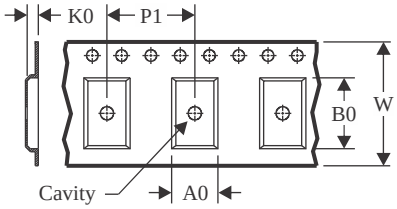
Orderable part number	Status	Material type	Package | Pins	Package qty | Carrier	RoHS	Lead finish/Ball material	MSL rating/Peak reflow	Op temp (°C)	Part marking
ESD1LIN24DYFRQ1	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM,	-55 to 150	1VA
ESD1LIN24DYFRQ1.B	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	1VA
ESD1LIN24DYFRQ1	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	2QKF
ESD1LIN24DYFRQ1.B	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	2QKF
ESD751DYARQ1	Active	Production	SOT-5X3 (DYA) | 2	8000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1MO
ESD751DYARQ1.B	Active	Production	SOT-5X3 (DYA) | 2	8000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1MO
ESD761DPYRQ1	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	NF
ESD761DPYRQ1.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	NF

TAPE AND REEL INFORMATION

REEL DIMENSIONS

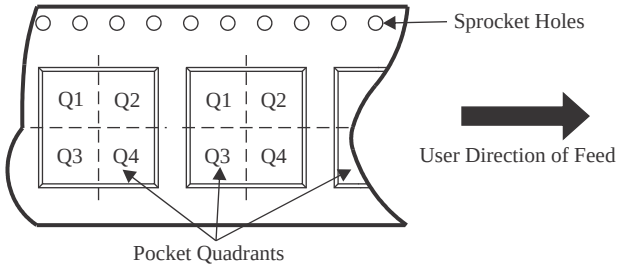


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

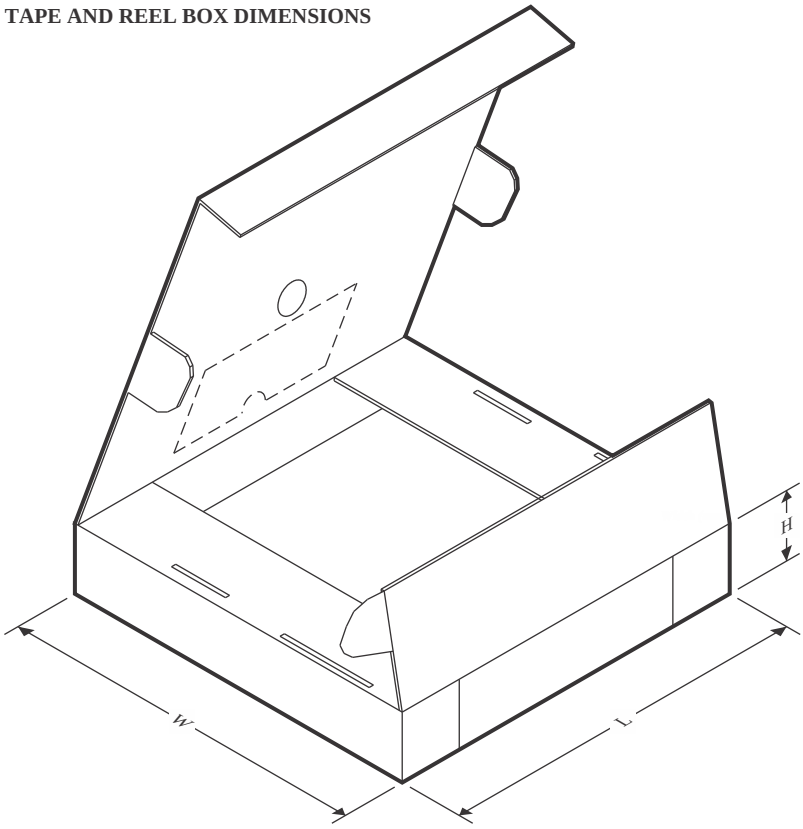
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD1LIN24DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
ESD751DYARQ1	SOT-5X3	DYA	2	8000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
ESD761DPYRQ1	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD1LIN24DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
ESD751DYARQ1	SOT-5X3	DYA	2	8000	210.0	200.0	42.0
ESD761DPYRQ1	X1SON	DPY	2	10000	205.0	200.0	33.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

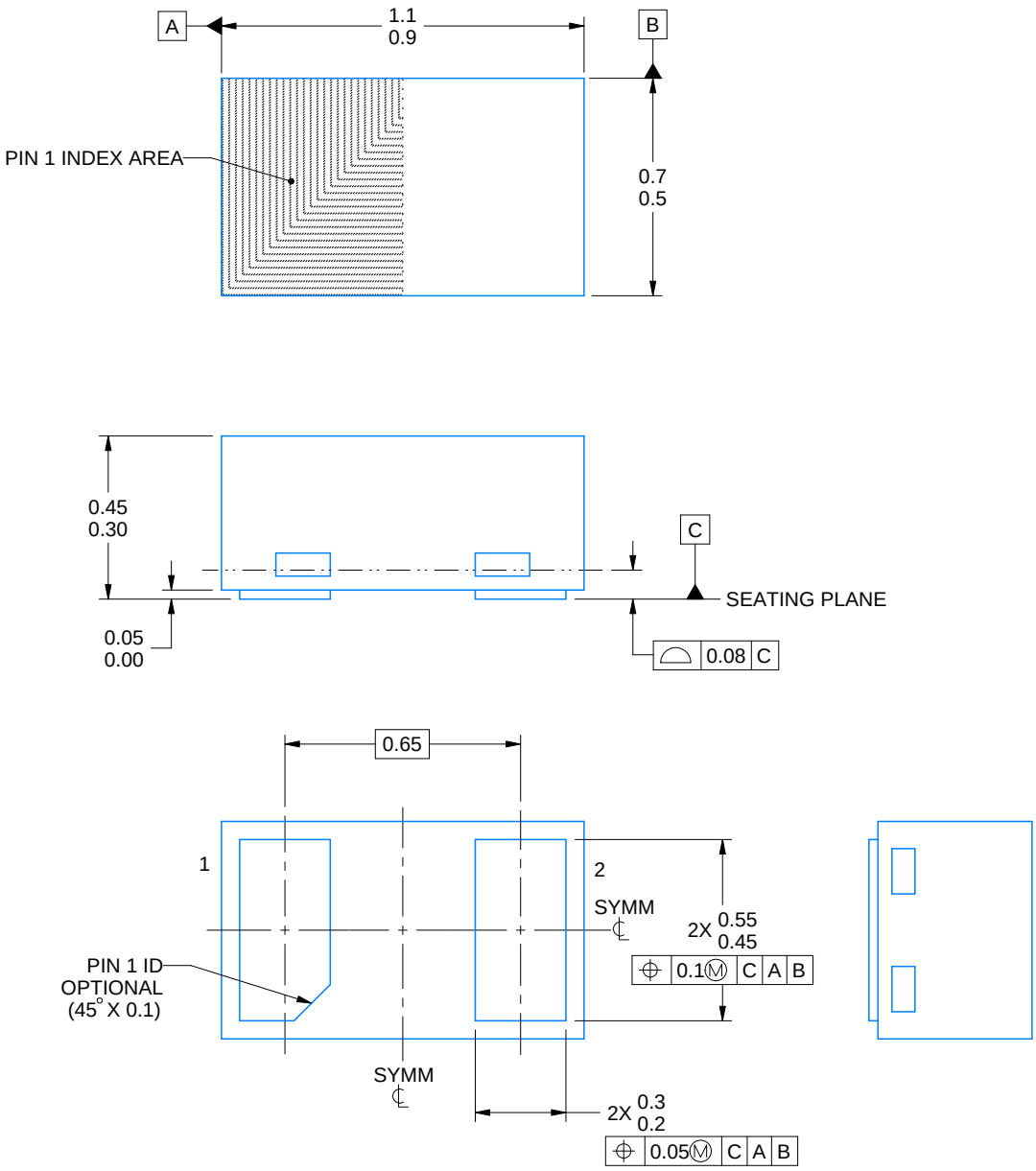
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

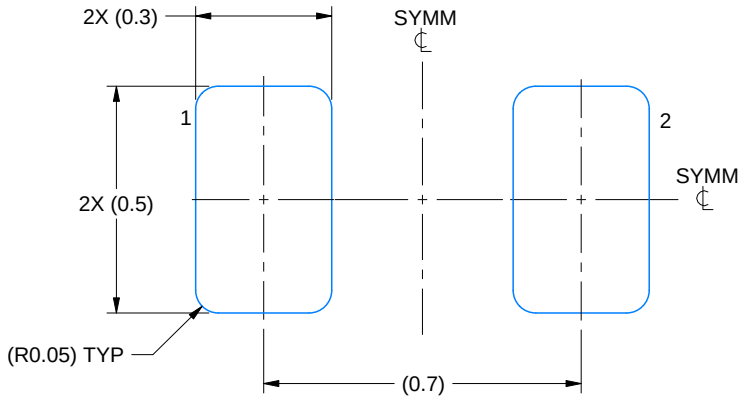
PLASTIC SMALL OUTLINE - NO LEAD



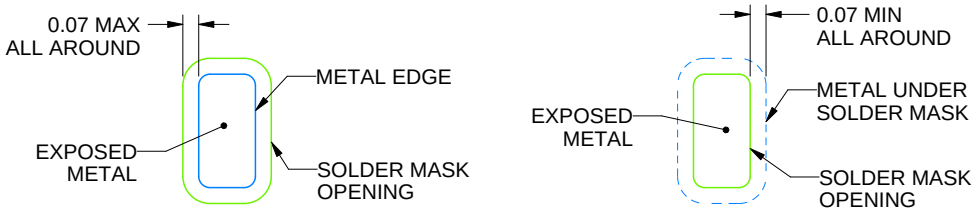
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

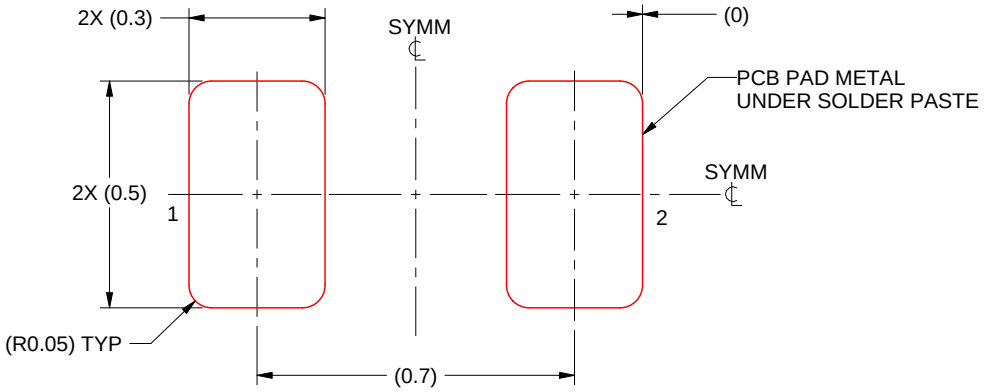


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

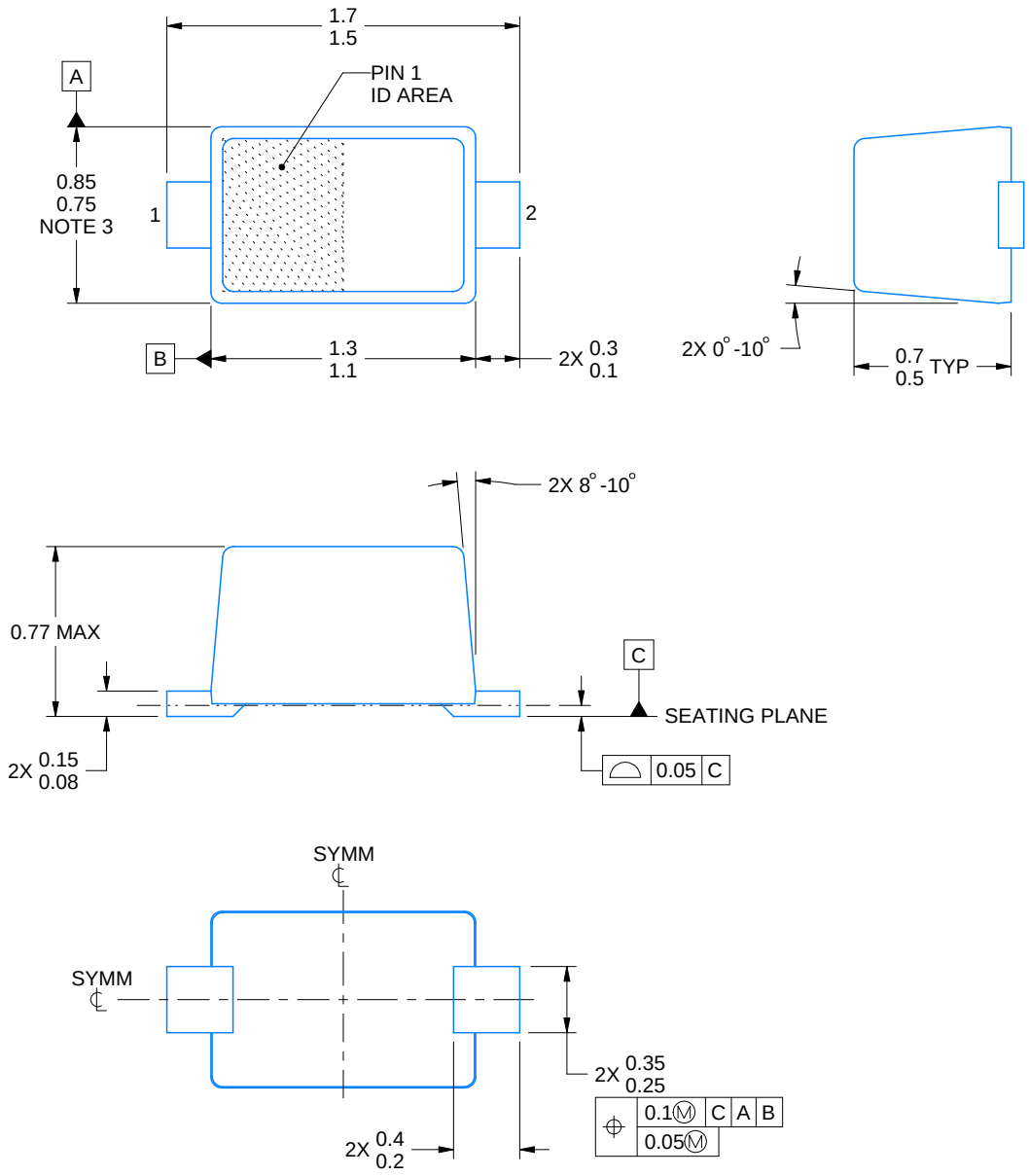
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



4224978/C 11/2024

NOTES:

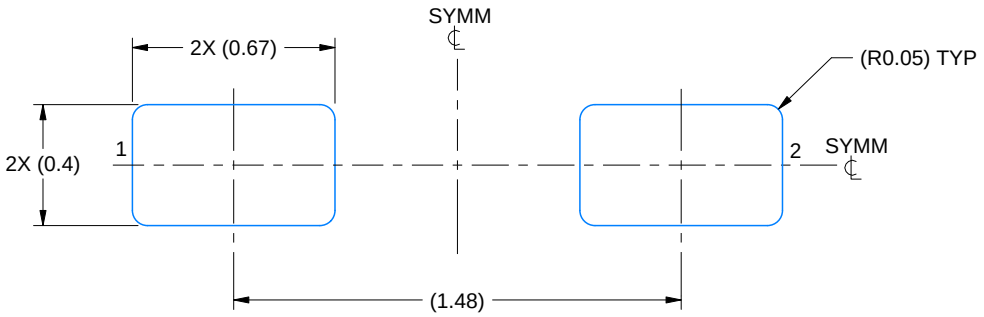
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height

EXAMPLE BOARD LAYOUT

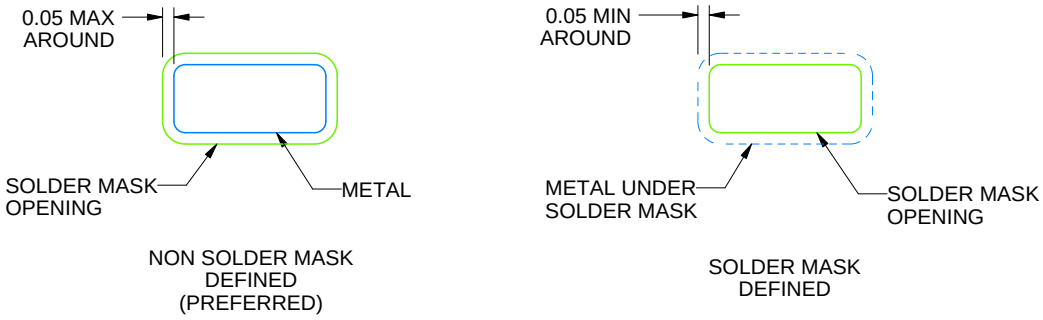
DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:40X

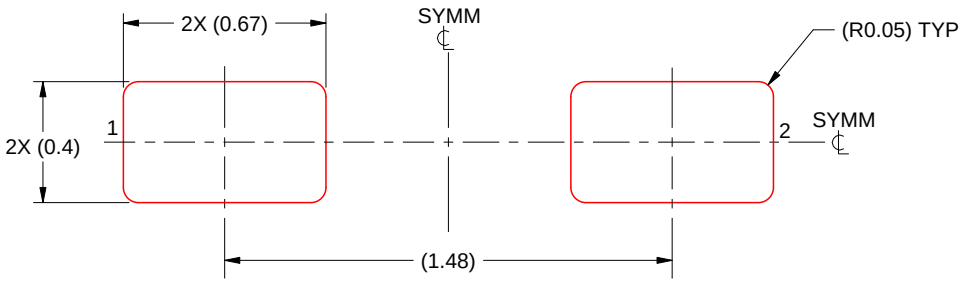


SOLDERMASK DETAILS

4224978/C 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/C 11/2024

NOTES: (continued)

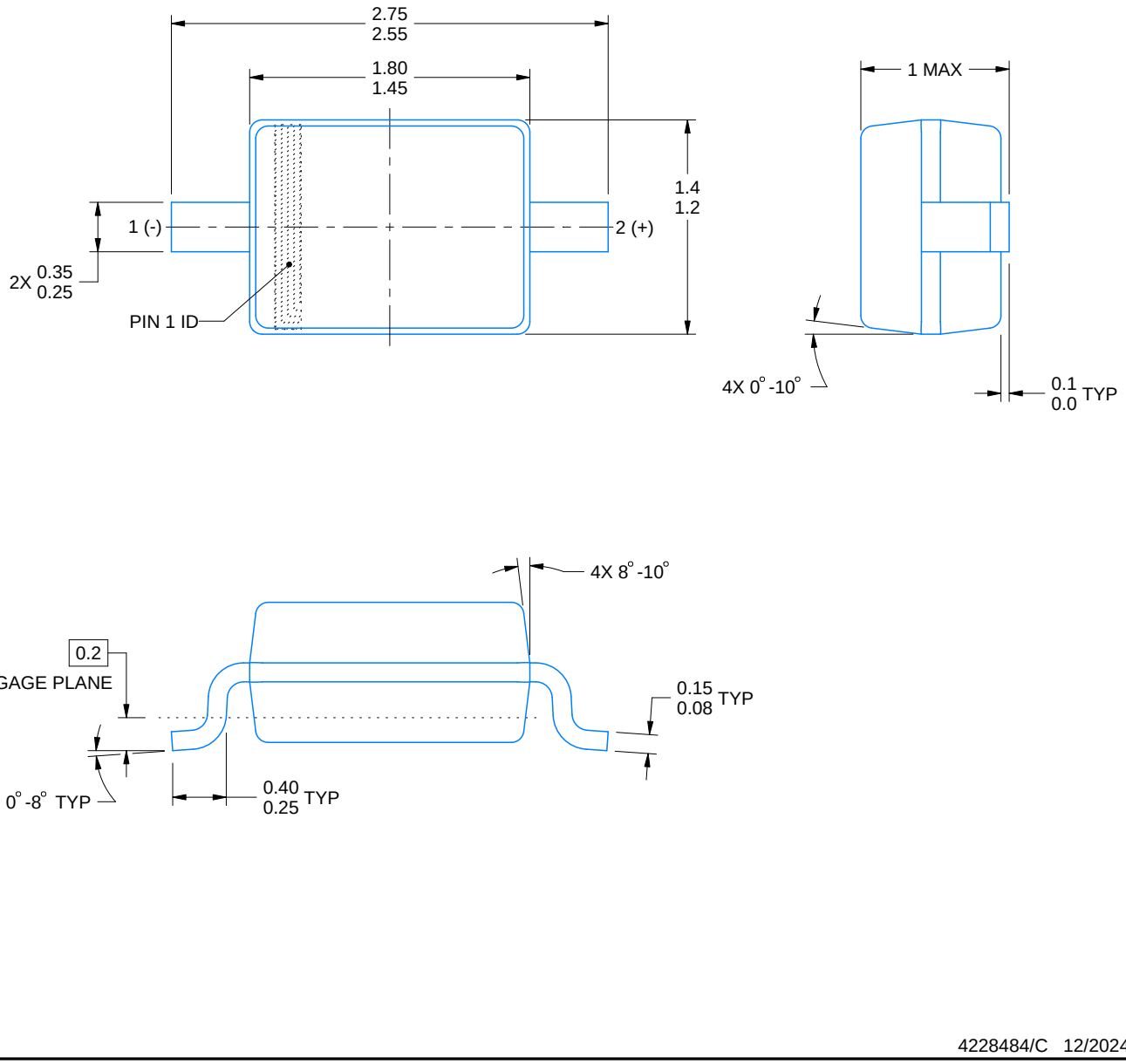
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYF0002A

SOT(SOD-323) - 1 mm max height

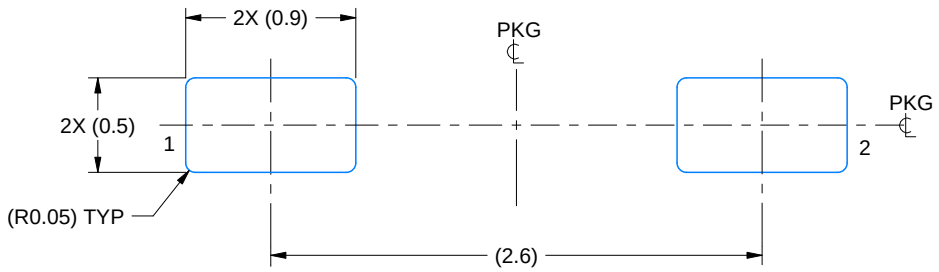
SMALL OUTLINE TRANSISTOR



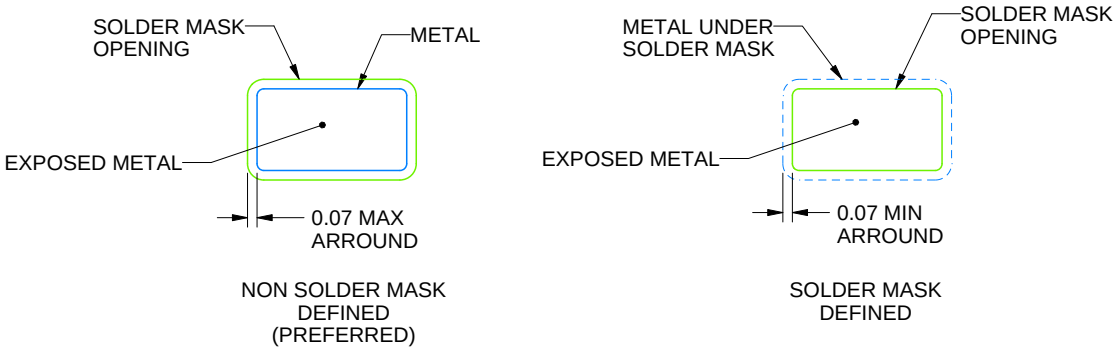
4228484/C 12/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

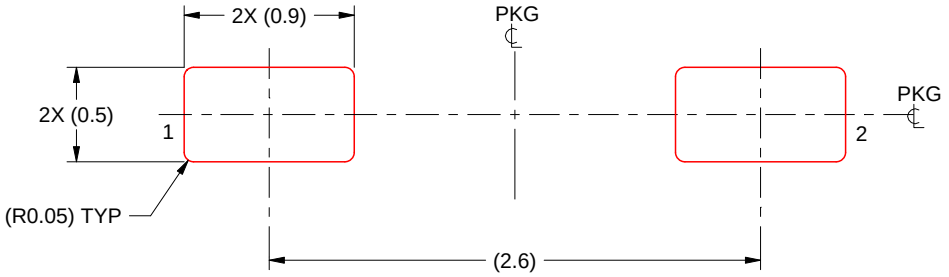


SOLDER MASK DETAILS

4228484/C 12/2024

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/C 12/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025