INA132 Low Power, Single-Supply Difference Amplifier

1 Features

- Wide supply range:
  - Single supply: 2.7V to 36V
  - Dual supplies: ±1.35V to ±18V
- DC precision performance:
  - Low gain error: ±0.075% (maximum)
  - Low nonlinearity: 0.001% (maximum)
  - High common-mode rejection: 90dB (typical)
- Low quiescent current: 175µA

2 Applications

- Optical modules
- Building security gateways
- AC analog input module
- Mass spectrometer
- CPU (PLC Controller)
- Lab and field instrumentation

3 Description

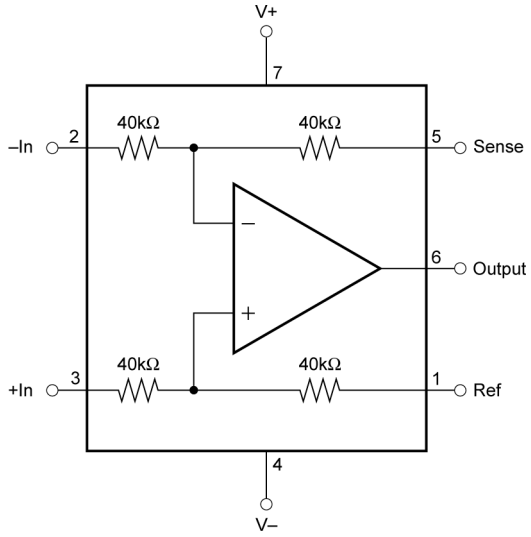
The INA132 is a low-power, unity-gain differential amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The internal op amp common-mode range extends to the negative supply —an excellent choice for single-supply applications. The INA132 operates on single (2.7V to 36V) or dual (±1.35V to ±18V) supplies.

The differential amplifier is the foundation of many commonly used circuits. The INA132 provides this circuit function without using an expensive precision resistor network. The INA132 is available in an SO-8 surface-mount package and operates over the industrial temperature range of –40°C to +85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA132	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Diagram

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4 Pin Configuration and Functions

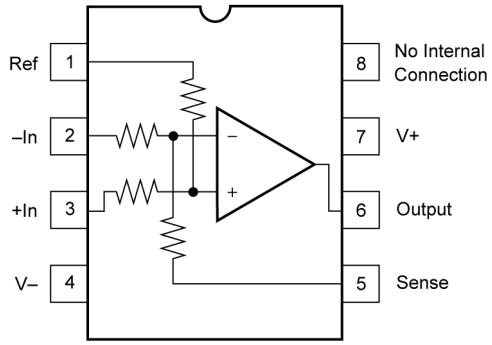


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–In	2	Input	Negative (inverting) input
+In	3	Input	Positive (noninverting) input
No Internal Connection	8	—	No internal connection. Leave unconnected.
Output	6	Output	Output
Ref	1	—	Reference input. Drive this pin with a low impedance source. Interchanging pin 1 and 3 degrade CMR.
Sense	5	—	Sense input. Drive this pin with a low impedance source. Interchanging pin 2 and 5 degrade CMR.
V–	4	Input	Negative supply
V+	7	Input	Positive supply

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 7.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0V		36	
	Input voltage range			±80	V
	Output short-circuit to (V_S / 2)		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±750	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply	2.7	36	V
		Dual-supply	±1.35	±18	
T_A	Specified temperature		–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA132 D (SOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics 15V

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S/2, G = 1, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage(1)	RTO	INA132		±75	±250	µV
			INA132A		±75	±500	
	Offset voltage drift(1)	RTO, T_A = –40°C to +85°C	INA132		±1	±5	µV/°C
			INA132A		±1	±10(4)	
	Long-term stability(1)				±0.3		µV/mo
PSRR	Power-supply rejection ratio(1)	RTO, V_S = ±1.35V to ±18V			±5	±30	µV/V
V_{CM}	Common-mode voltage	V_O = 0V		(V–)		2(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = –15V to +28V, R_S = 0Ω	INA132	76	90		dB
			INA132A	70	90		dB
	Differential input impedance(2)				80		kΩ
	Common-mode input impedance(2)				80		kΩ
NOISE							
e_N	Voltage noise(3)	RTO, f_B = 0.1Hz to 10Hz			1.6		μV_{PP}
		RTO, f = 1kHz			75		nV/√Hz
GAIN							
	Gain				1		V/V
GE	Gain error	V_O = –14V to +13.5V	INA132		±0.01	±0.075	%
			INA132A		±0.01	±0.1	
	Gain error drift(4)	T_A = –40°C to +85°C			±1	±10	ppm/°C
	Gain nonlinearity	V_O = –14V to +13.5V	INA132		±0.0001	±0.001	% of FSR
			INA132A		±0.0001	±0.002	
OUTPUT							
	Positive output voltage swing	R_L = 100kΩ		(V+) – 1	(V+) – 0.8		V
		R_L = 10kΩ		(V+) – 1.5	(V+) – 0.8		
	Negative output voltage swing	R_L = 100kΩ		(V–) + 0.5	(V–) + 0.15		V
		R_L = 10kΩ		(V–) + 1	(V–) + 0.25		
C_L	Load capacitance	Stable operation			10000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2	CSO: SHE		+6/-15		mA
			CSO: TID		+26/-22		
FREQUENCY RESPONSE							
BW	Small signal bandwidth, –3dB				300		kHz
SR	Slew rate	CSO: SHE			0.1		V/µs
		CSO: TID			0.25		
t_S	Settling time	V_O = 10V step	0.1%		85		µs
			0.01%		88		
	Overload recovery time	50% input overdrive	CSO: TID		2.35		µs
			CSO: SHE		7		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V			±175	±230	µA

(1) Includes effects of amplifier input bias and offset currents.
(2) 40kΩ resistors are ratio matched but have ±20% absolute value.
(3) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.
(4) Specified by wafer test to 95% confidence level.

5.6 Electrical Characteristics 5V

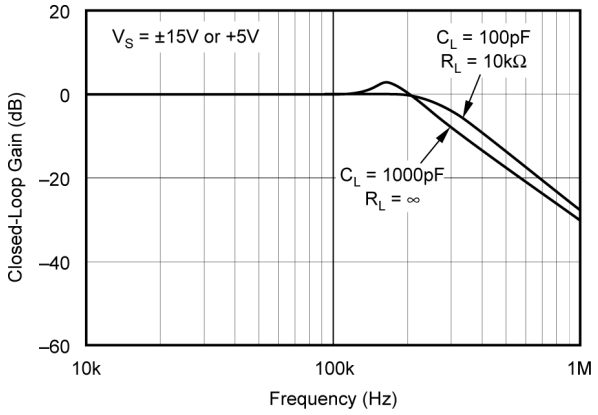
at T_A = 25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{REF} = $V_S/2$, V_{CM} = $V_S/2$, G = 1, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage(1)	RTO	INA132		±150	±500	µV
			INA132A		±150	±750	
	Offset voltage drift(1)	RTO, T_A = –40°C to +85°C			±2		µV/°C
V_{CM}	Common-mode voltage	V_O = 0V		(V–)		2(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = 0V to 8V, R_S = 0Ω	INA132	76	90		dB
			INA132A	70	90		
OUTPUT							
	Positive output voltage swing	R_L = 100kΩ		(V+) – 1	(V+) – 0.75		V
		R_L = 10kΩ		(V+) – 1	(V+) – 0.8		
	Negative output voltage swing	R_L = 100kΩ		(V–) + 0.25	(V–) + 0.06		V
		R_L = 10kΩ		(V–) + 0.25	(V–) + 0.12		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V			±175	±230	µA

(1) Includes effects of amplifier input bias and offset currents.

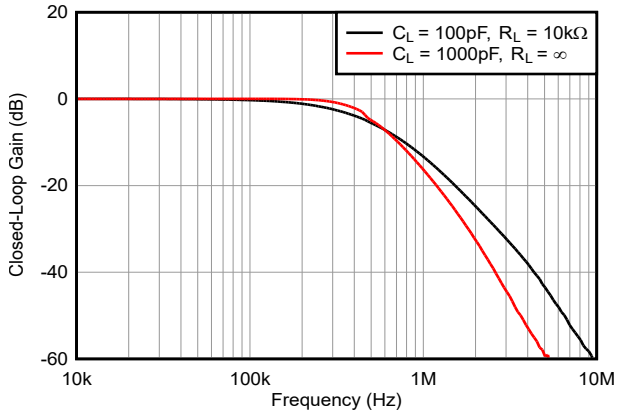
5.7 Typical Characteristics

at T_A = +25°C and V_S = ±15V, and all chip site origins (CSO), unless otherwise noted.



CSO: SHE

Figure 5-1. Gain vs Frequency



CSO: TID

Figure 5-2. Gain vs Frequency

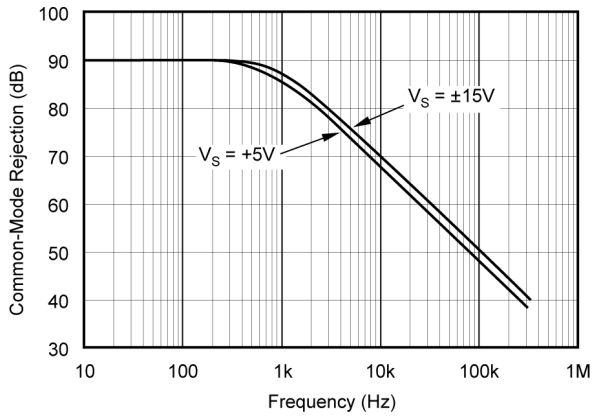
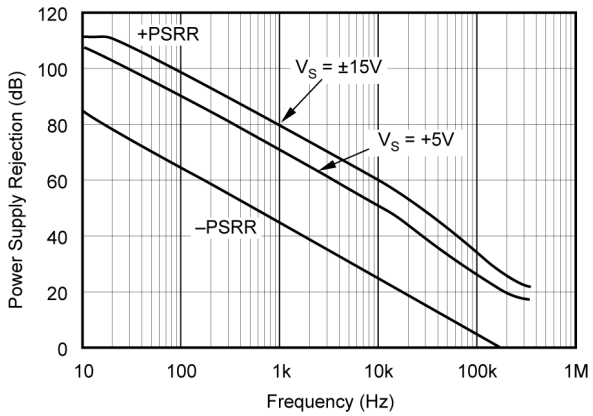
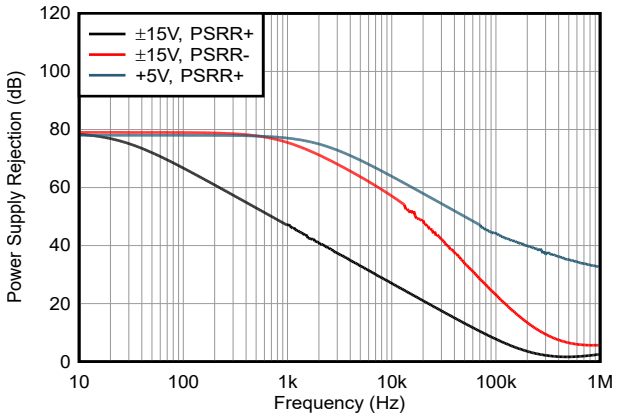


Figure 5-3. Common-Mode Rejection vs Frequency



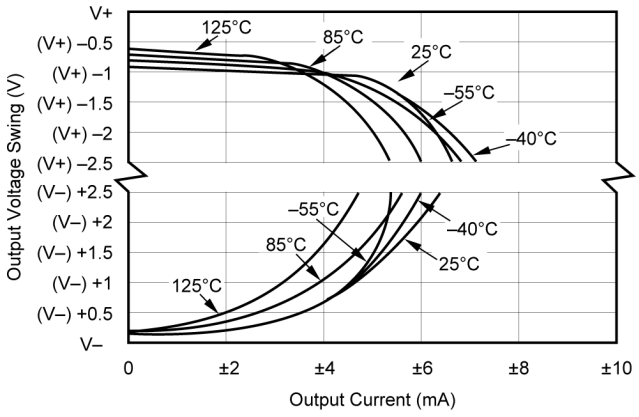
CSO: SHE

Figure 5-4. Power Supply Rejection vs Frequency



CSO: TID

Figure 5-5. Power Supply Rejection vs Frequency

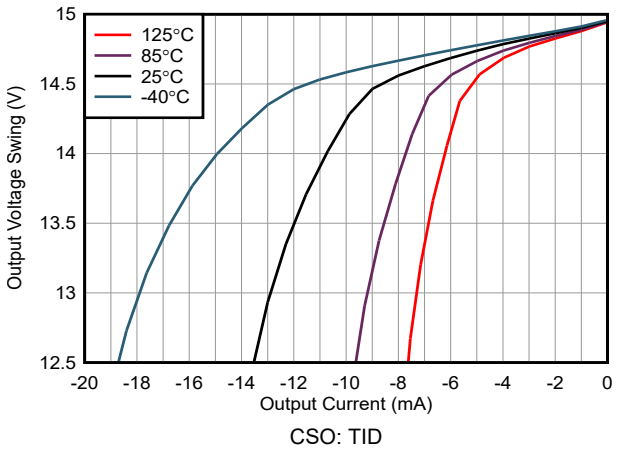


CSO: SHE

Figure 5-6. Output Voltage Swing vs Output Current

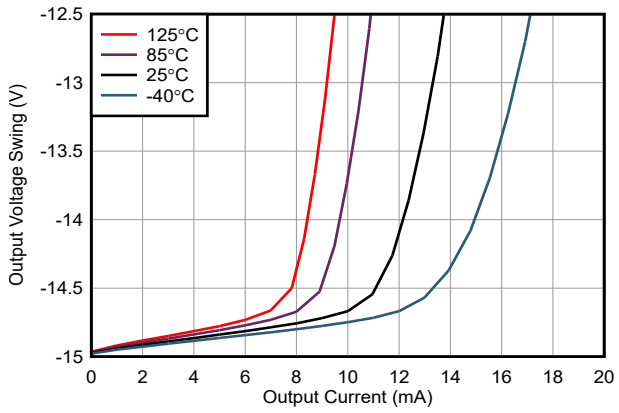
5.7 Typical Characteristics (continued)

at T_A = +25°C and V_S = ±15V, and all chip site origins (CSO), unless otherwise noted.



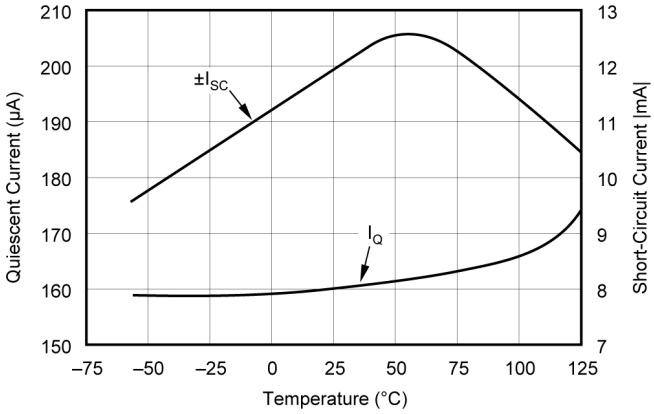
CSO: TID

Figure 5-7. Output Voltage Swing vs Output Current



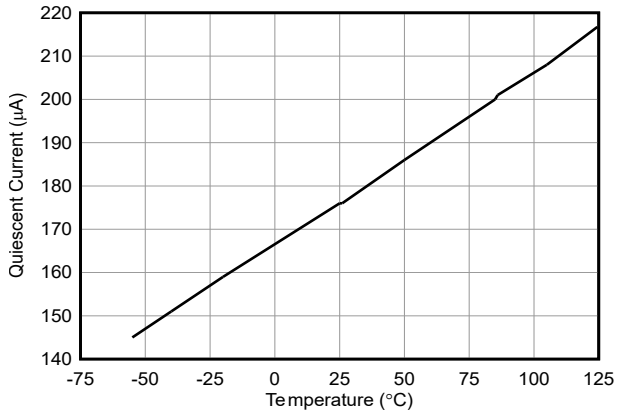
CSO: TID

Figure 5-8. Output Voltage Swing vs Output Current



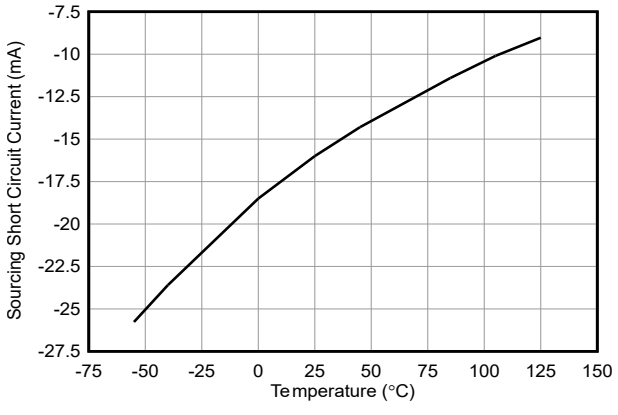
CSO: SHE

Figure 5-9. Quiescent and Short-Circuit Current vs Temperature



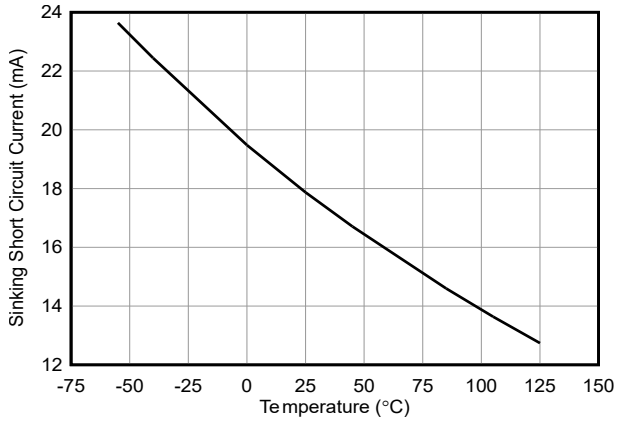
CSO: TID

Figure 5-10. Quiescent Current vs Temperature



CSO: TID

Figure 5-11. Short-Circuit Current vs Temperature



CSO: TID

Figure 5-12. Short-Circuit Current vs Temperature

5.7 Typical Characteristics (continued)

at T_A = +25°C and V_S = ±15V, and all chip site origins (CSO), unless otherwise noted.

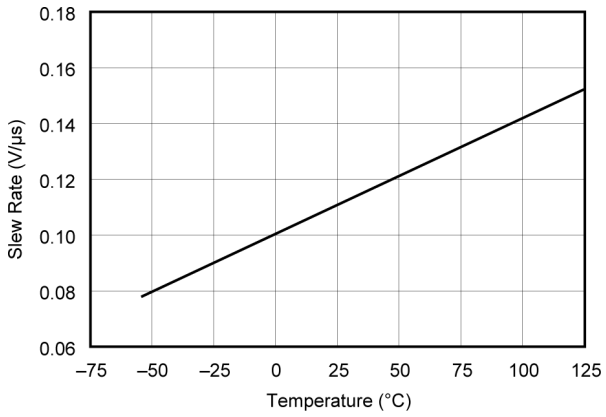
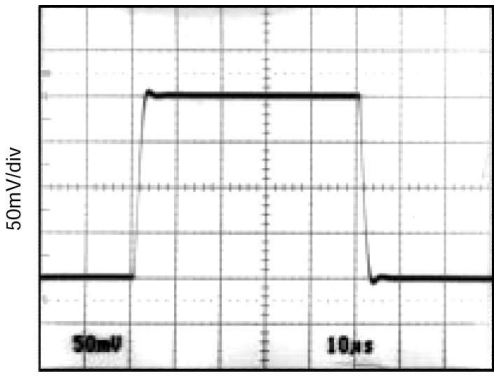
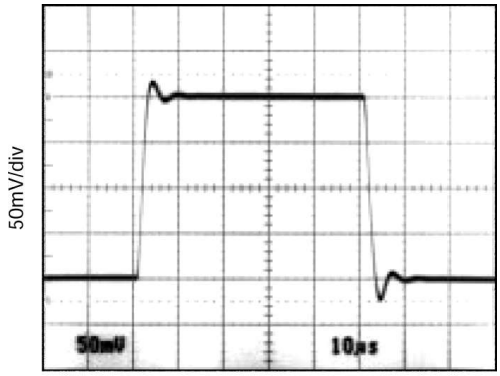


Figure 5-13. Slew Rate vs Temperature



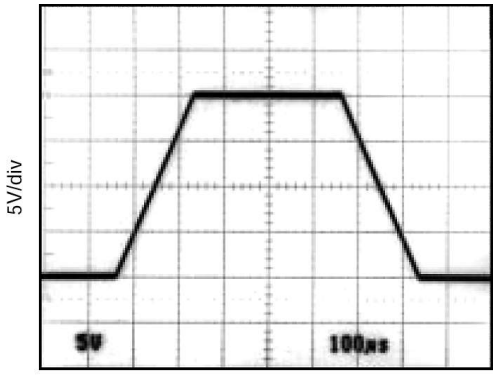
C_L = 200pF

Figure 5-14. Small-Signal Step Response



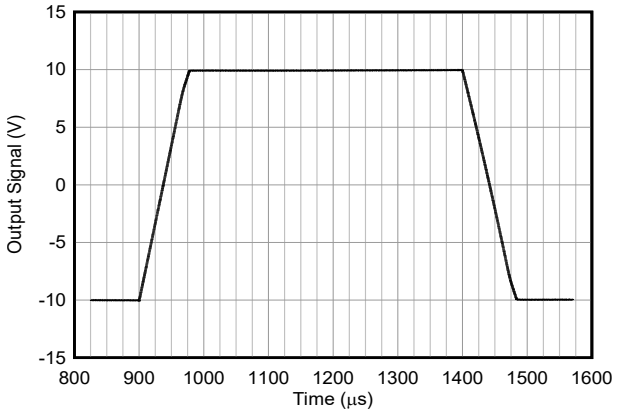
C_L = 1000pF

Figure 5-15. Small-Signal Step Response



CSO: SHE

Figure 5-16. Large-Signal Step Response



CSO: TID

Figure 5-17. Large-Signal Step Response

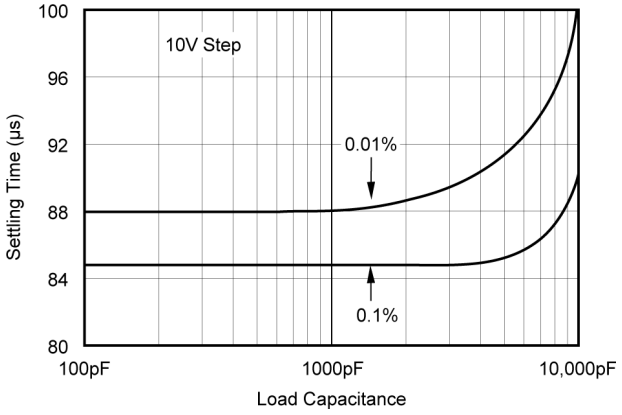


Figure 5-18. Settling Time vs Load Capacitance

5.7 Typical Characteristics (continued)

at T_A = +25°C and V_S = ±15V, and all chip site origins (CSO), unless otherwise noted.

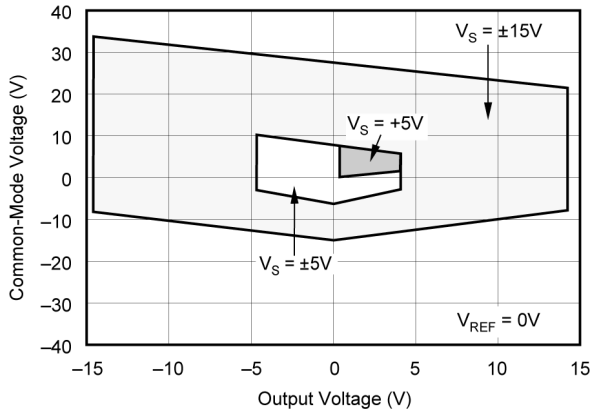


Figure 5-19. Input Common-mode Voltage Range vs Output Voltage

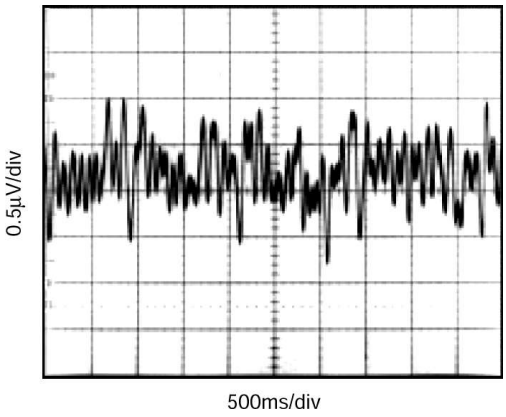


Figure 5-20. 0.1-Hz to 10-Hz Peak-to-Peak Voltage Noise

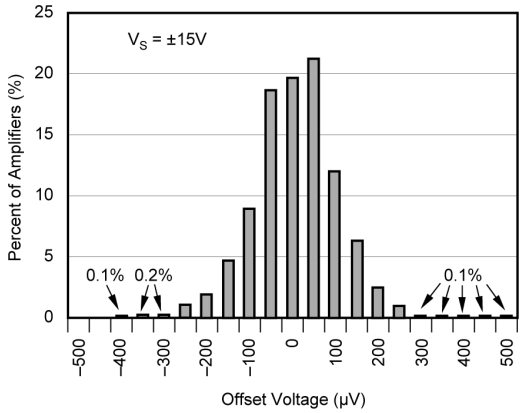


Figure 5-21. Offset Voltage Production Distribution

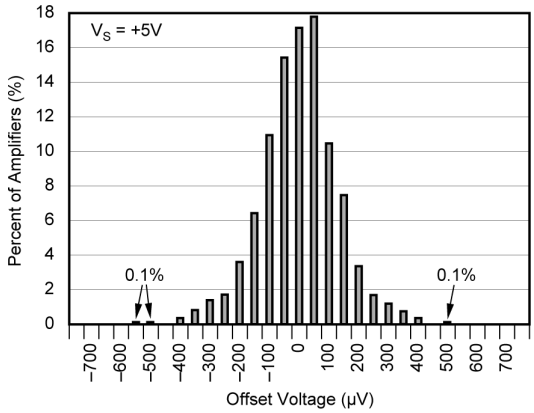


Figure 5-22. Offset Voltage Production Distribution

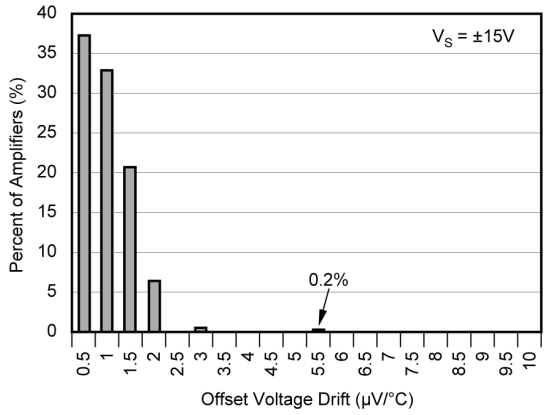


Figure 5-23. Offset Voltage Drift Production Distribution

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Applications Information

Figure 6-1 shows the basic connections required for operation of the INA132. Connect power-supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. Verify that the source impedances connected to the inputs are nearly equal to maintain good common-mode rejection. An 8Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80dB. Gain accuracy is also slightly affected. If the source has a known impedance mismatch, use an additional resistor in series with one input to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins does not provide specified performance. Sense measurements at the load, as in Figure 6-1.

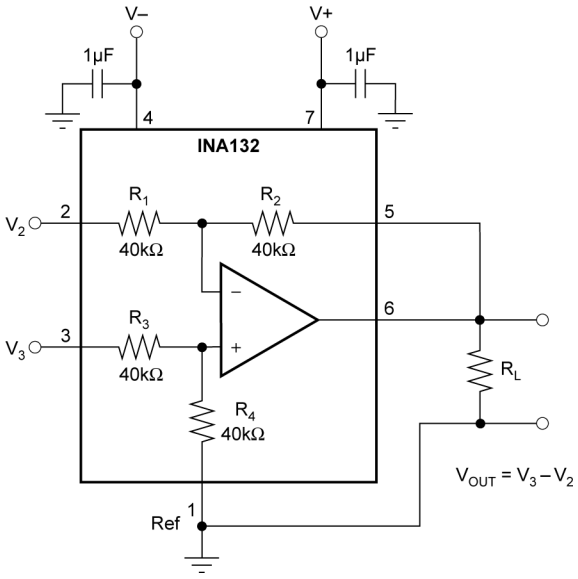


Figure 6-1. Basic Power Supply and Signal Connections

6.1.1 Operating Voltage

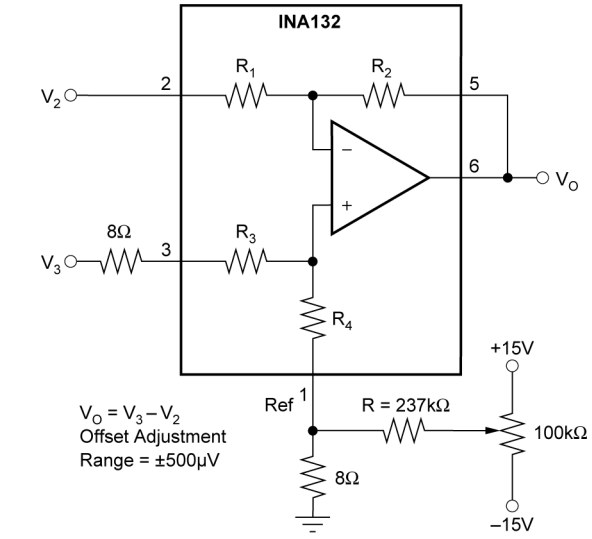
The INA132 operates from single (2.7V to 36V) or dual (±1.35V to ±18V) supplies with excellent performance. Specifications are production tested with +5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics*.

The internal op amp in the INA132 is a single-supply design. This design allows linear operation with the op-amp common-mode voltage equal to, or slightly below V– (or single supply ground). Although input voltages on pins 2 and 3 that are less than the negative supply voltage do not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal less than the negative supply can cause a positive feedback condition that can lock the INA132 output to the negative rail.

The INA132 can accurately measure differential signals that are greater than the positive power supply. The linear common-mode range extends to nearly twice the positive power supply voltage—see typical characteristics curve, *Common-Mode Range vs Output Voltage*.

6.1.2 Offset Voltage Trim

The INA132 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal, and can be used to null offset voltage. Verify that the source impedance of a signal applied to the Ref terminal is less than 8Ω to maintain good common-mode rejection. To maintain low impedance at the Ref terminal, the trim voltage can be buffered with an op amp, such as the OPA177.



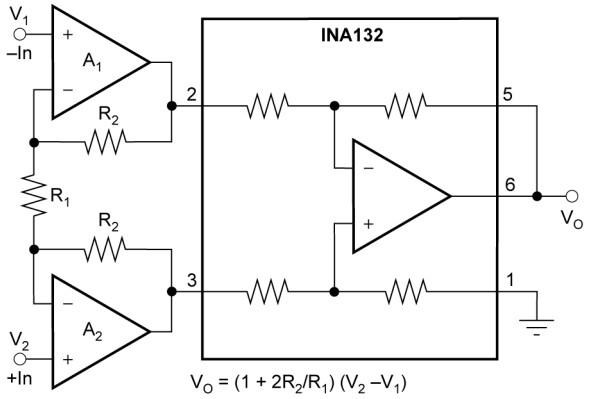
NOTE: For ±750µV range, R = 158kΩ.

Figure 6-2. Offset Adjustment.

6.1.3 Capacitive Load Drive Capability

The INA132 drives large capacitive loads, even at low supplies. The device is stable with a 10,000-pF load. See the *Small-Signal Step Response* and *Settling Time vs Load Capacitance* typical characteristics.

6.2 Typical Applications



The INA132 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right.

A_1, A_2	FEATURE	SIMILIAR COMPLETE BURR-BROWN IA
OPA27	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA177	Low Offset Drift, Low Noise	INA114,INA128
OPA2130	Low Power, FET-Input (pA)	INA111
OPA2234	Single Supply, Precision, Low Power	INA122(1), INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122(1), INA126(1)

NOTE: (1) Available 1Q'97.

Figure 6-3. Precision Instrumentation Amplifier

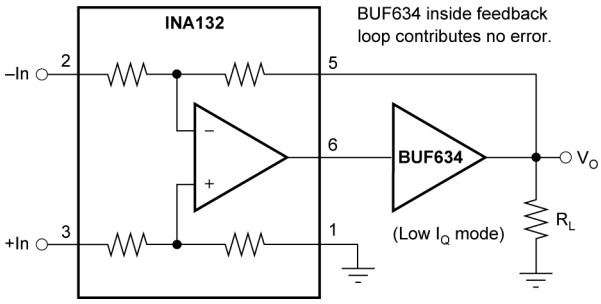


Figure 6-4. Low Power, High Output Current Precision Difference Amplifier

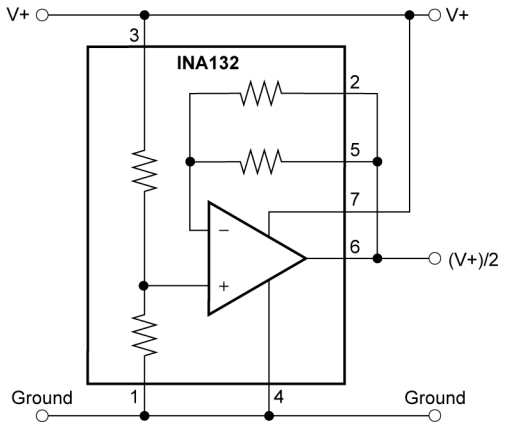


Figure 6-5. Pseudoground Generator

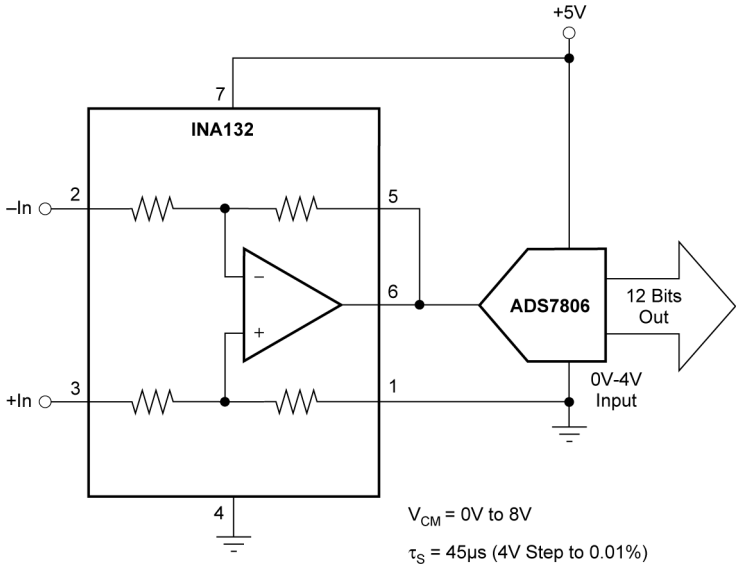


Figure 6-6. Differential Input Data Acquisition

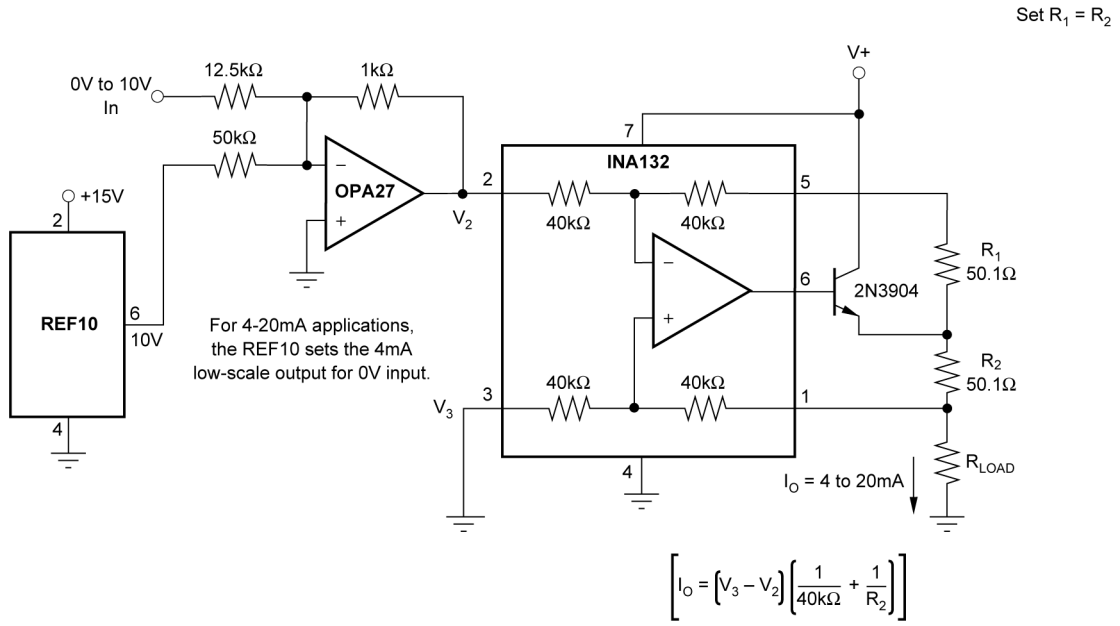


Figure 6-7. Precision Voltage-to-Current Conversion

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current receiver with compliance to rails
- Precision unity-gain inverting amplifier
- ±10-V precision voltage reference
- ±5-V precision voltage reference
- Precision unity-gain buffer
- Precision average value amplifier
- Precision G = 2 amplifier
- Precision summing amplifier
- Precision G = 1/2 amplifier
- Precision bipolar offsetting
- Precision summing amplifier with gain
- Instrumentation amplifier guard drive generator
- Precision summing instrumentation amplifier
- Precision absolute value buffer
- Precision voltage-to-current converter with differential inputs
- Differential input voltage-to-current converter for low I_{OUT}
- Isolating current source
- Differential output difference amplifier
- Isolating current source with buffering amplifier for greater accuracy
- Window comparator with window span and window center inputs
- Precision voltage-controlled current source with buffered differential inputs and gain
- Digitally controlled gain of ±1 amplifier

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Nomenclature

Table 7-1. Device Nomenclature

Part Number	Definition
INA132U INA132U/2K5 INA132UA INA132UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

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All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2024) to Revision B (January 2026)	Page
• Added description of device flow information in *Specifications*	3
• Added all chip site origins (CSO) condition to the typical test conditions in the *Electrical Characteristics*	4
• Added different fabrication process specifications for short-circuit current in the *Electrical Characteristics*	4
• Added different fabrication process specifications for slew rate in the *Electrical Characteristics*	4
• Added different fabrication process specifications for overload recovery in the *Electrical Characteristics*	4
• Added all chip site origins (CSO) condition to the typical test conditions in the *Typical Characteristics*	6
• Added "CSO:SHE" to Gain vs Frequency, Power Supply Rejection vs Frequency, Output Voltage Swing vs Output Current, Quiescent and Short-Circuit Current vs Temperature, and Large-Signal Step Response curves in the *Typical Characteristics*	6

- Added Gain vs Frequency, Power Supply Rejection vs Frequency, Output Voltage Swing vs Output Current, Quiescent Current vs Temperature, Short-Circuit Current vs Temperature, and Large-Signal Step Response curves for CSO: TID in the *Typical Characteristics* 6
- Added Part Number flow information table to the *Device Nomenclature* 15

Changes from Revision * (November 1996) to Revision A (February 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added the *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Application and Implementation*, *Typical Applications*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections.....1
- Deleted DIP package and associated content from data sheet.....1
- Updated *Features* bullets..... 1
- Updated *Applications* bullets..... 1
- Added *Pin Functions* table.....2
- Added dual supply specification to *Absolute Maximum Ratings* 3
- Changed output short-circuit from "ground" to "V_S / 2" in *Absolute Maximum Ratings* 3
- Added V_{REF} = 0V, V_{CM} = V_S / 2, and G = 1 to test conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity..... 4
- Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added T_A = –40°C to +85°C test condition for clarity.....4
- Changed "Offset Voltage vs Time" to "Long-term stability" for clarity.....4
- Changed "Offset Voltage vs Power Supply" to Power-supply rejection ratio for clarity.....4
- Changed voltage noise typical value at 1kHz from 65nV/√Hz to 75nV/√Hz 4
- Changed "Gain Error vs Temperature" to "Gain error drift" and added T_A = –40°C to +85°C test condition for clarity.....4
- Changed "Voltage, Positive" to "Positive output voltage swing" and from "Voltage, Negative" to "Negative output voltage swing".....4
- Added test condition of "Continuous to V_S / 2" to short-circuit current for clarity.....4
- Changed short-circuit current typical value from ±12mA to +6mA/–15mA.....4
- Deleted power supply voltage range typical value of ±15V.....4
- Moved voltage range, operating temperature range, and thermal resistance from *Electrical Characteristics* to *Recommended Operating Conditions* and *Thermal Information* 4
- Changed quiescent current typical value from ±160µA to ±175µA and maximum value from ±185µA to ±230µA..... 4
- Added V_{REF} = V_S / 2, V_{CM} = V_S / 2, and G = 1 to test conditions in *Electrical Characteristics: V_S = 5V* for clarity..... 5
- Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added T_A = –40°C to +85°C test condition for clarity.....5
- Added (V–) to negative output voltage swing minimum and typical values.....5
- Deleted power supply voltage range typical value of +5V.....5
- Moved voltage range from *Electrical Characteristics: V_S = 5V* to *Recommended Operating Conditions* 5
- Changed quiescent current typical value from ±155µA to ±175µA and maximum value from ±185µA to ±230µA..... 5

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA132U	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-	INA 132U
INA132U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 132U
INA132U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 132U
INA132UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	INA 132U A
INA132UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A
INA132UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

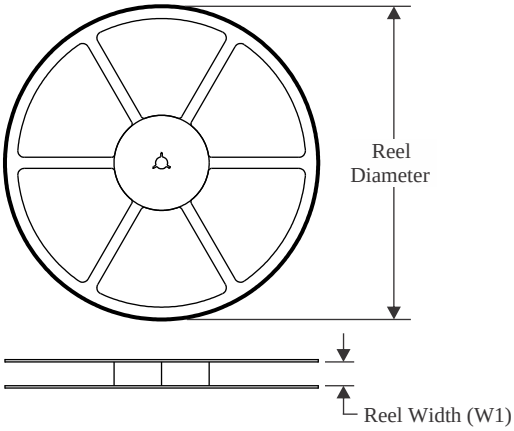
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

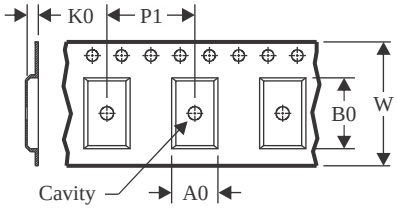
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

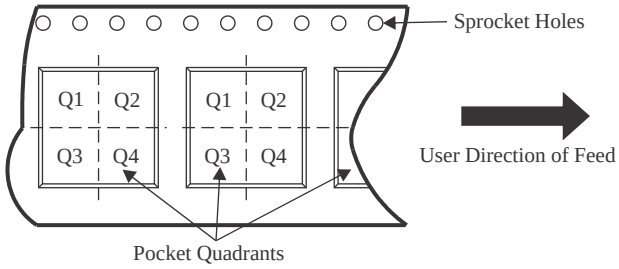


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

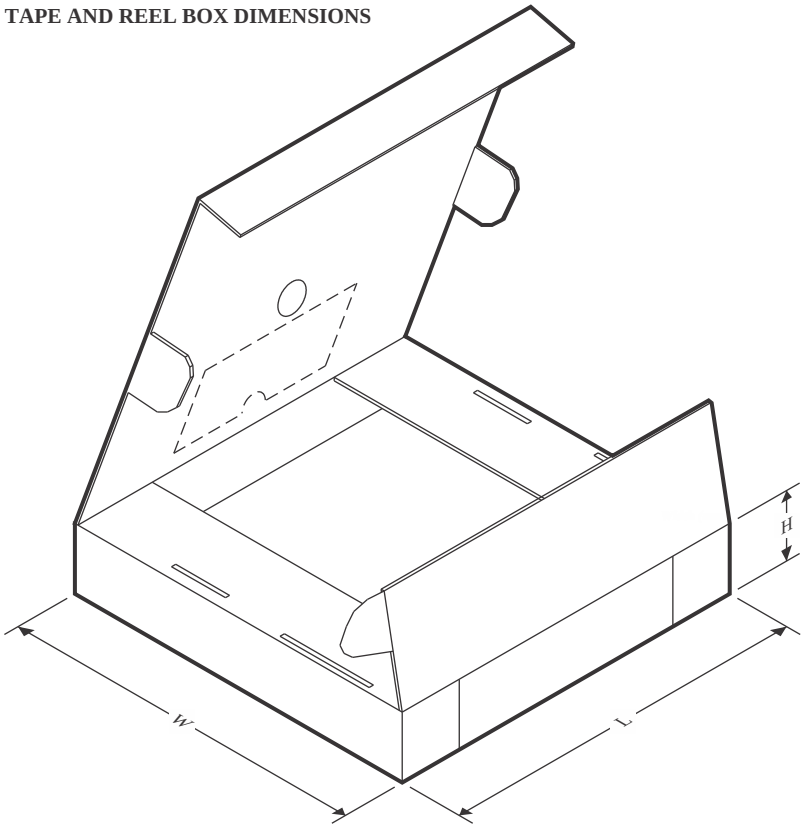
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

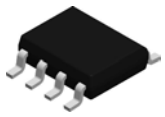
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA132UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

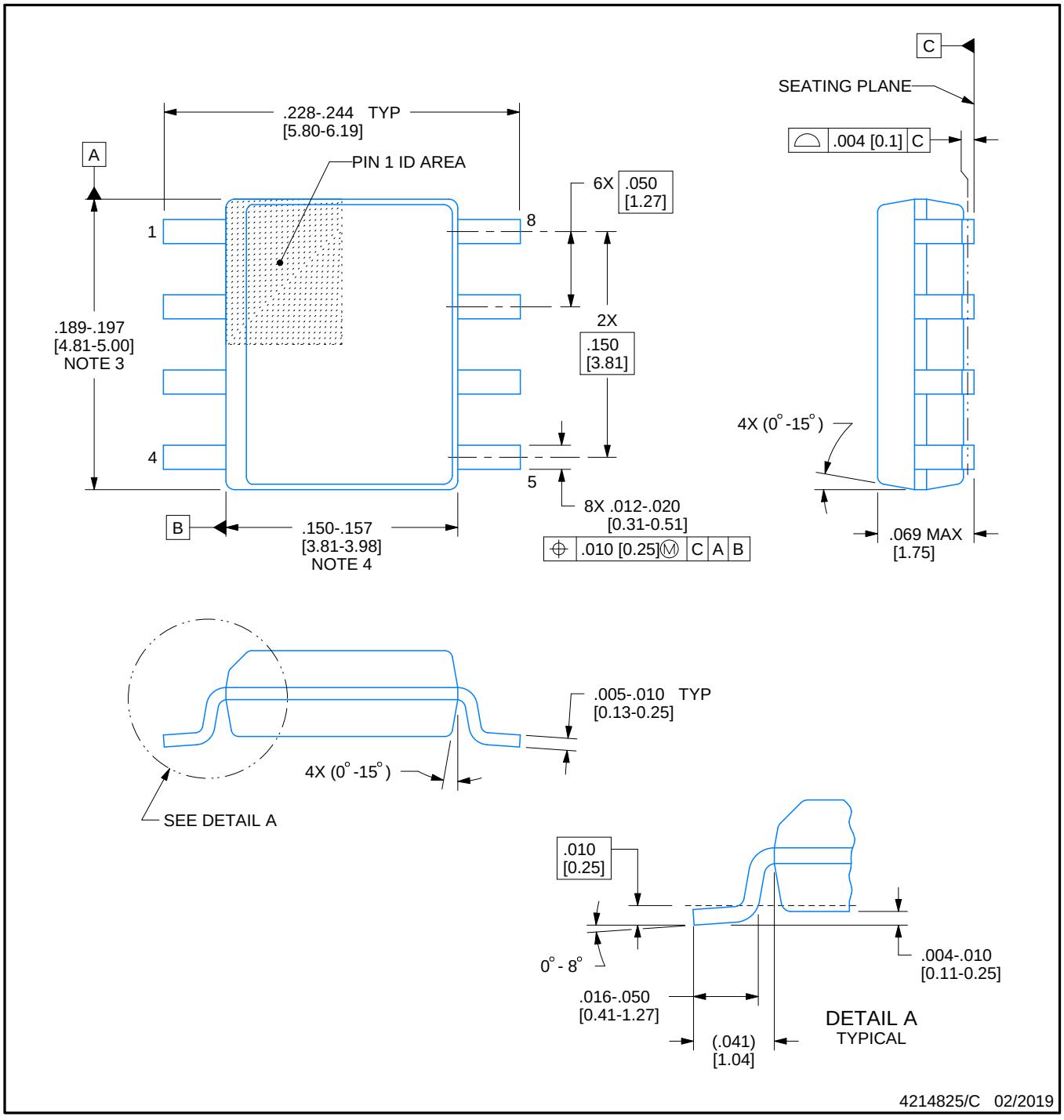


PACKAGE OUTLINE

D0008A

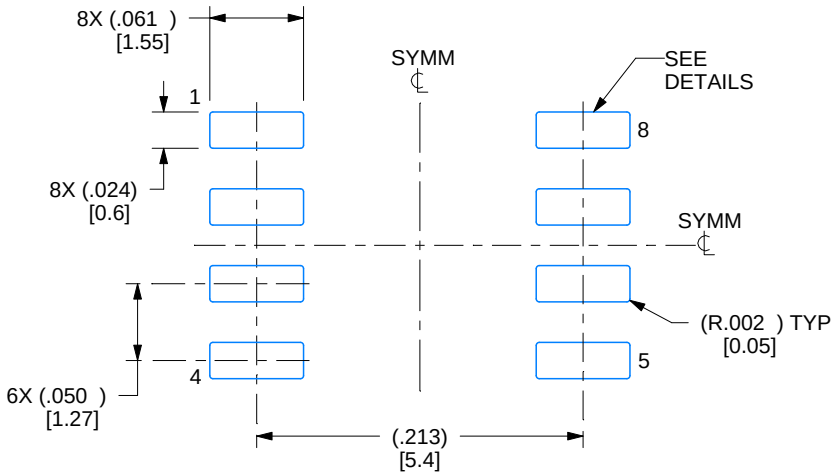
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

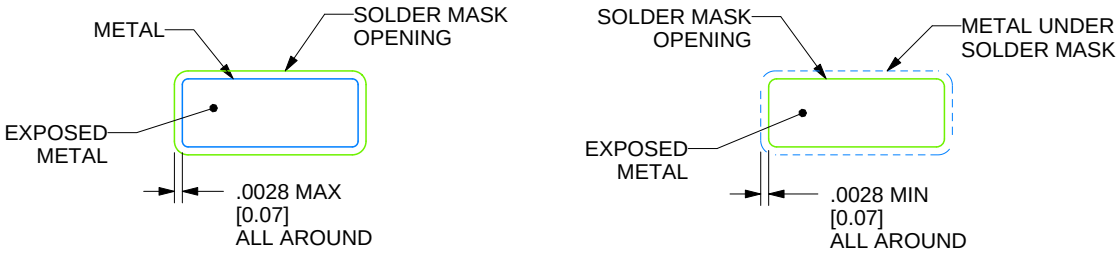


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

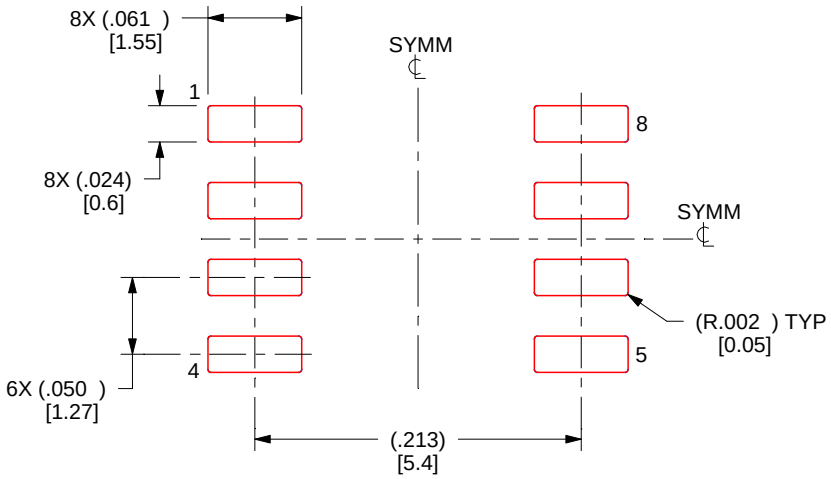
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025