# INAx181-Q1 Automotive, Bidirectional, Low- and High-Side Voltage Output, Current-Sense Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: $-40°C \leq T_A \leq 125°C$
  - HBM ESD classification level 2
  - CDM ESD classification level C6
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Common-mode range (V_{CM}): –0.2V to 26V
- High bandwidth: 350kHz (A1 devices)
- Offset voltage:
  - ±150µV (maximum) at V_{CM} = 0V
  - ±500µV (maximum) at V_{CM} = 12V
- Output slew rate: 2V/µs
- Bidirectional current-sensing capability
- Accuracy:
  - ±1% gain error (maximum)
  - 1µV/°C offset drift (maximum)
- Gain options:
  - 20V/V (A1 devices)
  - 50V/V (A2 devices)
  - 100V/V (A3 devices)
  - 200V/V (A4 devices)
- Quiescent current: 260µA maximum (INA181-Q1)

2 Applications

- Motor control
- Battery monitors and balancers
- Power management
- Lighting control
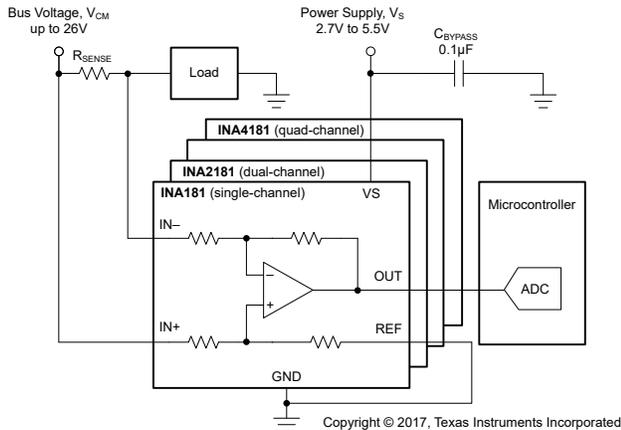
Typical Application Circuit

3 Description

The INA181-Q1, INA2181-Q1, and INA4181-Q1 (INAx181-Q1) current sense amplifiers are designed for cost-optimized applications. These devices are part of a family of bidirectional, current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2V to 26V, independent of the supply voltage. The INAx181-Q1 family integrates a matched resistor gain network in four, fixed-gain device options: 20V/V, 50V/V, 100V/V, or 200V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

These devices operate from a single 2.7-V to 5.5-V power supply. The single-channel INA181-Q1 draws a maximum supply current of 260µA; whereas, the dual-channel INA2181-Q1 draws a maximum supply current of 500µA, and the quad-channel INA4181-Q1 draws a maximum supply current of 900µA.

The INA181-Q1 is available in both the 6-pin, SOT-23 and SC70 packages. The INA2181-Q1 is available in a 10-pin, VSSOP package. The INA4181-Q1 is available in a 20-pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
INA181-Q1	DBV (SOT-23, 6)	2.90mm × 2.80mm
	DCK (SC70, 6)	2.00mm × 2.10mm
INA2181-Q1	DGS (VSSOP, 10)	3.00mm × 4.90mm
INA4181-Q1	PW (TSSOP, 20)	6.50mm × 6.40mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Device Comparison

Table 4-1. Device Comparison

PRODUCT	NUMBER OF CHANNELS	GAIN (V/V)
INA181A1-Q1	1	20
INA181A2-Q1	1	50
INA181A3-Q1	1	100
INA181A4-Q1	1	200
INA2181A1-Q1	2	20
INA2181A2-Q1	2	50
INA2181A3-Q1	2	100
INA2181A4-Q1	2	200
INA4181A1-Q1	4	20
INA4181A2-Q1	4	50
INA4181A3-Q1	4	100
INA4181A4-Q1	4	200

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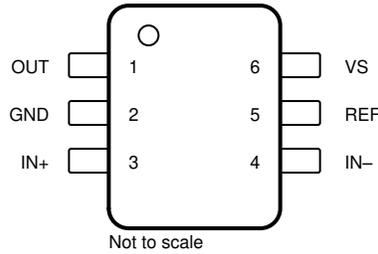Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

5 Pin Configuration and Functions

Figure 5-1. INA181-Q1: DBV Package 6-Pin SOT-23 Top View
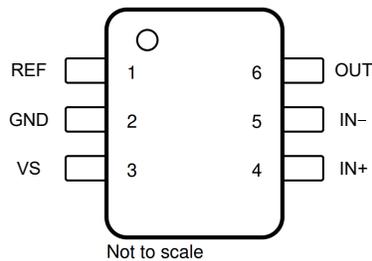
Figure 5-2. INA181-Q1: DCK Package 6-Pin SC70 Top View

Table 5-1. Pin Functions: INA181-Q1 (Single Channel)

PIN			TYPE	DESCRIPTION
NAME	SOT-23	SC70		
GND	2	2	Analog	Ground
IN–	4	5	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	3	4	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
OUT	1	6	Analog output	Output voltage
REF	5	1	Analog input	Reference input
VS	6	3	Analog	Power supply, 2.7 V to 5.5 V

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*
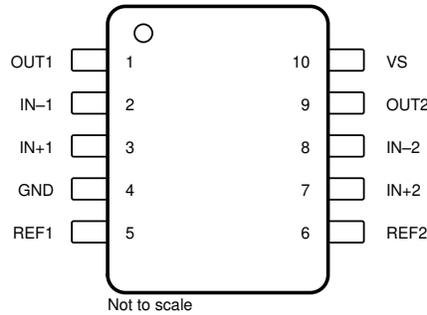
Figure 5-3. INA2181-Q1: DGS Package 10-Pin VSSOP Top View
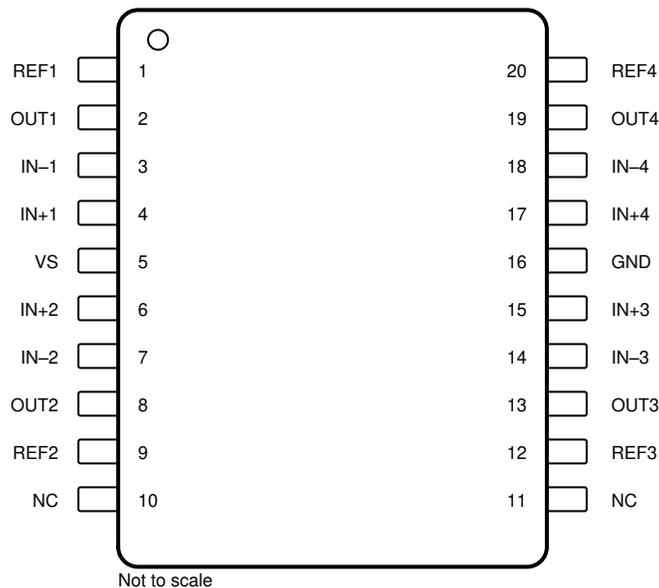
Figure 5-4. INA4181-Q1: PW Package 20-Pin TSSOP Top View

Table 5-2. Pin Functions: INA2181-Q1 (Dual Channel) and INA4181-Q1 (Quad Channel)

PIN			TYPE	DESCRIPTION
NAME	INA2181-Q1	INA4181-Q1		
GND	4	16	Analog	Ground
IN–1	2	3	Analog input	Current-sense amplifier negative input for Channel 1. For high-side applications, connect to load side of Channel 1 sense resistor. For low-side applications, connect to ground side of Channel 1 sense resistor.
IN+1	3	4	Analog input	Current-sense amplifier positive input for Channel 1. For high-side applications, connect to bus-voltage side of Channel 1 sense resistor. For low-side applications, connect to load side of Channel 1 sense resistor.
IN–2	8	7	Analog input	Current-sense amplifier negative input for Channel 2. For high-side applications, connect to load side of Channel 2 sense resistor. For low-side applications, connect to ground side of Channel 2 sense resistor.
IN+2	7	6	Analog input	Current-sense amplifier positive input for Channel 2. For high-side applications, connect to bus-voltage side of Channel 2 sense resistor. For low-side applications, connect to load side of Channel 2 sense resistor.
IN–3	—	14	Analog input	Current-sense amplifier negative input for Channel 3. For high-side applications, connect to load side of Channel 3 sense resistor. For low-side applications, connect to ground side of Channel 3 sense resistor.
IN+3	—	15	Analog input	Current-sense amplifier positive input for Channel 3. For high-side applications, connect to bus-voltage side of Channel 3 sense resistor. For low-side applications, connect to load side of Channel 3 sense resistor.

Table 5-2. Pin Functions: INA2181-Q1 (Dual Channel) and INA4181-Q1 (Quad Channel) (continued)

PIN			TYPE	DESCRIPTION
NAME	INA2181-Q1	INA4181-Q1		
IN–4	—	18	Analog input	Current-sense amplifier negative input for Channel 4. For high-side applications, connect to load side of Channel 4 sense resistor. For low-side applications, connect to ground side of Channel 4 sense resistor.
IN+4	—	17	Analog input	Current-sense amplifier positive input for Channel 4. For high-side applications, connect to bus-voltage side of Channel 4 sense resistor. For low-side applications, connect to load side of Channel 4 sense resistor.
NC	—	10, 11	—	NC denotes no internal connection. These pins can be left floating or connected to any voltage between V_S and ground.
OUT1	1	2	Analog output	Channel 1 output voltage
OUT2	9	8	Analog output	Channel 2 output voltage
OUT3	—	13	Analog output	Channel 3 output voltage
OUT4	—	19	Analog output	Channel 4 output voltage
REF1	5	1	Analog input	Channel 1 reference voltage, 0 to V_S
REF2	6	9	Analog input	Channel 2 reference voltage, 0 to V_S
REF3	—	12	Analog input	Channel 3 reference voltage, 0 to V_S
REF4	—	20	Analog input	Channel 4 reference voltage, 0 to V_S
VS	10	5	Analog	Power supply pin, 2.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs, IN+, IN– [2]	Differential $(V_{IN+}) - (V_{IN-})$	−28	28	V
	Common-mode [3]	GND – 0.3	28	
Input voltage range	at REF pin	GND – 0.3	V_S + 0.3	V
Output Voltage		GND – 0.3	V_S + 0.3	V
Maximum output current, I_{OUT}			8	mA
Operating fee-air temperature, T_A		−55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1)   Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.
(3)   Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage (IN+ and IN–)	−0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC [1]		INA181-Q1		INA2181-Q1		INA4181-Q1	UNIT
		DCK (SC70)	DBV (SOT-23)	DSQ (WSON)	DGS (VSSOP)	PW (TSSOP)	
		6 PINS	6 PINS	10 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.0	198.7	74.5	177.3	97.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	140.8	120.9	89.7	68.7	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.8	52.3	39.8	98.4	48.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	62.1	30.3	3.7	12.6	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.5	52.0	39.7	96.9	47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	16.8	N/A	N/A	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = 5V, V_{REF} = V_S / 2, V_{IN+} = 12V, and V_{SENSE} = V_{IN+} − $V_{IN−}$ (unless otherwise noted)

| PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection ratio, RTI [1]	V_{IN+} = 0V to 26V, V_{SENSE} = 0mV, T_A = −40°C to +125°C	84	100		dB
V_{OS}	Offset voltage, RTI	V_{SENSE} = 0mV, V_{IN+} = 0V		±25	±150	µV
		V_{SENSE} = 0mV		±100	±500	µV
dV_{OS}/dT	Offset drift, RTI	V_{SENSE} = 0mV, T_A = −40°C to +125°C		0.2	1	µV/°C
PSRR	RTI vs power supply ratio	V_S = 2.7V to 5.5V, V_{IN+} = 12V, V_{SENSE} = 0mV		±8	±40	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0mV, V_{IN+} = 0V		-6		µA
		V_{SENSE} = 0mV		75		µA
I_{IO}	Input offset current	V_{SENSE} = 0mV		±0.05		µA
OUTPUT						
G	Gain	A1 devices		20		V/V
		A2 devices		50		V/V
		A3 devices		100		V/V
		A4 devices		200		V/V
E_G	Gain error	V_{OUT} = 0.5V to V_S − 0.5V, T_A = −40°C to +125°C		±0.1%	±1%	
	Gain error vs temperature	T_A = −40°C to +125°C		1.5	20	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5V to V_S − 0.5V		±0.01%		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT [2]						
V_{SP}	Swing to V_S power-supply rail [3]	R_L = 10kΩ to GND, T_A = −40°C to +125°C		(V_S) − 0.02	(V_S) − 0.03	V
V_{SN}	Swing to GND [3]	R_L = 10kΩ to GND, T_A = −40°C to +125°C		(V_{GND}) + 0.0005	(V_{GND}) + 0.005	V
FREQUENCY RESPONSE						
BW	Bandwidth	A1 devices, C_{LOAD} = 10pF		350		kHz
		A2 devices, C_{LOAD} = 10pF		210		kHz
		A3 devices, C_{LOAD} = 10pF		150		kHz
		A4 devices, C_{LOAD} = 10pF		105		kHz
SR	Slew rate			2		V/µs
NOISE, RTI [1]						
	Voltage noise density			40		nV/√Hz
POWER SUPPLY						
I_Q	Quiescent current	INA181	V_{SENSE} = 0mV		195	260	µA
			V_{SENSE} = 0mV, T_A = −40°C to +125°C			300	
		INA2181	V_{SENSE} = 0mV		356	500	µA
			V_{SENSE} = 0mV, T_A = −40°C to +125°C			520	
		INA4181	V_{SENSE} = 0mV		690	900	µA
			V_{SENSE} = 0mV, T_A = −40°C to +125°C			1000	

(1)   RTI = referred-to-input.
(2)   See Output Voltage Swing vs Output Current
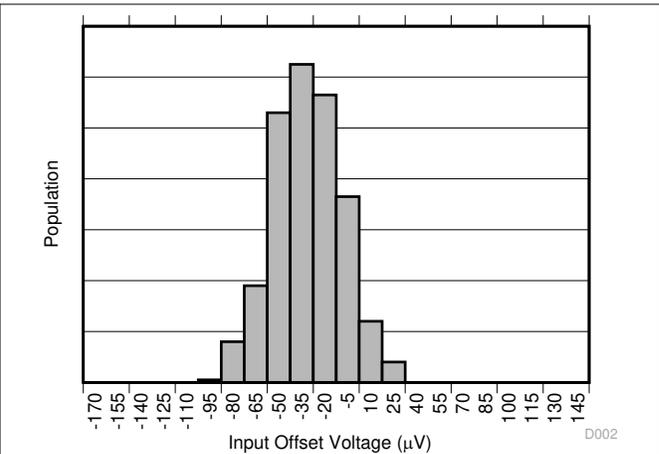(3)   Swing specifications are tested with an overdriven input condition.
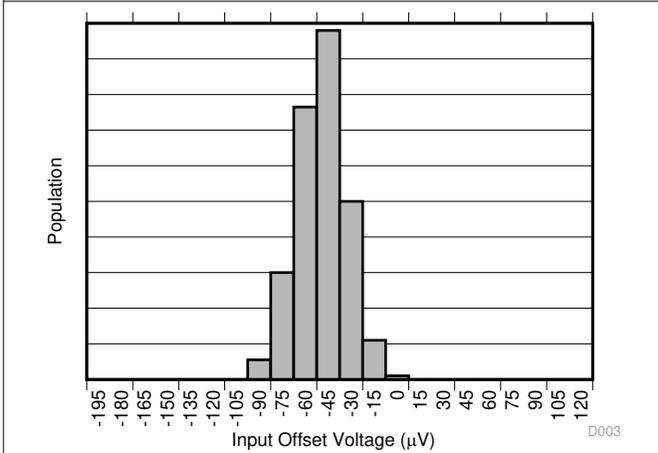
6.6 Typical Characteristics

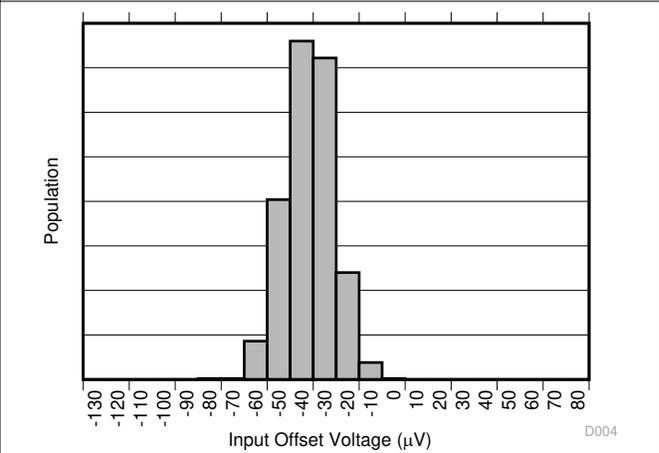at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)
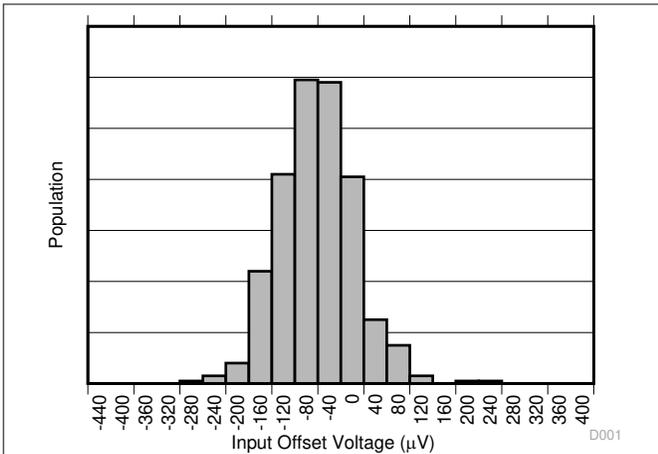
Figure 6-1. Input Offset Voltage Production Distribution A1
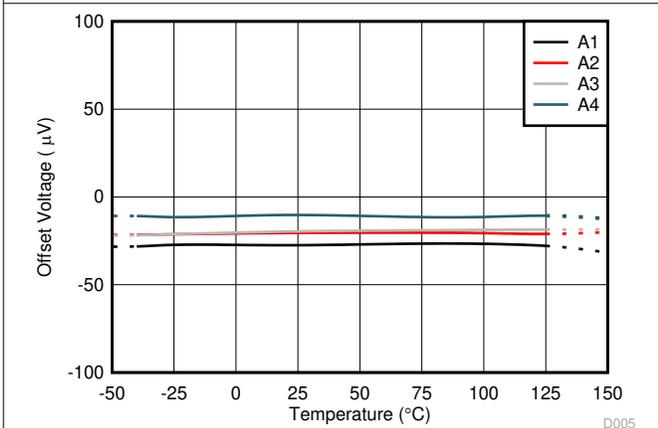

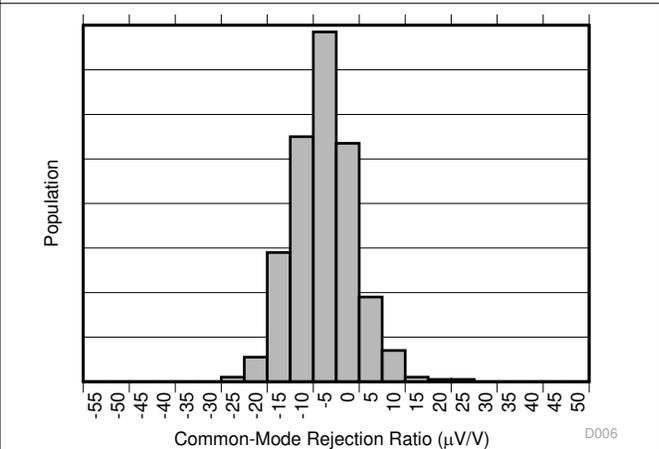**Figure 6-2. Input Offset Voltage Production Distribution A2**

Figure 6-3. Input Offset Voltage Production Distribution A3

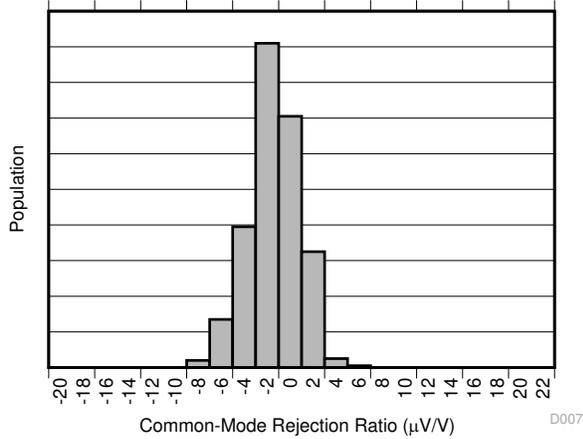**Figure 6-4. Input Offset Voltage Production Distribution A4**

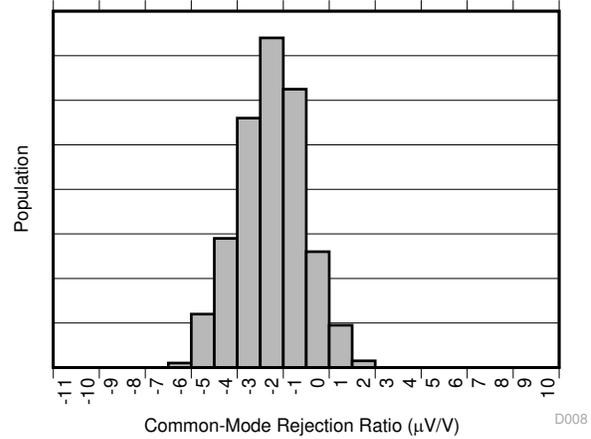**Figure 6-5. Offset Voltage vs Temperature**

Figure 6-6. Common-Mode Rejection Production Distribution A1

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

Figure 6-7. Common-Mode Rejection Production Distribution A2

Figure 6-8. Common-Mode Rejection Production Distribution A3
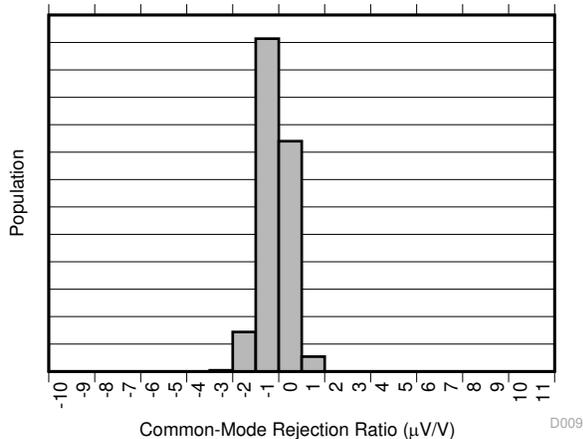
Figure 6-9. Common-Mode Rejection Production Distribution A4

Figure 6-10. Common-Mode Rejection Ratio vs Temperature
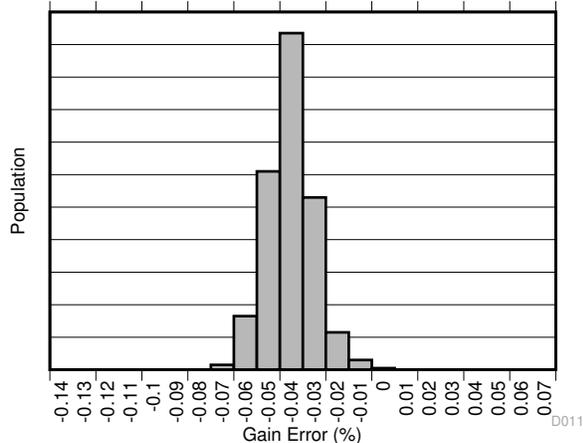
Figure 6-11. Gain Error Production Distribution A1
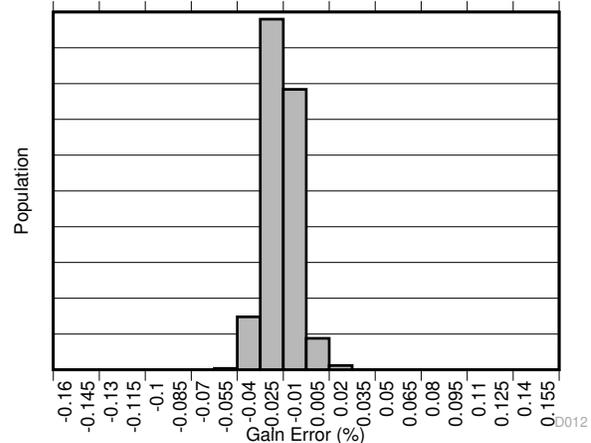
Figure 6-12. Gain Error Production Distribution A2

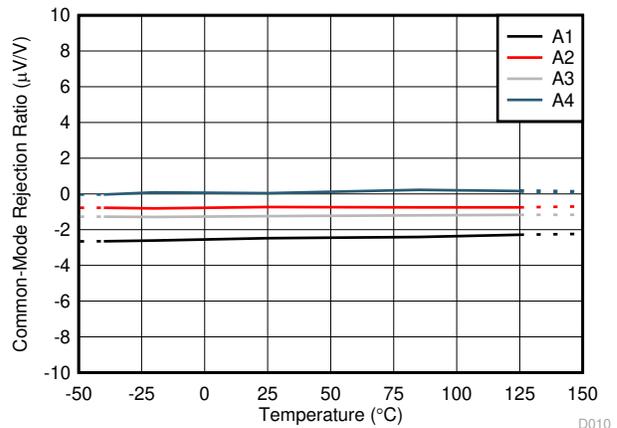Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)
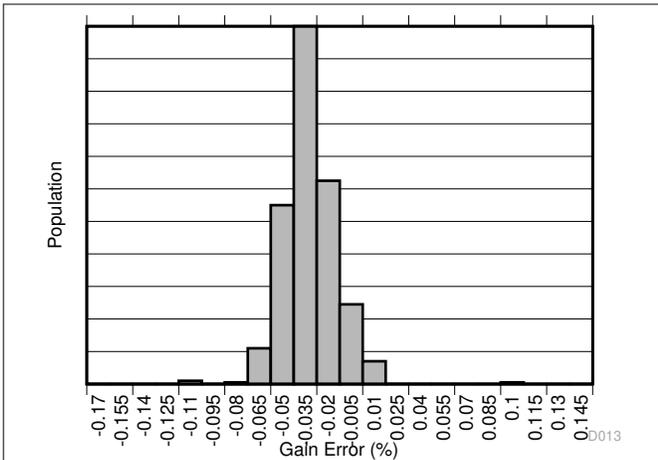
Figure 6-13. Gain Error Production Distribution A3
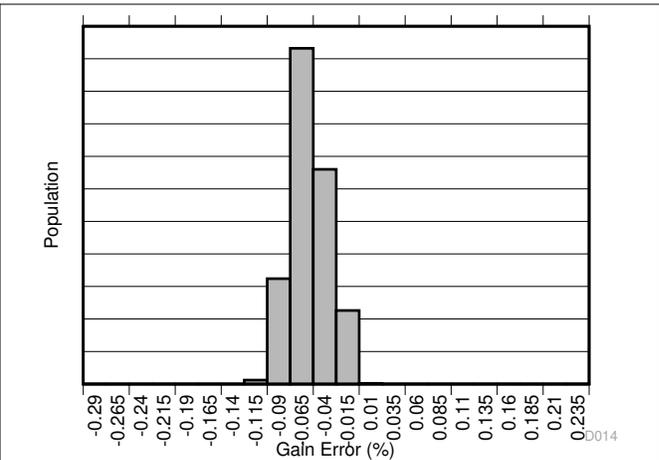
Figure 6-14. Gain Error Production Distribution A4
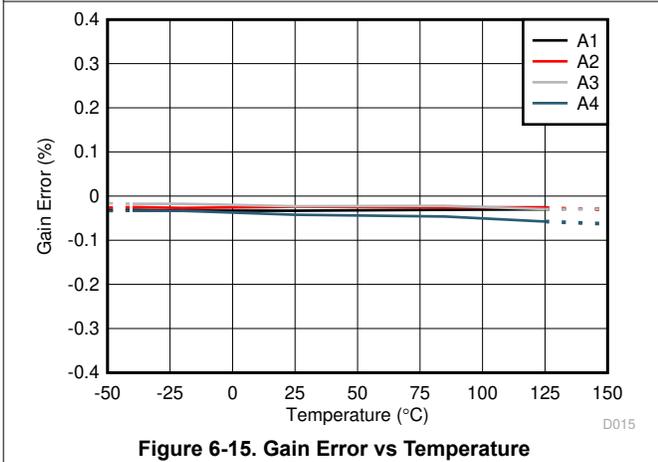
Figure 6-15. Gain Error vs Temperature
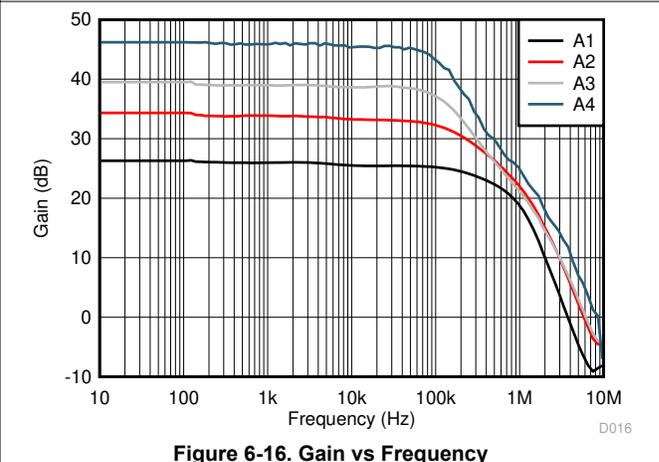
Figure 6-16. Gain vs Frequency
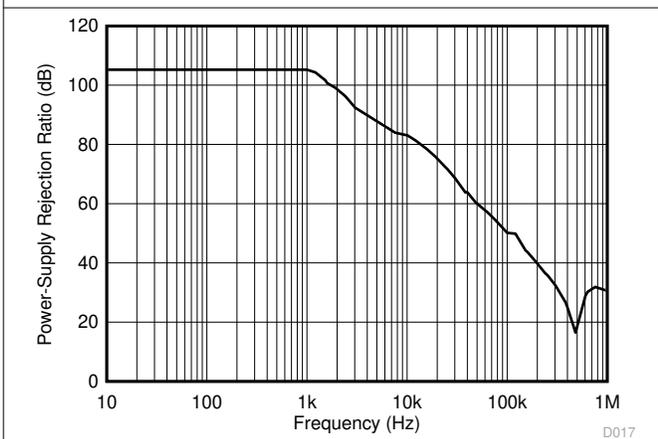
Figure 6-17. Power-Supply Rejection Ratio vs Frequency
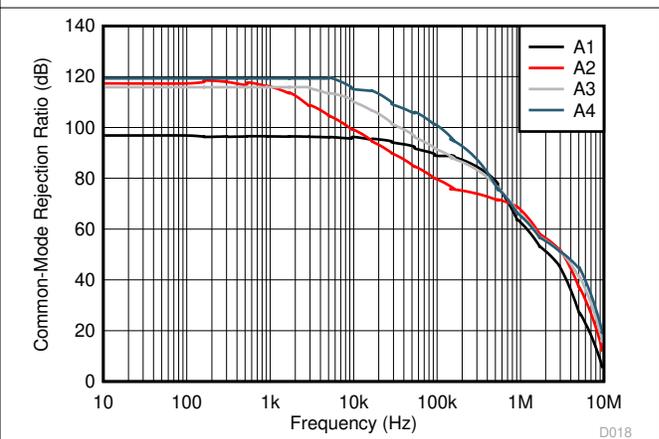
Figure 6-18. Common-Mode Rejection Ratio vs Frequency

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

Figure 6-19. Output Voltage Swing vs Output Current

Supply voltage = 5 V

Figure 6-20. Input Bias Current vs Common-Mode Voltage

Supply voltage = 0 V

Figure 6-21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

Figure 6-22. Input Bias Current vs Temperature

Figure 6-23. Quiescent Current vs Temperature (INA181-Q1)

Figure 6-24. Quiescent Current vs Temperature (INA2181-Q1)

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*
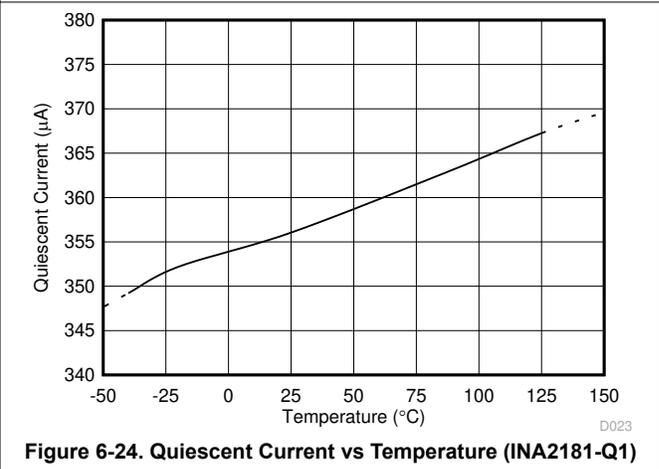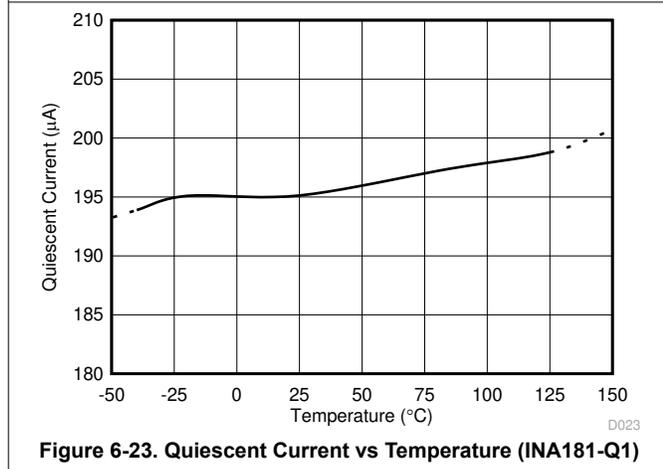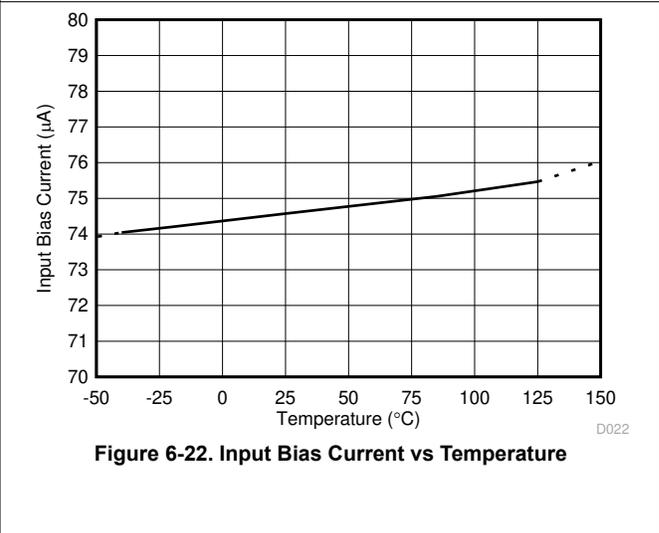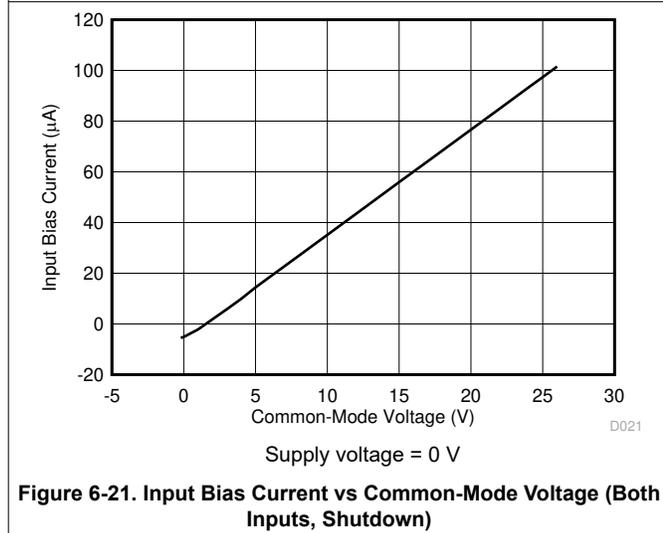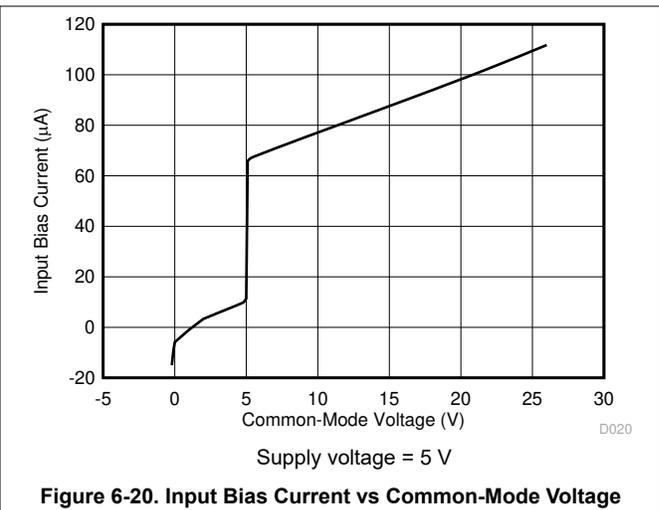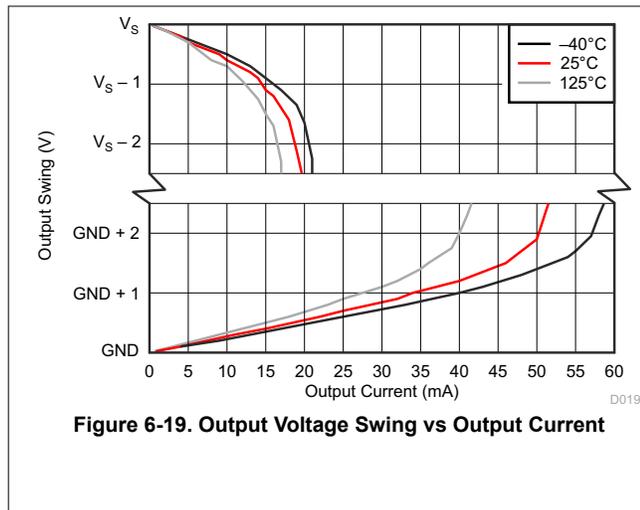
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)
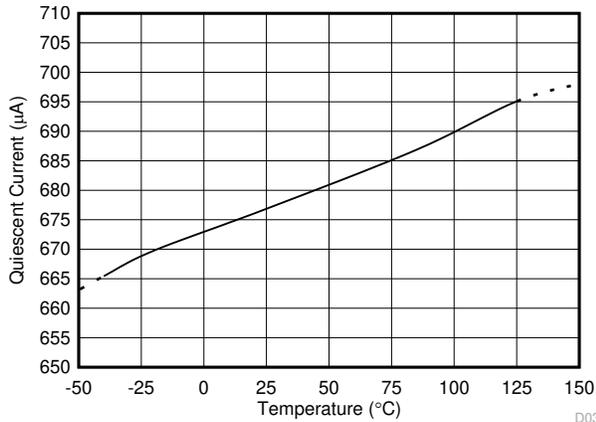
Figure 6-25. Quiescent Current vs Temperature (INA4181-Q1)
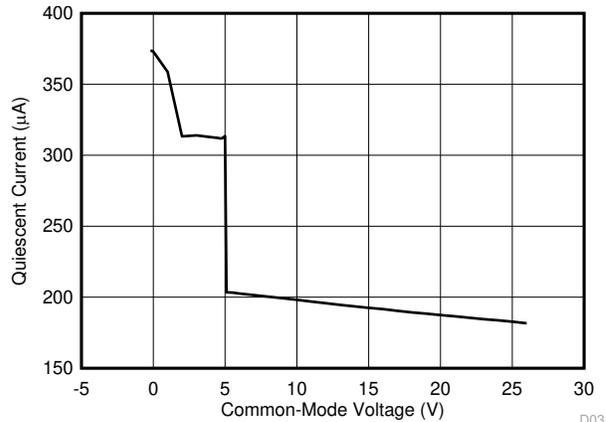
Figure 6-26. I_Q vs Common-Mode Voltage (INA181-Q1)
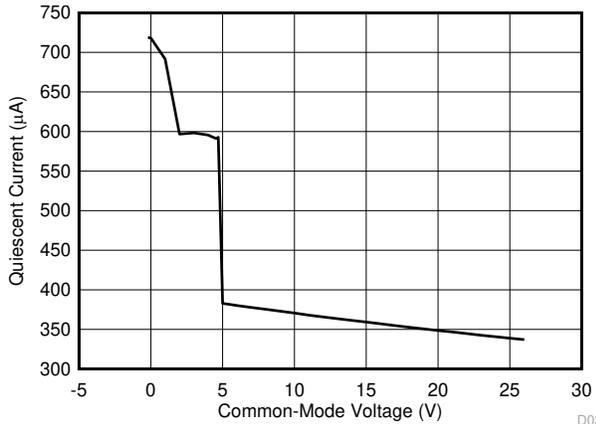
Figure 6-27. I_Q vs Common-Mode Voltage (INA2181-Q1)
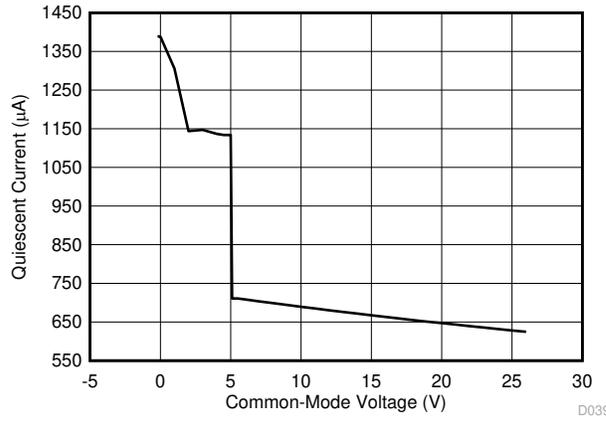
Figure 6-28. I_Q vs Common-Mode Voltage (INA4181-Q1)
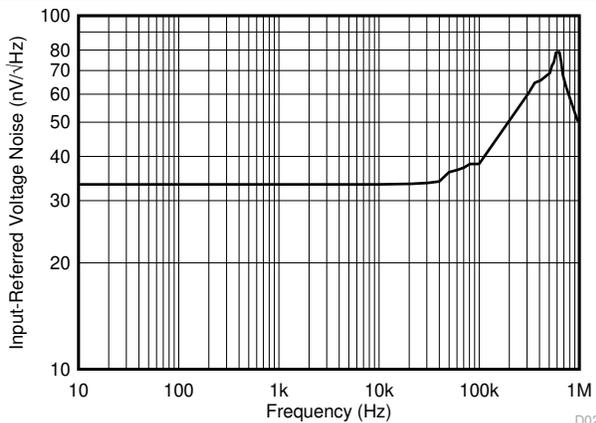
Figure 6-29. Input-Referred Voltage Noise vs Frequency (A3 Devices)
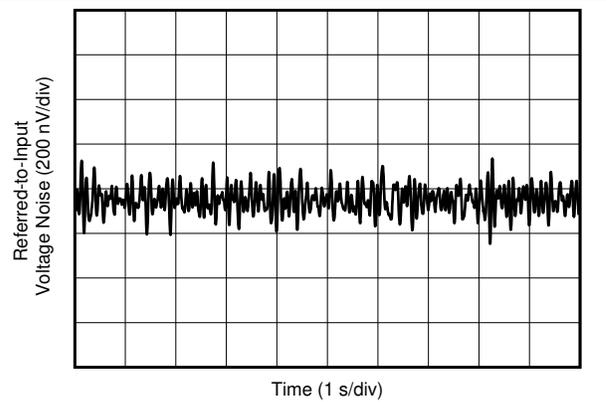
Figure 6-30. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

80-mV$_{PP}$ input step
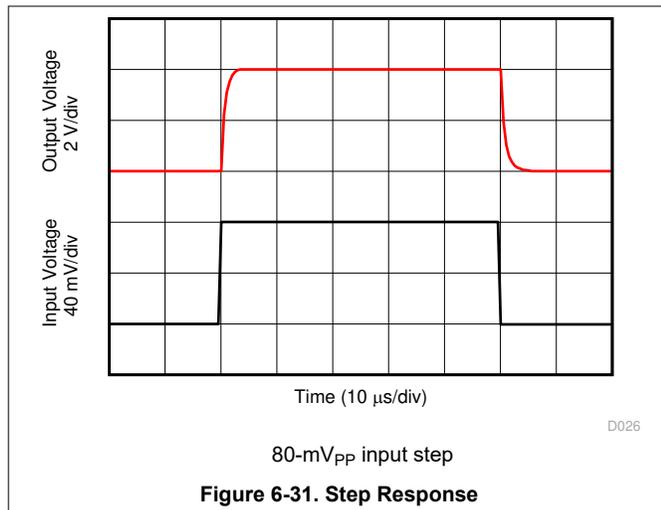
Figure 6-31. Step Response
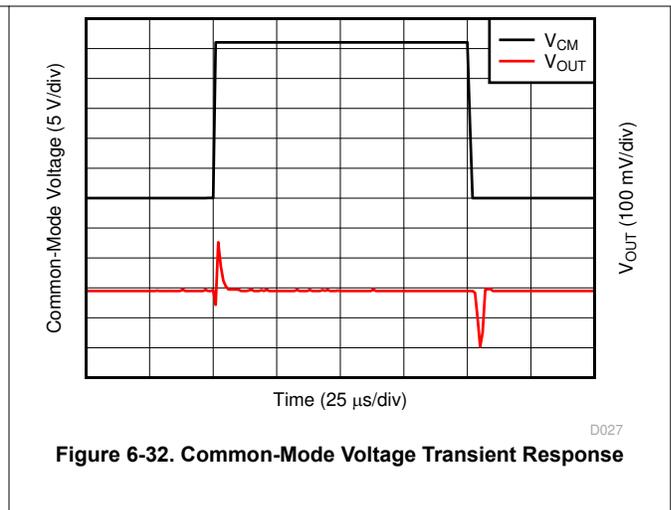
Figure 6-32. Common-Mode Voltage Transient Response
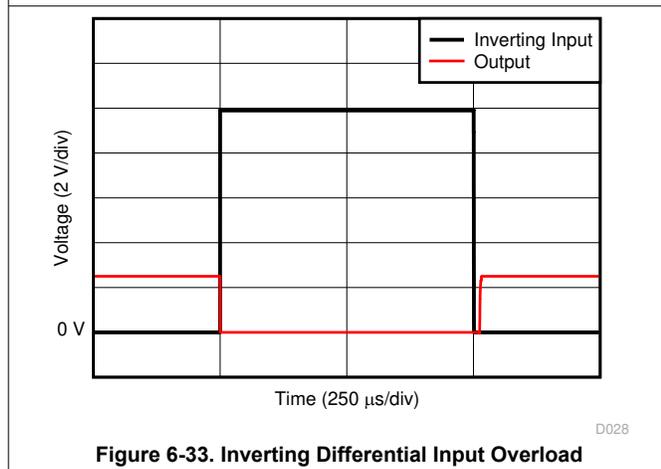
Figure 6-33. Inverting Differential Input Overload
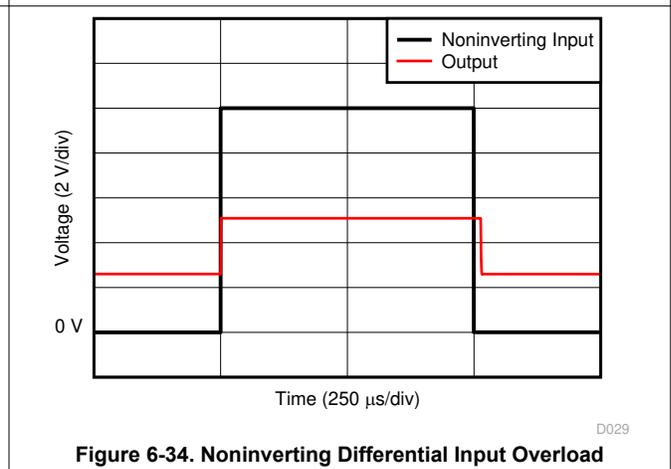
Figure 6-34. Noninverting Differential Input Overload
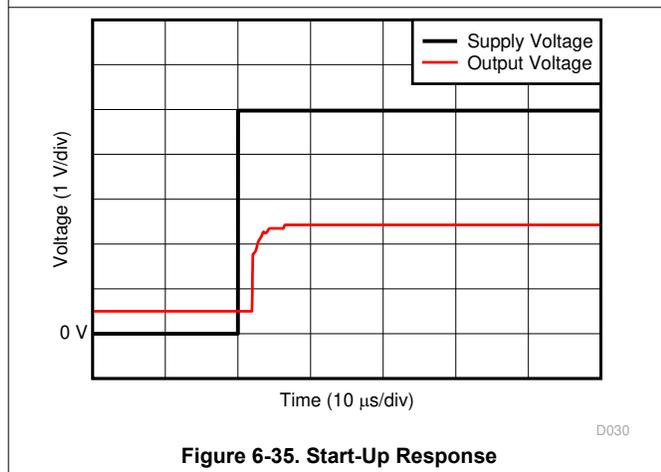
Figure 6-35. Start-Up Response
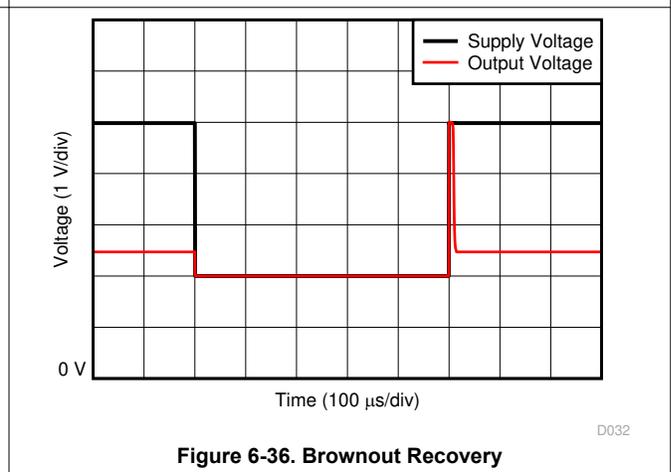
Figure 6-36. Brownout Recovery

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

Figure 6-37. Output Impedance vs Frequency

Figure 6-38. Channel Separation vs Frequency (INA2181-Q1)
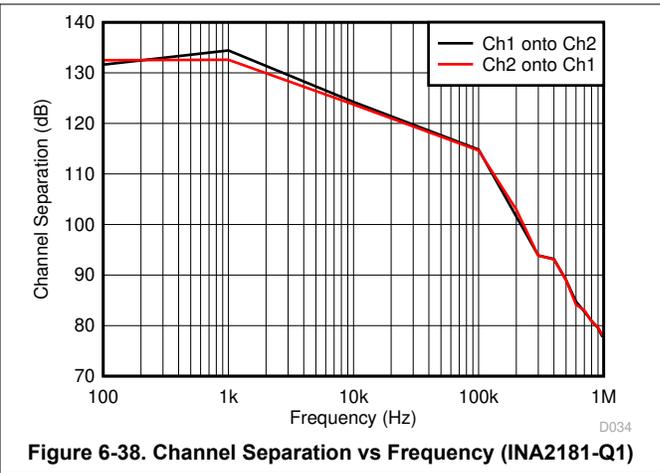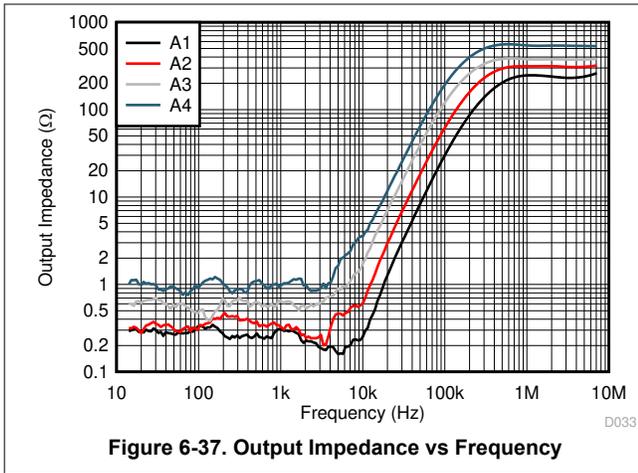
7 Detailed Description

7.1 Overview

The INA181-Q1, INA2181-Q1, and INA4181-Q1 (INAx181-Q1) are automotive-grade, 26-V common-mode, current-sensing amplifiers used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the devices can be powered from supply voltages as low as 2.7 V.

7.2 Functional Block Diagrams
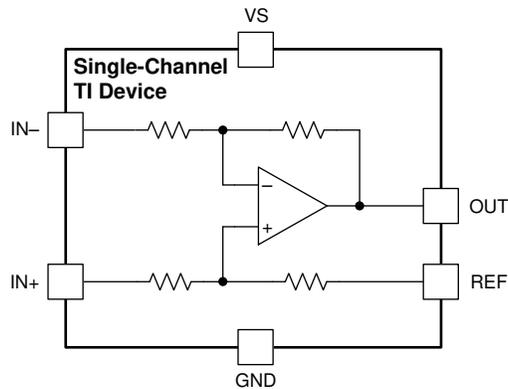
Figure 7-1. INA181-Q1 Functional Block Diagram
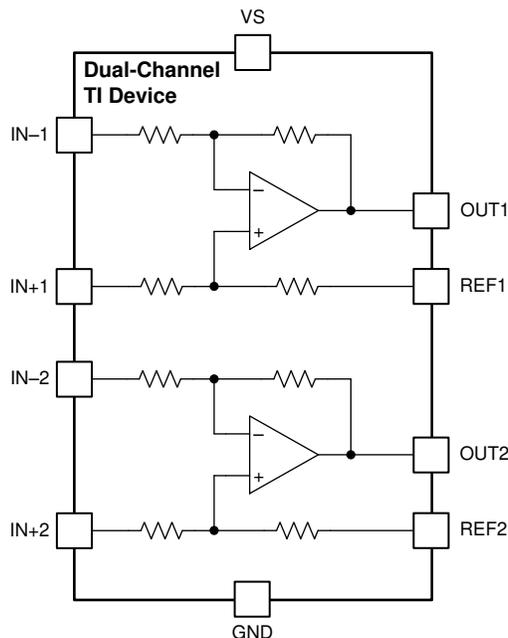
Figure 7-2. INA2181-Q1 Functional Block Diagram

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*
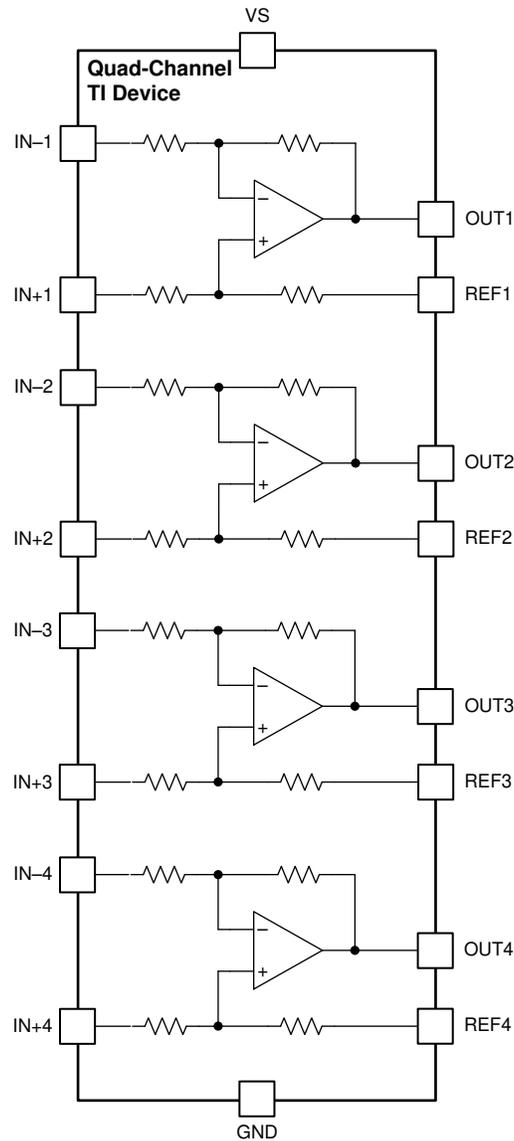
Figure 7-3. INA4181-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 High Bandwidth and Slew Rate

The INAx181-Q1 support small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, make the INAx181-Q1 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection, where the INAx181-Q1 are used with an external comparator and a reference to quickly detect when the sensed current is out of range.

7.3.2 Bidirectional Current Monitoring

The INA181-Q1 senses current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The output voltage of the current-sense amplifier is shown in Equation 1.

$$V_{OUT} = (I_{LOAD} \times R_{SENSE} \times GAIN) + V_{REF}$$ (1)

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the selected device.
- V_{REF} is the voltage applied to the REF pin.

7.3.3 Wide Input Common-Mode Voltage Range

The INAx181-Q1 support input common-mode voltages from –0.2 V to +26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. The ability to operate with common-mode voltages greater or less than V_S allow the INAx181-Q1 to be used in high-side, as well as low-side, current-sensing applications, as shown in Figure 7-4.
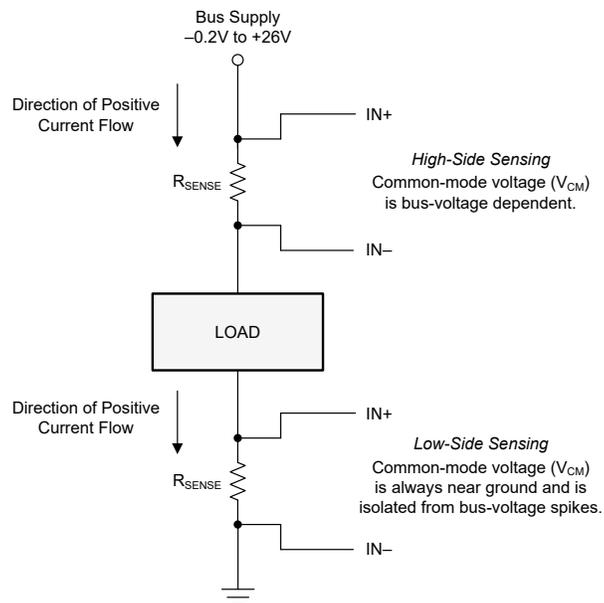
Figure 7-4. High-Side and Low-Side Sensing Connections

7.3.4 Precise Low-Side Current Sensing

When used in low-side current sensing applications the offset voltage of the INAx181-Q1 is within ±150 µV. The low offset performance of the INAx181-Q1 has several benefits. First, the low offset allows these devices to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the INAx181-Q1 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.

7.3.5 Rail-to-Rail Output Swing

The INAx181-Q1 allow linear current sensing operation with the output close to the supply rail and GND. The maximum specified output swing to the positive rail is 30 mV, and the maximum specified output swing to GND is only 5 mV. To compare the output swing of the INAx181-Q1 to an equivalent operational amplifier (op amp), the inputs are overdriven to approximate the open-loop condition specified in operational amplifier data sheets. The current-sense amplifier is a closed-loop system; therefore, the output swing to GND can be limited by the product of the offset voltage and amplifier gain during unidirectional operation (V_{REF} = 0 V).

For devices that have positive offset voltages, the swing to GND is limited by the larger of either the offset voltage multiplied by the gain or the swing to GND specified in the *Electrical Characteristics* table.

For example, in an application where the INA181A4-Q1 (gain = 200 V/V) is used for low-side current sensing and the device has an offset of 40 µV, the product of the device offset and gain results in a value of 8 mV, greater than the specified negative swing value. Therefore, the swing to GND for this example is 8 mV. If the same device has an offset of –40 µV, then the calculated zero differential signal is –8 mV. In this case, the offset helps overdrive the swing in the negative direction, and swing performance is consistent with the value specified in the *Electrical Characteristics* table.

The offset voltage is a function of the common-mode voltage as determined by the CMRR specification; therefore, the offset voltage increases when higher common-mode voltages are present. The increase in offset voltage limits how low the output voltage can go during a zero-current condition when operating at higher common-mode voltages with V_{REF} = 0 V . The typical limitation of the zero-current output voltage vs common-mode voltage for each gain option is shown in Figure 7-5.
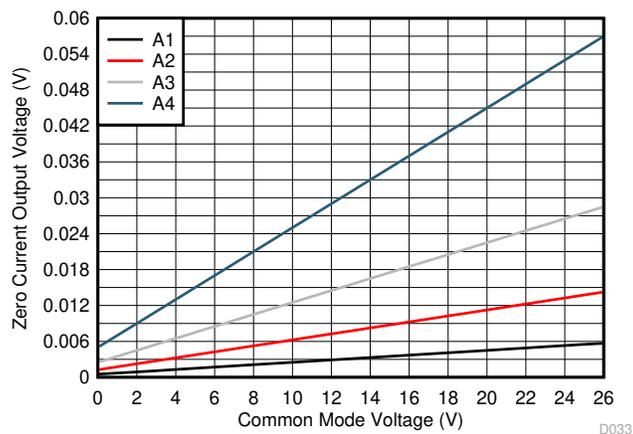
Figure 7-5. Zero-Current Output Voltage vs Common-Mode Voltage

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

7.4 Device Functional Modes

7.4.1 Normal Mode

The INAx181-Q1 are in normal operation when the following conditions are met:

- The power supply voltage (V_S) is between 2.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +26 V.
- The maximum differential input signal times gain plus V_{REF} is less than V_S minus the output voltage swing to V_S.
- The minimum differential input signal times gain plus V_{REF} is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, these devices produce an output voltage that is the *gained-up* representation of the difference voltage from IN+ to IN– plus the reference voltage at V_{REF}.

7.4.2 Unidirectional Mode

These devices can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 7-6. When the current flows from the bus supply to the load, the input signal across IN+ to IN– increases, and causes the output voltage at the OUT pin to increase.
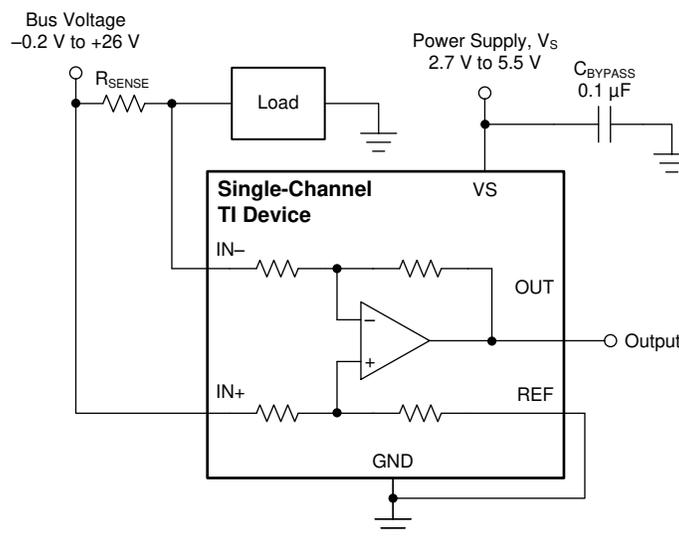
Figure 7-6. Unidirectional Application

The linear range of the output stage is limited by how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, buffer the reference voltage connected to the REF pin.

A less-frequently used output biasing method is to connect the REF pin to the power-supply voltage, V_S. This method results in the output voltage saturating at 200 mV less than the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed V_S.

7.4.3 Bidirectional Mode

The INAx181-Q1 are bidirectional, current-sense amplifiers capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flowing through the resistor can change directions.
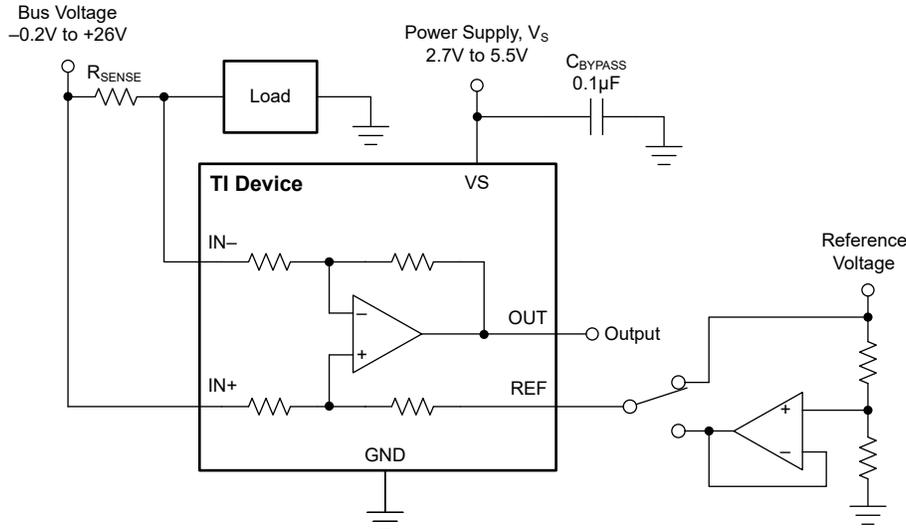
Figure 7-7. Bidirectional Application

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 7-7. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

7.4.4 Input Differential Overload

If the differential input voltage ($V_{IN+} − V_{IN–}$) multiplied by the gain exceeds the voltage swing specification, the INAx181-Q1 drives the output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INAx181-Q1 returns to the expected value approximately 20 µs after the fault condition is removed.

When the INAx181-Q1 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not surpassed. Following these guidelines, the INAx181-Q1 output maintains polarity, and phase reversal does not occur.

7.4.5 Shutdown Mode

Although the INAx181-Q1 do not have a shutdown pin, the low power consumption of these devices allows the output of a logic gate or transistor switch to power the INAx181-Q1. This gate or switch turns on and off the INAx181-Q1 power-supply quiescent current.

However, in current shunt monitoring applications, the amount of current drained from the shunt circuit in shutdown conditions is also a concern. Evaluating this current drain involves considering the simplified schematic of the INAx181-Q1 in shutdown mode, as shown in Figure 7-8.
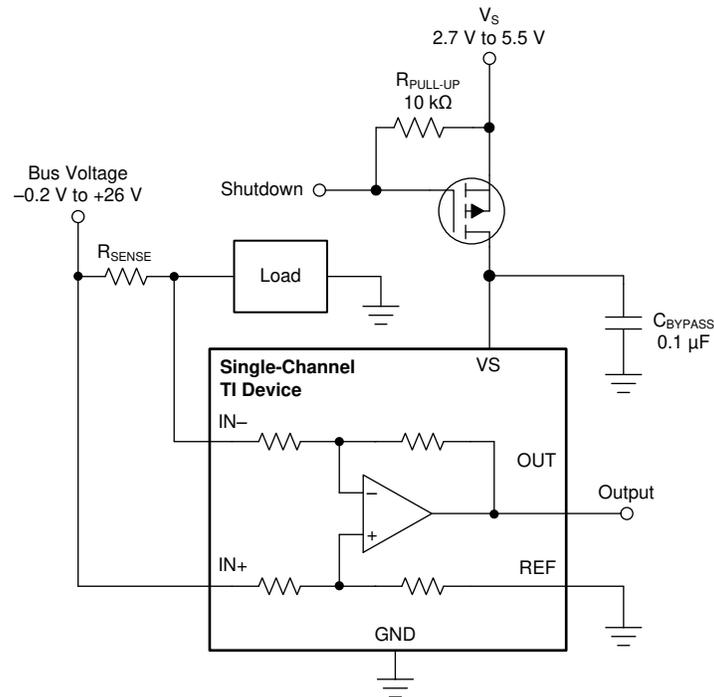
Figure 7-8. Basic Circuit to Shut Down the INA181-Q1 With a Grounded Reference

There is typically more than 500 kΩ of impedance (from the combination of 500-kΩ feedback and input gain set resistors) from each input of the INAx181-Q1 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the voltage at the connection. For example, if the REF pin is grounded, the calculation of the effect of the 500 kΩ impedance from the shunt to ground is straightforward. However, if the reference is powered while the INAx181-Q1 is in shutdown mode, the input current is determined by the 500-kΩ impedance and the voltage difference between the positive input and the voltage applied to the reference voltage.

Regarding the 500-kΩ path to the output pin, the output stage of a disabled INAx181-Q1 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 500-kΩ resistor.

As long as the shunt common-mode voltage is greater than V_S when the device is powered up, there is an additional and well-matched 55-µA typical current that flows in each of the inputs. If less than V_S, the common-mode input currents are negligible, and the only current effects are the result of the 500-kΩ resistors.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INAx181-Q1 amplify the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed in previous sections.

8.1.1 Basic Connections

Figure 8-1 shows the basic connections of the INA181-Q1. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.
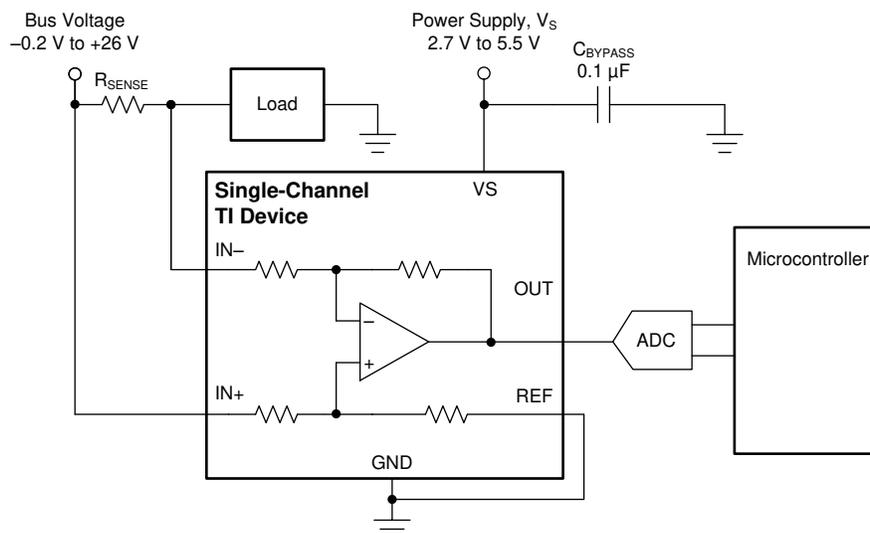
NOTE: To help eliminate ground offset errors between the device and the analog-to-digital converter (ADC), connect the REF pin to the ADC reference input and then to ground. For best performance, use an RC filter between the output of the INAx181-Q1 and the ADC. See *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* application note for more details.

Figure 8-1. Basic Connections for the INA181-Q1

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

8.1.2 R$_{SENSE}$ and Device Gain Selection

The accuracy of the INAx181-Q1 is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application. The INAx181-Q1 have typical input bias currents of 75 µA for each input when operated at a 12-V common-mode voltage input. When large current-sense resistors are used, these bias currents cause increased offset error and reduced common-mode rejection. Therefore, using current-sense resistors larger than a few ohms is generally not recommended for applications that require current-monitoring accuracy. Another common restriction on the value of the current-sense resistor is the maximum allowable power dissipation that is budgeted for the resistor. Equation 2 gives the maximum value for the current sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2}$$

(2)

where:

- PD$_{MAX}$ is the maximum allowable power dissipation in R$_{SENSE}$.
- I$_{MAX}$ is the maximum current that flows through R$_{SENSE}$.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V$_S$, and device swing to rail limitations. To make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 3 provides the maximum values of R$_{SENSE}$ and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} - V_{REF}$$

(3)

where:

- I$_{MAX}$ is the maximum current that flows through R$_{SENSE}$.
- GAIN is the gain of the current sense-amplifier.
- V$_{SP}$ is the positive output swing specified in the data sheet.
- V$_{REF}$ is the externally applied voltage on the REF pin.

To avoid positive output swing limitations when selecting the value of R$_{SENSE}$, there is always a trade-off between the value of the sense resistor and the gain of the device to consider. If the sense resistor selected for the maximum power dissipation is too large, then selecting a lower-gain device to avoid positive swing limitations is possible.

The negative swing limitation places a limit on how small of a sense resistor can be used in a given application. Equation 4 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} - V_{REF}$$

(4)

where:

- I$_{MIN}$ is the minimum current that flows through R$_{SENSE}$.
- GAIN is the gain of the current sense amplifier.
- V$_{SN}$ is the negative output swing of the device (see *Rail-to-Rail Output Swing*).
- V$_{REF}$ is the externally applied voltage on the REF pin.

In addition to adjusting the offset and gain, the voltage applied to the REF pin can be slightly increased to avoid negative swing limitations.

8.1.3 Signal Filtering

Provided that the INAx181-Q1 output is connected to a high-impedance input, the best location to filter is at the device output using a simple RC network from OUT to GND. Filtering at the output attenuates high-frequency

disturbances in the common-mode voltage, differential input signal, and INAx181-Q1 power-supply voltage. If filtering at the output is not possible, or filtering of only the differential input signal is required, required, then apply a filter at the input pins of the device. Figure 8-2 provides an example of how a filter can be used on the input pins of the device.
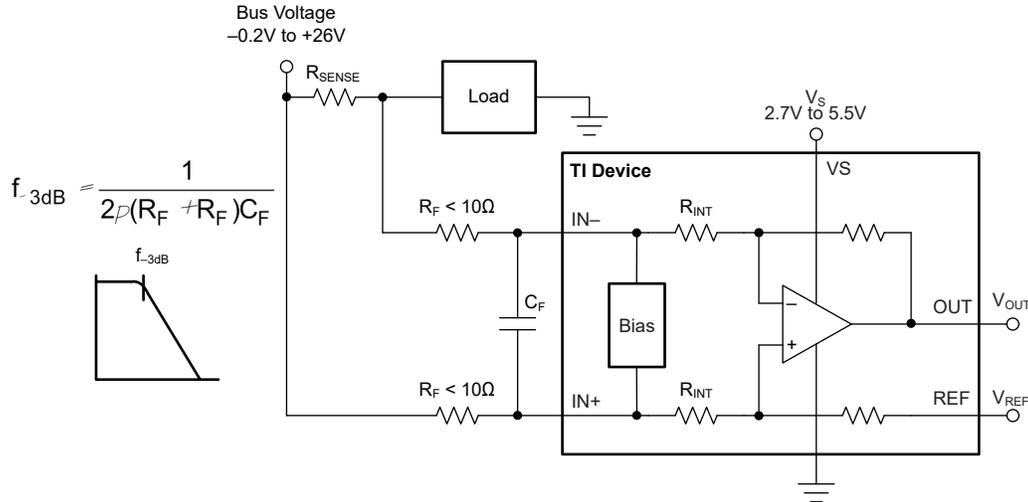
Figure 8-2. Filter at Input Pins

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in Figure 8-2 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using Equation 6, where the gain error factor is calculated using Equation 5.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}, as shown in Figure 8-2. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given using Equation 5:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \tag{5}$$

where:

- R_{INT} is the internal input resistor.
- R_F is the external series resistance.

With the adjustment factor from Equation 5, including the device internal input resistance, this factor varies with each gain version, as shown in Table 8-1. Each individual device gain error factor is shown in Table 8-2.

Table 8-1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INAx181A1-Q1	20	25
INAx181A2-Q1	50	10
INAx181A3-Q1	100	5
INAx181A4-Q1	200	2.5

Table 8-2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INAx181A1-Q1	$\dfrac{25000}{(21 \times R_F) + 25000}$
INAx181A2-Q1	$\dfrac{10000}{(9 \times R_F) + 10000}$
INAx181A3-Q1	$\dfrac{1000}{R_F + 1000}$
INAx181A4-Q1	$\dfrac{2500}{(3 \times R_F) + 2500}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \tag{6}$$

For example, using an INA181A2-Q1 and the corresponding gain error equation from Table 8-2, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 6, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

8.1.4 Summing Multiple Currents

The outputs of the INA2181-Q1 are easily summed by connecting the output of one channel to the reference input of a second channel. The circuit configuration shown in Figure 8-3 is an easy method to achieve current summing. To correctly sum multiple output currents, the values for the current sense resistor R_{SENSE} must be the same for all channels.

$$V_{OUT2} = (I_{LOAD1} + I_{LOAD2}) \times R_{SENSE} \times GAIN$$
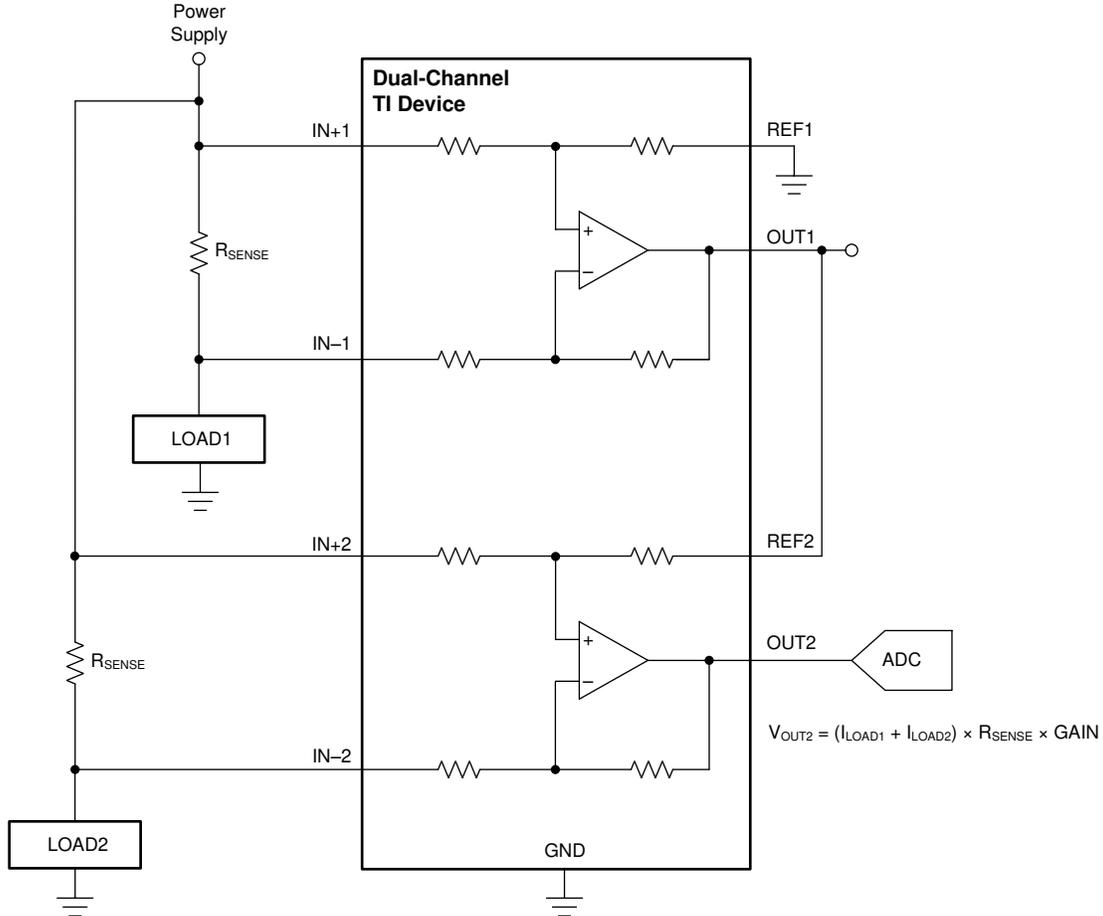
Figure 8-3. Summing Multiple Currents

Connect the output of one channel of the INA2181-Q1 to the reference input of the other channel. Use the reference input of the first circuit to set the reference of the final summed output operating point. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

An example output response of a summing configuration is shown in Figure 8-4. The reference pin of the first circuit is connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.

Time (4 ms/div)

$V_{REF} = 0\ V$
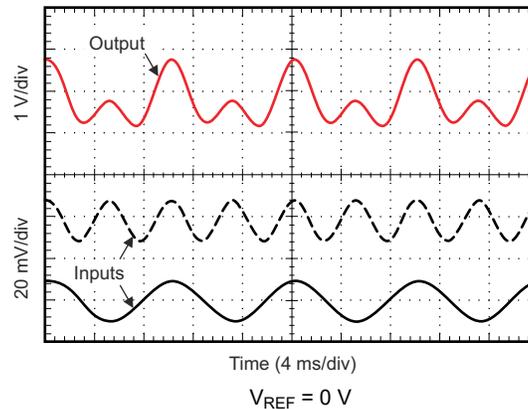
Figure 8-4. Current Summing Application Output Response (A2 Devices)

8.1.5 Detecting Leakage Currents

Occasionally, the need arises to confirm that the current going into a load is identical to the current coming out of a load; typically, as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing, except that the two amplifiers have the inputs connected opposite of each other. To correctly detect leakage currents, the values for the current sense resistor R_{SENSE} must be the same for all channels. Provide an external reference voltage to the REF1 input to allow bidirectional leakage current detection.

If the current into a load is equal to the current out of the load, then the voltage at OUT2 is the same as the applied voltage to REF1. To enable accurate differences between the two currents, a reference voltage must be applied. The reference voltage prevents the output of the device from being driven to ground, and also enables detection if the current into the load is either greater than or less than the current coming out of the load.

For current differencing, the dual-channel INA2181-Q1 must have the inputs connected opposite to each other, as shown in Figure 8-5. The reference input of the first channel sets the output quiescent level for all the devices in the string. Connect the output of the first channel to the reference input of the second channel. The reference input of the first channel sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current into and out of a load do not match.
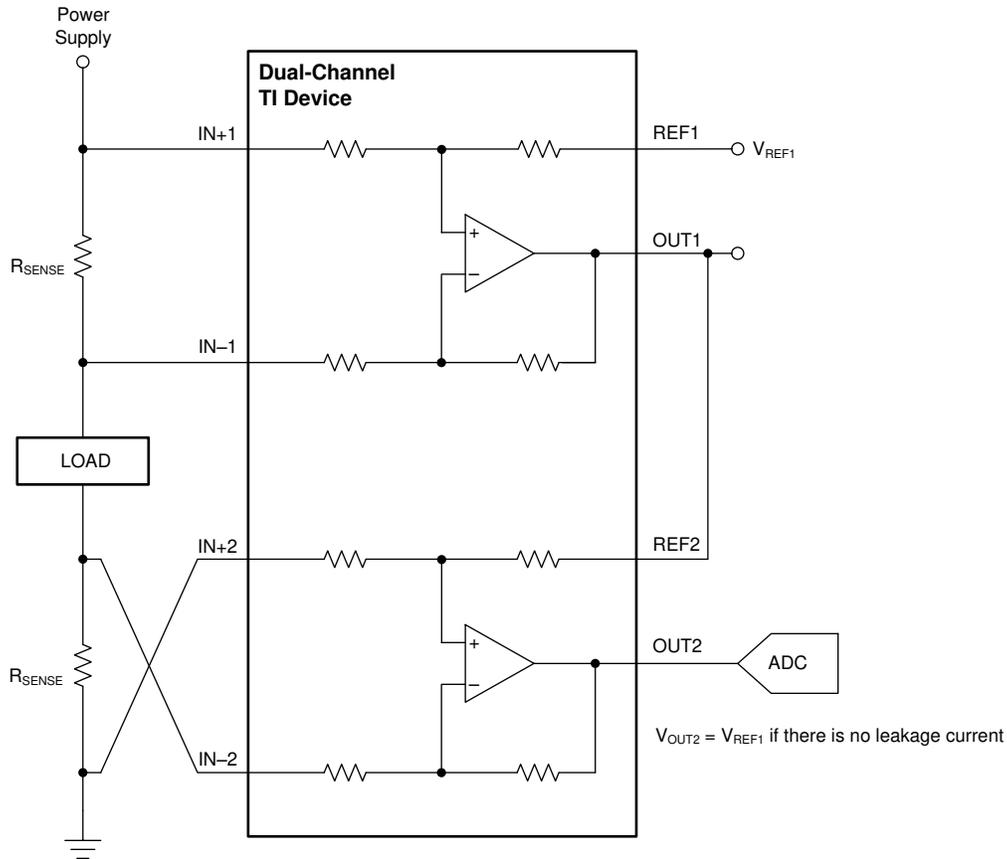
Figure 8-5. Detecting Leakage Currents

An example output response of a difference configuration is shown in Figure 8-6. The reference pin of the first channel is connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out-of-phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.

V_{REF} = 2.048 V
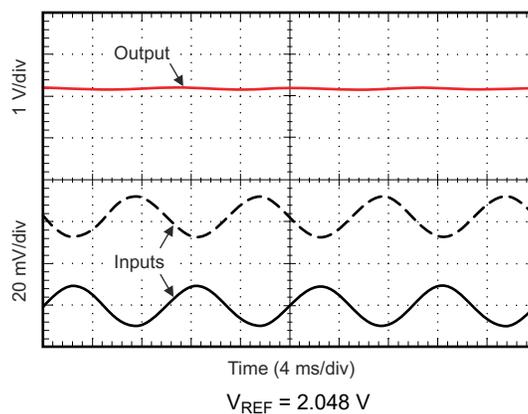
Figure 8-6. Current Differencing Application Output Response (A2 Devices)

8.2 Typical Application

One application for the INAx181-Q1 is to monitor bidirectional currents. Bidirectional currents are present in systems that have to monitor currents in both directions; common examples are monitoring the charging and discharging of batteries and bidirectional current monitoring in motor control. The device configuration for bidirectional current monitoring is shown in Figure 8-7. Applying stable REF pin voltage closer to the middle of device supply voltage allows both positive- and negative-current monitoring, as shown in this configuration. Configure the INAx181-Q1 to monitor unidirectional currents by grounding the REF pin.
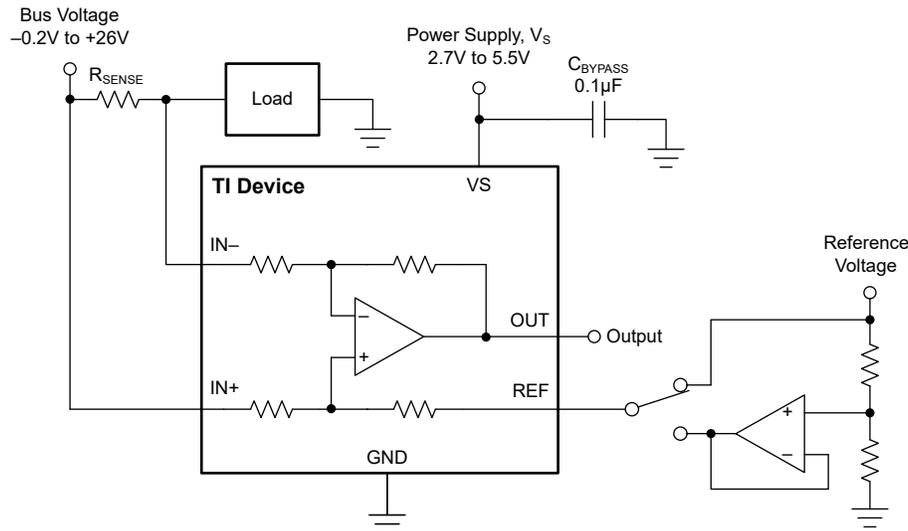
Figure 8-7. Measuring Bidirectional Current

8.2.1 Design Requirements

The design requirements for the circuit shown in Figure 8-7, are listed in Table 8-3.

Table 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage, V_S	5 V
Bus supply rail, V_{CM}	12 V
R_{SENSE} power loss	< 450 mW
Maximum sense current, I_{MAX}	±20 A
Current sensing error	Less than 3.5% at maximum current, T_J = 25°C
Small-signal bandwidth	> 100 kHz

8.2.2 Detailed Design Procedure

The maximum value of the current sense resistor is calculated based on the maximum power loss requirement. By applying Equation 2, the maximum value of the current-sense resistor is calculated to be 1.125 mΩ. This is the maximum value for sense resistor R_{SENSE}; therefore, select R_{SENSE} to be 1 mΩ because this value is the closest standard resistor value that meets the power-loss requirement.

The next step is to select the appropriate gain and reduce R_{SENSE}, if needed, to keep the output signal swing within the V_S range. The design requirements call for bidirectional current monitoring; therefore, a voltage between 0 and V_S must be applied to the REF pin. The bidirectional currents monitored are symmetric around 0 (that is, ±20 A); therefore, the ideal voltage to apply to V_{REF} is V_S / 2 or 2.5 V. If the positive current is greater than the negative current, using a lower voltage on V_{REF} has the benefit of maximizing the output swing for the given range of expected currents. Using Equation 3, and given that I_{MAX} = 20 A, R_{SENSE} = 1 mΩ, and V_{REF} = 2.5 V, the maximum current-sense gain calculated to avoid the positive swing-to-rail limitations on the output is 122.5. Likewise, using Equation 4 for the negative-swing limitation results in a maximum gain of 124.75.

Selecting the gain-of-100 device maximizes the output range while staying within the output swing range. If the maximum calculated gains are slightly less than 100, the value of the current-sense resistor can be reduced to keep the output from hitting the output-swing limitations.

To calculate the accuracy at peak current, the two factors that must be determined are the gain error and the offset error. The gain error of the INAx181-Q1 is specified to be a maximum of 1%. The error due to the offset is constant, and is specified to be 500 µV (maximum) for the conditions where V_{CM} = 12 V and V_S = 5 V. Using Equation 7, the percentage error contribution of the offset voltage is calculated to be 2.5%, with total offset error = 500 µV, R_{SENSE} = 1 mΩ, and I_{SENSE} = 20 A.

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \tag{7}$$

One method of calculating the total error is to add the gain error to the percentage contribution of the offset error. However, in this case, the gain error and the offset error do not have an influence or correlation to each other. A more statistically-accurate method of calculating the total error is to use the RSS sum of the errors, as shown in Equation 8:

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \tag{8}$$

After applying Equation 8, the total current sense error at maximum current is calculated to be 2.7%, and that is less than the design example requirement of 3.5%.

The INA181A3-Q1 (gain = 100) also has a bandwidth of 150 kHz that meets the small-signal bandwidth requirement of 100 kHz. If higher bandwidth is required, lower-gain devices can be used at the expense of either reduced output voltage range or an increased value of R_{SENSE}.

8.2.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 8-8. With the REF pin connected to a reference voltage (2.5 V in this case), the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals, and falls below the reference voltage for negative differential input signals.
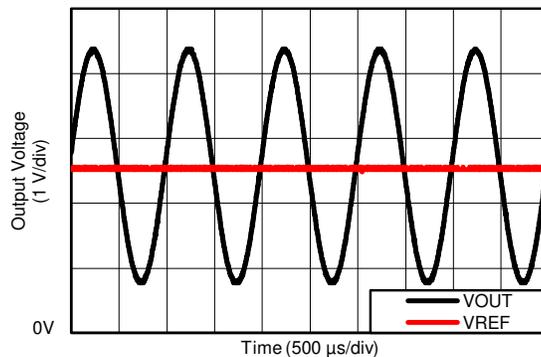
Figure 8-8. Bidirectional Application Output Response

8.3 Power Supply Recommendations

The input circuitry of the INAx181-Q1 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the VS pin. The INAx181-Q1 also withstand the full

differential input signal range up to 26 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin.

8.3.1 Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INAx181-Q1 can be used in circuits that are subjected to transients higher than 26 V, such as automotive applications. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode. See Figure 8-9. Keep these resistors as small as possible; most often, around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Filtering* section. This circuit limits on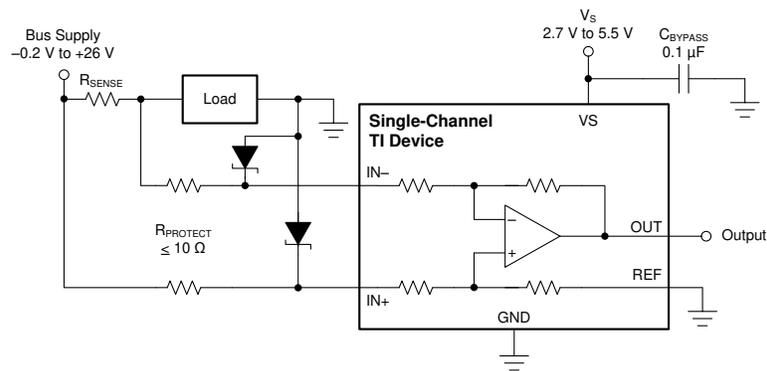ly short-term transients; therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

Figure 8-9. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in Figure 8-10. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in Figure 8-9 and Figure 8-10, the total board area required by the INAx181-Q1 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.
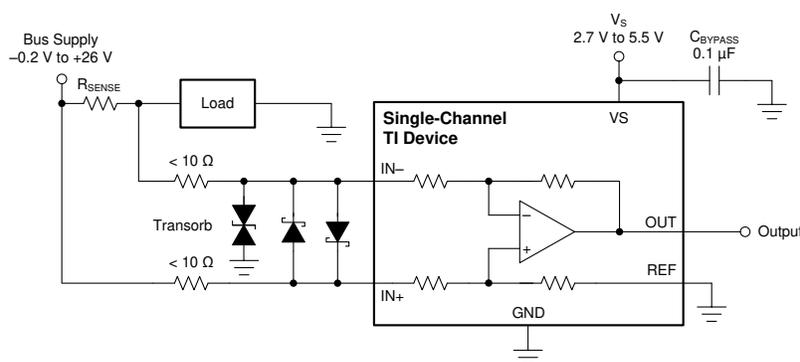
Figure 8-10. Transient Protection Using a Single Transorb and Input Clamps

For more information, see the *Current Shunt Monitor With Transient Robustness* reference design.

Product Folder Links: *INA181-Q1 INA2181-Q1 INA4181-Q1*

8.4 Layout

8.4.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very-low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current sense resistor to the device, keep the trace lengths as close as possible to minimize any impedance mismatch..

8.4.2 Layout Example
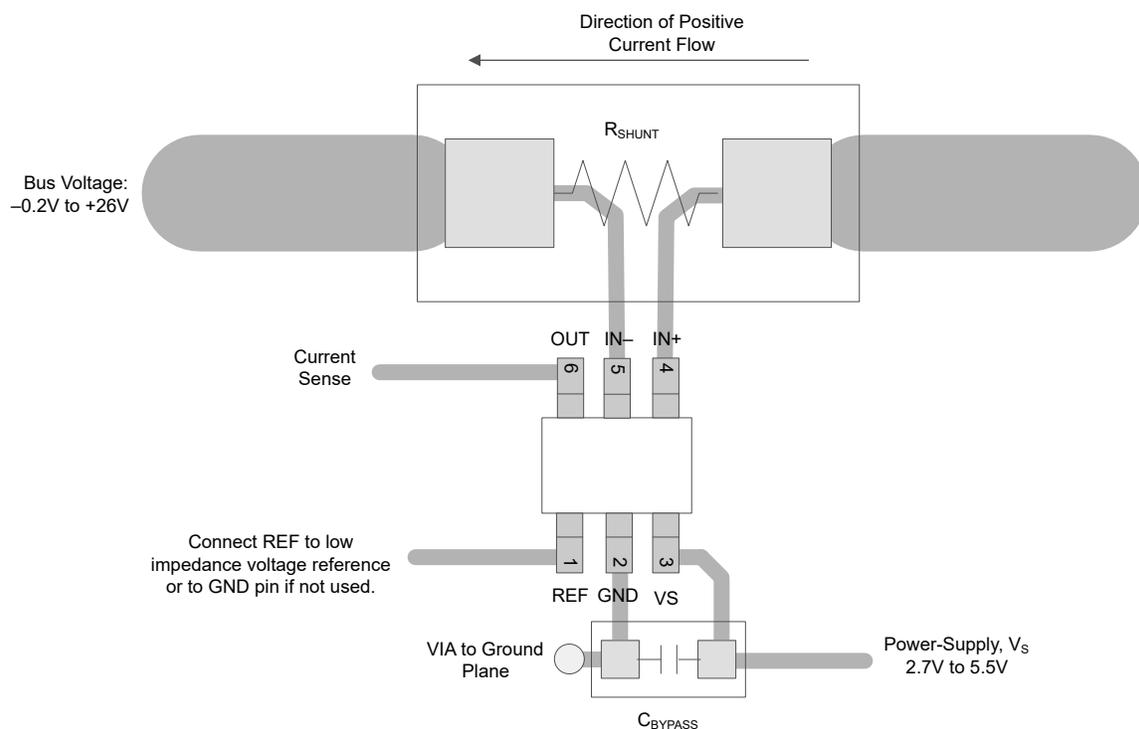
Figure 8-11. Single-Channel Recommended Layout (SC70)
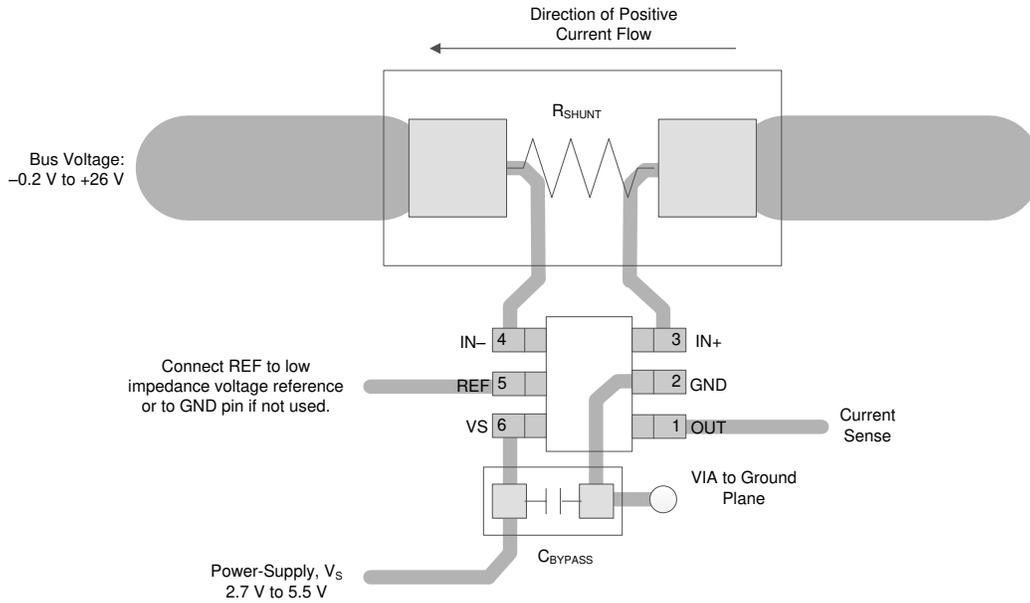
Figure 8-12. Single-Channel Recommended Layout (SOT-23)
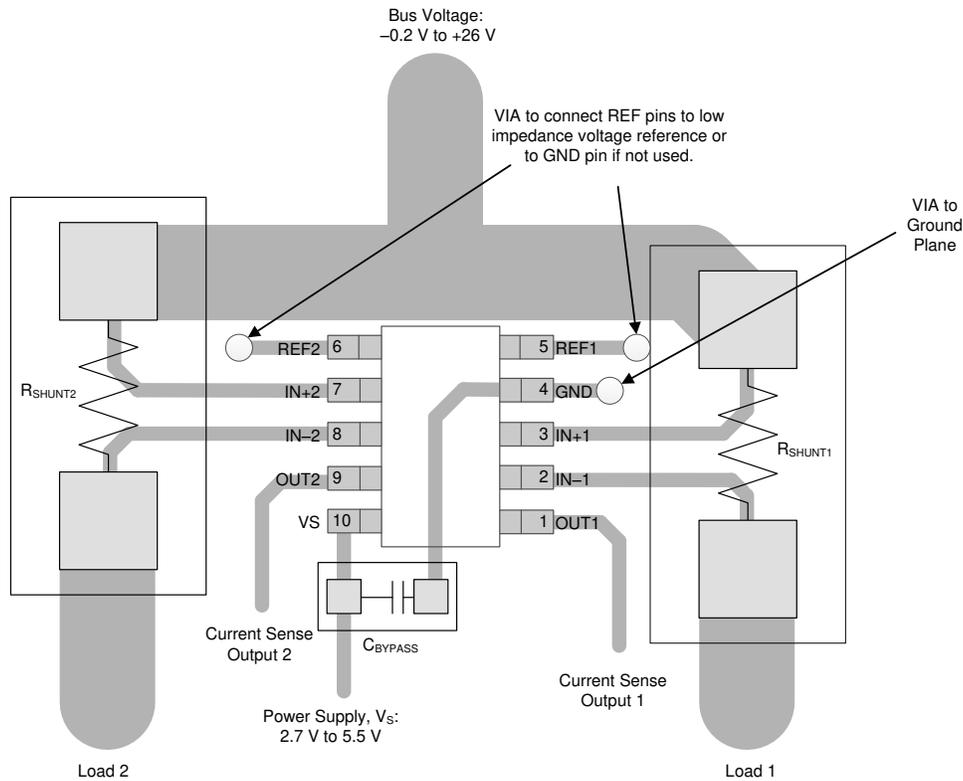
Figure 8-13. Dual-Channel Recommended Layout (VSSOP)
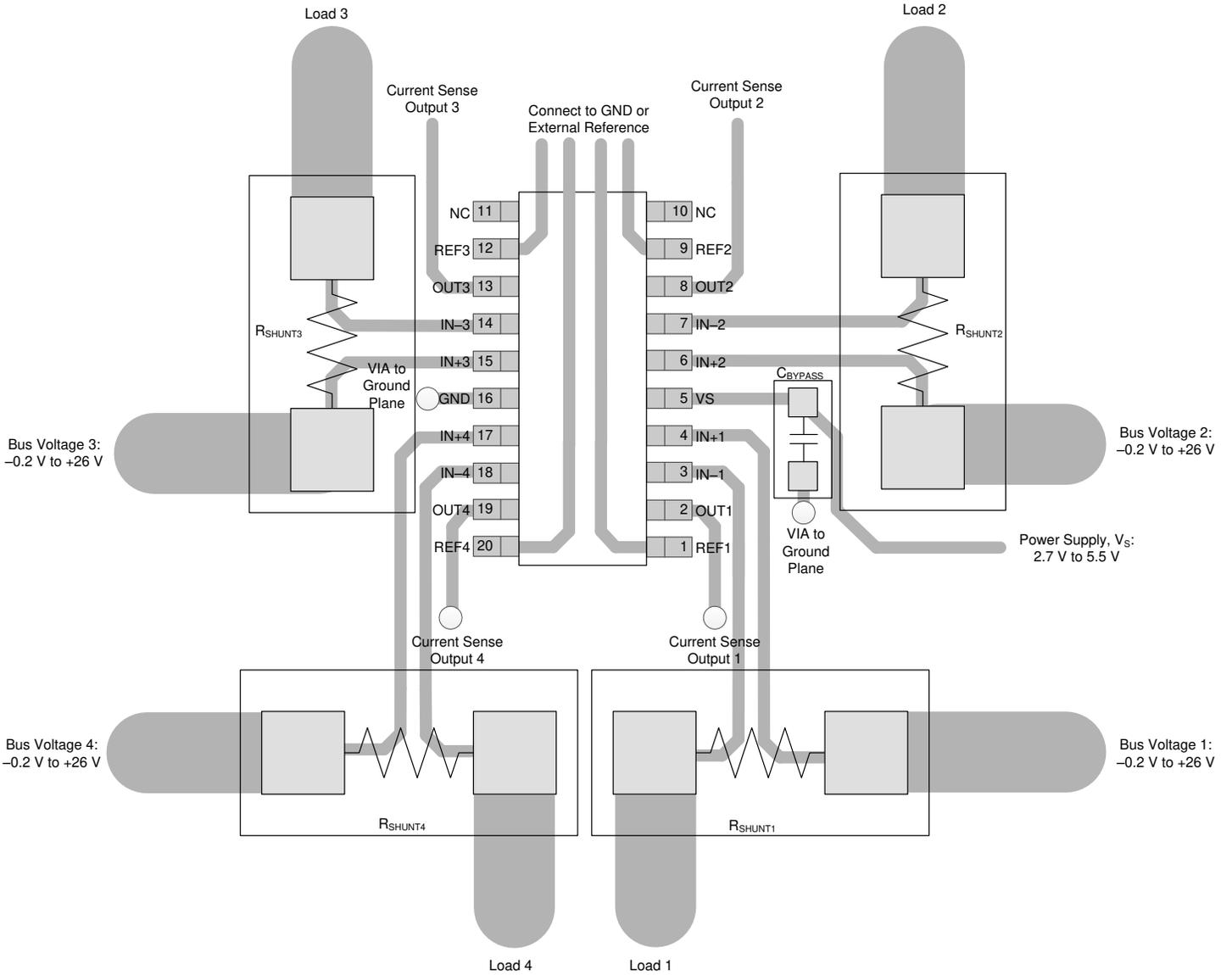
Figure 8-14. Quad-Channel Recommended Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

• Texas Instruments, *Current Shunt Monitor With Transient Robustness*, reference design

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

• Texas Instruments, *INA180-181EVM*, user's guide
• Texas Instruments, *INA2180-2181EVM*, user's guide
• Texas Instruments, *INA4180-4181EVM*, user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA181A1QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N13
INA181A1QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N13
INA181A1QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q4
INA181A1QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q4
INA181A2QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MS3
INA181A2QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MS3
INA181A2QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q5
INA181A2QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q5
INA181A3QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1MT3
INA181A3QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MT3
INA181A3QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q6
INA181A3QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q6
INA181A4QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MU3
INA181A4QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MU3
INA181A4QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q7
INA181A4QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1Q7
INA2181A1QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O56
INA2181A1QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O56
INA2181A2QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O66
INA2181A2QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O66
INA2181A3QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O76
INA2181A3QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O76
INA2181A4QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O86
INA2181A4QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O86
INA4181A1QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A1Q
INA4181A1QPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A1Q
INA4181A2QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A2Q
INA4181A2QPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A2Q
INA4181A3QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A3Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA4181A3QPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A3Q
INA4181A4QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A4Q
INA4181A4QPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A4Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF INA181-Q1, INA2181-Q1, INA4181-Q1 :

• Catalog : INA181, INA2181, INA4181

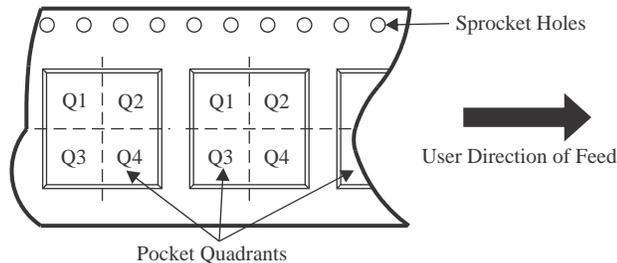NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA181A1QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA181A1QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA181A2QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA181A2QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA181A3QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA181A3QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA181A4QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA181A4QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA2181A1QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A2QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A4QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA4181A1QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A2QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A3QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A4QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

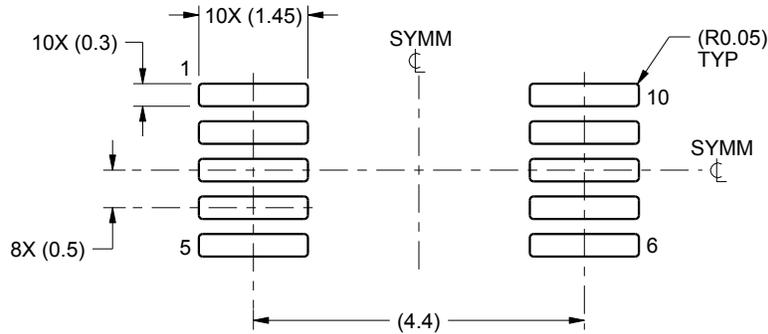| Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA181A1QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA181A1QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA181A2QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA181A2QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA181A3QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA181A3QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA181A4QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA181A4QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA2181A1QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A2QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A3QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A4QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA4181A1QPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0
INA4181A2QPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0
INA4181A3QPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0
INA4181A4QPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0
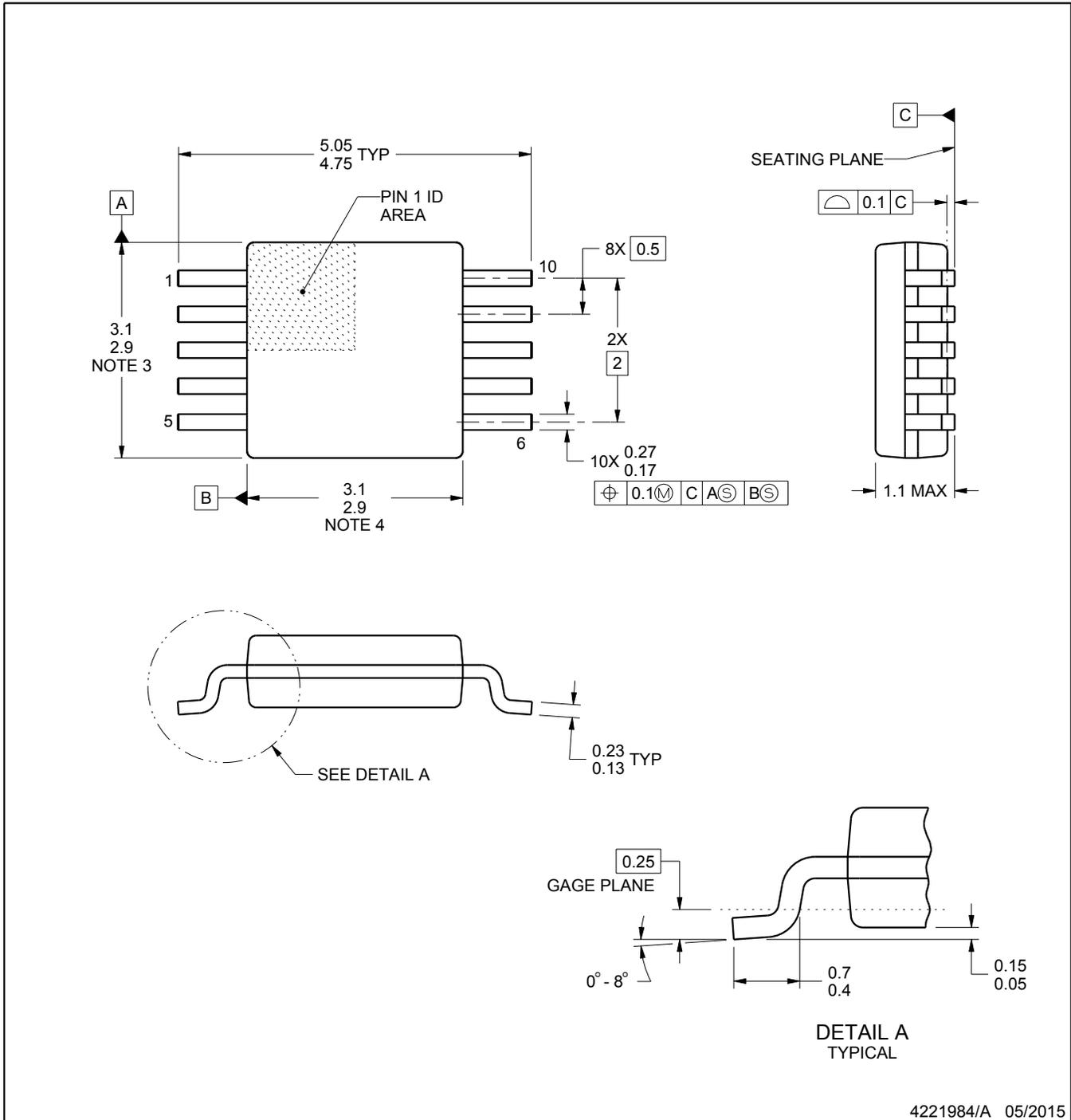
4221984/A   05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

TEXAS
INSTRUMENTS
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10X (1.45)

10X (0.3)

1

SYMM

(R0.05)
TYP

10

SYMM

8X (0.5)

5

6

(4.4)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
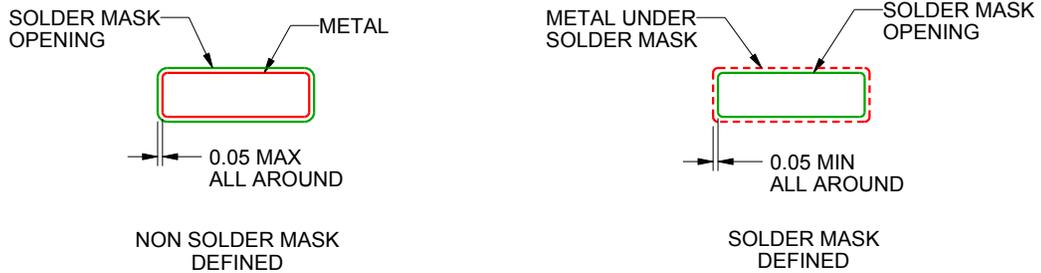
SOLDER MASK DETAILS
NOT TO SCALE

4221984/A   05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
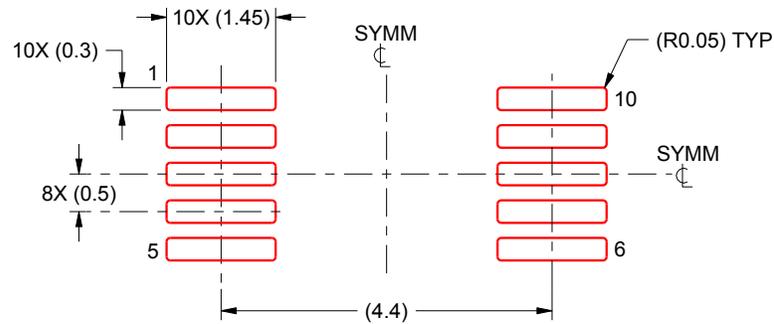
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A   05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PIN 1
INDEX AREA

3.0
2.6

1.75
1.45

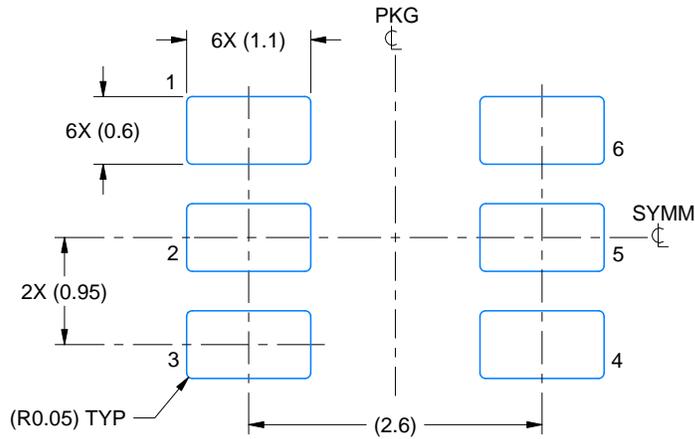B

A

1

6

2X 0.95

2

5

1.9

3

4

6X 0.50
0.25

⊕ 0.2 Ⓜ C A B

3.05
2.75

C

◯ 0.1 C

4X 0°-15°

(1.1)

1.45
0.90

0.15
0.00 TYP

0.25

GAGE PLANE

4X 4°-15°

0.22
0.08 TYP

8°
0° TYP

0.6
0.3 TYP

SEATING PLANE

4214840/G   08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

PKG

6X (1.1)

1

6X (0.6)

6

2

SYMM

5

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214840/G   08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (1.1)

1

6X (0.6)

2

SYMM

5

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G　08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
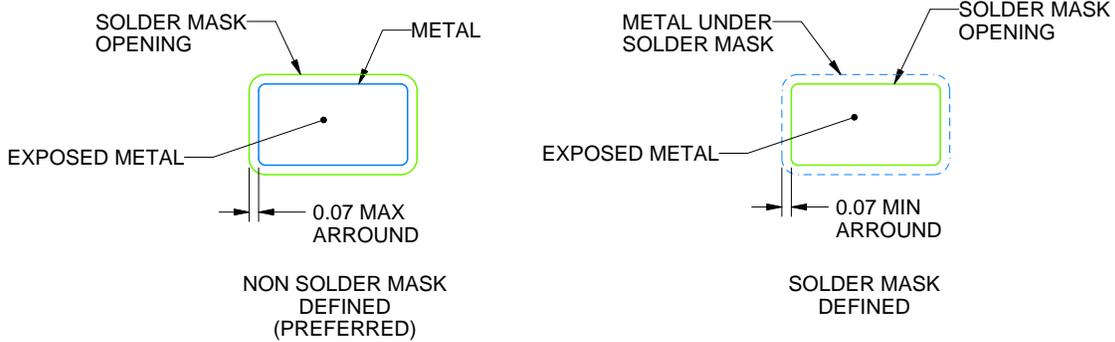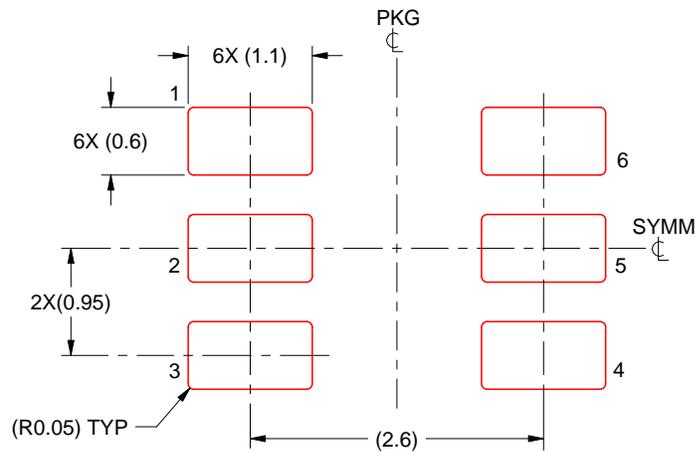9. Board assembly site may have different recommendations for stencil design.
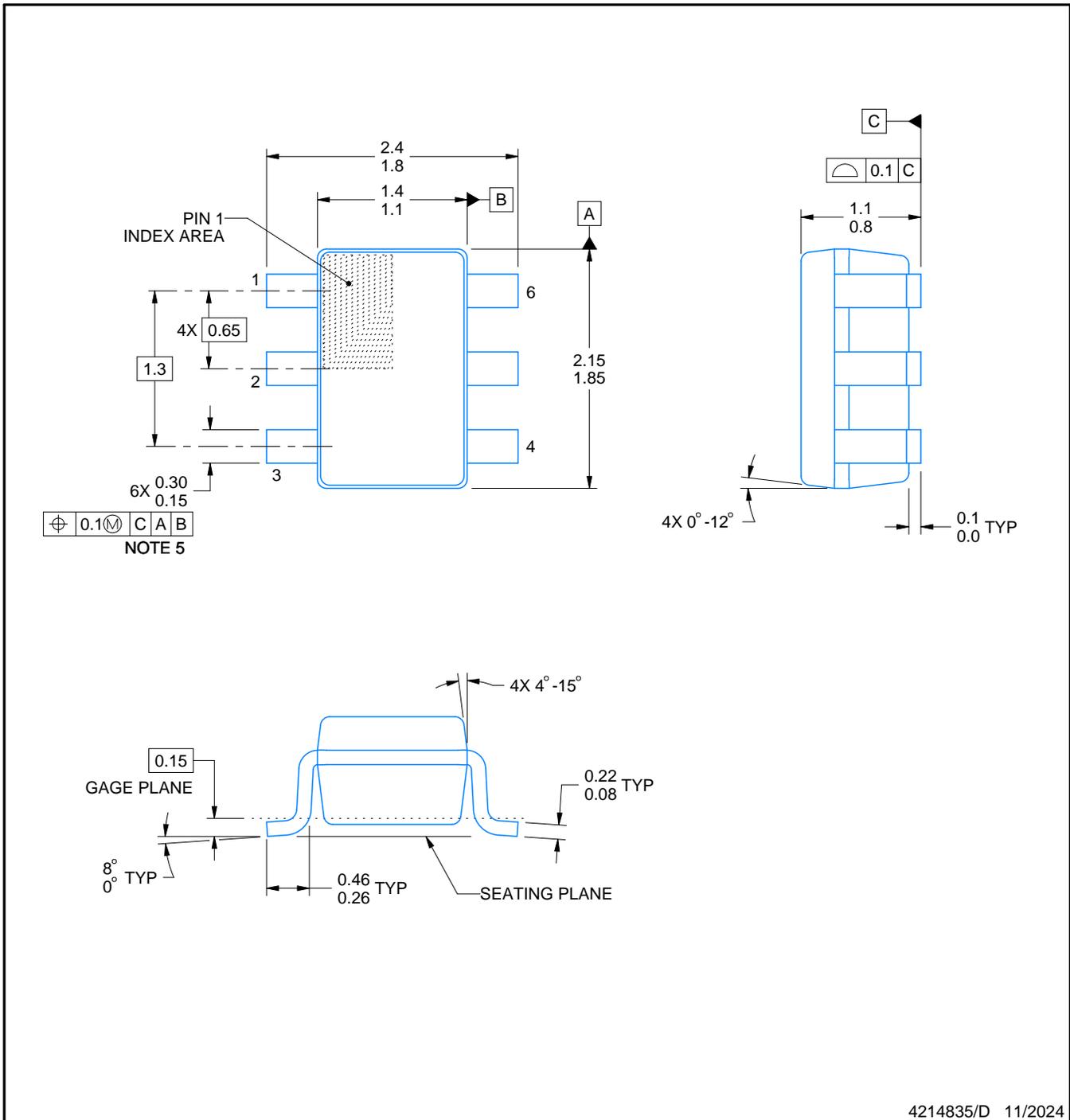
2.4
1.8

1.4
1.1

B

A

PIN 1
INDEX AREA

1

6

4X 0.65

1.3

2.15
1.85

2

4

3

6X 0.30
0.15

⊕ 0.1 Ⓜ C A B
NOTE 5

C

⌓ 0.1 C

1.1
0.8

4X 0° -12°

0.1
0.0 TYP

4X 4° -15°

0.15

GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

0.46
0.26 TYP
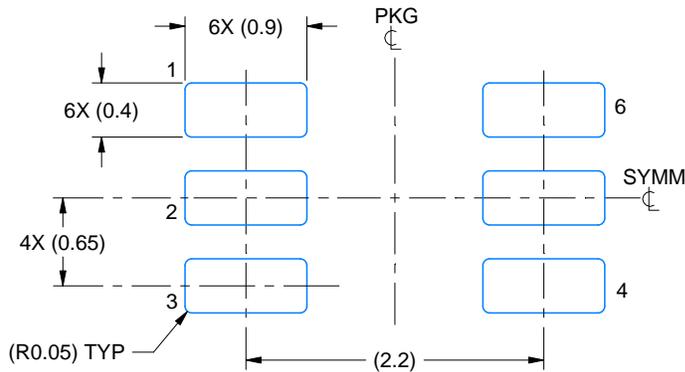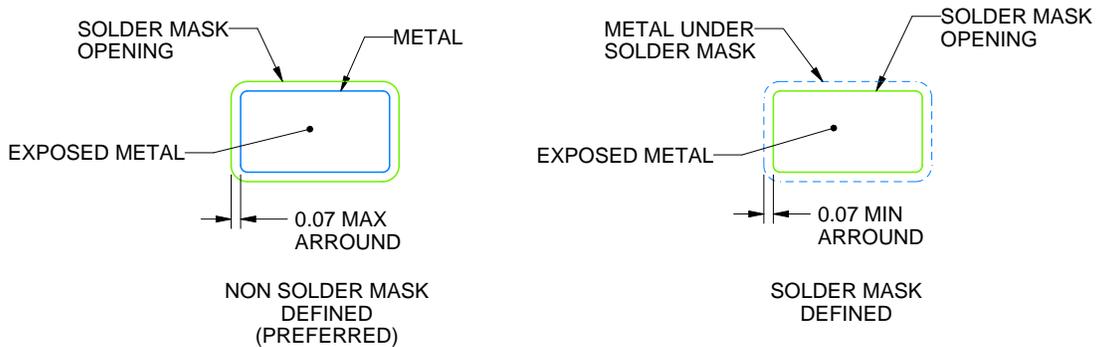
SEATING PLANE

4214835/D   11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

Texas
Instruments
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6X (0.9)

PKG ℄

1

6X (0.4)

6

2

SYMM ℄

4X (0.65)

3

4

(R0.05) TYP

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL
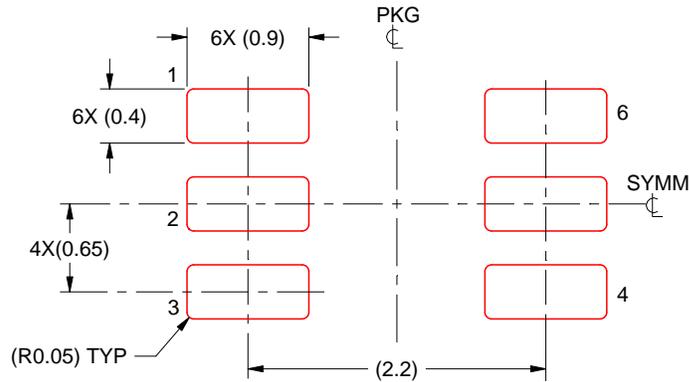
0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214835/D   11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (0.9)

1

6X (0.4)

6

2

SYMM

4X(0.65)

3
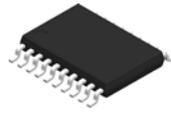
4

(R0.05) TYP

(2.2)

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D   11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.
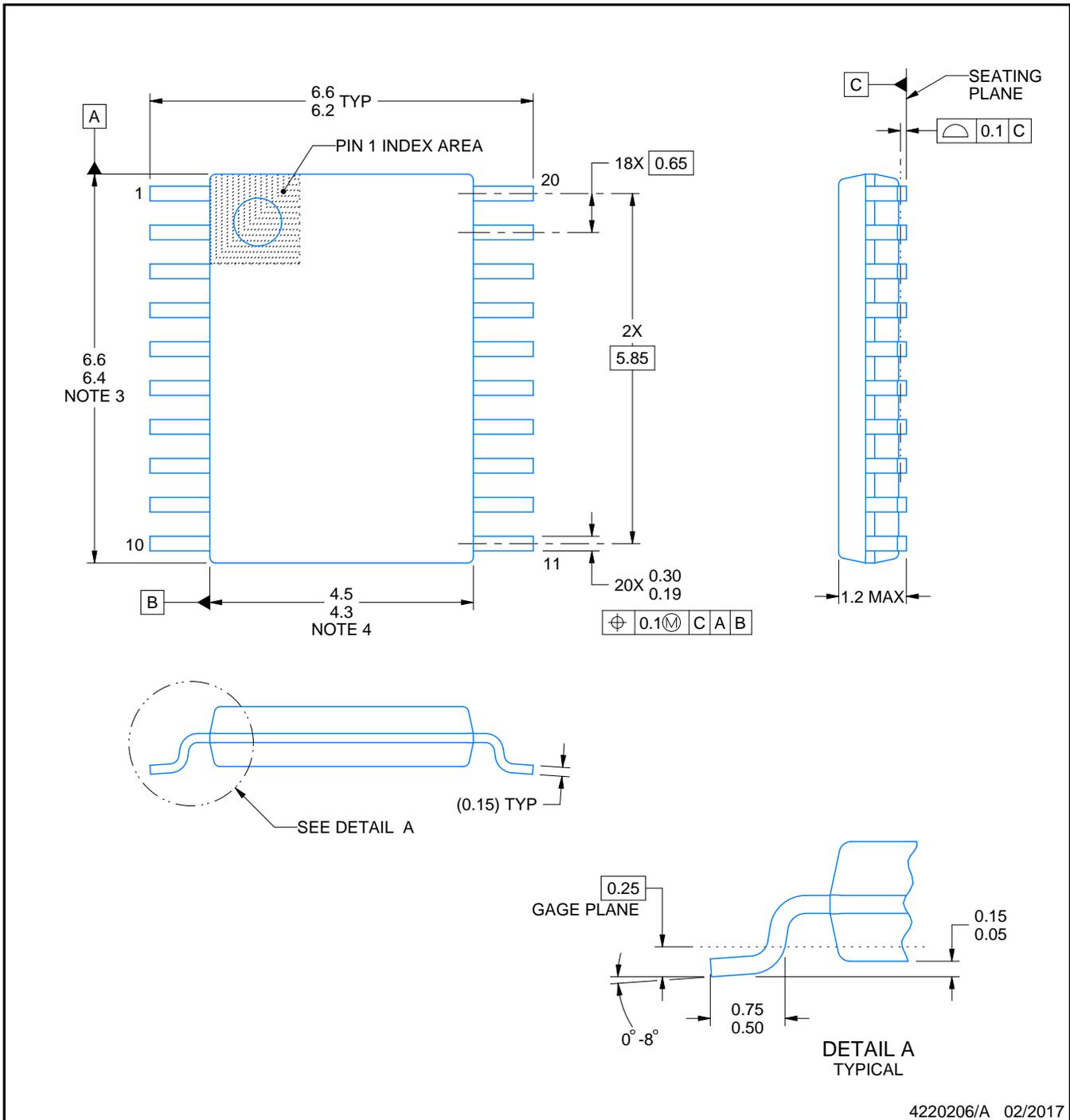
A

6.6
6.2 TYP

PIN 1 INDEX AREA

1

20

18X $\boxed{0.65}$

6.6
6.4
NOTE 3

2X

$\boxed{5.85}$

10

11

B

4.5
4.3
NOTE 4

20X $\begin{array}{c}0.30\\0.19\end{array}$

$\boxed{\oplus\ |\ 0.1\ⓂC\ |\ A\ |\ B}$

C

SEATING
PLANE

$\boxed{\bigtriangleup\ |\ 0.1\ |\ C}$

1.2 MAX

SEE DETAIL A

(0.15) TYP

$\boxed{0.25}$

GAGE PLANE

0.15
0.05

0°-8°

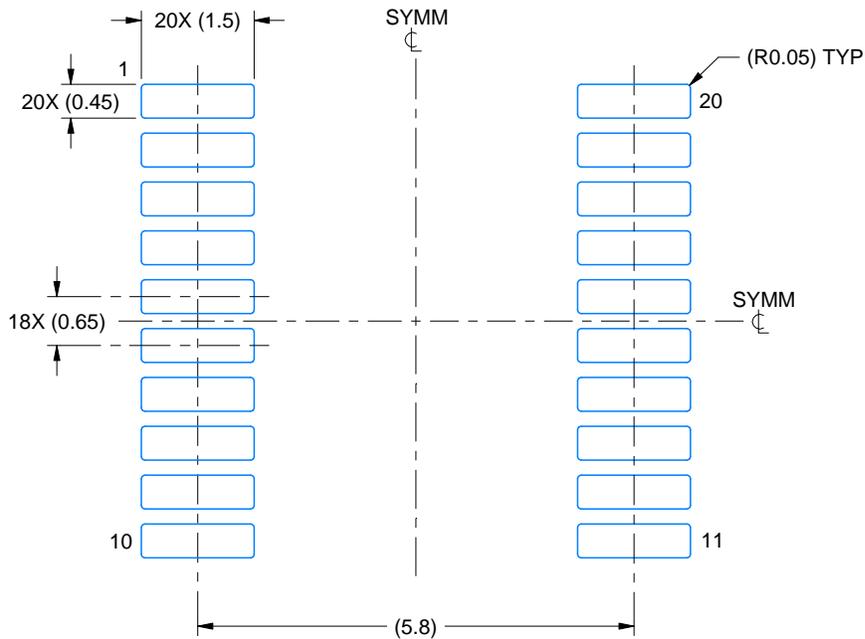0.75
0.50

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

1

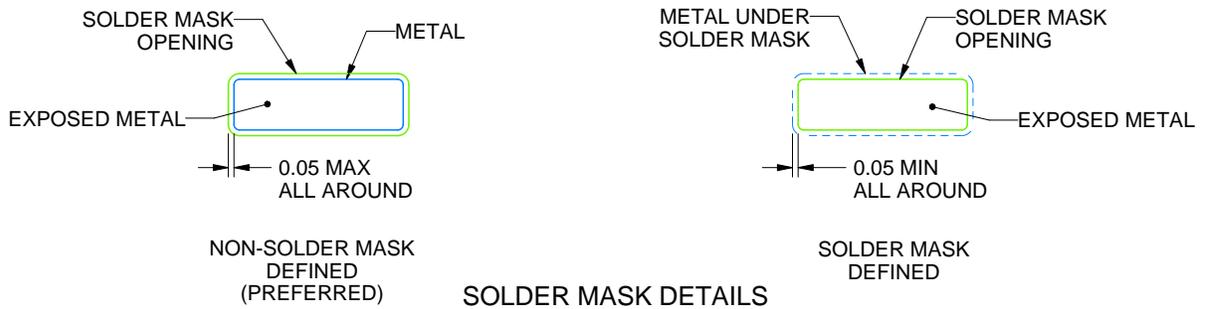20X (0.45)

(R0.05) TYP

20

SYMM

18X (0.65)

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

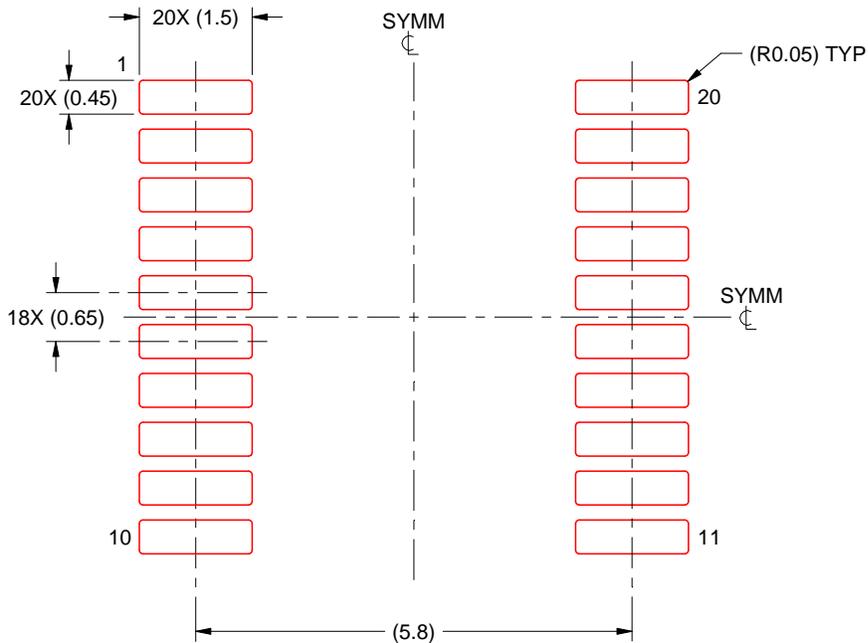**SOLDER MASK DETAILS**

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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