

LF147JAN Wide Bandwidth Quad JFET Input Operational Amplifier

Check for Samples: [LF147JAN](#)

FEATURES

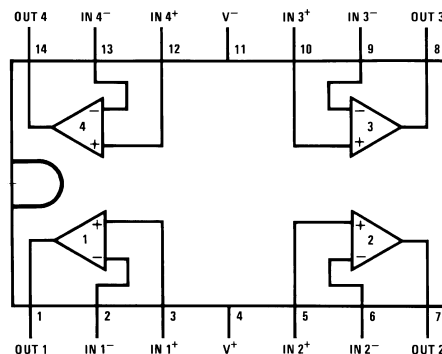
- **Internally Trimmed Offset Voltage:** 5 mV Max
- **Low Input Bias Current:** 50 pA Typ.
- **Low Input Noise Current:** 0.01 pA/√Hz Typ.
- **Wide Gain Bandwidth:** 4 MHz Typ.
- **High Slew Rate:** 13 V/μs Typ.
- **Low Supply Current:** 7.2 mA Typ.
- **High Input Impedance:** $10^{12}\Omega$ Typ.
- **Low Total Harmonic Distortion:**
 - $A_V = 10$, $R_L = 10K\Omega$, $V_O = 20V_{P-P}$
 - $BW = 20Hz - 20KHz \leq 0.02\%$ Typ.
- **Low 1/f Noise Corner:** 50 Hz Typ.
- **Fast Settling Time to 0.01%:** 2 μs Typ.

DESCRIPTION

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET™ II technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Connection Diagram



**Figure 1. CDIP Package
Top View
See Package Number J**



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Simplified Schematic

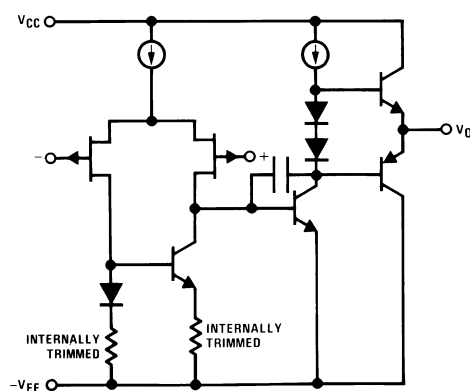
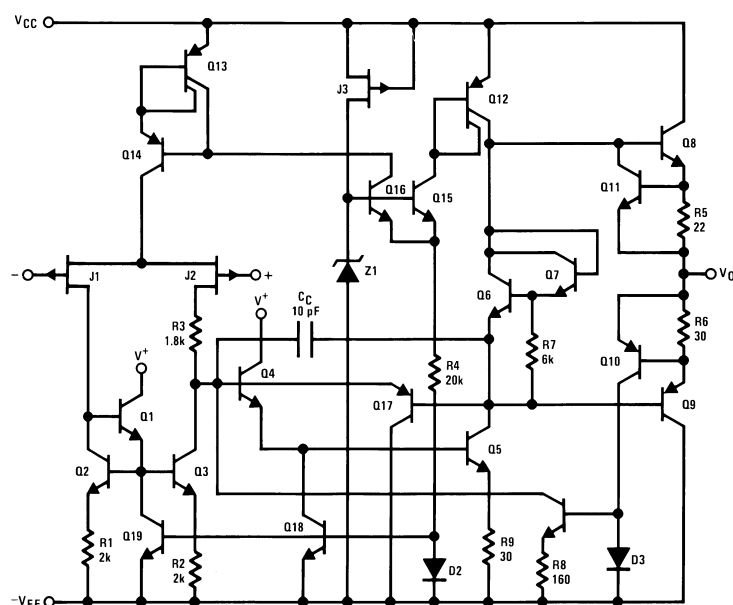


Figure 2. $\frac{1}{4}$ Quad

Detailed Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range ⁽²⁾	±15V
Output Short Circuit Duration ⁽³⁾	Continuous
Power Dissipation ⁽⁴⁾⁽⁵⁾	900 mW
T _J max	150°C
θ _{JA} CDIP	70°C/W
Operating Temperature Range	–55°C ≤ T _A ≤ 125°C
Storage Temperature Range	–65°C ≤ T _A ≤ 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD ⁽⁶⁾	900V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- (3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} – T_A) / θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
- (6) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

Supply Voltage Range	±5V to ±15V
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Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55
12	Settling Time at	25

LF147JAN Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified: $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 26V$, $-V_{CC} = -4V$, $V_{CM} = -11V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 4V$, $-V_{CC} = -26V$, $V_{CM} = 11V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 26V$, $-V_{CC} = -4V$, $V_{CM} = -11V$		-0.4	0.2	nA	1
				-10	50	nA	2
		$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-0.2	0.2	nA	1
				-10	50	nA	2
		$+V_{CC} = 4V$, $-V_{CC} = -26V$, $V_{CM} = 11V$		-0.2	1.2	nA	1
				-10	70	nA	2
I_{IO}	Input Offset Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-0.1	0.1	nA	1
				-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	$-V_{CC} = -15V$, $+V_{CC} = 20V$ to $10V$		80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to $-10V$		80		dB	1, 2, 3
CMRR	Input Voltage Common Mode Rejection	$\pm V_{CC} = \pm 4V$ to $\pm 26V$, $V_{CM} = -11V$ to $+11V$		80		dB	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = -10V$, $t \leq 25mS$		-80		mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 10V$, $t \leq 25mS$			80	mA	1, 2, 3
I_{CC}	Supply Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$			14	mA	1, 2
					16	mA	3
Delta V_{IO} / Delta T	Input Offset Voltage Temp. Sensitivity	$25^{\circ}C \leq T_A \leq +125^{\circ}C$	See ⁽¹⁾	-30	30	$\mu V/^{\circ}C$	2
		$-55^{\circ}C \leq T_A \leq 25^{\circ}C$	See ⁽¹⁾	-30	30	$\mu V/^{\circ}C$	3
$+V_{OP}$	Output Voltage Swing	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 10K\Omega$, $V_{CM} = -15V$		12		V	4, 5, 6
		$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 2K\Omega$, $V_{CM} = -15V$		10		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 10K\Omega$, $V_{CM} = 15V$			-12	V	4, 5, 6
		$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 2K\Omega$, $V_{CM} = 15V$			-10	V	4, 5, 6
$+A_{VS}$	Open Loop Voltage Gain	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 2K\Omega$, $V_O = 0$ to $10V$		50		V/mV	4
				25		V/mV	5, 6
$-A_{VS}$	Open Loop Voltage Gain	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $R_L = 2K\Omega$, $V_O = 0$ to $-10V$		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain	$+V_{CC} = 5V$, $-V_{CC} = -5V$, $R_L = 10K\Omega$, $V_O = \pm 2V$		20		V/mV	4, 5, 6

(1) Calculated parameters.

LF147JAN Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified: $V_{CC} = \pm 15V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
+SR	Slew Rate	$V_I = -5V$ to $+5V$		7		V/ μ S	7
				5		V/ μ S	8A, 8B
-SR	Slew Rate	$V_I = +5V$ to $-5V$		7		V/ μ S	7
				5		V/ μ S	8A, 8B
TR _{TR}	Transient Response Rise Time	AV=1, $V_I=50mV$, $C_L = 100pF$, $R_L=2K\Omega$			200	nS	7, 8A, 8B
TR _{OS}	Transient Response Overshoot	AV=1, $V_I=50mV$, $C_L = 100pF$, $R_L=2K\Omega$			40	%	7, 8A, 8B
NI _{BB}	Noise Broadband	BW = 10Hz to 15KHz, $R_S = 0\Omega$			15	μV_{RMS}	7
NI _{PC}	Noise Popcorn	BW = 10Hz to 15KHz, $R_S = 100K\Omega$			80	μV_{PK}	7
C _S	Channel Separation	$R_L = 2K\Omega$		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, A to B		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, A to C		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, A to D		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, B to A		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, B to C		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, B to D		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, C to A		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, C to B		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, C to D		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, D to A		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, D to B		80		dB	7
		$R_L = 2K\Omega$, $V_I = \pm 10V$, D to C		80		dB	7
$\pm t_S$	Settling Time	$A_V = 1$			1,500	nS	12

LF147JAN Electrical Characteristics Drift Values

The following conditions apply, unless otherwise specified: DC $\pm V_{CC} = \pm 15V$, $V_{CM} = 0V$, "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only"

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V _{IO}	Input Offset Voltage	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-1.0	1.0	mV	1
+I _{IB}	Input Bias Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-0.1	0.1	nA	1
-I _{IB}	Input Bias Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-0.1	0.1	nA	1

Typical Performance Characteristics

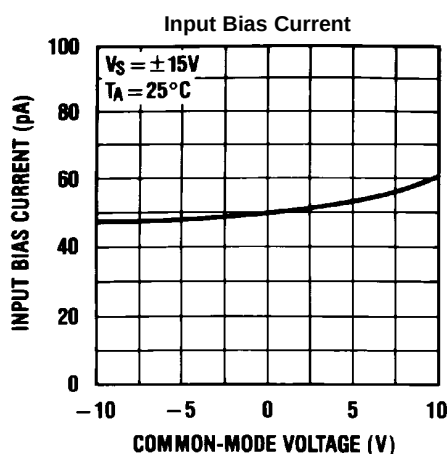


Figure 3.

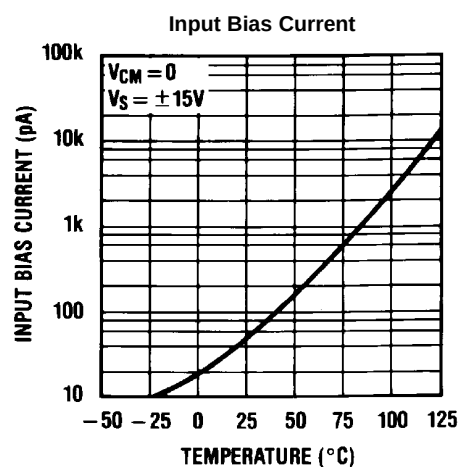


Figure 4.

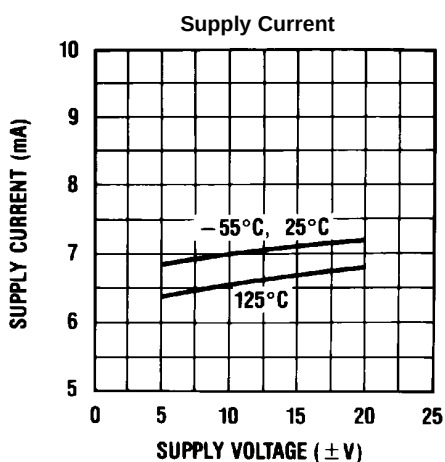


Figure 5.

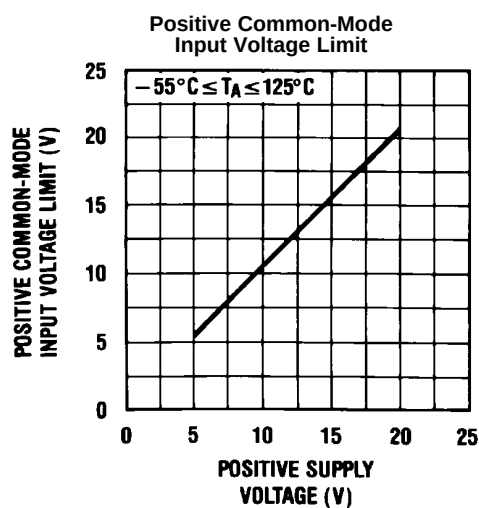


Figure 6.

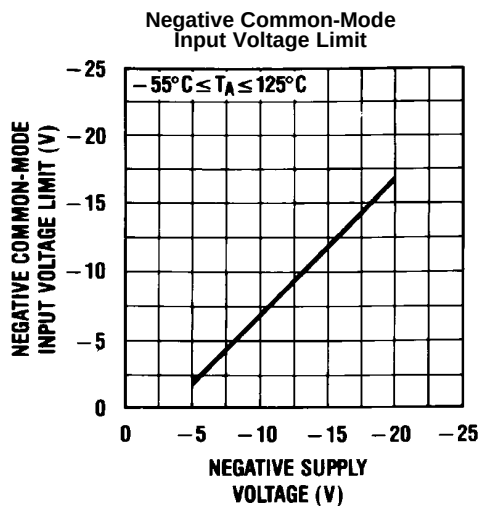


Figure 7.

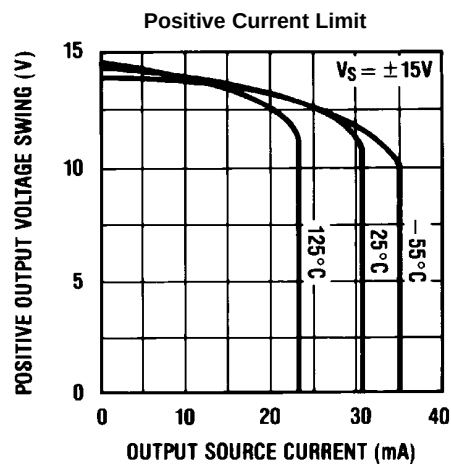


Figure 8.

Typical Performance Characteristics (continued)

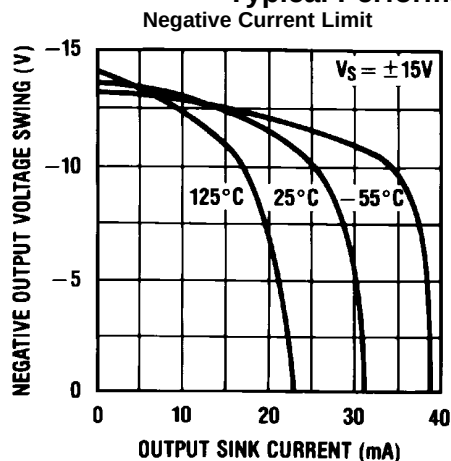


Figure 9.

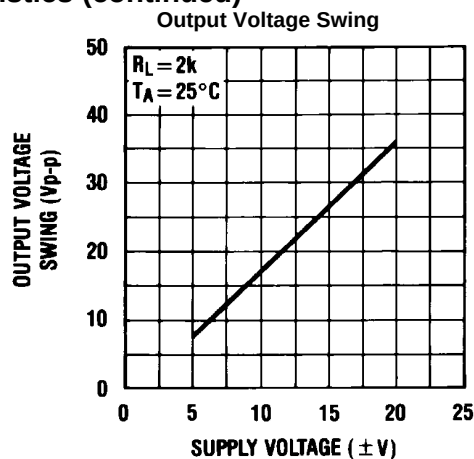


Figure 10.

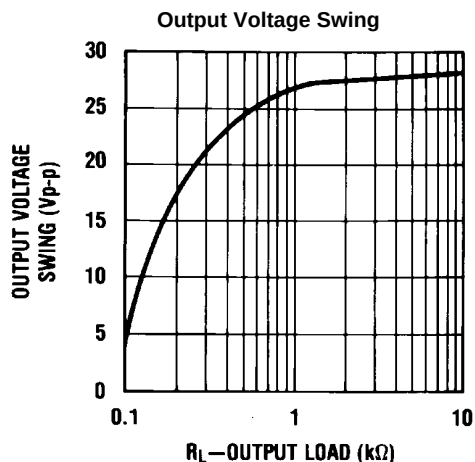


Figure 11.

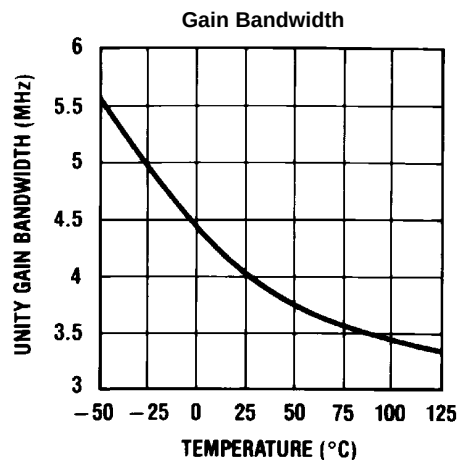


Figure 12.

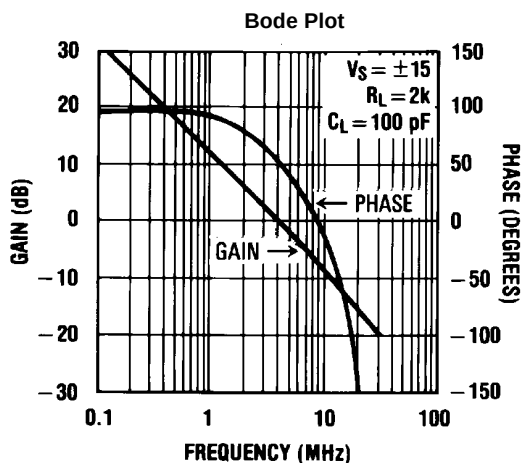


Figure 13.

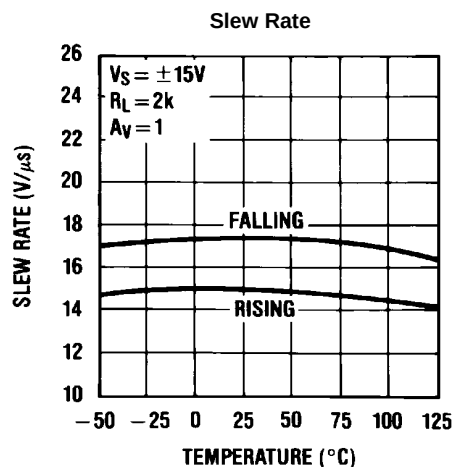


Figure 14.

Typical Performance Characteristics (continued)

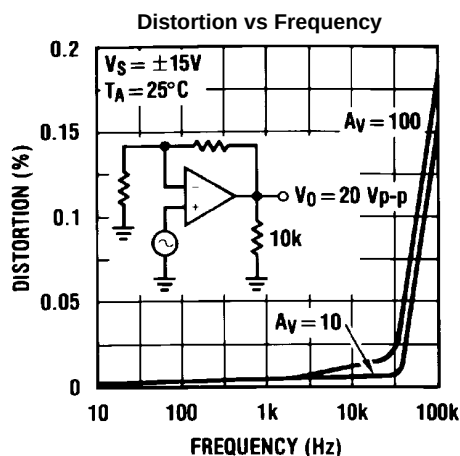


Figure 15.

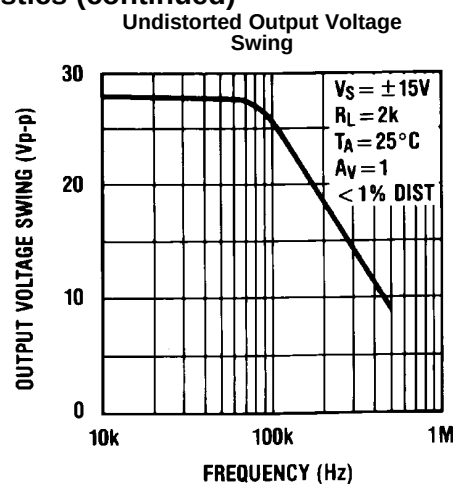


Figure 16.

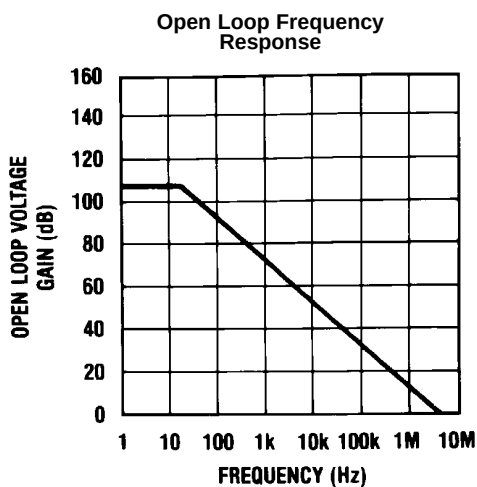


Figure 17.

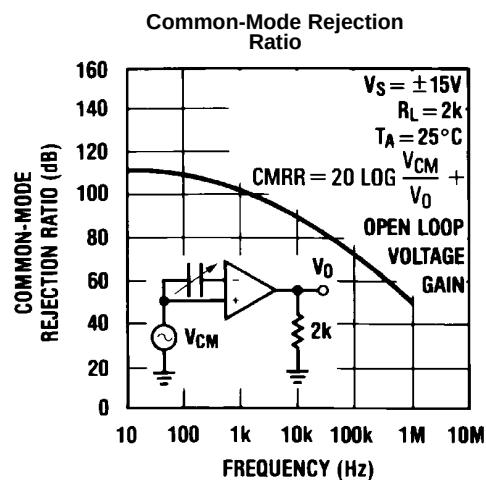


Figure 18.

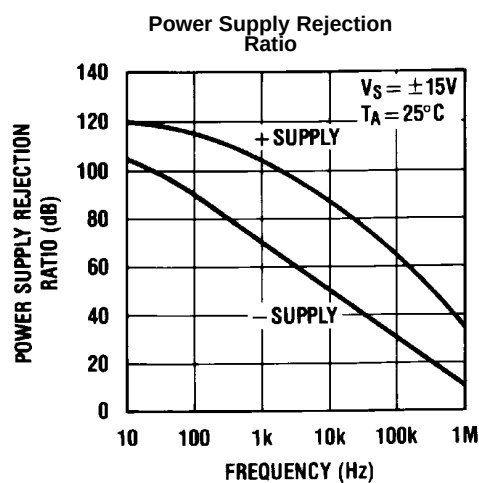


Figure 19.

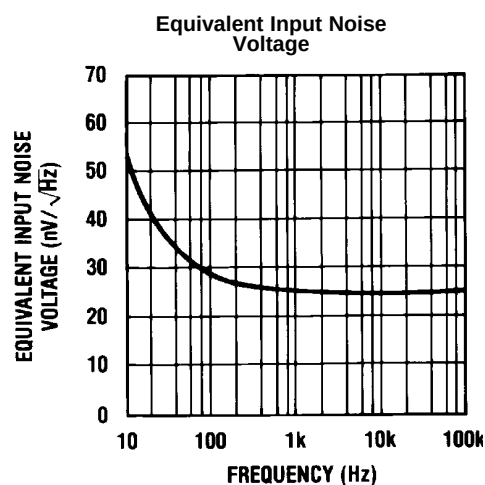


Figure 20.

Typical Performance Characteristics (continued)

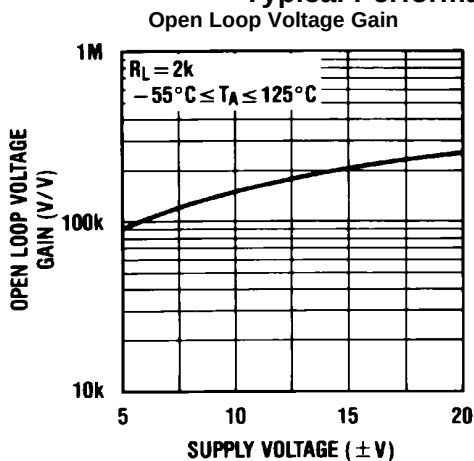


Figure 21.

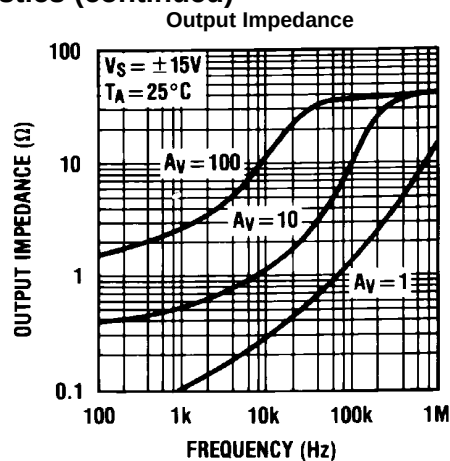


Figure 22.

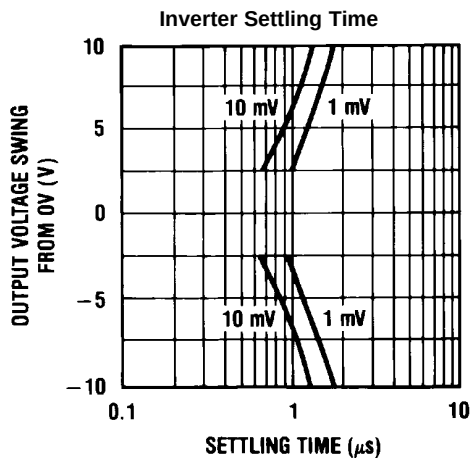


Figure 23.

Pulse Response

$R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$

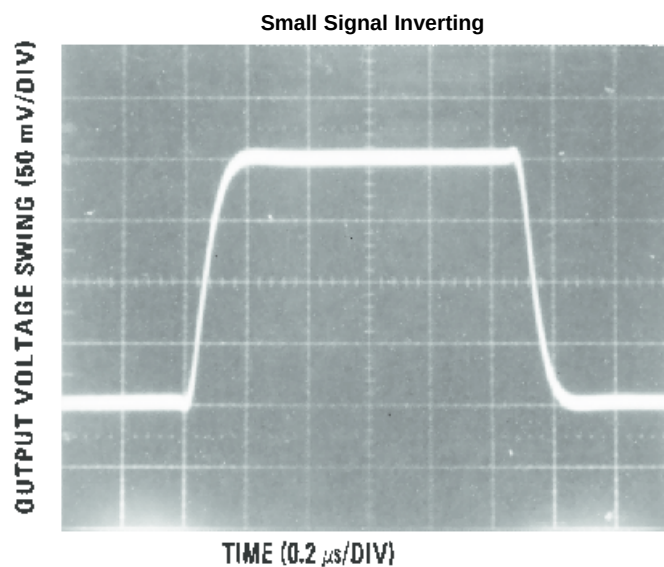


Figure 24.

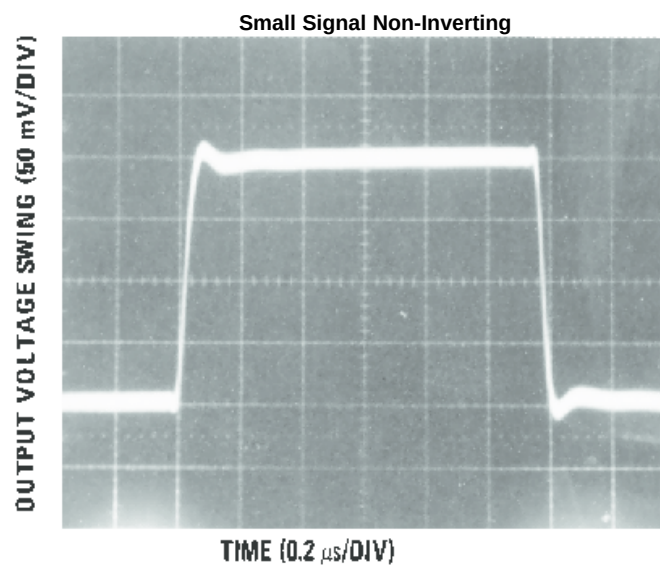


Figure 25.

Pulse Response (continued)

$R_L=2\text{ k}\Omega$, $C_L=10\text{ pF}$

Large Signal Inverting

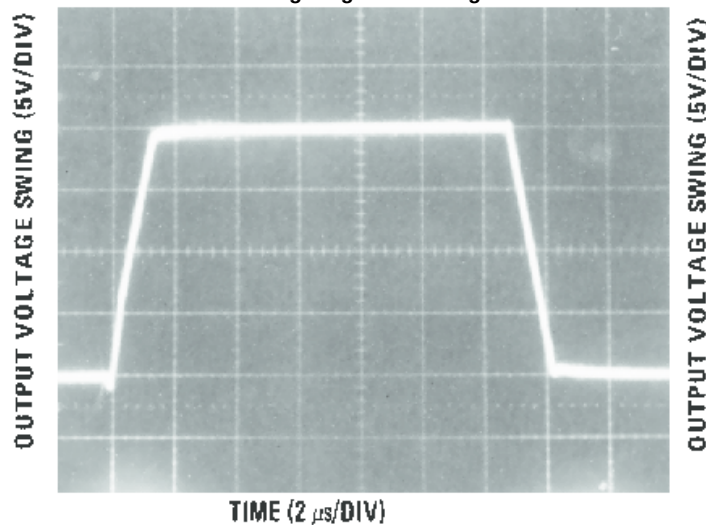


Figure 26.

Large Signal Non-Inverting

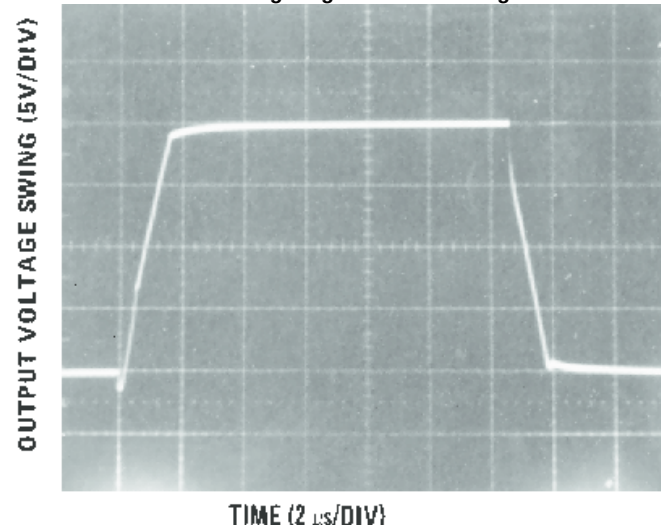


Figure 27.

Current Limit ($R_L=100\Omega$)

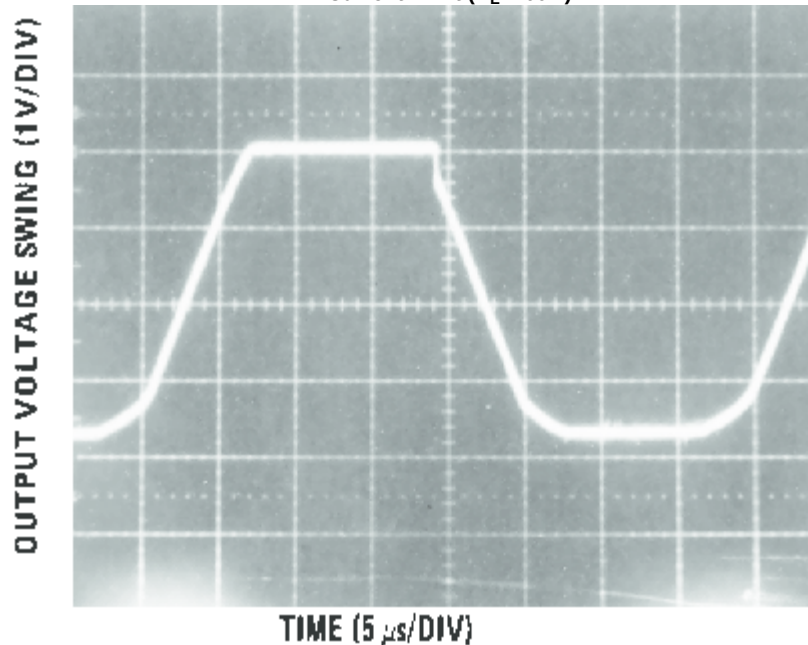


Figure 28.

APPLICATION HINTS

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 4.5\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 k Ω load resistance to $\pm 10\text{V}$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

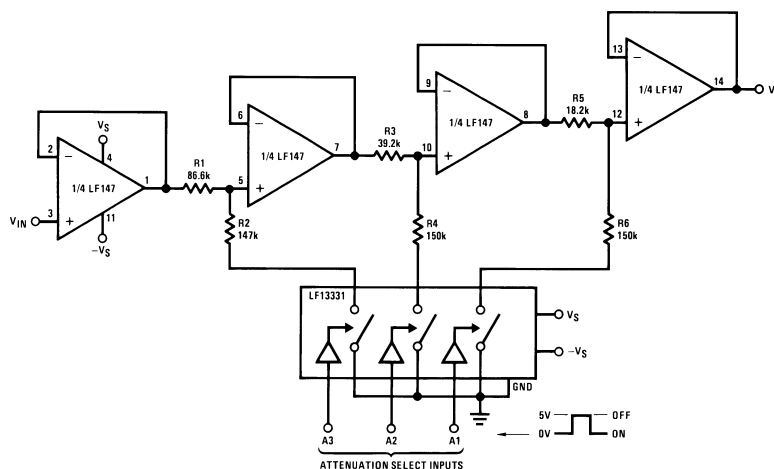
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Figure 29. Digitally Selectable Precision Attenuator

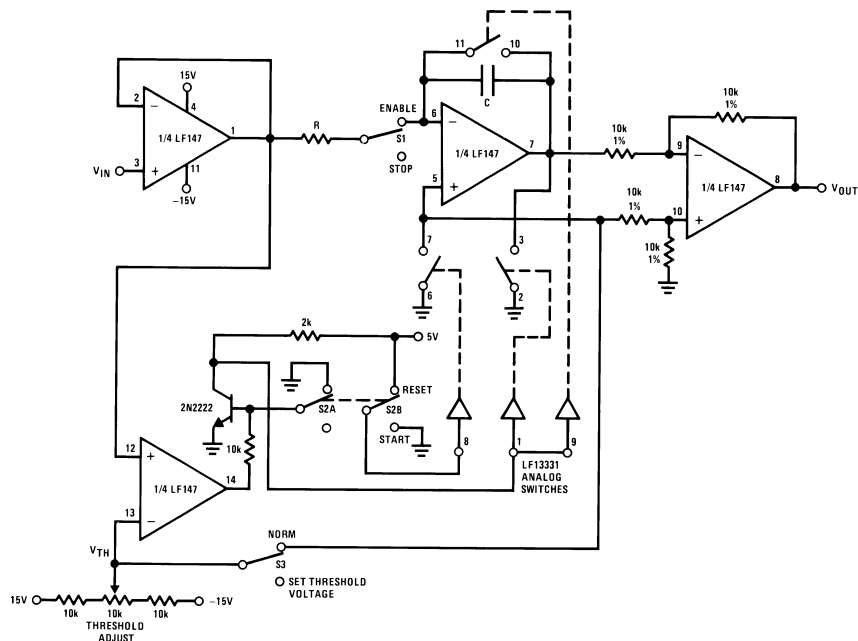


All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	-1 dB
0	1	0	-2 dB
0	1	1	-3 dB
1	0	0	-4 dB
1	0	1	-5 dB
1	1	0	-6 dB
1	1	1	-7 dB

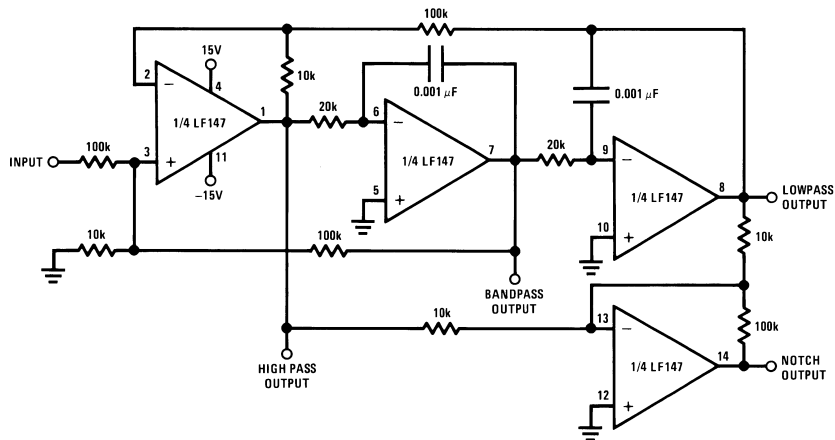
Figure 30. Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



- V_O starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$
- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Figure 31. Universal State Variable Filter



For circuit shown:

$f_0 = 3$ kHz, $f_{NOTCH} = 9.5$ kHz

$Q = 3.4$

Passband gain:

Highpass – 0.1

Bandpass – 1

Lowpass – 1

Notch – 10

- $f_0 \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

Date Released	Revision	Section	Originator	Changes
04/18/05	A	New Release into corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. MJLF147–X rev 1B1 MDS will be archived
03/20/13	A	All		Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JL147BCA	Active	Production	CDIP (J) 14	25 TUBE	No	Call TI	Call TI	-55 to 125	JL147BCA JM38510/11906BCA Q
JM38510/11906BCA	Active	Production	CDIP (J) 14	25 TUBE	No	Call TI	Call TI	-55 to 125	JL147BCA JM38510/11906BCA Q
M38510/11906BCA	Active	Production	CDIP (J) 14	25 TUBE	No	Call TI	Call TI	-55 to 125	JL147BCA JM38510/11906BCA Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

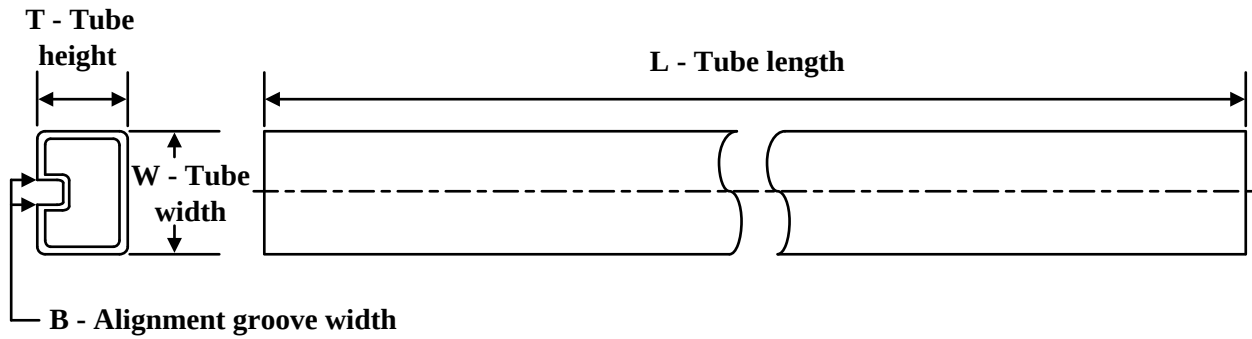
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

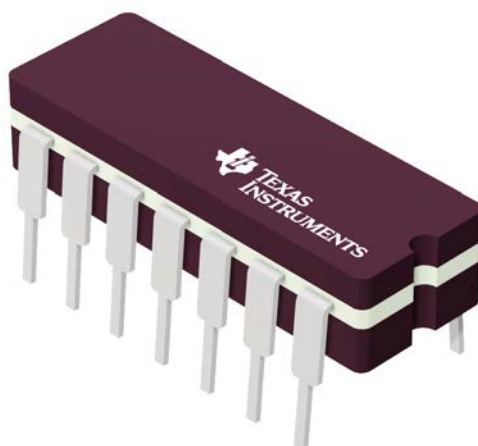
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JL147BCA	J	CDIP	14	25	506.98	15.24	13440	NA
JM38510/11906BCA	J	CDIP	14	25	506.98	15.24	13440	NA
M38510/11906BCA	J	CDIP	14	25	506.98	15.24	13440	NA

J 14

GENERIC PACKAGE VIEW

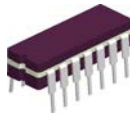
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

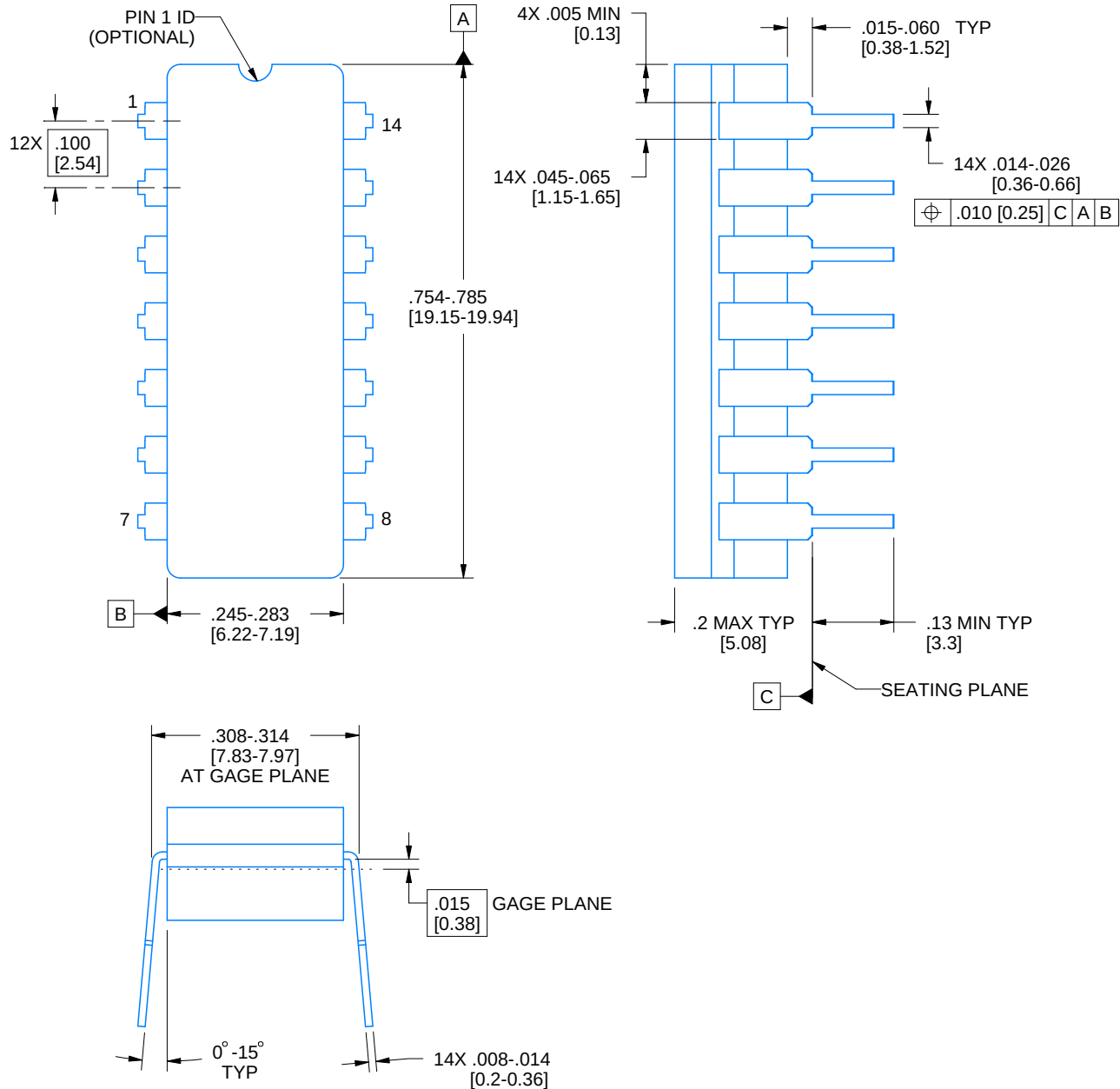


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



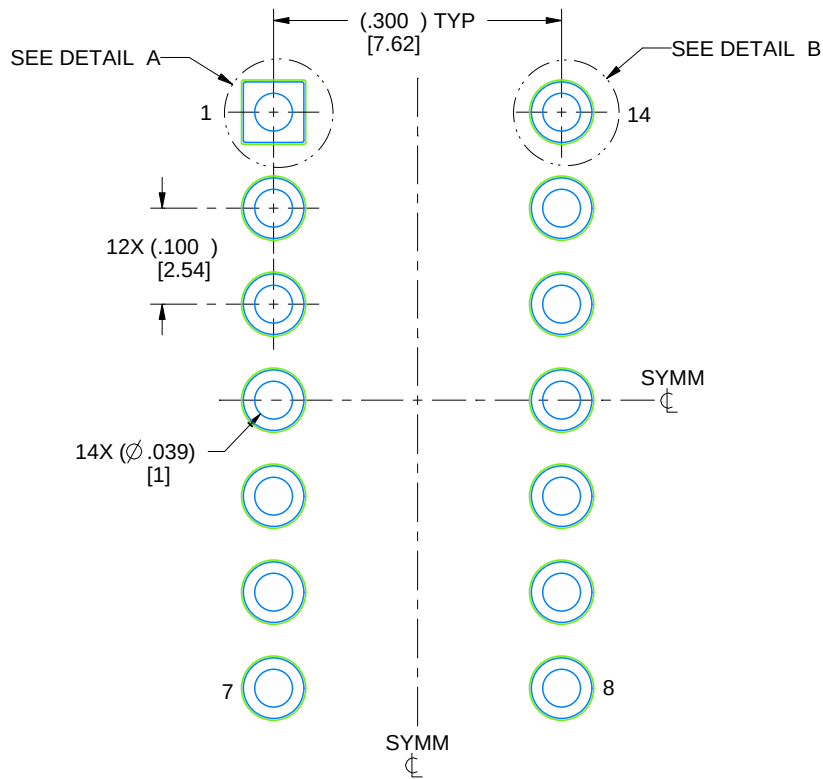
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EXAMPLE BOARD LAYOUT

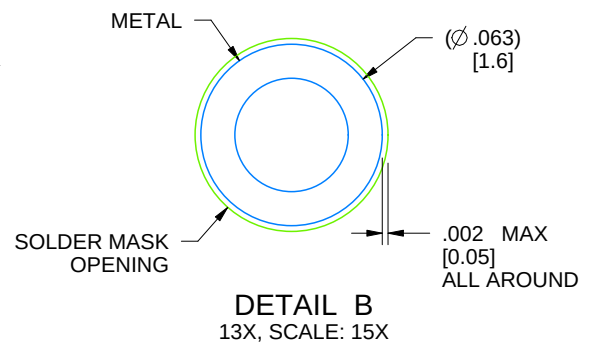
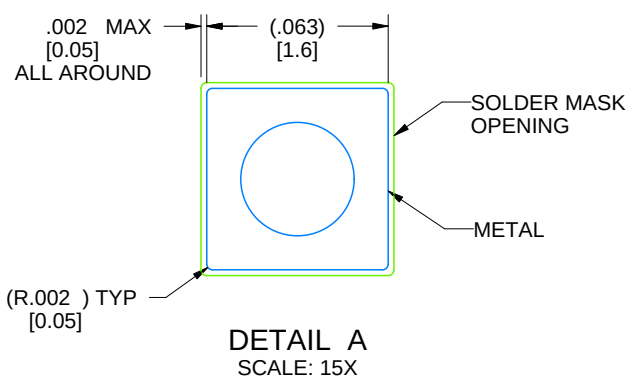
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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