LF412C Dual FET-Input Operational Amplifier

1 Features

- Low input bias current: ±10pA typ
- Low input noise current: 2fA/√Hz typ
- Low supply current: 0.560mA typ
- High input impedance
- Internally trimmed offset voltage
- Wide gain bandwidth: 4.5MHz typ
- High slew rate: 21V/µs typ (new die performance with V_{ID} = 1V)

2 Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side or low side sensing
- Headphone amplifier

3 Description

This device is a low-cost, FET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. The operational amplifier requires low supply current yet maintains a large gain bandwidth product. In addition, the input stage provides very low input bias and offset currents.

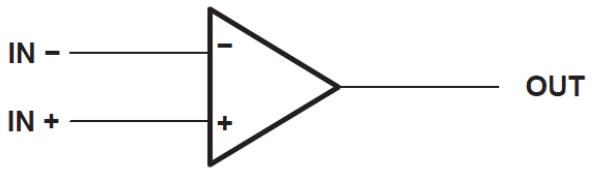
The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LF412CD	D (SOIC, 8)	4.90mm × 3.90mm
LF412CP	P (PDIP, 8)	9.81mm × 6.35mm

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (each amplifier)

Table of Contents

4 Pin Configuration and Functions

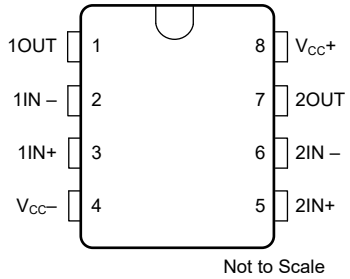


Figure 4-1. D or P Package
Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1OUT	1	O	Output, channel 1
1IN −	2	I	Inverting input, channel 1
1IN +	3	I	Non-inverting input, channel 1
V_{CC}–	4	—	Positive (highest) power supply
V_{CC}+	5	—	Negative (lowest) power supply
2OUT	6	O	Output, channel 2
2IN −	7	I	Inverting input, channel 2
2IN +	8	I	Non-inverting input, channel 2

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage, positive		18	V
V_{CC-}	Supply voltage, negative		–18	V
V_{ID}	Differential input voltage(3)		±30	V
V_I	Input voltage(2)		±15	V
	Duration of output short circuit	Unlimited		
	Continuous total power dissipation		500	mW
T_A	Operating temperature range	0	70	℃
T_{stg}	Storage temperature	–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Temperature and supply voltages must be limited to make sure that the dissipation rating is not exceeded.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage, positive	3.5	18	V
V_{CC-}	Supply voltage, negative	−3.5	–18	V

5.3 Electrical Characteristics

over operating free-air temperature range, $V_{CC\pm}$ = ±15V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0	R_S = 10kΩ	25°C		±0.125	3	mV
a_{VIO}	Average temperature coefficient of input offset voltage	V_{IC}= 0	R_S = 10kΩ	Full Range		±0.3	20(2)	µV/°C
I_{IO}	Input offset current(3)	V_{IC} = 0		25°C		±10	100	pA
				70°C			4	nA
I_{IB}	Input bias current(3)	V_{IC} = 0		25°C		±10	200	pA
				70°C			8	nA
V_{ICR}	Common-mode input voltage range				±11	− 11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	R_L = 10kΩ			±12	±14.950		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V,	R_L = 2kΩ	25°C	88	130		dB
				Full range	83.5			
r_{ID}	Differential Input resistance			25°C		540		GΩ
r_{ICM}	Common-mode Input resistance					6		TΩ
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR_{min}}$, R_S ≤ 10kΩ			70	100		dB
k_{SVR}	Supply-voltage rejection ratio(4)				70	100		dB
I_{CC}	Supply current (per amplifier)					0.560	3.4	mA

(1) Full range is 0°C to 70°C.

(2) At least 90% of the devices meet this limit for a_{VIO}.
(3) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.
(4) Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

5.4 Operating Characteristics

$V_{CC±}$ = ±15V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1kHz			120		dB
SR	Slew rate	R_L = 2kΩ, C_L = 100pF	V_{ID} = 1V		21		V/μs
			V_{ID} = 100mV		0.5		
B_1	Unity-gain bandwidth				4.5		MHz
V_n	Equivalent input noise voltage	f = 1kHz,	R_S = 20Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz			2		fA/√Hz

5.5 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

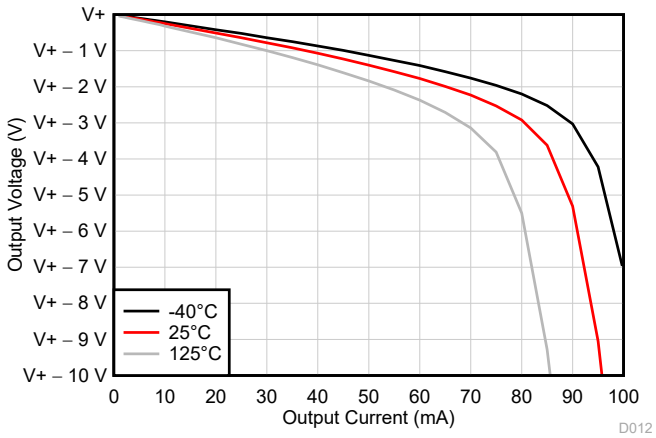


Figure 5-1. Output Voltage Swing vs Output Current (Sourcing), New Die

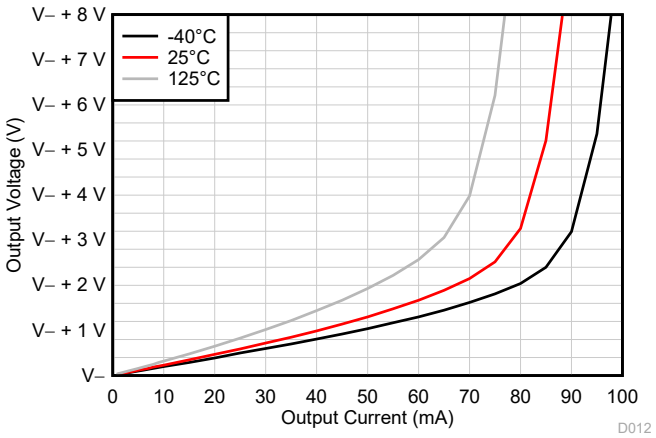
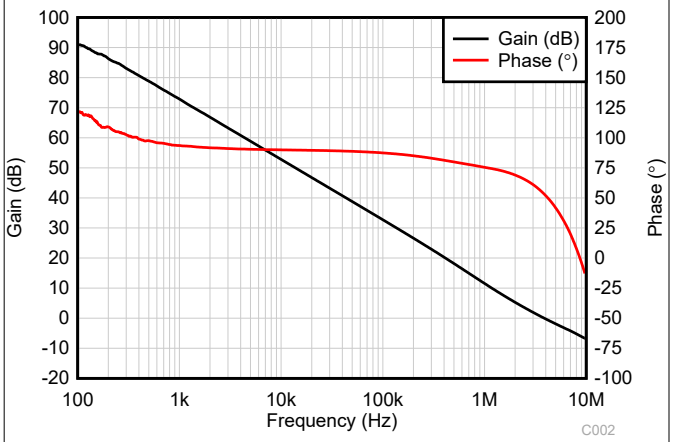


Figure 5-2. Output Voltage Swing vs Output Current (Sinking), New Die



C_L = 20pF

Figure 5-3. Open-Loop Gain and Phase vs Frequency, New Die

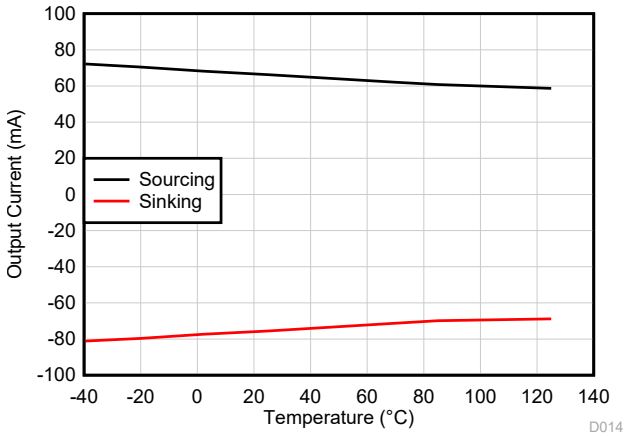
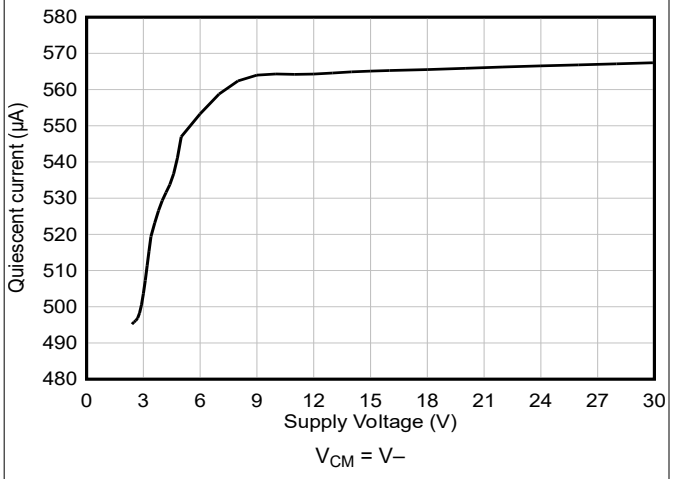


Figure 5-4. Short-Circuit Current vs Temperature, New Die



V_{CM} = V–

Figure 5-5. Quiescent Current vs Supply Voltage, New Die

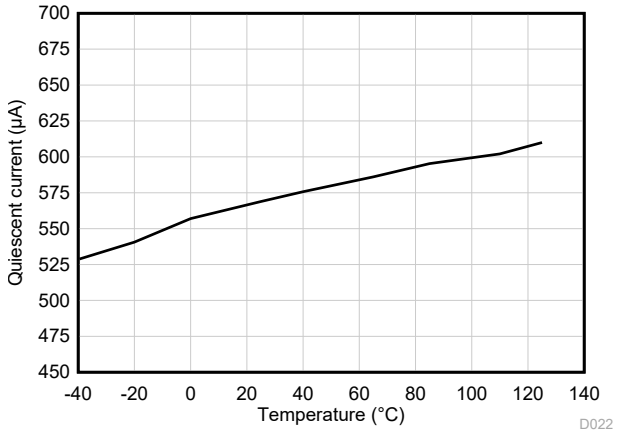


Figure 5-6. Quiescent Current vs Temperature, New Die

5.5 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

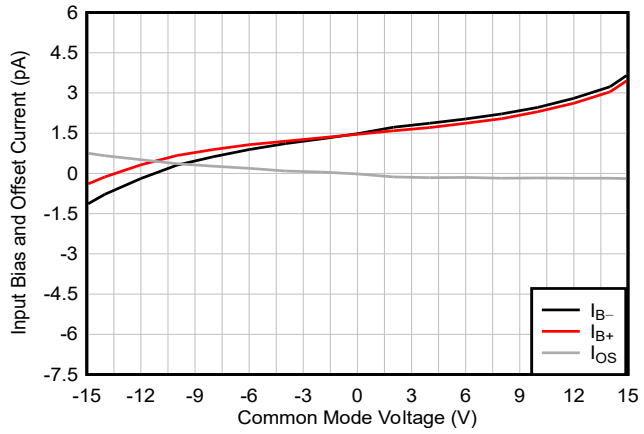


Figure 5-7. Input Bias Current vs Common-Mode Voltage, New Die

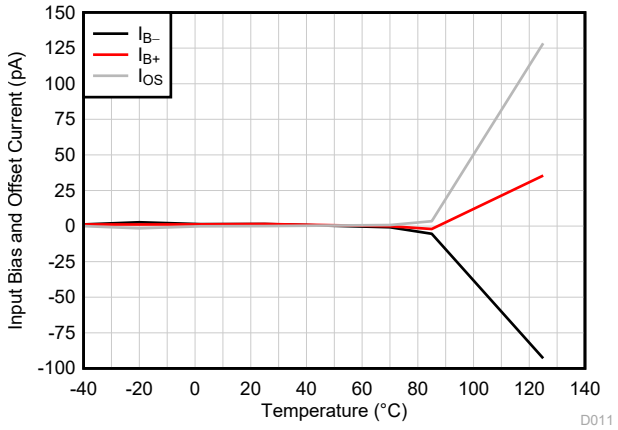


Figure 5-8. Input Bias Current vs Temperature, New Die

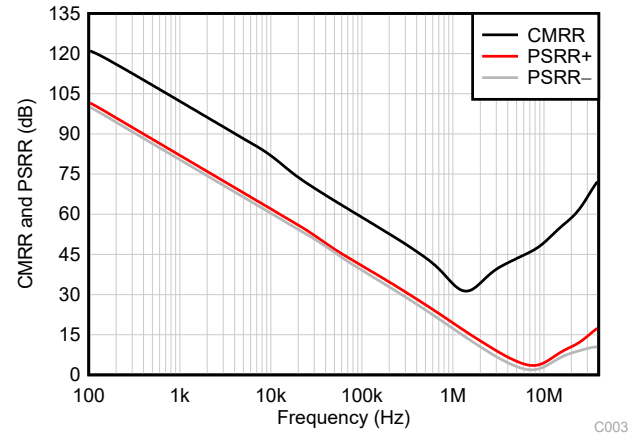


Figure 5-9. CMRR and PSRR vs Frequency, New Die

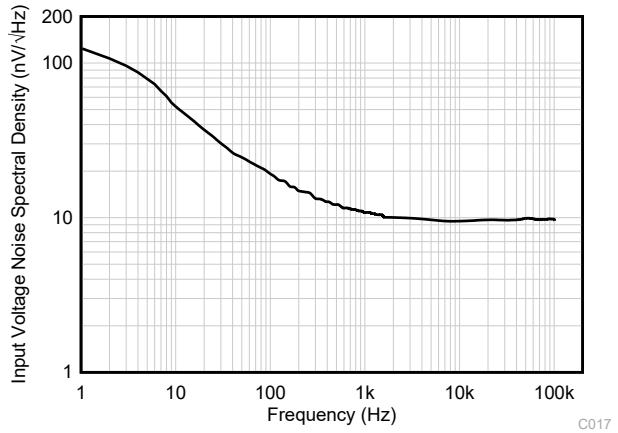
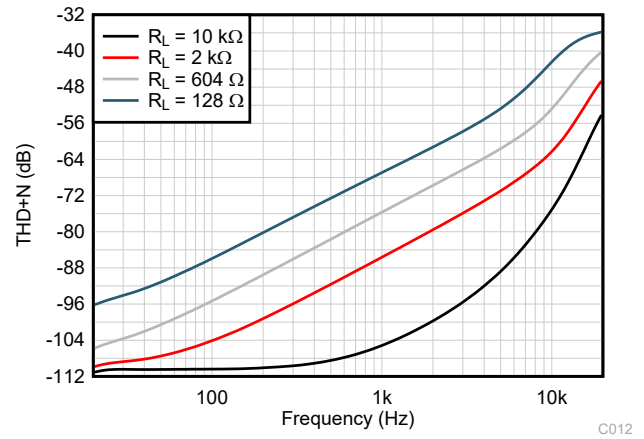
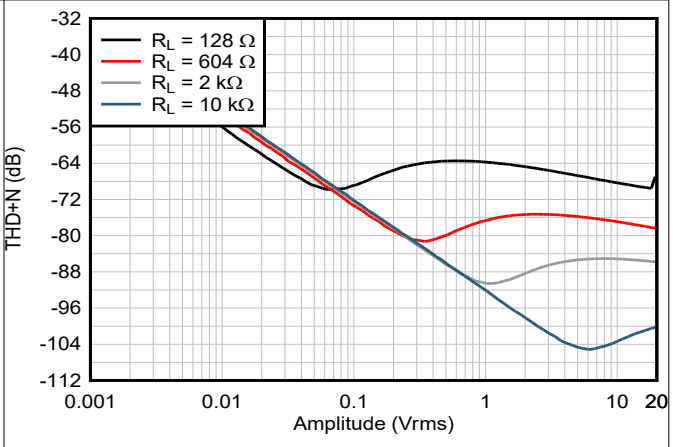


Figure 5-10. Input Voltage Noise Spectral Density vs Frequency, New Die



BW = 80kHz, V_{OUT} = 1V_{RMS}

Figure 5-11. THD+N Ratio vs Frequency, New Die



BW = 80kHz, f = 1kHz

Figure 5-12. THD+N vs Output Amplitude, New Die

5.6 Old Versus New Die Comparison

As of the publication of revision C of this datasheet, Texas Instruments has moved manufacturing of the die for LF412 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “SHE”, for the new die the CSO is “RFB”. The old die information is in the shipping information. The old die information is maintained in this datasheet for comparison purposes, but all new manufacturing has moved to the new die.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 1994) to Revision C (August 2026)	Page
• Changed all instances of *JFET* to *FET* throughout the document	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated datasheet text and format to the latest TI documentation and translations standards	1
• Updated low input bias current from 50pA to ±10pA	1
• Updated low input noise current from 0.01pA/√Hz to 2fA/√Hz	1
• Updated low supply current from 4.5mA to 0.560mA	1
• Updated wide gain bandwidth from 3MHz to 4.5MHz	1
• Updated high slew rate from 13V/µs to 21V/µs	1
• Added *Applications* section	1
• Changed Device Information table to Package Information table	1
• Deleted "...high speed," and "...and a fast slew rate..."	1
• Changed "...the matched high-voltage JFET input..." to "...the input stage..."	1
• Added *Pin Configuration and Functions* section	3
• Added footnotes	4
• Updated Supply voltages to Supply voltage, positive and Supply voltage, negative	4
• Updated Supply voltages to Supply voltage, positive and Supply voltage, negative	4
• Updated Differential input voltage maximum value from 30V to ±30	4
• Removed Differential input voltage minimum value	4
• Updated Supply voltages to Supply voltage, positive and Supply voltage, negative	4

- Changed Input offset voltage typical value from 1mV to ±0.125mV....4
- Changed Average temperature coefficient of input offset voltage typical value from 10µV/°C to ±0.3µV/°C....4
- Changed Input offset current typical value from 25pA to ±10pA....4
- Changed Input bias current typical value from 50pA to ±10pA....4
- Changed Maximum peak output voltage swing typical value from ±13.5V to ±14.950V....4
- Changed Large-signal differential voltage swing minimum value at 25°C from 25V/mV to 88dB and Full Range value from 15V/mV to 83.5dB....4
- Changed Large-signal differential voltage swing typical value at 25°C from 200V/mV to 130dB....4
- Deleted Large-signal differential voltage swing typical value at Full Range....4
- Removed Input resistance....4
- Added Differential and Common-mode Input resistance....4
- Changed Total Supply Current to Supply Current (per amplifier)....4
- Changed Slew Rate typical value from 13V/µs to 21V/µs....5
- Added Slew Rate typical value for V_{ID} = 100mV....5
- Changed Unity-gain bandwidth typical value from 3MHz to 4.5MHz....5
- Removed Unity-gain bandwidth minimum value....5
- Changed Equivalent input noise voltage typical value from 18nV/√Hz to 10.8nV/√Hz....5
- Changed Equivalent input noise voltage typical value from 0.01pA/√Hz to 2fA/√Hz....5
- Added *Typical Characteristics* section....6
- Added *Old Versus New Die Comparison* section....8

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF412 MWC	Active	Production	WAFERSALE (YS) | 0	1 | NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-40 to 85	
LF412CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LF412C
LF412CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF412CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF412CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF412CP
LF412CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF412CP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

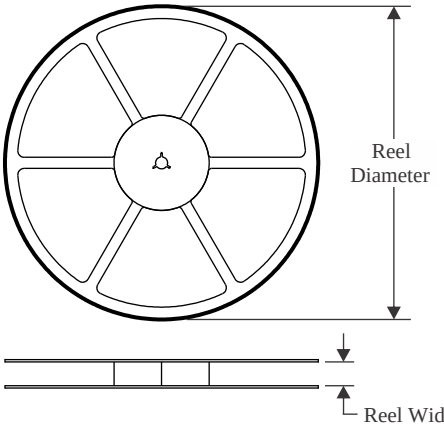
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

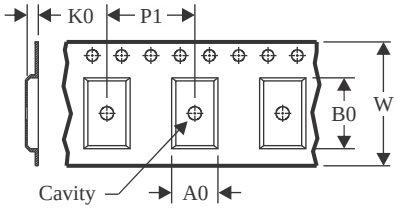
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

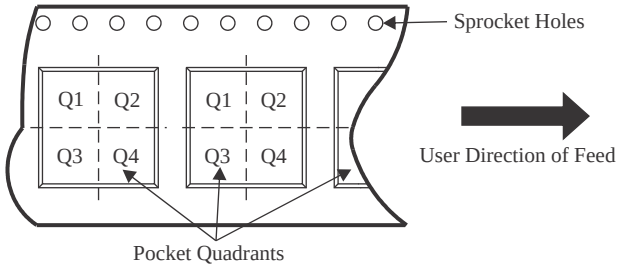


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

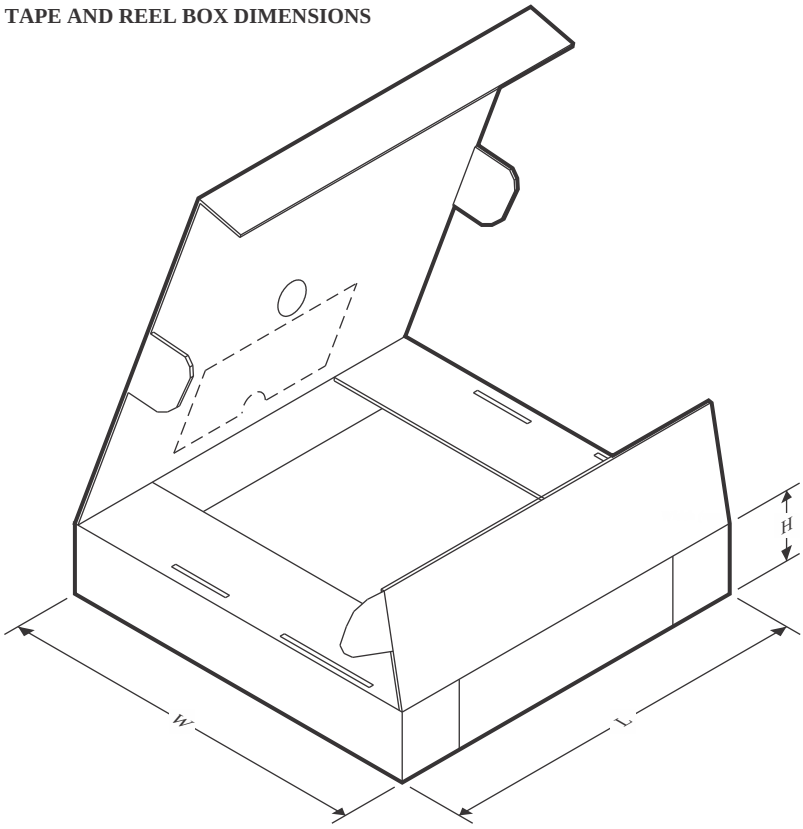
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF412CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LF412CDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

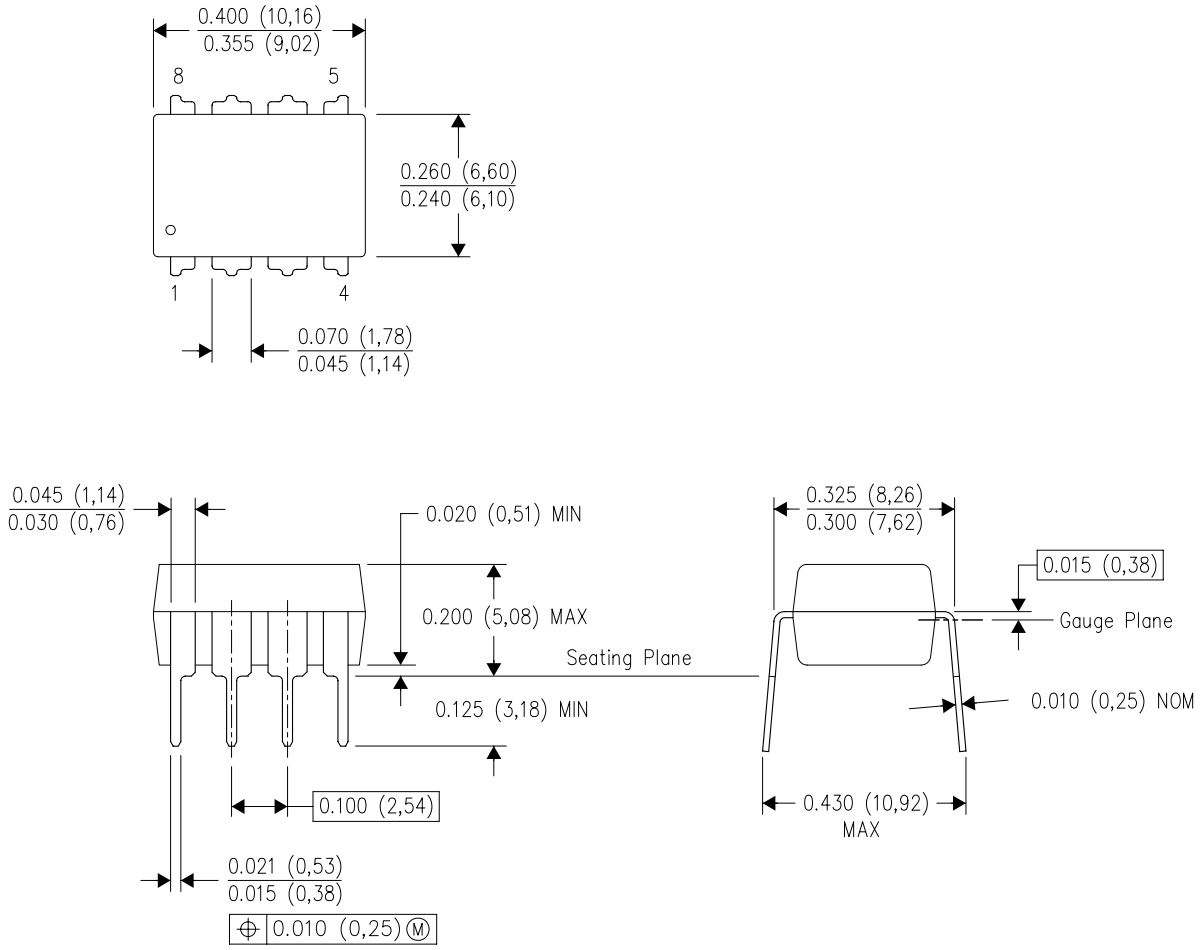
TAPE AND REEL BOX DIMENSIONS



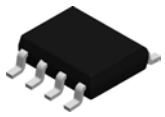
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF412CDR	SOIC	D	8	2500	353.0	353.0	32.0
LF412CDR1G4	SOIC	D	8	2500	353.0	353.0	32.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

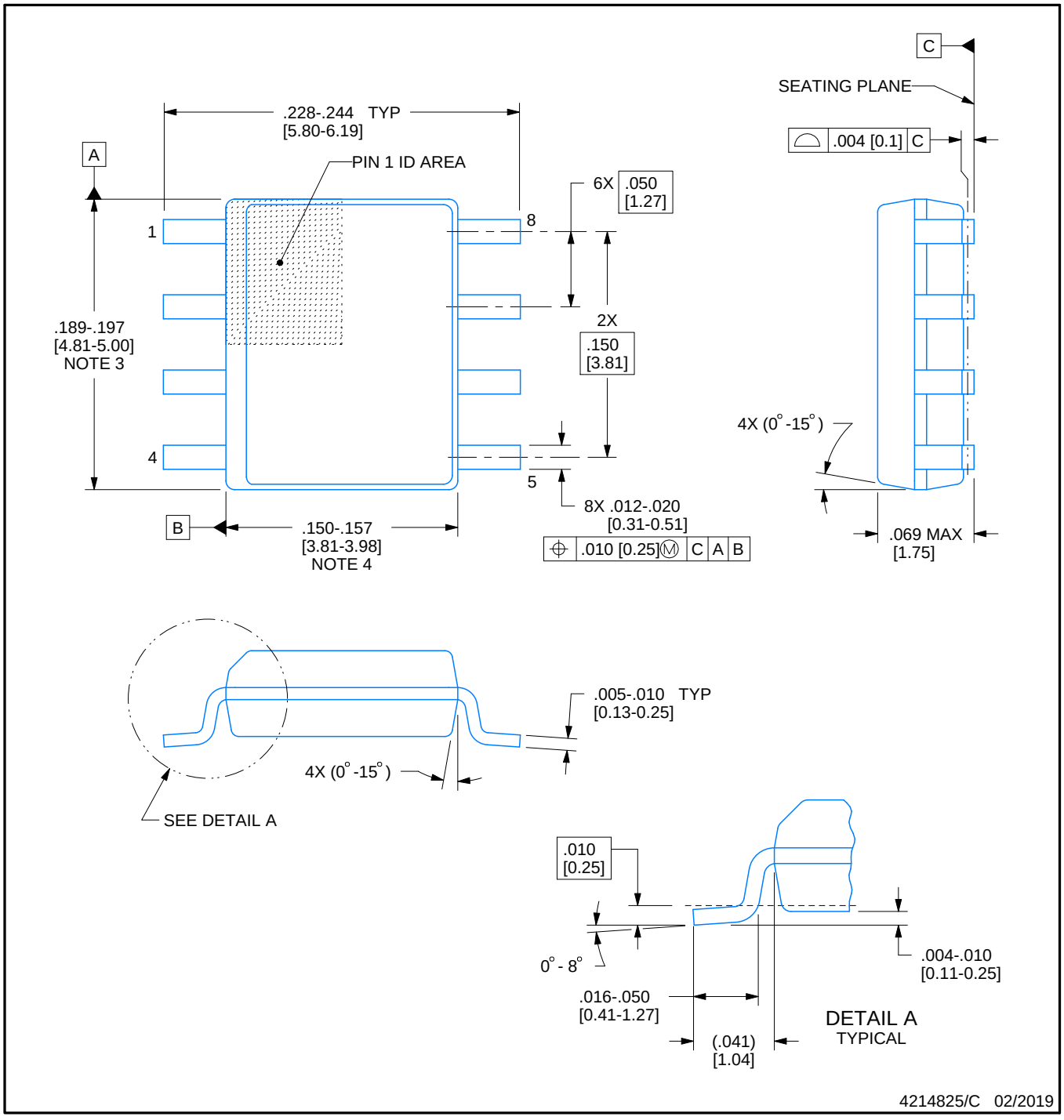


PACKAGE OUTLINE

D0008A

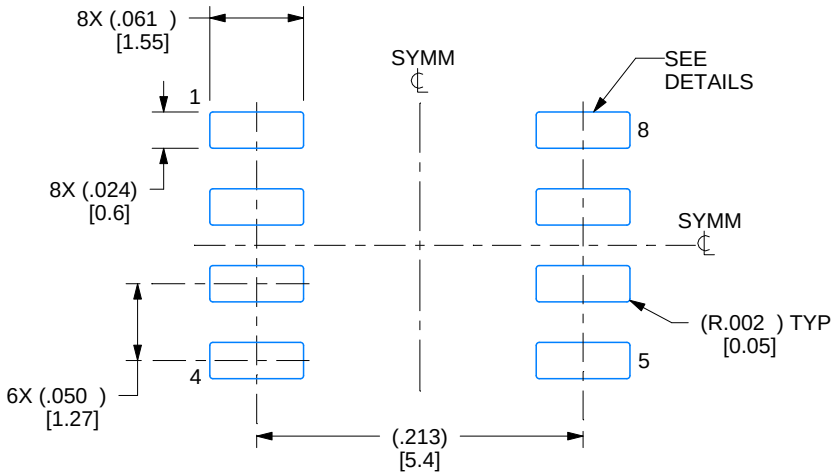
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

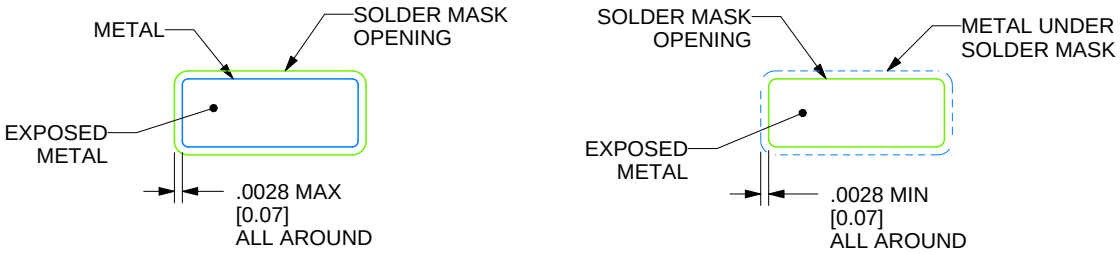


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

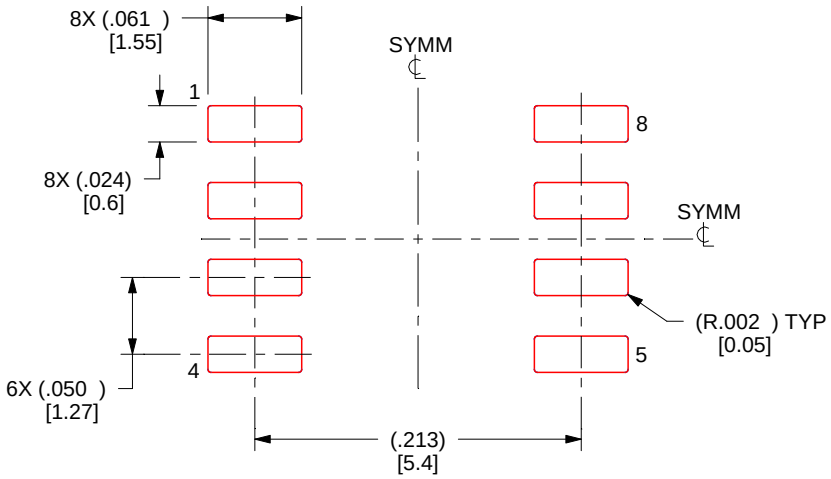
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025