LF442QML Dual Low Power JFET Input Operational Amplifier

Check for Samples: LF442QML

FEATURES

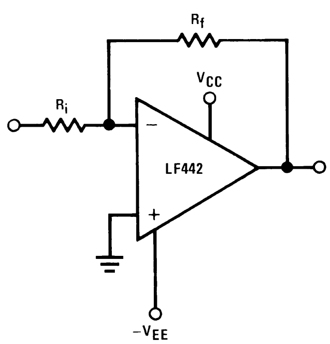
- **1/10 Supply Current of a LM1458: 400 μA (Max)**
- **Low Input Bias Current: 50 pA (Typ)**
- **Low Input Offset Voltage: 1 mV (Typ)**
- **Low Input Offset Voltage Drift: 7 μV/°C (Typ)**
- **High Gain Bandwidth: 1 MHz (Typ)**
- **High Slew Rate: 1 V/μs (Typ)**
- **Low Noise Voltage for Low Power: 35 nV/$\sqrt{Hz}$ (Typ)**
- **Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$ (Typ)**
- **High Input Impedance: $10^{12}\Omega$**

DESCRIPTION

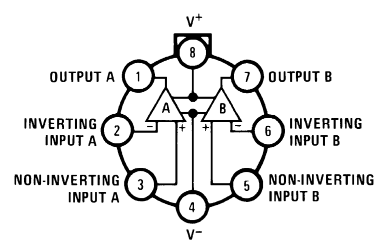
The LF442 dual low power operational amplifier provides many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draws one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming ensures very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Typical Connection



Connection Diagram

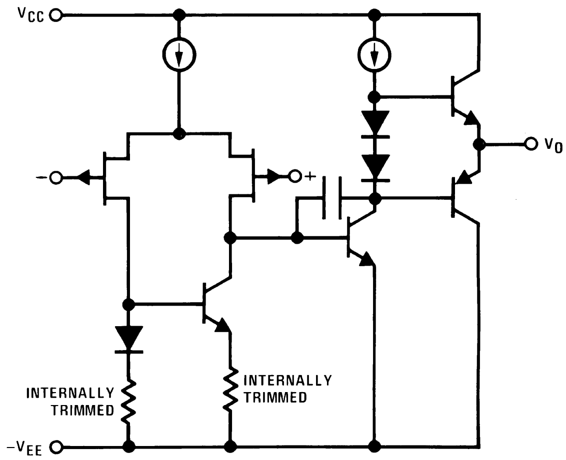


Pin 4 connected to case

Figure 1. Top View TO-99 Package See Package Number LMC

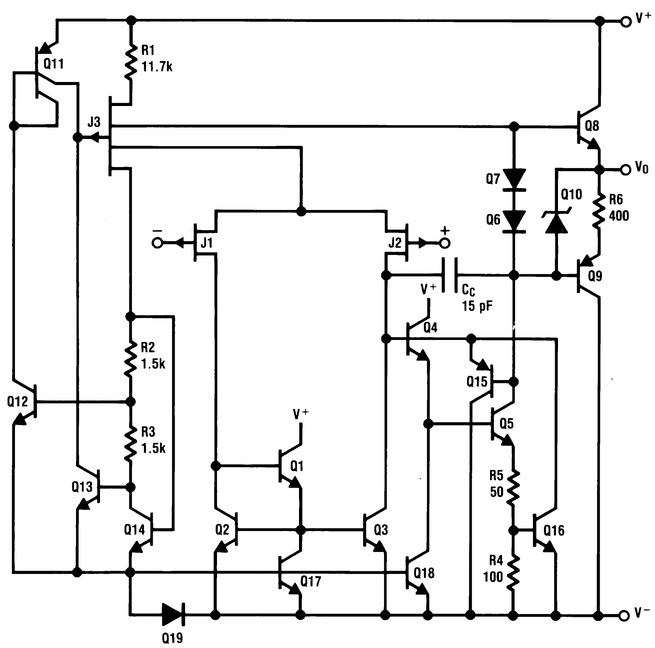
Simplified Schematic

Figure 2. 1/2 Dual



Detailed Schematic

Figure 3. 1/2 Dual



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)]

Supply Voltage			±18V
Differential Input Voltage			±30V
Input Voltage Range[(2)]			±15V
Output Short Circuit Duration[(3)]			Continuous
Maximum Power Dissipation[(4)]			900mW
T_J max			150°C
Thermal Resistance	θ_{JA}	Still Air	161°C/W
		500LF/Min Air flow	87°C/W
	θ_{JC}		33°C/W
Operating Temperature Range			$-55°C \leq T_A \leq 125°C$
Storage Temperature Range			$-65°C \leq T_A \leq 150°C$
Lead Temperature (Soldering, 10 sec.)			260°C
ESD Tolerance[(5)]			500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Human Body Model, 100pF discharged through 1.5KΩ

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LF442 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V_S = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current				500	µA	1, 2, 3
V_{IO}	Input Offset Voltage	$R_S = 10K\Omega$		-5.0	5.0	mV	1
				-7.5	7.5	mV	2, 3
$\pm I_{IB}$	Input Bias Current				0.1	nA	1
					20	nA	2
I_{IO}	Input Offset Current			-0.05	0.05	nA	1
				-10	10	nA	2
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11V$, $R_S = 10K$		70		dB	1, 2, 3
PSRR	Power Supply Rejection Ratio	$V_S^+ = +15V$ to $+6V$, $V_S^- = -15V$		70		dB	1, 2, 3
		$V_S^- = -15V$ to $-6V$, $V_S^+ = +15V$		70		dB	1, 2, 3
$+A_{VS}$	Large Signal Voltage Gain	$V_O = 0V$ to $+10V$, $R_L = 10K\Omega$	See (1)	25		V/mV	4
				15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	$V_O = 0V$ to $-10V$, $R_L = 10K\Omega$	See (1)	25		V/mV	4
				15		V/mV	5, 6
V_O^+	Output Voltage Swing	$V_I = \pm11V$, $R_L = 10K$		12		V	4, 5, 6
V_O^-	Output Voltage Swing	$V_I = \pm11V$, $R_L = 10K$			-12	V	4, 5, 6
V_{CM}	Input Common Mode Voltage Range		See (2)	11	-11	V	4, 5, 6

(1) V/mV in units column is equivalent to K in datalog.
(2) Parameter tested go-no-go only, specified by CMRR test..

AC Parameters

The following conditions apply, unless otherwise specified. $V_S = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR^+	Slew Rate	$V_O = -5V$ to $+5V$, $A_V = 1$, $R_L = 2K\Omega$, C_L - 100pF		0.6		V/µS	7
SR^-	Slew Rate	$V_O = +5V$ to $-5V$, $A_V = 1$, $R_L = 2K\Omega$, C_L - 100pF		0.6		V/µS	7
GBW	Gain Band Width	$V_I = 50mV$, $f = 20KHz$		0.6		MHz	7

Typical Performance Characteristics

Input Bias Current

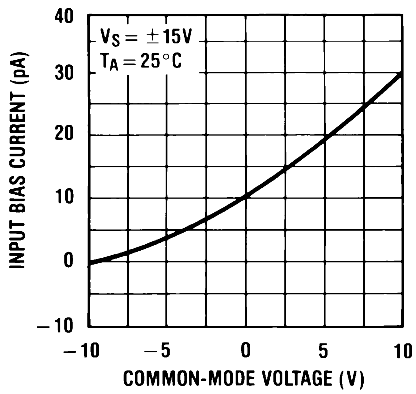


Figure 4.

Input Bias Current

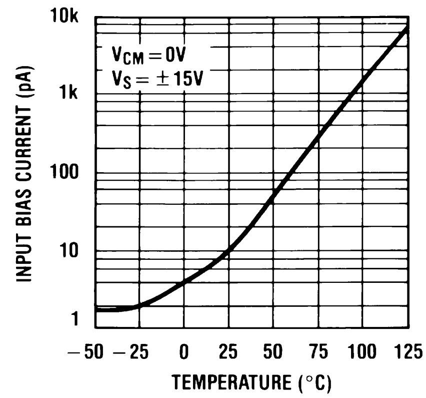


Figure 5.

Supply Current

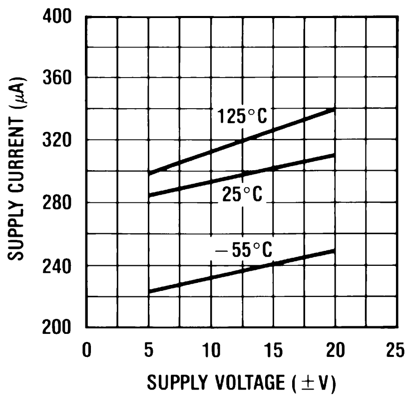


Figure 6.

Positive Common-Mode Input Voltage Limit

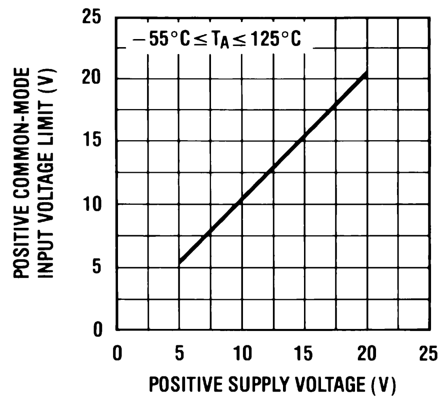


Figure 7.

Negative Common-Mode Input Voltage Limit

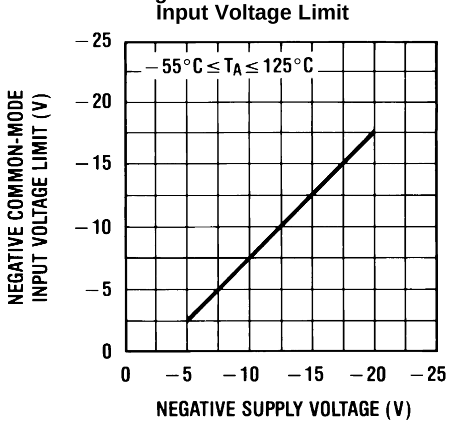


Figure 8.

Positive Current Limit

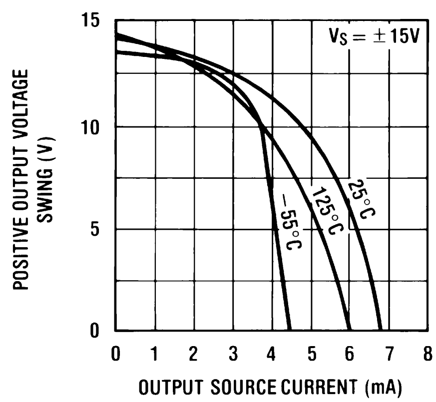


Figure 9.

Typical Performance Characteristics (continued)

Negative Current Limit

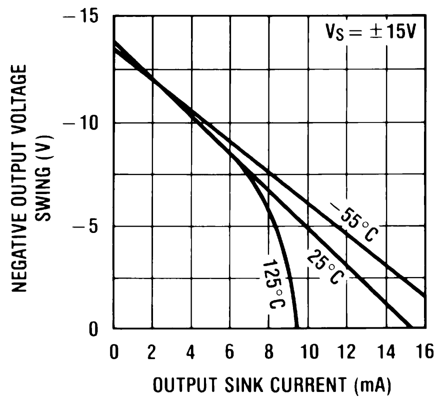


Figure 10.

Output Voltage Swing

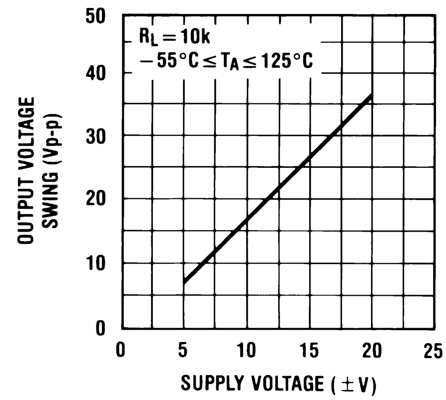


Figure 11.

Output Voltage Swing

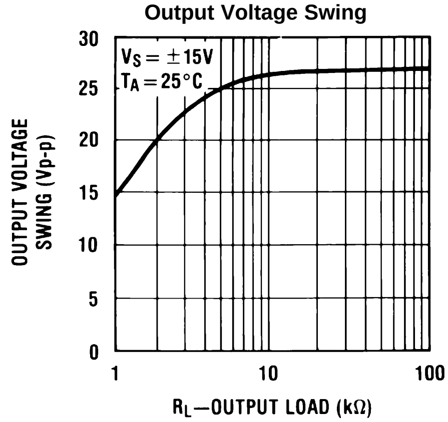


Figure 12.

Gain Bandwidth

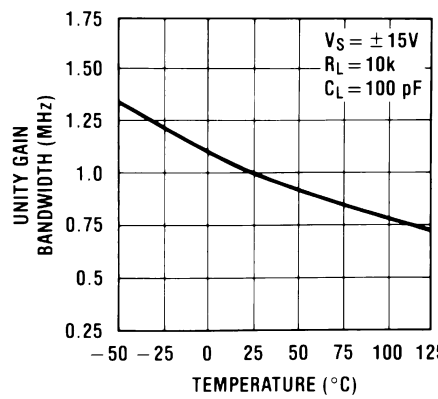


Figure 13.

Bode Plot

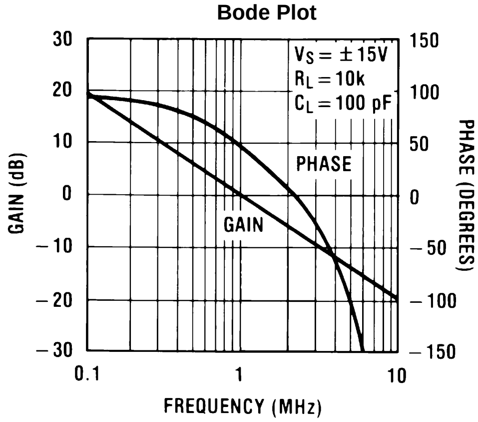


Figure 14.

Slew Rate

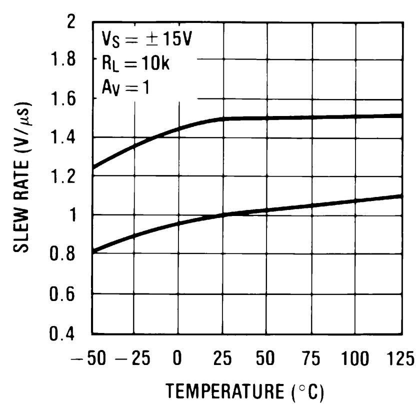


Figure 15.

Typical Performance Characteristics (continued)

Distortion vs Frequency

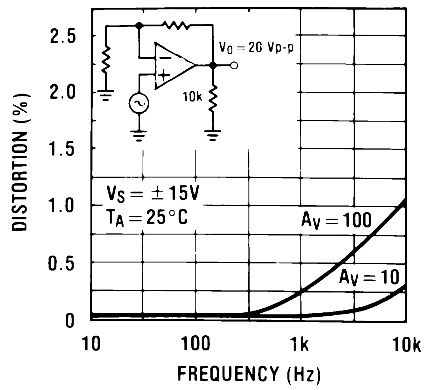


Figure 16.

Undistorted Output Voltage Swing

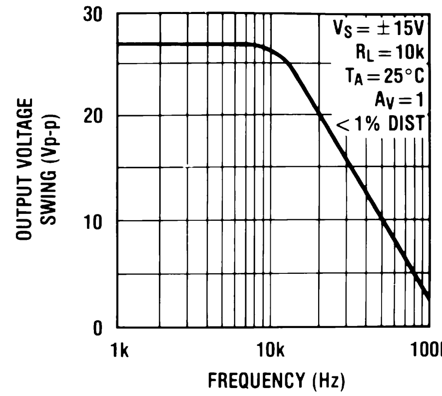


Figure 17.

Open Loop Frequency Response

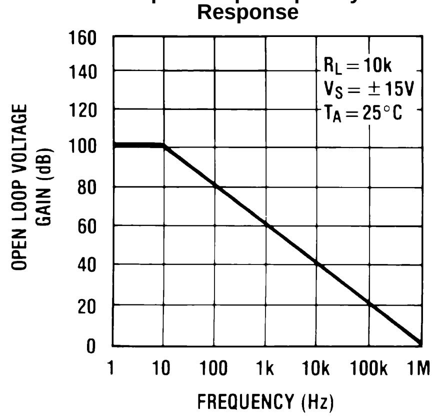


Figure 18.

Common-Mode Rejection Ratio

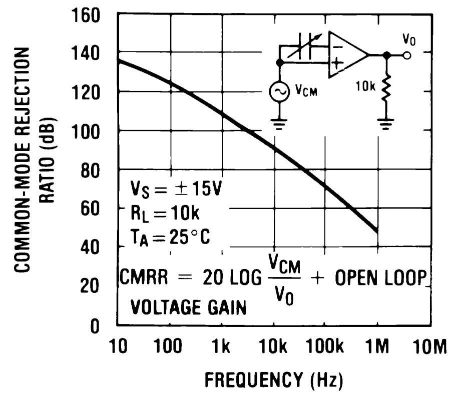


Figure 19.

Power Supply Rejection Ratio

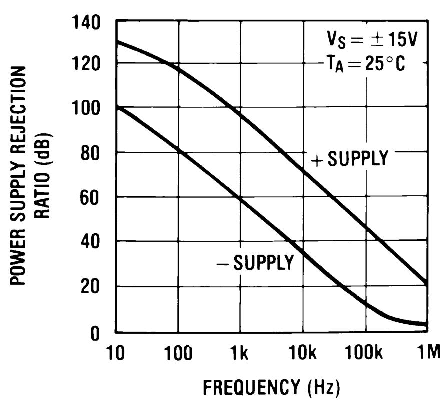


Figure 20.

Equivalent Input Noise Voltage

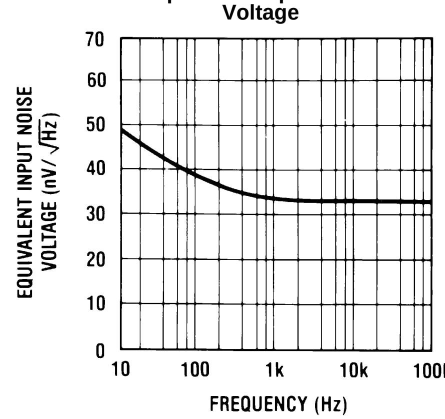


Figure 21.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain

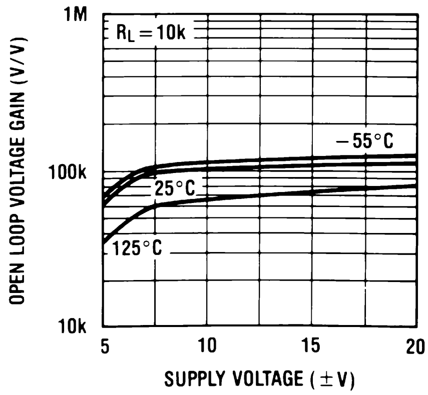


Figure 22.

Output Impedance

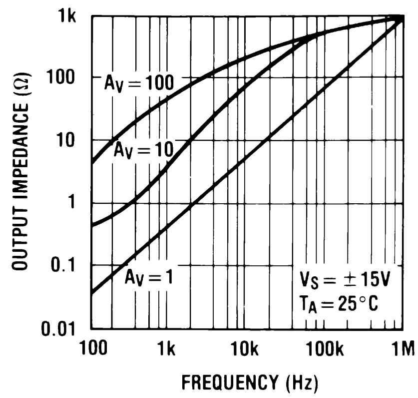


Figure 23.

Inverter Settling Time

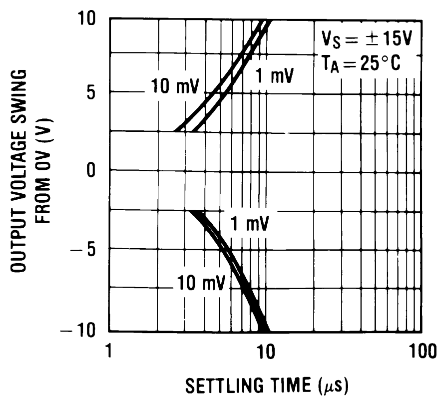
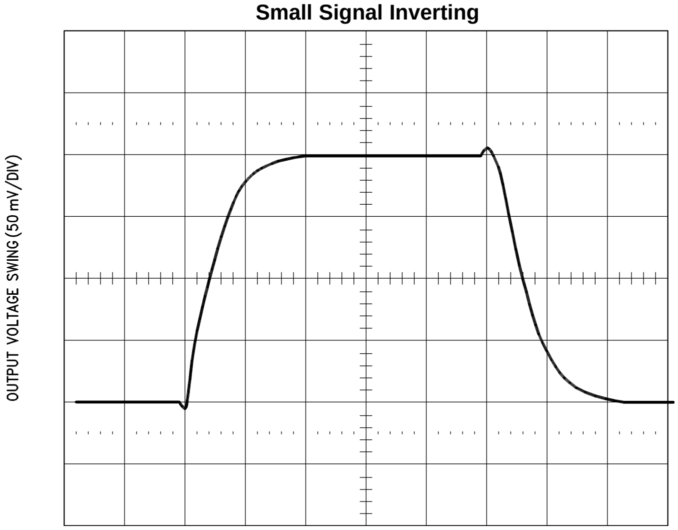


Figure 24.

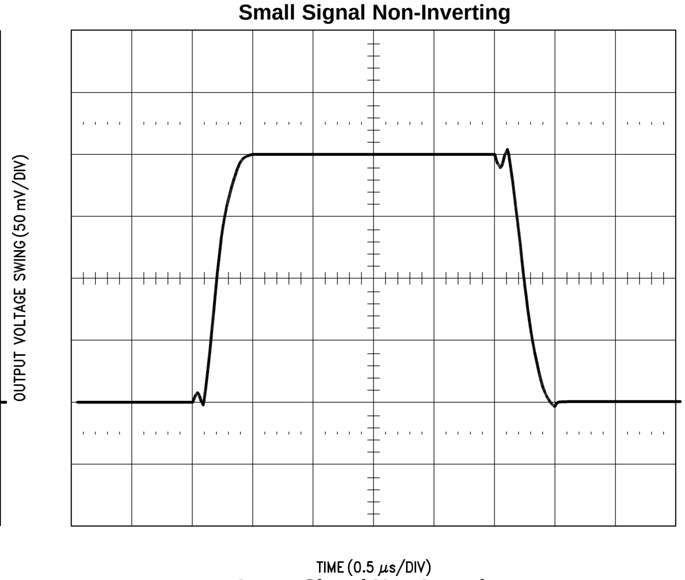
Pulse Response

R_L = 10 kΩ, C_L = 10 pF

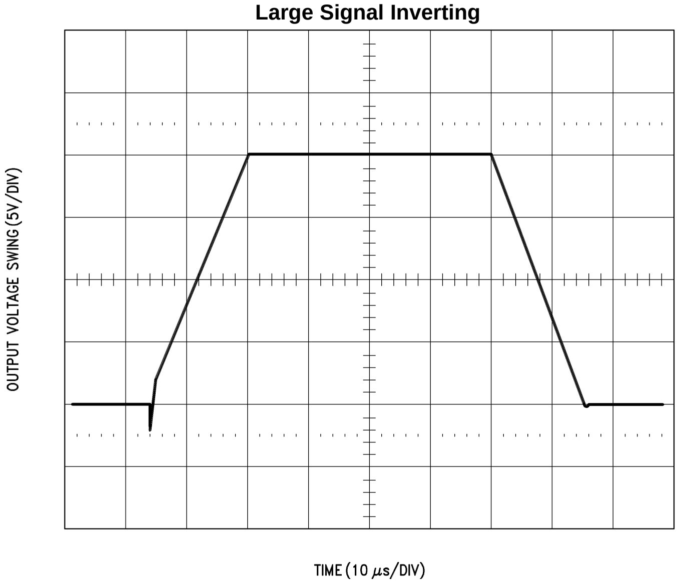
Small Signal Inverting



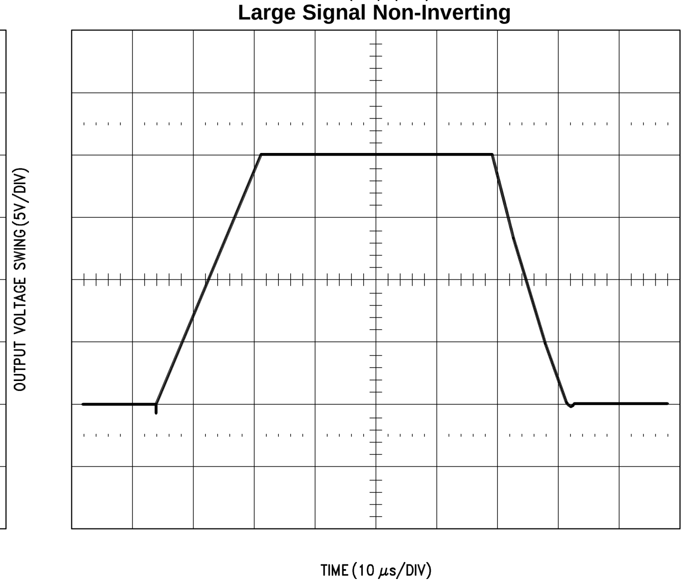
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting



APPLICATION HINTS

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

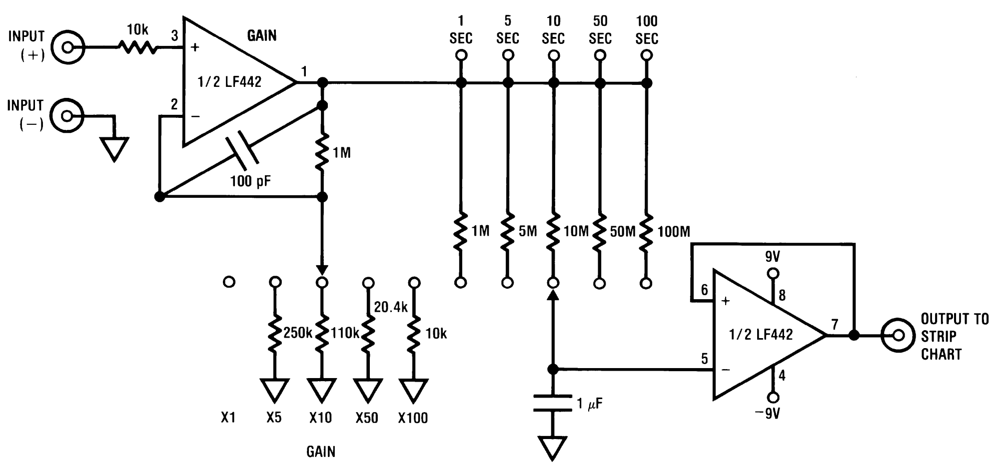
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

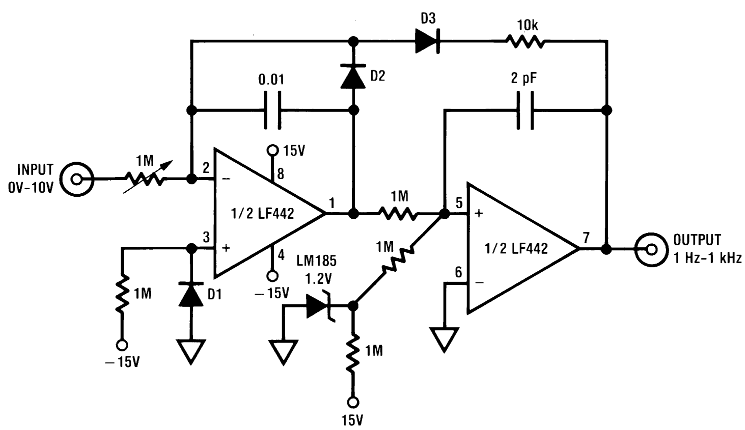
Typical Applications

Figure 25. Battery Powered Strip Chart Preamplifier



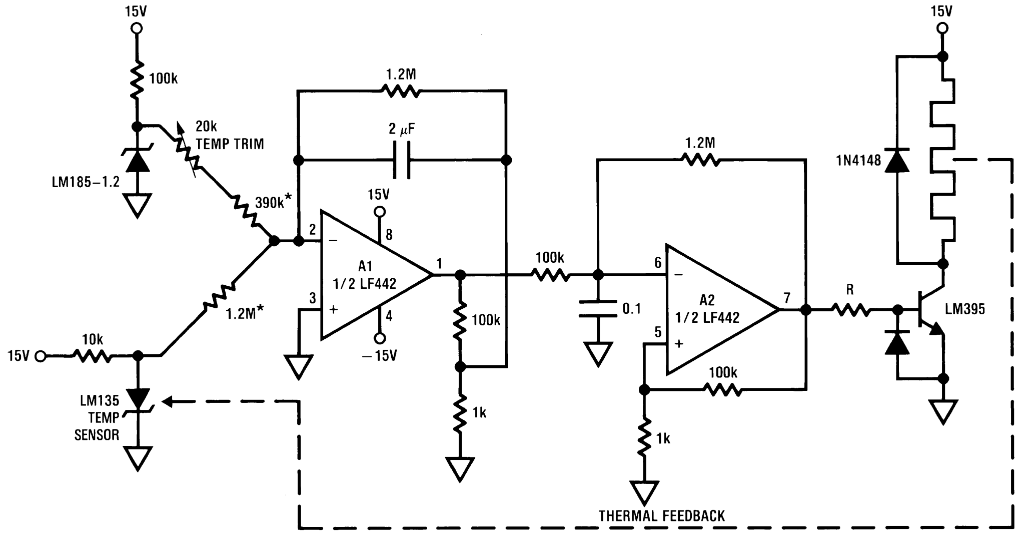
Runs from 9v batteries (±9V supplies)
Fully settable gain and time constant
Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

Figure 26. “No FET” Low Power V→F Converter



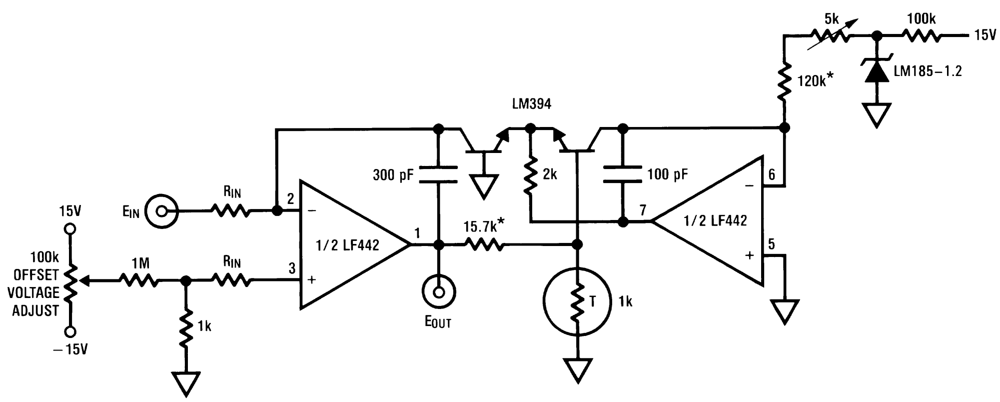
Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

Figure 27. High Efficiency Crystal Oven Controller



- $T_{control}$= 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor

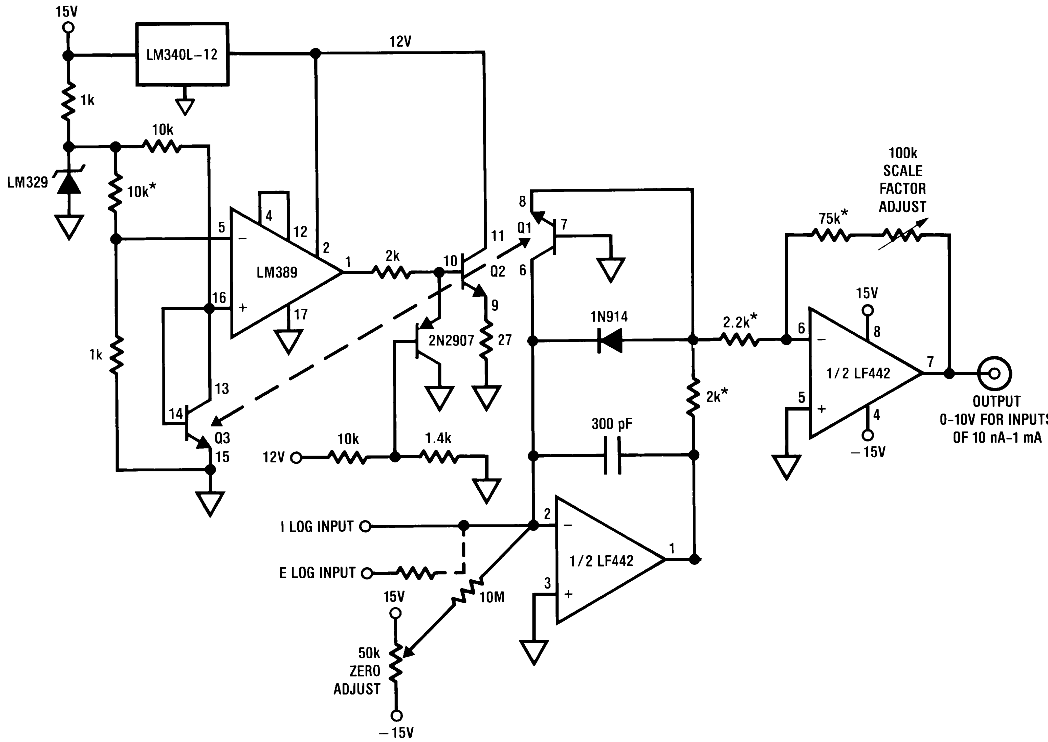
Figure 28. Conventional Log Amplifier



$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81
Trim 5k for 10 μA through the 5k–120k combination
*1% film resistor

Figure 29. Unconventional Log Amplifier



Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

Table 2. Revision History

Date Released	Revision	Section	Changes
12/16/2010	A	New release to corporate format	1 MDS datasheet converted into one corporate datasheet format. MNLF442M-X Rev 0A1 will be archived.
03/26/2013	A	All Sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF442MH/883	Obsolete	Production	TO-99 (LMC) | 8	-	-	Call TI	Call TI	-	LF442MH/883 5962-9763301QGA Q ACO 5962-9763301QGA Q >T

[(1)] **Status:** For more details on status, see our product life cycle.

[(2)] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[(3)] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[(4)] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[(5)] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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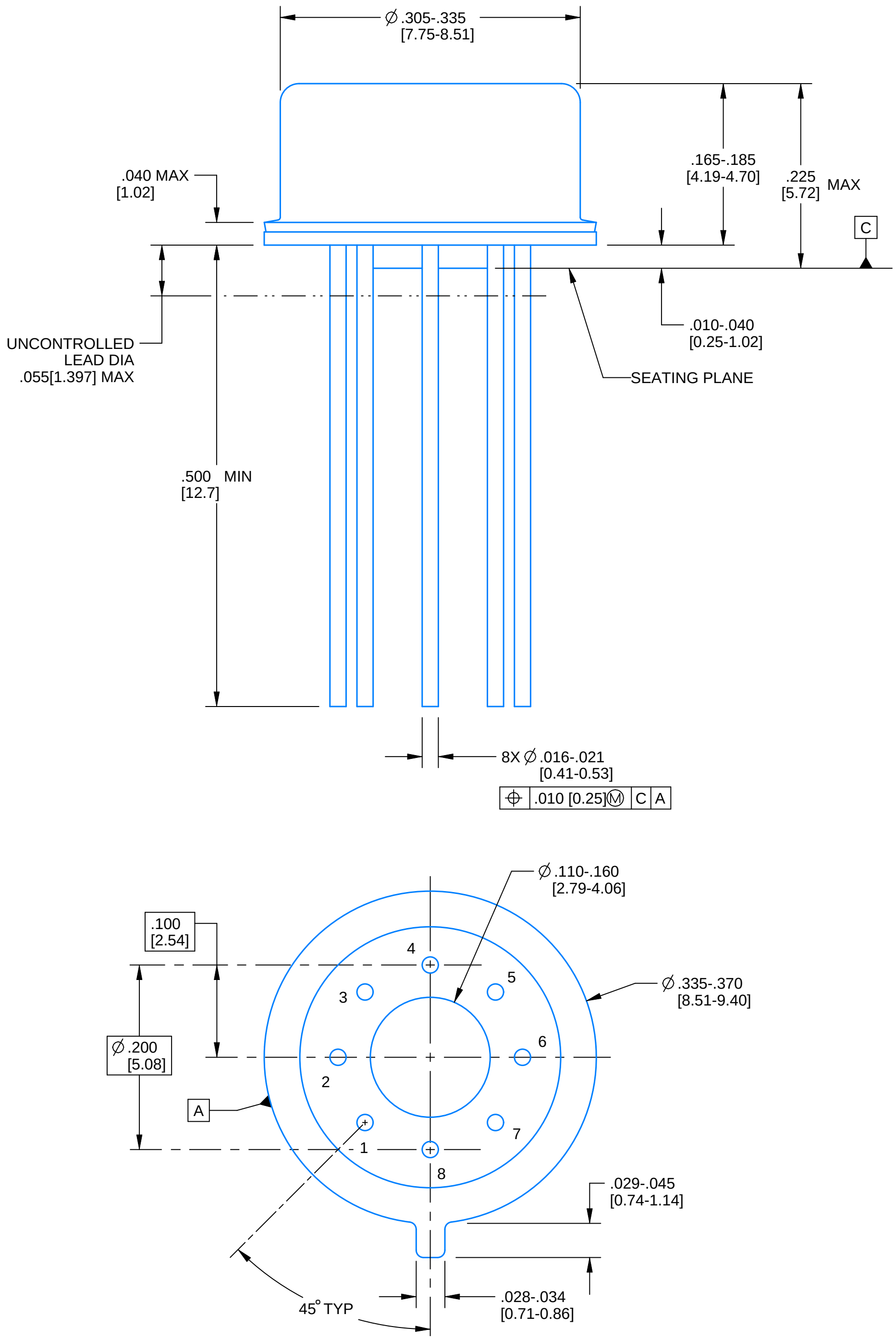
LMC0008A

TO-CAN - 5.72 mm max height

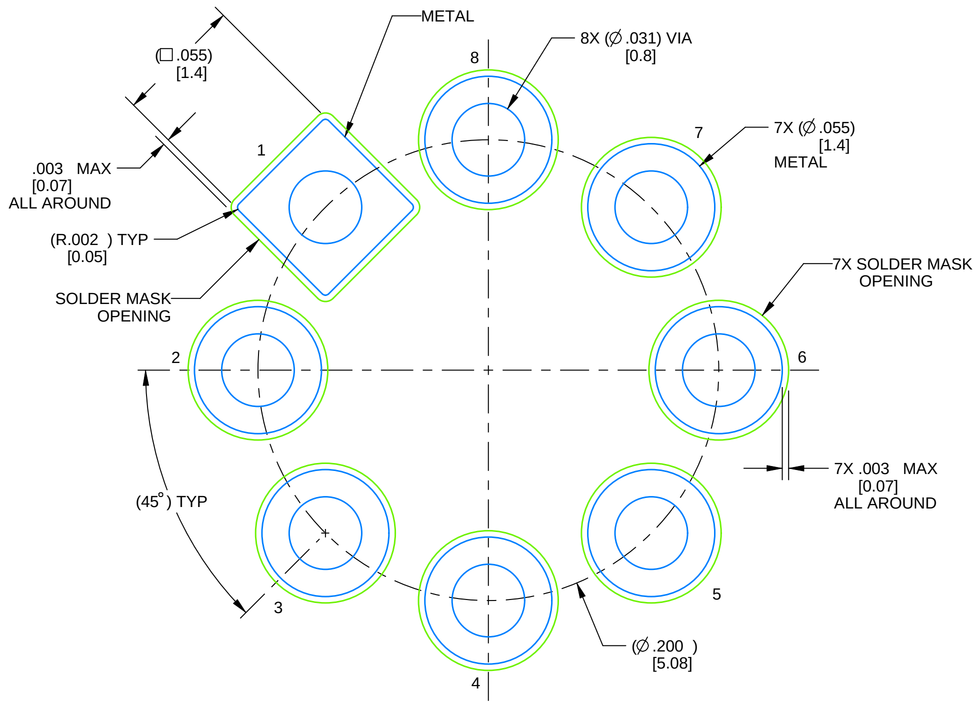
TRANSISTOR OUTLINE



4220610/B 09/2024

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X