

## LM111JAN Voltage Comparator

Check for Samples: [LM111JAN](#)

### FEATURES

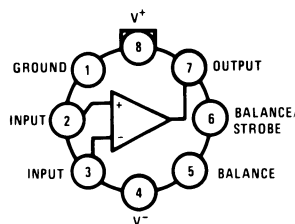
- Operates from Single 5V Supply
- Input Current: 200 nA max. Over Temperature
- Offset Current: 20 nA max. Over Temperature
- Differential Input Voltage Range:  $\pm 30V$
- Power Consumption: 135 mW at  $\pm 15V$
- Power Supply Voltage, single 5V to  $\pm 15V$
- Offset Voltage Null Capability
- Strobe Capability

### DESCRIPTION

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages: from standard  $\pm 15V$  op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

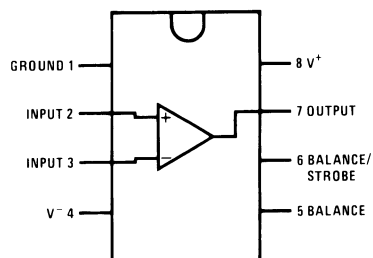
Both the inputs and the outputs of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

### Connection Diagrams

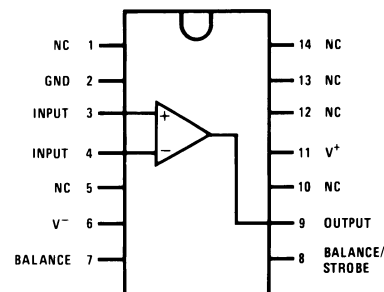


**Note:** Pin 4 connected to case

**Figure 1. Metal Can Package  
Top View  
See Package Number LMC0008C**



**Figure 2. Dual-In-Line Package  
Top View  
See Package Number NAB0008A**



**Figure 3. Dual-In-Line Package  
Top View  
See Package Number J0014A**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

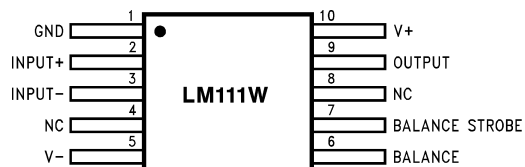
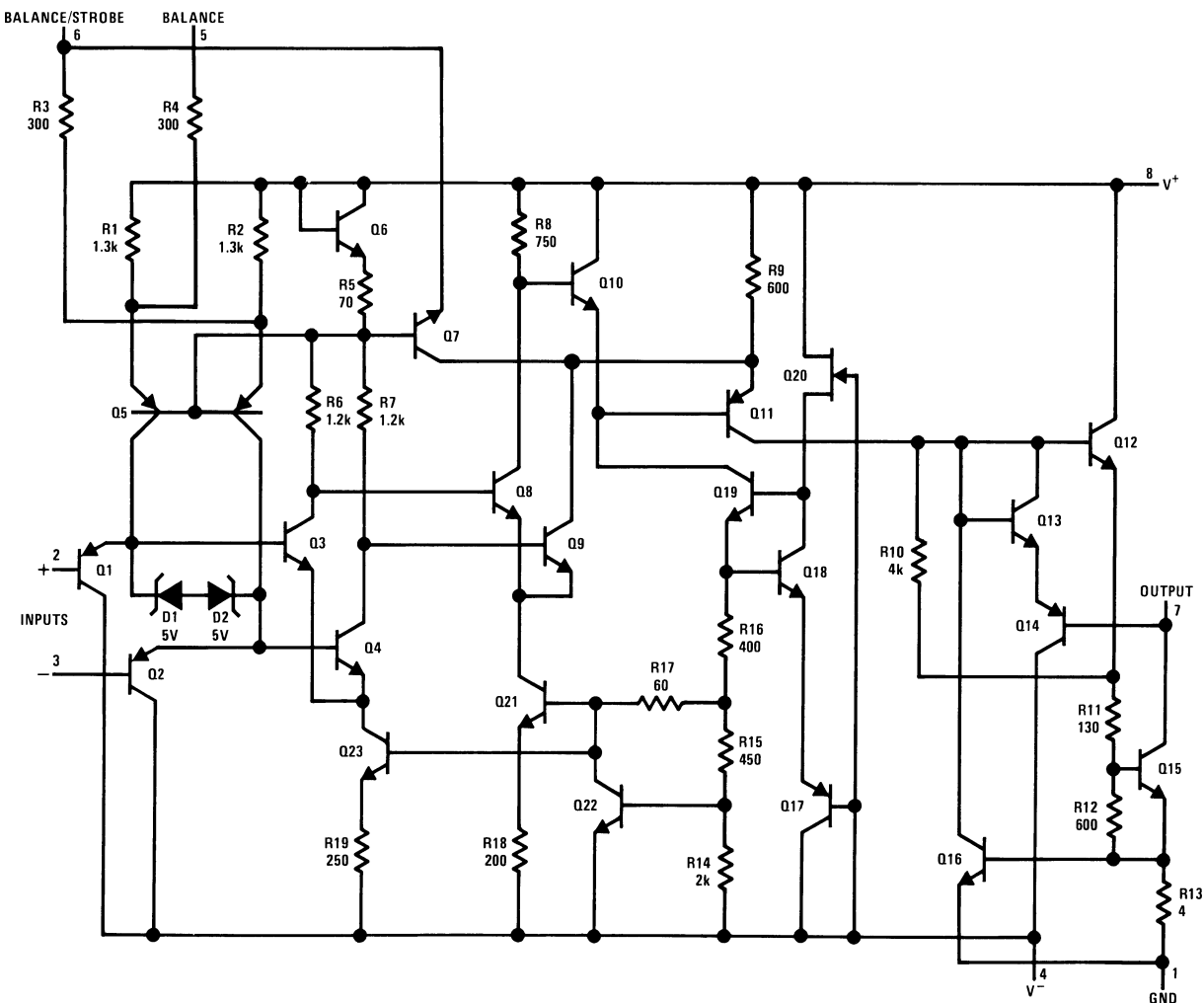


Figure 4. See Package Number NAD0010A, NAC0010A

## Schematic Diagram



**Note:** Pin connections shown on schematic diagram are for LMC0008C package.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)</sup>**

Positive Supply Voltage			+30.0V
Negative Supply Voltage			-30.0V
Total Supply Voltage			36V
Output to Negative Supply Voltage			50V
GND to Negative Supply Voltage			30V
Differential Input Voltage			±30V
Sink Current			50mA
Input Voltage <sup>(2)</sup>			±15V
Power Dissipation <sup>(3)</sup>	8 LD Cerdip		400mW @ 25°C
	8 LD Metal Can		330mW @ 25°C
	10 LD CERPACK		330mW @ 25°C
	10 LD Ceramic SOIC		330mW @ 25°C
	14 LD Cerdip		400mW @ 25°C
Output Short Circuit Duration			10 seconds
Maximum Strobe Current			10mA
Operating Temperature Range			-55°C ≤ T <sub>A</sub> ≤ 125°C
Thermal Resistance	θ <sub>JA</sub>	8 LD Cerdip (Still Air @ 0.5W)	120°C/W
		8 LD Cerdip (500LF/Min Air flow @ 0.5W)	76°C/W
		8 LD Metal Can (Still Air @ 0.5W)	150°C/W
		8 LD Metal Can (500LF/Min Air flow @ 0.5W)	92°C/W
		10 Ceramic SOIC (Still Air @ 0.5W)	231°C/W
		10 Ceramic SOIC (500LF/Min Air flow @ 0.5W)	153°C/W
		10 CERPACK (Still Air @ 0.5W)	231°C/W
		10 CERPACK (500LF/Min Air flow @ 0.5W)	153°C/W
		14 LD Cerdip (Still Air @ 0.5W)	120°C/W
		14 LD Cerdip (500LF/Min Air flow @ 0.5W)	65°C/W
	θ <sub>JC</sub>	8 LD Cerdip	35°C/W
		8 LD Metal Can Pkg	40°C/W
		10 LD Ceramic SOIC	60°C/W
		10 LD CERPACK	60°C/W
		14 LD Cerdip	35°C/W
Storage Temperature Range			-65°C ≤ T <sub>A</sub> ≤ 150°C
Maximum Junction Temperature			175°C
Lead Temperature (Soldering, 60 seconds)			300°C
Voltage at Strobe Pin			V <sup>+</sup> -5V
Package Weight (Typical)	8 LD Metal Can		965mg
	8 LD Cerdip		1100mg
	10 LD CERPACK		250mg
	10 LD Ceramic SOIC		225mg
	14 LD Cerdip		TBD
ESD Rating <sup>(4)</sup>			300V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) This rating applies for ±15V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>Jmax</sub> (maximum junction temperature), θ<sub>JA</sub> (package junction to ambient thermal resistance), and T<sub>A</sub> (ambient temperature). The maximum allowable power dissipation at any temperature is P<sub>Dmax</sub> = (T<sub>Jmax</sub> - T<sub>A</sub>)/θ<sub>JA</sub> or the number given in the Absolute Maximum Ratings, whichever is lower.
- (4) Human body model, 1.5 kΩ in series with 100 pF.

## Recommended Operating Conditions

Supply Voltage	$V_{CC} = \pm 15V_{DC}$
Operating Temperature Range	$-55^{\circ}C \leq T_A \leq 125^{\circ}C$

## Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature ( $^{\circ}C$ )
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

## LM111 JAN Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.

DC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$V_{IO}$	Input Offset Voltage	$V_I = 0V$ , $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
$V_{IO R}$	Raised Input Offset Voltage	$V_I = 0V$ , $R_S = 50\Omega$	See <sup>(1)</sup>	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50\Omega$	See <sup>(1)</sup>	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50\Omega$	See <sup>(1)</sup>	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
$I_{IO}$	Input Offset Current	$V_I = 0V$ , $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3

(1) Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to  $+V_{CC}$ .

## LM111 JAN Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified.

DC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{IO}R$	Raised Input Offset Current	$V_I = 0V$ , $R_S = 50K\Omega$	See <sup>(1)</sup>	-25	+25	nA	1, 2
				-50	+50	nA	3
$\pm I_{IB}$	Input Bias Current	$V_I = 0V$ , $R_S = 50K\Omega$		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50K\Omega$		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50K\Omega$		-150	0.1	nA	1, 2
				-200	0.1	nA	3
$V_{OSt}$	Collector Output Voltage (Strobe)	$+V_I = Gnd$ , $-V_I = 15V$ , $I_{St} = -3mA$ , $R_S = 50\Omega$	See <sup>(2)</sup>	14		V	1, 2, 3
CMRR	Common Mode Rejection	$-28V \leq -V_{CC} \leq -0.5V$ , $R_S = 50\Omega$ , $2V \leq +V_{CC} \leq 29.5V$ , $R_S = 50\Omega$ , $-14.5V \leq V_{CM} \leq 13V$ , $R_S = 50\Omega$		80		dB	1, 2, 3
$V_{OL}$	Low Level Output Voltage	$+V_{CC} = 4.5V$ , $-V_{CC} = Gnd$ , $I_O = 8mA$ , $\pm V_I = 0.5V$ , $V_{ID} = -6mV$	See <sup>(3)</sup>		0.4	V	1, 2, 3
		$+V_{CC} = 4.5V$ , $-V_{CC} = Gnd$ , $I_O = 8mA$ , $\pm V_I = 3V$ , $V_{ID} = -6mV$	See <sup>(3)</sup>		0.4	V	1, 2, 3
		$I_O = 50mA$ , $\pm V_I = 13V$ , $V_{ID} = -5mV$	See <sup>(3)</sup>		1.5	V	1, 2, 3
		$I_O = 50mA$ , $\pm V_I = -14V$ , $V_{ID} = -5mV$	See <sup>(3)</sup>		1.5	V	1, 2, 3
$I_{CEX}$	Output Leakage Current	$+V_{CC} = 18V$ , $-V_{CC} = -18V$ , $V_O = 32V$		-1.0	10	nA	1
				-1.0	500	nA	2
$I_{IL}$	Input Leakage Current	$+V_{CC} = 18V$ , $-V_{CC} = -18V$ , $+V_I = +12V$ , $-V_I = -17V$		-5.0	500	nA	1, 2, 3
		$+V_{CC} = 18V$ , $-V_{CC} = -18V$ , $+V_I = -17V$ , $-V_I = +12V$		-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient Input Offset Voltage	$25^\circ C \leq T \leq 125^\circ C$	See <sup>(4)</sup>	-25	25	$\mu V/^\circ C$	2
		$-55^\circ C \leq T \leq 25^\circ C$	See <sup>(4)</sup>	-25	25	$\mu V/^\circ C$	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient Input Offset Current	$25^\circ C \leq T \leq 125^\circ C$	See <sup>(4)</sup>	-100	100	$pA/^\circ C$	2
		$-55^\circ C \leq T \leq 25^\circ C$	See <sup>(4)</sup>	-200	200	$pA/^\circ C$	3
$I_{OS}$	Short Circuit Current	$V_O = 5V$ , $t \leq 10mS$ , $-V_I = 0.1V$ , $+V_I = 0V$			200	mA	1
					150	mA	2
					250	mA	3
$+V_{IO} \text{ adj.}$	Input Offset Voltage (Adjustment)	$V_O = 0V$ , $V_I = 0V$ , $R_S = 50\Omega$		5.0		mV	1
$-V_{IO} \text{ adj.}$	Input Offset Voltage (Adjustment)	$V_O = 0V$ , $V_I = 0V$ , $R_S = 50\Omega$			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	$R_L = 600\Omega$	See <sup>(5)</sup>	10		V/mV	4
			See <sup>(5)</sup>	8.0		V/mV	5, 6

(2)  $I_{ST} = -2mA$  at  $-55^\circ C$

(3)  $V_{ID}$  is voltage difference between inputs.

(4) Calculated parameter.

(5) Datalog reading in  $K=V/mV$ .

## LM111 JAN Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$t_{R_{LHC}}$	Response Time (Collector Output)	$V_{OD}(\text{Overdrive}) = -5mV$ , $C_L = 50pF$ , $V_I = -100mV$			300	nS	7, 8B
					640	nS	8A
$t_{R_{HLC}}$	Response Time (Collector Output)	$V_{OD}(\text{Overdrive}) = 5mV$ , $C_L = 50pF$ , $V_I = 100mV$			300	nS	7, 8B
					500	nS	8A

## LM111 JAN Electrical Characteristics DC Drift Parameters

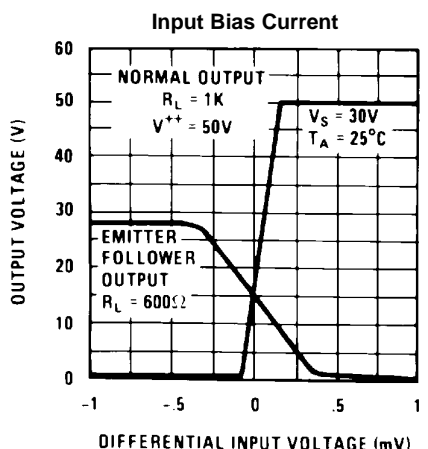
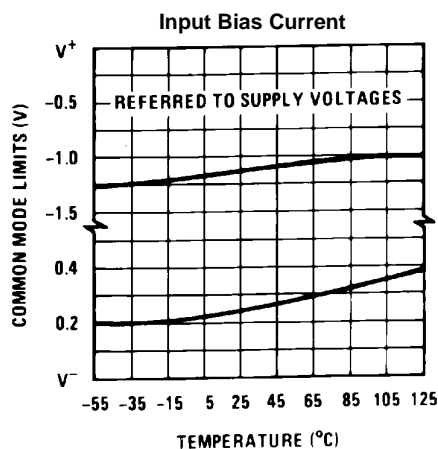
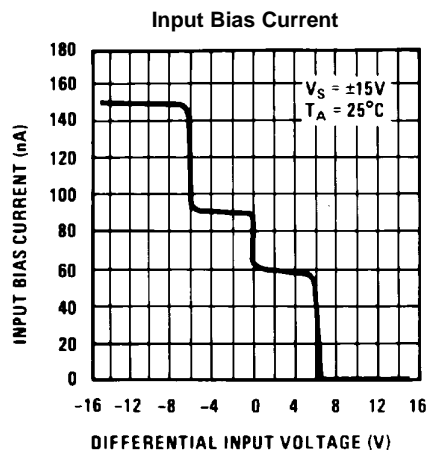
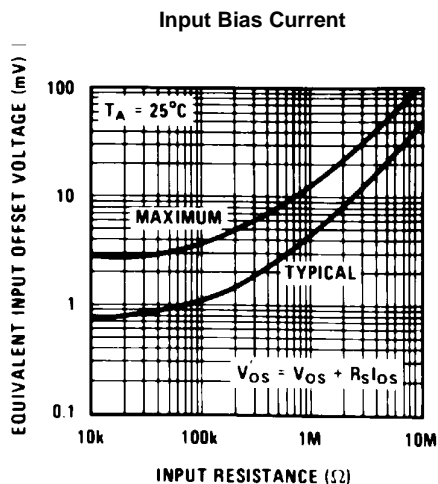
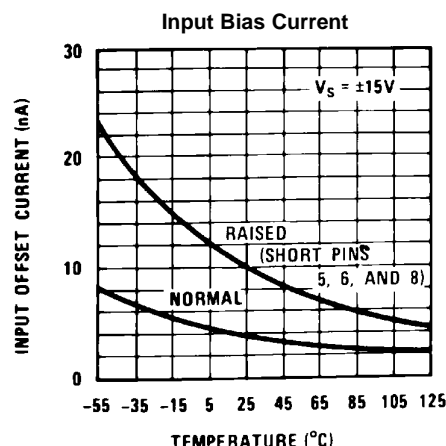
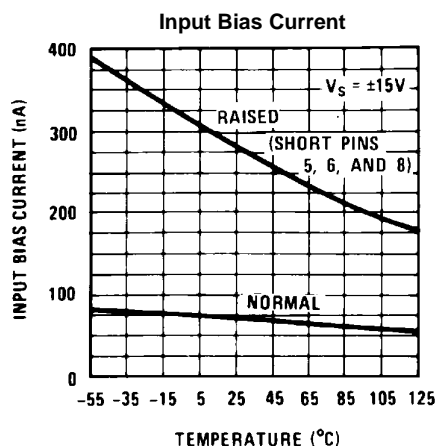
The following conditions apply, unless otherwise specified.

DC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0$

Delta calculations performed on JANS devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$V_{IO}$	Input Offset Voltage	$V_I = 0V$ , $R_S = 50\Omega$		-0.5	0.5	mV	1
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50\Omega$		-0.5	0.5	mV	1
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50\Omega$		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	$V_I = 0V$ , $R_S = 50K\Omega$		-12.5	12.5	nA	1
		$+V_{CC} = 29.5V$ , $-V_{CC} = -0.5V$ , $V_I = 0V$ , $V_{CM} = -14.5V$ , $R_S = 50K\Omega$		-12.5	12.5	nA	1
		$+V_{CC} = 2V$ , $-V_{CC} = -28V$ , $V_I = 0V$ , $V_{CM} = +13V$ , $R_S = 50K\Omega$		-12.5	12.5	nA	1
$I_{CEX}$	Output Leakage Current	$+V_{CC} = 18V$ , $-V_{CC} = -18V$ , $V_O = 32V$		-5.0	5.0	nA	1

## LM111 Typical Performance Characteristics



## LM111 Typical Performance Characteristics (continued)

Input Bias Current  
Input Overdrives

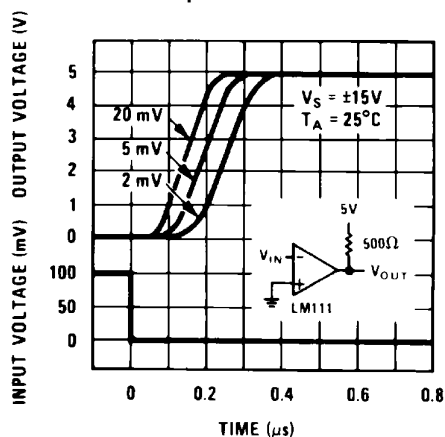


Figure 11.

Input Bias Current  
Input Overdrives

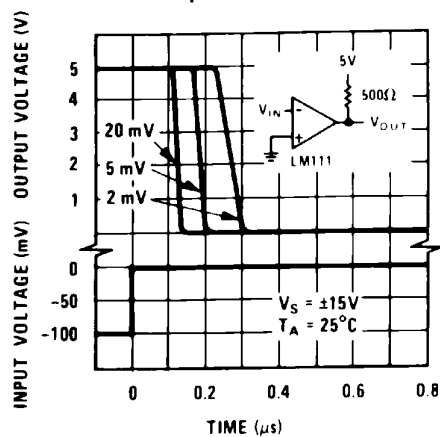


Figure 12.

Input Bias Current

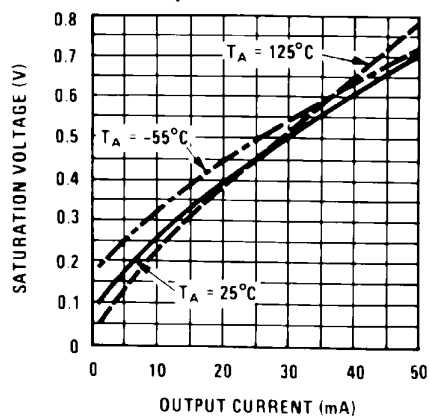


Figure 13.

Response Time for Various  
Input Overdrives

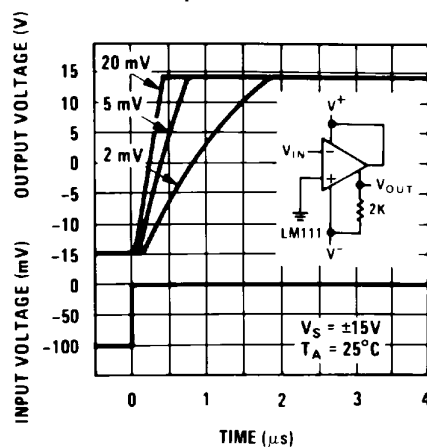


Figure 14.

Response Time for Various  
Input Overdrives

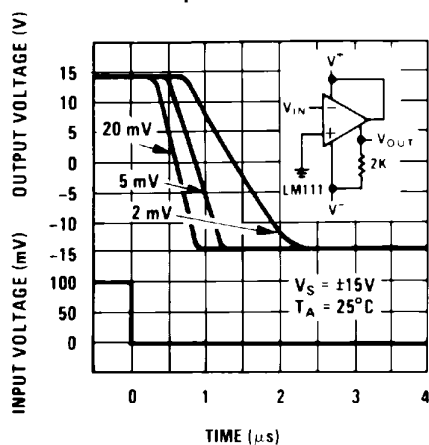


Figure 15.

Output Limiting Characteristics

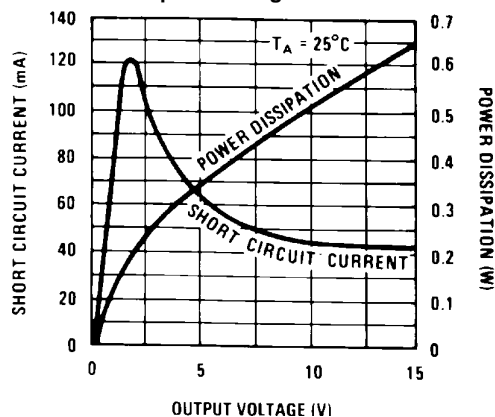


Figure 16.



## LM111 Typical Performance Characteristics (continued)

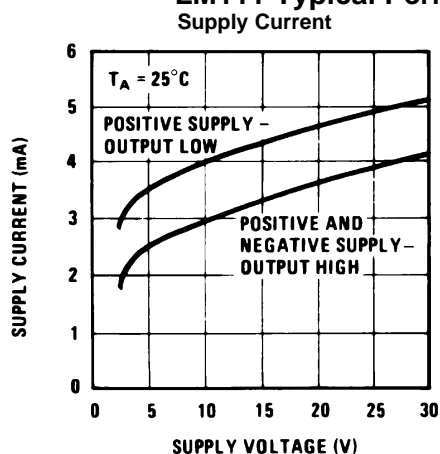


Figure 17.

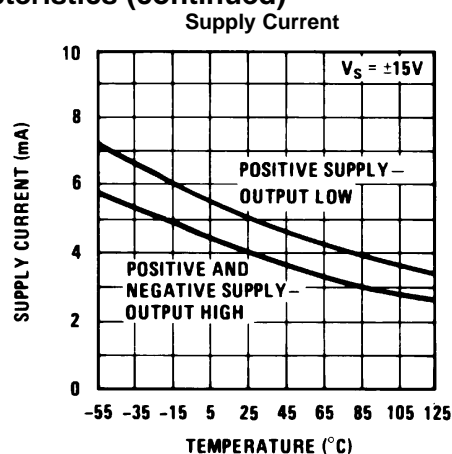


Figure 18.

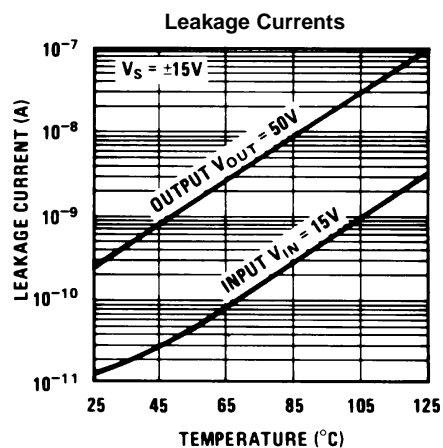


Figure 19.

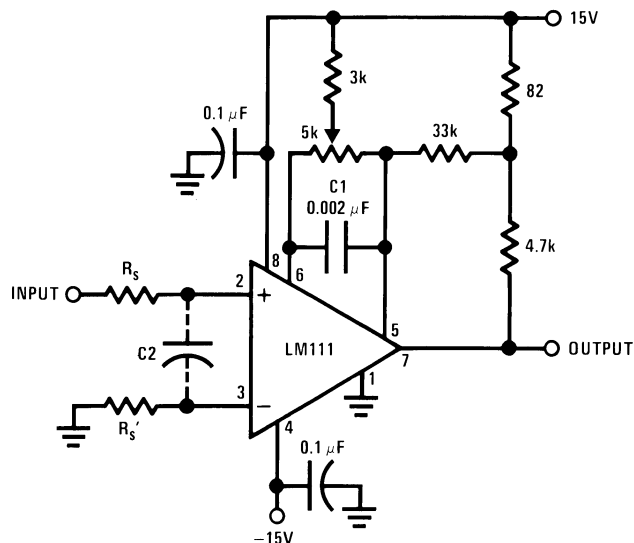
## APPLICATION HINTS

### CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1  $\mu\text{F}$  disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

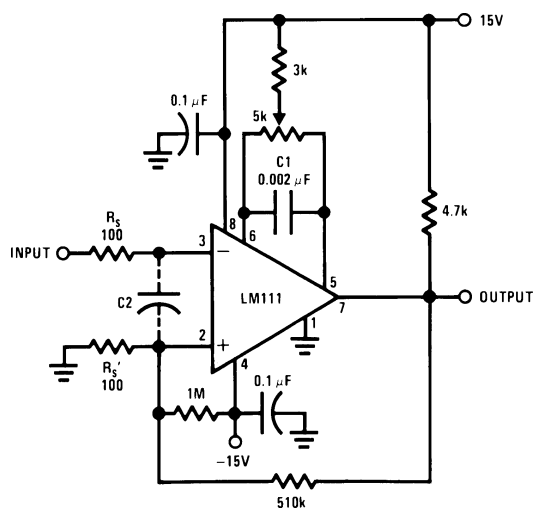
However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1  $\text{k}\Omega$  to 100  $\text{k}\Omega$ ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators such as the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in [Figure 20](#) below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01  $\mu\text{F}$  capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in [Figure 20](#).
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network,  $R_S$ , it is usually advantageous to choose an  $R_S$  of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if  $R_S=10\text{ k}\Omega$ , as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01  $\mu\text{F}$  capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of [Figure 21](#), the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if  $R_S$  is larger than 100  $\Omega$ , such as 50  $\text{k}\Omega$ , it would not be reasonable to simply increase the value of the positive feedback resistor above 510  $\text{k}\Omega$ . The circuit of [Figure 22](#) could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of [Figure 20](#) is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82  $\Omega$  resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the  $V_{OS}$  of the comparator. As much as 8 mV of  $V_{OS}$  can be trimmed out, using the 5  $\text{k}\Omega$  pot and 3  $\text{k}\Omega$  resistor as shown.
8. These application notes apply specifically to the LM111 and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



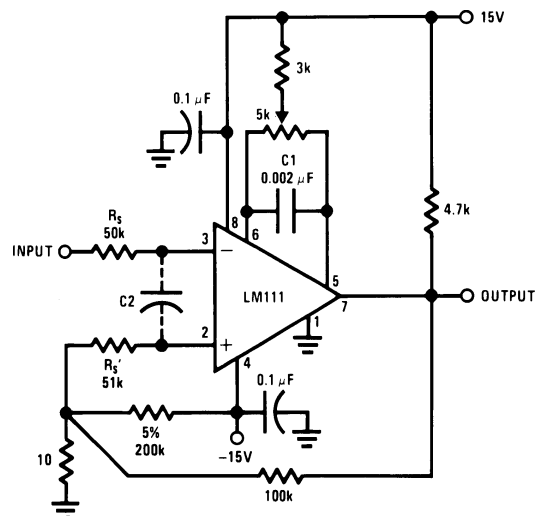
Pin connections shown are for LM111H in the LMC0008C hermetic package

**Figure 20. Improved Positive Feedback**



Pin connections shown are for LM111H in the LMC0008C hermetic package

**Figure 21. Conventional Positive Feedback**

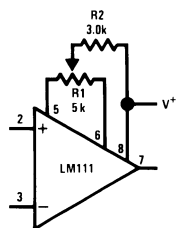


**Figure 22. Positive Feedback with High Source Resistance**

## Typical Applications

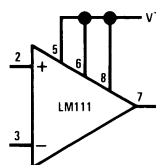
Pin connections shown on schematic diagram and typical applications are for LMC0008C metal can package.

**Offset Balancing**



**Figure 23.**

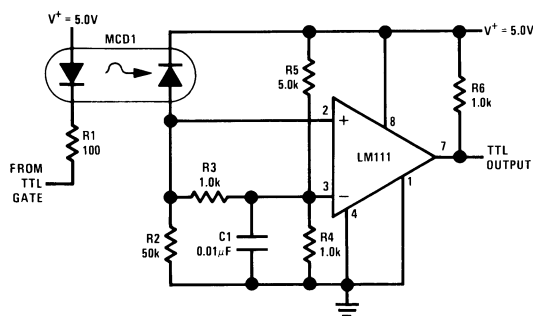
**Increasing Input Stage Current**



**Note:** Increases typical common mode slew from 7.0V/μs to 18V/μs.

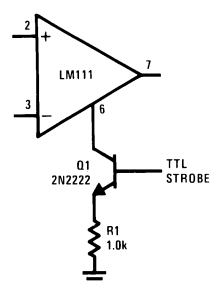
**Figure 25.**

**Digital Transmission Isolator**



**Figure 27.**

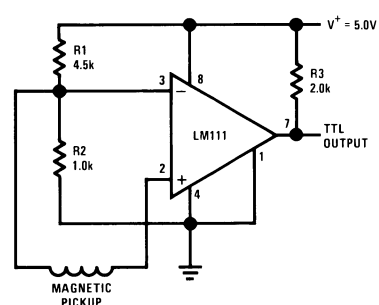
**Strobing**



**Note:** Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

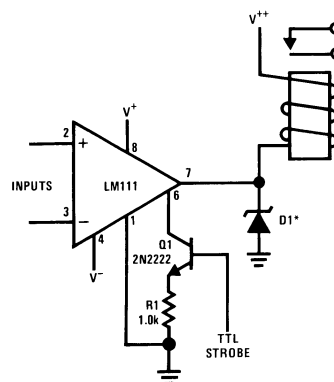
**Figure 24.**

**Detector for Magnetic Transducer**



**Figure 26.**

**Relay Driver with Strobe**

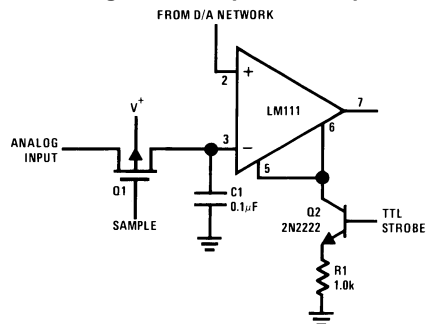


\*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

**Note:** Do Not Ground Strobe Pin.

**Figure 28.**

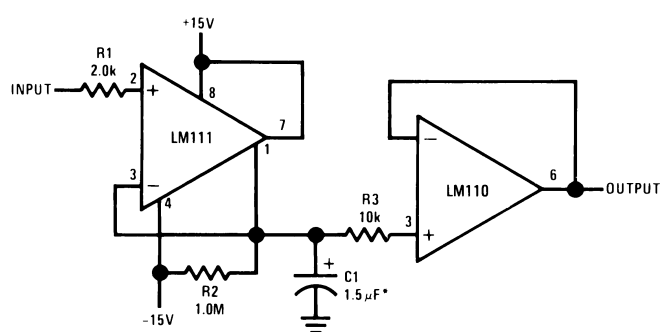
### Strobing off Both Input and Output Stages



Note: Typical input current is 50 pA with inputs strobed off.

Figure 29.

### Positive Peak Detector



\*Solid tantalum

Figure 30.

### Zero Crossing Detector Driving MOS Logic

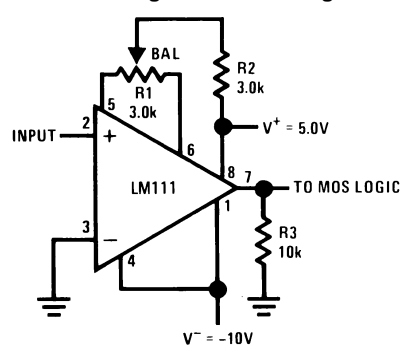


Figure 31.

## Typical Applications

(Pin numbers refer to LMC0008C package)

### Zero Crossing Detector Driving MOS Switch

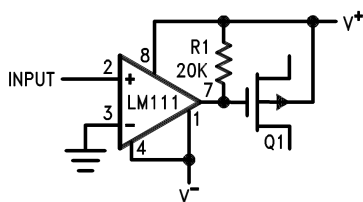
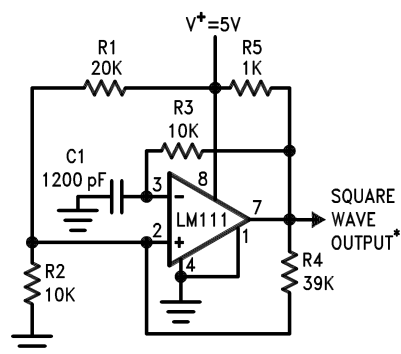


Figure 32.

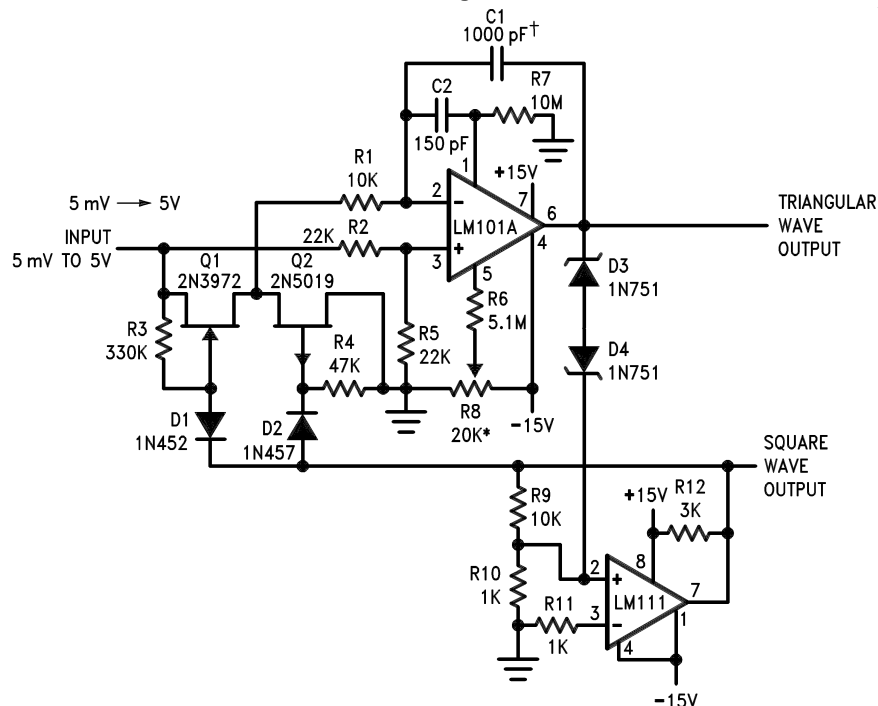
### 100 kHz Free Running Multivibrator



\*TTL or DTL fanout of two

Figure 33.

### 10 Hz to 10 kHz Voltage Controlled Oscillator

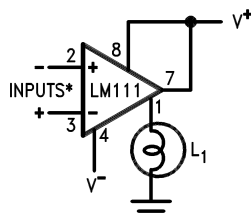


\*Adjust for symmetrical square wave time when  $V_{IN} = 5 \text{ mV}$

†Minimum capacitance 20 pF Maximum frequency 50 kHz

Figure 34.

### Driving Ground-Referred Load



\*Input polarity is reversed when using pin 1 as output.

Figure 35.

### Using Clamp Diodes to Improve Response

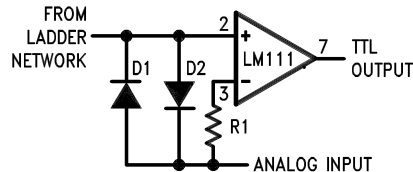
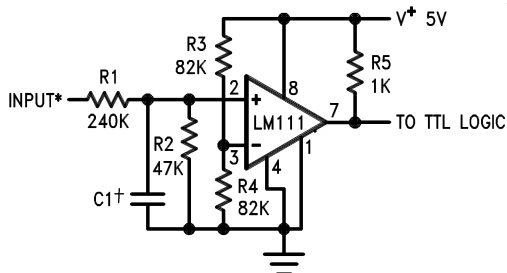


Figure 36.

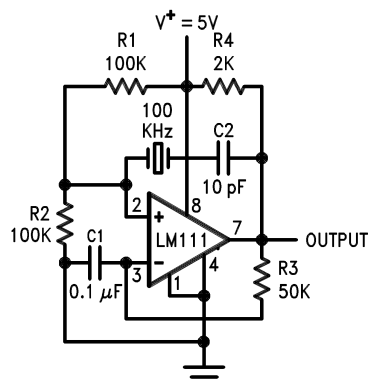
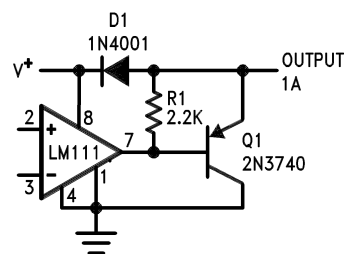
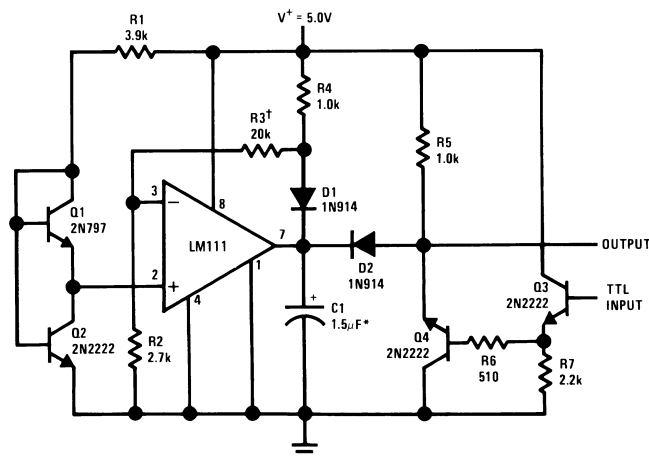
### TTL Interface with High Level Logic



\*Values shown are for a 0 to 30V logic swing and a 15V threshold.

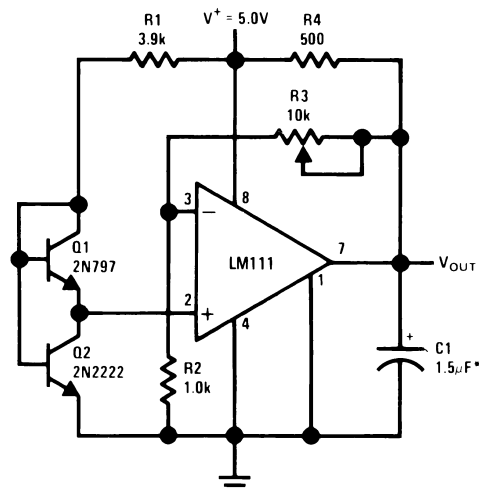
†May be added to control speed and reduce susceptibility to noise spikes.

Figure 37.

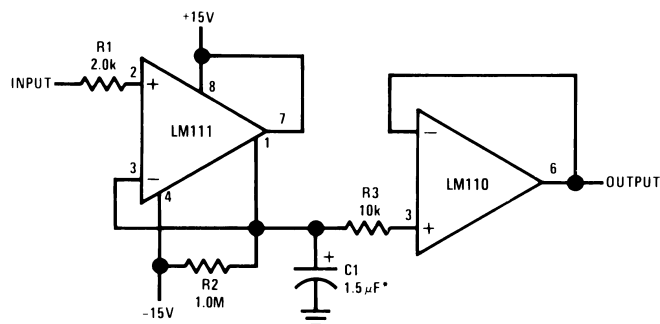
**Crystal Oscillator****Figure 38.****Comparator and Solenoid Driver****Figure 39.****Precision Squarer**

\*Solid tantalum

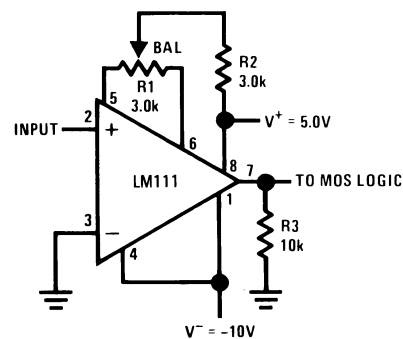
†Adjust to set clamp level

**Figure 40.****Low Voltage Adjustable Reference Supply**

\*Solid tantalum

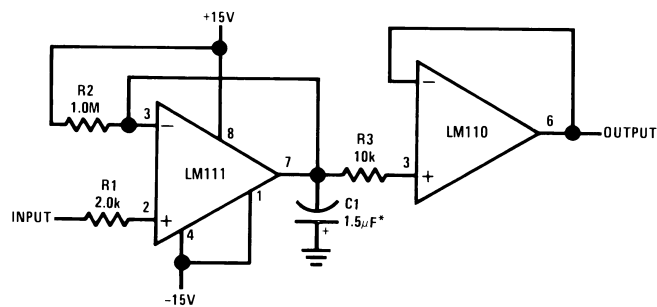
**Figure 41.****Positive Peak Detector**

\*Solid tantalum

**Figure 42.****Zero Crossing Detector Driving MOS Logic****Figure 43.**



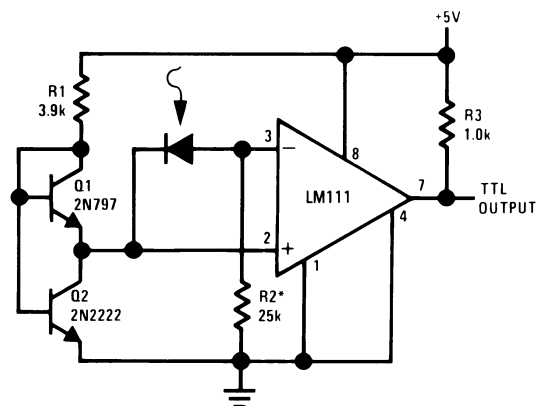
Negative Peak Detector



\*Solid tantalum

Figure 44.

Precision Photodiode Comparator



\*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Figure 45.

Switching Power Amplifier

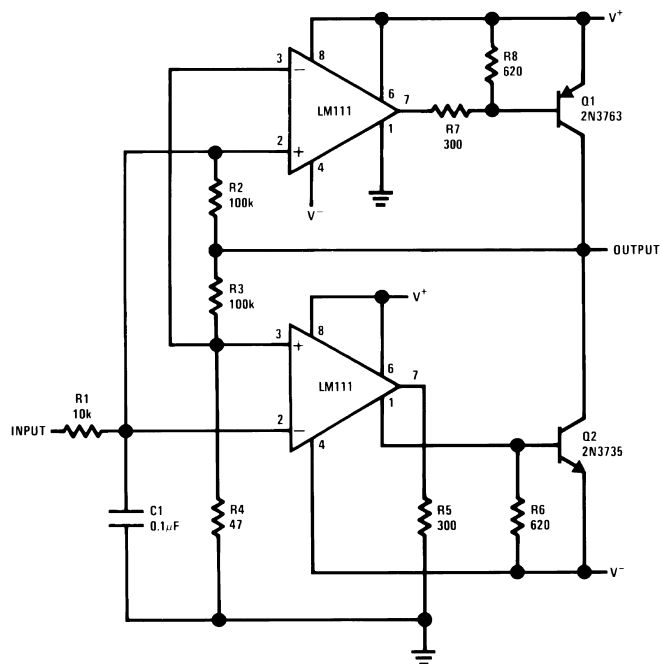


Figure 46.

Switching Power Amplifier

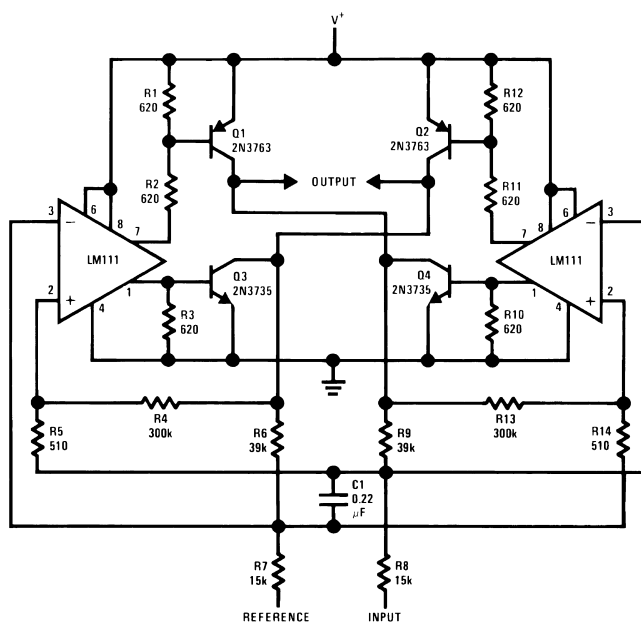


Figure 47.

**REVISION HISTORY SECTION**

Released	Revision	Section	Originator	Changes
05/09/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheets converted into one Corp. data sheet format. MJLM111–X Rev 0D3 will be archived.
03/26/2013	B	All Sections		Changed layout of National Data Sheet to TI format

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">JL111BGA</a>	Active	Production	TO-99 (LMC)   8	20   JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T
<a href="#">JM38510/10304BGA</a>	Active	Production	TO-99 (LMC)   8	20   JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T
<a href="#">M38510/10304BGA</a>	Active	Production	TO-99 (LMC)   8	20   JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

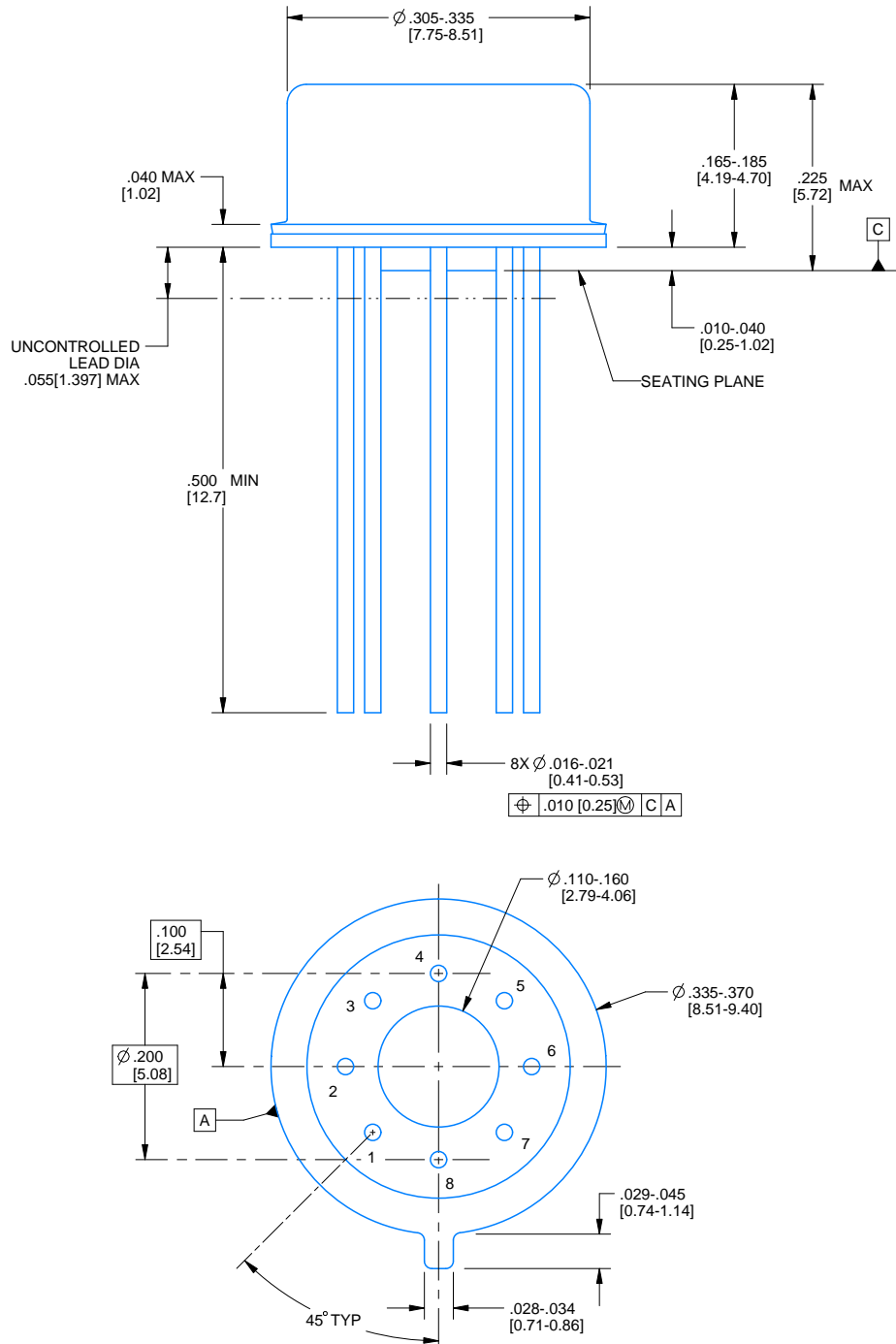
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
JL111BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
JM38510/10304BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
M38510/10304BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

# PACKAGE OUTLINE

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220610/B 09/2024

## NOTES:

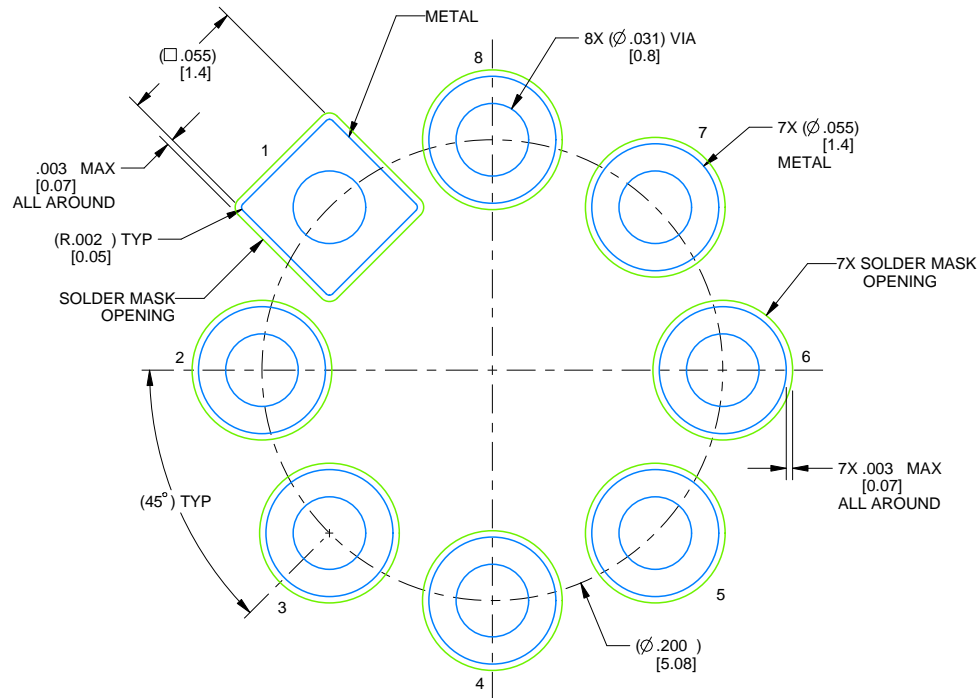
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.

# EXAMPLE BOARD LAYOUT

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 12X

4220610/B 09/2024

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025