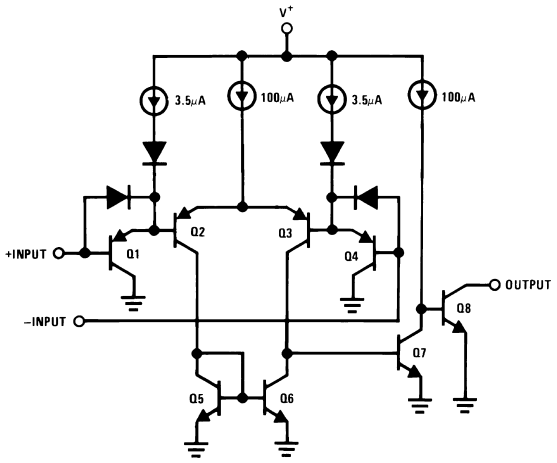
LM139AQML and LM139QML Low Power Low Offset Voltage Quad Comparators

1 Features

- Available As Radiation Tolerant
  - Total Ionizing Dose 100krad(Si)
  - ELDRS Free 100krad(Si)
- Wide Supply Voltage Range
- LM139/139A Series 2 to 36V_{DC} or ±1 to ±18V_{DC}
- Very Low Supply Current Drain (0.8mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25nA
- Low Input Offset Current: ±5nA
- Offset Voltage: ±1mV
- Input Common-mode Voltage Range Includes GND
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250mV at 4mA
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS Logic Systems
- Available in Space Enhanced Product (SEP) in plastic.

2 Advantages

- High Precision Comparators
- Reduced V_{OS} Drift Over Temperature
- Eliminates Need for Dual Supplies
- Allows Sensing Near GND
- Compatible with all Forms of Logic
- Power Drain is Excellent for Battery Operation



Schematic Diagram

3 Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2mV max for all four comparators. These are designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series is designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, can directly interface with MOS logic, where the low power drain of the LM139/LM139A is a distinct advantage over standard comparators.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM139-883, LM139A-883, 5962–8773801, 5962–8773901	CDIP 14 (J)	6.67mm × 19.56mm
	LCCC 20 (NAJ)	8.89mm × 8.89mm
	CFP 14 (NAC) CFP 14 (NAD)	6.35mm × 9.91mm
	SINGLE DIE (0)	1067µm x 1041µm
LM139A-SEP	SOT-23-14 (DYY)	4.20mm × 2.00mm
LM139AQMLV(-SP), 5962R9673801, 5962R9673802	CFP 14 (NAC) CFP 14 (NAD)	6.35mm × 9.91mm
	CDIP 14 (J)	6.67mm × 19.56mm
	SINGLE DIE (0)	1067µm x 1041µm
LM139AQML-SP, 5962R2620501	SOT-23-14 (DYY)	4.20mm × 2.00mm

(1) For all available packages, see Section 9.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

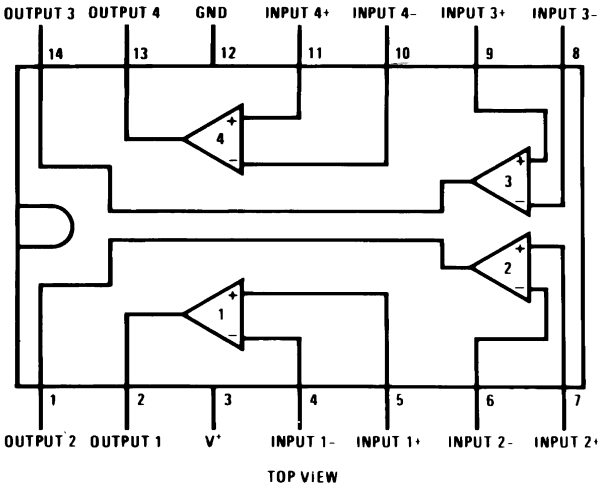


Figure 4-1.
J, DYY Packages
14-Pin CDIP, SOT-23-14
Top View

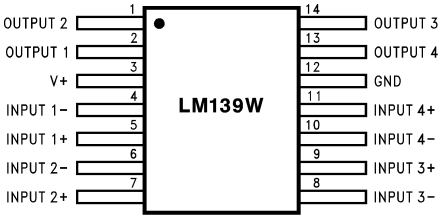


Figure 4-2.
NAC, NAD Packages
14-Pin CFP (trimmed), CFP (full)
Top View

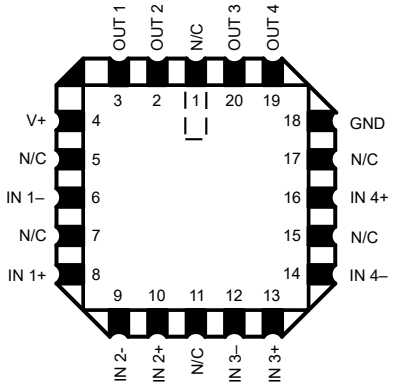


Figure 4-3.
NAJ Package
20-Pad LCCC
Top View

For the **LM139MD8/MDE/MDR** bare die, please see the LM139MDE/MDR die data sheet for pad locations.

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Table 4-1. Pin Functions

PINS			I/O	DESCRIPTION
NAME	NAC, NAD, DYY, J	LCCC		
OUTPUT 2	1	2	Output	Output pin of comparator 2
OUTPUT 1	2	3	Output	Output pin of comparator 1
V+	3	4	—	Positive supply
INPUT 1–	4	6	Input	Negative input pin of comparator 1
INPUT 1+	5	8	Input	Positive input pin of comparator 1
INPUT 2–	6	9	Input	Negative input pin of comparator 2
INPUT 2+	7	10	Input	Positive input pin of comparator 2
INPUT 3–	8	12	Input	Negative input pin of comparator 3
INPUT 3+	9	13	Input	Positive input pin of comparator 3
INPUT 4–	10	14	Input	Negative input pin of comparator 4
INPUT 4+	11	16	Input	Positive input pin of comparator 4
GND	12	18	—	Negative supply
OUTPUT 4	13	19	Output	Output pin of comparator 4
OUTPUT 3	14	20	Output	Output pin of comparator 3
N/C	—	1,5,7,11,15,17	—	No Internal Connection - Leave floating or GND

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5 Specifications

5.1 Absolute Maximum Ratings

			LM139 / LM139A
Supply Voltage, V^+			$36V_{DC}$ or $\pm18V_{DC}$
Differential Input Voltage(1)			$36V_{DC}$
Input Voltage			$-0.3V_{DC}$ to $+36V_{DC}$
Input Current ($V_{IN} < -0.3V_{DC}$)(2)			50mA
Power Dissipation(3)(4)			
LCCC			1250mW
CDIP			1200mW
CLGA (NAD)			680mW
CLGA (NAC)			680mW
SOT-23-14 (DYY)			
Sink Current (approx)(5)			20mA
Output Short-Circuit to GND(6)			Continuous
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Maximum Junction Temperature (T_J)			+150°C
Lead Temperature (Soldering, 10 seconds)			300°C
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Thermal Resistance	θ_{JA}	LCCC (Still Air)	100°C/W
		LCCC (500LF / Min Air flow)	73°C/W
		CDIP (Still Air)	103°C/W
		CDIP (500LF / Min Air flow)	65°C/W
		CLGA (NAD) (Still Air)	183°C/W
		CLGA (NAD) (500LF / Min Air flow)	120°C/W
		CLGA (NAC) (Still Air)	183°C/W
		CLGA (NAC) (500LF / Min Air flow)	120°C/W
		SOT-23-14 (DYY / Still Air)	127°C/W
	θ_{JC}	LCCC	28°C/W
		CDIP	23°C/W
		CLGA (NAD)	23°C/W
		CLGA (NAC)	23°C/W
		SOT-23-14 (DYY)	67°C/W
Package Weight (typical)	LCCC		470mg
	CDIP		2,190mg
	CLGA (NAD)		460mg
	CLGA (NAC)		410mg
	SOT-23-14 (DYY)		36mg
ESD rating(7)			600V

(1) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$below the magnitude of the negative power supply, if used) (at 25°C).

(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$ (at 25°C).

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(3) The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) SMD 5962–8773901 only
(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V^+.
(7) Human Body model, 1.5KΩ in series with 100pF

5.2 Recommended Operating Conditions

Parameter	Value
Supply Voltage	$5.0V_{DC}$ to $+30V_{DC}$
Ambient Operating Temperature Range	$-55°C \leq T_A \leq +125°C$

5.3 Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

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5.4 LM139: 883 Electrical Characteristics, DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
	Supply Current	+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
V_{IO}	Input Offset Voltage	+V = 30V		-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-5.0	5.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-9.0	9.0	mV	2, 3
				-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-100	-1.0	nA	1
			See(1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
A_V	Voltage Gain	+V = 15V, R_L ≥ 15ΩK, V_I = 1V to 11V		50		V/mV	1
V_{CM}	Common Mode Voltage Range	+V = 30V	See(2)	0	V^+ - (1.5)	V	1
			See(2)	0	V^+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V = 0V, $+V_I$ = 36V, $-V_I$ = 0V	See(3)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	See(3)		500	nA	1, 2, 3

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(2) Parameter ensured by V_{IO} tests
(3) The value for V_{Diff} is not data logged during Read and Record.

5.5 LM139: 883 Electrical Characteristics, AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

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5.6 LM139A: SMD 5962–8773901 Electrical Characteristics, DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	+V = 30V, R_L = Infinity			3.0	mA	1, 2, 3
		R_L = Infinity			3.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, -V_I = 0V, +V_I ≥ 1V, V_O = 30V			0.5	µA	1
					1.0	µA	2, 3
V_{Sat}	Saturation Voltage	I_{Sink} ≤ 4mA, -V_I = 1V, +V_I = 0V			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	V_O ≥ 1.5V, -V_I = 1V, +V_I = 0V		6.0		mA	1
V_{IO}	Input Offset Voltage	R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28V, V_O = 1.4V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
±I_{IB}	Input Bias Current	V_O = 1.5V	See(1)	-100	-1.0	nA	1
			See(1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28V, R_L ≥ 15KΩ		70		dB	1, 2, 3
A_V	Voltage Gain	+V = 15V, R_L ≥ 15KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6
V_{CM}	Common Mode Voltage Range	+V = 30V	See(2)	0	V^+ - (2.0)	V	1, 2, 3
		+V = 5V	See(2)	0	V^+ - (2.0)	V	1, 2, 3

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(2) Parameter ensured by V_{IO} tests

5.7 LM139A: SMD 5962–8773901 Electrical Characteristics, AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			5.0	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			2.5	µS	9

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5.8 LM139A: 883, QMLV and RH, SEP, 5962x9673801, 5962R2620501 Electrical Characteristics, DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
		+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V, V_O = 1.5V		-4.0	4.0	mV	2, 3
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-100	-1.0	nA	1
			See(1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
A_V	Voltage Gain	+V = 15V, R_L ≥ 15KΩ, V_O = 1V to 11V		50		V/mV	1
V_{CM}	Common Mode Voltage Range	+V = 30V	See(3) See(2)	0	V^+ - (1.5)	V	1
			See(3) See(2)	0	V^+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V =0V, $+V_I$ = 36V, $-V_I$ = 0V	(4)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	(4)		500	nA	1, 2, 3

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(2) Parameter ensured by V_{IO} tests
(3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V for Subgroup 1, or V^+ −2.0V for Subgroup 2 & 3. Either or both inputs can go to $+30V_{DC}$ without damage, independent of the magnitude of V^+.
(4) The value for V_{Diff} is not data logged during Read and Record.

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5.9 LM139A: 883, QMLV and RH, SEP, 5962x9673801, 5962R2620501 Electrical Characteristics, AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	4
		V_{OD} = 50mV			0.8	µS	4
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	4
		V_{OD} = 50mV			0.8	µS	4

5.10 LM139A: 883, QMLV and RH, SEP, 5962x9673801, 5962R2620501 Electrical Characteristics, DC Parameters Delta Values

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V
Deltas required for S-Level, MLS (as specified on Internal Processing instructions (IPI)), and QMLV product at Group B, Subgroup 5.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-15	15	nA	1
I_{IO}	Input Offset Current	V_O = 1.5V		-10	+10	nA	1

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

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5.11 LM139A: 883, QMLV and RH, 5962R9673801, 5962R2620501 Electrical Characteristics, DC/AC Parameters 50K Post Rad Limits +25°C

The following conditions apply, unless otherwise specified.
DC: +V = 5V, V_{CM} = 0V
AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0V		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 0V		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.5	2.5	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			0.9	µS	4

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

5.12 LM139A: 883, QMLV and RH, 5962R9673801, 5962R2620501 Electrical Characteristics, DC/AC Parameters 100K Post Rad Limits +25°C

The following conditions apply, unless otherwise specified.
DC: +V = 5V, V_{CM} = 0V
AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0V		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 0V		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-4.0	4.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			1.0	µS	4

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

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5.13 Typical Performance Characteristics

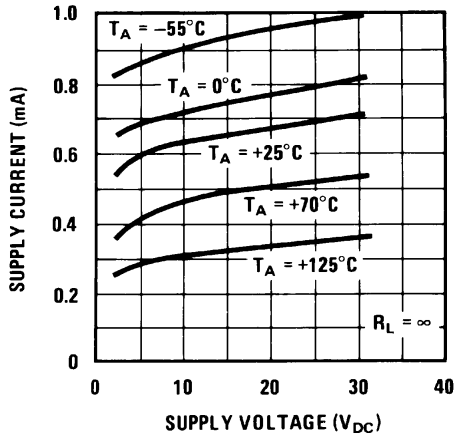


Figure 5-1. Supply Current

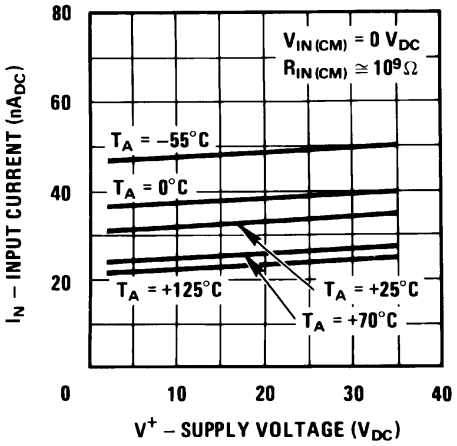


Figure 5-2. Input Current

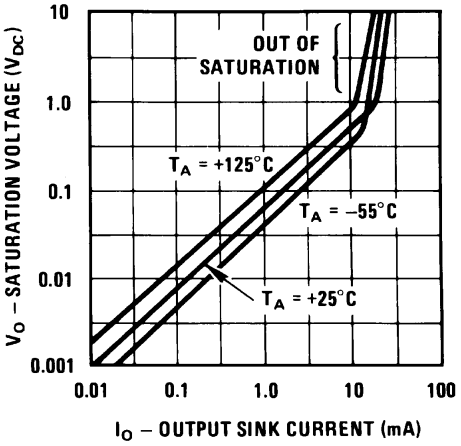


Figure 5-3. Output Saturation Voltage

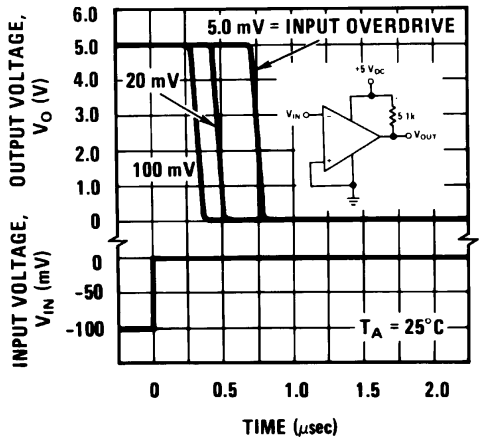


Figure 5-4. Response Time for Various Input Overdrives —Negative Transition

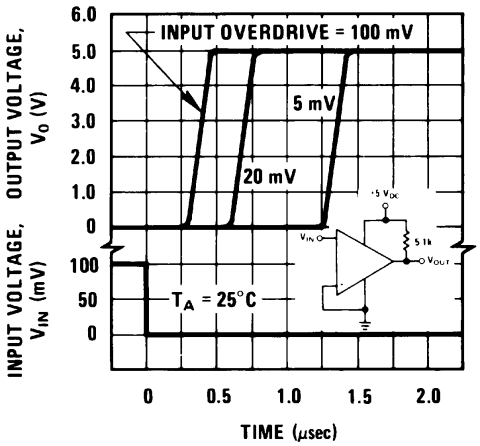


Figure 5-5. Response Time for Various Input Overdrives —Positive Transition

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30V_{DC}$.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the Section 6.2 section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1mV) allows the output to clamp essentially to ground level for small load currents.

6.2 Typical Applications

($V^+ = 5.0V_{DC}$)

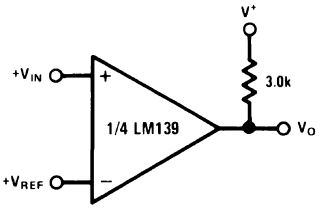


Figure 6-1. Basic Comparator

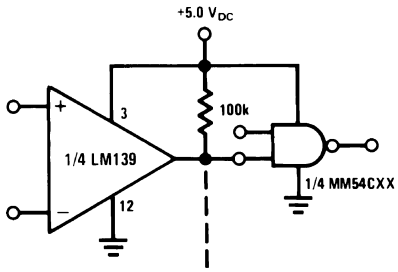


Figure 6-2. Driving CMOS

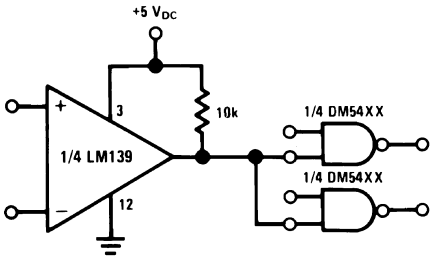


Figure 6-3. Driving TTL

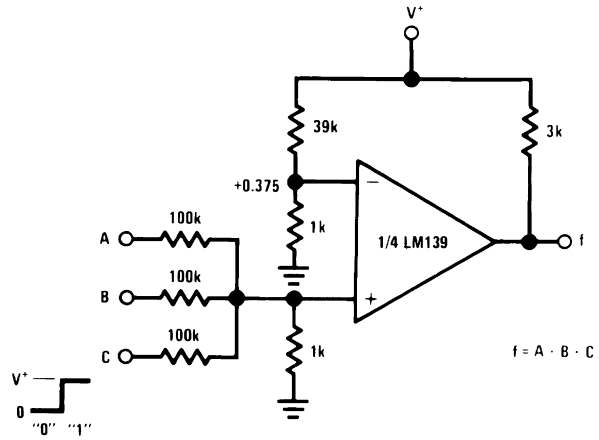


Figure 6-4. AND Gate

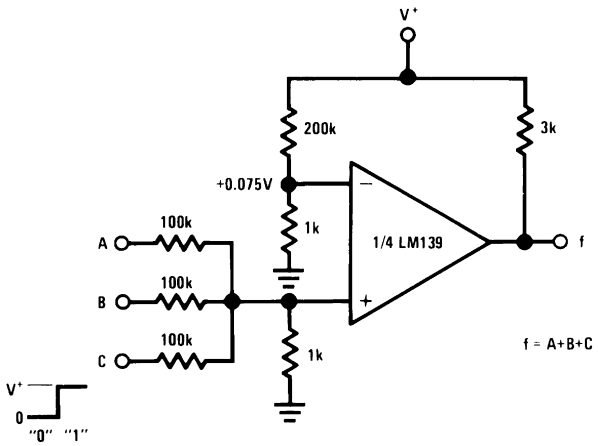


Figure 6-5. OR Gate

6.3 Typical Applications

(V^+= 15V_{DC})

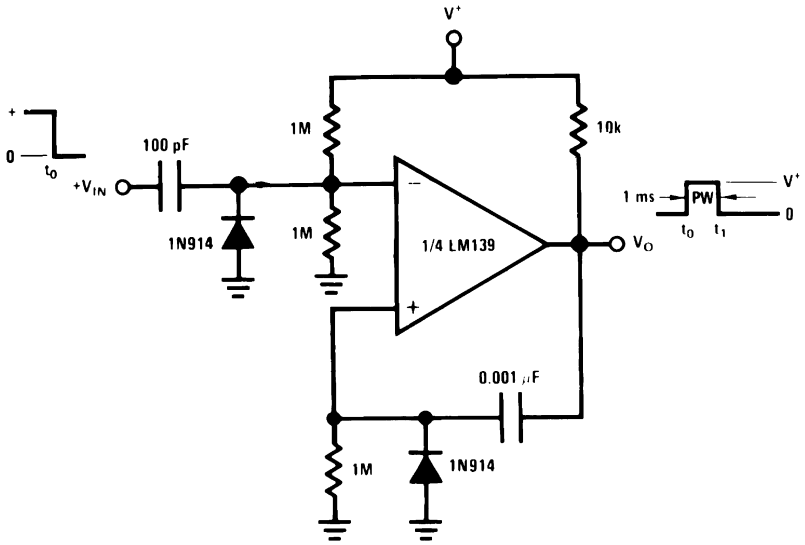


Figure 6-6. One-Shot Multivibrator

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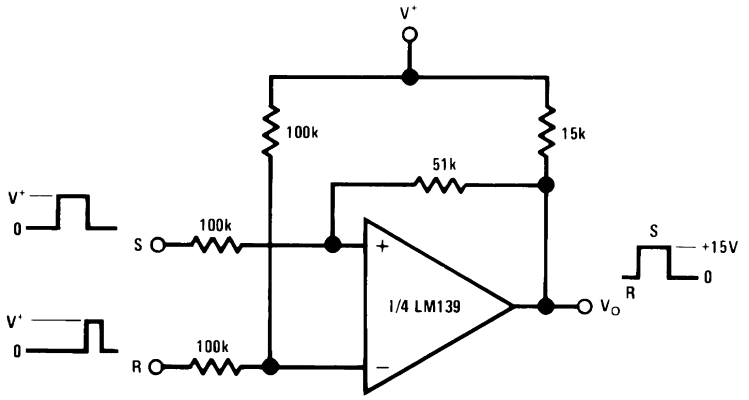


Figure 6-7. Bi-Stable Multivibrator

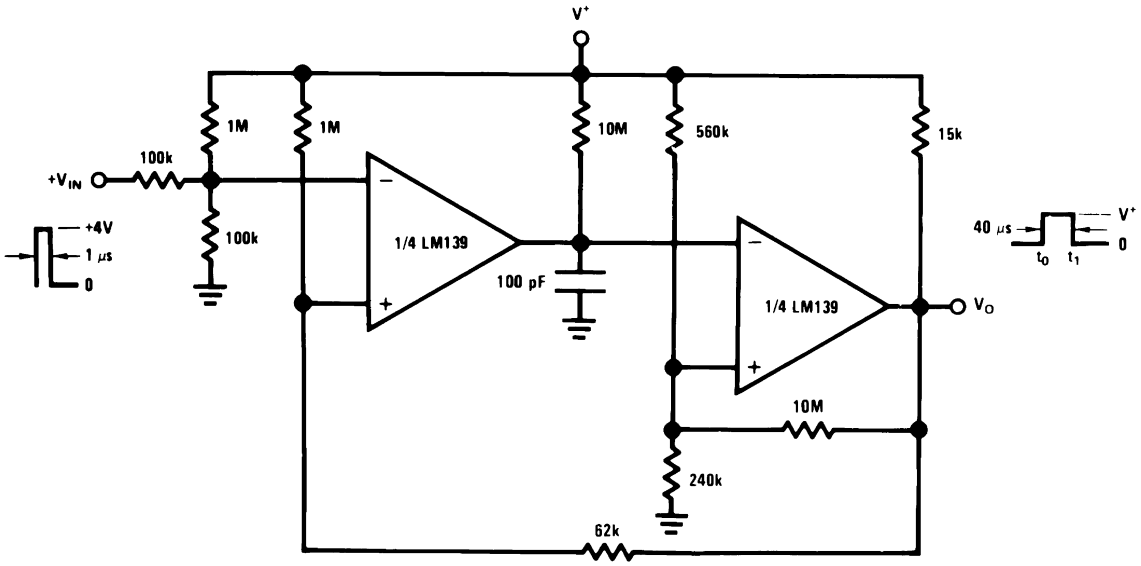


Figure 6-8. One-Shot Multivibrator With Input Lock Out

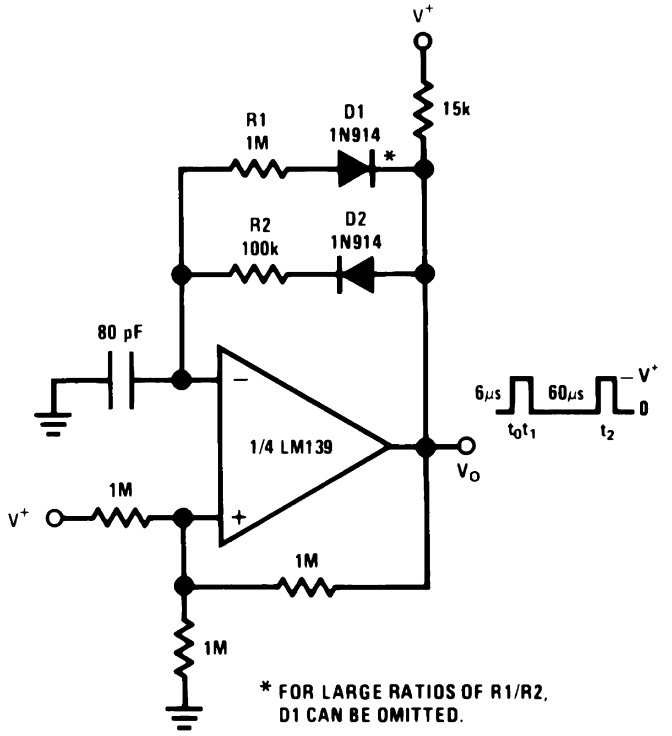


Figure 6-9. Pulse Generator

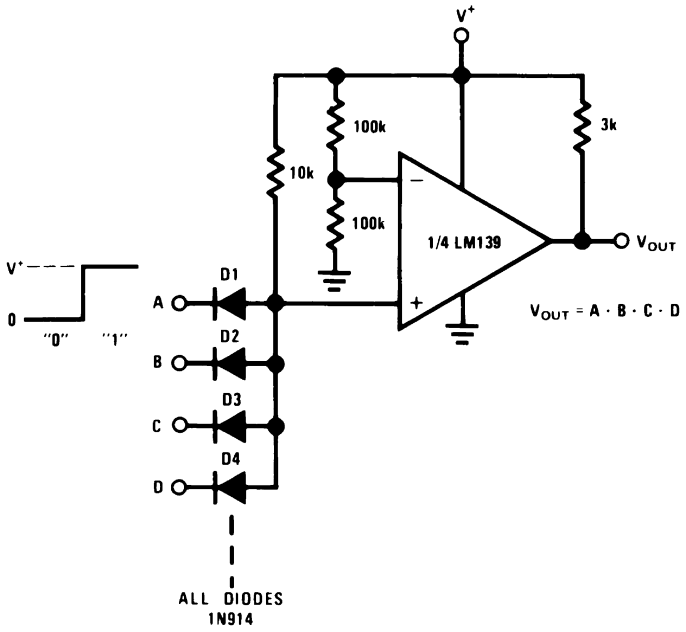


Figure 6-10. Large Fan-In AND Gate

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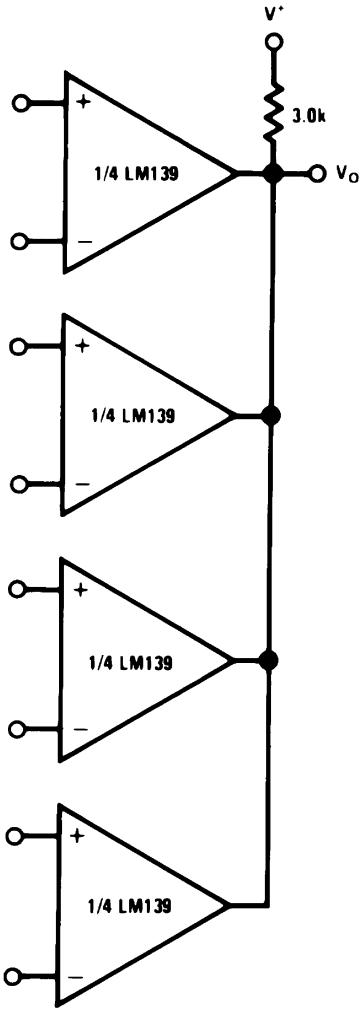


Figure 6-11. ORing the Outputs

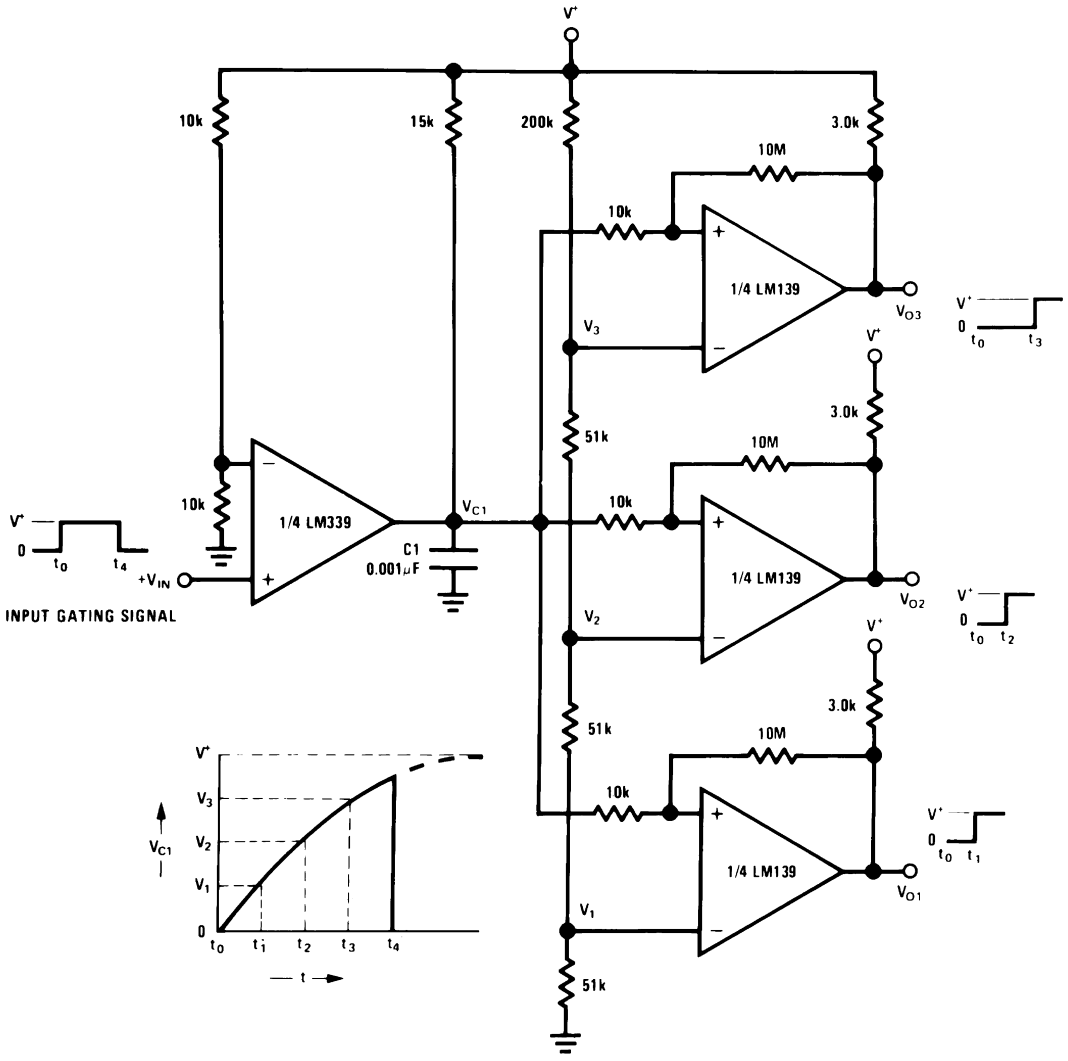


Figure 6-12. Time Delay Generator

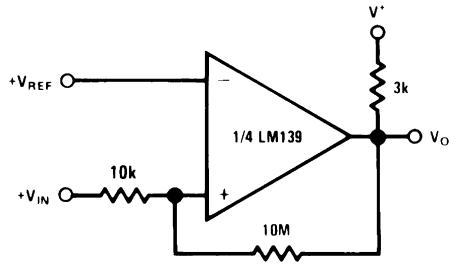


Figure 6-13. Non-Inverting Comparator With Hysteresis

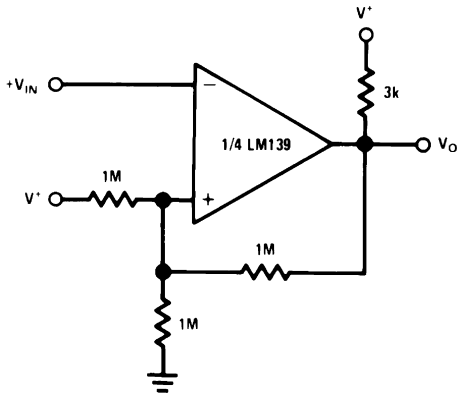


Figure 6-14. Inverting Comparator With Hysteresis

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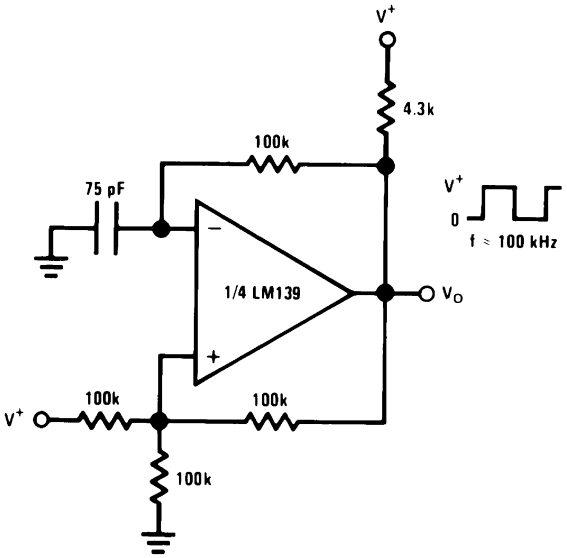


Figure 6-15. Squarewave Oscillator

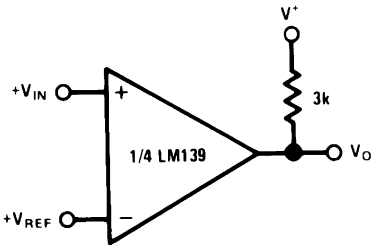


Figure 6-16. Basic Comparator

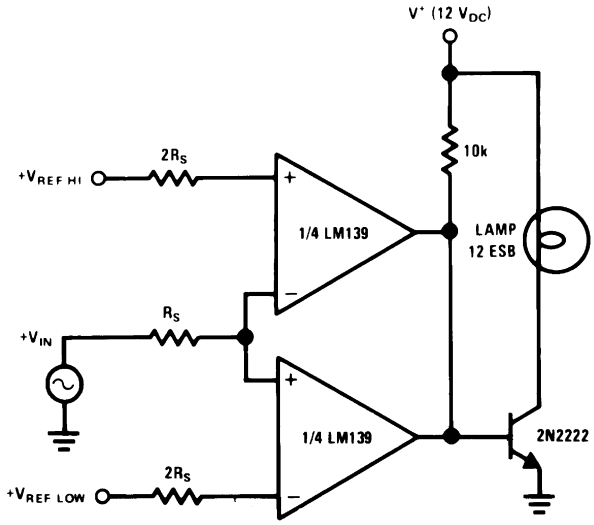


Figure 6-17. Limit Comparator

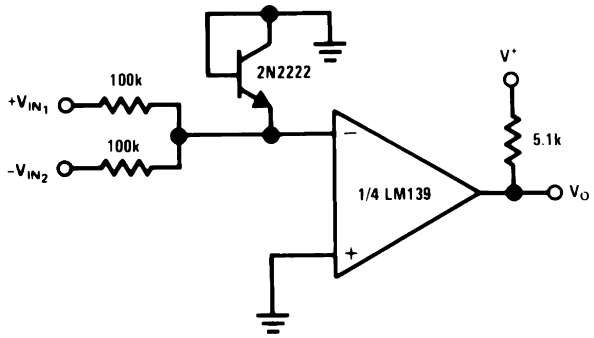
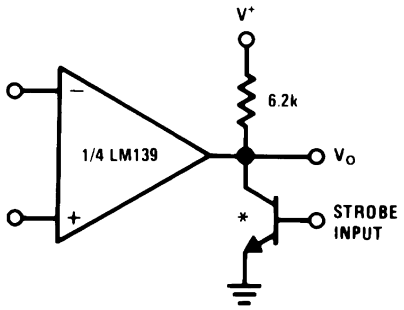


Figure 6-18. Comparing Input Voltages of Opposite Polarity



* Or open-collector logic gate without pull-up resistor

Figure 6-19. Output Strobing

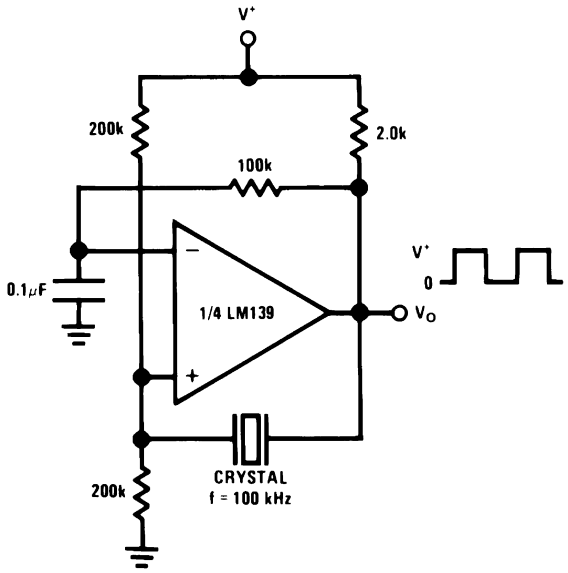
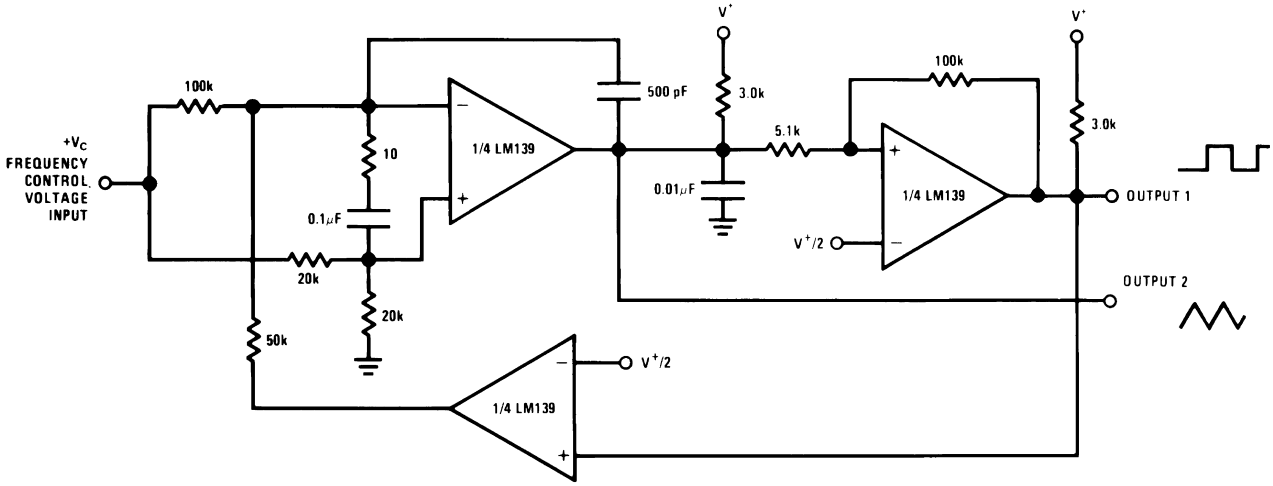


Figure 6-20. Crystal Controlled Oscillator



$V^+ = +30V_{DC}$ $250mV_{DC} \leq V_C \leq +50V_{DC}$ $700Hz \leq f_O \leq 100kHz$

Figure 6-21. Two-Decade High-Frequency VCO

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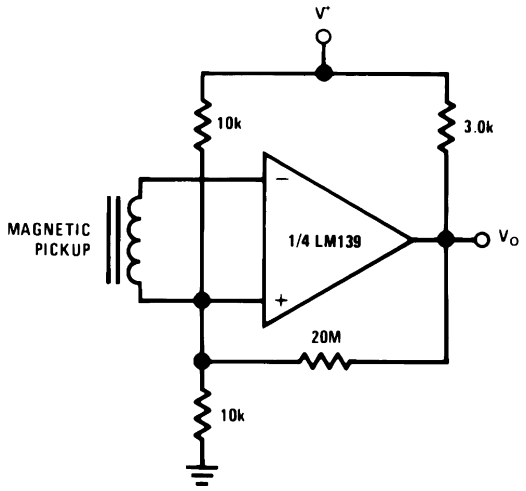


Figure 6-22. Transducer Amplifier

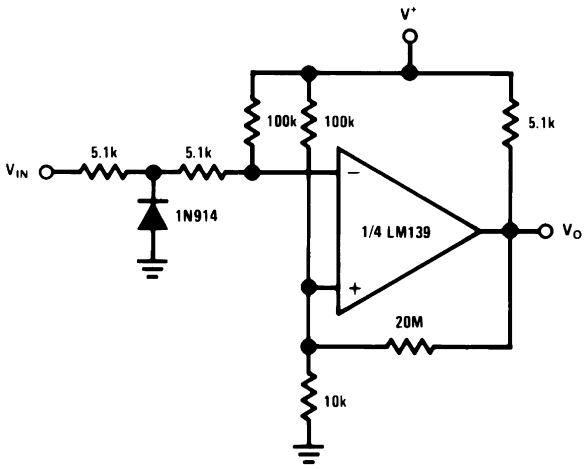


Figure 6-23. Zero Crossing Detector (Single Power Supply)

6.4 Split-Supply Applications

(V^+ = +15V_{DC} and V^- = −15V_{DC})

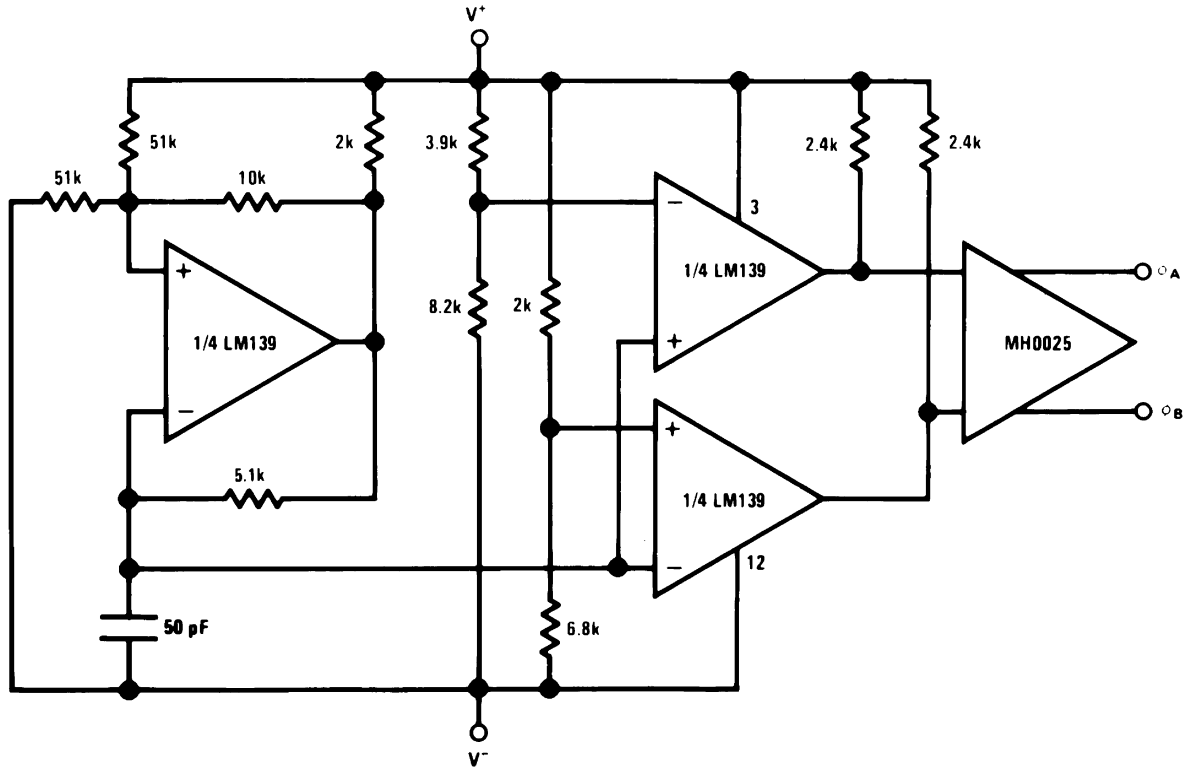


Figure 6-24. MOS Clock Driver

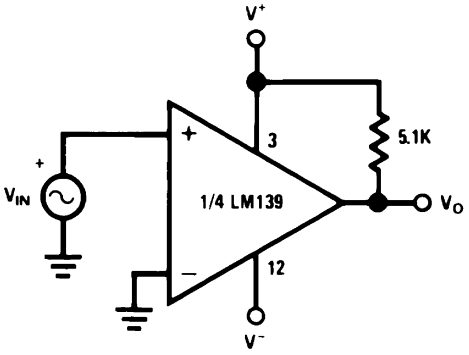


Figure 6-25. Zero Crossing Detector

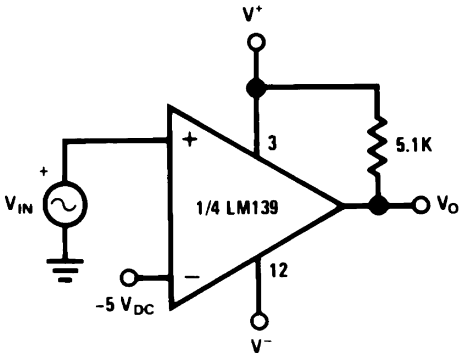


Figure 6-26. Comparator With a Negative Reference

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H (October 2026)	Page
• Added LM139A-SEP in DYY package	1
• Added DYY package, updated page format	3

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8773901XA	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWG -SMD Q 5962-87739 01XA ACO 01XA >T
5962-9673801VDA	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AW- QMLV Q 5962-96738 01VDA ACO 01VDA >T
5962-9673801VXA	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWG- QMLV Q 5962-96738 01VXA ACO 01VXA >T
5962R9673801V9A	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9673801VCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AJRQMLV 5962R9673801VCA Q
5962R9673801VDA	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWR QMLV Q 5962R96738 (01VDA ACO, 02VDA ACO) (01VDA >T, 02VDA > T)
5962R9673801VXA	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWGR QMLV Q 5962R96738 01VXA ACO 01VXA >T
5962R9673802V9A	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9673802VCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AJRLQMLV 5962R9673802VCA Q

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5962R9673802VDA	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWRL QMLV Q 5962R96738 02VDA ACO 02VDA >T
5962R9673802VXA	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWGRL QMLV Q 5962R96738 02VXA ACO 02VXA >T
LM139 MD8	Active	Production	DIESALE (Y) | 0	400 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM139 MDE	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM139 MDR	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM139AE/883	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM139AE /883 Q ACO 5962-90765 /883 Q >T
LM139AJ/883	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AJ/883 Q
LM139AJRLQMLV	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AJRLQMLV 5962R9673802VCA Q
LM139AJRQMLV	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AJRQMLV 5962R9673801VCA Q
LM139AW-QMLV	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AW- QMLV Q 5962-96738 01VDA ACO 01VDA >T
LM139AW-SMD	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AW -SMD Q 5962-87739 01DA ACO 01DA >T
LM139AW/883	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AW /883 Q ACO /883 Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM139AWG-QMLV	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWG-QMLV Q 5962-96738 01VXA ACO 01VXA >T
LM139AWG-SMD	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWG -SMD Q 5962-87739 01XA ACO 01XA >T
LM139AWG/883	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWG /883 Q ACO 5962-87739 /883 Q >T
LM139AWGRLQMLV	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWGRL QMLV Q 5962R96738 02VXA ACO 02VXA >T
LM139AWGRQMLV	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWGR QMLV Q 5962R96738 01VXA ACO 01VXA >T
LM139AWRLQMLV	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWRL QMLV Q 5962R96738 02VDA ACO 02VDA >T
LM139AWRQMLV	Active	Production	CFP (NAD) | 14	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139AWR QMLV Q 5962R96738 (01VDA ACO, 02VDA ACO) (01VDA >T, 02VDA >T)
LM139E/883	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM139E /883 Q ACO /883 Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM139J/883	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM139J/883 Q
PLM139MDYYTSEP	Active	Preproduction	null (null) |	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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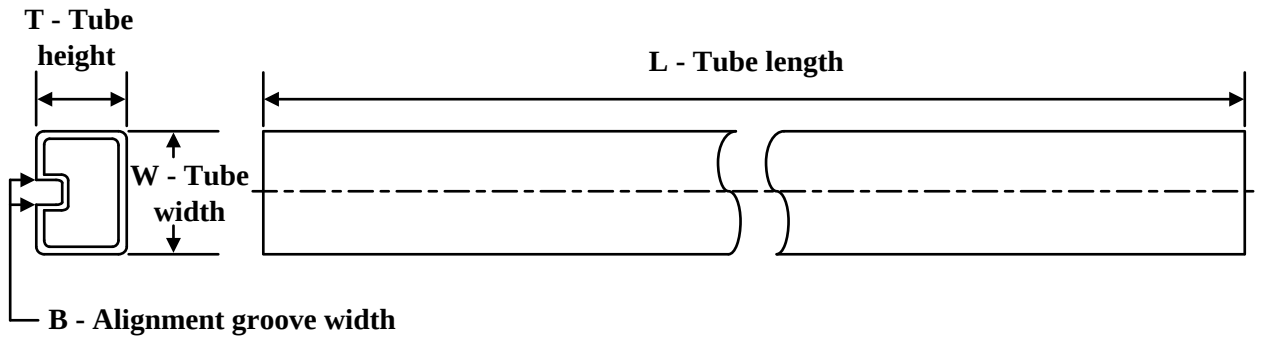
OTHER QUALIFIED VERSIONS OF LM139AQML, LM139AQML-SP :

- Military : LM139AQML
- Space : LM139AQML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

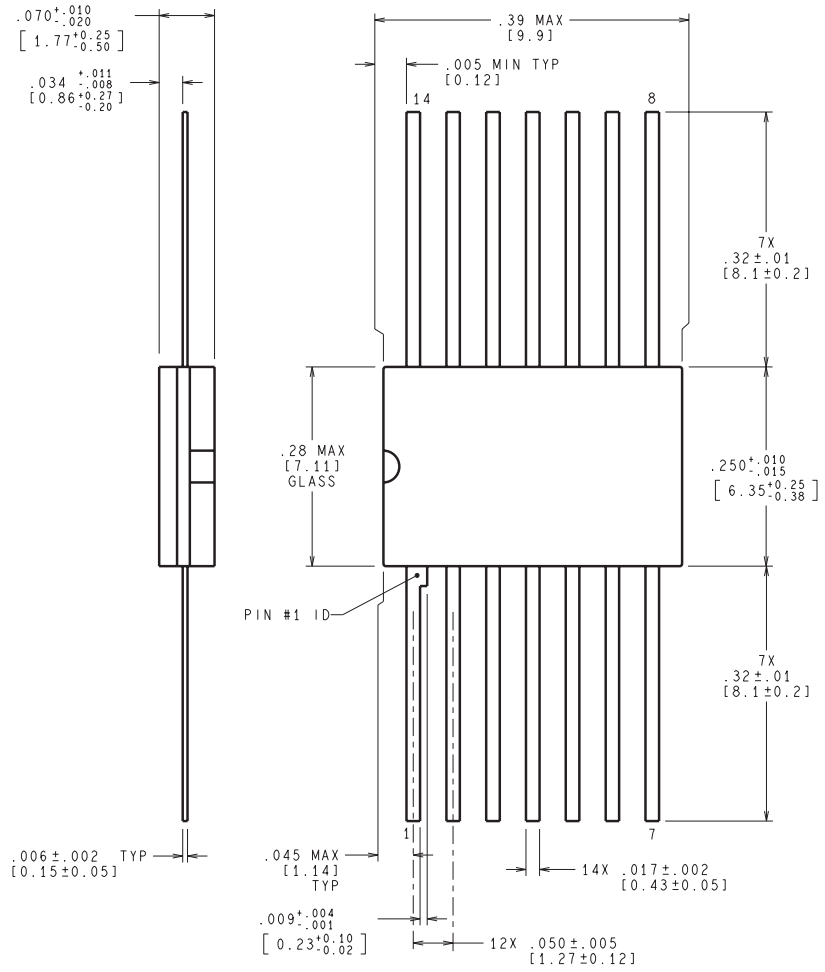
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9673801VDA	NAD	CFP	14	19	502	23	9398	9.78
5962R9673801VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R9673801VDA	NAD	CFP	14	19	502	23	9398	9.78
5962R9673802VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R9673802VDA	NAD	CFP	14	19	502	23	9398	9.78
LM139AE/883	NAJ	LCCC	20	50	470	11	3810	0
LM139AJ/883	J	CDIP	14	25	506.98	15.24	13440	NA
LM139AJRLQMLV	J	CDIP	14	25	506.98	15.24	13440	NA
LM139AJRQMLV	J	CDIP	14	25	506.98	15.24	13440	NA
LM139AW-QMLV	NAD	CFP	14	19	502	23	9398	9.78
LM139AW-SMD	NAD	CFP	14	19	502	23	9398	9.78
LM139AW/883	NAD	CFP	14	19	502	23	9398	9.78
LM139AWRLQMLV	NAD	CFP	14	19	502	23	9398	9.78
LM139AWRQMLV	NAD	CFP	14	19	502	23	9398	9.78
LM139E/883	NAJ	LCCC	20	50	470	11	3810	0
LM139J/883	J	CDIP	14	25	506.98	15.24	13440	NA

NAD0014B



W14B (Rev P)

MIL-PRF-38535 CONFIGURATION CONTROL

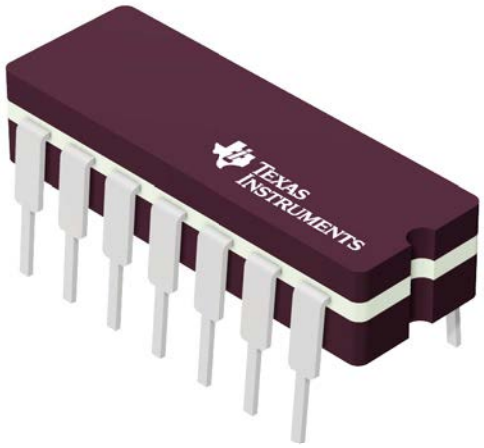
MIL-STD-1835B CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

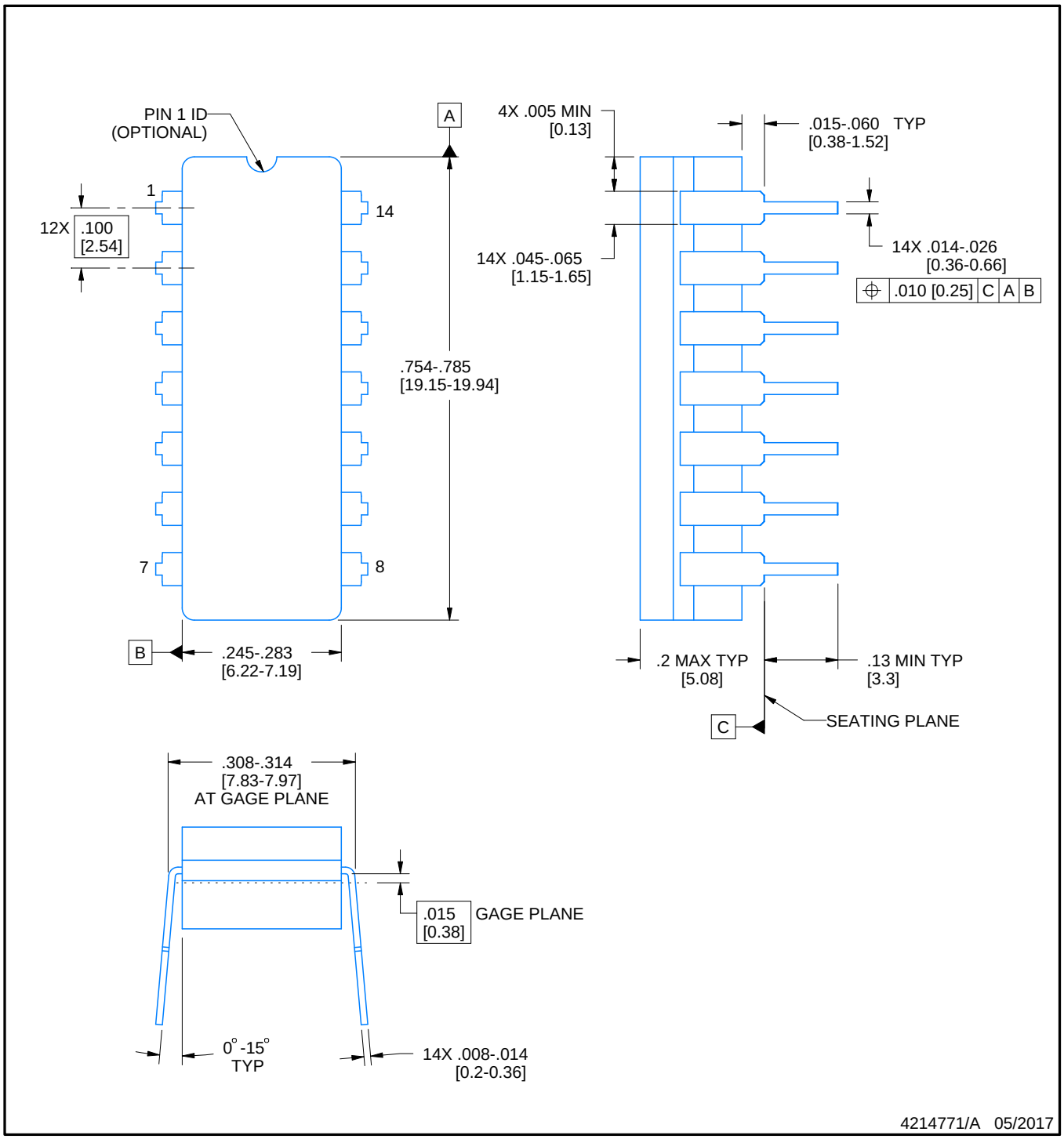


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

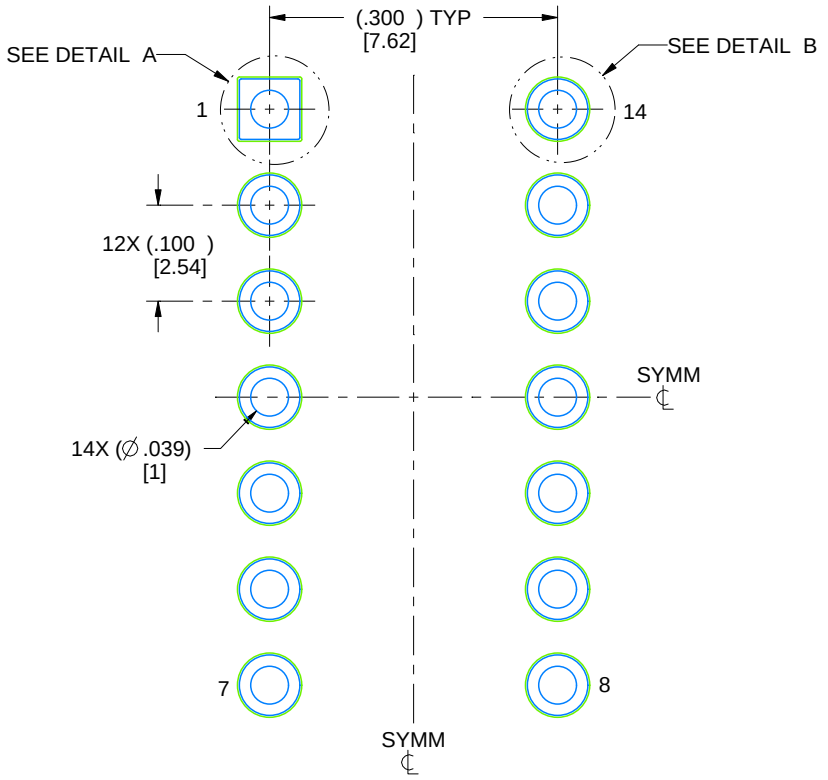
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

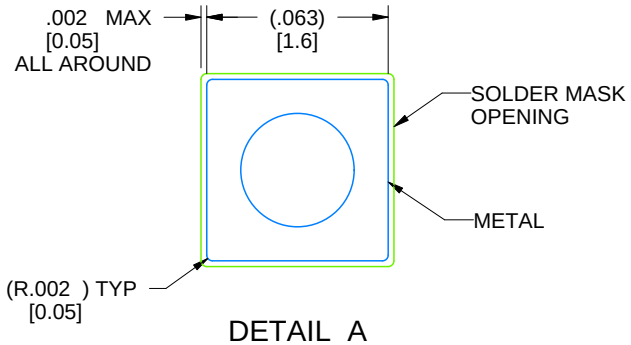
J0014A

CDIP - 5.08 mm max height

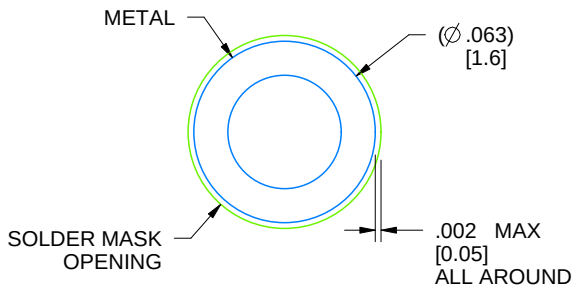
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

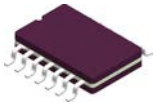


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

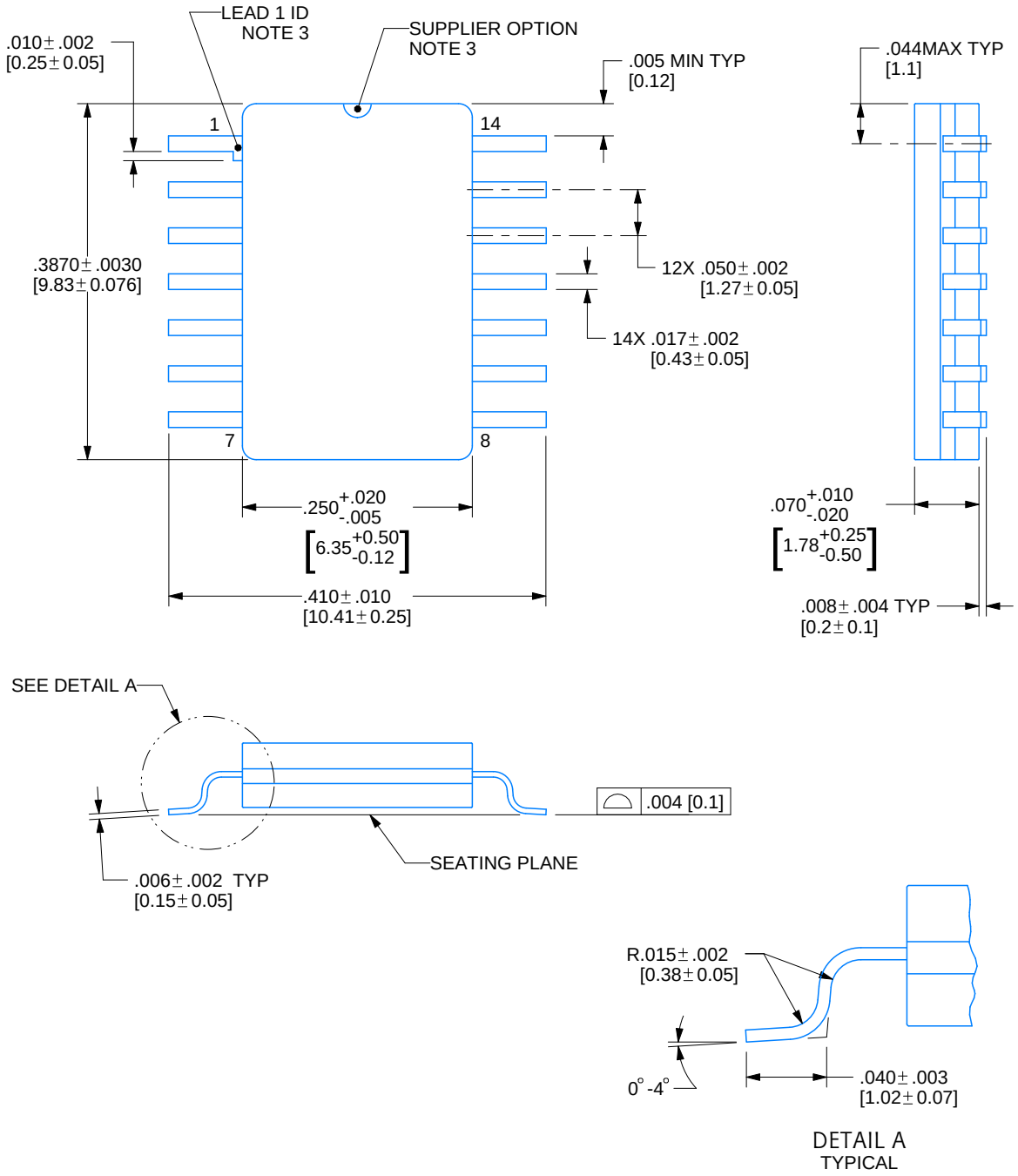


PACKAGE OUTLINE

NAC0014A

CERPACK

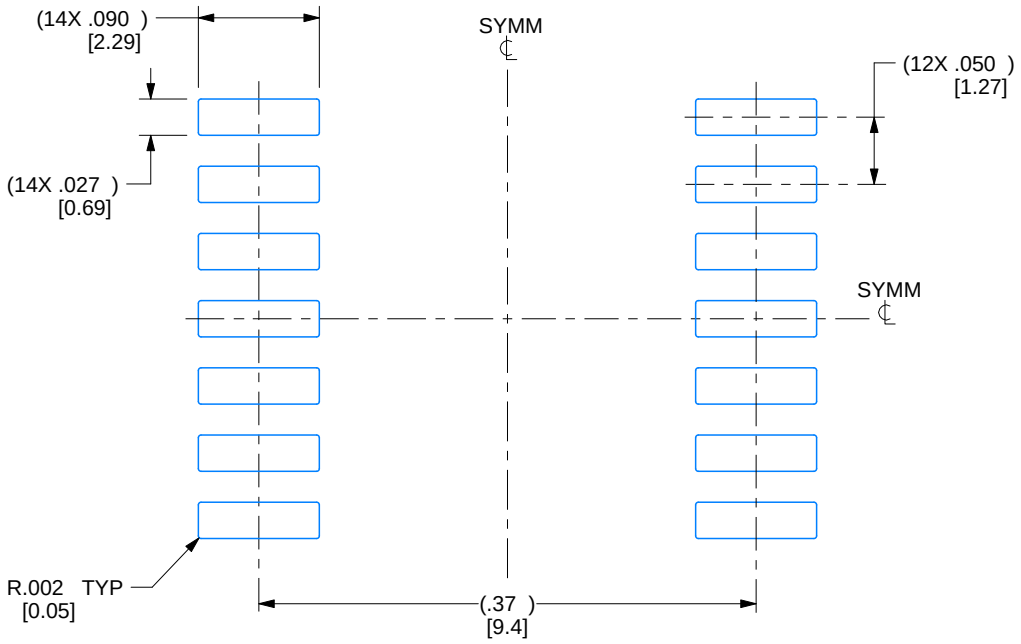
CERAMIC FLATPACK



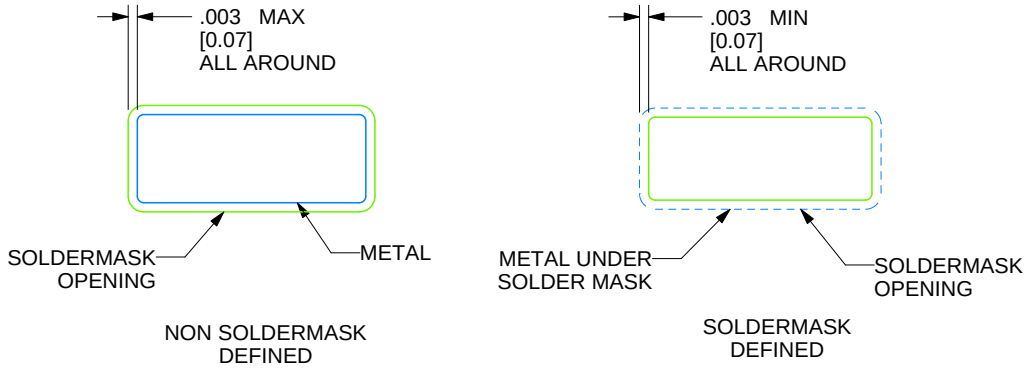
4215197/C 08/2022

NOTES:

1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021



RECOMMENDED LAND PATTERN

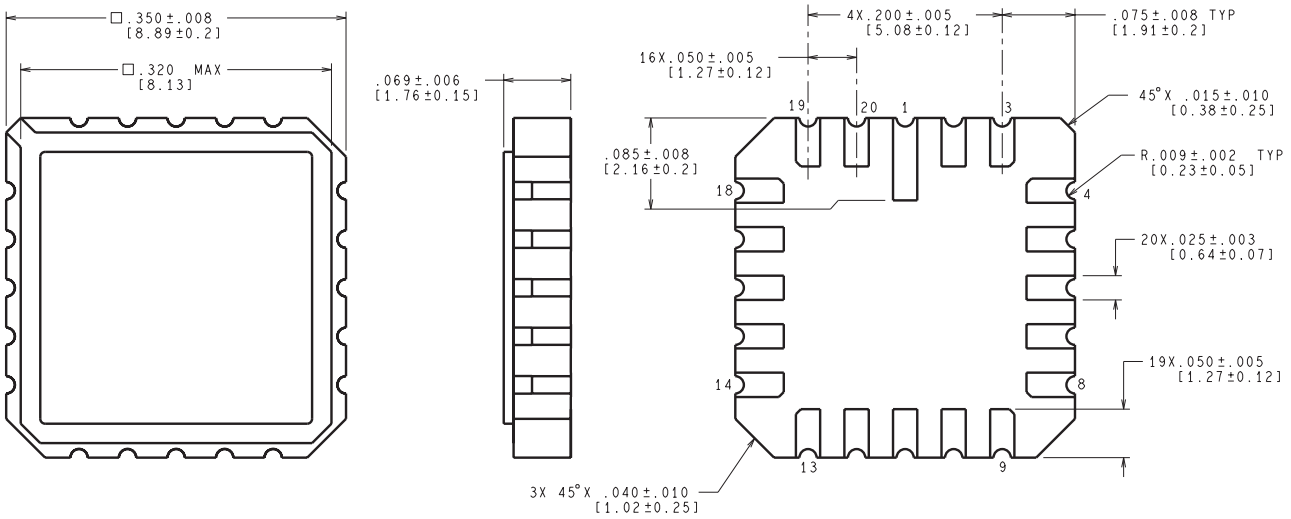


4215197/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197878	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198833	02/15/2022	K. SINCERBOX
C	.3870± .0030 WAS .39000± .00012;	2200916	08/08/2022	D. CHIN / K. SINCERBOX

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

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